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M 700 COMPUTERS
PART 2: CLASS 1

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REVISION NOTE

Issue 2 of this Standard has been prepared in order to update the technical content and prevent any misinterpretation of Page 1, Section 3.

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M700 COMPUTERS

PART 2: CLASS 1

This Defence Standard supersedes DEF STAN 00-21 (PART 2), Issue 1, dated 20th September 1982

1. This PART of the Defence Standard defines Class 1 of the M700 computer series. Class 1 computers meet the basic specification defined by PART 1 of the Defence Standard together with the more specific definition contained in this PART.

2. The terminology and definitions quoted in PART 1 of this Defence Standard shall normally apply throughout all parts of Defence Standard 00-21, except where more specific terms are defined.

3. The M700 Architecture is proprietary to Ferranti plc and is derived from their Argus* 700 computer series. Intellectual Property Rights in the M700 architecture are owned by Ferranti plc. Prior to designing and/or manufacturing a computer to the M700 specification, it is necessary to enter into a Licence Agreement with Ferranti plc unless all the M700 processors included in the said computer have been supplied by Ferranti plc or one of their existing licencees.

   It is the intention of the Ministry of Defence to fund such a licence, where it is required, in pursuance of a Ministry contract. Nominated licencees will also be required to agree to a suitable undertaking with respect to the Ministry. Further details are available from the Computing Policy and Standards Section of the Royal Signals and Radar Establishment, MoD(PE), Malvern.

   Users of M700 computers have free access to the information contained in this Defence Standard, subject to the provision of the Crown Copyright accorded.

4. This PART of the Defence Standard has been prepared by the RSRE Computing Policy and Standards Section in co-operation with Ferranti Computer Systems Limited. RSRE is the authority responsible for amending and updating this PART of the Defence Standard. The format differs from that used in Defence Standards prepared by the Directorate of Standardization.

5. RSRE is the authority responsible for evaluating all M700 implementations, whatever the manufacturer, that are supplied to the Ministry of Defence.

* Argus is a registered trademark of Ferranti plc

6. This Defence Standard has been agreed by all the authorities concerned. It is to be implemented, wherever practicable, in all designs, contracts, orders etc, commencing after its date of publication. If a difficulty arises which prevents application of the Defence Standard, the Directorate of Standardization shall be informed so that a remedy can be sought.

7. This PART of the Defence Standard has been devised for the use of the Crown and of its contractors in the execution of contracts for the Crown and, subject to the Unfair Contract Terms Act 1977, the Crown will not be liable in any way whatever (including but without limitation negligence on the part of the Crown its servants or agents) where the Defence Standard is used for other purposes.

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1. INTRODUCTION

This Class of M700 defines the basic 16-bit M700 processor.

2. GENERAL FEATURES

a) 16-bit word length

b) 64K/256K word address range for program and data

c) 2 word integer and 2 word floating point arithmetic

3. PROCESSOR ARCHITECTURE

3.1 PROCESSOR REGISTERS

As defined in PART 1.

3.2 PROCESSOR MODES

3.2.1 Arithmetic Modes

The following modes are implemented:

a) Word Mode

The normal arithmetic mode of Class 1 is word mode, ie 16-bit data and arithmetic.

b) Byte Mode

Byte mode is included.

c) 2 Word Integer Mode

Double length data is accessed and the processor performs 32-bit arithmetic.

d) 2 Word Floating Point Mode

The data is held as a 24-bit mantissa and an 8-bit exponent and the processor carries out 24-bit arithmetic.

3.2.2 Operating Modes

As defined in PART 1.

3.2.3 Interrupts

M700 Class 1 processors implement the following interrupt types:

a) Type A - 1 Interrupt

b) Type B - 4 Interrupts

c) Type C - 6 to 8 Interrupts

3.2.4 Environment Changing

As defined in PART 1.

3.3 ADDRESSING

As defined in PART 1.

3.4 STACKING

In Class 1 there is an arithmetic stack and a link stack as defined by PART 1.

3.5 INSTRUCTION SET

The instruction set for Class 1 computers is as defined in PART 1. The following extra instructions are also implemented for Class 1 computers.

1	2	3	4	5	6	7					
						5	4	3	2	1	0
PHO			15	026602	Maintain hardware operating lamp on - required at 100ms intervals						
SHO			15	026603	Clear Fail Staticiser and switch on hardware operating lamp						
CSO			15	026600	Switches off software operating lamp						
SSO			15	026601	Switches on software operating lamp						

NOTE: The format and abbreviations used in this table extract are similar to those defined in Appendix 1 of PART 1.

4. SYSTEM CONFIGURATIONS

4.1 Class 1 M700 processors have a capability of communicating with memory by a separate memory bus as well as the main input/output bus. This memory is either private to the processor (Fig 4.1.a) or it may be shared, using the Eurobus, between processors (Fig 4.1.b) or it may be a mixture of shared bus and Private Memory (Fig 4.1.c). Access to memory via the processor part is transparent to the instruction set and software.

Figure 4.1.a M700 with Private Memory

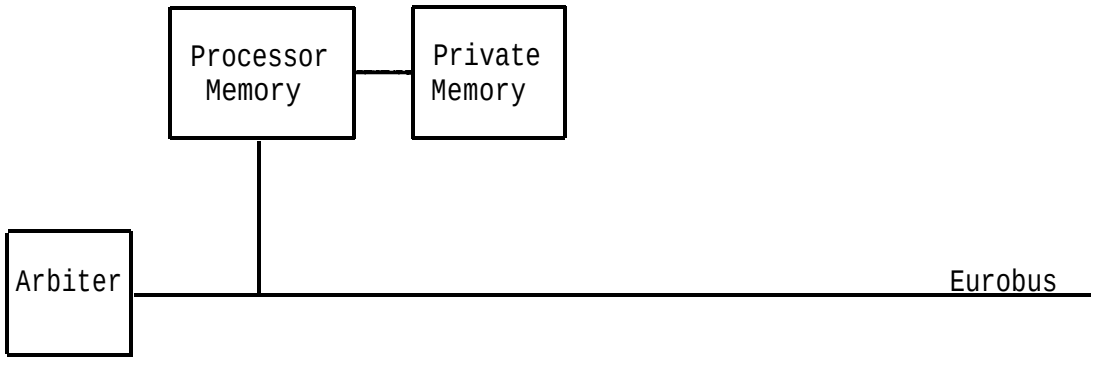


Figure 4.1.b M700 Processors with Shared Memory

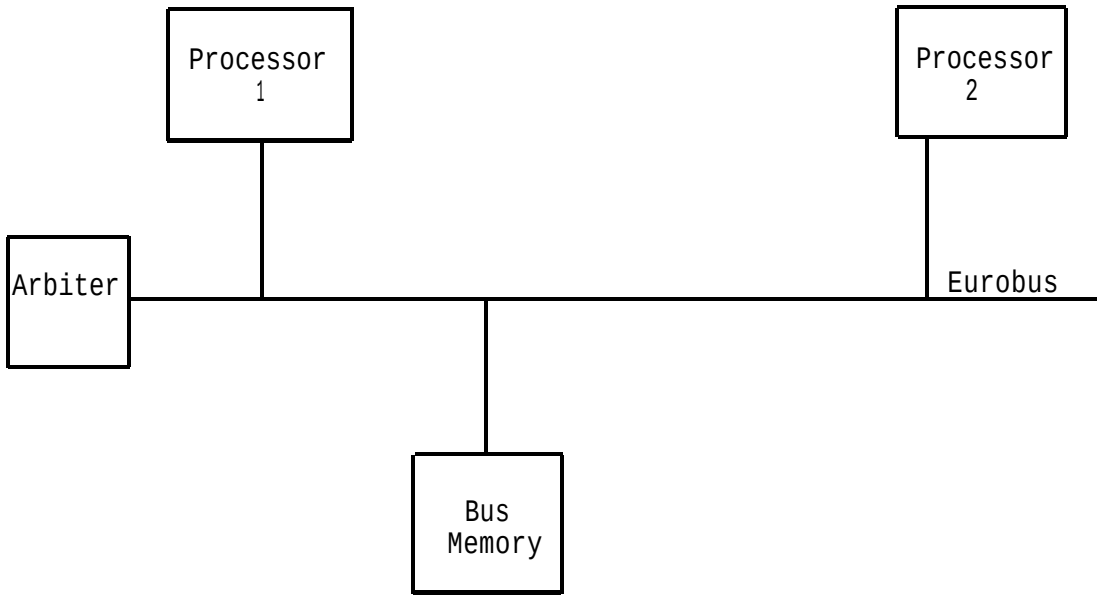
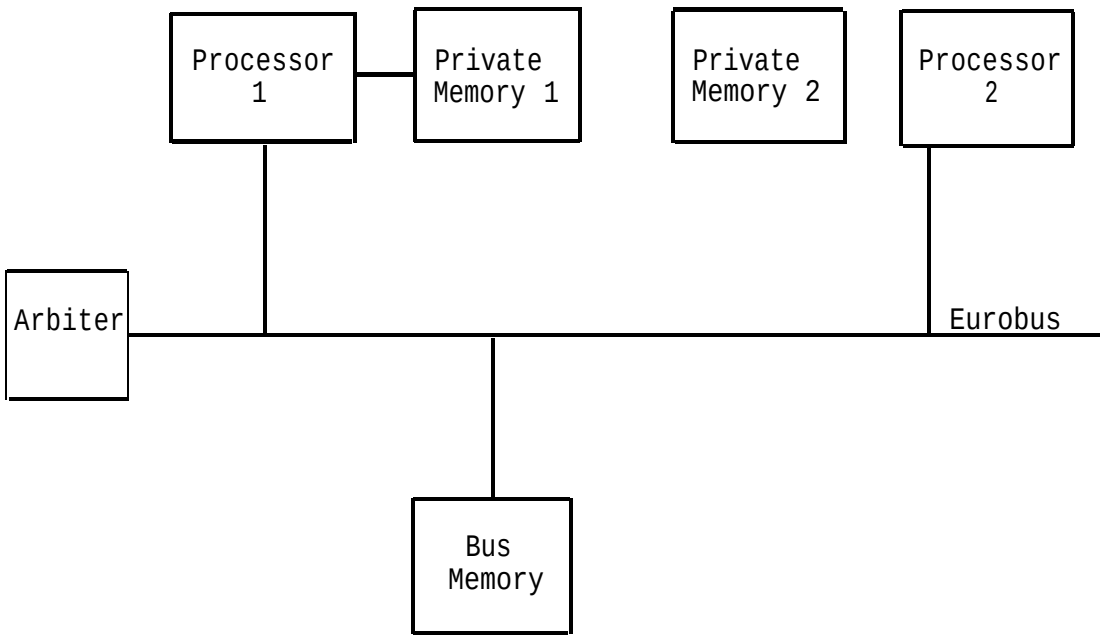


Figure 4.1.c M700 Processors with Private and Shared Memory



4.2 With the exception of the shared memory interface defined above, the monitor interface and any memory extension interface, all communications with main memory, peripherals and other processors is by the processor port to the input/output bus. The input/output bus is Eurobus 18A (DEF STAN 00-20).

5 INITIALISATION AND FILL

For Class 1 M700 processors, the following FILL modes are mandatory:

a) FILL mode 0 - Fount and Go

b) FILL Mode 1 - FILL via Paper Tape

c) FILL Mode 2 - FILL via V24 Interface

d) FILL Mode 3 - Slave FILL

e) FILL Mode 4 - Non Directive Paper Tape

FILL is implemented as a processor initialisation mode using built in control logic. Other 'special to system' FILLs are therefore possible.

6. FAILURE HANDLING

Class 1 M700 processors have facilities for detecting both hardware and software detected failures. The failure signals are available from the hardware such that they can be used to trigger visible indicators or else to link into the test facilities of the system configuration.

6.1 HARDWARE DETECTED FAILURES

6.1.1 Bus Interface Failure

The failure of a bus cycle initiated by the processor causes the arbiter to signal the failure to the processor, clearing the hardware operating staticiser. The processor resets as a result of a failure and enters a Type A interrupt, provided PSW bit 12 is set.

6.1.2 Invalid Instructions

If the processor encounters an instruction which is not included in the instruction set then that instruction is terminated and a Type A interrupt is entered, provided PSW bit 12 is set.

6.1.3 Pump Up Alarm

Class 1 M700 processors implement the Pump Up Alarm facility via the PHO instruction. The alarm signal is raised if the PHO instruction is not called every 100ms.

6.2 SOFTWARE DETECTED FAILURES

A software operating staticiser is included which is manipulated by the SSO and CSO instructions. This staticiser enables software detected errors to be recognised and signalled.

7. MONITORING

Monitoring facilities are provided to monitor operation of the processor and bus transfers. The following functions are included:

a) The suspension of the execution of a program.

b) Reading and writing of private or local memory.

c) Reading and writing of Eurobus memory.

d) Reading and writing to a Pseudo Address location.

e) Reading and writing to any processor register (including the PSW).

f) The initiation and/or continuation of a program

g) The execution of a program FILL mode.

Other ‘special to system’ monitoring functions are permitted.