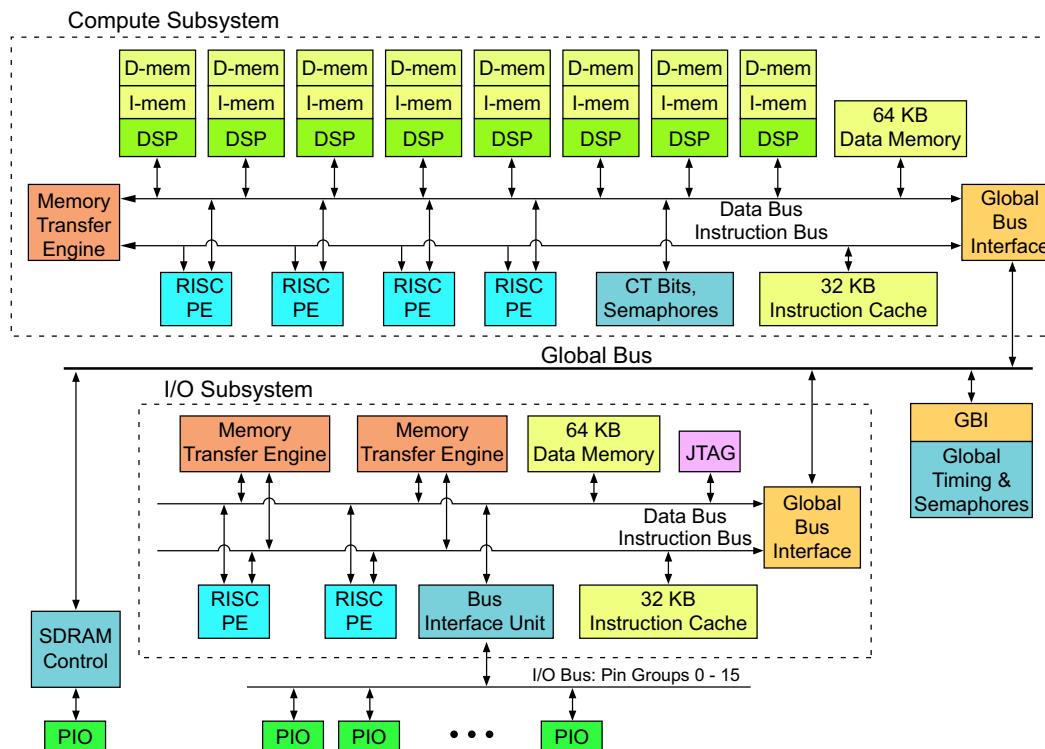


## FEATURES

- ◆ Scalable Loosely-Coupled Multiprocessor DSP Architecture
  - Eight 32-bit DSPs
  - Six 32-bit RISC-like CPUs
  - Three 32-bit Memory Transfer DMA-like CPUs
  - Three-level memory bus hierarchy
    - ▶ Dedicated local memory for each DSP
    - ▶ 192 KB shared on-chip memory
    - ▶ Dedicated 64-bit SDRAM 133-MHz interface
  - 1.25-Volt Core and 3.3-Volt I/O  $V_{dd}$
  - 230-MHz processor clock rate, 330-MHz clock rate for 32-bit global bus
  - Package choice: 420-pin BGA (35 x 35 mm) or 456-pin fine-pitch BGA (27 x 27 mm)
  - 0.15- $\mu$ m CMOS process
- ◆ High-Performance DSP Processors
  - RISC-like instruction set
  - SIMD instructions
  - Optimized DSP MAC with 128 8x8 bit multiplies/cycle or 32 16x16 bit multiplies/cycle
  - Sum of Absolute Differences (SAD) support
  - Fixed or floating-point DSP operation; fix/float conversion with no performance degradation

- ◆ Programmable I/O Subsystem
  - External interfaces defined by software
  - Two RISC-like CPUs with local memory and DMA
  - Software defined I/O—typical interfaces
    - ▶ 10/100 Ethernet MAC
    - ▶ 32-Bit, 33-MHz PCI
    - ▶ CCITT 601/656
    - ▶ Custom interfaces
- ◆ Multiprocessor Development Tools
  - C Language programming
    - ▶ ANSI C compiler/GNU libraries
    - ▶ Cradle C language for DSP timing optimization
    - ▶ eCOS RTOS
  - INSPECTOR™ design and debug console
    - ▶ Single step, set breakpoints
    - ▶ Cycle accurate simulator
  - RDS3400 hardware development platform
- ◆ Example Applications
  - Video Surveillance Systems
    - ▶ Video over IP gateways/servers
    - ▶ Video Cameras
    - ▶ Digital Video Recorders
  - IP Video Conferencing Equipment
  - IP Video Phones



**Figure 1. Functional Block Diagram**

## Multiprocessor DSP

The CT3400 is a new, high-performance, multiprocessor DSP designed for video, image, and audio processing applications. The device's DSP engines are capable of delivering up to 29.5 billion multiply-accumulate (MAC) operations per second on 8-bit data, running at a clock speed of 230 MHz. At the same time, the device's RISC engines provide overall system control, provide additional computing capability and control applications running on the DSP engines.

The single-chip CT3400 processor consists of a Compute Subsystem, an I/O Subsystem, an SDRAM Controller, a Global Timing Unit and a set of programmable I/O peripherals as shown in Figure 1. The architecture of the device is a loosely coupled, multiprocessor DSP with multi-tiered buses, multi-tiered memory and data prefetching capability that can easily be scaled from a small to a large number of DSP and RISC processors.

The device can run a Real Time Operating System (RTOS) on any one of the RISC devices configured as an on-chip host processor. Applications can be written in the C language and the Cradle C Language for DSP Timing Optimization for both ease of programming and assembly code-like performance.

## Compute Subsystem

The Compute Subsystem of the CT3400 contains eight independent DSP engines (DSP) with Single Instruction Multiple Data (SIMD) instructions and 4 independent RISC general-purpose processing engines (PE). The DSP engines have an instruction set that supports the math intensive and multi-dimensional operations found in digital signal processing, such as, voice, video, and multimedia applications. The PE cores support efficient, RISC, load and store operations and handle the serial and irregular code found in control and data driven tasks. These DSP and PE computing resources can work independently or in parallel and can also work in tightly coupled groupings under the control of specified PEs.

The DSP engines and PE cores are supported by a memory transfer engine (MTE) with four Memory Transfer Controllers (MTC) for data movement, 32 KB of instruction cache, 64 KB of local data memory, and 64-bit instruction and data buses. The Compute Subsystem has a global bus interface to connect to the global bus of the CT3400 device. This combination of RISC processor and DSP processor capability makes the CT3400 a cost-effective, high-performance platform for embedded systems and customer premises equipment and appliances.

### DSP Engine

The eight DSP engines in the Compute Subsystem are identical digital signal processing engines that operate independently and concurrently. Each DSP engine contains a Single Instruction Multiple Data, Arithmetic Logic Unit (SIMD ALU), a Packed Integer Multiplier Accumulator (PIMAC), a Floating Point Unit (FPU), bi-directional FIFO data buffers and DMA channels, a 128 x 32 register and a 512 x 20 program memory as shown in Figure 2.

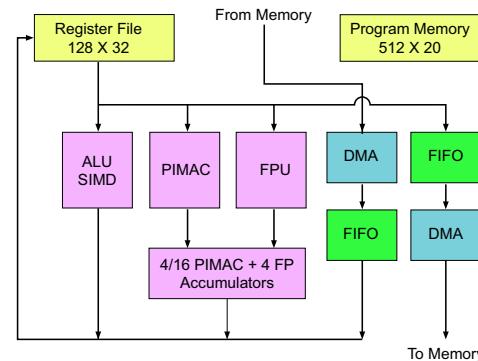


Figure 2. CT3400 DSP Engine Block Diagram

### ALU

The integer SIMD ALU executes 32-bit integer arithmetic operations and logic, field access and flow control operations, as well as 32-bit load and store operations. It has a 32-bit adder and shifter with support for 8, 16, or 32-bit Single Instruction Multiple Data (SIMD) operations. This allows the ALU to perform the same base operation on 8-bit or 16-bit packed data in the 32-bit registers. For instance, an 8-bit, partitioned, subtraction operation can perform four subtractions, each on a byte partition.

### PIMAC (Packed Integer MAC)

The PIMAC unit supports 8, 16, or 32-bit multiply-accumulate operations (MACs) with the capability of sixteen 8-bit MACs, four 16-bit MACs, or a 32-bit MAC operation per cycle. This capability can be very powerful when implementing signal processing tasks like FIR filters, convolutions and similar functions.

### SIMD ALU and PIMAC Parallelism

In addition to parallel DSP engines, the CT3400 provides further parallelism through SIMD instruction parallelism within each individual DSP engine. The general SIMD instruction operation in the DSP engines is shown in Figure 3.

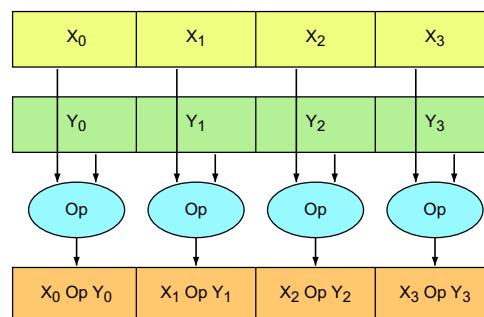


Figure 3. SIMD Instruction Operations

For a given instruction operation within a single DSP engine, four sets of 8-bit packed (32 bits) data operands can be processed in parallel with the four, packed, eight-bit results being returned to a single 32-bit register. This parallelism is particularly useful in video and image processing applications where the same computation must be performed on a stream of closely related pixels, in space or in time, or in both. For instance, the Sum of Absolute Difference (SAD) instruction can be used in intra-prediction of pixels within a block and inter-prediction motion estimation between blocks in successive frames.

The PIMAC, in a fashion similar to the SIMD ALU, can perform sixteen 8-bit multiplies in parallel on packed 8-bit data. Therefore, the CT3400 can perform 29.5 GMAC per second on 8-bit partitioned data running on all eight DSP engines concurrently at a clock frequency of 230 MHz.

## FPU

The FPU has a 24-bit multiplier, four floating-point registers and a floating-point ALU. It supports floating-point arithmetic operations, including multiply-accumulate (MAC) operations. The CT3400 processor can perform 1.8 billion floating-point MAC's per second on floating point data running on all eight DSP engines concurrently at a clock frequency of 230 MHz.

## General-Purpose Processing Engine (PE)

The four PE cores in the Compute Subsystem are identical, 32-bit RISC-like processing engines with interrupts. Each PE contains a 32-bit ALU, a 32-bit integer multiplier, single precision floating point logic and 32 general-purpose registers and 32 special-purpose registers. The PEs use a Harvard architecture, with separate data and instruction memories.

The instruction set includes both fixed-point and floating-point operations, and accommodates 8, 16, or 32-bit data formats. The PEs have instructions for the manipulation of bit string data to accelerate operations such as entropy coding. The PE cores also provide set-up, management and control for the DSP engines and the MTE engine, based on configuration assignments established by the programmer.

In addition to the four PE cores in the Compute Subsystem, two more PE cores in the I/O Subsystem perform data preprocessing and I/O management and control functions.

## Memory Transfer Engine

The Memory Transfer Engine (MTE) is a data transfer engine independent of the eight DSP and four PE processing engines. The MTE is a multi-threaded processor with four

Memory Transfer Controllers (MTC). Each MTC has its own program counter, its own group of 16 data registers, its own group of 16 hardware registers, and its own memory read and write FIFOs. The MTCs can perform data ordering, as well as data transfer functions under program control, to optimize the performance of data intensive applications such as video and image processing.

Each MTC performs a single task, such as transferring one Global Bus block of data (8, 16, or 32 bytes), then relinquishes control to the next MTC in a round robin fashion. The MTE communicates with the local data memory and the global bus through its 32-byte deep, Read and Write FIFOs. One MTE in the Compute Subsystem manages data movement for the DSP and PE cores and two more MTEs in the I/O Subsystem manage data for input and output ports and external memory. Each MTE can transfer data in the background, independent of the operation of the PEs or DSPs.

## I/O Subsystem

The I/O Subsystem consists of two PE engines, two MTE engines, 64 KB of local data memory, 32 KB of instruction cache, a boot ROM, a JTAG interface, a global bus interface, and a bus interface unit (BIU) to programmable I/O. The I/O Subsystem supports processor initialization from the boot ROM and program loading through a serial or parallel I/O port typically connected to adjacent Flash memory. In operation, the I/O Subsystem supports memory mapped I/O devices, and data transfers internally and externally.

The I/O Subsystem communicates with pin groups through the BIU connected to a 32-bit pipelined I/O bus. At 230 MHz, the pipelined bus has a peak transfer rate of 920 Mbytes/second. The CT3400 provides a programmable I/O interface to various buses and I/O devices, such as USB, Ethernet, PCI interfaces, I<sup>2</sup>C, RS-232 serial ports, video and audio interfaces and others.

The programmable I/O system has sixteen pin groups and each group has eight I/O pins. The processor accommodates the wide variety of potential interfaces by using a combination of configurable I/O pins, firmware programmable state machines and software to provide the functions of designated I/O device interfaces. Since the definition and function of each I/O device interface is defined by firmware, the Programmable I/O system is completely flexible and the functions of each I/O device can be modified or upgraded by changing its I/O firmware.

## GENERAL CHARACTERISTICS

### Typical Operating Conditions

Specification	Value	Units	Comment
Configurable I/O	128	Pins	Eight pins per pin group
Quad Clock Frequency	230	MHz	
Global Bus Frequency	330	MHz	
SDRAM Frequency	133	MHz	

### Absolute Maximum Ratings (Commercial Temperature Range)

Specification	Value
Voltage Range on any pin relative to ground	-1.0V to +5.5V
Operating Case Temperature Range	0°C to +90°C
Maximum Junction Temperature	105°C
Storage Temperature Range	-55°C to +150°C

## ELECTRICAL SPECIFICATIONS

### AC and DC Electrical Characteristics

Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
$V_{ddc}$	Core supply voltage		1.20	1.25	1.30	V
$V_{ddio}$	I/O supply voltage		3.0	3.3	3.6	V
$V_{oh}$	Output HIGH voltage	$I_{oh} = 20 \text{ mA}$	2.4			V
$V_{ol}$	Output low voltage	$I_{ol} = 20 \text{ mA}$			0.4	V
$V_{ih}$	Input HIGH voltage		2.0			V
$V_{il}$	Input low voltage				0.8	V
$I_{in}$	Input leakage current	$V_i = 3.3\text{V or } 0\text{V}$			+10	$\mu\text{A}$
$I_{oz}$	Output leakage current	$V_i = 3.3\text{V or } 0\text{V}$			-10	$\mu\text{A}$
$I_{cc}$	Core supply current, dynamic	230 MHz, 1.25V		TBD		A
$I_{cc1}$	Core supply current, standby	1.25V, no clock		400		$\text{mA}$
$I_{ccio}$	I/O supply current	3.3V, 32/33 MHz PCI, 133 MHz SDRAM		150		$\text{mA}$
$C_{in}$	Input capacitance				5	$\text{pF}$
$C_{out}$	Output capacitance				5	$\text{pF}$

This device supports four  $I_{oh}/I_{ol}$  drive strengths for SDRAM and I/O interfaces which are programmable. This table details the voltage characteristics for each of the drive strengths and each of the interfaces. The level of drive strength for each external I/O or SDRAM pin group is chosen via a programmable Sdram INput Sample (SINS) clock register.

### Drive Strengths (Typical)

Pins	Symbol	Test Conditions	Strength 1	Strength 2	Strength 3	Strength 4
SDRAM Clock	$I_{ol}$ [mA]	$V_{ol} = 0.4V$	11	20	28	35
	$I_{oh}$ [mA]	$V_{oh} = 2.7V$	6	12	22	28
SDRAM Data Control	$I_{ol}$ [mA]	$V_{ol} = 0.4V$	3	5	10	19
	$I_{oh}$ [mA]	$V_{oh} = 2.7V$	6	12	22	28
Programmable I/O (PIO)	$I_{ol}$ [mA]	$V_{ol} = 0.4V$	5	8	13	19
	$I_{oh}$ [mA]	$V_{oh} = 2.7V$	3	6	12	20

### External Clock Oscillator Characteristics (clk0, clk1)

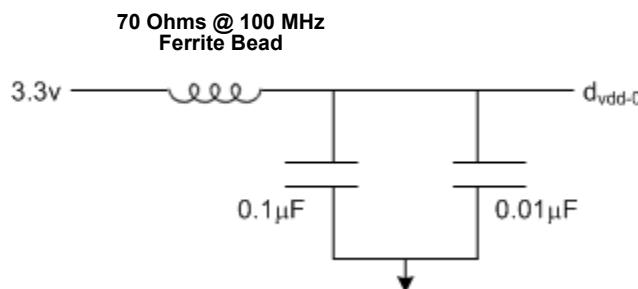
Parameter	Symbol	Min	Typ	Max	Unit
Clock frequency	$F_{clk}$	5	10	30	MHz
Duty cycle		45%	50%	55%	Clock Oscillator Period
Transition time		1	6	10	ns
Frequency stability				$\pm 25$ ppm	

### Notes

1. External Chip Reset: The RESET signal (rst\_n) should be held active low for a minimum of 20 external clock cycles after power is stable to ensure proper operation of the chip.
2. Input to clock pin is 5V tolerant TTL.
3. Transition time: Measured 0.1V<sub>dd</sub> to 0.9V<sub>dd</sub> with load of 15 pF.

### Clock PLL Circuitry

The following circuitry is required for both clock PLL inputs ( $d_{vdd-0}$ ,  $d_{vdd-1}$ ) to remove noise that would otherwise disrupt the clocking circuitry. Each pin needs its own external circuitry.



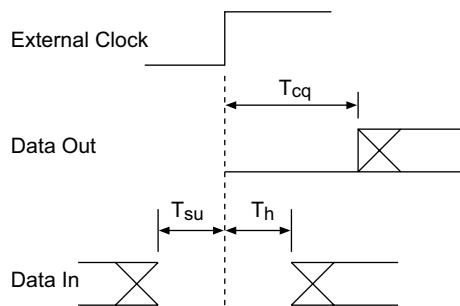
The preferred power-on sequence is to power up the core 1.25V supply and the I/O 3.3V supply at the same time. If this is not possible, power up the core 1.25V and the I/O 3.3V supply within 100ms of each other in any order. The power-down sequence is the reverse of the power-up sequence.

# TIMING AND WAVEFORM DIAGRAMS

All external clock pins (`ext_io_clk[0:5]`) have DLLs for synchronizing external clock sources with the data pins. The following table describes timing when DLL is in and out of circuit.

## Programmable I/O Pins Timing and Waveforms

Pin Type	Symbol	With DLL	Without DLL	Unit	Comments
Data Out (max)	$T_{cq}$	7	17	ns	30pF load
Data in Set Up (min)	$T_{su}$	2	2	ns	30pF load
Data in Hold (min)	$T_h$	2	12	ns	30pF load



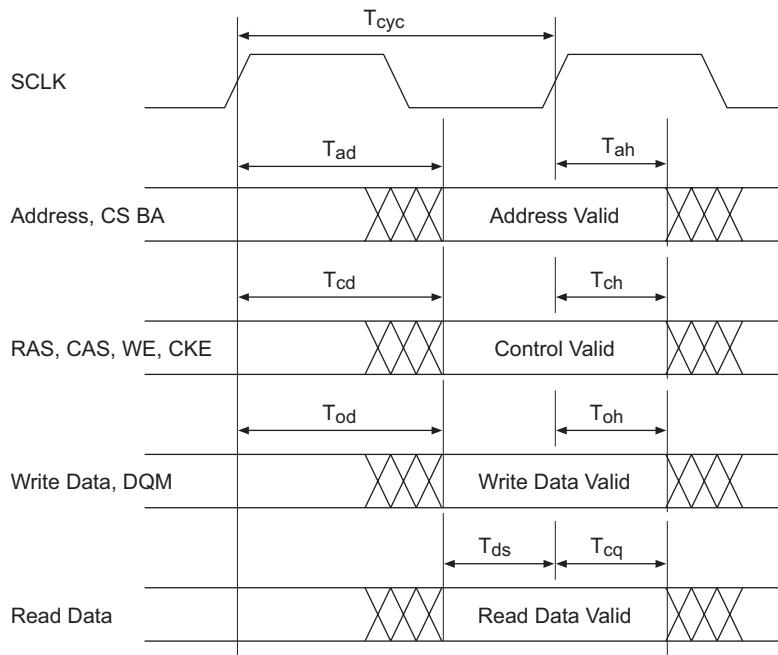
## SDRAM Controller Timing and Waveforms

Pin Type	Parameter	Symbol	Min	Max	Units	Notes
SCLK Clock (sd_clk[0:3])	Frequency	$F_{\text{sclk}}$	33	133	MHz	
	Period	$T_{\text{cyc}}$	7.5	30	ns	2
Address, CS, BA, from CRA to DRAM	Output delay	$T_{\text{ad}}$	$(T_{\text{cyc}}/2)-1$	$(T_{\text{cyc}}/2)+1$	ns	3
	Hold	$T_{\text{ah}}$	$(T_{\text{cyc}}/2)-2$		ns	3
RAS, CAS, WE, CKE from CRA to SDRAM	Output delay	$T_{\text{cd}}$	$(T_{\text{cyc}}/2)-1$	$(T_{\text{cyc}}/2)+1$	ns	3
	Hold	$T_{\text{ch}}$	$(T_{\text{cyc}}/2)-2$		ns	3
Write Data, DQM from CRA to SDRAM	Output delay	$T_{\text{od}}$	$(T_{\text{cyc}}/2)-1$	$(T_{\text{cyc}}/2)+1$	ns	3
	Hold	$T_{\text{oh}}$	$(T_{\text{cyc}}/2)-2$		ns	3
Read Data from SDRAM to CRA	Setup	$T_{\text{ds}}$	TBD	TBD	ns	4
	Hold	$T_{\text{dh}}$	TBD		ns	4

## Notes

1. Timing measurements were made at  $0.5V_{dd}$ , 30pF with 2 ns input rise and fall times.
  2. SCLK  $T_{cyc}$  is produced by programming the SDRAM clock generator registers “SPER, SMID, SEND” in the Global Functions block, and is output to the SDRAM.
  3. Write output delay/hold times are output from CRA with respect to the SCLK, and are dependent on the programming of the SDRAM clock generator register “SOUT.”
  4. Read output delay/hold times are input to CRA with respect to SCLK and are dependent on the programming of the SDRAM clock generator register “SINS.”

## SDRAM Controller Timing and Waveforms



## SIGNAL PIN DESCRIPTIONS

### System Signals

There are the following 16 pins for system clock, reset and test signals.

### Clock/Reset/Test Pins (BG420 and FG456)

Pin Name	I/O	BG420 Pin #	FG456 Pin #	Pin Name	I/O	BG420 Pin #	FG456 Pin #
rst_n	I	M4	M25	ext_io_clk_3	I/O	K1	K25
clk0	I	L3	L25	ext_io_clk_4	I/O	L5	K26
clk1	I	L2	L26	ext_io_clk_5	I/O	L4	L24
clk_bypass	I	M5	M24	jtag_tdo	O	N3	P26
ext_gwi	I	M3	M26	jtag_tdi	I	N4	N26
ext_io_clk_0	I/O	J1	J24	jtag_tck	I	M2	N25
ext_io_clk_1	I/O	K3	J25	jtag_tms	I	M1	N24
ext_io_clk_2	I/O	K2	K24	jtag_trst	I	N2	P25

## External SDRAM

The following 100 signals are for external SDRAM or PIO.

### SDRAM Controller Pins (BG420 and FG456)

Pin Name	I/O	BG420 Pin #	FG456 Pin #	Pin Name	I/O	BG420 Pin #	FG456 Pin #
sd_a_0	O	C18	A6	sd_d_21	I/O	D11	B16
sd_a_1	O	B18	A7	sd_d_22	I/O	A10	C16
sd_a_2	O	E17	B8	sd_d_23	I/O	B10	A17
sd_a_3	O	D17	C9	sd_d_24	I/O	D8	C19
sd_a_4	O	C17	A8	sd_d_25	I/O	E8	B20
sd_a_5	O	B17	B9	sd_d_26	I/O	A7	A21
sd_a_6	O	A17	C10	sd_d_27	I/O	B7	A22
sd_a_7	O	C16	A9	sd_d_28	I/O	C7	B21
sd_a_8	O	B16	B10	sd_d_29	I/O	D7	C20
sd_a_9	O	A16	C11	sd_d_30	I/O	A6	A23
sd_a_10	O	E15	A10	sd_d_31	I/O	B6	B22
sd_a_11	O	D15	B11	sd_dqm_0	O	E20	D4
sd_a_12	O	C15	A11	sd_dqm_1	O	B22	C4
sd_a_13	O	B15	C12	sd_dqm_2	O	A22	B3
sd_ba_0	O	A15	B12	sd_dqm_3	O	B21	C5
sd_ba_1	O	A14	A12	sd_dqm_4	O	A21	B4
sd_cs0	O	B19	C8	sd_dqm_5	O	E19	A3
sd_cs1	O	A19	B7	sd_dqm_6	O	D20	C6
sd_d_0	I/O	N24	N1	sd_dqm_7	O	C20	B5
sd_d_1	I/O	N25	N3	sd_ras_n	O	D19	B6
sd_d_2	I/O	N26	N4	sd_cas_n	O	C19	A5
sd_d_3	I/O	M26	N2	sd_cke	O	B20	A4
sd_d_4	I/O	M25	M1	sd_fb_clk_out	O	B12	C14
sd_d_5	I/O	M24	M2	sd_fb_clk_in	I	C12	D14
sd_d_6	I/O	M22	M3	sd_clk_0	O	B14	C13
sd_d_7	I/O	M23	L1	sd_clk_1	O	B13	B13
sd_d_8	I/O	J25	J3	sd_clk_2	O	C13	A13
sd_d_9	I/O	J24	H2	sd_clk_3	O	A12	B14
sd_d_10	I/O	J23	G1	sd_we_n	O	A20	C7
sd_d_11	I/O	J22	H3	sd_d_32	I/O	L25	L2
sd_d_12	I/O	H26	G2	sd_d_33	I/O	L24	L3
sd_d_13	I/O	H25	F1	sd_d_34	I/O	L23	K1
sd_d_14	I/O	H24	E1	sd_d_35	I/O	L22	K2
sd_d_15	I/O	G25	F2	sd_d_36	I/O	K26	J1
sd_d_16	I/O	D12	A14	sd_d_37	I/O	K25	K3
sd_d_17	I/O	E12	A15	sd_d_38	I/O	K24	J2
sd_d_18	I/O	A11	B15	sd_d_39	I/O	J26	H1
sd_d_19	I/O	B11	C15	sd_d_40	I/O	G24	G3
sd_d_20	I/O	C11	A16	sd_d_41	I/O	G23	D1

**SDRAM Controller Pins (BG420 and FG456) (Continued)**

Pin Name	I/O	BG420 Pin #	FG456 Pin #	Pin Name	I/O	BG420 Pin #	FG456 Pin #
sd_d_42	I/O	F26	E2	sd_d_53	I/O	C9	C18
sd_d_43	I/O	F25	F3	sd_d_54	I/O	B8	B19
sd_d_44	I/O	G22	D2	sd_d_55	I/O	C8	A20
sd_d_45	I/O	E26	E3	sd_d_56	I/O	E7	C21
sd_d_46	I/O	E25	C2	sd_d_57	I/O	A5	A24
sd_d_47	I/O	D25	D3	sd_d_58	I/O	B5	B23
sd_d_48	I/O	C10	B17	sd_d_59	I/O	A4	C22
sd_d_49	I/O	D10	A18	sd_d_60	I/O	E2	A25
sd_d_50	I/O	E10	C17	sd_d_61	I/O	F2	B25
sd_d_51	I/O	A9	B18	sd_d_62	I/O	F1	A26
sd_d_52	I/O	B9	A19	sd_d_63	I/O	G5	B26

**Notes**

1. These pins are all bidirectional. There are two operating modes: sdram and pio. The directionality shown above is for sdram mode. On power-up, they are configured in pio mode as inputs. They are then under software control (via the Direction register).
2. All unconnected SDRAM Controller I/O pins should be pulled up to  $V_{ddio}$  with a 10K-ohm resistor.

## Programmable Input/Output

The following 128 signals are for programmable input/output.

### Programmable I/O Pins (BG420 and FG456)

Pin Name	I/O	BG420 Pin #	FG456 Pin #	Pin Name	I/O	BG420 Pin #	FG456 Pin #
p0_0_0	I/O	N1	P24	p0_5_0	I/O	AE7	AE21
p0_0_1	I/O	P3	R26	p0_5_1	I/O	AF7	AF22
p0_0_2	I/O	P2	R25	p0_5_2	I/O	AB8	AF21
p0_0_3	I/O	P1	R24	p0_5_3	I/O	AC8	AE20
p0_0_4	I/O	R2	T26	p0_5_4	I/O	AD8	AD19
p0_0_5	I/O	R3	T25	p0_5_5	I/O	AE8	AF20
p0_0_6	I/O	R4	U26	p0_5_6	I/O	AD9	AE19
p0_0_7	I/O	R5	T24	p0_5_7	I/O	AE9	AD18
p0_1_0	I/O	T1	U25	p0_6_0	I/O	AF9	AF19
p0_1_1	I/O	T2	V26	p0_6_1	I/O	AB10	AE18
p0_1_2	I/O	T3	U24	p0_6_2	I/O	AC10	AD17
p0_1_3	I/O	T4	V25	p0_6_3	I/O	AD10	AF18
p0_1_4	I/O	U1	W26	p0_6_4	I/O	AE10	AE17
p0_1_5	I/O	U2	V24	p0_6_5	I/O	AF10	AF17
p0_1_6	I/O	U3	W25	p0_6_6	I/O	AC11	AD16
p0_1_7	I/O	U4	Y26	p0_6_7	I/O	AD11	AE16
p0_2_0	I/O	U5	AA26	p0_7_0	I/O	AE11	AF16
p0_2_1	I/O	V1	W24	p0_7_1	I/O	AF11	AD15
p0_2_2	I/O	V2	V23	p0_7_2	I/O	AB12	AE15
p0_2_3	I/O	V3	Y25	p0_7_3	I/O	AC12	AF15
p0_2_4	I/O	W2	AB26	p0_7_4	I/O	AD12	AD14
p0_2_5	I/O	W3	AA25	p0_7_5	I/O	AE12	AC14
p0_2_6	I/O	W4	Y24	p0_7_6	I/O	AF12	AE14
p0_2_7	I/O	W5	AC26	p0_7_7	I/O	AE13	AF14
p0_3_0	I/O	Y1	AB25	p0_8_0	I/O	AD13	AF13
p0_3_1	I/O	Y2	AA24	p0_8_1	I/O	AE14	AE13
p0_3_2	I/O	Y3	AD26	p0_8_2	I/O	AF14	AD13
p0_3_3	I/O	Y4	AC25	p0_8_3	I/O	AF15	AF12
p0_3_4	I/O	Y5	AB24	p0_8_4	I/O	AE15	AE12
p0_3_5	I/O	AA1	AE26	p0_8_5	I/O	AD15	AD12
p0_3_6	I/O	AA2	AF26	p0_8_6	I/O	AC15	AF11
p0_3_7	I/O	AB2	AE25	p0_8_7	I/O	AB15	AE11
p0_4_0	I/O	AE5	AF25	p0_9_0	I/O	AF16	AD11
p0_4_1	I/O	AF4	AD22	p0_9_1	I/O	AE16	AF10
p0_4_2	I/O	AB7	AE23	p0_9_2	I/O	AD16	AE10
p0_4_3	I/O	AF5	AF24	p0_9_3	I/O	AF17	AF9
p0_4_4	I/O	AE6	AD21	p0_9_4	I/O	AE17	AD10
p0_4_5	I/O	AF6	AE22	p0_9_5	I/O	AD17	AE9
p0_4_6	I/O	AC7	AF23	p0_9_6	I/O	AC17	AF8
p0_4_7	I/O	AD7	AD20	p0_9_7	I/O	AB17	AD9

**Programmable I/O Pins (BG420 and FG456) (Continued)**

Pin Name	I/O	BG420 Pin #	FG456 Pin #	Pin Name	I/O	BG420 Pin #	FG456 Pin #
p0_10_0	I/O	AE18	AE8	p0_13_0	I/O	Y25	Y3
p0_10_1	I/O	AD18	AF7	p0_13_1	I/O	Y26	AA2
p0_10_2	I/O	AF19	AF6	p0_13_2	I/O	W22	AB1
p0_10_3	I/O	AE19	AD8	p0_13_3	I/O	W23	W3
p0_10_4	I/O	AD19	AE7	p0_13_4	I/O	W24	Y2
p0_10_5	I/O	AC19	AF5	p0_13_5	I/O	W25	AA1
p0_10_6	I/O	AF20	AE6	p0_13_6	I/O	V24	Y1
p0_10_7	I/O	AE20	AD7	p0_13_7	I/O	V25	W2
p0_11_0	I/O	AD20	AF4	p0_14_0	I/O	V26	V3
p0_11_1	I/O	AB19	AE5	p0_14_1	I/O	U22	W1
p0_11_2	I/O	AC20	AD6	p0_14_2	I/O	U23	V2
p0_11_3	I/O	AF21	AF3	p0_14_3	I/O	U24	U3
p0_11_4	I/O	AE21	AE4	p0_14_4	I/O	U25	V1
p0_11_5	I/O	AF22	AF2	p0_14_5	I/O	U26	U2
p0_11_6	I/O	AB20	AD5	p0_14_6	I/O	T23	T3
p0_11_7	I/O	AE22	AE2	p0_14_7	I/O	T24	U1
p0_12_0	I/O	AC25	AF1	p0_15_0	I/O	T25	T2
p0_12_1	I/O	AB25	AB3	p0_15_1	I/O	T26	T1
p0_12_2	I/O	Y22	AE1	p0_15_2	I/O	R22	R3
p0_12_3	I/O	AB26	AC2	p0_15_3	I/O	R23	R2
p0_12_4	I/O	AA25	AD1	p0_15_4	I/O	R24	R1
p0_12_5	I/O	AA26	AA3	p0_15_5	I/O	R25	P3
p0_12_6	I/O	Y23	AB2	p0_15_6	I/O	P26	P2
p0_12_7	I/O	Y24	AC1	p0_15_7	I/O	P25	P1

**Note**

1. All unconnected Programmable I/O pins should be pulled up to  $V_{ddio}$  with a 10K-ohm resistor.

## POWER AND GROUND PINS

### V<sub>dd</sub> For Input/Output

The following 38 pins for the BG420 package and 42 pins for the FG456 package are all +3.3 Volts for V<sub>ddio</sub>.

### 3.3V Power Pins (BG420 and FG456)

Pin Name	I/O	BG420 Pin #	FG456 Pin #	Pin Name	I/O	BG420 Pin #	FG456 Pin #
ahvdd_0	P	G4	C26	vddio	P	C5	AC22
ahvdd_1	P	H2	F24	vddio	P	D22	D5
ahvdd2_0	P	G2	D26	vddio	P	D5	D6
ahvdd2_1	P	J5	H24	vddio	P	E13	D7
ahvddg_0	P	G4	D25	vddio	P	E14	D20
ahvddg_1	P	H2	G24	vddio	P	E21	D21
vddio	P	AA22	AA4	vddio	P	E23	D22
vddio	P	AA5	AA5	vddio	P	E24	E4
vddio	P	AB13	AA22	vddio	P	E3	E5
vddio	P	AB14	AA23	vddio	P	E4	E6
vddio	P	AB21	AB04	vddio	P	E6	E21
vddio	P	AB23	AB05	vddio	P	F22	E22
vddio	P	AB24	AB06	vddio	P	F5	E23
vddio	P	AB3	AB21	vddio	P	N22	F4
vddio	P	AB4	AB22	vddio	P	N5	F5
vddio	P	AB6	AB23	vddio	P	P22	F22
vddio	P	AC22	AC5	vddio	P	P5	F23
vddio	P	AC5	AC6	vddio	P	None	G4
vddio	P	AD22	AC7	vddio	P		G23
vddio	P	AD5	AC20	vddio	P		Y4
vddio	P	C22	AC21	vddio	P		Y23

## V<sub>dd</sub> For The Core

The following 28 pins for the BG420 package and 66 pins for the FG456 package are all +1.25 Volts for V<sub>ddc</sub>.

### 1.25V Power Pins (BG420 and FG456)

Pin Name	I/O	BG420 Pin #	FG456 Pin #	Pin Name	I/O	BG420 Pin #	FG456 Pin #
dvdd_0 <sup>1</sup>	P	H4	F26	vddc	P		E20
dvdd_1 <sup>1</sup>	P	J3	J26	vddc	P		G5
vddc	P	AB22	AB7	vddc	P		G22
vddc	P	AB5	AB8	vddc	P		H4
vddc	P	AC13	AB9	vddc	P		H5
vddc	P	AC14	AB10	vddc	P		H22
vddc	P	AC23	AB11	vddc	P		H23
vddc	P	AC4	AB12	vddc	P		J5
vddc	P	AD14	AB13	vddc	P		J22
vddc	P	AD24	AB14	vddc	P		K5
vddc	P	AD3	AB15	vddc	P		K22
vddc	P	AE2	AB16	vddc	P		L5
vddc	P	AE25	AB17	vddc	P		L22
vddc	P	B2	AB18	vddc	P		M5
vddc	P	B25	AB19	vddc	P		M22
vddc	P	C14	AB20	vddc	P		N5
vddc	P	C24	AC8	vddc	P		N22
vddc	P	C3	AC19	vddc	P		P5
vddc	P	D13	D8	vddc	P		P22
vddc	P	D14	D19	vddc	P		R5
vddc	P	D23	E7	vddc	P		R22
vddc	P	D4	E8	vddc	P		T5
vddc	P	E22	E9	vddc	P		T22
vddc	P	E5	E10	vddc	P		U5
vddc	P	N23	E11	vddc	P		U22
vddc	P	P23	E12	vddc	P		V5
vddc	P	P24	E13	vddc	P		V22
vddc	P	P4	E14	vddc	P		W4
vddc	P		E15	vddc	P		W5
vddc	P		E16	vddc	P		W22
vddc	P		E17	vddc	P		W23
vddc	P		E18	vddc	P		Y5
vddc	P		E19	vddc	P		Y22

### Notes

- These PU clock pins need to be decoupled as described in the *Clock PLL Circuitry* section.

## Vss Ground

There are the following 78 ground pins for the BG420 package and 104 ground pins for the FG456 package.

### Ground Pins (BG420 and FG456)

Pin Name	I/O	BG420 Pin #	FG456 Pin #	Pin Name	I/O	BG420 Pin #	FG456 Pin #
ahvss_0 <sup>1</sup>	P	G3	E24	vss	P	AA4	D9
ahvss_1 <sup>1</sup>	P	H1	G25	vss	P	AB11	D10
ahvss2_0 <sup>1</sup>	P	H5	E26	vss	P	AB16	D11
ahvss2_1 <sup>1</sup>	P	J4	H25	vss	P	AB18	D12
ahvssg_0 <sup>1</sup>	P	H3	E25	vss	P	AB9	D13
ahvssg_1 <sup>1</sup>	P	J2	G26	vss	P	AC16	D15
dvss_0	P	H3	F25	vss	P	AC18	D16
dvss_1	P	J2	H26	vss	P	AC21	D17
vss	P	A1	A1	vss	P	AC6	D18
vss	P	A13	A2	vss	P	AC9	D23
vss	P	A18	AC3	vss	P	AD21	D24
vss	P	A24	AC4	vss	P	AD6	J4
vss	P	A26	AC9	vss	P	C21	J23
vss	P	A3	AC10	vss	P	C6	K4
vss	P	A8	AC11	vss	P	D16	K23
vss	P	AC1	AC12	vss	P	D18	L4
vss	P	AC26	AC13	vss	P	D21	L11
vss	P	AE26	AC15	vss	P	D6	L12
vss	P	AF1	AC16	vss	P	D9	L13
vss	P	AF13	AC17	vss	P	E11	L14
vss	P	AF18	AC18	vss	P	E16	L15
vss	P	AF24	AC23	vss	P	E18	L16
vss	P	AF26	AC24	vss	P	E9	L23
vss	P	AF3	AD2	vss	P	F23	M4
vss	P	AF8	AD3	vss	P	F24	M11
vss	P	B1	AD4	vss	P	F3	M12
vss	P	C1	AD23	vss	P	F4	M13
vss	P	C26	AD24	vss	P	H22	M14
vss	P	G1	AD25	vss	P	H23	M15
vss	P	G26	AE3	vss	P	K22	M16
vss	P	L1	AE24	vss	P	K23	M23
vss	P	L26	B1	vss	P	K4	N11
vss	P	R1	B2	vss	P	K5	N12
vss	P	R26	B24	vss	P	T22	N13
vss	P	W1	C1	vss	P	T5	N14
vss	P	W26	C3	vss	P	V22	N15
vss	P	AA23	C23	vss	P	V23	N16
vss	P	AA24	C24	vss	P	V4	N23
vss	P	AA3	C25	vss	P	V5	P4

**Ground Pins (BG420 and FG456) (Continued)**

Pin Name	I/O	BG420 Pin #	FG456 Pin #	Pin Name	I/O	BG420 Pin #	FG456 Pin #
VSS	P	None	P11	VSS	P	None	R16
VSS	P		P12	VSS	P		R23
VSS	P		P13	VSS	P		T4
VSS	P		P14	VSS	P		T11
VSS	P		P15	VSS	P		T12
VSS	P		P16	VSS	P		T13
VSS	P		P23	VSS	P		T14
VSS	P		R4	VSS	P		T15
VSS	P		R11	VSS	P		T16
VSS	P		R12	VSS	P		T23
VSS	P		R13	VSS	P		U4
VSS	P		R14	VSS	P		U23
VSS	P		R15	VSS	P		V4

**Notes**

1. All ahvss\* pins must go to analog ground.

**No Connection**

There are the following 36 pins which have no connection on the BG420 package.

**No Connect Pins (BG420)**

Pin Name	BG420 Pin #	FG456 Pin #	Pin Name	BG420 Pin #	FG456 Pin #
NC	A2	None	NC	AF2	None
NC	A23		NC	AF23	
NC	A25		NC	AF25	
NC	AB1		NC	B23	
NC	AC2		NC	B24	
NC	AC24		NC	B26	
NC	AC3		NC	B3	
NC	AD1		NC	B4	
NC	AD2		NC	C2	
NC	AD23		NC	C23	
NC	AD25		NC	C25	
NC	AD26		NC	C4	
NC	AD4		NC	D1	
NC	AE1		NC	D2	
NC	AE23		NC	D24	
NC	AE24		NC	D26	
NC	AE3		NC	D3	
NC	AE4		NC	E1	

## PIN SUMMARY (BG420)

This table lists the signals and power for the BG420 package in the alphanumerical order of the pin numbers.

### Pins Organized by Pin Number (BG420)

Pin #	Pin Name	I/O	Type	Pin #	Pin Name	I/O	Type	Pin #	Pin Name	I/O	Type
A1	vss	P	GND	AB3	vddio	P	vddio	AC15	p0_8_6	I/O	I/O
A2	NC		NC	AB4	vddio	P	vddio	AC16	vss	P	GND
A3	vss	P	GND	AB5	vddc	P	vddc	AC17	p0_9_6	I/O	I/O
A4	sd_d_59	I/O	S	AB6	vddio	P	vddio	AC18	vss	P	GND
A5	sd_d_57	I/O	S	AB7	p0_4_2	I/O	I/O	AC19	p0_10_5	I/O	I/O
A6	sd_d_30	I/O	S	AB8	p0_5_2	I/O	I/O	AC20	p0_11_2	I/O	I/O
A7	sd_d_26	I/O	S	AB9	vss	P	GND	AC21	vss	P	GND
A8	vss	P	GND	AB10	p0_6_1	I/O	I/O	AC22	vddio	P	vddio
A9	sd_d_51	I/O	S	AB11	vss	P	GND	AC23	vddc	P	vddc
A10	sd_d_22	I/O	S	AB12	p0_7_2	I/O	I/O	AC24	NC		NC
A11	sd_d_18	I/O	S	AB13	vddio	P	vddio	AC25	p0_12_0	I/O	I/O
A12	sd_clk_3	O	S	AB14	vddio	P	vddio	AC26	vss	P	GND
A13	vss	P	GND	AB15	p0_8_7	I/O	I/O	AD1	NC		NC
A14	sd_ba_1	O	S	AB16	vss	P	GND	AD2	NC		NC
A15	sd_ba_0	O	S	AB17	p0_9_7	I/O	I/O	AD3	vddc	P	vddc
A16	sd_a_9	O	S	AB18	vss	P	GND	AD4	NC		NC
A17	sd_a_6	O	S	AB19	p0_11_1	I/O	I/O	AD5	vddio	P	vddio
A18	vss	P	GND	AB20	p0_11_6	I/O	I/O	AD6	vss	P	GND
A19	sd_cs_1	O	S	AB21	vddio	P	vddio	AD7	p0_4_7	I/O	I/O
A20	sd_we_n	O	S	AB22	vddc	P	vddc	AD8	p0_5_4	I/O	I/O
A21	sd_dqm_4	O	S	AB23	vddio	P	vddio	AD9	p0_5_6	I/O	I/O
A22	sd_dqm_2	O	S	AB24	vddio	P	vddio	AD10	p0_6_3	I/O	I/O
A23	NC		NC	AB25	p0_12_1	I/O	I/O	AD11	p0_6_7	I/O	I/O
A24	vss	P	GND	AB26	p0_12_3	I/O	I/O	AD12	p0_7_4	I/O	I/O
A25	NC		NC	AC1	vss	P	GND	AD13	p0_8_0	I/O	I/O
A26	vss	P	GND	AC2	NC		NC	AD14	vddc	P	vddc
AA1	p0_3_5	I/O	I/O	AC3	NC		NC	AD15	p0_8_5	I/O	I/O
AA2	p0_3_6	I/O	I/O	AC4	vddc	P	vddc	AD16	p0_9_2	I/O	I/O
AA3	vss	P	GND	AC5	vddio	P	vddio	AD17	p0_9_5	I/O	I/O
AA4	vss	P	GND	AC6	vss	P	GND	AD18	p0_10_1	I/O	I/O
AA5	vddio	P	vddio	AC7	p0_4_6	I/O	I/O	AD19	p0_10_4	I/O	I/O
AA22	vddio	P	vddio	AC8	p0_5_3	I/O	I/O	AD20	p0_11_0	I/O	I/O
AA23	vss	P	GND	AC9	vss	P	GND	AD21	vss	P	GND
AA24	vss	P	GND	AC10	p0_6_2	I/O	I/O	AD22	vddio	P	vddio
AA25	p0_12_4	I/O	I/O	AC11	p0_6_6	I/O	I/O	AD23	NC		NC
AA26	p0_12_5	I/O	I/O	AC12	p0_7_3	I/O	I/O	AD24	vddc	P	vddc
AB1	NC		NC	AC13	vddc	P	vddc	AD25	NC		NC
AB2	p0_3_7	I/O	I/O	AC14	vddc	P	vddc	AD26	NC		NC

**Pins Organized by Pin Number (BG420) (Continued)**

Pin #	Pin Name	I/O	Type	Pin #	Pin Name	I/O	Type	Pin #	Pin Name	I/O	Type
AE1	NC		NC	AF15	p0_8_3	I/O	I/O	C3	vddc	P	vddc
AE2	vddc	P	vddc	AF16	p0_9_0	I/O	I/O	C4	NC		NC
AE3	NC		NC	AF17	p0_9_3	I/O	I/O	C5	vddio	P	vddio
AE4	NC		NC	AF18	vss	P	GND	C6	vss	P	GND
AE5	p0_4_0	I/O	I/O	AF19	p0_10_2	I/O	I/O	C7	sd_d_28	I/O	S
AE6	p0_4_4	I/O	I/O	AF20	p0_10_6	I/O	I/O	C8	sd_d_55	I/O	S
AE7	p0_5_0	I/O	I/O	AF21	p0_11_3	I/O	I/O	C9	sd_d_53	I/O	S
AE8	p0_5_5	I/O	I/O	AF22	p0_11_5	I/O	I/O	C10	sd_d_48	I/O	S
AE9	p0_5_7	I/O	I/O	AF23	NC		NC	C11	sd_d_20	I/O	S
AE10	p0_6_4	I/O	I/O	AF24	vss	P	GND	C12	sd_fb_clk_in	I	S
AE11	p0_7_0	I/O	I/O	AF25	NC		NC	C13	sd_clk_2	O	S
AE12	p0_7_5	I/O	I/O	AF26	vss	P	GND	C14	vddc	P	vddc
AE13	p0_7_7	I/O	I/O	B1	vss	P	GND	C15	sd_a_12	O	S
AE14	p0_8_1	I/O	I/O	B2	vddc	P	vddc	C16	sd_a_7	O	S
AE15	p0_8_4	I/O	I/O	B3	NC		NC	C17	sd_a_4	O	S
AE16	p0_9_1	I/O	I/O	B4	NC		NC	C18	sd_a_0	O	S
AE17	p0_9_4	I/O	I/O	B5	sd_d_58	I/O	S	C19	sd_cas_n	O	S
AE18	p0_10_0	I/O	I/O	B6	sd_d_31	I/O	S	C20	sd_dqm_7	O	S
AE19	p0_10_3	I/O	I/O	B7	sd_d_27	I/O	S	C21	vss	P	GND
AE20	p0_10_7	I/O	I/O	B8	sd_d_54	I/O	S	C22	vddio	P	vddio
AE21	p0_11_4	I/O	I/O	B9	sd_d_52	I/O	S	C23	NC		NC
AE22	p0_11_7	I/O	I/O	B10	sd_d_23	I/O	S	C24	vddc	P	vddc
AE23	NC		NC	B11	sd_d_19	I/O	S	C25	NC		NC
AE24	NC		NC	B12	sd_fb_clk_out	O	S	C26	vss	P	GND
AE25	vddc	P	vddc	B13	sd_clk_1	O	S	D1	NC		NC
AE26	vss	P	GND	B14	sd_clk_0	O	S	D2	NC		NC
AF1	vss	P	GND	B15	sd_a_13	O	S	D3	NC		NC
AF2	NC		NC	B16	sd_a_8	O	S	D4	vddc	P	vddc
AF3	vss	P	GND	B17	sd_a_5	O	S	D5	vddio	P	vddio
AF4	p0_4_1	I/O	I/O	B18	sd_a_1	O	S	D6	vss	P	GND
AF5	p0_4_3	I/O	I/O	B19	sd_cs_0	O	S	D7	sd_d_29	I/O	S
AF6	p0_4_5	I/O	I/O	B20	sd_cke	O	S	D8	sd_d_24	I/O	S
AF7	p0_5_1	I/O	I/O	B21	sd_dqm_3	O	S	D9	vss	P	GND
AF8	vss	P	GND	B22	sd_dqm_1	O	S	D10	sd_d_49	I/O	S
AF9	p0_6_0	I/O	I/O	B23	NC		NC	D11	sd_d_21	I/O	S
AF10	p0_6_5	I/O	I/O	B24	NC		NC	D12	sd_d_16	I/O	S
AF11	p0_7_1	I/O	I/O	B25	vddc	P	vddc	D13	vddc	P	vddc
AF12	p0_7_6	I/O	I/O	B26	NC		NC	D14	vddc	P	vddc
AF13	vss	P	GND	C1	vss	P	GND	D15	sd_a_11	O	S
AF14	p0_8_2	I/O	I/O	C2	NC		NC	D16	vss	P	GND

**Pins Organized by Pin Number (BG420) (Continued)**

Pin #	Pin Name	I/O	Type	Pin #	Pin Name	I/O	Type	Pin #	Pin Name	I/O	Type
D17	sd_a_3	O	S	F5	vddio	P	vddio	K5	vss	P	GND
D18	vss	P	GND	F22	vddio	P	vddio	K22	vss	P	GND
D19	sd_ras_n	O	S	F23	vss	P	GND	K23	vss	P	GND
D20	sd_dqm_6	O	S	F24	vss	P	GND	K24	sd_d_38	I/O	S
D21	vss	P	GND	F25	sd_d_43	I/O	S	K25	sd_d_37	I/O	S
D22	vddio	P	vddio	F26	sd_d_42	I/O	S	K26	sd_d_36	I/O	S
D23	vddc	P	vddc	G1	vss	P	GND	L1	vss	P	GND
D24	NC		NC	G2	ahvdd2_0	P	vddio	L2	clk1	I	C
D25	sd_d_47	I/O	S	G3	ahvss_0	P	GND	L3	clk0	I	C
D26	NC		NC	G4	ahvdd_0	P	vddio	L4	ext_io_clk_5	I/O	C
E1	NC		NC	G5	sd_d_63	I/O	S	L5	ext_io_clk_4	I/O	C
E2	sd_d_60	I/O	S	G22	sd_d_44	I/O	S	L22	sd_d_35	I/O	S
E3	vddio	P	vddio	G23	sd_d_41	I/O	S	L23	sd_d_34	I/O	S
E4	vddio	P	vddio	G24	sd_d_40	I/O	S	L24	sd_d_33	I/O	S
E5	vddc	P	vddc	G25	sd_d_15	I/O	S	L25	sd_d_32	I/O	S
E6	vddio	P	vddio	G26	vss	P	GND	L26	vss	P	GND
E7	sd_d_56	I/O	S	H1	ahvss_1	P	GND	M1	jtag_in_3	I	J
E8	sd_d_25	I/O	S	H2	ahvdd_1	P	vddio	M2	jtag_in_2	I	J
E9	vss	P	GND	H3	dvss_0	P	GND	M3	ext_gwi	I	C
E10	sd_d_50	I/O	S	H4	dvdd_0	P	vddc	M4	rst_n	I	C
E11	vss	P	GND	H5	ahvss2_0	P	GND	M5	clk_bypass	I	C
E12	sd_d_17	I/O	S	H22	vss	P	GND	M22	sd_d_6	I/O	S
E13	vddio	P	vddio	H23	vss	P	GND	M23	sd_d_7	I/O	S
E14	vddio	P	vddio	H24	sd_d_14	I/O	S	M24	sd_d_5	I/O	S
E15	sd_a_10	O	S	H25	sd_d_13	I/O	S	M25	sd_d_4	I/O	S
E16	vss	P	GND	H26	sd_d_12	I/O	S	M26	sd_d_3	I/O	S
E17	sd_a_2	O	S	J1	ext_io_clk_0	I/O	C	N1	p0_0_0	I/O	I/O
E18	vss	P	GND	J2	dvss_1	P	GND	N2	jtag_trst_n	I	J
E19	sd_dqm_5	O	S	J3	dvdd_1	P	vddc	N3	jtag_in_0	O	J
E20	sd_dqm_0	O	S	J4	ahvss2_1	P	GND	N4	jtag_in_1	I	J
E21	vddio	P	vddio	J5	ahvdd2_1	P	vddio	N5	vddio	P	vddio
E22	vddc	P	vddc	J22	sd_d_11	I/O	S	N22	vddio	P	vddio
E23	vddio	P	vddio	J23	sd_d_10	I/O	S	N23	vddc	P	vddc
E24	vddio	P	vddio	J24	sd_d_9	I/O	S	N24	sd_d_0	I/O	S
E25	sd_d_46	I/O	S	J25	sd_d_8	I/O	S	N25	sd_d_1	I/O	S
E26	sd_d_45	I/O	S	J26	sd_d_39	I/O	S	N26	sd_d_2	I/O	S
F1	sd_d_62	I/O	S	K1	ext_io_clk_3	I/O	C	P1	p0_0_3	I/O	I/O
F2	sd_d_61	I/O	S	K2	ext_io_clk_2	I/O	C	P2	p0_0_2	I/O	I/O
F3	vss	P	GND	K3	ext_io_clk_1	I/O	C	P3	p0_0_1	I/O	I/O
F4	vss	P	GND	K4	vss	P	GND	P4	vddc	P	vddc

**Pins Organized by Pin Number (BG420) (Continued)**

Pin #	Pin Name	I/O	Type	Pin #	Pin Name	I/O	Type	Pin #	Pin Name	I/O	Type
P5	vddio	P	vddio	T23	p0_14_6	I/O	I/O	V25	p0_13_7	I/O	I/O
P22	vddio	P	vddio	T24	p0_14_7	I/O	I/O	V26	p0_14_0	I/O	I/O
P23	vddc	P	vddc	T25	p0_15_0	I/O	I/O	W1	vss	P	GND
P24	vddc	P	vddc	T26	p0_15_1	I/O	I/O	W2	p0_2_4	I/O	I/O
P25	p0_15_7	I/O	I/O	U1	p0_1_4	I/O	I/O	W3	p0_2_5	I/O	I/O
P26	p0_15_6	I/O	I/O	U2	p0_1_5	I/O	I/O	W4	p0_2_6	I/O	I/O
R1	vss	P	GND	U3	p0_1_6	I/O	I/O	W5	p0_2_7	I/O	I/O
R2	p0_0_4	I/O	I/O	U4	p0_1_7	I/O	I/O	W22	p0_13_2	I/O	I/O
R3	p0_0_5	I/O	I/O	U5	p0_2_0	I/O	I/O	W23	p0_13_3	I/O	I/O
R4	p0_0_6	I/O	I/O	U22	p0_14_1	I/O	I/O	W24	p0_13_4	I/O	I/O
R5	p0_0_7	I/O	I/O	U23	p0_14_2	I/O	I/O	W25	p0_13_5	I/O	I/O
R22	p0_15_2	I/O	I/O	U24	p0_14_3	I/O	I/O	W26	vss	P	GND
R23	p0_15_3	I/O	I/O	U25	p0_14_4	I/O	I/O	Y1	p0_3_0	I/O	I/O
R24	p0_15_4	I/O	I/O	U26	p0_14_5	I/O	I/O	Y2	p0_3_1	I/O	I/O
R25	p0_15_5	I/O	I/O	V1	p0_2_1	I/O	I/O	Y3	p0_3_2	I/O	I/O
R26	vss	P	GND	V2	p0_2_2	I/O	I/O	Y4	p0_3_3	I/O	I/O
T1	p0_1_0	I/O	I/O	V3	p0_2_3	I/O	I/O	Y5	p0_3_4	I/O	I/O
T2	p0_1_1	I/O	I/O	V4	vss	P	GND	Y22	p0_12_2	I/O	I/O
T3	p0_1_2	I/O	I/O	V5	vss	P	GND	Y23	p0_12_6	I/O	I/O
T4	p0_1_3	I/O	I/O	V22	vss	P	GND	Y24	p0_12_7	I/O	I/O
T5	vss	P	GND	V23	vss	P	GND	Y25	p0_13_0	I/O	I/O
T22	vss	P	GND	V24	p0_13_6	I/O	I/O	Y26	p0_13_1	I/O	I/O

**Key**

The following abbreviations are used in the I/O column:

P = Power  
 I/O = Input/Output  
 I = Input  
 O = Output  
 blank = No Connect

The following abbreviations are used in the type column:

C = Clock/Reset  
 J = JTAG  
 NC = No Connect  
 S = SDRAM Controller  
 I/O = Programmable I/O  
 GND = Ground  
 vddio = +3.3V Power  
 vddc = +1.25V Power

## PIN SUMMARY (FG456)

This table lists the signals and power for the FG456 package in the alphanumerical order of the pin numbers.

### Pins Organized by Pin Number (FG456)

Pin #	Pin Name	I/O	Type	Pin #	Pin Name	I/O	Type	Pin #	Pin Name	I/O	Type
A1	vss	P	GND	AB3	p0_12_1	I/O	I/O	AC15	vss	P	GND
A2	vss	P	GND	AB4	vddio	P	vddio	AC16	vss	P	GND
A3	sd_dqm_5	O	S	AB5	vddio	P	vddio	AC17	vss	P	GND
A4	sd_cke	O	S	AB6	vddio	P	vddio	AC18	vss	P	GND
A5	sd_cas_n	O	S	AB7	vddc	P	vddc	AC19	vddc	P	vddc
A6	sd_a_0	O	S	AB8	vddc	P	vddc	AC20	vddio	P	vddio
A7	sd_a_1	O	S	AB9	vddc	P	vddc	AC21	vddio	P	vddio
A8	sd_a_4	O	S	AB10	vddc	P	vddc	AC22	vddio	P	vddio
A9	sd_a_7	O	S	AB11	vddc	P	vddc	AC23	vss	P	GND
A10	sd_a_10	O	S	AB12	vddc	P	vddc	AC24	vss	P	GND
A11	sd_a_12	O	S	AB13	vddc	P	vddc	AC25	p0_3_3	I/O	I/O
A12	sd_ba_1	O	S	AB14	vddc	P	vddc	AC26	p0_2_7	I/O	I/O
A13	sd_clk_2	O	S	AB15	vddc	P	vddc	AD1	p0_12_4	I/O	I/O
A14	sd_d_16	I/O	S	AB16	vddc	P	vddc	AD2	vss	P	GND
A15	sd_d_17	I/O	S	AB17	vddc	P	vddc	AD3	vss	P	GND
A16	sd_d_20	I/O	S	AB18	vddc	P	vddc	AD4	vss	P	GND
A17	sd_d_23	I/O	S	AB19	vddc	P	vddc	AD5	p0_11_6	I/O	I/O
A18	sd_d_49	I/O	S	AB20	vddc	P	vddc	AD6	p0_11_2	I/O	I/O
A19	sd_d_52	I/O	S	AB21	vddio	P	vddio	AD7	p0_10_7	I/O	I/O
A20	sd_d_55	I/O	S	AB22	vddio	P	vddio	AD8	p0_10_3	I/O	I/O
A21	sd_d_26	I/O	S	AB23	vddio	P	vddio	AD9	p0_9_7	I/O	I/O
A22	sd_d_27	I/O	S	AB24	p0_3_4	I/O	I/O	AD10	p0_9_4	I/O	I/O
A23	sd_d_30	I/O	S	AB25	p0_3_0	I/O	I/O	AD11	p0_9_0	I/O	I/O
A24	sd_d_57	I/O	S	AB26	p0_2_4	I/O	I/O	AD12	p0_8_5	I/O	I/O
A25	sd_d_60	I/O	S	AC1	p0_12_7	I/O	I/O	AD13	p0_8_2	I/O	I/O
A26	sd_d_62	I/O	S	AC2	p0_12_3	I/O	I/O	AD14	p0_7_4	I/O	I/O
AA1	p0_13_5	I/O	I/O	AC3	vss	P	GND	AD15	p0_7_1	I/O	I/O
AA2	p0_13_1	I/O	I/O	AC4	vss	P	GND	AD16	p0_6_6	I/O	I/O
AA3	p0_12_5	I/O	I/O	AC5	vddio	P	vddio	AD17	p0_6_2	I/O	I/O
AA4	vddio	P	vddio	AC6	vddio	P	vddio	AD18	p0_5_7	I/O	I/O
AA5	vddio	P	vddio	AC7	vddio	P	vddio	AD19	p0_5_4	I/O	I/O
AA22	vddio	P	vddio	AC8	vddc	P	vddc	AD20	p0_4_7	I/O	I/O
AA23	vddio	P	vddio	AC9	vss	P	GND	AD21	p0_4_4	I/O	I/O
AA24	p0_3_1	I/O	I/O	AC10	vss	P	GND	AD22	p0_4_1	I/O	I/O
AA25	p0_2_5	I/O	I/O	AC11	vss	P	GND	AD23	vss	P	GND
AA26	p0_2_0	I/O	I/O	AC12	vss	P	GND	AD24	vss	P	GND
AB1	p0_13_2	I/O	I/O	AC13	vss	P	GND	AD25	vss	P	GND
AB2	p0_12_6	I/O	I/O	AC14	p0_7_5	I/O	I/O	AD26	p0_3_2	I/O	I/O

**Pins Organized by Pin Number (FG456) (Continued)**

Pin #	Pin Name	I/O	Type	Pin #	Pin Name	I/O	Type	Pin #	Pin Name	I/O	Type
AE1	p0_12_2	I/O	I/O	AF15	p0_7_3	I/O	I/O	C3	vss	P	GND
AE2	p0_11_7	I/O	I/O	AF16	p0_7_0	I/O	I/O	C4	sd_dqm_1	O	S
AE3	vss	P	GND	AF17	p0_6_5	I/O	I/O	C5	sd_dqm_3	O	S
AE4	p0_11_4	I/O	I/O	AF18	p0_6_3	I/O	I/O	C6	sd_dqm_6	O	S
AE5	p0_11_1	I/O	I/O	AF19	p0_6_0	I/O	I/O	C7	sd_we_n	O	S
AE6	p0_10_6	I/O	I/O	AF20	p0_5_5	I/O	I/O	C8	sd_cs_0	O	S
AE7	p0_10_4	I/O	I/O	AF21	p0_5_2	I/O	I/O	C9	sd_a_3	O	S
AE8	p0_10_0	I/O	I/O	AF22	p0_5_1	I/O	I/O	C10	sd_a_6	O	S
AE9	p0_9_5	I/O	I/O	AF23	p0_4_6	I/O	I/O	C11	sd_a_9	O	S
AE10	p0_9_2	I/O	I/O	AF24	p0_4_3	I/O	I/O	C12	sd_a_13	O	S
AE11	p0_8_7	I/O	I/O	AF25	p0_4_0	I/O	I/O	C13	sd_clk_0	O	S
AE12	p0_8_4	I/O	I/O	AF26	p0_3_6	I/O	I/O	C14	sd_fb_clk_out	O	S
AE13	p0_8_1	I/O	I/O	B1	vss	P	GND	C15	sd_d_19	I/O	S
AE14	p0_7_6	I/O	I/O	B2	vss	P	GND	C16	sd_d_22	I/O	S
AE15	p0_7_2	I/O	I/O	B3	sd_dqm_2	O	S	C17	sd_d_50	I/O	S
AE16	p0_6_7	I/O	I/O	B4	sd_dqm_4	O	S	C18	sd_d_53	I/O	S
AE17	p0_6_4	I/O	I/O	B5	sd_dqm_7	O	S	C19	sd_d_24	I/O	S
AE18	p0_6_1	I/O	I/O	B6	sd_ras_n	O	S	C20	sd_d_29	I/O	S
AE19	p0_5_6	I/O	I/O	B7	sd_cs_1	O	S	C21	sd_d_56	I/O	S
AE20	p0_5_3	I/O	I/O	B8	sd_a_2	O	S	C22	sd_d_59	I/O	S
AE21	p0_5_0	I/O	I/O	B9	sd_a_5	O	S	C23	vss	P	GND
AE22	p0_4_5	I/O	I/O	B10	sd_a_8	O	S	C24	vss	P	GND
AE23	p0_4_2	I/O	I/O	B11	sd_a_11	O	S	C25	vss	P	GND
AE24	vss	P	GND	B12	sd_ba_0	O	S	C26	ahvdd_0	P	vddio
AE25	p0_3_7	I/O	I/O	B13	sd_clk_1	O	S	D1	sd_d_41	I/O	S
AE26	p0_3_5	I/O	I/O	B14	sd_clk_3	O	S	D2	sd_d_44	I/O	S
AF1	p0_12_0	I/O	I/O	B15	sd_d_18	I/O	S	D3	sd_d_47	I/O	S
AF2	p0_11_5	I/O	I/O	B16	sd_d_21	I/O	S	D4	sd_dqm_0	O	S
AF3	p0_11_3	I/O	I/O	B17	sd_d_48	I/O	S	D5	vddio	P	vddio
AF4	p0_11_0	I/O	I/O	B18	sd_d_51	I/O	S	D6	vddio	P	vddio
AF5	p0_10_5	I/O	I/O	B19	sd_d_54	I/O	S	D7	vddio	P	vddio
AF6	p0_10_2	I/O	I/O	B20	sd_d_25	I/O	S	D8	vddc	P	vddc
AF7	p0_10_1	I/O	I/O	B21	sd_d_28	I/O	S	D9	vss	P	GND
AF8	p0_9_6	I/O	I/O	B22	sd_d_31	I/O	S	D10	vss	P	GND
AF9	p0_9_3	I/O	I/O	B23	sd_d_58	I/O	S	D11	vss	P	GND
AF10	p0_9_1	I/O	I/O	B24	vss	P	GND	D12	vss	P	GND
AF11	p0_8_6	I/O	I/O	B25	sd_d_61	I/O	S	D13	vss	P	GND
AF12	p0_8_3	I/O	I/O	B26	sd_d_63	I/O	S	D14	sd_fb_clk_in	I	S
AF13	p0_8_0	I/O	I/O	C1	vss	P	GND	D15	vss	P	GND
AF14	p0_7_7	I/O	I/O	C2	sd_d_46	I/O	S	D16	vss	P	GND

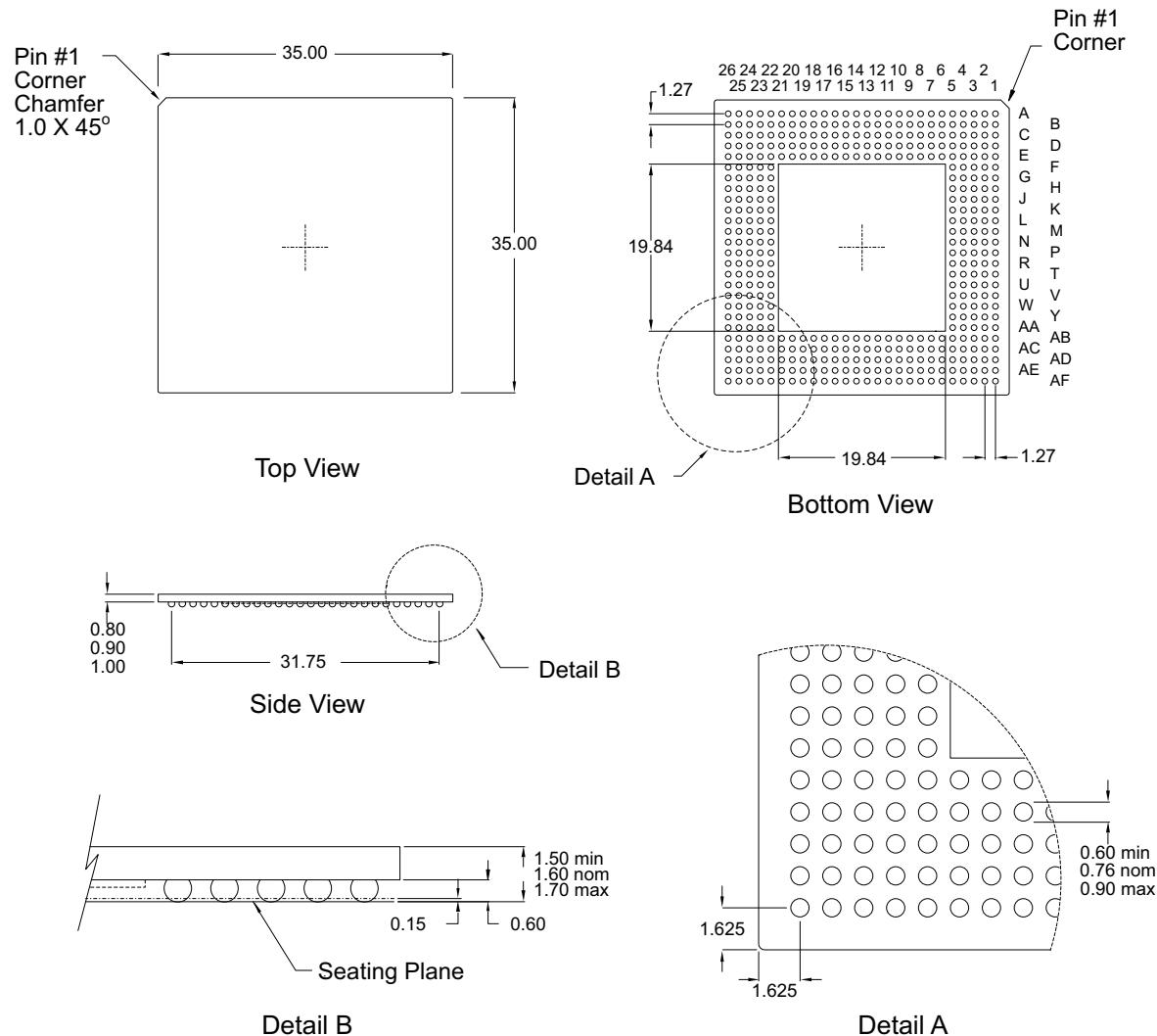
**Pins Organized by Pin Number (FG456) (Continued)**

Pin #	Pin Name	I/O	Type	Pin #	Pin Name	I/O	Type	Pin #	Pin Name	I/O	Type
D17	vss	P	GND	F5	vddio	P	vddio	K5	vddc	P	vddc
D18	vss	P	GND	F22	vddio	P	vddio	K22	vddc	P	vddc
D19	vddc	P	vddc	F23	vddio	P	vddio	K23	vss	P	GND
D20	vddio	P	vddio	F24	ahvdd_1	P	vddio	K24	ext_io_clk_2	I/O	C
D21	vddio	P	vddio	F25	dvss_0	P	GND	K25	ext_io_clk_3	I/O	C
D22	vddio	P	vddio	F26	dvdd_0	P	vddc	K26	ext_io_clk_4	I/O	C
D23	vss	P	GND	G1	sd_d_10	I/O	S	L1	sd_d_7	I/O	S
D24	vss	P	GND	G2	sd_d_12	I/O	S	L2	sd_d_32	I/O	S
D25	ahvddg_0	P	vddio	G3	sd_d_40	I/O	S	L3	sd_d_33	I/O	S
D26	ahvdd2_0	P	vddio	G4	vddio	P	vddio	L4	vss	P	GND
E1	sd_d_14	I/O	S	G5	vddc	P	vddc	L5	vddc	P	vddc
E2	sd_d_42	I/O	S	G22	vddc	P	vddc	L11	vss	P	GND
E3	sd_d_45	I/O	S	G23	vddio	P	vddio	L12	vss	P	GND
E4	vddio	P	vddio	G24	ahvddg_1	P	vddio	L13	vss	P	GND
E5	vddio	P	vddio	G25	ahvss_1	P	GND	L14	vss	P	GND
E6	vddio	P	vddio	G26	ahvssg_1	P	GND	L15	vss	P	GND
E7	vddc	P	vddc	H1	sd_d_39	I/O	S	L16	vss	P	GND
E8	vddc	P	vddc	H2	sd_d_9	I/O	S	L22	vddc	P	vddc
E9	vddc	P	vddc	H3	sd_d_11	I/O	S	L23	vss	P	GND
E10	vddc	P	vddc	H4	vddc	P	vddc	L24	ext_io_clk_5	I/O	C
E11	vddc	P	vddc	H5	vddc	P	vddc	L25	clk0	I	C
E12	vddc	P	vddc	H22	vddc	P	vddc	L26	clk1	I	C
E13	vddc	P	vddc	H23	vddc	P	vddc	M1	sd_d_4	I/O	S
E14	vddc	P	vddc	H24	ahvdd2_1	P	vddio	M2	sd_d_5	I/O	S
E15	vddc	P	vddc	H25	ahvss2_1	P	GND	M3	sd_d_6	I/O	S
E16	vddc	P	vddc	H26	dvss_1	P	GND	M4	vss	P	GND
E17	vddc	P	vddc	J1	sd_d_36	I/O	S	M5	vddc	P	vddc
E18	vddc	P	vddc	J2	sd_d_38	I/O	S	M11	vss	P	GND
E19	vddc	P	vddc	J3	sd_d_8	I/O	S	M12	vss	P	GND
E20	vddc	P	vddc	J4	vss	P	GND	M13	vss	P	GND
E21	vddio	P	vddio	J5	vddc	P	vddc	M14	vss	P	GND
E22	vddio	P	vddio	J22	vddc	P	vddc	M15	vss	P	GND
E23	vddio	P	vddio	J23	vss	P	GND	M16	vss	P	GND
E24	ahvss_0	P	GND	J24	ext_io_clk_0	I/O	C	M22	vddc	P	vddc
E25	ahvssg_0	P	GND	J25	ext_io_clk_1	I/O	C	M23	vss	P	GND
E26	ahvss2_0	P	GND	J26	dvdd_1	P	vddc	M24	clk_bypass	I	C
F1	sd_d_13	I/O	S	K1	sd_d_34	I/O	S	M25	rst_n	I	C
F2	sd_d_15	I/O	S	K2	sd_d_35	I/O	S	M26	ext_gwi	I	C
F3	sd_d_43	I/O	S	K3	sd_d_37	I/O	S	N1	sd_d_0	I/O	S
F4	vddio	P	vddio	K4	vss	P	GND	N2	sd_d_3	I/O	S

**Pins Organized by Pin Number (FG456) (Continued)**

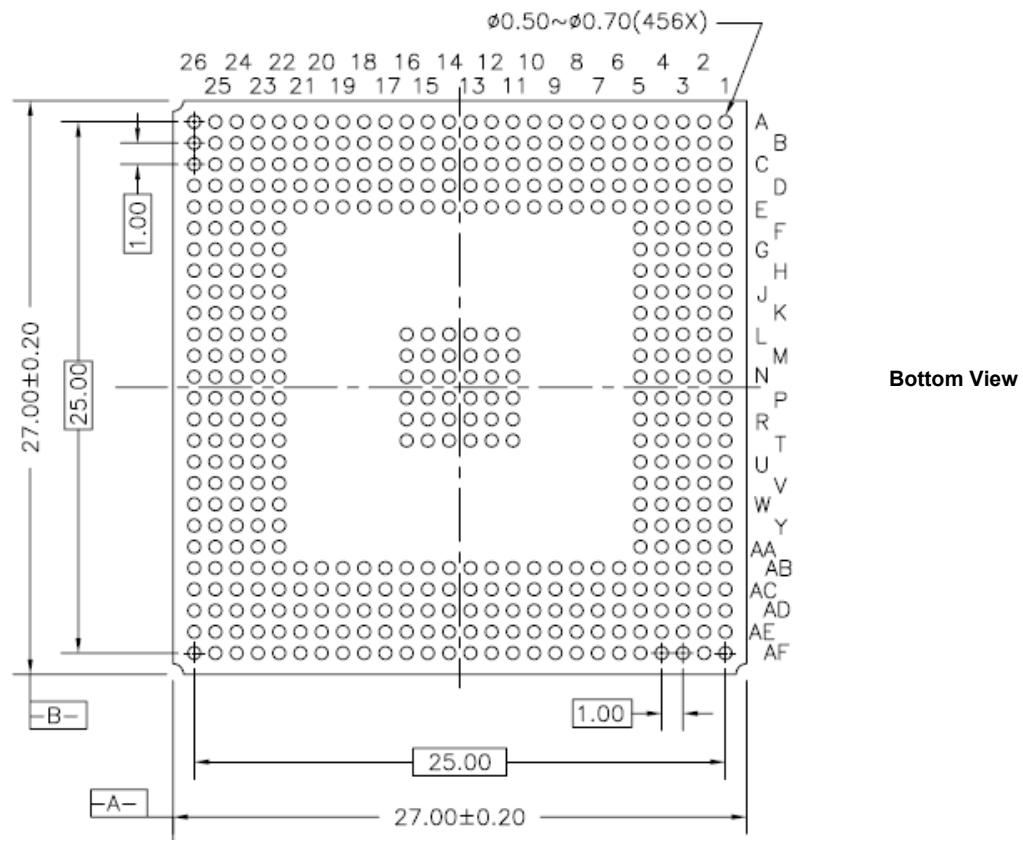
Pin #	Pin Name	I/O	Type	Pin #	Pin Name	I/O	Type	Pin #	Pin Name	I/O	Type
N3	sd_d_1	I/O	S	R5	vddc	P	vddc	U23	vss	P	GND
N4	sd_d_2	I/O	S	R11	vss	P	GND	U24	p0_1_2	I/O	I/O
N5	vddc	P	vddc	R12	vss	P	GND	U25	p0_1_0	I/O	I/O
N11	vss	P	GND	R13	vss	P	GND	U26	p0_0_6	I/O	I/O
N12	vss	P	GND	R14	vss	P	GND	V1	p0_14_4	I/O	I/O
N13	vss	P	GND	R15	vss	P	GND	V2	p0_14_2	I/O	I/O
N14	vss	P	GND	R16	vss	P	GND	V3	p0_14_0	I/O	I/O
N15	vss	P	GND	R22	vddc	P	vddc	V4	vss	P	GND
N16	vss	P	GND	R23	vss	P	GND	V5	vddc	P	vddc
N22	vddc	P	vddc	R24	p0_0_3	I/O	I/O	V22	vddc	P	vddc
N23	vss	P	GND	R25	p0_0_2	I/O	I/O	V23	p0_2_2	I/O	I/O
N24	jtag_tms	I	J	R26	p0_0_1	I/O	I/O	V24	p0_1_5	I/O	I/O
N25	jtag_tck	I	J	T1	p0_15_1	I/O	I/O	V25	p0_1_3	I/O	I/O
N26	jtag_tdi	I	J	T2	p0_15_0	I/O	I/O	V26	p0_1_1	I/O	I/O
P1	p0_15_7	I/O	I/O	T3	p0_14_6	I/O	I/O	W1	p0_14_1	I/O	I/O
P2	p0_15_6	I/O	I/O	T4	vss	P	GND	W2	p0_13_7	I/O	I/O
P3	p0_15_5	I/O	I/O	T5	vddc	P	vddc	W3	p0_13_3	I/O	I/O
P4	vss	P	GND	T11	vss	P	GND	W4	vddc	P	vddc
P5	vddc	P	vddc	T12	vss	P	GND	W5	vddc	P	vddc
P11	vss	P	GND	T13	vss	P	GND	W22	vddc	P	vddc
P12	vss	P	GND	T14	vss	P	GND	W23	vddc	P	vddc
P13	vss	P	GND	T15	vss	P	GND	W24	p0_2_1	I/O	I/O
P14	vss	P	GND	T16	vss	P	GND	W25	p0_1_6	I/O	I/O
P15	vss	P	GND	T22	vddc	P	vddc	W26	p0_1_4	I/O	I/O
P16	vss	P	GND	T23	vss	P	GND	Y1	p0_13_6	I/O	I/O
P22	vddc	P	vddc	T24	p0_0_7	I/O	I/O	Y2	p0_13_4	I/O	I/O
P23	vss	P	GND	T25	p0_0_5	I/O	I/O	Y3	p0_13_0	I/O	I/O
P24	p0_0_0	I/O	I/O	T26	p0_0_4	I/O	I/O	Y4	vddio	P	vddio
P25	jtag_trst	I	J	U1	p0_14_7	I/O	I/O	Y5	vddc	P	vddc
P26	jtag_tdo	O	J	U2	p0_14_5	I/O	I/O	Y22	vddc	P	vddc
R1	p0_15_4	I/O	I/O	U3	p0_14_3	I/O	I/O	Y23	vddio	P	vddio
R2	p0_15_3	I/O	I/O	U4	vss	P	GND	Y24	p0_2_6	I/O	I/O
R3	p0_15_2	I/O	I/O	U5	vddc	P	vddc	Y25	p0_2_3	I/O	I/O
R4	vss	P	GND	U22	vddc	P	vddc	Y26	p0_1_7	I/O	I/O

## PACKAGE OUTLINE DIMENSIONS (BG420)



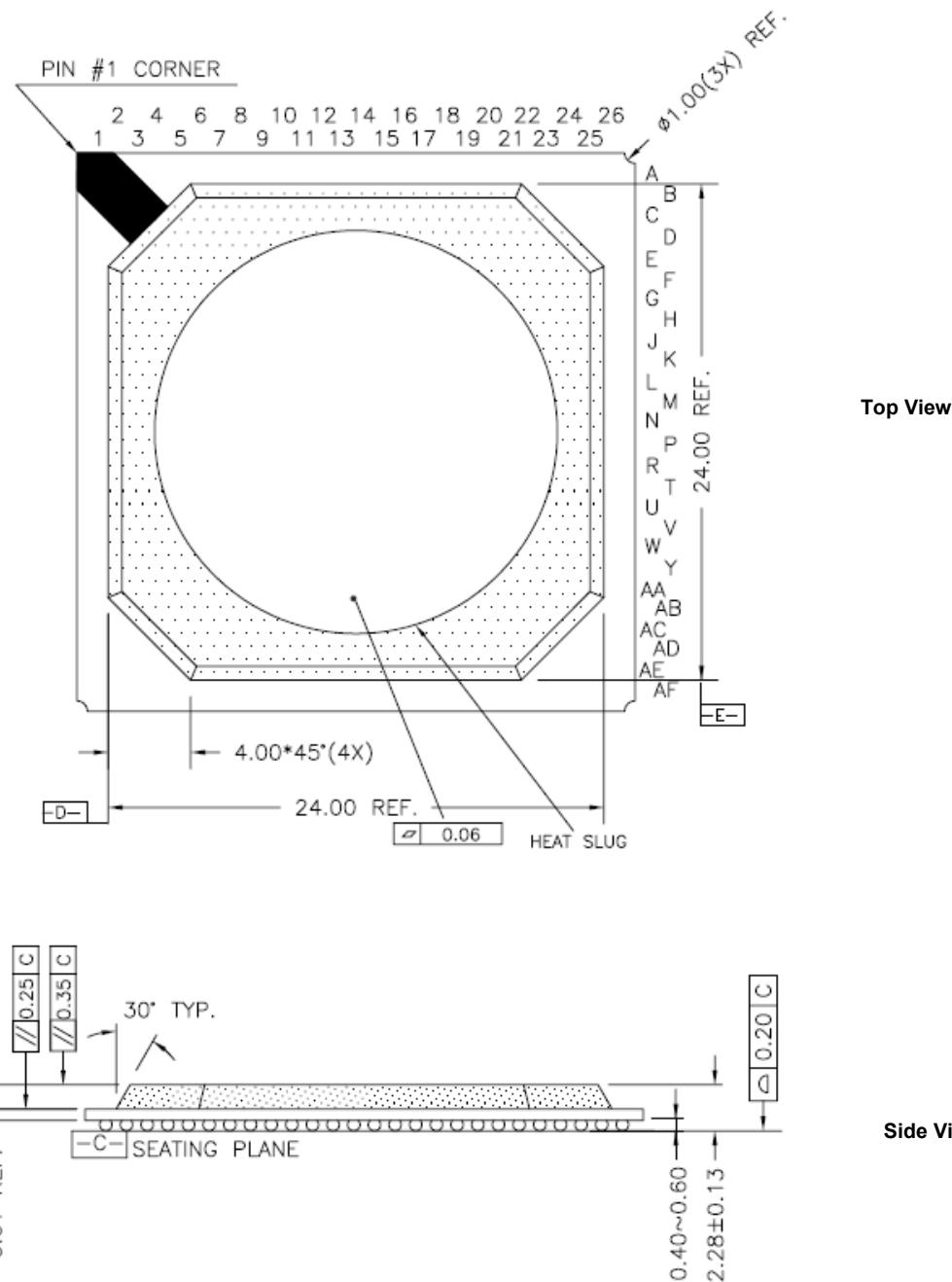
Note: All dimensions are in millimeters.

## PACKAGE OUTLINE DIMENSIONS (FG456)



NOTE: All dimensions are in millimeters.

## PACKAGE OUTLINE DIMENSIONS (FG456) (CONTINUED)



NOTE: All dimensions are in millimeters.

## THERMAL CHARACTERISTICS

### BG420 Package

#### Thermal Characteristics of BGA 420-Pin Package

Characteristic	Symbol	BG420 35 x 35 mm <sup>2</sup>			Units
		Natural Convection	200 ft/min (1 m/s) airflow	400 ft/min (2 m/s) airflow	
Junction-to-ambient <sup>1,2</sup>	$\theta_{JA}$	10	6.4	5.7	°C/W
Junction-to-case <sup>3</sup>	$\theta_{JC}$	0.5	-	-	°C/W

#### Notes

1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2. Per SEMI G38-87 and EIA/JESD51-2 with the single layer (1s) board horizontal.
3. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

### FG456 Package

#### Thermal Characteristics of BGA 456-Pin Package

Characteristic	Symbol	FG456 27 x 27 mm <sup>2</sup>			Units
		Natural Convection	200 ft/min (1 m/s) airflow	400 ft/min (2 m/s) airflow	
Junction-to-ambient <sup>1,2</sup>	$\theta_{JA}$	14	11.4 / 9.8 <sup>4</sup>	10.6 / 8.1 <sup>4</sup>	°C/W
Junction-to-case <sup>3</sup>	$\theta_{JC}$	3.3	-	-	°C/W

#### Notes

1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and EIA/JESD51-2 with the single layer (1s) board horizontal.

3. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.
4. With Cradle recommended heat sink. Estimated using an AAVID Thermalloy tape-mounted heat sink part number 374424B00032. See [www.aavidthermalloy.com](http://www.aavidthermalloy.com).