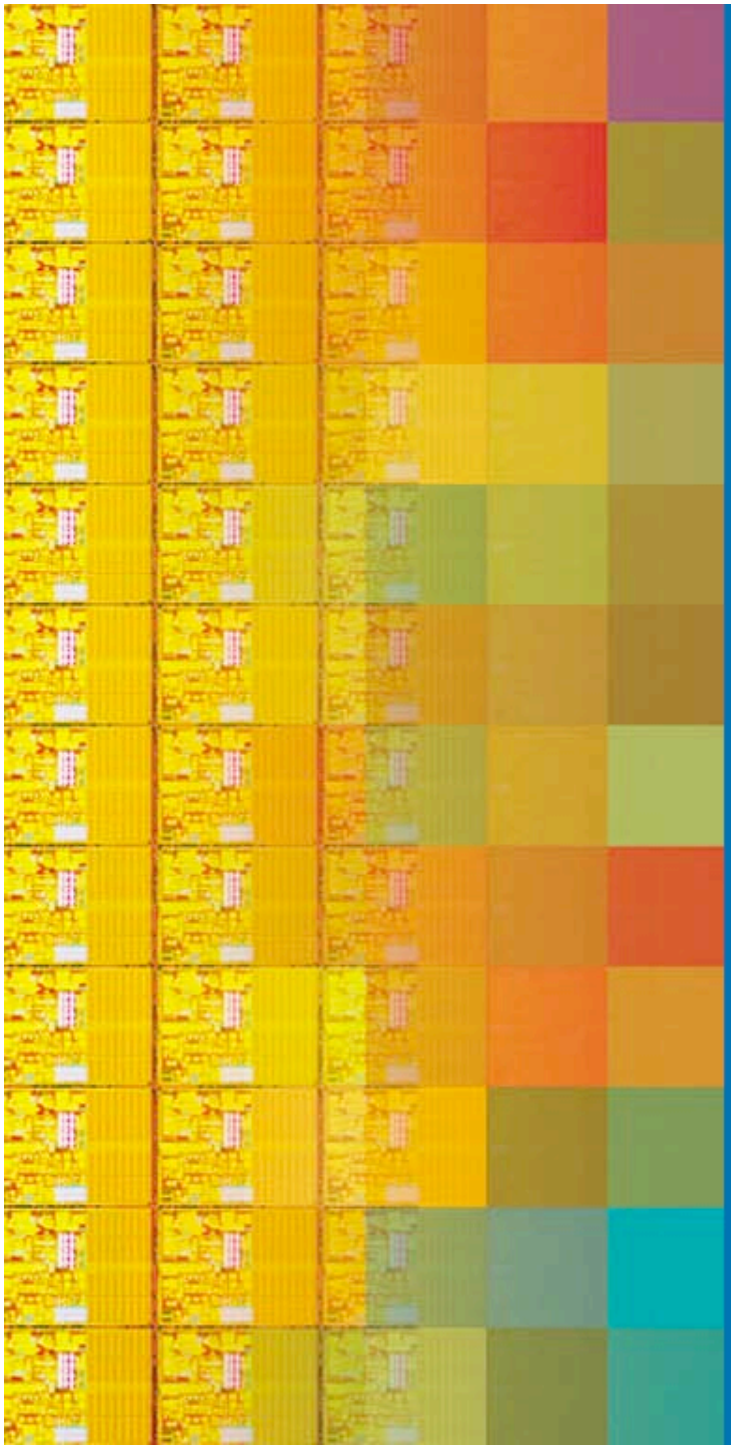

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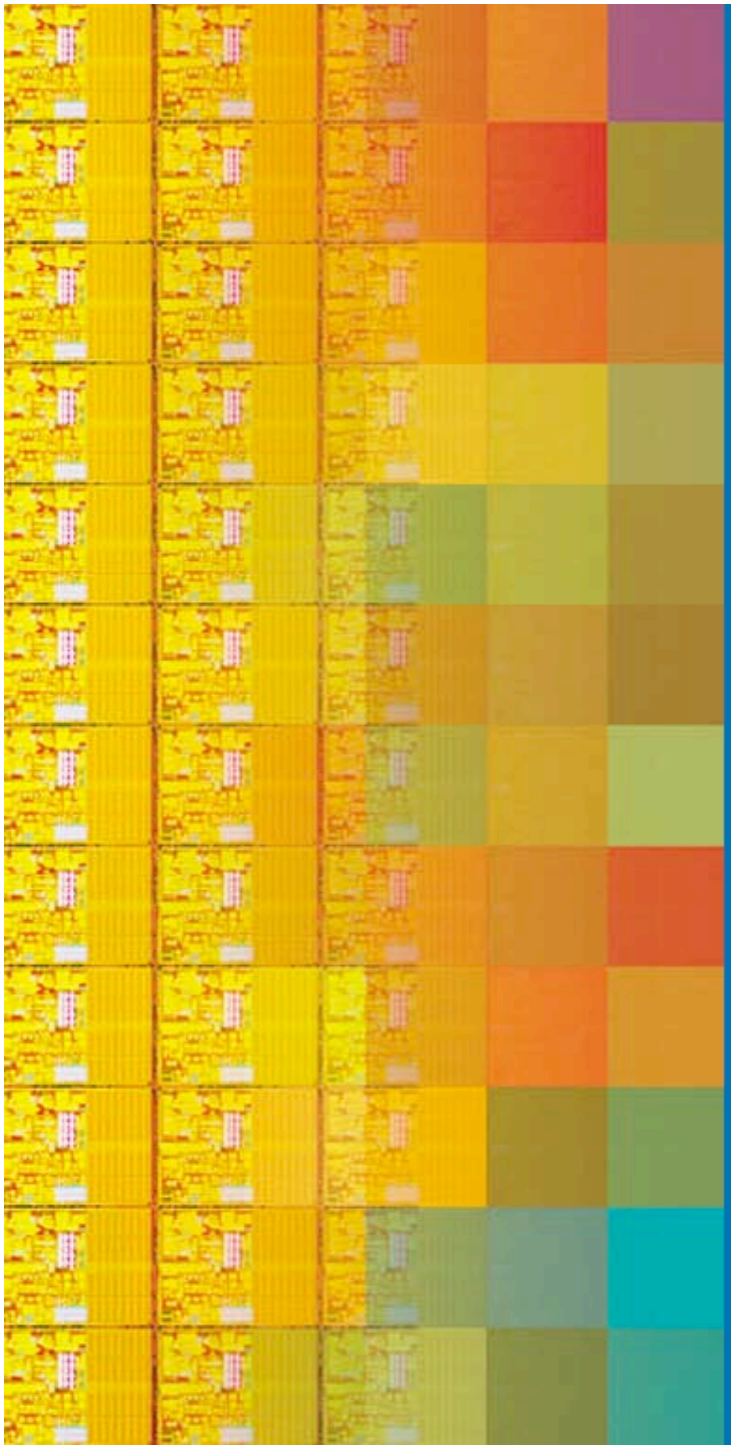

Unified Display Interface (UDI) Technical Overview

George Hayek
Principal Engineer
Client Ingredient Architecture

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LEGAL INFORMATION

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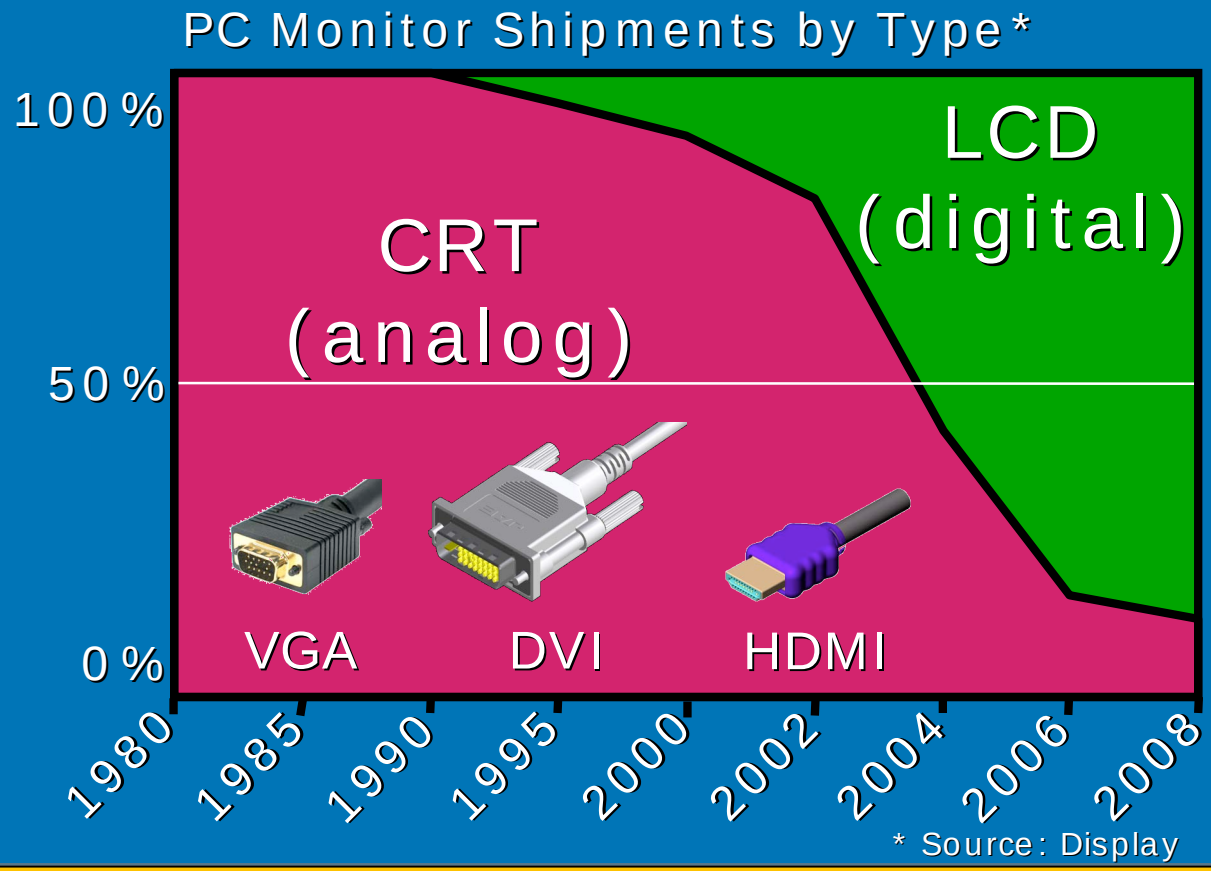
Agenda

- VGA Successor
- Requirements
- Usage Model
- Architecture
- Roadmap

Wither VGA?



* Source: Display Search

Platform Needs a Digital Successor to VGA

Clear Need Exists...

- LVDS - Higher DPI → More B/W, but neither faster nor wider practical
- DVI – Challenged by lack of compliance program and viable spec evolution path
- HDMI – Rapidly becoming a PC requirement for DTV connectivity, but... doesn't satisfy PC needs as-is

•*Plus Deep Submicron Process Integration Challenges*

PC Industry Needs a Better Solution for Future

Requirements for a Viable Replacement Candidate

Technology

- Cost
- Performance
- Features

Industry

- Risk-feasible industry transition
- Effective PC industry technology management organization

End User Experience

- Ease of use

Prior VGA Replacement Efforts Fell Short

CE Solution: HDMI

Technology

- Acceptable cost
- Performance exceeding first product need
- No key feature gaps

Industry

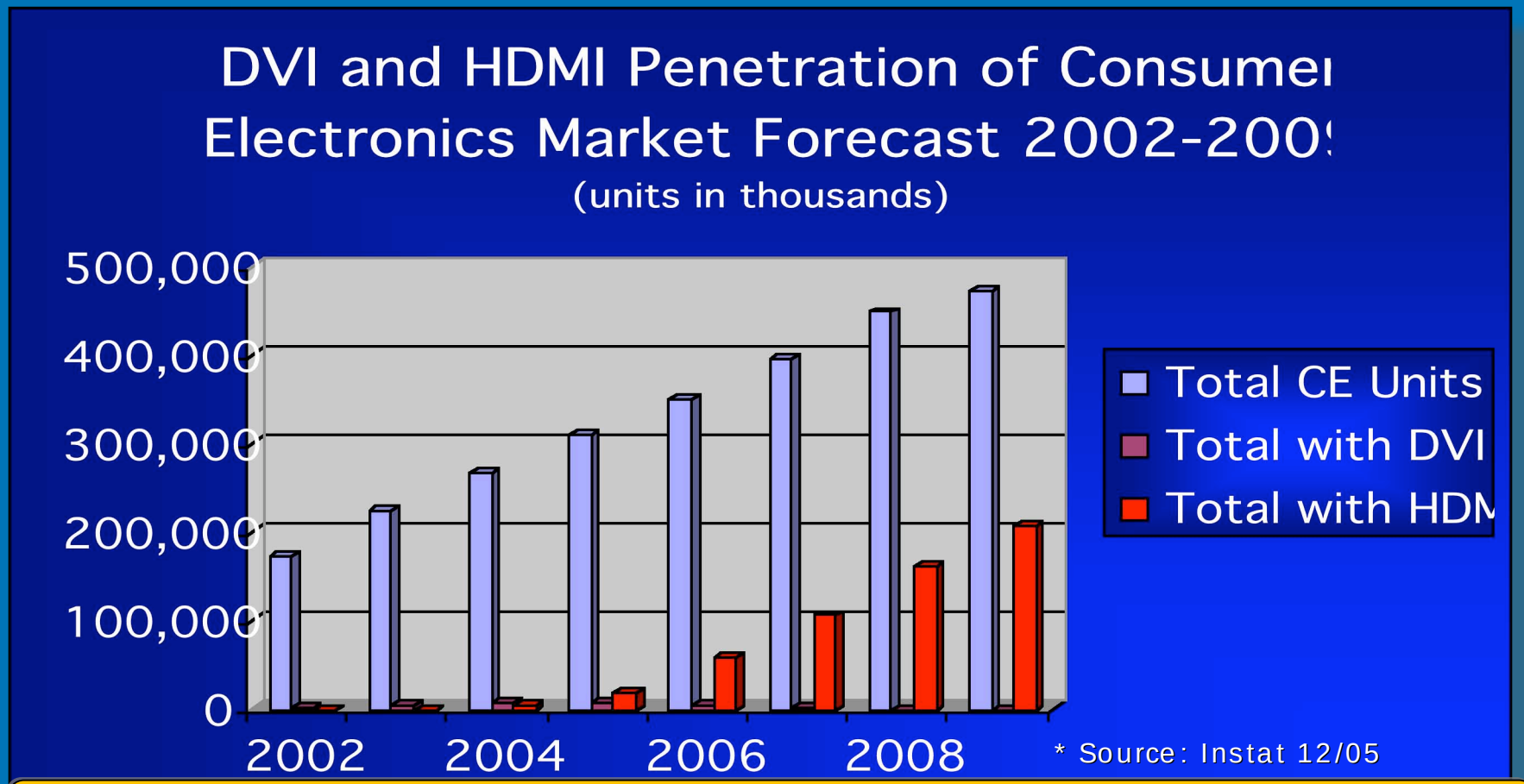
- DVI interoperability to smooth transition
- HDMI LLC
- Robust compliance program

End User Experience

- Promising

Overall an Evolutionary Approach

HDMI Forecasts



HDMI Strong Ramp with Evolutionary Approach

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PC Solution: A Unified Display Interface (UDI)

Technology

- All digital LCD monitors
- Single connector for PC
- AC coupled I/F
- Bandwidth for today's & tomorrow
- CE interop (HDMI)
- Industry accepted digital content protection (HDCP)
- Low power

Industry

- Backwards compatibility to ease market transition
- Extensibility path
- Strong compliance program commitment

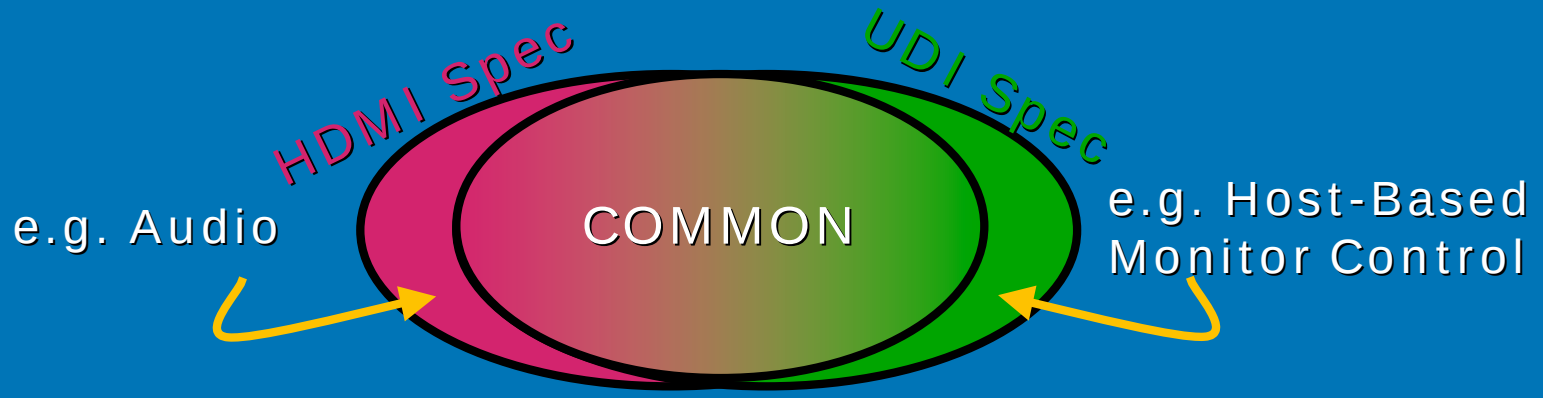
End User Experience

- Simple connectivity

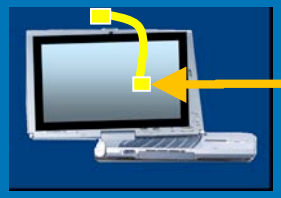
UDI *is* "HDMI Optimized for the PC"
Best Current Successor Candidate

UDI / HDMI Interoperability

- Significant commonality between UDI & HDMI
  - UDI alone meets PC needs, including HDMI interoperability
  - For full HDMI (e.g. audio), implementations license HDMI
- Products can easily support either or both
  - Allows existing implementations to quickly adopt UDI



Multiple Usages Via Simple Cable Options



Embedded – No end user access

Video where HDMI is not required

PC Display

UDI

UDI

OR

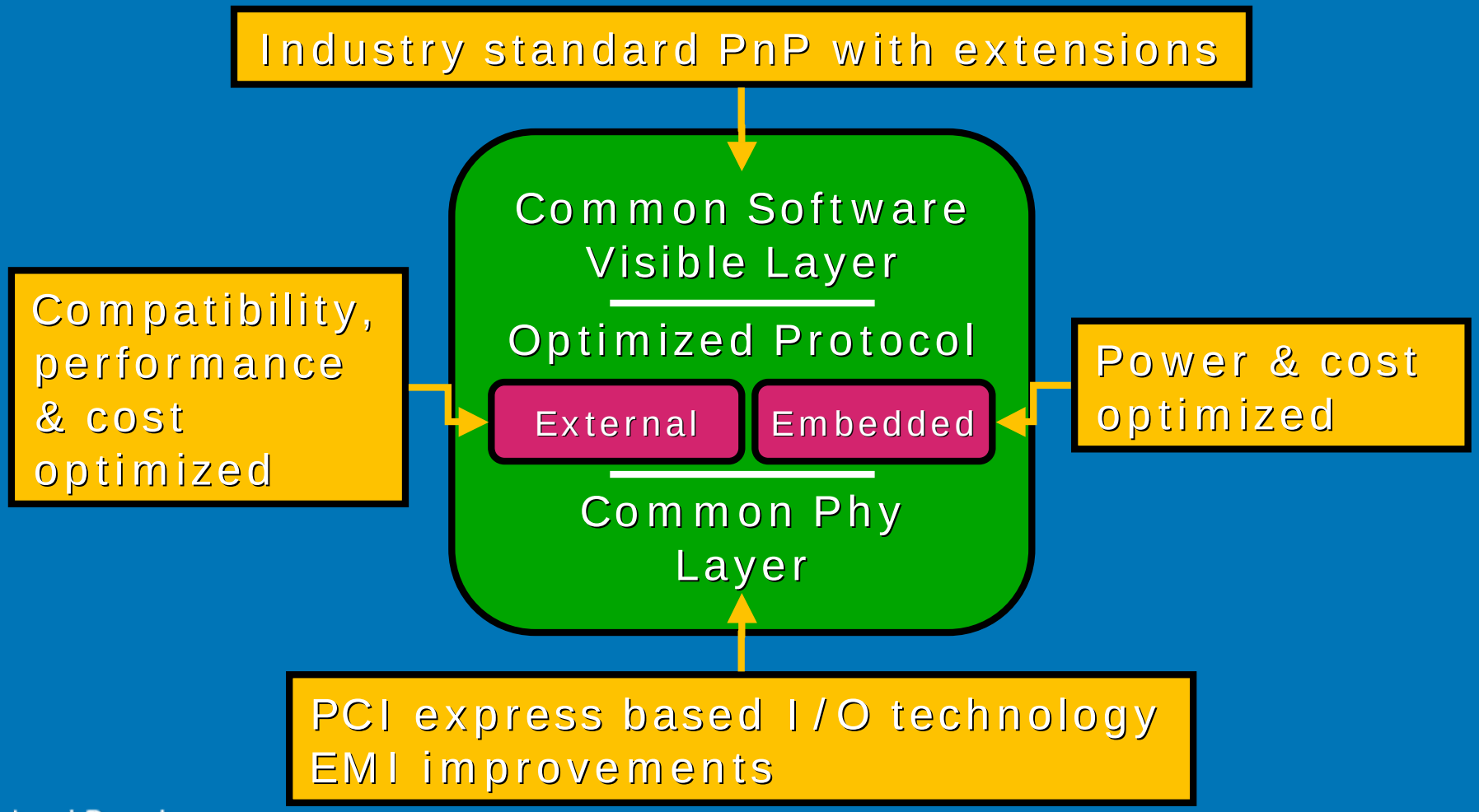
HDMI compatibility, video or audio+video

HDMI

HDTV

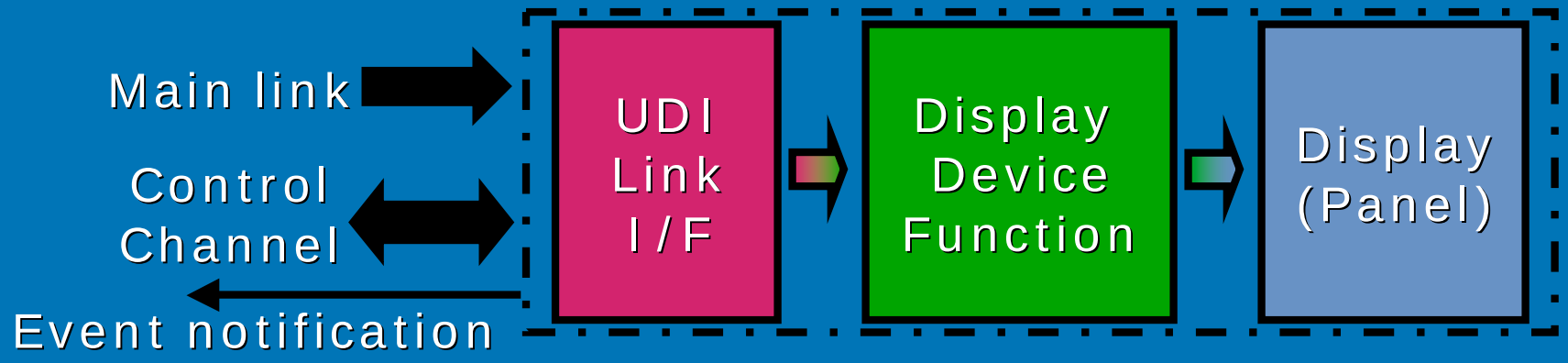
UDI Provides a SINGLE Connector Solution for the PC

Key Spec Architectural Features



Common Software Visible Layer

- Interface & display device function discovery/initialization/control
- Uses Control Channel (I2C)
- Sink event notification (new)



Simple Extensions to Existing Industry Practice

Optimized Profile: External

- 3 data pair “lanes” (RGB)
- 1 clock pair – frequency reference *only*
- HDMI Compatible Framing
  - Active video & non-video
  - HSync, VSync timing
- HDCP

Compatibility, Performance & Cost Optimized

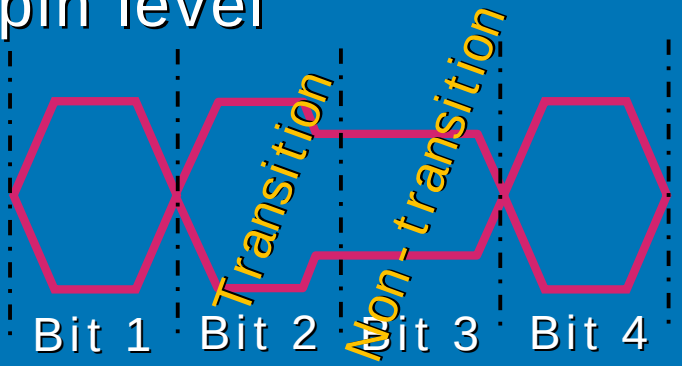
Optimized Profile: Embedded

- 1 or 3 lanes (RGB)
- Display-Enable (DE) Only Framing
  - Active video & non-video
  - Start of Blank, Start of Active indicators
- PLL training pattern in VBlank

Cost/Power Optimized for Notebook LVDS Replacement

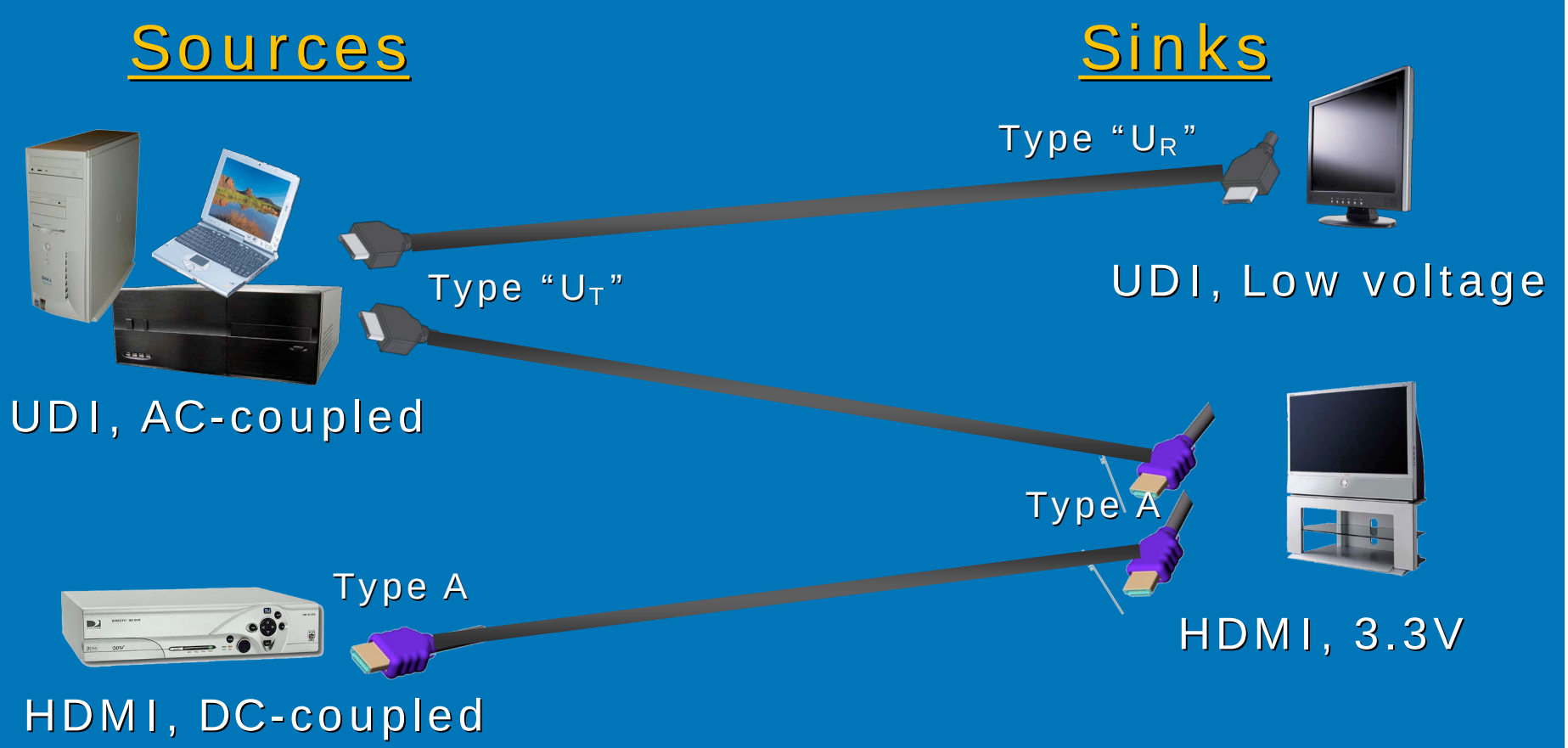
Common Phy Layer

- Logical sub-layer (details in backup)
  - Scrambling & Encoding (profile-specific)
- Electrical sub-layer
  - Optimized for PCI Express I/O buffer technology
  - Connector level spec – not pin level
  - TX eye differs for transition & non-transition bits
  - AC-coupled



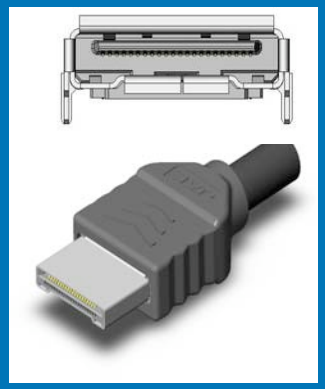
- Clocking (details in backup)

Typed Connectors Manage Electrical Interoperability



External Cable/Connector

Sources



Type "U_T"

Type "U_R"

Sinks

- Key Connector Features
  - Compact size
  - Improved performance - single row, minimized crosstalk
  - Improved EMI performance
  - Uniform contact type for simple tooling
  - Aux Power delivery
- Ease of Use
  - No mis-mating w/USB/LAN/HDMI…
  - Mechanical lock option

(Drawings courtesy of JAE)

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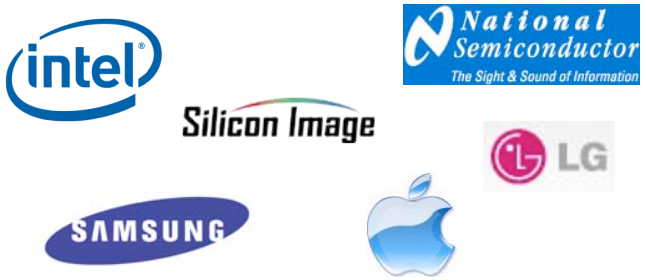
Embedded Cable/Connector

- Standard panel-side connector
  - Extension of existing SPWG LVDS standard
- Guidelines provided for motherboard connector
- Twin-ax and u-coax cable support
- Details in backup

UDI Special Interest Group

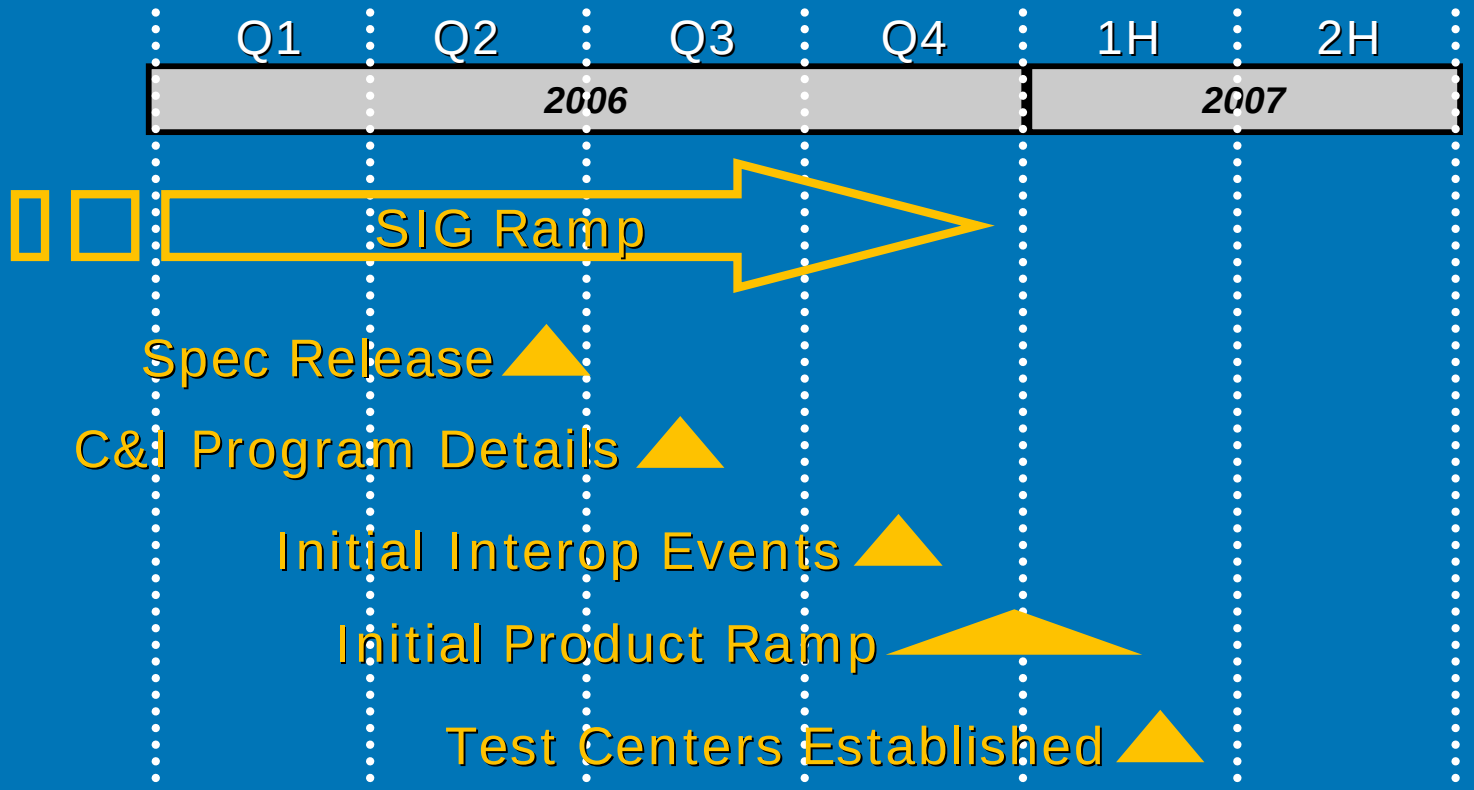
- UDI SIG Formed & Ramping
  - Industry involvement opportunity
  - Modeled after existing industry SIGs (PCI, USB, Bluetooth…)
  - Robust compliance & interoperability (see backup)
  - Open group with industry standard licensing terms
  - www.udisigwebsite.com
- Recognized support from the HDMI Licensing LLC
- HDCP support from DCP LLC
  - Over 200 licensees

UDI Promoters



UDI Contributors

SIG ROADMAP



Visit SIG Web-site for add'l information

Summary

- PC needs a Digital Successor to VGA
- UDI *is* "HDMI optimized for the PC"
  - Evolutionary approach
  - Unified single connector with CE/PC interoperability
  - UDI meets PC needs, full HDMI available on same connector
  - Embedded & external optimized protocol profiles
  - High degree of technology reuse (PCIe, DDC/I2C PnP, HDCP…)
- SIG formed and ramping – Call to Action to get engaged

Please fill out the Session Evaluation Form.

Additional sources of information on this topic:

- UDI Informational Brochure
- Related Session -- DHDS002 “Delivering HDTV Capable PCs for the Digital Home”
- Web: http://www.udisigwebsite.com

Join us at the Fall 2006 IDF, Sept 26-28 to learn more about these related topics:

- UDI SIG Updates

Session presentation available on IDF web site –
when prompted enter:
Username: idf
Password: SPR2006

Thank You!

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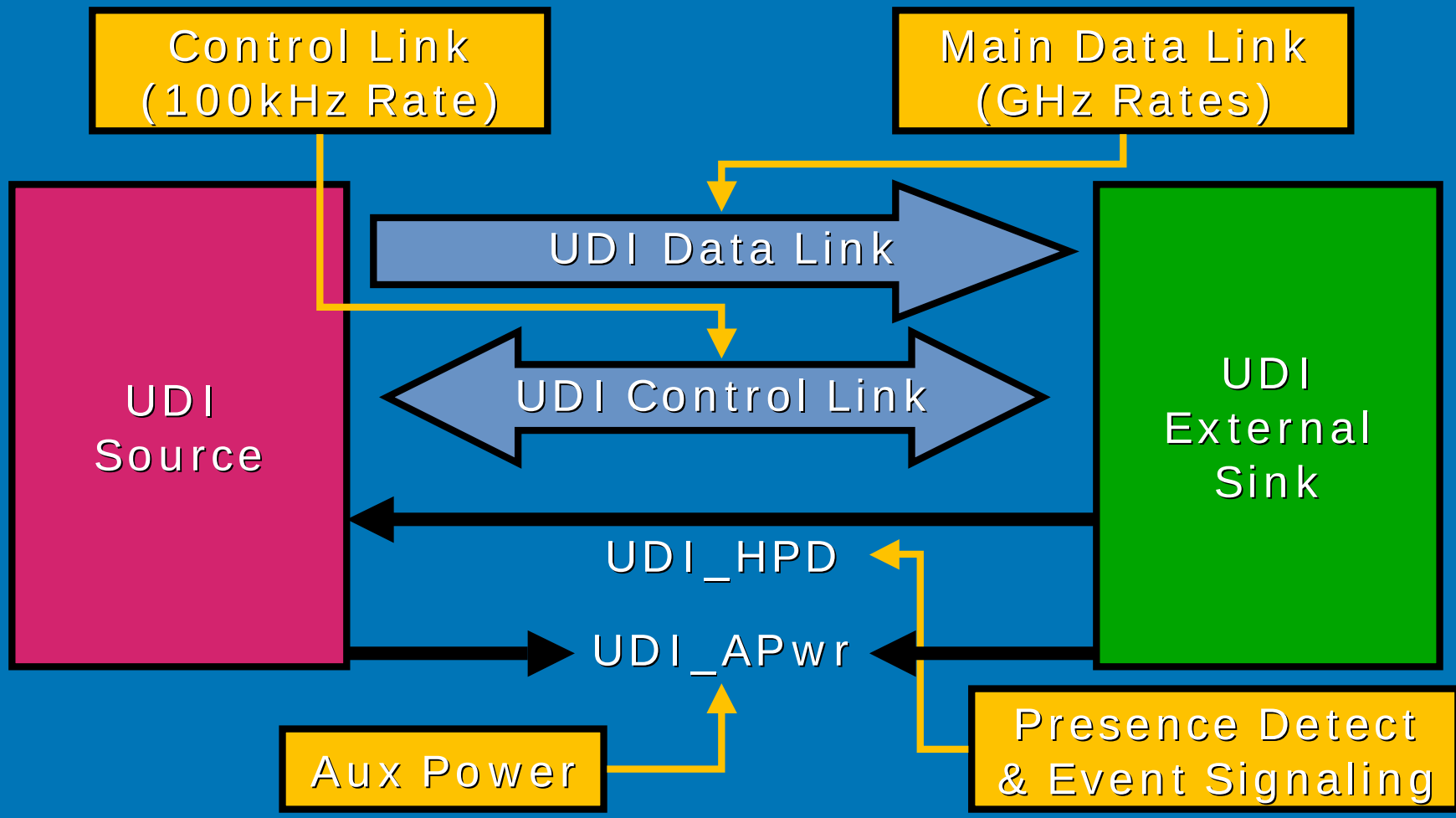
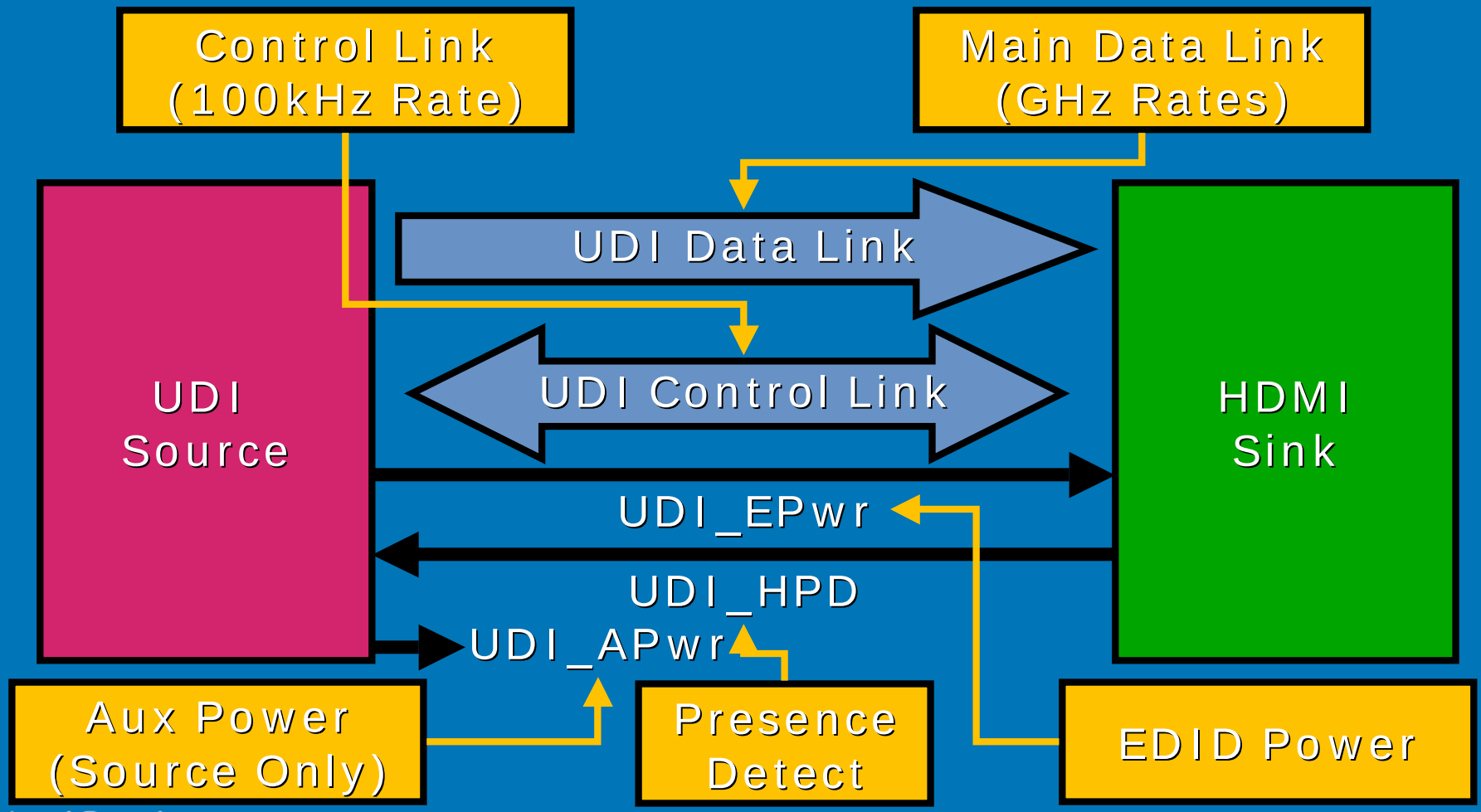
BACKUP

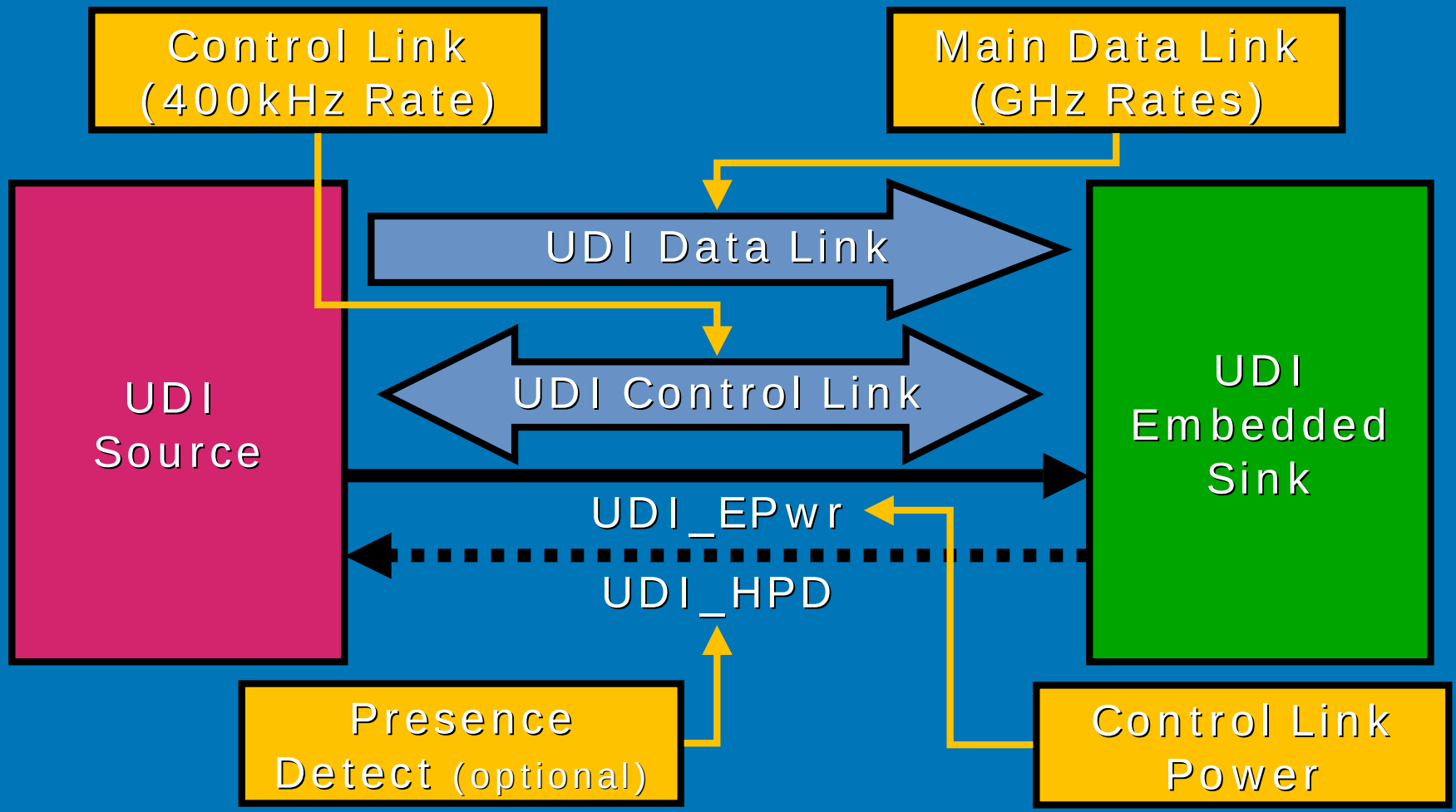
Signal Overview (UDI External Sink)



Signal Overview (HDMI Sink)

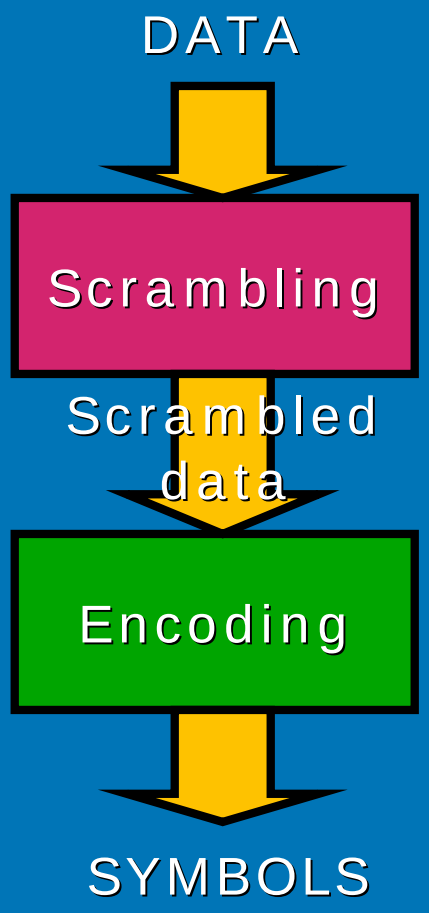


Signal Overview (UDI Embedded Sink)



Phy Logical sub-Layer

- Scrambling
  - Data first scrambled to spread frequency content
  - Performed Per-lane
  - Uses proven PCI Express LFSR polynomial - G(X)=X16+X5+X4+X3+1
  - Disable option required for TX, recommended for RX
- Encoding (8b10b)
  - 8b scrambled data encoded to 10b SYMBOLs for DC balance
  - Special characters convey control
  - 8b10b code sets profile-specific



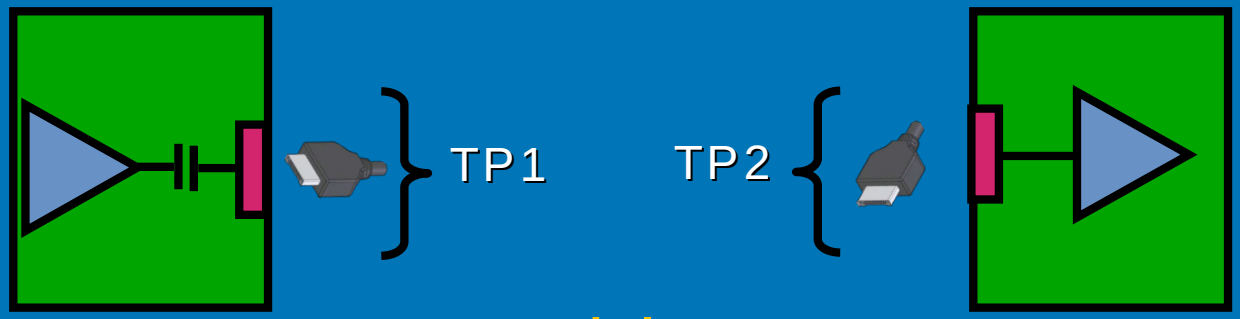
Clocking

- Variable rate, proportional to pixel clock
  - Power advantage vs. fixed rate approach
  - Minimizes process technology requirements
- Forwarded clock at symbol rate (1/10 bit rate)
  - Continuous in external profile
  - Periodic in embedded profile ("*Inferred*" clock recovery)
- .5% Spread Spectrum Support
- Ideal Recovered Clock (IRC) defines jitter requirements -- *Not* a PLL B/W spec!

Test Points: External

Sources

Sinks



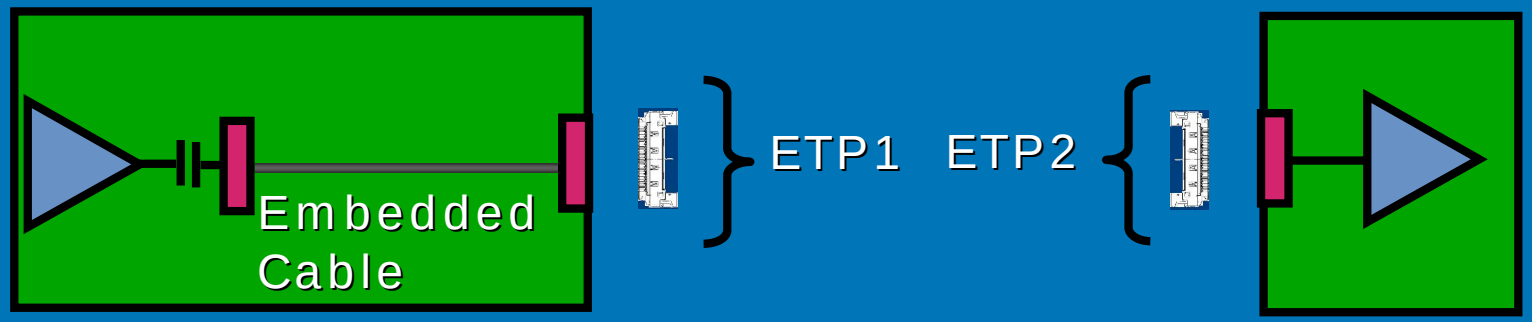
Cables

Compliance Tested at Relevant Interoperability Points

Test Points: Embedded

Sources

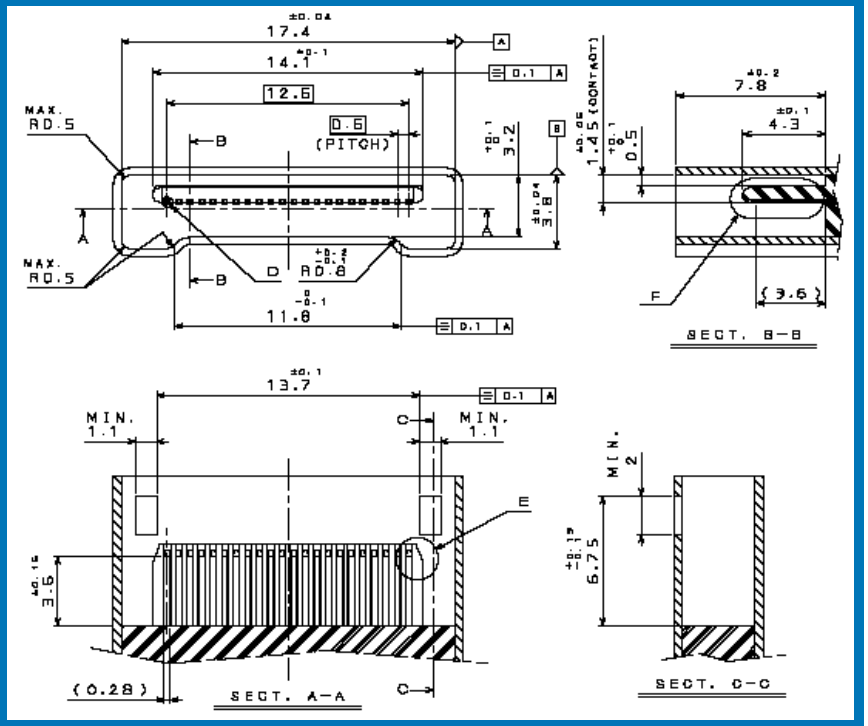
Sinks



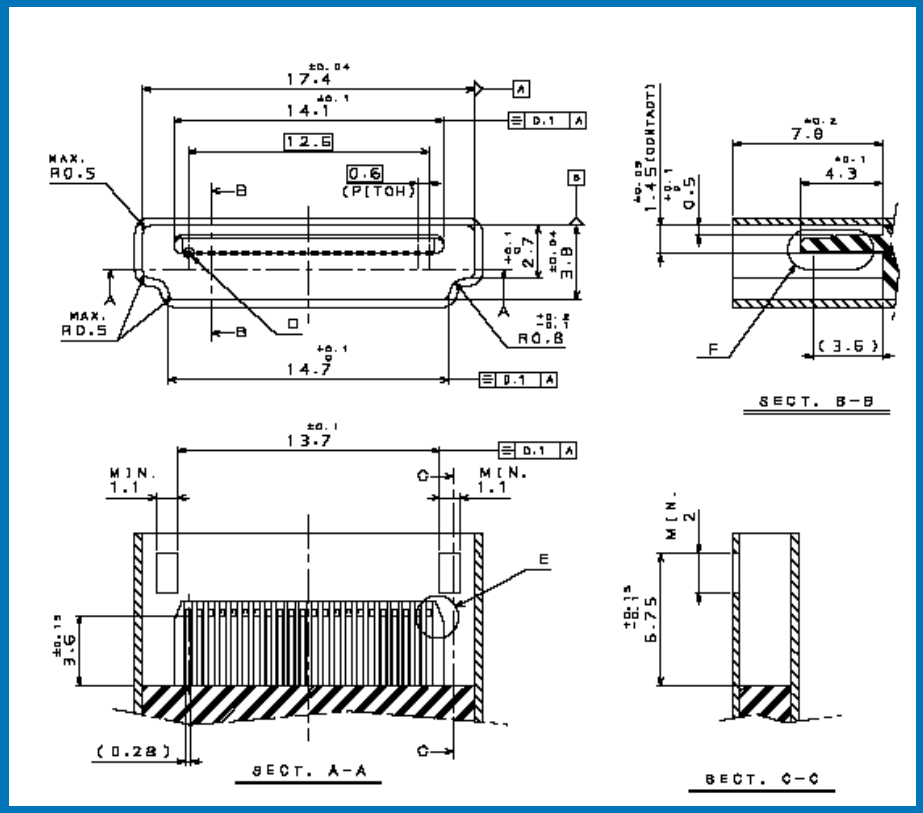
- No end user accessible cable
- Cable included in source budget

Compliance Tested at Relevant Interoperability Points

Receptacle Connectors



Source



Sink

(From JAE drawings)

Single Row, 0.6mm Pitch Interfaces

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Pin List & Cable Mapping (External)

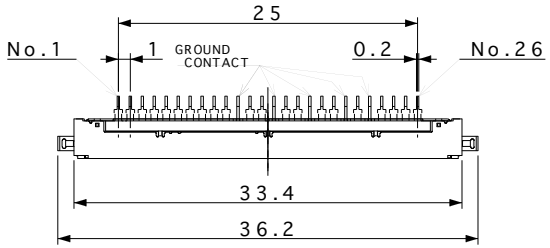
Pin Name	Count	Comment
UDI_data0+/- and Gnd (drain)	3	Twinax cable
UDI_data1+/- and Gnd (drain)	3	Twinax cable
UDI_data2+/- and Gnd (drain)	3	Twinax cable
UDI_clk+/- and Gnd (drain)	3	Twinax cable
UDI_CtrlClk, UDI_CtrlData	2	I2C, discrete wire
UDI_LPwr	1	5V power, last mate
UDI_HPD	1	Hotplug detect
CEC	1	
Gnd	1	Discrete wire
UDI_APwr	1	Aux power (tbd)
Reserved in connector	3	NC in cable
Total	22	19 in cable

Reserved 3 pins in connector for an additional diff pair

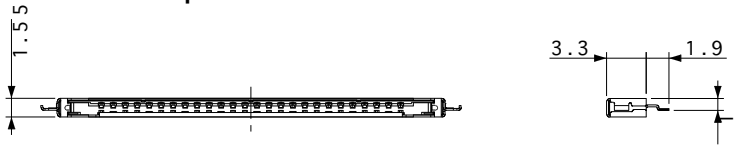
UDI Src Pin	UDI Signal	UDI Sink Pin	HDMI Signal	HDMI Sink Pin
1	RSVD	1		
2	RSVD	2		
3	RSVD	3		
4	Gnd	4	TMDS Date2 Shield	2
5	UDI_Data2+	5	TMDS Data2+	1
6	UDI_Data2-	6	TMDS Data2-	3
7	Gnd	7	TMDS Date1 Shield	5
8	UDI_Data1+	8	TMDS Data1+	4
9	UDI_Data1-	9	TMDS Data1-	6
10	Gnd	10	TMDS Date0 Shield	8
11	UDI_Data0+	11	TMDS Data0+	7
12	UDI_Data0-	12	TMDS Data0-	9
13	Gnd	13	TMDS Clock Shield	11
14	UDI_Clk+	14	TMDS Clock+	10
15	UDI_Clk-	15	TMDS Clock-	12
16	Gnd	16	DDC/CEC Ground	17
17	CEC	17	CEC	13
18	RSVD	18	Reserved	14
19	UDI_CtrlClk	19	SCL	15
20	UDI_CtrlData	20	SDA	16
21	UDI_LPwr	21	+5V Power	18
22	UDI_HPD	22	Hot Plug Detect	19
	Connector shell		Connector shell	

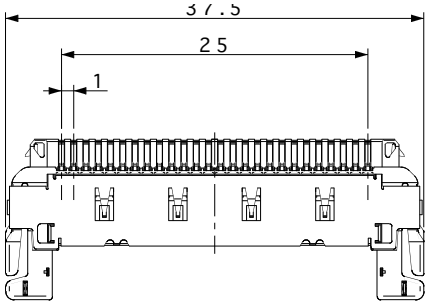
Embedded Connector Pin List (Panel Connector Side)

Pin Name	Count	Comment
UDI_data0+/- and Gnd (drain)	3	
UDI_data1+/- and Gnd (drain)	3	
UDI_data2+/- and Gnd (drain)	3	
UDI_CtrlClk, UDI_CtrlData	2	Control, discrete wire
UDI_HPD	1	Hotplug detect
VDD_UDL	2	Data link supply
VSS	2	Data/control return
VDD_UCL	1	Control link supply
Reserved in connector	3	NC in cable
Total	20	

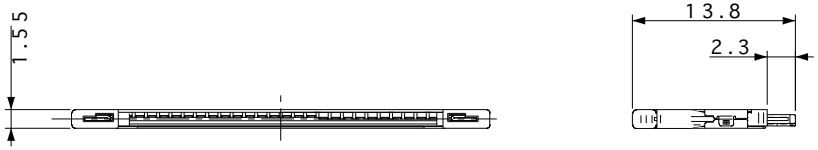


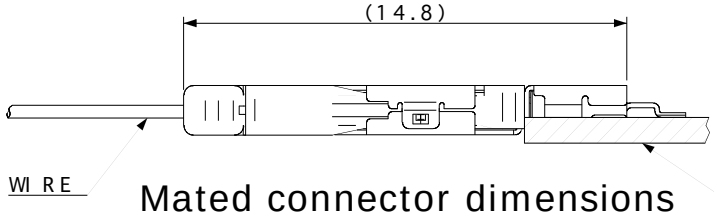
Panel receptacle interface dimensions





Panel plug interface dimensions





Mated connector dimensions

(From JAE Drawings)

UDI Compliance Program

- Scope
  - UDI-UDI interoperability, external and embedded
  - Spec compliance + system-level interoperability
  - Compliance certification allows inclusion on UDI SIG's Qualified Products List
- Venues for compliance certification
  - Periodic/Quarterly: UDI interoperability workshops
  - Permanent: Authorized test centers (may include HDMI ATCs)
- Test methodology
  - Focus on features that affect interoperability
  - Based on UDI SIG defined test tools (patterned after successful USB-IF model)
- Timeframe
  - Policies and procedures: Q2'06
  - Initial compliance test spec draft: Q2'06
  - Test tools: Q3/Q4 '06
  - Interoperability events: start 2H '06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