

## Understanding Signal Integrity

Signal integrity is becoming a more significant problem as clock frequencies increase.

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It is sometimes said that there are two types of engineers—those who have signal integrity problems and those who will. As clock frequencies increase, magnifying signal integrity problems, this saying will become even more accurate.

The first step in solving signal integrity problems is understanding what signal integrity is. A signal with acceptable signal integrity has not been distorted by the electrical properties of the interconnects. Maintaining signal integrity means preventing the electrical properties of interconnects from disrupting this undistorted state.

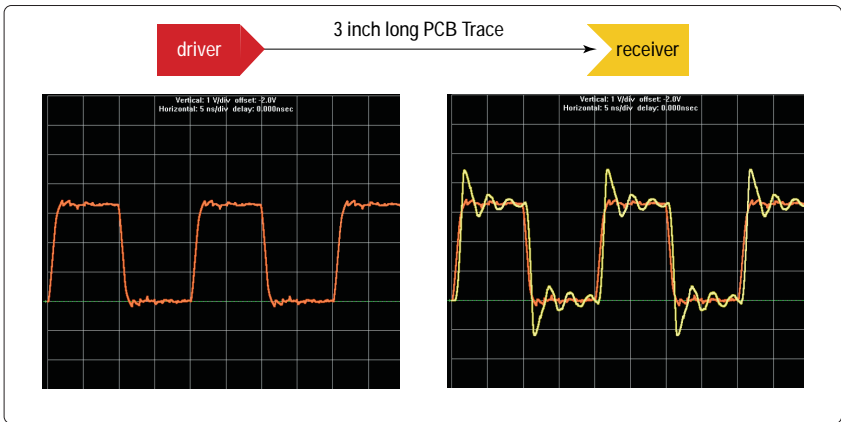


Figure 1. A signal as it emerges from the driver chip (left) is distorted by multiple reflections from impedance discontinuities at both ends (right).

As an example, consider a driver chip that is sending a signal out on a very short inter-

connect, a controlled-impedance line on a circuit board to a receiver (figure 1). The simulation



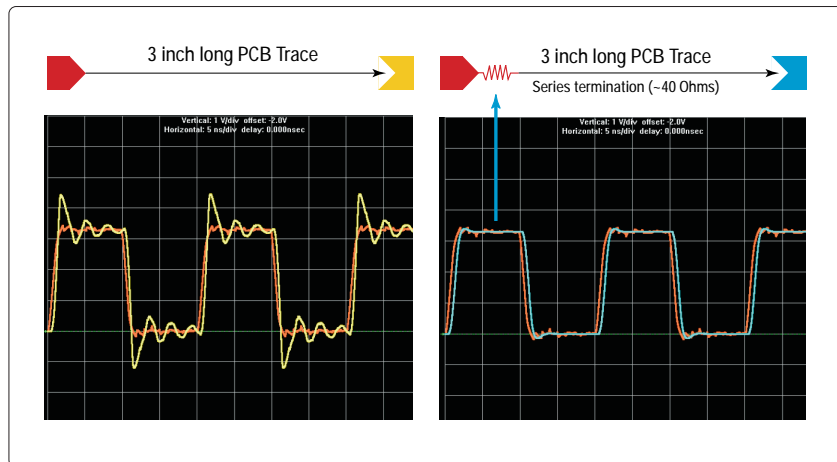


Figure 2. A signal with ringing (left) is returned to an acceptable state by the addition of a series termination resistor on the driver side (right).

on the left shows a 100-MHz clock signal coming out of the driver as it would be if there was nothing connected to the driver. However, the simulation on the right shows what the receiver would detect just 3 inches away on a controlled-impedance circuit board. The ringing is obvious.

What is the cause of this ringing? As a signal propagates down an interconnect, if it encounters a change in the instantaneous impedance of the interconnect, some of it will reflect back to its source and some will become distorted.

This change in instantaneous impedance is known as an impedance discontinuity. What is called ringing is actually due to multiple reflections between impedance discontinuities, typically at the ends.

Consider a driver chip driving a 3 inch, 50-Ω PCB trace and a receiver. This is the physical perspective. From an electrical perspective, as a signal is launched into the transmission line, it encounters the 50-Ω impedance. When the signal reaches the end, it encounters

a high impedance, so it reflects back. When the reflected signal returns to the low impedance of the driver side, another impedance change, it reflects back again. So the origin of the ringing is the signal bouncing back and forth between the impedance discontinuities at the two ends.

Once the source of the problem is identified, a solution can be determined. Figure 2 shows how

to eliminate the ringing problem for this case. The left side shows the ringing from the 3 inch circuit-board trace for the 100-MHz clock. The right side shows the signal after a series terminating resistor was implemented on the driver side. This resistance plus the source resistance of the driver must match the  $50\ \Omega$  of the transmission line. In this case, after the signal is launched into the transmission line, it still will see the  $50\ \Omega$  in the circuit trace, hit the open end of the receiver, and produce a reflection. However, now there won't be another reflection at the driver side, so the multiple bounces will be eliminated. The ringing effects are removed by controlling the impedance mismatch at one end of the line.

This simple example shows that determining the cause of a signal integrity problem is a key to eliminating that problem. Likewise, failure to understand the root causes of signal integrity problems is one of the biggest barriers to success in solving them.

### **Bringing Order to Chaos**

If you have been involved with signal integrity for a while, you have no doubt encountered an avalanche of terms describing the causes and manifestations of signal integrity problems. Ground bounce, crosstalk, non-monotonic edges, skin depth, undershoot, overshoot, parasitics, stub length, gaps in planes, and rise-time degradation are all words or phrases related to signal integrity. It may be difficult to put them into perspective. Classifying these terms into groups can make it easier to isolate a problem and determine its cause.

All the innumerable signal integrity problems and effects can be categorized into four "families". The first is related to signal quality associated with one net, which consists of all the components connected to the same conductor in a circuit board or product. This might be a package lead going to a trace on a circuit board or it may have a couple of branches going to other packages and other receivers. As long as they are all connected together, they are considered to be one net. This includes the return path, which in most boards is one of the planes associated with the multilayer stackup. Minimizing impedance discontinuities is the most critical part of maintaining signal integrity in one net.

The second family of signal integrity problems is related to coupling between multiple signal nets. If there are two traces on a circuit board and a signal is sent into one of them while the other is quiet, some of the

energy from the active trace will couple over to the quiet trace, either through mutual capacitance or mutual inductance. When the return path is an ideal plane, as in most circuit-board applications, the relative amount of capacitive and inductive coupling is about the same for a given system, establishing the geometry for minimum crosstalk. When the return path consists of discrete leads in a package or discrete pins in a connector rather than that ideal plane, the mutual inductance between the signal paths is dramatically increased, which contributes to a large increase in coupling. An example of this type of signal integrity problem is the noise created from coupling through non-ideal return paths, sometimes referred to as simultaneous switching noise (SSN).

The third general family of signal integrity problems is related not to the signal paths but to the power and ground paths in the power distribution network. The problems arise from impedance in the power distribution network, typically implemented as separate planes on a multi-layer printed circuit board. As a chip switches and current flows through the core as well as through the I/O drivers, transient currents flow in the power distribution network, causing voltage drops in the impedance of the power and ground planes. The larger the impedance in the power distribution network, the larger the voltage drop, and less voltage gets to the chip. The way to prevent these problems is to minimize the impedance in the power distribution network. One way is to use planes for power and ground distribution, and to keep them very close together

and as large an area as possible. Another way is to add decoupling capacitors, which decrease the impedance in the power distribution network.

The fourth family of signal integrity problems is related to electromagnetic interference (EMI). EMI includes the susceptibility of a product to fields from the outside world that couple in, and radiated emissions from a product that cause it to fail compliance tests. Reducing other signal integrity problems helps to minimize EMI.

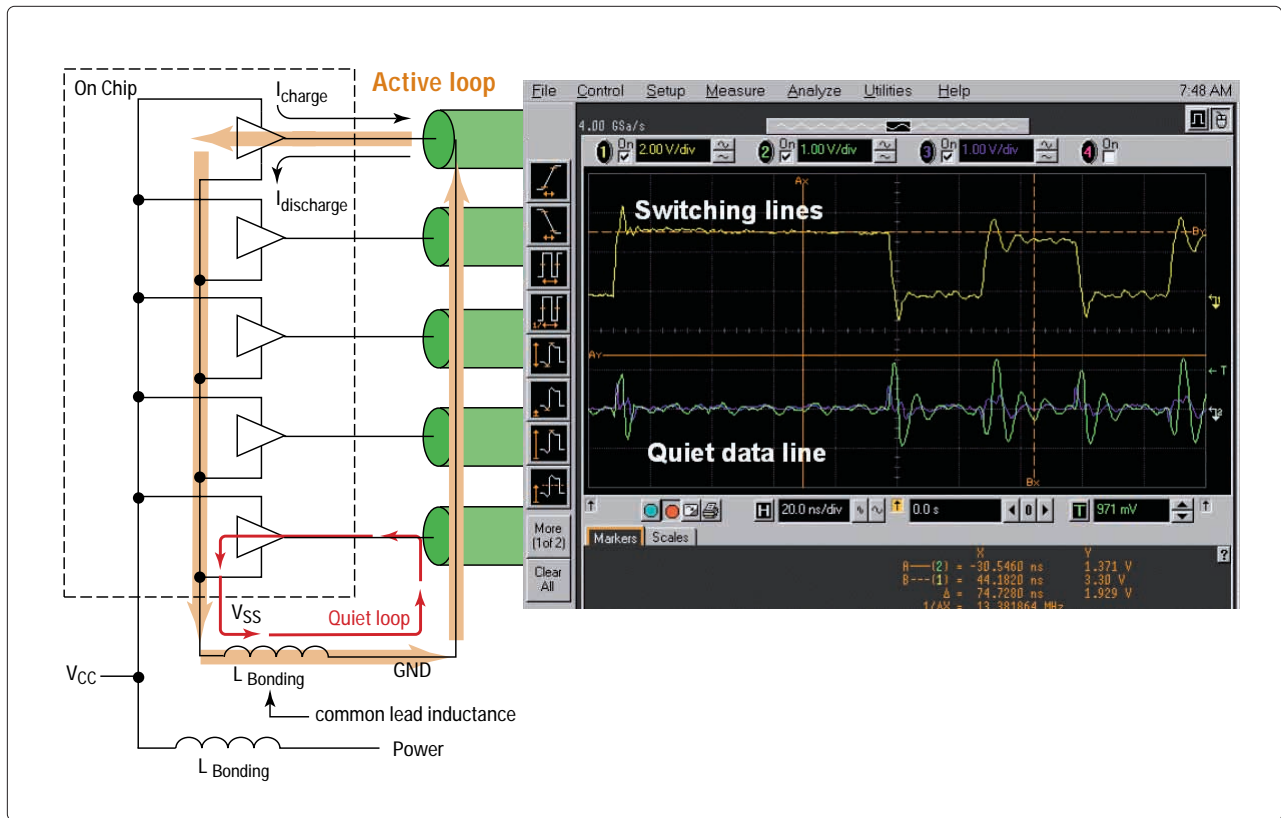


Figure 3. When current flows in the active loop, simultaneous switching noise is generated in the quiet loop.

### Examining SSN

A closer look at a coupling problem can show the role of mutual inductance and how the rise time affects the amount of SSN. Figure 3 shows an example of this. On the right side, measured signals from two data lines exhibit what appears to

be ringing. This turns out to be caused by ground bounce from the various switching lines. The bottom trace shows a line that is not switching, but picks up noise voltage wherever the active lines switch. This noise is generated by mutual inductance between the switching lines and the quiet lines.

The left side of the figure shows a schematic of the setup for this system. It is a small two-layer BGA package with five output drivers connected to transmission lines on the circuit board. These are drawn as small coax cables to emphasize that there is a very specific return path associated with each of the signal lines.

In this particular case, a couple of active lines are switching. As they transition from high to low, they discharge current out of the signal path. This current goes through the driver, through the ground path on the chip itself, out through the ground lead in the chip, and then back to the return path of the transmission line, and continues that current loop as the high-to-low transition propagates down the transmission line.

So current is flowing in a loop that includes a couple of the package leads and part of the trace from the circuit board. This is the active loop. A second, quiet loop is the signal path going through the chip connected to the ground path, and on the chip going through the ground lead and the package and back to the return path. When current flows in the active loop, it generates noise in the quiet loop, resulting in the noise shown on the quiet line. This noise is called simultaneous switching noise because it is coincident with switching on

the active lines. This noise, also called  $dI/dt$  or Delta I noise, depends upon:

- the mutual inductance between the two loops
- how many gates are simultaneously switching
- the mutual inductance between each of those other gates
- how fast the current changes ( $dI/dt$ )

The magnitude of the noise depends first upon the mutual inductance and second upon  $dI/dt$ , so as the rise time decreases,  $dI/dt$  increases, and therefore the amount of SSN is going to increase. This is fundamentally why SSN increases as rise times decrease, which is of course inevitable as clock frequencies increase.

So the future looks perilous for the signal integrity engineer. The channel lengths of transistors are getting smaller, allowing them to switch faster. This results in shorter rise times and therefore higher clock frequencies, so it will become even more difficult to maintain signal integrity.

And then there is the other ominous technology trend: In the globally competitive marketplace, there is less and less time available to get a product to market successfully. Design cycle times are getting shorter, and there isn't time for numerous iterations. The design has to work right the first time. So if you don't have signal integrity problems now, as systems progress to higher speeds, you soon will.

Fortunately, tools and techniques for solving signal integrity problems keep improving as well, so the situation is not hopeless.

In particular, predicting system performance using modeling and simulation, rather than iterative designing, building, testing, and redesigning, is important for signal integrity engineering. Creating high-bandwidth interconnect models for the purpose of improving signal integrity will be covered in the next issue of the Agilent Measurement Solutions Newsletter.

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