Physics and Applications of the Schottky Junction Transistor

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***Abstract*—This paper presents the results from numerical simulations of a novel subthreshold transistor configuration. The device uses the input current from a forward-biased Schottky gate to control the larger current flowing in a depleted channel. Analytical approximations are used to derive the current gain of the transistor. The numerical simulations confirm the analytical derivation and show that a 0.5 μm gate length device would have a cutoff frequency approaching 10 GHz for supply voltages less than 0.5 V. Possible applications of the device in the areas of micropower analog circuits and ULSI logic are discussed.**

***Index Terms*—Metal semiconductor field effect transistors (MESFETs), Schottky barriers, semiconductor device modeling.**

I. Introduction

THE BIPOLAR junction transistor (BJT) and field effect transistor (FET) are the most commonly used transistor configurations. For the case of the BJT, a collector current I_c is controlled by a smaller base current I_b, and the device is modeled as a current-controlled current source. This is in contrast to the FET, where a gate voltage V_{gs} is used to control a drain current I_d, i.e., the FET behaves as a voltage-controlled current-source. Recently, the Schottky Junction Transistor (SJT) has been proposed as a novel micropower device with characteristics similar to both BJTs and FETs [1]. This paper extends the work presented in [1] and discusses possible applications of the SJT.

The cross-section of an SJT is shown schematically in Fig. 1. The doping and thickness are chosen such that the device operates in the subthreshold regime and the drain current varies exponentially with the gate voltage V_{gs}. The input to the SJT is a Schottky gate, and for small forward biases, the gate current I_g also varies exponentially with V_{gs}. By appropriate design of the channel thickness a, channel doping N_D, and gate length L_g, the SJT can be designed to function as a current-controlled current source with a current gain $\beta = I_d/I_g > 1$. Although the SJT resembles an enhancement mode metal semiconductor field effect transistor (MESFET), the use of a current gain to control the drain current gives it features in common with a BJT. However, unlike a BJT, the SJT is a majority carrier device, and it does not suffer from minority charge storage effects due to the diffusion capacitance associated with p-n junction devices. For micropower applications, SJT-based circuits are expected to have certain advantages over their CMOS and BJT-based counterparts. Before discussing possible applications of the SJT, we first describe an analytical approximation for the current gain that is subsequently confirmed by the numerical simulations.

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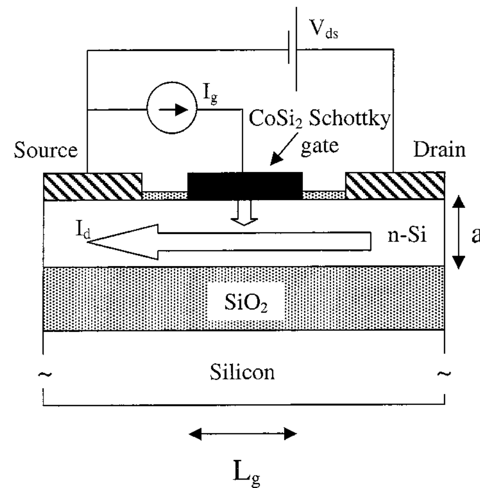

Fig. 1. Cross section of the proposed transistor configuration. Although the modeling has been performed with parameters corresponding to a $CoSi_2$ Schottky gate, any metal or silicide that forms a Schottky contact to silicon could be used.

II. Analytical Derivation of the Current Gain of an SJT

For an FET with a threshold voltage V_{th} and drain bias V_{ds}, the subthreshold current can be written as [2], [3]

$$I_d = I_0 \left[\exp\left(\frac{V_{gs} - V_{th}}{mU_T}\right)\right]\left[1 - \exp\left(\frac{V_{ds}}{U_T}\right)\right] \quad (1)$$

where I_0 is a constant, and $U_T = kT/e$ is the thermal voltage. The parameter m in (1) determines the subthreshold slope of the I_d–V_{gs} curve and is usually close to unity. It is difficult to derive generalized analytical forms for I_0 because it depends upon the choice of boundary conditions at the ends of the channel region. Liang *et al.* [2] have considered the case in which the channel is abruptly terminated by heavily doped source and drain contacts. For a channel of thickness a and uniform doping concentration N_D, they derive $I_0 = \alpha(N_+/N_D a)(W/L_g)\varepsilon U_T^2 \mu$ where α is a constant between 1 and 2, N_+ is the doping concentration in the source and drain contacts, W is the width of the gate, ε is the permittivity of the channel, and μ is the electron mobility. For the SJT geometry shown in Fig. 1, the heavily doped source and drain contacts are some distance from the channel. The appropriate boundary condition for the doping at the ends of the SJT channel is therefore $N_+ \rightarrow N_D$ and for convenience, we

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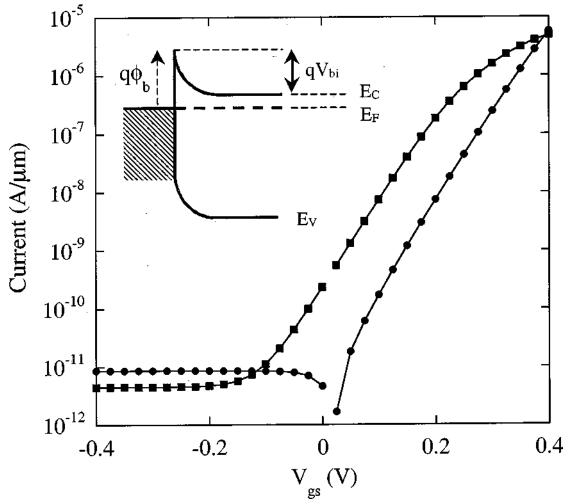

Fig. 2. Drain current (squares) and gate current (circles) as functions of gate voltage for a 0.5 μm gate length SJT with a channel thickness and doping of 70 nm and 3 $\times$ 10^{16} cm^{-3}, respectively. The drain voltage is $V_{ds} = 0.5$ V. This plot resembles the Gummel–Poon plot used to characterize bipolar junction transistors. The inset shows the energy band diagram of a Schottky barrier formed between a metal and an n-type semiconductor.

assume $\alpha N_+/N_D = 1$. As a result $I_0 \approx W\varepsilon U_T^2\mu/aL_g$, and we can rewrite (1) as

$$I_d \approx \frac{W}{aL_g}\varepsilon U_T^2\mu\left[\exp\left(\frac{V_{gs}-V_{th}}{mU_T}\right)\right]\left[1-\exp\left(\frac{V_{ds}}{U_T}\right)\right]. \quad (2)$$

For the current flowing in an ideal Schottky contact, we can write [4]

$$I_g = WL_gA^*T^2e^{-\phi_b/U_T}\left[\exp\left(\frac{V_{gs}}{nU_T}\right)-1\right] \quad (3)$$

where

- ϕ_b Schottky barrier height;
- A^* Richardson constant;
- n ideality factor which can approach unity for a good quality Schottky diode.

The ratio of I_d to I_g gives the current gain β, and assuming that $V_{ds} > 3U_T$ and that $m = n = 1$, we get the result

$$\beta = \frac{I_d}{I_g} \cong \frac{\varepsilon k^2\mu}{aL_g^2q^2A^*}\exp\left(\frac{\varphi_b - V_{th}}{U_T}\right). \quad (4)$$

The difference between the Schottky barrier height and V_{th} can be determined by considering the built-in voltage V_{bi} formed across a metal-semiconductor Schottky barrier as shown in the inset to Fig. 2. By inspection, we see that $q\phi_b = qV_{bi} + (E_C - E_F)$ and the energy difference between the bottom of the conduction band and the Fermi energy can be written as $(E_C - E_F) = kT/\ln(N_C/N_D)$, where N_C is the conduction band effective density of states [4]. The threshold voltage of a MESFET is determined by V_{bi}, the channel thickness and doping concentration, i.e., $V_{th} = V_{bi} - (qN_Da^2/2\varepsilon)$. From these results, we obtain

$$\phi_b - V_{th} = U_T\ln\left(\frac{N_C}{N_D}\right) + \frac{qN_Da^2}{2\varepsilon} \quad (5)$$

and substituting into (5) gives the current gain of the SJT as

$$\beta = \frac{\varepsilon k^2\mu}{aL_g^2q^2A^*}\frac{N_C}{N_D}\exp\left(\frac{qN_Da^2}{2\varepsilon U_T}\right). \quad (6)$$

To obtain an analytical expression for the current gain, several assumptions have been made in the derivation of (6). In particular, the use of (2) assumes that the channel thickness is larger than the Debye length, i.e., $a > L_D = (\varepsilon kT/q^2N_D)^{1/2}$ (see [2], the appendix). For a device in which $a \leq L_D$, the drain current and current gain would both approach zero rather than the $1/a$ singularity suggested by (6). The assumption that $m = n = 1$ has been made to obtain a compact expression for β, but more realistic values can be readily incorporated. The analytical derivation also ignores the two-dimensional (2-D) nature of the current flow indicated in Fig. 1. In a real SJT, the gate current would vary with V_{ds} and there would be a higher current density at the source than at the drain end of the gate. As a consequence, (3) overestimates the current flowing into the gate. To accurately model the device, 2-D simulations are required as described below.

III. Numerical Simulations of the SJT

We have performed numerical simulations of an SJT using Medici [5]. The simulated device uses an SOI substrate with a buried oxide thickness of 0.43 μm and a silicon surface layer of thickness 0.07 μm. The channel is capped with a protective oxide layer. The gate length is 0.5 μm, and the Schottky barrier height is taken to be 0.58 eV, corresponding to $CoSi_2$ [6], [7]. The doping under the source and drain contacts is 10^{20} cm^{-3}, and the distance between them is 0.6 μm. A positive fixed oxide charge of 5 $\times$ 10^{10} cm^{-2} is present at each $Si:SiO_2$ interface [8]. Fig. 2 shows I_d and I_g as a function of gate voltage for a uniform channel doping of $N_D = 3\times10^{16}$ cm^{-3}. Both vary exponentially with V_{gs} over a wide range of currents. For gate voltages greater than ~0.25 V the drain current grows less rapidly as the channel leaves the subthreshold regime. However, for gate voltages in the range $0.05 < V_{gs} < 0.25$ V, the drain current can be controlled over three orders of magnitude while maintaining an approximately constant current gain $\beta > 1$. The current gain is plotted in Fig. 3 as a function of drain current for channels with different doping concentrations. The current gain is not constant, as predicted by (6), in part due to the 2-D nature of the current flow, but also because of the different ideality factors that emerge from the simulations ($m = 1.2$, $n = 1.03$). At high drain currents, the channel is no longer depleted, the exponential variation of I_d with V_{gs} is replaced by a power law dependence, and the current gain falls off quickly. However, below this transition, there is a region of approximately constant current gain that persists for drain currents varying over several orders of magnitude.

To better illustrate the operation of the SJT, Fig. 4 shows contour plots of the free electron concentration and current density at three gate biases ($V_{gs} = 0.05$, 0.2 and 0.4 V) that cover the practical operating range of the device. For $V_{gs} > 0.05$ V, the exponential term in the Schottky diode equation begins to dominate [see (3)] and the device is entering the regime of approximately constant current gain. At $V_{gs} = 0.2$ V the device

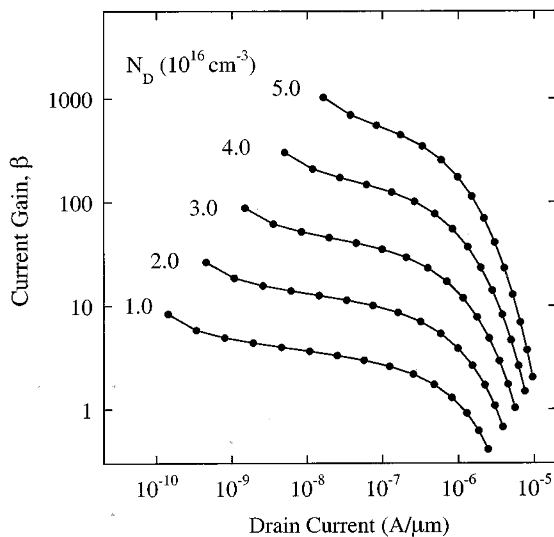

Fig. 3. Current gain β as a function of drain current. The results are derived from a 0.5 μm gate length device with a channel thickness of 70 nm for doping concentrations varying in the range 1–5 $\times$ 10^16 cm^{-3} as shown. $V_{ds} = 0.5$ V.

is within the range of optimal d.c. bias. For $V_{gs} \geq 0.4$ V the drain current is no longer increasing exponentially with V_{gs} and the gate current exceeds the drain current. The contour plots in Fig. 4(a) show the free electron concentration in the range 10^{11} to 10^{20} cm^{-3}. It is evident from these contour plots that for $V_{gs} = 0.05$ and 0.2 V the depletion layer from the gate extends completely across the channel. However, for $V_{gs} = 0.4$ V, the charge begins to accumulate in the channel, especially at the source end where the depletion under the gate is smaller than the channel thickness. When it comes to designing SJTs with different channel thickness, and doping the data in Fig. 4(a) shows that values of N_D and channel thickness need to be chosen such that the channel is partially depleted over the desired range of operating bias.

Fig. 4(b) shows the current density contours for the same gate voltages discussed earlier. For $V_{gs} = 0.05$ and 0.2 V, the current flow is predominantly confined to the lower $Si : SiO_2$ interface and runs parallel to it. Although some gate current is flowing at these biases, it is too small to be resolved in the contour plots. However, for $V_{gs} = 0.4$ V, the gate current is approximately equal to the drain current (see Fig. 2) and the current flow lines are no longer confined to the interface but have an appreciable vertical component. Fig. 4(b)(iii) shows that the majority of the gate current flows into the channel at the source end. This is to be expected because the gate-to-channel potential drop is largest at the source when a positive drain bias is applied.

Fig. 4 confirms that for the intended operating mode of the SJT, the drain current is confined to the buried $Si : SiO_2$ interface. This makes it susceptible to interface charge and interface roughness. The interface charge in SOI wafers is positive and is typically in the range 5–10 $\times$ 10^{10} cm^{-2} [8]. The value used in the simulations is 5 $\times$ 10^{10}, which is on the low side for SOI wafers and perhaps more in line with the values expected for bonded SOI wafers [9]. However, a larger positive interface charge will simply increase the electron concentration at the buried interface, with a corresponding increase in the drain current for a given gate current bias. This increase in I_d can be compensated for by a reduction in the channel thickness and/or doping.

If significant interface roughness scattering occurs at the buried $Si : SiO_2$ interface it will lower the effective channel mobility and degrade subsequent d.c. and r.f. device performance. The simulations described here have used a concentration dependent mobility model appropriate to bulk silicon. For a donor concentration of 3 $\times$ 10^{16} cm^{-3}, the electron mobility is $\sim$900 cm^2/Vs. Hall effect measurements of electron mobility in SIMOX SOI [10] and bonded SOI [11] have shown values comparable to those measured in bulk silicon, which somewhat justifies the constant mobility model used here. However, some additional interface scattering is expected, particularly at low gate bias when a larger proportion of the channel current is confined to the interface. It is worth noting that the additional scattering at the interface will be less than that occurring in a MOSFET. The reason is that interface roughness scattering increases with the perpendicular electric field resulting from the gate bias. The SJT operates under depletion rather than inversion conditions, and the vertical electric field at the buried interface is considerably less than that at the inversion layer of a MOSFET.

To explore the validity of (6), we have extracted the current gain for SJTs of varying channel doping concentration, channel thickness, and gate lengths. The results are shown in Fig. 5. Because β is not strictly constant, we have plotted the current gain obtained for a gate current of 10^{-9} A/μm. This value was chosen because it is in the center of the operating regime of the device. Using a current gain obtained from different gate current biases gives similar results. Fig. 5(a) plots β as a function of N_D for a device with a gate length of 0.5 μm. The solid line is a fit to (6) in the form $\beta \propto (1/N_D)\exp(C_1 N_D)$, where C_1 is a constant that is predicted to be $qa^2/2\varepsilon U_T$. At room temperature, and for a channel thickness of 70 nm, $C_1 = 1.46 \times 10^{-22}$ cm^3 which is the value used to fit the data. A reasonable fit to the numerical data is obtained, except at the lowest channel doping concentrations. For $N_D = 10^{16}$ cm^{-3}, the Debye length of 412 Å is approaching the channel thickness, and the assumptions made in the derivation of (6) are no longer valid as discussed previously.

The current gain as function of channel thickness a is shown in Fig. 5(b) for $N_D = 3 \times 10^{16}$ cm^{-3} and $L_g = 0.5$ μm. This time, the solid line represents a fit to (6) in the form $\beta \propto (1/a)\exp(C_2 a^2)$, where $C_2 = qN_D/2\varepsilon U_T = 9 \times 10^{14}$ m^{-2}. The data from the numerical simulations are increasing somewhat faster than that predicted by (6). However, the agreement with the analytical expression is reasonable, given the assumptions made in its derivation.

In Fig. 5(c), we plot β as a function of L_g. Equation (6) predicts a $\beta \propto L_g^{-2}$ dependence, which is shown as a solid line in the figure. The variation of β with L_g appears to be approaching an L_g^{-2} asymptote for long gate lengths but grows faster than an inverse quadratic for $L_g < 0.8$ μm. We attribute this discrepancy to a reduced effective channel length due to depletion from the positively biased drain [2]. This is analogous to base width narrowing in a BJT and channel length modulation in an FET. For long gate lengths, the extra depletion at the drain end is insignificant, and the expected L_g^{-2} dependence is recovered. The

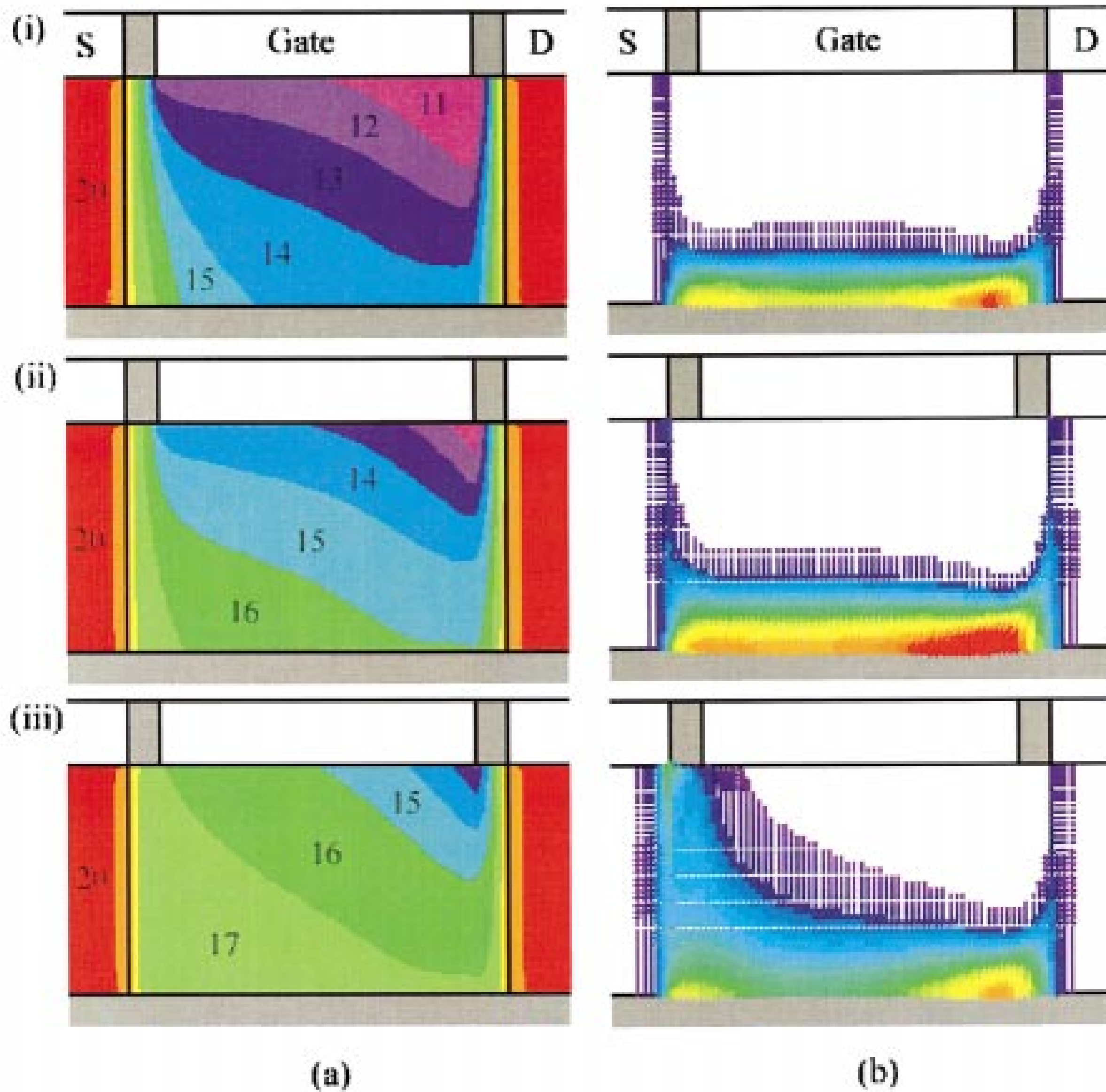

Fig. 4. Contour plots showing (a) free electron concentration N_e and (b) current density flow lines for gate biases of (i) 0.05 V, (ii) 0.2 V, and (iii) 0.4 V. For the electron concentration plots in (a), $\log_{10}(N_e)$ is indicated. For the current density flowlines in (b), the maximum current densities indicated in red correspond to (i) >15 A/cm^2, (ii) >1400 A/cm^2, and (iii) >40 kA/cm^2.

additional depletion is expected to be smaller for smaller drain biases, and the data in Fig. 5(b) at a drain bias of 0.1 V does indeed follow the expected behavior more closely than for the case of $V_{ds} = 0.5$ V. Overall, the agreement between the results from the numerical simulations and those predicted from (6) is very good. This gives us confidence that the essential physics of the operation of the SJT is accurately described by the analytical derivation.

In Fig. 6, we plot the drain current as a function of drain voltage for different gate input currents, i.e., the SJT family of curves. For subthreshold channel conduction, the drain current saturates for drain voltages greater than $3U_T$ [12]. This behavior can be seen in Fig. 6, where the "knee" in the output characteristics occurs for $V_{ds} < 0.1$ V. The finite output resistance in saturation is another manifestation of the channel length reduction as V_{ds} is increased.

An important measure of the high-frequency performance of a transistor is its cutoff frequency f_T, i.e., the frequency at which the gain is unity. The cutoff frequency can be written as $f_T = g_m/2\pi C_g$, where g_m is the transconductance, and C_g is the total gate capacitance given by the sum of gate-source, gate-drain, and gate-substrate capacitances [12]. Both C_g and g_m can be extracted by using Medici to perform a small-signal analysis of the SJT. The results are plotted in Fig. 7 for a device with a gate length of 0.5 μm. The gate capacitance, shown in Fig. 7(a), varies by only a factor of ~3 over the entire operating range of the device. The transconductance varies approximately linearly with $I_d (g_m \approx I_d/U_T)$, as shown in Fig. 7(b). The cutoff frequency derived from g_m and C_g is shown in Fig. 7(c) and approaches 10 GHz for this 0.5 μm gate length device. Considerably higher values of f_T can be expected for devices with shorter gate lengths.

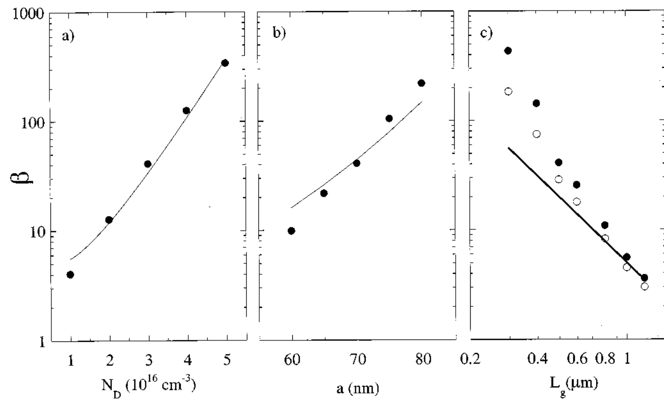

Fig. 5. (a) Current gain for an SJT with channel thickness of 70 nm as a function of channel doping for a gate length of 0.5 μm with $V_{ds} = 0.5$ V. The solid line is a fit to (6). (b) Current gain as a function of channel thickness a for $N_D = 3 \times 10^{16}$ cm^{-3} and $L_g = 0.5$ μm. The solid line is a fit to (6). (c) Current gain as a function of gate length for a channel doping of 3 × 10^{16} cm^{-3} and drain bias of 0.5 V (solid circles) and 0.1 V (open circles). The solid line in is a guide for the eye showing the L_g^{-2} behavior expected from (6).

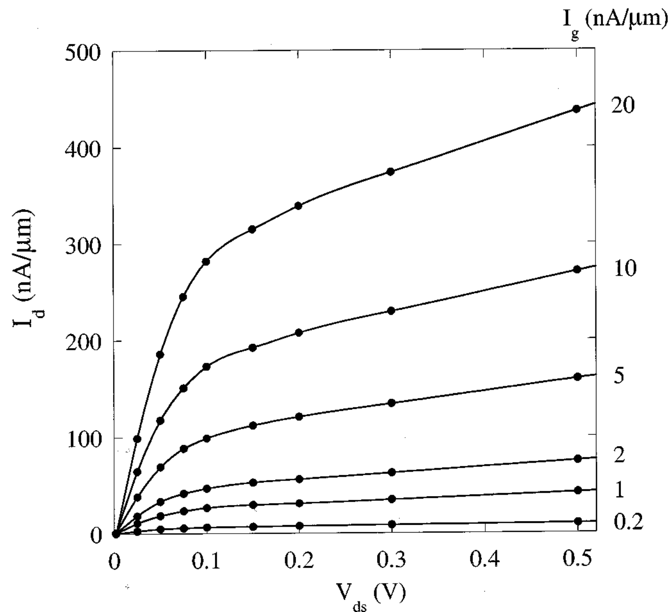

Fig. 6. Drain current for a 0.5 μm gate length device versus drain voltage as a function of gate input current; channel thickness $a = 70$ nm and doping concentration $N_D = 3 \times 10^{16}$ cm^{-3}.

IV. Possible Applications of the SJT

From the results of the numerical simulations given earlier, the SJT is clearly a very low power device that would be well suited to micropower circuit applications. Micropower circuits such as those used in digital watches and medical implant applications, including pacemakers and artificial cochlea, use a subthreshold CMOS technology based on weakly inverted MOSFETs [13]. Although capable of very low power operation, these circuits are limited to operating frequencies below a few MHz because of the relatively low cutoff frequency of a weakly inverted MOSFET. Below threshold, the maximum possible cutoff frequency of a MOSFET can be written as [12]

$$f_T = \frac{\mu U_T}{2\pi L_g^2}. \quad (6)$$

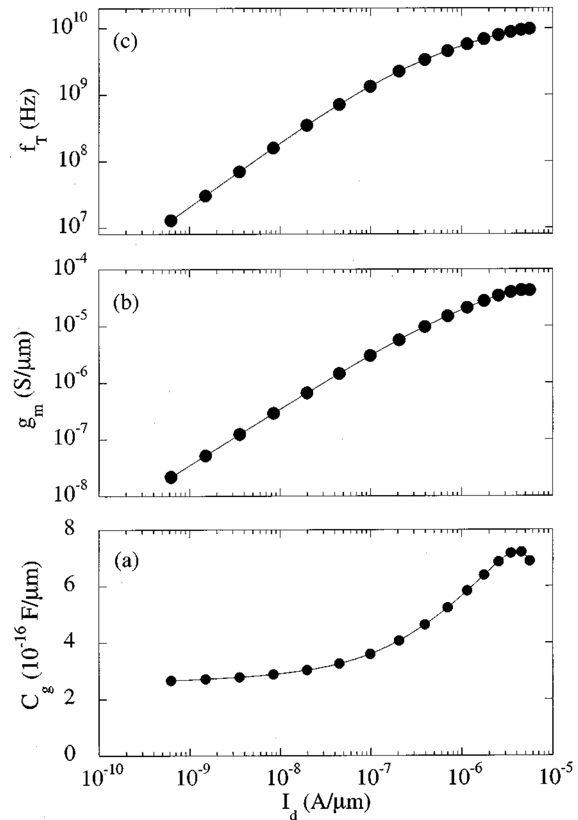

Fig. 7. (a) Gate capacitance, (b) transconductance, and (c) cutoff frequency of a 0.5 μm gate length SJT as a function of drain current ($V_{ds} = 0.5$ V, $a = 70$ nm and $N_D = 3 \times 10^{16}$ cm^{-3}).

The electron mobility in a weakly inverted MOSFET is ~200 cm^2/Vs [14] (about three times smaller than the case of a strongly inverted MOSFET) and for a 1 μm gate length device, we get $f_T \sim 80$ MHz. It is not practical to increase the cutoff frequency by reducing the gate length because of problems with transistor matching in the subthreshold regime [13]. Below threshold, the drain current of a MOSFET varies exponentially with threshold voltage. As L_g is decreased, the statistical variations in the threshold voltage ΔV_{th} tend to increase, leading to excessive variations in I_d. For this reason, state-of-the-art micropower circuits typically use gate lengths $L_g > 1$ μm and operate at frequencies below 1 MHz [15].

The numerical simulations of the SJT suggest that it may be more suited to high-frequency micropower circuits than weakly inverted MOSFETs. This is because the SJT has a higher cutoff frequency than a MOSFET with the same gate length conducting the same drain current. The higher cutoff frequency is due in part to the higher mobility of the lightly doped channel, which would typically be 800–1000 cm^2/Vs compared to ~200 cm^2/Vs for a weakly inverted MOSFET. Also significant is the smaller capacitance of a Schottky diode compared to the oxide capacitance of an equivalent MOS structure. For example, a 0.5 × 1.0 μm^2 MOS capacitor with a 10 nm oxide, biased into strong inversion, has a capacitance of ~17 × 10^{-16} F (neglecting fringing fields). This value would be expected to fall by about one half when biased into the weak inversion regime. In contrast, as shown in Fig. 7(a), the gate capacitance (*including* fringing fields) of the SJT is less than

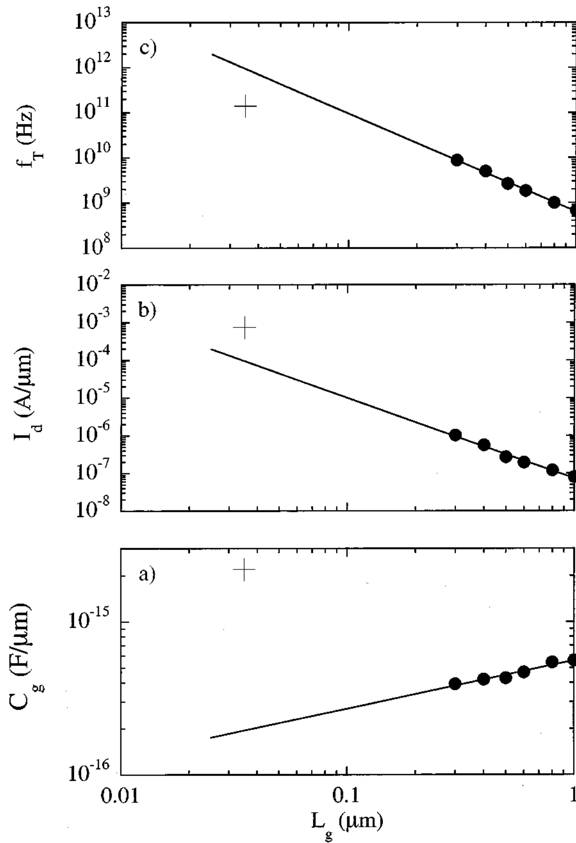

Fig. 8. Gate capacitance, saturated drain current, and cutoff frequency as a function of gate length for $V_{ds} = 0.5$ V. The solid lines are power law fits (derived from the numerical simulations of a channel of thickness 70 nm and doping concentration 3×10^{16} cm^{-3}) extrapolated to the deep submicron regime. The crosses are the corresponding data from the ITRS Roadmap.

8×10^{-16} F over its entire operating range. The capacitance of a Schottky gate scales inversely with the depletion length L_{dep}, while that of a MOSFET scales inversely with the oxide thickness T_{ox}. For most practical cases, $L_{dep} > T_{ox}$ and the capacitance of the Schottky gate will be less than that of the MOS structure, even after the difference in relative permittivity is taken into account.

An interesting feature of the SJT is the cancellation of terms in V_{th} from the expression for the current gain [see (6)]. This means that when the SJT is biased with a gate current rather than a gate voltage, the magnitude of the current gain is less susceptible to device fluctuations that would otherwise lead to unacceptable variations in the threshold voltage. The reason for this can be understood by considering the effect that a small change in Schottky barrier height would have on I_d and I_g. Both currents vary as $e^{-\phi_b/U_T}$ and hence, a small change in barrier height will lead to the same relative change in I_d and I_g, and the current gain is unaffected. Of course, β is a strong function of device parameters such as channel thickness a, channel doping N_D, gate length L_g, and interface charges [see (6) and Fig. 5(a)]. However, these parameters can be controlled with great precision and it should be possible to fabricate well-matched SJTs with submicron gate lengths. Fig. 7 shows that such devices might be expected to have cutoff frequencies exceeding 10 GHz. Although dynamic power consumption will be important at such high frequencies, SJT-based micropower circuits may be able to operate at frequencies that are orders of magnitude higher than those currently obtainable.

Another possible application of SJTs is for digital logic using deep submicron devices. The International Technology Roadmap for Semiconductors (the ITRS Roadmap) identifies the device performance required to continue the current CMOS scaling trends to devices with gate lengths of 35 nm [16]. The performance targets are very challenging, and some of the hardest obstacles to be overcome are associated with the very thin gate oxides that will be required. Being a Schottky barrier device, the SJT does not depend on a gate oxide for its operation, making it a possible contender for ULSI integration beyond the 35 nm node. In an attempt to assess the likely performance of short gate length SJTs, we have taken the results derived from relatively long devices and extrapolated them to the deep submicron regime using a power-law fit to the data (see Fig. 8). Two of the most important performance indicators are the gate capacitance and saturated drain current as these determine the time it takes to switch the next gate stage. Consider a simple inverter that is loaded by another identical inverter. During the switching transition, the inverter can be modeled as a conductance $g = eI_0/kT$ where I_0 is the drain current flowing when both transistors are on [17]. This conductance charges the capacitance of the inverter load so that the switching time $\tau \propto C_g/g$. For fast switching times, we therefore require small capacitance and large drain current. The gate capacitance varies with device bias [see Fig. 7(a)] and to make a comparison between devices with different gate lengths we plot the value of C_g for a constant gate current density of 20 nA/μm^2 [see Fig. 8(a)]. This is the gate leakage current observed in ultra-scaled MOS devices with an oxide thickness of 1.4 nm [18]. When the power-law fit is extrapolated to gate lengths of 35 nm the gate capacitance is $\sim 2 \times 10^{-16}$ F/μm. This compares favorably to the value of $\sim 2 \times 10^{-5}$ F/μm from the ITRS Roadmap at the 35 nm node. The reason for the smaller gate capacitance of the SJT is that it is due to the depletion capacitance of the underlying semiconductor, which is invariably smaller than the oxide capacitance of an MOS capacitor with a thin gate oxide.

Although attractive for high frequency operation, a small gate capacitance is of little value for digital logic unless it is accompanied by a sufficient current-drive capability. In Fig. 8(b), we show the saturated drain current as a function of gate length. Again, the results are plotted for a constant gate current density of 20 nA/μm^2. When the power law fit is extrapolated to devices with a gate length of 35 nm we get a current drive of $\sim$0.1 mA/μm, which is smaller than the ITRS Roadmap projection of 0.75 mA/μm for n-channel devices. However, because of the smaller input capacitance of the SJT, a current drive of 0.1 mA/μm will allow each stage in an SJT inverter chain to switch in less than 100 femtoseconds. Finally, for completeness, we show in Fig. 8(c) the cutoff frequency as a function of gate length, and its extrapolation to the 35 nm node. The maximum cutoff frequency exceeds that required by the ITRS Roadmap by almost an order of magnitude. This suggests that the switching time of the inverter discussed above will not be limited by the intrinsic switching speed of the SJT.

It is worth pointing out here that any conclusions drawn from the extrapolated data shown in Fig. 8 must be treated with some caution. While reducing the gate length, the only parameter that has been scaled proportionally is the gate current. Many other parameters will have to be considered before accurate scaling predictions can be achieved. In particular, it will be necessary to reduce the channel thickness, a, to mitigate short channel effects. This in turn will require increased channel doping such that the product aN_D^2 remains unchanged to keep the current gain constant [see (6)].

Another issue that will have to be addressed in the deep submicron regime is the accuracy of the transport models used for the simulations. The extrapolations in Fig. 8 are based on data that has been derived using a drift-diffusion transport model. For subthreshold devices with $L_g > 0.3$ μm, a drift-diffusion approach is adequate because the dominant transport mechanism in the subthreshold regime is carrier diffusion [12]. However, for the very short gate lengths indicated in Fig. 8, more advanced simulations based on hydrodynamic models may be required.

V. Summary and Conclusions

This paper has described numerical simulations of a new subthreshold device, the Schottky Junction Transistor. The results for a device with a 0.5 μm gate length suggest that cutoff frequencies approaching 10 GHz can be achieved, making the SJT ideally suited for radio frequency (rf) micropower analog circuit applications. Extrapolation of the data to gate lengths of 35 nm suggests that the SJT would also satisfy the requirements of the ITRS Roadmap for sub-100 nm CMOS, but without the need for ultra-thin gate oxides. Although such extrapolations must be treated with some caution, they do illustrate the intriguing ULSI possibilities of this new device configuration.

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