

A Low Jitter, Consumer/Professional Digital Audio Interface

PRECIS

This paper describes a new digital audio interface specification, called the *I²S•e* interface, which is designed for the purpose of interconnecting consumer and professional digital audio products with very low Jitter clock recovery for precise digital to analog conversion.

The most common digital audio interface today is the S/PDIF (Sony / Philips Digital Interface). The S/PDIF cleverly utilizes biphasemark encoding techniques to reduce the number of cable conductors to one, thereby offering a very efficient means of inter-connecting two digital audio products. However, when transmitted through a real-world band limited cable and circuitry, the biphasemark encoded signal is susceptible to crosstalk from the data portion to the clock. The clock that is recovered from the received digital audio signal will therefore possess jitter that is related to the audio data signal. Since this clock is used to perform the subsequent digital to analog conversion there will be timing errors in the conversion that will result in voltage errors in the recovered analog signal that are related to the audio signal itself, thereby resulting in jitter-induced distortion.

I²S•e

The interface solves this problem by transmitting the clock and data signals along separate conductors. A protocol very similar to the Philips 12S bus is used for audio data and clocks while the complete channel status and user bits are transmitted separately. In addition, the *I²S•e* allows the master dock to be generated in the receiving product with the transmitting product operating as a slave. Full compatibility with various consumer and professional products is achieved. For example, both 384xFs and 256xFs based CD (or DVD) players are compatible. Sampling frequencies of today's 32k, 44.1k, 48k products as well as the future 88.1k and 96k rates are allowed. The transmission cable is specified as the 13W3 which contains 3 coax conductors and 5 twisted pair conductors. Motorola PECL high speed driver/receiver technology is specified to achieve clock dsetime speeds on the order of 1 nanosecond.

There are 2 levels of implementation: Level 1 and Level 2. Products complying with Level 1 will result in the best jitter performance while Level 2 offers a simpler implementation. In the Level 1 implementation the Master Clock, for the digital to analog conversion that occurs in the receiver, is generated by the receiver and is transmitted to the transmitter. In Level 2 the Master Clock is generated in the transmitter and is transmitted to the receiver. Both levels offer a significant improvement in jitter performance relative to the widely used S/PDIF format (and its close relatives AES3, ANSI S4.40, [EC 958, EIAJ CP-340) which use biphasemark encoding to combine the clock and audio data into one serial signal. All products conforming to this specification must implement the Level 2 requirements; the Level 1 requirements are optional. When a Level 1 transmitter is connected to a Level 2 receiver (or vice-versa) the transmitter and receiver will automatically operate in Level 2 mode. When a Level 1 transmitter is connected to a Level 1 receiver the system will automatically operate in Level 1 mode. Thus the components are capable of sensing and operating at the highest level of performance attainable without the need for user switches or jumper adjustments. True 'plug and play' operation is achieved for any two *I²S•e* products to operate.

The *I²S•e* interface allows for a complete transmission of the channel status and user bits commonly transmitted in today's equipment utilizing the S/PDIF, AES/EBU, and related standards. This is accomplished by including, as a subset of the 12S - e specification, a biphasemark signal that carries the entire channel status and user bits of today's consumer and professional serial interface (S/PDIF, AES/EBU, etc.). Thus the *I²S•e* not only transmits the preemphasis status, but other important information such as the consumer copy-protect bit and various bits to further extend the 12S - e capabilities to include professional products and multiple sampling rates, including the imminent 88k Hz or 96k Hz sample rates. Although theoretically the addition of the biphasemark signal complicates the circuitry by requiring encoding and decoding of the biphasemark signal, pragmatically this circuitry is presumed to already exist in the products to allow compatibility with the multitude of non- 12S - e products. Thus this biphasemark channel status and user information is transmitted and received using existing, and otherwise dormant, circuitry.

To date, a Level 2 product combination of CD player and DAC has been produced and the jitter performance measured at the digital to analog converter word clock; improvements over the standard SPDIF of 6:1 have been documented for well implemented S/PDIF; for typical S/PDIF implementations the jitter is improved 10:1. It is expected that a Level 1 combination would yield even more attractive numbers.

The **I²S•e** interface can be implemented in products demanding the best performance possible, particularly in audio playback devices that incorporate a digital to analog conversion. The circuitry required to implement a level 2 product is minimal and results in a significant improvement in the recovered clock jitter performance.

I²S • *Enhanced*

Digital Audio Interface

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ULTRANALOG, INC.

1075A Serpentine Lane
Pleasanton, CA

Tel: (510) 485-9550 Fax: (510) 485-9565

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1. Scope

This specification describes a low jitter interface between two digital audio products such as a consumer transport (CD or DVD) and processor (digital to analog converter) or between the various professional recording and broadcast products. There are 2 levels of implementation: Level 1 and Level 2. Products complying with Level 1 will result in the best jitter performance while Level 2 offers a simpler implementation. In the Level 1 implementation the Master Clock, for the digital to analog conversion that occurs in the processor, is generated by the processor and is transmitted to the transport. In Level 2 the Master Clock is generated in the transport and is transmitted to the processor. Both levels offer a significant improvement in jitter performance relative to the widely used S/PDIF format (and its close relatives AES3, ANSI S4.40, IEC 958, EIAJ CP-340) which use biphasemark encoding to combine the clock and audio data into one serial signal. The *I²S•e* standard transmits the clocks and data separately thereby eliminating the inherent data to clock crosstalk of the biphasemark encoding scheme.

All products conforming to this specification must implement the Level 2 requirements; the Level 1 requirements are optional. When a Level 1 transport is connected to a Level 2 processor (or vice-versa) the transport and processor will automatically operate in Level 2 mode. When a Level 1 transport is connected to a Level 1 processor the system will automatically operate in Level 1 mode. Thus the components are capable of sensing and operating at the highest level of performance attainable without the need for user switches or jumper adjustments. In addition both 256x Fs and 384x Fs based Master Clock systems are permitted. True 'plug and play' operation is achieved with any transport / processor combination conforming to this specification.

Throughout this document the term 'transmitter' will refer to a product (such as a transport) that is a source of digital audio and thus provides an *I²S•e* output; likewise the term 'receiver' will refer to a product that has an *I²S•e* input and digital to analog conversion.

2. References

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- [4] Philips Semiconductors Audio / Radio Handbook, "Bus Specification", 1993.
- [5] Halverson, Kevin, "The 13W3 ", Muse Electronics, Inc., 1997.
- [6] Audio Engineering Society, INC., AES3-1992, "AES Recommended Practice for Digital Audio Engineering - Serial Transmission Format for Two-Channel Linearly Represented Digital Audio Data", 1992 (AES serial interface specification).
- [7] International Electrotechnical Commission, IEC-958 "Digital Audio Interface", 1985.
- [8] Standards of Electronic Industries Association of Japan, EIAJ CP-340 "Digital Audio Interface", 1989.

3. Background

The most common digital audio interface today is the S/PDIF (Sony / Philips Digital Interface). The S/PDIF cleverly utilizes biphasemark encoding techniques to reduce the number of cable conductors to one, thereby offering a very efficient means of inter-connecting two digital audio products. However, when transmitted through a real-world band limited cable and circuitry, the biphasemark encoded signal is susceptible to crosstalk from the data portion to the clock [1], [2],[3]. The clock that is recovered from the received digital audio signal will therefore possess jitter that is related to the audio data signal. Since this clock is used to perform the subsequent digital to analog conversion there will be timing errors in the conversion that will result in voltage errors in the recovered analog signal that are related to the audio signal itself, thereby resulting in jitter-induced distortion.

The bus specification [4] was developed by Philips Semiconductors as a means to transfer sound data between integrated circuits. This interface is commonly used in compact disc and various other audio products. The bus uses 3 signal lines to transmit the audio data from one IC to another; serial clock, word select, and serial data. In this, and other publications, these signals are often referred to as bit clock, word clock, and data. The fact that the data is transmitted on a separate line from the bit and word clocks makes this protocol resistant to data-to-clock crosstalk, which is a shortcoming of the common inter-product formats such as S/PDIF, AES/EBU, and the others mentioned in section 1. Since many integrated circuits are available that use the protocol it makes sense to extend the usage from inter-IC-sound to inter-product-sound. This idea is not novel; there have been high-end CD transport and processor manufacturers that have used this approach for quite some time. The problem, however, is that no universal standard has been established to allow compatibility between products of different manufacturers.

In early 1997 Kevin Halverson of Muse Electronics, Inc. proposed such a format, named the 13W3 [5]. One of the key features of this proposal is the usage of the 13W3 cable which includes 3 coax and 5 twisted-pair lines. While this cable was designed for the computer industry to transmit component video and control signals, Kevin has shown that it is well suited for the task of audio inter-product communication. However, the 13W3 fell short as far as allowing universal compatibility with all compact disc transports, specifically concerning the transport's internal Master Clock frequency. Some transports use a $256x F_s$ clock and others use a $384x F_s$ clock (where F_s is the audio sample frequency, usually 44.1k Hz). The 13W3 allows for $256x F_s$ transports but not the $384x F_s$ based transports. Another shortcoming of the 13W3 is that it specifies 4 variations (Level 1, Level 2, Level 3A, and Level 3B) but these variations are not necessarily compatible with each other; that is to say a Level 3B processor may not be compatible with a Level 1 transport thus creating compatibility issues in the field.

The *I²S•e* interface combines the protocol of the Phillips with the 13W3 cable to generate a specification that is compatible with both $256x F_s$ and $384x F_s$ transports, has only 2 levels of implementation (both of which are compatible with each other), and utilizes Motorola PECL high speed driver/receiver technology to achieve clock risetime speeds on the order of 1 nanosecond. Products manufactured to the *I²S•e* specification are truly 'plug-and-play'; no user-selectable jumpers or switches are required for any two *I²S•e* products to operate.

In addition the interface allows for a complete transmission of the channel status and user bits commonly transmitted in today's equipment utilizing the S/PDIF, AES/EBU, and related standards [6], [7], [8].

This is accomplished by including, as a subset of the *I²S•e* specification, a biphasemark signal that carries the entire channel status and user bits of today's consumer and professional serial interface (S/PDIF, AES/EBU, etc.). Thus the *I²S•e* not only transmits the preemphasis status, but other important information such as the consumer copy-protect bit and various bits to further extend the capabilities to include professional products and multiple sampling rates, including the imminent 88k Hz or 96k Hz sample rates. Although theoretically the addition of the biphasemark signal complicates the circuitry by requiring encoding and decoding of the biphasemark signal, pragmatically this circuitry is presumed to already exist in the products to allow compatibility with the multitude of non- products. Thus this biphasemark channel status and user information is transmitted and received using existing, and otherwise dormant, circuitry.

The use of a biphasemark decoder in the processor offers another advantage when considering the fact that the receiver must determine the sample clock rate (32k, 44.1k, 48k, etc.). The simple solution is to use the frequency detector inherent in the biphasemark decoder (PLL) to provide a sample rate indication to the processor clock circuitry.

Although the *I²S•e* interface is designed to allow multiple sampling rates (32k, 44.1k, 48k, 88.2k, 96k) it is not required for all products to include all of the rates; it is presumed that the products will include only those sample rates deemed appropriate for the market that it serves.

4. Interface Format

4.1 Level 2 (minimum requirement)

The Master Clock (either 256x F_s or 384x F_s) is generated by the transmitter. The transmitter transmits the following signals to the receiver using the cable and connectors specified in section 6.0:

- Master Clock: Frequency = 256 (or 384) x sample clock frequency
- Word Clock: Frequency = sample Clock frequency
- Bit Clock: Frequency = 64 (or 48) x sample clock frequency
- Data:Left and Right Audio data
- Channel Status: Biphasemark encoded
- Clock Flag: Logic 0 = transmitter Master Clock frequency = 256 x F_s ,
Logic 1 = transmitter Master Clock frequency = 384 x F_s

For specific Channel Status and User information refer to [6], or [7], or [8]. Both Professional and Consumer bits are incorporated. The audio signal may be transmitted along with the Channel Status and User bits in the biphasemark signal. Thus the signal transmitted could very well be an S/PDIF or AES3 signal as far as the biphasemark encoding is concerned; the difference between this signal and a true S/PDIF or AES3 is in the voltage levels and connector type. The clock and audio data recovered in the receiver biphasemark decoder are ignored by the receiver.

The receiver sends no signal to the transmitter.

4.2 Level 1 (optional)

The Master Clock (either 256x F_s or 384x F_s) is generated in the receiver and is used to provide a low jitter reference for the digital to analog conversion. In addition this frequency is divided to 64x F_s and transmitted to the transmitter as the Slave Clock. The transmitter (if it is a Level 1 device) will phase-lock to the Slave Clock signal to generate either 256x F_s or 384x F_s as desired for internal usage. If the transmitter is a Level 2 device it ignores the Slave Clock transmitted by the receiver, however, it is required that all Level 2 transmitters provide a proper termination for the Slave Clock. A Level 1 receiver is required to implement a simple FIFO buffer to allow the transmitter Bit Clock, Word Clock, and Data transitions to be of arbitrary phase with respect to the receiver clocks. Contact UltraAnalog, Inc. at (510) 485-9550 for additional support information.

4.3 Automatic Configuration

4.3.1 Requirements

In order to ensure 'plug and play' compatibility between both level (1 and 2) products the Master Clock, Slave Clock, and Clock Flag signals are used to allow the transmitter and receiver to determine and implement the highest level of performance that the particular transmitter / receiver combination will allow.

Clock Flag (Pins 1 and 6): This signal is generated by the transmitter and used by the receiver to configure its internal circuitry (i.e.: digital filter) to use a 256xFs clock or 384xFs clock.

Clock Flag = 0 indicates Master Clock freq = 384xFs

Clock Flag = 1 indicates Master Clock freq = 256xFs

Slave Clock (Pin A1): This signal is only generated by Level 1 receivers. It consists of a constant clock of frequency = 64xFs. In addition to providing the transmitter with a clock reference the very presence of this signal serves as a request to the transmitter to operate in Level 1. When a Level 1 transmitter detects the presence of this clock it is required to phase-lock to it. A Level 2 transmitter ignores the Slave Clock signal, however, it does terminate A1 properly. All Level 1 receivers must power up in a mode that transmits the Slave Clock to the transmitter.

Master Clock (Pins A2 and A3): This signal is generated by Level 1 and Level 2 transmitters but is not active if a Level 1 receiver is connected (as determined by the presence of a Slave Clock). When a Level 1 transmitter senses the presence of (and phase-locks to) the Slave Clock input it is required to inhibit the Master Clock output to the receiver within 5 seconds. This serves as an indicator to the receiver that a Level 1 transmitter is connected and the receiver can now switch over to its internal clock. Level 1 receivers are required to use the transmitter generated Master Clock until the receiver senses the loss of Master Clock.

A Level 1 receiver is required to poll the transport (by activating the slave clock as described above) at power-up after it senses the presence of a transmitter clock. It is also suggested (although not required) that the Level 1 processor poll the transport after a momentary loss of $128 \cdot e$ clocks from the transmitter. If the processor does not sense a Level 1 transmitter within 5 seconds of sensing a transport clock then the receiver can conclude that a Level 2 transport is connected. It is suggested (although not required) that Level 1 processors disable the internal clock oscillator when not connected to a Level 1 transport.

4.3.2 Examples

Assume a Level 2 transmitter is connected to a Level 1 receiver. The transmitter and receiver start (by default) both in Level 2, but the receiver (being Level 1) transmits the Slave Clock to the transmitter. Since the transmitter is only capable of Level 2 performance it ignores the Slave Clock and continues to transmit the Master Clock. The receiver, in turn, senses that the Master Clock persists and thus remains in Level 2 mode.

Assume a Level 1 transmitter is connected to a Level 1 receiver. The transmitter and receiver start at power-up (by default) both in Level 2, but the receiver transmits the Slave Clock to the transmitter. The transmitter senses the presence of the Slave Clock and achieves successful phase-lock to the receiver. Then the transmitter inhibits the Master Clock transmission to the receiver. The receiver then senses that the Master Clock is gone and changes to Level 1 resulting in the optimum jitter performance for the system.

In both of the above examples the transmitter sets the Clock Flag according to its internal clock (either 256xFs or 384xFs). However, when a receiver is operating in Level 1 mode it must ignore this flag since it is using an internal clock.

5.0 Interface Signal Timing

The timing diagram shown in figures 5.1 and 5.2 are valid for both Level 1 and Level 2 devices.

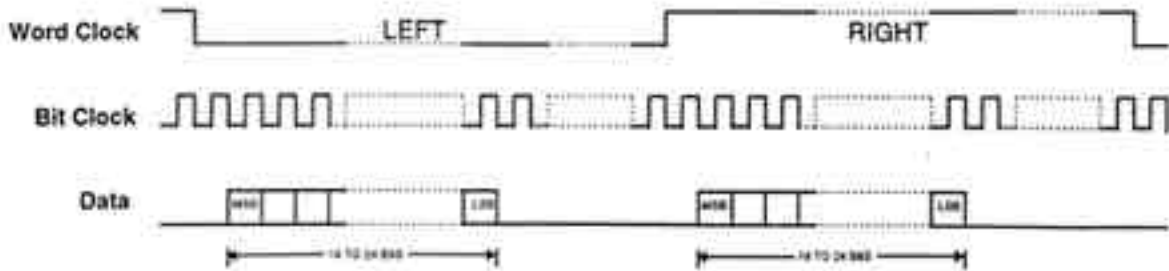


Figure 5.1

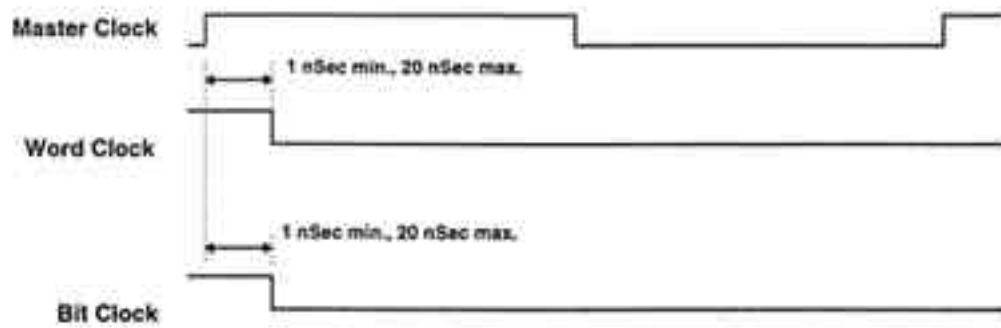


Figure 5.2

6.0 Interface Electrical and Mechanical Characteristics

6.1 General

The signals are transmitted using a single 13W3 cable between the transmitter and receiver. The 13W3 connector consists of three 75 Ω coaxial transmission lines (referred to as A1, A2, and A3) and 5 twisted-pair 110 Ω cables (referred to as pins 1 through 10).

The Slave Clock (optional) is transmitted from the receiver to the transmitter in a single-ended configuration using the A1 75 Ω transmission line.

The Master Clock is transmitted from the transmitter to the receiver in a balanced configuration using two 75 Ω coaxial transmission lines. The + phase of the Master Clock is transmitted on A2 while the - phase of the Master Clock is transmitted on A3.

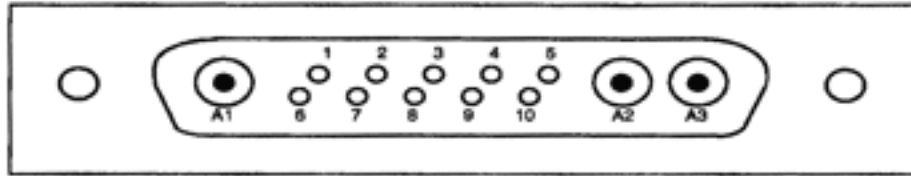
The Bit Clock, Word Clock, Data, and Channel status signals are transmitted from the transmitter to the receiver in a balanced configuration using 4 of the 110 Ω twisted-pair transmission lines.

The Clock Flag is transmitted as single-ended signal with CMOS compatible levels using the remaining twisted-pair line. The driver for this signal must be able to source 10 mA so as to be compatible with receivers that use an input opto-coupler device.

The 13W3 outer foil shield is connected to chassis ground at both ends.

6.2 Connector Pin Assignment

The 13W3 (also known as 13C3) female connector is shown below. Both transmitter and receiver use the female (receptacle) connector. Both ends of the cable are male and mate to the connector shown here.



- A1:Slave Clock
- A2:Master Clock +
- A3:Master Clock -
- Pin 1:Clock Flag
- Pin 6:Transmitter Digital Ground
- Pin 2:Word Clock +
- Pin 7:Word Clock -
- Pin 3:Data +
- Pin 8:Data -
- Pin 4:Channel status & user bits +
- Pin 9:Channel status & user bits -
- Pin 5:Bit Clock +
- Pin 10:Bit Clock -

6.3 Transmitter Circuit Requirements

It is required to use the Motorola PECL driver, part number MC10H352 or equivalent as the transmitter drivers for the Master Clock, Bit Clock, Word Clock, Data, Channel status, and Slave Clock (if implemented). The Master Clock is ac coupled, the others are dc coupled. A source impedance of 75 Ω (+-1%) is required for the three coax signals. A source impedance of 110 Ω (+-1%) (54.9 Ω on each pin) is required for the Bit Clock, Word Clock, Channel status, and Data signals. Contact UltraAnalog, Inc. at (510) 485-9550 for more specific schematic requirements.

If the Slave output feature is not implemented then the A1 coax is not connected at the receiver end.

The Clock output must be a CMOS compatible level and capable of driving 10mA for compatibility with receivers that use opto-coupling for isolation. In addition the Clock Flag (pin 1) must have a 100 Ω series resistor at the transmitter side for protection.

6.4 Receiver Circuit Requirements

It is required to use the Motorola PECL receiver, part number MC10H350 or equivalent as the receiver for the Master Clock, Bit Clock, Word Clock, Data, Channel status, and Slave Clock (if implemented). The A1, A2, and A3 connectors will be terminated with a 75 Ω (+-1%) resistor. The Word Clock, Bit Clock, Channel status, and Data twisted-pair signals will be terminated with 110 Ω (+-1%) resistor. These signals are received in a balanced mode with a differential receiver for each signal; the MC10H350 consists of 4 differential receivers. Contact UltraAnalog, Inc. at (510) 485-9550 for more specific schematic requirements.

If the Slave input feature is not implemented then the transmitter must still terminate the A1 cable into 75 Ω .

6.5 Isolation circuits

For the more robust implementations isolation components (pulse transformers and opto-couplers) can be used, presumably only at the receiver end. It is not necessary to use such components at both ends of the cable.

licensing or royalty fees are required to design, manufacture, and / or sell equipment conforming to this specification.

For a nominal fee UltraAnalog, Inc. will test products for conformity to this specification.

UltraAnalog, Inc. will publish a list of products that have been tested and conform to the specification.

) Acknowledgments

This specification represents the culmination of work performed over several years, by many individuals, in many parts of the world, all with the common purpose of improving the science and art of audio reproduction. In addition to those individuals cited in the references section of this document the author of this specification would like to acknowledge the following individuals who contributed directly to the generation of the specification: Peter Schut of Axon Digital Design B.V., Chris Johnson of Sonic Frontiers, Inc., and John Ferguson of UltraAnalog, Inc.

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