TECHNOLOGICAL INNOVATION IN THE SEMICONDUCTOR INDUSTRY: A CASE STUDY OF THE INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS (ITRS)

by

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A Dissertation
Submitted to the Graduate Faculty
of
George Mason University
In Partial Fulfillment of
The Requirements for the Degree
of
Doctor of Philosophy
Public Policy

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Spring Semester 2004
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DEDICATION

In memory of Donald LeRoy Schaller, who understood well the value of completing a life-long educational endeavor. He earned his high school diploma at age sixty-one. Dad, thank you.

ACKNOWLEDGEMENTS

Writing a dissertation is hard work. Finishing it is even harder. As anyone who has done this knows it is not possible without lots of help. While it might not take a village, it easily takes a family and then some. I am eternally grateful to the countless people who have helped me along the way. I would like to acknowledge some of them here.

Our youngest daughter, Clara, was born ten days before I started my Ph.D. studies. She is now finishing the fourth grade and plays the upright bass, an instrument as tall as me. She is my constant reminder of what is most important. Clara and her six older sisters and brothers have been my inspiration. Their mother, my wife and lifelong partner, Wendy, has been the single, most important person in this endeavor. She is the bedrock on which I have depended for many things, with motivation ranking at the top. Words cannot describe my gratitude. Wendy, I love you. Along the way our family has shared many experiences. We now have a son-in-law, daughter-in-law, a future son-in-law, and recent grandson, but I have lost a brother, father, and grandmother. We've seen scores of baseball, basketball, field hockey, lacrosse, and soccer games; attended many graduations; and watched children become young adults. To all these experiences I am grateful.

I am indebted to my employer, the College of Southern Maryland (CSM), for the flexibility and support shown from start to finish of my studies. I thank my colleagues for covering my classes when necessary, my Chair, Rex Bishop, and Dean Ann Smith for accommodating a schedule that could best be described as "unusual," and President Elaine Ryan for balancing my committee responsibilities accordingly. I especially thank my close colleague Professor Joe Seremet, for his encouragement and the nickname, "Dr. Bob," dubbed years ago that has somehow grown on me.

To all my students of the past ten years, far too many to count; as I promised I will return your papers (if I can still find them). I especially thank the Spring 2004 students who lived through the final throes of this with me, repeatedly asking "well, did you finish?" and gradually hearing a more definitive answer.

To the School of Public Policy (SPP) at George Mason University (GMU) including Kingsley Haynes, Roger Stough, Jim Finkelstein, and other faculty, staff, and fellow students. I think I might hold a record for the most *Incomplete* grades for a single student, but this is a testament to the understanding and support shown to SPP students who must balance school with work, family, and other obligations. Additionally, I am grateful for the financial support provided through assistantships and grants. In particular, two summer grants in 2000 and 2002 helped me to dedicate time to this effort as opposed to normal teaching assignments. Finally, Jennifer Arnold and Beth Eck were instrumental in helping me often meet department deadlines, minimizing the number of 160 mile round-trip drives to and from campus.

To Fred Phillips and the Oregon Graduate Institute for sponsoring me as Visiting Faculty member the summer of 1999 which greatly helped in getting my field work started.

To my committee members, Don Kash, Chris Hill, Roger Stough, Edgar Sibley, and Bob Rycroft for their time and effort to critique my 'tome' of a manuscript. In the process they not only provided meaningful feedback that improved this document, but more importantly reinforced the

importance of balanced skepticism in research through their own critical assessment of my findings and conclusions.

To my fellow SPP students, especially Steve Lieberman and Kathy Emmons, for mutual support and collaboration throughout different phases of our studies.

To Ron Kostoff at the Office of Naval Research for serving on my proposal committee; for providing valuable insight on science, technology, and innovation; for making available his extensive collection of writings and other resources; and for co-authoring a paper with me that appears here in part.

To Bob Vay, GMU Dissertation & Thesis Coordinator, for his assistance and patience in getting this document into a publishable format. Also to Mary Johnson, Jan Carey, and other members of the library staffs at CSM, GMU, St. Mary's College of Maryland, and International Sematech for their patience, persistence and resourcefulness in locating documents and other materials that proved invaluable to the historical research for this study.

With regard to the study of the ITRS and the semiconductor industry more broadly, special thanks go to International Sematech for making possible this research through defrayed travel and communication costs, access to Roadmap workshops, archival records, and assistance in identifying potential interview candidates. I thank the almost 100 interviewees who helped inform this study for their time and patience. I particularly wish to thank Bob Burger, Turner Hasty, Bob Doering, Tak Ning, Bill Howard, and the many at Motorola, past and present, who have been so forthcoming with technology roadmaps and roadmapping background materials. Most especially, I wish to express gratitude to Linda Wilson and Sarah Mangum who manage, edit, and produce the ITRS at International Sematech. Beyond all the Roadmaps, participant interviews, workshops, and other data sources, several dozen conversations with Linda over about a 4yr period helped in piecing the complex puzzle together. There are still many missing pieces, but far fewer as a result of Linda's unselfish assistance.

Along the way valuable connections were made with fellow "roadmappers" who practice and refine this new craft, including Tom Kappel, Rob Phaal, Irene Petrick, Pieter Groenveld, Jack Fisher, and many others. I wish to especially acknowledge Carl Dietz, founder and CEO of Strateva (formerly Learning Trust), for allowing me to be part of his determined attempt at raising roadmapping methods and practice to a new level.

Most especially I wish to thank Don Kash as advisor, mentor, prodder, colleague, and friend. How he has been able to serve as dissertation committee chair for up to a dozen students at a time, maintain an active research, publication, and teaching schedule, while still giving individual attention to his students (his time with you is truly yours) is simply amazing. The lessons learned as his student are enduring. A brief story about Professor Kash is very telling. In my very first Ph.D. class he was reviewing the syllabus for a required Science & Technology Policy course. He emphasized to a bunch of nervous new students that doctoral studies were markedly different than previous coursework. Here, persistence was a far better success factor than semester grades. During this discussion one student asked about his grade policy. His response was patently Don Kash: to underscore his point he stated that anyone who could stick it out through the heavy reading schedule and other course requirements would get a B (passing grade). None of us was quite sure if he was serious or not, but we did not ask. During the semester a few students withdrew from the course (and the program). At the end of the semester, e*veryone else got a B*. Some arguably deserved a higher grade, but no one seemed disappointed. The lesson from 'getting a B' in that first class has since served me well both in and out of the classroom. This dissertation is but one example.

With Don's steadfast guidance and patience it is possible (but not probable) to finish a dissertation "15 minutes at a time," as he would often say. Don, I wish you happy retirement!

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ABSTRACT

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Robert R. Schaller, Ph.D.

George Mason University, 2004

Program Director: Dr. Don E. Kash

This dissertation is an historical and evaluative study of the Semiconductor Industry Association's (SIA) Technology Roadmap, now referred to as the *International Technology Roadmap for Semiconductors (ITRS)* or simply, the "Roadmap." Technology roadmaps and roadmapping practices comprise new and emerging tools in technology strategy, planning and management that have gained increasing attention by researchers. This study addresses how technology roadmaps affect technological innovation, corporate strategies, and public policies in the semiconductor industry.

This inquiry is accomplished through an examination of the technology roadmap 'landscape' more generally and a case-based analysis of the ITRS in particular. Several hypotheses were formulated to help seek greater and deeper understanding of not just the Roadmap but the surrounding context within which it emerged and has since evolved. This unique approach will demonstrate the overall thesis that the Roadmap is part of a continuing tradition wedded to the goal of sustaining historical industrial productivity—also referred to as "Moore's Law."

In support of this, an important contribution of the study is substantial historical research of key developments within the semiconductor industry. The findings depart from more widely-

accepted interpretations of technological innovation advanced by much previous research. Specifically, this research is concerned with the industry's heritage of incremental or evolutionary technological change following a *normal* innovation pattern, particularly involving manufacturing *process* innovations in semiconductors.

The findings also suggest that the Roadmap continues the decades-long heritage of normal innovation, now conducted at an international level and reaching across a wide and complex supply chain network. Finally, the analysis supports a new structural approach to technological innovation, one that is more coordinated with the help of a global industry roadmap. Thus a theory of *organized innovation* is advanced that helps explain how the increasingly fragmented semiconductor innovation community is able to continue working in cadence to address the daunting technical and economic challenges facing the industry 'down the road'.

Topical Chapter Outline

Preface

1. Introduction

This chapter sets up the thesis as an historical and evaluative study of the ITRS—its origin, evolution, and future role in influencing industry strategies and public policies. The overall research question is posed: *How have technology roadmaps affected innovation, strategy, and policy in the semiconductor industry?* This is followed by a review of nine hypotheses that guided the research.

Part One: Theory

2. Technology roadmaps and roadmapping for strategic planning

This chapter introduces the emerging field of technology roadmaps and roadmapping in an increasingly "hi-tech" environment. Technology roadmapping is briefly compared with other technology planning methods such as technological forecasting and technology assessment. Various types, uses, benefits, and other characteristics of technology roadmaps are discussed. This provides the necessary context for subsequent discussion and analysis.

3. The complexity challenge of industrial innovation in semiconductors

The purpose of this chapter is to begin to provide the conceptual framework for the research into the Roadmap and the Roadmap process. Important concepts from Complexity Science have been selected to inform this study. The chapter provides detailed description and application of complexity science concepts that draws heavily on *The Complexity Challenge: Technological Innovation for the 21st Century* by Rycroft and Kash (1999).

4. Emerging pattern of organized innovation

This chapter introduces a theory of a distinct pattern called "Organized Innovation" that helps explain the evolutionary behavior of the semiconductor industry. As background it provides an in-depth review of evolutionary theory including application of additional topics from *The Complexity Challenge.* Taken together, this and the previous chapter form the conceptual framework for this study. The Roadmap process is viewed within a normal innovation pattern that extends across international borders.

5. Research design

This chapter describes the qualitative research design used in this investigation. The research design is a two-pronged strategy: (1) historiography and (2) case study method. The research type is inductive within the tradition of grounded theory, which affords an opportunity to build theory that offers significant explanatory power from the evidence gathered. Each of these three approaches—historiography (the past), case study (the present), and grounded theory (implications for the future)—is complementary to the overall research design and intended to help establish face validity of the study.

Part Two: History

6. History and evolution of the integrated circuit industry

Chapters 6, 7 and 8 provide background and context to help support the concepts put forth in Chapters 2 and 3. These three chapters review important elements of industrial history that have shaped the innovation process. The Roadmap is derived from innovation practices and patterns that formed early on. Chapter 6 provides a brief history of innovation in the IC industry. By no means an exhaustive historical treatment of the IC industry, particular elements are highlighted and discussed (e.g., MOS technology) that would become critical to the success of the industry.

7. The *invention* of the microprocessor, *revisited*

The purpose of this analysis is to underscore the incremental (or normal) innovation pattern built upon accumulated knowledge that so characterizes this industry, in contrast with what many have since referred to as a revolutionary or discontinuous innovation. This writing looks back to the late 1960s and early 1970s with a perspective that draws on a variety of sources and is organized in a way that offers new insight into the innovation process.

8. Moore's Law: basis for industrial cadence

This chapter explores one factor—perhaps the most significant factor—from the previous chapters that determines the pace of innovation in semiconductors. Based originally on a simple observation of a few data points, this early extrapolation has been elevated to a meta-law that must continue to be validated by the semiconductor community. Reflecting its universal appeal, a much broader interpretation of Moore's Law has evolved.

9. Early history and evolution of semiconductor roadmaps

This chapter is concerned with the early history and evolution of semiconductor technology roadmaps and includes a significant amount of original research findings of a practice that dates back much earlier than what is commonly understood. This covers a fifteen-year span of roughly the mid 1970s through Micro Tech 2000 developed in 1991. Elements of a successful roadmap—long-range view, multi-disciplinary participation, and consensus-based methodology—are evident throughout the progressive expansion of scope from individual firm, to supply chain, and eventually to industry, national, international levels.

Part Three: ITRS Case Study

10. ITRS: A decade of industry roadmapping

This chapter picks up with the events immediately following Micro Tech 2000 that led to the first official industry roadmap developed by the SIA in 1992. This chapter is an historical thematic examination of published industry roadmap editions beginning with the 1992 Roadmap. A form of content analysis is used to study the major topics, considerations, and other salient features of each Roadmap edition to better understand its evolving nature.

11. Summary findings (ITRS assessment)

This chapter summarizes the major findings of extensive research into the ITRS process based primarily on a survey administered to fifty Roadmap participants. Note that this chapter is of primary interest to Sematech as part of a joint research project.

12. Implications for industry strategies and public policies

This chapter examines macro level effects of the Roadmap in both private and public arenas. Regarding industry strategies, the Roadmap plays a central role in helping prioritize resource investments from research to semiconductor equipment and materials suppliers. From a public

policy standpoint, similar benefits are derived from mission agencies and national labs engaged in semiconductor R&D. In both cases, however, a more general question concerns the traditional industry-government connection that has diminished over the years in this "critical technology" area. The Roadmap, in many ways, represents this linkage, but in a far different manner.

13. Conclusions

'What would the industry be like without a roadmap?' is a question that elicits a wide range of answers from interviewees. The consensus is, however, that the roadmap is not only useful, but increasingly vital to the continued technological advance, and thus industrial growth of the industry. As the industry—and supporting processes like the Roadmap—fully adjust to international involvement, the former CEO of Sematech has stated, "For the next 10 years, there's a different crisis. It's no longer 'beat Japan', but to stay on the productivity curve."[1] The purpose of the Roadmap is to 'show the way'—at least technically—to this end. Additional conclusions are discussed.

[1] C. Mark Melliar-Smith, quoted in Jeff Dorsch, "*Sematech*: and then there were nine," *Electronic News*, Vol. 44, Iss. 2227, July 13, 1998, 38.

PREFACE

The U.S. semiconductor industry is one of the industrial success stories of the past fifty years. Semiconductor devices (or "chips") drive our modern electronics era and are the basis of the technology-based *knowledge* economy. One recent study reports that the semiconductor industry is now the leading manufacturing industry in America, producing 20 percent more value added than any other manufacturing industry.[1] This success is attributable to the industry's ability to continuously deliver new technological innovations at a phenomenal rate. The semiconductor industry is now truly global and easily a contemporary model of today's dynamic, high-tech environment.

As expected, market forces have played a significant role in the industry's growth and development as scholars and investors alike have discovered in studying the behavior of this dynamic industry. Another part of the explanation, however, rests on the cooperative nature of the semiconductor community (i.e., industry, universities, research consortia, and government agencies and labs) as evidenced by the important role played by research consortia such as Sematech, SRC, IMEC, Selete, and many others. These developments have also been studied by industrial researchers.

One particular outcome of this unique industrial arrangement is an industry-wide *Technology Roadmap*. Interestingly, this development has not received much attention from researchers (aside from the practitioners who develop and use this Roadmap).

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[1] Robert J. Damuth, *America's Semiconductor Industry: Turbocharging the U.S. Economy*, report for the Semiconductor Industry Association, San Jose, CA, 1998.

This dissertation is an historical and evaluative study of the Semiconductor Industry Association's (SIA) Technology Roadmap, now referred to as the *International Technology Roadmap for Semiconductors (ITRS)* or simply, the "Roadmap."[2] It is a comprehensive case study of not just the Roadmap but the surrounding context within which it emerged and has since evolved. Past and future roles in influencing industry strategies and public policies are addressed. The ITRS, accessible online at http://public.itrs.net/, is a cooperative effort of global industry manufacturers and suppliers, government organizations, consortia, and universities that identifies the technological challenges and needs facing the semiconductor industry over the next 15 years. The Roadmap plays a vital role in research and industrial planning throughout the semiconductor community. Increasingly, it serves as a guide which individual organizations in industry, research consortia, government, and academic communities reference in strategic decision making including the multi-billions in capital investments needed for plant and equipment. The scope has broadened substantially over time; the Roadmap process is now international, including representation from the five largest producing regions of the world: the U.S., Japan, Taiwan, Korea, and Europe.

The ITRS provides a reference document of technology requirements, potential solutions, and their timing. It is a collaborative planning process that involves all parts of the semiconductor value chain from raw materials suppliers, to semiconductor equipment manufacturers who make sophisticated photolithography and other tools, to device makers who produce microprocessors, DRAMs, and other types of chips. Research consortia, academic, and government representatives also participate in the technology roadmapping process. Interestingly, the process is entirely voluntary.

Perceived by some as a novel—even unusual or unnatural—activity in such a highly dynamic industry, the Roadmap is actually one important element of a broader industrial arrangement that has evolved from the convergence of technological, economic, institutional, and cultural factors,

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[2] The terms *SIA Roadmap*, *ITRS*, and *Roadmap* are used interchangeably throughout this document.

all hinged on the goal of sustaining historical industrial productivity—also referred to as "Moore's Law."

Technology roadmaps and roadmapping practices have emerged recently as new forms of strategic technology planning in a wide variety of settings, most notably in semiconductors. One reason for this is the pervasiveness of semiconductor technology in today's industrial environment. Another reason for the widespread adoption is that roadmapping was advanced within industry and thus differs from other, more academic methods like technological forecasting. The ITRS has been on the forefront of this trend as an industry-wide compilation of future technology needs. As such, it is often cited as the exemplar, model, or "mother" roadmap as other industry roadmapping efforts have been patterned after the ITRS.[3] The reasons for its success are many and complex, but central to the answer is that, as Bob Burger, former research executive at the SRC, states "the Roadmap is one of the building blocks to a comprehensive process" that distinguishes the collaborative, yet competitive nature of this industry.[4]

Thus, the Roadmap has become an integral part of the industry, publicly capturing the best available knowledge of future needs and requirements for the bulk planar CMOS technological trajectory to continue unabated.[5] At the same time, the pace of progress moves so rapidly in semiconductor technology that as soon as the Roadmap is published it is out of date. As a result, the Roadmap process is now, for all practical purposes, on-going. Asked what life would be like without a Roadmap, informants for this research from throughout the semiconductor community consistently have difficulty answering the question.

The role of the Roadmap is explained in the Foreword of the *2001 ITRS* as follows:

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[3] David Probert and Michael Radnor, "Frontier Experiences from Industry-Academia Consortia," *Research Technology Management*, Vol. 46, No. 2, Mar/Apr 2003, 29.

[4] Robert M. Burger, personal interview, January 14, 2000. By 'building blocks' Burger is referring to the incremental approach the industry has taken toward collaboration: the 5yr cycle starting with SIA (1977), then SRC (1982), then Sematech (1987); also NACS (1988) that spawned Micro Tech 2000 (1991), the forerunner to the SIA Roadmap (1992, 1994, 1997) and ITRS (1999, 2001 and continuing). Also included are the MARCO Focus Centers initiated in 1998 to address long-term research needs.

[5] CMOS (complementary metal-oxide semiconductor) has been the dominant IC technology since 1980.

> It is the purpose of this *2001 ITRS* to provide a reference document of requirements, potential solutions, and their timing for the semiconductor industry. This objective has been accomplished by providing a forum for international discussion, cooperation, and agreement among the leading semiconductor manufacturers and the leading suppliers of equipment, materials, and software, as well as researchers from university and government labs. It is hoped that in the future—starting with this document as a common reference and through *cooperative efforts among the various ITRS participants*—the challenge of R&D investments will be cooperatively and more uniformly *shared by the whole industry* while, at the same time, *the fundamental elements that foster innovation will continue to be valued and cultivated by individual companies*.[6]

The most recent *2003 ITRS* comprises 646 pages that comprehensively address the technology needs and challenges over the next 15 years (through 2018). To do this, the ITRS pulls together individual requirements from a broad spectrum of a dozen technology areas that reflect the complexity of semiconductor manufacturing, arguably one of the most complex manufacturing processes today.

This dissertation attempts to explain the Roadmap in a manner that provides broader context and meaning. It is argued that the Roadmap is the culmination of a series of important events along a rich, but short history of a dynamic technology and equally dynamic community involved in the research, development, and commercialization of semiconductor devices. With this deeper understanding, implications for industry strategies and public policies can more readily be understood. To accomplish this important topics are examined, beginning with the general area of technology roadmaps. This is followed by a review of relevant theoretical concepts drawn from Complexity Science and Evolutionary Theory where a model of the Roadmap as a distinguishable pattern of "organized innovation" is proposed. To place the background, evolution, and assessment of the ITRS in context, the history of the semiconductor industry is reviewed, with emphasis on the IC, the microprocessor, and Moore's Law as the basis for the technological innovation "cadence" that the Roadmap intends to sustain. The final part of the dissertation is a comprehensive case study of the ITRS where industry strategy and public policy implications of the Roadmap are explored.

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[6] Semiconductor Industry Association, *International Technology Roadmap for Semiconductors: 2001*, San Jose, CA: SIA, 2001, ii, emphasis in original.

CHAPTER 1: Introduction

> "A technological innovation is like a river – its growth and development depending on its tributaries and on the conditions it encounters on its way. The tributaries to an innovation are inventions, technologies and scientific discoveries; the conditions are the vagaries of the market-place."
>
> - Ernest Braun & Stuart Macdonald[1]

> "I guess part of why a road map makes sense to us is that with complex technology there's no one right way to go."
>
> - William Spencer[2]

This chapter sets up the dissertation as an historical and evaluative study of the International Technology Roadmap for Semiconductors (ITRS)—its origin, evolution, and future role in influencing industry strategies and public policies. The thesis is that the Roadmap is one important element of a broader industrial innovation arrangement that has evolved from the convergence of technological, economic, institutional, and cultural factors, all hinged on the goal of sustaining historical industrial productivity trends.

Technology Roadmaps are cropping up everywhere in industrial circles. To some this might appear as the latest management technique or 'fad' following a long succession of innovative practices such as benchmarking, TQM, portfolio management, and many others. But to others—especially roadmap practitioners and users—this is far from a fad, and is finding application in a wide range of settings. This is particularly true within the semiconductor industry where technology roadmaps seem to be the most widely used.

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[1] Ernest Braun & Stuart Macdonald, *Revolution in Miniature: The history and impact of semiconductor electronics re-explored in an updated and revised second edition*, Cambridge: Cambridge University Press, 1982, 1.
[2] William J. Spencer, personal interview by Don E. Kash and Richard C. Adams, October 2, 1995.

This inquiry seeks to better understand the landscape of technology roadmaps and roadmapping practices by examining what roadmaps are (and are not); why and how roadmaps developed, evolved, and diffused as technology planning and management tools; their many uses (and misuses); and their benefits and consequences of use. The literature suggests that the technology roadmapping landscape is seemingly fragmented in scope, approach, and use. At the same time, the literature reveals that the metaphor "roadmap" appears to be a simple, identifiable concept that may afford this approach broader acceptance than related technology planning methods such as technological forecasting and technology foresight.

Given a better understanding of roadmaps in general, this study examines much closer one particular application: the semiconductor industry's Roadmap or *ITRS*. The ITRS was chosen as a single case study because it is widely acknowledged throughout the literature as a *model* roadmap. In the process of this examination, a wide range of contributing factors is presented to better explain why and how the Roadmap has developed. Following is a review of the purpose and scope that framed this inquiry.

The Research Question

Technology Roadmaps and related roadmapping practices comprise a new and emerging field of strategic technology planning as discussed in this dissertation. The overarching research question is:

How have technology roadmaps affected innovation, strategy, and policy in the semiconductor industry?

This question has been explored in detail through an examination of the technology roadmap 'landscape' more generally and a case study of the ITRS in particular. Several hypotheses were formulated to help seek greater and deeper understanding of this new field. These hypotheses were considered starting points to guide the research.

Hypothesis 1: Roadmapping differs from other methods of technology planning and forecasting due in large part to its inherent practical nature. A roadmap is not a prediction of future breakthroughs in science or technology, but rather an articulation of requirements to support future technical needs. A roadmap assumes a given future and provides a framework toward realizing it.

Hypothesis 2: Technology roadmapping, as a practice, emerged from industry as a practical method of planning for new technology and product requirements. Therefore its adoption rate is much greater than its more academic cousins such as technological forecasting and technology foresight.

Hypothesis 3: Existence of a consensus paradigm increases the success rate of S&T roadmaps. Thus, the unique pattern of technological change in semiconductors following "Moore's Law" is a key factor in the success of the SIA Roadmap.

Hypothesis 4: Roadmapping works better for technologies experiencing incremental vs. discontinuous or disruptive innovations. Thus, development of technology roadmaps is consistent with strategies for a normal innovation pattern (i.e., the coevolution of an established network and technology along an established trajectory).[3]

Hypothesis 5: The widespread presence of technology roadmaps at all levels within the semiconductor industry has contributed to a qualitatively different landscape for innovation, strategy, and policy in the (Roadmap era) 1990s and continuing as compared with the (pre-Roadmap era) 1980s.

Hypothesis 6: The SIA Roadmap, in particular, has contributed to a more regular and more predictable pace of innovation through deliberate coordination of pre-competitive R&D and related strategic semiconductor resources.

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[3] Robert W. Rycroft and Don E. Kash, *The Complexity Challenge: Technological Innovation for the 21st Century*, London: Pinter, 1999.

This hypothesis poses several additional questions:

1. Why has the semiconductor industry in particular embraced roadmapping so enthusiastically?
2. What benefits does technology roadmapping offer semiconductor firms (and industry) that other methods of technology/product planning do not?
3. To what extent do organizations such as organizational networks or technological communities (e.g., SIA) affect the process?
4. Does the SIA Roadmap foster roadmapping activities in firms, or vice versa?
5. To what extent do industry and firm roadmaps line up? Is there an underlying structural hierarchy among various roadmaps? If so, is it intentional?
6. How does the industry know if technology roadmaps work and how is success measured?
7. Is there a relationship between product/technology or industry life cycles and technology roadmap success?
8. What relationships exist between technology roadmaps and innovation, strategy, and policy?

Hypothesis 7: The SIA Roadmapping process involves a broad organizational network. Thus, collaboration in the roadmapping process is not new. Yet the structure and methods employed (e.g., pre-competitive basis, broad participant network, process—not product—emphasis) are clearly unique.

Hypothesis 8: The key driver for the SIA Roadmap has evolved from a competitively defensive, national industry strategy to a more universal and global strategy to stay on the industry's productivity curve as defined by Moore's Law.

Hypothesis 9: The SIA Roadmap has qualitatively affected R&D expenditure patterns of the U.S. semiconductor industry in significant ways. The emphasis seems to me more on "D" than "R."

In the course of this research, these hypotheses were tested and modified accordingly as a deeper understanding and appreciation developed. What became more evident was the significance of *context*, or the surrounding technological, economic, institutional and cultural environment. One starts this process of understanding by picking up a Roadmap and thumbing through it, noting its unique—and somewhat sterile—format and structure. Although the publisher

of the Roadmap is listed as the Semiconductor Industry Association (SIA), the first few pages reveal that the real 'authors' of the Roadmap number in the several hundreds and come from all corners of the semiconductor community, doing so voluntarily.

> The ITRS is produced by a global community of researchers, manufacturers, and suppliers who *volunteer* to travel; meet; build teams; examine material…; discuss, write, and reach consensus on key industry needs; and identify opportunities for new devices, materials, and technologies to help foster continued industry success.[4]

Structure of the Dissertation

This dissertation is organized into three parts. *Part One: Theory* follows this introductory chapter, and begins with Chapter 2 where the field of technology roadmaps and roadmapping practices is introduced. Chapters 3 and 4 provide the theoretical foundations for this thesis including relevant reviews of the literature and an attempt at original theory. Chapter 5 then describes the research design and data collection methodology used for this study. *Part Two: History* is a comprehensive descriptive treatment of essential background and context for this study. Chapter 6 provides a brief history of the IC industry as it pertains here. Chapter 7 revisits the invention of the microprocessor as more of an evolutionary than revolutionary discovery that it has mostly been described as. Chapter 8 discusses in detail Moore's Law, a key precept recognized throughout the semiconductor community. Finally, Chapter 9 reviews the early history of semiconductor roadmaps. *Part Three: ITRS Case Study* consolidates the bulk of original research around the Roadmap. Chapter 10 examines the origin of the SIA Roadmap and the series of successive industry Roadmaps now spanning more than a decade. Chapter 11 provides the summary findings of a detailed survey involving several dozen Roadmap participants. This chapter also includes an assessment of the ITRS process as requested by Sematech. Chapter 12 discusses implications of this research for public policies and corporate strategies while Chapter 13 provides conclusions.

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[4] *ITRS*, 1999 Edition, Acknowledgements, emphasis in original.

Appendices include: Sematech research arrangement, list of interviewees, interview instrument, etc.; detailed findings; Moore's Law retrospective; and individual chapter appendices and references.

PART ONE: THEORY

CHAPTER 2: Technology Roadmaps and Roadmapping for Strategic Planning[1]

> "A 'roadmap' is an extended look at the future of a chosen field of inquiry composed from the collective knowledge and imagination of the brightest drivers of change in that field... Roadmaps communicate visions, attract resources from business and government, stimulate investigations, and monitor progress. They become *the* inventory of possibilities for a particular field."
>
> - Robert Galvin[2]

> "[R]oadmapping must be recognized as a linchpin management tool that can help support integration with other needed strategic and operational management processes—it does not stand alone. And, bottom line, it is 'roadmapping' that delivers results; the focus cannot be on just the 'roadmaps'."
>
> - Michael Radnor and David R. Probert[3]

This chapter provides essential concepts and principles of science and technology (S&T) roadmaps and roadmapping practices. Later chapters in Parts 2 and 3 explore the evolution of semiconductor roadmaps including, in particular, the ITRS, the focus of this study. Application of basic roadmapping principles in the ITRS (and vice versa, i.e., reflection of ITRS practices reflected in general roadmapping principles) will become increasingly evident as this dissertation is considered in total.

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[1] This chapter is based largely on an article co-authored with Dr. Ronald N. Kostoff (Office of Naval Research), "Science and Technology Roadmaps," *IEEE Transactions on Engineering Management*, Vol. 48, No. 2, May 2001, 132-143.
[2] Robert Galvin, "Science Roadmaps," *Science*, Vol. 280, May 8, 1998, 803, emphasis in original.
[3] Michael Radnor and David R. Probert, "Viewing the Future," *Research Technology Management*, Vol. 47, No. 2, Mar/Apr 2004, 26.

Introduction

S&T, or in this application, technology roadmaps are used in industry, government, and academia to portray the structural and temporal relationships among science, technology, and applications. Roadmaps are employed as decision aids to improve coordination of activities and resources in increasingly complex and uncertain environments. Specific uses of technology roadmaps include: technology strategy, planning, and management; technology marketing; enhancing communications among researchers, technologists, product managers, suppliers, users, and other stakeholders; identifying gaps and opportunities in technology programs; and identifying obstacles to rapid and low-cost product development. Technology managers also use roadmaps to help identify those areas that have high potential promise, and to accelerate the transfer of technology to eventual products.

A recent assessment places technology roadmapping (TRM)[4] within the domain of strategic planning and foresight methods, however noting that TRM differs from these traditions' positivistic and deterministic view of scientific progress. Roadmapping is perceived as a practical approach to deal with the complex process of technological innovation. The state of theoretical understanding is summarized as follows:

> The direction in which this [strategic foresight method] evolves is typically of a more "constructivist" one, whereby methods, techniques and processes are used to have actors within the innovation process communicate with each other in a structured and organised fashion. The aim of such processes is to collectively define future scenarios, visions and the like, and, from them, derive options for technological development. Since relevant actors are involved, it would be easier to implement those options.[5]

Despite widespread usage of technology roadmaps, there has been relatively little attention paid to the theory and practice of roadmapping in the published literature. Indeed, practice leads theory in roadmapping, however this situation is undergoing change. Within the past year, two

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[4] TRM is a widely-accepted acronym in Europe where the study was published. TRM is not commonly used in the U.S.

[5] Bastiaan de Laat and Shonie McKibbin (Technopolis), "The Effectiveness of Technology Road Mapping: Building a strategic vision," a study for the Dutch Ministry of Economic Affairs, est. 2002, 2, emphasis in original.

relevant journals have published special feature issues comprising twenty articles on roadmapping.[6] Research centers engaged in technology roadmaps and roadmapping have been established at Purdue University in the U.S. and Cambridge University in the U.K.[7] Roadmapping methods and practices workshops and other forms of educational venues are now scheduled on a monthly basis by Strateva, a U.S.-based software and consulting firm.[8] In Europe, an active TRM Users Group (TRMUG) meets on a quarterly basis to advance roadmapping best practices. Taken together, these and similar activities represent a growing academic interest in the topic.

For expository purposes, this chapter attempts to bring some common understanding to roadmaps and roadmapping practices. The chapter begins with generic roadmap definitions, including a taxonomy of roadmaps that better classifies the broad spectrum of roadmap objectives and uses. Characteristics of retrospective and prospective roadmaps are then identified and analyzed. The roadmap construction process, referred to as *roadmapping*, is presented in detail. Finally, a brief assessment of quality characteristics of successful roadmaps is presented.

Why Roadmap?

The rapid pace of technological growth and globalization has increased the complexity of technology management substantially. At the same time, the dissolution of central R&D labs has shifted the focus of technological innovation to more decentralized structures increasingly including external organizations such as suppliers and customers. Closer coordination under ever shorter and tighter development schedules necessitates more powerful decision aids including the umbrella group of techniques commonly referred to as "roadmaps." Figures 2-1 and 2-2 illustrate two key challenges underpinning semiconductor technology roadmapping. Figure 2-1

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[6] The special feature issues are: 1) *Research-Technology Management*, Vol. 46, No. 2, March-April 2003 (5 articles) and Vol. 47, No. 2, March-April 2004 (6 articles); and 2) *Technological Forecasting and Social Change*, Vol. 71, 2004 (9 articles).

[7] The research centers are: 1) the Center for Technology Roadmapping (CTR) at Purdue University, http://roadmap.itap.purdue.edu/CTR/default.htm; and 2) the Centre for Technology Management within the Institute for Manufacturing at Cambridge University (UK) http://www-mmd.eng.cam.ac.uk/ctm/trm/index.htm

[8] See http://www.strateva.com/

shows the possibility (dotted line) of not continuing the historic rates of reducing cost per function as technical and economic obstacles of shrinking device feature sizes are faced.

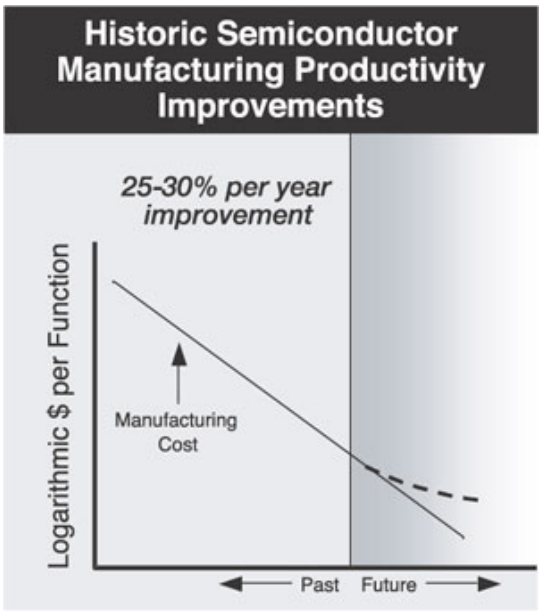

Figure 2-1. Past and Future Semiconductor Manufacturing Productivity

Source: Walter J. Trybula, "Technology Acceleration and the Economics of Lithography (Cost Containment and ROI)," *Future Fab International*, Issue 14, Section 5, Figure 1, 2003.

Figure 2-2 depicts collapsing product life cycles of popular microprocessor chips. Note how earlier microprocessor family life cycles averaged several years (as much as eight years for the Intel 386 including all three frequency versions) while the most recent chips average closer to six to nine months for each single-frequency version. Additionally, the business model of product introduction at high price followed by successive "shrinks" (i.e., the same chips manufactured with smaller feature sizes) at dramatically lower prices places significant timing pressures on chip makers to meet these ever tighter schedules. Thus roadmaps help microprocessor makers, along with their suppliers and customers, to meet these challenges in a much more coordinated manner. Probert and Radnor (2003) underscore this point:

It could be said that the upsurge in interest in roadmapping that surfaced in the 1990s was a direct consequence of the ever-shortening product development cycle times, creating a greater need for coordination (i.e., customer desires to build new technologies into products as soon as they are available). Speed (and hence time-related processes) became a premier consideration in an era where "the fast ate the slow." In turn, this triggered the beginnings of an expanding demand for roadmaps that continues and appears to be accelerating.[9]

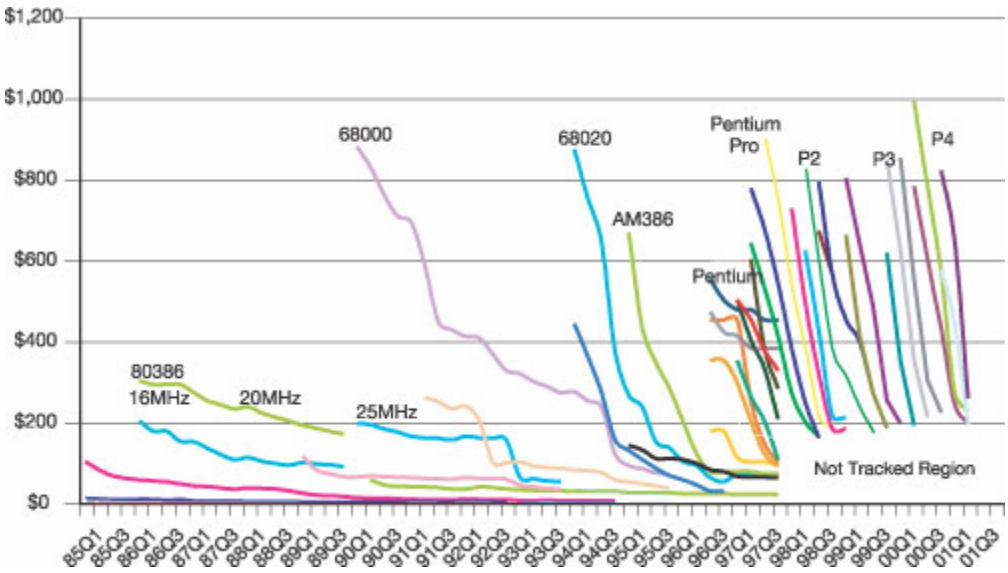

Figure 2-2. Shortening Life Cycles of Microprocessors

Source: Ibid., Figure 3.

Definitions

Generically, a "road map" is a layout of paths or routes that exist (or could exist) in some particular geographical space. In everyday life, road maps are used by travelers to decide among alternative routes toward a physical destination. Thus, a road map serves as a traveler's tool that provides essential understanding, proximity, direction, and some degree of certainty in travel planning.

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[9] David Probert and Michael Radnor, "Frontier Experiences from Industry-Academia Consortia," *Research Technology Management*, Vol. 46, No. 2, Mar/Apr 2003, 28, emphasis in original.

In the past few years the single word "roadmap" has surfaced as a popular metaphor for planning S&T resources. The variant "roadmapping" is a new verb that describes the process of roadmap development. The practice of roadmapping typically involves social mechanisms, and is both a learning experience as well as a communication tool for roadmap participants.

Robert Galvin (1998), former Motorola chairman and prominent advocate of S&T roadmaps, offered the opening definition of a roadmap as "an extended look at the future of a chosen field of inquiry composed from the collective knowledge and imagination of the brightest drivers of change in that field." He further asserted, "In engineering, the roadmapping process has so positively influenced public and industry officials that their questioning of support for fundamental technology support is muted."[10]

Therefore, a technology roadmap provides a consensus view or vision of the future technology landscape available to decision makers. The roadmapping process provides a way to identify, evaluate, and select strategic alternatives that can be used to achieve a desired technology objective. For example, the introduction section of the 1997 Semiconductor Industry Association's (SIA's) *National Technology Roadmap for Semiconductors* provides a conceptual illustration showing the possible spectrum of technology alternatives in photolithography in future semiconductor technology generations (Figure 2-3). There are certainly more future alternatives, however the process of roadmapping helps narrow the field of requirements and possible solutions to those most likely to be pursued. Note that since this graphic was created the industry has 'chosen' to pursue extension of DUV (deep ultra-violet) and EUV (extreme ultra-violet) lithography as will be discussed in later chapters. Both technologies follow their respective roadmaps, but are interdependent as EUV is slated to replace DUV around 2009. Further, both techniques share some enabling technologies that must be reflected in their roadmaps.

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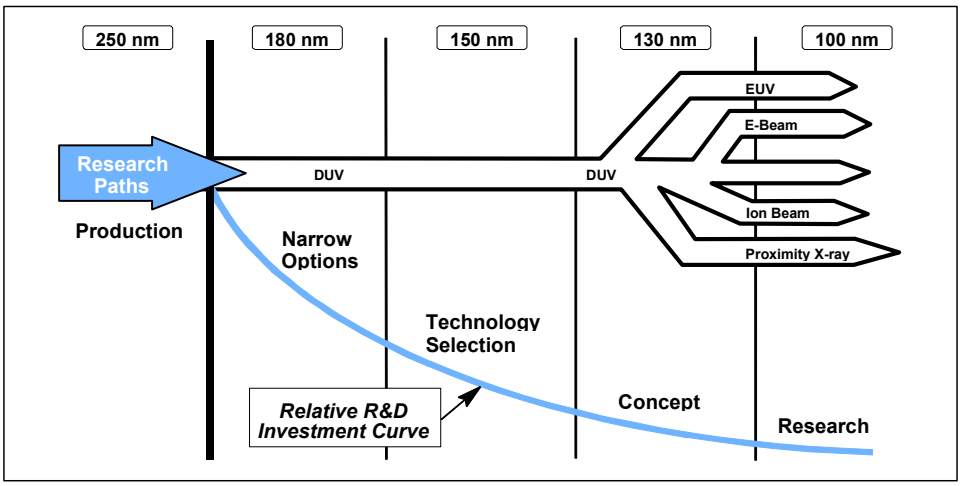
[10] Galvin, op. cit.



DUV—deep ultraviolet
EUV—extreme ultraviolet
E-beam—electron beam

Conceptual Illustration of Today's Research and Development Investments for Future Production Technologies

Figure 2-3. Future Lithography Technology Alternatives

Source: Semiconductor Industry Association, *The National Technology Roadmap for Semiconductors: Technology Needs*, December 1997, Figure 1, 2.

At the application level, a product-technology roadmap is a disciplined, focused, multi-year, business planning methodology. For the product manager, a roadmap's implementability is as important as its strategic value. Numerous firms including Motorola, Philips, Lucent, Honeywell, Rockwell, and GM, to name a few, have employed product-technology roadmapping on a large scale. Most recently, Motorola has championed a firm-wide Enterprise Roadmap Management System (ERMS) that provides "a common roadmapping process, a common software solution, and a common information architecture for all of Motorola… Currently, Motorola has approximately 3,000 [Geneva] Vision Strategist users with over 5,000 roadmaps created in the

roadmap library"[11] Additionally, many of these roadmaps are linked externally with supplier and customer roadmaps.

A common descriptive thread of technology roadmaps is the representation in portrayable dimensions of the structural and temporal relations among elements as they evolve toward practical applications in products. As in the case of ordinary highway maps, a technology roadmap can be viewed as consisting conceptually (if not always physically) of nodes and links. These roadmap nodes and links can have, in the most general case, quantitative and qualitative attributes. For example, in a highway map, a link (road) has a direction, a length, and sometimes an effective width (two lanes, etc.). These are essentially quantitative attributes. However, sometimes a highway map will show a dotted line next to a road, denoting that road as scenic. This is a qualitative attribute. Similarly, a link in a technology roadmap could represent the qualitative attribute of the degree of impact a science program could potentially have on a technology program, and/or the quantitative attribute of the time estimated to proceed from the science program to the technology program.

The typical highway map usually consists of two dimensions in which the nodes and links are portrayed. The node locations and the links are vectors, and need both magnitude and direction to be described fully. Likewise, the generic S&T roadmap consists of spatial and temporal dimensions (see examples in Figure 2-4).

The spatial dimensions shown in Figure 2-4 reflects the relationship among S&T disciplines, programs, or projects at a given point in time, while the time dimension accounts for the evolution of the same S&T capabilities. As in the highway map, the S&T roadmap nodes and links are also vectors that need both magnitude and direction for full description. Since technology evolution processes are usually non-linear and unpredictable, and since roadmaps are used for both retrospective and prospective studies in time, the link vectors can assume forward and backward

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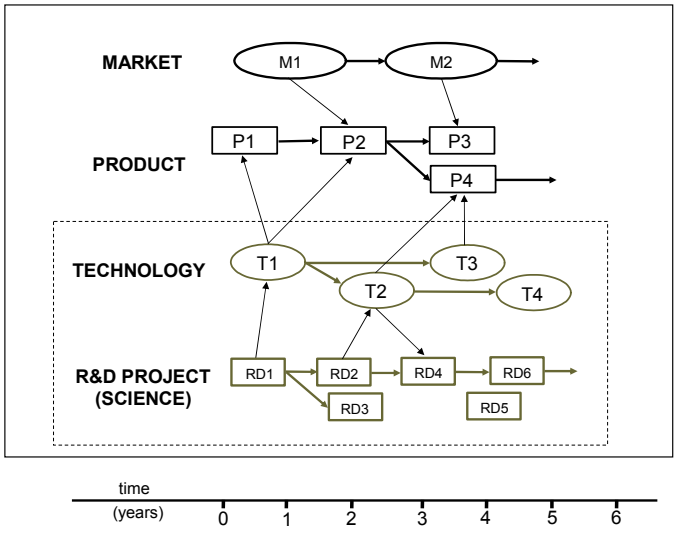
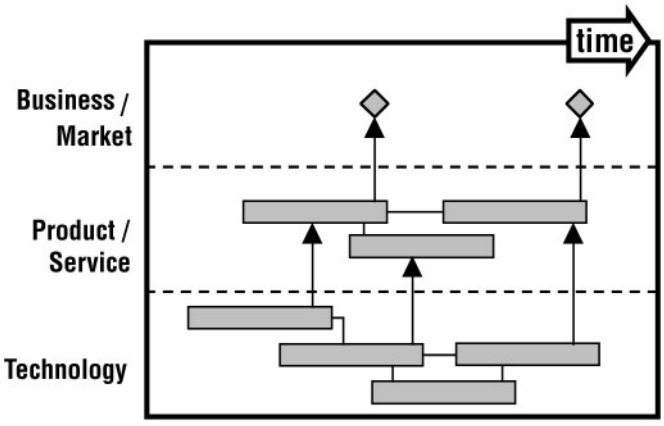
[11] James M. Richey and Mary Grinnell, "Evolution of Roadmapping at Motorola," *Research Technology Management*, Vol. 47, No. 2, Mar/Apr 2004, 37-38, 40. Note that Vision Strategist® is a roadmapping software platform developed by Strateva and in common use by other organizations.

directions in time. Construction of a roadmap thus requires identifying the nodes, specifying the node attributes, connecting the nodes with links, and specifying the link attributes.



(a)

Source: adapted from Pieter Groenveld, "The Roadmapping Creation Process," Presentation at the Technology Roadmap Workshop, Washington, DC, October 29, 1998.



(b)

Source: Robert Phaal, Clare J.P. Farrukh and David R. Probert, "Technology roadmapping—A planning framework for evolution and revolution," *Technological Forecasting & Social Change*, Vol. 71, 2004, Figure 2, 10.

Figure 2-4. Generic S&T Roadmaps Showing Nodes and Links

There are many ways to graphically portray roadmaps, however the format of a time-based tabular architecture is very common. Figure 2-5 depicts this format using a software platform.

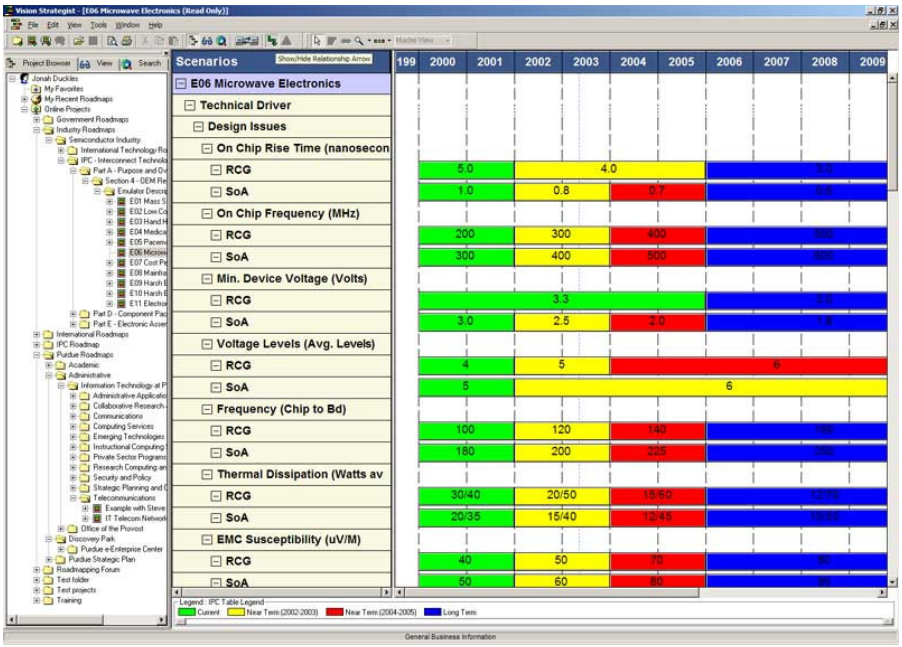


Figure 2-5. Software-Based Roadmap

Source: Purdue University Center for Technology Roadmapping (CTR), http://roadmap.itap.purdue.edu/CTR/default.htm The software is Geneva Vision Strategist® developed by Strateva, Irvine, CA.

Types of Roadmaps

Various roadmap types are now discussed. According to Radnor (1998), technology, product, and related forms of corporate and industry roadmapping are being implemented gradually in large-scale technically-centered firms. To date, the published literature on roadmapping is sparse; however, a significant amount of industry-based information (much from practitioners) can be found in the broader literature (Schaller, 1999; Kappel, 1998; Kostoff, 1997a). Additionally, Caswell and other researchers collected and catalogued more than 150 roadmap-related documents from industry, government, and academia to synthesize current thinking about technology and business practice strategies and needs. From this research, they prepared a comprehensive report on industry roadmaps in the form of a "digest" (NGM, 1997). More recently, Probert and Radnor (2003) estimate that as many as 250 U.S. industry roadmaps exist, a number

of which with the support of the U.S. Department Of Energy Office of Industrial Technology.[12] Internationally, industry (or *sector* as they are referred to in Europe) roadmaps are also becoming widely adopted. In a 2002 study for the Dutch Ministry of Economic Affairs, almost half of the 78 'supra-company' level TRM (technology roadmapping) exercises selected were from countries other than the U.S.[13] One can draw some preliminary conclusions from this literature. For instance, a distinct and credible classification of types or categories of roadmaps appears feasible. In a 1998 technology roadmap workshop, at least a dozen different applications of roadmaps were presented (ONR, 1998). These applications cover a wide spectrum of uses including:

- science / research roadmaps (e.g., science mapping)
- cross-industry roadmaps (e.g., Industry Canada initiative)
- industry roadmaps (e.g., International Technology Roadmap for Semiconductors)
- technology roadmaps (e.g., aerospace, aluminum, etc.)
- product roadmaps (e.g., Motorola, Intel, and others)
- product-technology roadmaps (e.g., Lucent Technologies, Philips International)
- project / issue roadmaps (e.g., for project administration)

From this variety of uses, a taxonomy was established that attempts to classify roadmaps according to their location in applications-objectives space (see Figure 2-6).

[12] Probert and Radnor, op. cit., 29.
[13] de Laat and McKibbin, op. cit., Exhibit 2, 9.

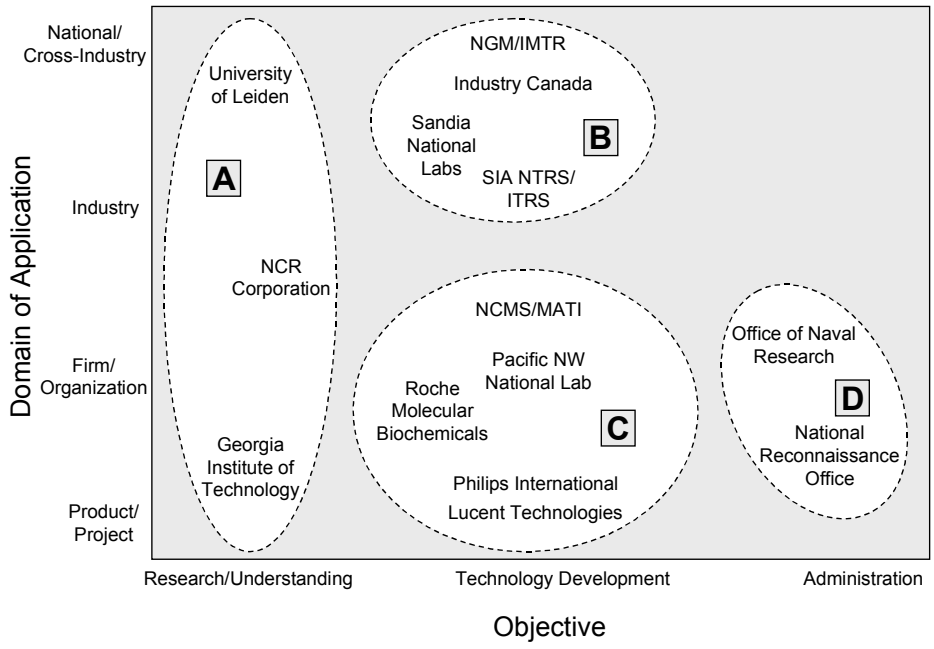


Figure 2-6. Taxonomy of Roadmaps

Source: Richard Albright and Robert Schaller, "Technology Roadmap Workshop," moderated by the Office of Naval Research, Washington, DC, October 30, 1998.

These independent roadmap applications can be classified broadly in Figure 2-6 as follows:

A. Science & Technology Maps or Roadmaps
B. Industry Technology Roadmaps
C. Corporate or Product-Technology Roadmaps
D. Product / Portfolio Management Roadmaps

More recently, Kappel (2001) has extended this classification yet further considering such characteristics as accuracy and influence as shown in Figure 2-7.

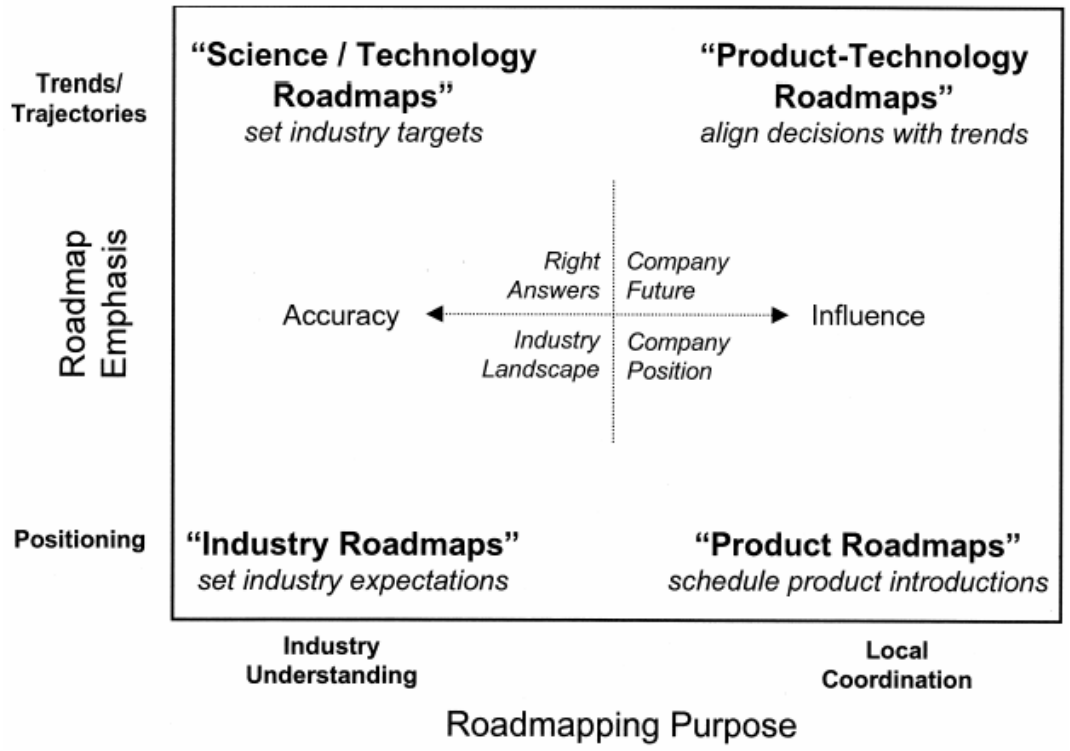


Figure 2-7. Kappel's Roadmapping Taxonomy

Source: Thomas A. Kappel, "Perspectives on roadmaps: how organizations talk about the future," *The Journal of Product Innovation Management*, Vol. 18, 2001, Figure 1, 40.

Additionally, in some technology areas a hierarchy of roadmaps is becoming increasingly evident in the literature. In an early bibliography of more than 400 specific references to roadmaps, no less than 25 of these were comprehensive industry technology roadmaps ranging from semiconductors to aluminum to wood and paper products (Schaller, 1999). From some of these industry roadmaps related technology, product, and even component product roadmaps can be traced. A very good example of this integration is the U.S. electronics industry, represented by the National Electronics Manufacturing Initiative (NEMI) Technology Roadmaps as shown in Figure 2-8, with participation from more than 175 organizations (NEMI, 1998). The following caption briefly describes the integration involved in the 2004 NEMI Roadmap process:

> The 2004 roadmap covers 18 technology and business process topics. Addressing the shifts in each of these areas, along with the related technology gaps and business needs, benefits the entire electronics industry. By helping organizations focus resources on

areas of greatest need, the roadmap improves technology development and deployment for greater manufacturing productivity…

NEMI coordinates with other roadmapping organizations to synchronize timelines, agree on and refine product sector definitions, identify common elements, facilitate cross-functional groups, and coordinate roadmapping schedules. Direct links with other roadmaps and other organizations include ITRS (semiconductors), IPC (interconnection substrates), the Optoelectronics Industry Development Association (OIDA; optoelectronics and optical storage), the Information Storage Industry Consortium (INSIC; magnetic and optical storage), the US Display Consortium (USDC; displays), the Supply Chain Council (SCC; product lifecycle information management), and the International Microelectronics Packaging Society (IMAPS; ceramic substrates).[14]

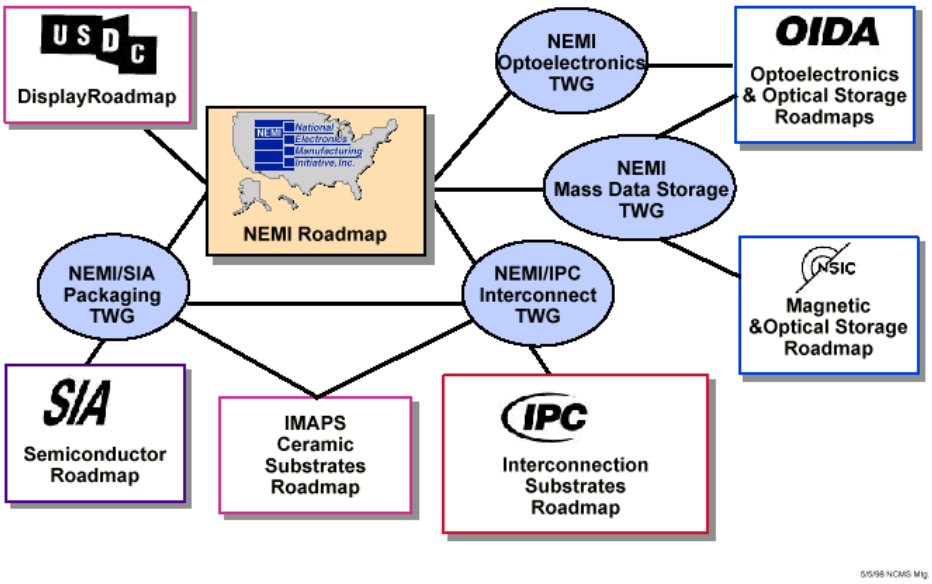


Figure 2-8. NEMI 1998 Roadmap Linkages

Source: Jim McElroy, "NEMI Roadmaps," Presentation at the 12th Annual NCMS Conference & Expo, Orlando, FL, May 5, 1998.

Uses and Benefits of Roadmapping

Garcia and Bray (1998) underscore the major uses of and benefits derived from technology roadmapping. Three major uses are:

[14] "The NEMI Roadmap," brochure obtained from http://www.nemi.org/

1. Roadmaps help develop consensus among decision makers about a set of technology needs,
2. Roadmapping provides a mechanism to help experts forecast technology developments in targeted areas, and
3. Roadmaps present a framework to help plan and coordinate technology developments at any level: within an organization / company, throughout an entire discipline / industry, even at cross-industry / national or international levels.

Overall, the main benefit of technology roadmapping is provision of information to help make better investment decisions. Kappel (1998) argues further that the roadmapping process not only produces more informed individual decisions, but brings with it better *alignment* of organizational decision making. One example of this type of synergistic effect has occurred at Lucent Technologies in the form of uncovering common technology needs through cross-roadmap reviews. Through a top-level review of multiple wireless communications product-technology roadmaps, it was discovered that all the individual roadmaps addressed the need for gating battery and antenna technologies. With this information, the corporate technology strategy office was able to recommend sharing and consolidation of R&D, supply-line, and other common resources (Albright, 1998).

Probert and Shehabuddeen (1999), in their description of a technology road map as a formalized method for organizations to assess future technological developments within an environment of constant change, emphasize taking a 'systems view' of technology change as a key benefit:

> "An important aspect of the road mapping technique is the multi-disciplinary, cross-functional working that it requires in order to fulfill its objective of providing common guidance for the whole organization."

Finally, Radnor (1998b) comments that long-term benefits of roadmapping have yet to be realized:

> "Roadmapping being relatively new, it is not yet clear how long it takes for different benefits to become evident - which manifest right away and which may require a learning process or even restructuring of related processes thereby increasing the time, effort and buy-in required. It is likely that initial investment could be high as training, for example, is implemented and that the cost-benefits would improve with later implementations of the process. It is also to be anticipated that roadmapping will grow as it evolves to

> incorporate new dimensions, e.g., PERT-like methods that may be part of a redefinition of the project manager role - something that may already be signaled by the roadmapping process."

The next section describes the two fundamental construction approaches employed in roadmapping, expert-based and computer-based. After this differentiation of construction methodology by source is shown, a further differentiation in construction methodology by temporal perspective—retrospective and prospective—is presented.

Roadmapping Process

Based on extensive literature reviews (Kostoff, 1997a; Schaller, 1999), many roadmap variants have been identified. These can be aggregated into two fundamental roadmapping approaches: expert-based and computer-based.

Expert-Based Approach

In this approach, a team, or teams, of experts is convened to identify and develop attributes for the nodes and links of the roadmap. For example, development of SIA's Roadmap involves participation by several different Technology Working Groups (TWGs). As is later discussed, these TWGs are staffed by a mixture of multi-national personnel from industry, government, and academia to ensure a balance of expertise and views.

This process is somewhat paradoxical in that the appropriate expertise must be employed to develop a roadmap, but the appropriate expertise becomes fully known only after a complete roadmap has been constructed. An iterative roadmap development process is therefore essential. This is most evident in the ITRS as it is renewed annually, thus is essentially an on-going process (see Chapter 10).

For an organization in which many of the roadmap components are being pursued in-house, such as a large focused government or corporate laboratory, much of the expertise can be assembled in-house. Researchers, developers, marketers and others with relevant knowledge of the overall roadmap theme can be readily convened to develop the framework. At the other

extreme, organizations with little expertise in the overall roadmap theme, such as venture capital groups or cash-rich organizations that wish to expand their boundaries, require external assistance to develop credible roadmaps.

Depending on the purposes for which the roadmap is being constructed, the team can initiate the process at the earliest development stage (basic research), middle time (technology development), or latest time (product development), and fill in the remainder of the roadmap. Most retrospective studies start with a successful final product that has already been achieved, and work backward in time to identify the characteristics and / or sponsors of successful research and development events. Some retrospective studies (looking backward in time from the present) start with initial research grants, and fill in the remainder of the roadmap to arrive at the product that exists today. Box 2-1 differentiates between these two basic types of analysis.

Box 2-1. Retrospective vs. Prospective Analysis

From a temporal perspective, there are two major variants of analyses that have examined the science-technology-application evolution process: retrospective analysis and prospective analysis.

Retrospective Analyses: Backward from the Present

Retrospective analysis has been used mainly for portraying the accomplishments and impacts of a specific sponsor's S&T investment, and for identifying the management and other environmental factors that promoted the successful S&T results. There have been two types of retrospective analysis. One type starts with a successful technology or system and works backward to identify the critical R&D events that led to the end product. The other type starts with initial S&T funding, and traces evolution forward to identify impacts. The tracing backwards approach is favored for two reasons: (1) the data are easier to obtain, since forward tracking is essentially non-existent for evolving S&T; and (2) the sponsors have little interest in examining

S&T that may have gone nowhere.

Prospective Analyses: Forward from the Present

Prospective analyses have been used to elicit champions for supporting S&T, for identifying S&T gaps and opportunities in large development programs, for enhancing communications among all the interested parties in S&T program development, and promoting a common understanding of the more global context of S&T development. By far, roadmaps in S&T today—and the general perception of almost every other roadmap—are based on a portrayal of a prospective evolution of S&T.

There are two types of prospective analysis. Technology-push prospective roadmaps (looking forward in time from the present) start with existing research projects, and fill in the remainder of the roadmap to identify the diversity of capabilities to which this research could lead. For example, the ITRS is based upon extending "Moore's Law," the semiconductor industry's historical exponential productivity growth rate, over the next 15 years (see Chapter 8). Staying on this path is the key to the industry's continued success in the future. As Gordon Moore himself states (Korcynski, 1997), "If we can stay on the SIA Roadmap, we can essentially stay on the [Moore's Law] curve. It really becomes a question of putting the track ahead of the train to stay on plan."

In contrast, requirements-pull prospective roadmaps start with desired technology or system or other end products (e.g., highly fuel-efficient motor vehicle or future defense weapon system), and works backwards to identify the critical research and development required to fill in the remainder of the roadmap to arrive at these products.

EIRMA (1997) simply refers to these two approaches as "backward" and "forward" and makes a further distinction:

> "There are two common approaches in TRM [technology road mapping]. 'Backward' involves finding out how to reach a given target (which could be a business goal, a product, process, fulfillment of a legislative requirement, or a technology), whilst 'forward' designates the process of building upon technologies until new targets appear. In the first case, the direction

of analysis is backwards in time (i.e., from the future), in the second case the direction is forwards (i.e., to the future). These methods are sometimes referred to as 'top-down' or 'bottom-up' respectively."

In the middle are technology-push / requirements-pull prospective roadmaps, that start with existing science or technology development programs which may be technology-driven or requirements-driven, and then identify both the research gaps which obstruct forward progress and the diversity of end products to which successful development could lead.

Retrospective analyses cover timeframes from typically decades past to the present, while prospective analyses cover time frames from the present to typically a decade or more into the future. Chosen time frames, of course, depend upon the technology aggregation level and the roadmapping organization’s planning horizons and objectives. Roadmaps presenting information at a high aggregation level generally cover a longer period than those showing more specific information.

Since the retrospective analyses use existing data, they obviously have a higher degree of certainty, reliability, and credibility than the prospective analysis. However, because of the multiple interpretations possible from the existing data, the difficulties in allocating costs and benefits, and the difficulty of assigning sponsor credits to specific development events, even the conclusions of the retrospective studies have not been accepted unambiguously.

Besides the two contrasting approaches described in Box 2-1, there are also combination retrospective-prospective roadmaps. These combine some historical development of a technology with a vision of where the technology is headed. Kostoff (2001) has found these roadmaps to be particularly helpful in reviews of ongoing research programs. These combination roadmaps provide a concise picture of the program's origins and past development, as well as coordination with and leveraging of the external S&T community, and give some indication of where the program is heading according to the vision of its promoters.

In all these cases, the main focus of the expert-based approach is to draw on the knowledge and experience of the participants to subjectively identify the structural relationships within the network and specify the quantitative and qualitative attributes of the links and nodes.

Computer-Based Approach

In this approach, large textual databases that describe science, technology, engineering, and end products are subject to computer analyses. These databases could include published papers, reports, memoranda, letters, etc. Through the use of generic computerized methodologies including computational linguistics and citation analyses, research, technology, engineering, and product areas are identified; their relative importance is estimated and quantified; and their relationships and linkages to other areas are identified and quantified. Once all these node and link attributes have been specified, the network is then constructed.

In contrast to the expert-based approach, the computer-based approach has more objectivity. It does not have the preconceived limitations, constraints, biases, and personal and organizational agendas of the experts. The computer-based computational linguistics approach does not start from one point in time (as does the expert-based approach) and evolve either forward or backward in time. It generates the network at all points in the time domain of the source database simultaneously. Temporal changes are usually obtained by examining full spatial networks derived at different points in time. The citation approaches march forward in historical time from the cited papers to the citing papers to generate the temporal aspects of the citation network.

Most of the computer-based computational linguistics studies have focused on the structural relationships among S&T disciplines and programs (spatial dimensions), because this was their main objective and because the source databases tended to contain much of this type of information. This focus is not a conceptual limitation of the process, but rather an implementational limitation that could be overcome by employing different research objectives

and additional source materials. The computer-based approach is in its infancy, due to the only recent emergence of large relevant textual databases and efficient information-extracting computational linguistic approaches.

Hybrid Approach

Another possible limitation of the computer-based approach has to do with the absence of interaction among experts that is vital to the roadmapping process. As Radnor (1998a) points out, "Companies want to 'mechanize' roadmapping, but much of it remains off the books. Roadmapping is political and involves negotiation and re-negotiation." As such, a balanced combination of the expert- and computer-based approaches may prove to be the most effective and efficient approach to roadmap construction. In sum, both expert- and computer-based approaches have value to offer, and the best features of each should be identified, extracted, and employed for optimal results.

Examples

Some sample prospective roadmaps from the literature will now be summarized. See Kostoff (1997a), Kappel (1998), and Schaller (1999) for a much more comprehensive and detailed literature sampling. Note that more recent abstracts reflect a more theoretical treatment of roadmapping, an evolution from the industry (practitioner)-based literature that has historically been predominant.

Kappel's (1998) dissertation provides an organizational perspective on roadmapping as currently practiced. It presents the experience of some large, decentralized firms that have implemented roadmapping, and evaluates the results. The dissertation is a case-based, exploratory study that seeks: (1) to understand better the nature of roadmapping by characterizing it and its tangible output, (2) to recognize the effects of roadmapping on the organization, and conversely, the organization's influence on roadmapping, (3) to identify the

appropriate circumstances for using the process, (4) to specify roadmapping quality assessment, and (5) to explore the theoretically interesting and practically useful features of roadmapping.

A master's thesis (Peet, 1998) examines the experiences of three European companies in using, or attempting to use technology roadmapping, along with problems and benefits experienced. It then continues to examine a pilot study of applying technology roadmapping to the Mixed Oxide Fuel unit of British Nuclear Fuels. The researcher's methodology is derived from EIRMA's (1997) documentation on the technique, relating the three companies experiences to projections, and questions the distinctive factors about a company that determine technology roadmapping’s appropriateness for the company.

Groenveld (1997) describes the product-technology roadmap process developed at Philips Electronics. Here, roadmapping aims at better integration of business and technology strategy and improvement of the front end of the product creation process (the concept and idea phase). The outcomes are roadmaps that present products and technologies required to realize these products, as well as their mutual relationship over a five-year period. Teamwork, integral involvement by the organization, and good communication are essential characteristics of the process.

Barker and Smith describe a unique approach to Technology Foresight (1995). It was used to devise an R&D strategy embracing the core business areas of the British Petroleum company. The process was based on the use of roadmaps that are visual descriptions summarizing the outcomes of numerous discussions involving all the personnel responsible for procuring, planning, funding, monitoring, and implementing R&D.

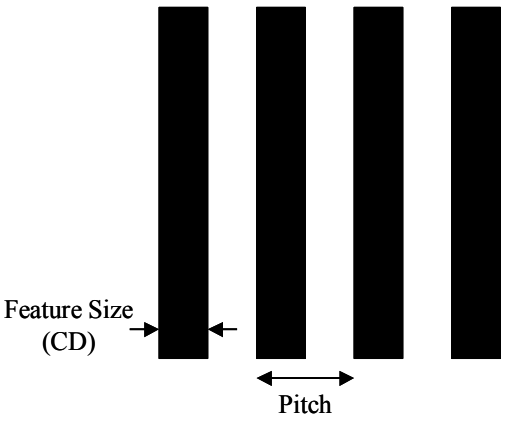
Motorola (Morone, 1993; Willyard and McClees, 1987) uses technology roadmaps to give business managers and other principals the comprehensive technology assessments required for a long range perspective of future product needs. The product technology roadmap is a compilation of documents providing a complete description of the product line, division, or operating group. The roadmap encourages use of structured tools in the planning and managing

of the complex technological environment, and furnishes a framework for review of present activities and progress.

This dissertation examines the ITRS in depth in subsequent chapters. As a brief introduction a few charts and tables from the 2003 ITRS are briefly presented. The principal metric of progress in semiconductor technology is device minimum *feature size*, or the process design rules for the smallest feature printed. Feature size is actually measured in different ways depending upon device type as described in Box 2-2.[15] For DRAM devices the metric is referred to as *half-pitch* or half the distance between the first-level interconnect dense lines. For logic devices such as microprocessors, transistor *gate length* is most representative.

Box 2-2. Device Minimum Feature Size—Key ITRS Metric

Optical lithography has been the mainstay of semiconductor patterning since the early days of integrated circuit production. The continual reduction of the dimensions of the features used to construct transistors has allowed these transistors to become ever smaller, faster, lower power-consuming, and cheaper. Historically, the smallest features on a wafer have been reduced in size by about 30% every two to three years. As a result, chips with features less than 100nm across are entering production today. Many technological barriers confront us when simultaneously shrinking transistor size and increasing the number of transistors on a chip. Ultimately, however, chip manufacturing has always been limited by our ability to print small features cost-effectively. As a result, the resolution limits of optical lithography tend to dictate the manufacturing capabilities of our industry. What limits our ability to print wafers with smaller dimensions? What are the implications of these limits to chip manufacturing?

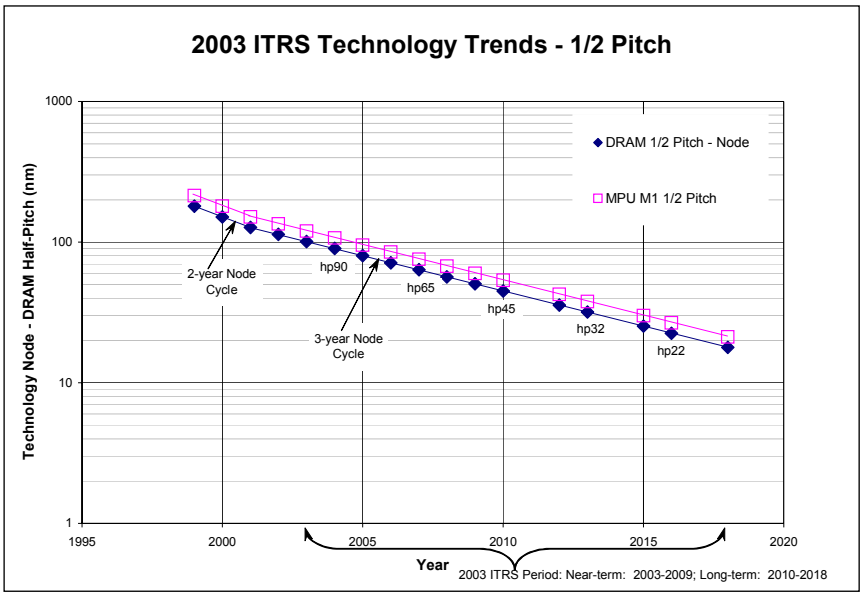


The resolution limit of optical lithography is not a simple function. In fact, resolution limits differ depending on what type of feature you are trying to print. In general, however, there are two types of resolution: the smallest pitch that you can print (the pitch resolution) and the smallest feature that you can print (the feature resolution). While related, these two resolutions are limited differently by the physics of lithography, and have different implications in terms of final device performance. Pitch resolution, the smallest linewidth + spacewidth pair that we can print, determines how closely we can pack transistors together on one chip. This resolution has the greatest impact on cost per function and functions per chip. Feature size resolution determines the characteristics and performance of an individual transistor, and has the greatest impact on chip speed and power

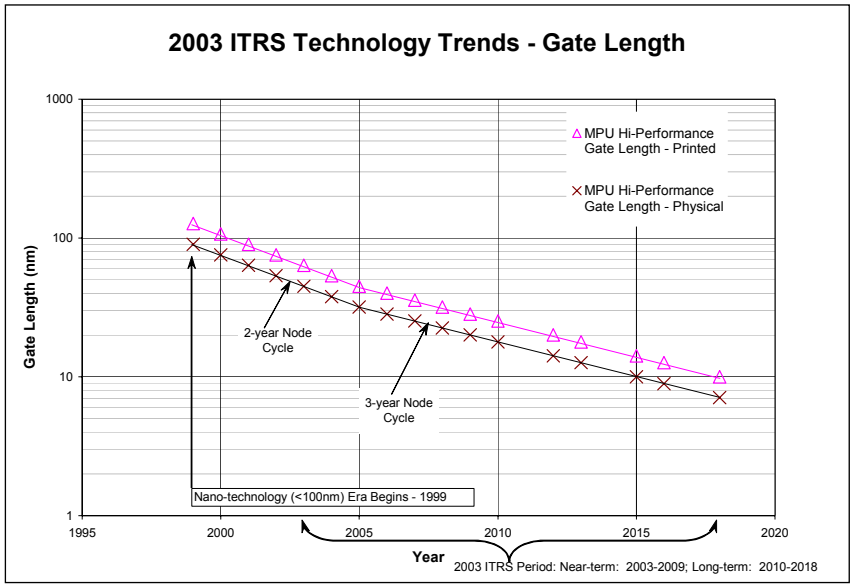
[15] Excerpted from Chris A. Mack, "Why is Semiconductor Lithography Hard?" manuscript obtained from the author, prepared October 15, 2003 for *Yield Solutions Magazine*. Mack is VP of KLA-Tencor FINLE Division, Austin, Texas.

consumption. Obviously both are very important.

The ITRS uses the term *technology node* as the targeted minimum feature size (presently half-pitch, see designation "hpXX" in Figure 2-9a) that represents future projections of leading-edge process technology. As will be discussed in subsequent chapters, *scaling* of ever smaller minimum feature sizes (or technology nodes or generations) is the legacy of the semiconductor industry. One major goal of the ITRS is to sustain this historic rate of technical advance as shown for both feature size metrics in Figures 2-9a and -9b.



(a)



(b)

Figure 2-9. 2003 ITRS Technology Trends

Source: *2003 ITRS*, Figures 7 and 8, 39-40.

Beginning with these high-level scaling assumptions (officially referred to as Overall Roadmap Technology Characteristics (ORTC)), technology requirements are mapped out in finer levels of detail within a dozen supporting technologies. Ultimately a comprehensive articulation of requirements is compiled as the ITRS. Table 2-1 shows a very small sample of tables that demonstrate the increased granularity found in the ITRS. Note that the 2003 ITRS contains more than 120 tables, most of which are multiple tables.

Table 2-1. Selected ITRS Tables

(a) Improvement Trends for ICs Enabled by Feature Scaling

TREND	EXAMPLE
Integration Level	**Components/chip, Moore's Law**
Cost	**Cost per function**
Speed	**Microprocessor clock rate, GHz**
Power	**Laptop or cell phone battery life**
Compactness	**Small and light-weight products**
Functionality	**Nonvolatile memory, imager**

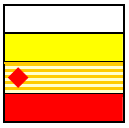
(b) ITRS Table Structure—Key Lithography-related Characteristics by Product Type

	Near-term Years								*Long-term Years*					
YEAR of Production	**2003**	**2004**	**2005**	**2006**	**2007**	**2008**	**2009**		**2010**	**2012**	**2013**	**2015**	**2016**	**2018**
Technology Node		**hp90**			**hp65**				**hp45**		**hp32**		**hp22**	
DRAM ½ Pitch (nm)	**100**	**90**	**80**	**70**	**65**	**57**	**50**		**45**	**35**	**32**	**25**	**22**	**18**
MPU/ASIC M1 ½ Pitch (nm)	**120**	**107**	**95**	**85**	**75**	**67**	**60**		**54**	**42**	**38**	**30**	**27**	**21**
MPU/ASIC Poly Si ½ Pitch (nm)	**107**	**90**	**80**	**70**	**65**	**57**	**50**		**45**	**35**	**32**	**25**	**22**	**18**
MPU Printed Gate Length (nm)	**65**	**53**	**45**	**40**	**35**	**32**	**28**		**25**	**20**	**18**	**14**	**13**	**10**
MPU Physical Gate Length (nm)	**45**	**37**	**32**	**28**	**25**	**22**	**20**		**18**	**14**	**13**	**10**	**9**	**7**

(c) Additional Design Technology Requirements

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*	*2012*	*2015*	*2018*	*Driver*
Technology Node		*hp90*			*hp65*						
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*	*35*	*25*	*18*	
MPU/ASIC ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	*57*	*50*	*35*	*25*	*18*	
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*	*20*	*15*	*10*	
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*	*14*	*10*	*7*	
SOC new design cycle (months)	**12**	**12**	**12**	**12**	**12**	**12**	**11**	**11**	**10**	**9**	SOC
SOC logic Mtx per designer-year (10-person team)	**1.9**	**2.5**	**3.3**	**4.3**	**5.4**	**7.4**	**10.6**	**24.6**	**73.4**	**113**	SOC
SOC dynamic power reduction beyond scaling (X)	**0**	**0.1**	**0.1**	**0.2**	**0.2**	**0.2**	**0.2**	**6**	**4.7**	**8.1**	SOC
SOC standby power reduction beyond scaling (X)	**0.37**	**1.4**	**2.4**	**3.4**	**5.1**	**6.4**	**8.73**	**18.8**	**44.4**	**232**	SOC
%Test covered by BIST	**20**	**20**	**25**	**30**	**35**	**40**	**45**	**60**	**75**	**90**	MPU, SOC

Mtx—Million transistors



Source: *2003 ITRS*, Tables A, B, and 19, 1, 7, 124.

Note also the color-coded boxes indicating the readiness of manufacturable solutions. This coding scheme is not that much different than the one used in Figure 2-5. While this initial descriptive analysis of the ITRS is brief, it does provide some basic understanding such as the commonality in roadmap designs that exists between generic formats and specific applications. Much more will be said about the ITRS in subsequent chapters.

As a counter-balance, two examples of unsuccessful roadmaps are briefly described in Box 2-3. These cases are a reminder that a roadmap (the document) is far less important than roadmapping (the process).

Box 2-3. Good Intentions: The *Road Map* to Peace and AMD's Internal Roadmap

Roadmaps and roadmapping have been used increasingly in many quarters of society. There seems practically no limit in usage beyond science, technology, or product-related applications where the process emerged. The *Road Map to Peace*, originally drafted by the U.S. State Department and since modified and endorsed by the group known as the "Quartet"—representatives of the European Union, Russia, the United Nations, and the United States, is the outcome of a speech given by President George W. Bush in June 2002 that laid out a vision of Israeli and Palestinian states living in peace. The U.S.-backed roadmap sets a series of benchmarks designed to move Israelis and Palestinians over three years to the creation of a Palestinian state that co-exists alongside Israel. The following State Department caption reveals that this roadmap incorporates many of the features commonly found in technology roadmaps:

> The following is a performance-based and goal-driven roadmap, with clear phases, timelines, target dates, and benchmarks aiming at progress through reciprocal steps by the two parties in the political, security, economic, humanitarian, and institution-building fields, under the auspices of the Quartet [the United States, European Union, United Nations, and Russia]. The destination is a final and comprehensive settlement of the Israel-Palestinian conflict by 2005…[16]

One noticeable difference though—other than the much broader socio-political application—is that authorship, thus ownership, of the roadmap was NOT by the parties affected. According to various sources, the Palestinians, Israelis, and other parties in the Middle East were consulted during the roadmap's development, but they did not directly participate in the plan's creation.[17]

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[16] U.S. Department of State, "A Performance-Based Roadmap to a Permanent Two-State Solution to the Israeli-Palestinian Conflict," Press Statement, Office of the Spokesman, Washington, DC, April 30, 2003, http://www.state.gov/r/pa/prs/ps/2003/20062pf.htm

[17] Sharon Otterman, "The Middle East: The Road Map to Peace," Updated: July 24, 2003, http://www.cfr.org/background/mideast_roadmap.php#

While peace in the Middle East is arguably very complex, this omission may help partly explain the lack of acceptance of the roadmap principles to date. Research into successful roadmapping practices consistently suggests that stakeholders must play an active role in roadmap development for it to ultimately be credible and useful. As an example, the 1999 ITRS was a significant milestone as the first *International Roadmap*, however many from the all-important equipment supplier and materials industry were very critical of the Roadmap's inaccurate timing of required technologies, particularly the transition to 300mm diameter wafers. One of the contributing factors was reduced involvement on the part of the supplier community. (Chapter 10 discusses this situation in more detail.)

Of course other preconditions are necessary. The ITRS has been successful partly because it follows decades of tradition and practice and has persisted from a strong leadership commitment behind it. Indeed the first semiconductor industry roadmap exercise, *Micro Tech 2000*, also met with much criticism as discussed in Chapters 9 and 10. Another roadmap experience that was short-lived was AMD's first internal roadmap, patterned after the recently-completed 1994 NTRS.

According to Don Wolleson, AMD's Director of Technology & Reliability Engineering, an effort was made in 1995 to create a similar technology roadmap for internal use within AMD. It was a large undertaking, involving about 70 people from throughout the corporation, and focused on both pre- and post-competitive areas. One of the principal aims of the internal roadmap was to develop an integrated *process* to better understand how all the technology pieces fit together. Wolleson had observed this unique value having been involved in Micro Tech 2000, the 1992 SIA Workshop, and the most recent 1994 NTRS and felt his company could benefit from such a collective and collaborative process. Unfortunately, not all groups within AMD shared Wolleson's vision as different factions viewed the roadmap with different (and sometimes conflicting)

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[18] Don Wolleson, telephone Interview, Aug 10, 1999.

expectations. For example, the marketing department saw the exercise as a marketing *forecast* while Wolleson tried to stress it as a technology *needs* statement similar to the SIA Roadmap where he had witnessed the dynamic nature of roadmapping toward a commonly-shared destination: "If people believe, then it becomes reality." But for AMD, the result fell far short of his expectations and the process was never repeated.[18]

As these examples illustrate, while the term *roadmap* finds its way into ever increasing applications, a full understanding and appreciation of the methods and practices of *roadmapping* continue to be major challenges for practitioners.

Principles of High Quality Roadmaps

The previous sections of this chapter have presented roadmap definitions, categorizations, and examples. One of the most interesting research questions arisen deals with determining and assessing quality and effectiveness of roadmapping processes and end products (roadmaps). The present section examines roadmaps from a product quality perspective, and proposes requirements and principles for generating high quality roadmaps.

Assessment of Roadmap Quality and Effectiveness

One major problem in assessing the published roadmaps is the inability of the reader to ascertain their quality. There are no independent objective tests of quality. Unlike the physical and engineering sciences, there are no primary physical reference standards against which one can benchmark the roadmap product.

Even the metrics of roadmap quality are unclear, as illustrated by the following example. Assume a prospective technology-push roadmap has been constructed for high energy-density batteries. Suppose further that fifteen years after the roadmap was developed, an assessment was performed of the roadmap predictions as compared to the battery state-of-the-art. Suppose

even further that the assessment showed that the roadmap development plan was followed religiously by the technical community, and the long-range technical goals were achieved exactly as predicted by the roadmap. Does that mean the roadmap was of high quality?

Not necessarily. The roadmap developers may have been very conservative in their targets, and did not 'push the envelope' to develop the field as vigorously as technology would have allowed. The developers may also have been very narrow in their outlook, and may not have drawn from other disciplines sufficiently to develop the batteries to the greatest extent. It could be stated that the roadmap was precise (in predicting the goals that were actually achieved), but was not visionary (the best goals were not predicted). On the other hand, the roadmap in this case may have been of the highest quality. The developers may well have had very ambitious targets, and may have drawn from other disciplines to the maximum extent possible.

A case in point is the ITRS. One could easily say that the ITRS has failed if measured simply on its forecast accuracy. It is widely recognized that future technology nodes (or generations) projected in previous roadmaps have, in fact, consistently been "pulled-in" or accelerated. Many argue that the roadmap process itself—consensus-driven, yet competitively challenging—has contributed to the behavior observed throughout the industry to 'beat the roadmap'. In evaluating the overall success of the Roadmap, most view technology acceleration as a very positive consequence.

The point to be made here is that the concepts of roadmap quality, and its associated metrics, are very complex and diffuse, yet very important if roadmaps are to become useful operational tools. A high quality roadmap, then, requires the following conditions:

1. The retrospective component must be a comprehensive reflection of the evolution and relation of all critical S&T that resulted in the technology of present interest,
2. The present time component must be a broad and comprehensive reflection of all critical S&T related to the technology of interest, and
3. The prospective component should reflect some degree of vision by the planners and should incorporate all the critical S&T areas that relate to the technology of interest and to the projected targets. The broader the reach across the S&T spectrum, the greater the opportunity for extrapolating insights and innovations from allied or disparate disciplines

to advance the technology of central interest.

Thus, a high quality roadmap is analogous to a high resolution picture that clearly portrays the evolving relationships among S&T areas as they pertain to the roadmap technology in focus, and incorporates especially the concepts of awareness, coordination, vision, relatedness, and completeness.

Critical Factors to High-Quality Roadmaps

More specific requirements, or underlying principles, necessary for a high quality roadmap can be formulated. These include:

- *Senior Management Commitment* The most important factor is the commitment of the roadmap-developing organization's senior management with decision authority to high-quality roadmaps, and the associated emplacement of rewards and incentives to encourage such roadmaps. This includes a commitment to a strategic long-term roadmapping process, not just an independent one-time exercise.
- *Role of Roadmap Manager* The next important factor is the roadmap development manager's motivation to construct a technically credible and visionary roadmap. The roadmap manager sets the boundary conditions and constraints on the roadmap scope, structures the working groups, and selects the final roadmap elements from myriad inputs. In some organizations, the roadmap manager has the latitude to establish the complete roadmap development process and criteria, and decide on the make-up of roadmap participants with the requisite expertise.
- *Competence of Roadmap Participants / Team* The development experts' competence and objectivity are extremely important. Each expert should be technically competent in his/ her subject area, and the competence of the total roadmap development team should cover the multiple research, technology, and mission / product-line areas critically related to the science or technology area of present interest. In addition, the team's focus should

not be limited to disciplines related only to the present technology area (that tends to reinforce the status quo and commit development along very narrow lines), but should be broadened to disciplines and technologies that have the potential to impact the overall roadmap's highest-level objectives (that would be more likely to provide equitable consideration to revolutionary new paradigms or innovations).

- *Stakeholder-Driven* A roadmap should have a clear sense of purpose and ownership for it to be successful. Thus, industry roadmaps are most successful when driven by industry, even if government, universities, and consortia are big players in the process. Likewise, product-technology roadmaps are best done by those responsible for the outcome (e.g., the product manager).

- *Normalization and Standardization* For roadmaps that will be used as a basis for comparison of S&T programs or projects, another important factor is normalization and standardization across different roadmaps, development teams, and S&T areas. For S&T areas that have some similarity, use of common experts (on the development teams) with broad backgrounds which overlap the disciplines can provide some degree of standardization. For very disparate S&T areas, some allowances need to be made for the relative strategic value of each discipline to the organization, and arbitrary corrections applied for benefit estimation differences and biases.

- *Roadmap Criteria* Criteria for roadmap component selection are also required. For retrospective roadmaps, that tend to focus on the critical S&T events that led to successful technologies / systems, the definition of criteria for 'successful' and 'critical' is of utmost importance for establishing the credibility of the roadmap. In all roadmaps, it is crucial to define criteria for selecting nodes, quantifying nodes, and quantifying links.

- *Reliability* A factor of equal importance to criteria is reliability or repeatability. To what degree would a roadmap be replicated if a completely different development team were

involved in its construction? If each development team were to construct a completely different roadmap for the same topic, then what meaning or credibility or value can be assigned to any roadmap? To minimize repeatability problems, a large segment of the competent technical community (to the degree possible within organizational constraints) should be involved in the construction and review of the roadmap.

- *Relevance to Future Actions* Another factor of equal importance to criteria is the relevance of the roadmap to future actions:

  Every S&T Roadmap, and associated data, presented in a study or briefing should have a decision focus; it should contribute to the answer of a question which in turn would be the basis of a recommendation for future action.

  Roadmaps which do not perform this function become an end in themselves, offer no insight, and provide no contribution to decision-making.

- *Cost* An additional critical factor is cost. The true total costs of developing a high quality roadmap with substantial community input can be considerable, but tend to be understated. For high quality roadmaps, where sufficient expertise is represented on the development team, the major contributor to total costs is the time of all the individuals involved in developing and reviewing the roadmap. With high quality personnel involved in the development and review process, time costs are high, and the total development costs can be non-negligible.

- *Global Data Awareness* A final factor is global data awareness. A quality roadmap should include all global S&T projects, developed systems or operations, or events, that are in any way supportive of or related to the overall roadmap objectives. This factor is foundational to S&T investment strategy, and how a program or body of S&T is planned, selected, managed, coordinated, integrated, and transitioned. It is imperative that the latest information technology resources be used to the greatest extent possible during the

complete roadmap development process to insure that global S&T resources are being exploited maximally.

Summary

Roadmapping has been practiced by some organizations for decades (and much longer under other titles), but the broader adoption of roadmapping practices is still relatively new. This chapter has attempted to display the underlying unity of seemingly fragmented roadmap approaches, and to develop characteristics and principles of high quality roadmaps. This concluding section adds some recommendations for consideration and future research.

Functional Roadmaps

From a technology planning and assessment perspective, roadmaps are fundamentally visual display aids that crystallize the linkages among the existing or proposed research programs, development programs, capability targets, and requirements. Because of the inherent uncertainties in research and development, as well as the continually evolving requirements and capability targets in large programs, roadmaps should have a sufficiently flexible structure to incorporate these dynamic changes. Thus, the linkage relationships should be functional, not static, and changes inserted at any node in the roadmap network should automatically impact the other network nodes through the linked functional relationships.

Thus, a useful roadmap for technology planning should provide the planners with the capability to perform sensitivity studies of the relationships between capability targets / requirements and program cost / performance / schedule / risk, and allow the planners the flexibility to specify changes of any parameter at any node in the network. It should have the flexibility to answer questions such as:

- If the downstream requirements targets for a development program are increased, what new performance / funding / schedule requirements are imposed on the component technology programs.
- If a new research program is initiated in a large scale development program, what

implications does it have for downstream capability targets, other technology program parameters (funding, performance targets, schedule), and what are its other potential impacts on capability targets beyond those of the specific development program.

- If the funding for an ongoing technology component of a large scale development program is reduced by some amount, what are the implications for achieving downstream capability targets by the designated milestone, and how should the other technology programs be modified for optimal resource expenditure.

To insure compatibility among: (1) the research and development programs that underlie the tactical and strategic plans; (2) feasibility of defined capability targets; and (3) technology program / project requirements, roadmaps that contain all these elements should be constructed. For completeness and operational utility, the roadmaps for a technical area should cover all global programs directly or indirectly related to that area's technology. Roadmaps that are restricted to internal agency or corporate programs only could be misleading, and could provide the basis for erroneous conclusions, recommendations, and decisions. These incomplete roadmaps would portray fragmented and isolated non-coordinated programs, where none of these gaps might exist in reality. This requirement for comprehensive coverage underscores the need for roadmapping to be integrated with other decision aid processes and tools within the organization, such as information retrieval and data mining capabilities.

Roadmaps and Roadmapping Integration

To be most effective, roadmapping and other management decision aids need to be fully integrated into the strategic planning and business operations of the organization (Peet, 1998). Employment of roadmaps in a band-aid or afterthought mode will result in a fragmented product with limited potential for organizational implementation. The combination of roadmapping with strategic planning, information retrieval, data mining, technology evaluation, and organizational performance metrics, has to be addressed well in advance of the implementation of a roadmapping process.

Finally, Radnor and Probert (2004) offer a more current reflection of lessons-learned from roadmapping in Box 2-4.[19]

Box 2-4. What We Have Learned (About Roadmapping)

Having presented the 11 individual papers contained in the two parts of this roadmapping special report, we can now identify a number of overall and cumulative messages:

* Roadmapping has evolved from, and appears to meet, the increasing need of firms (varying by size, type, etc.) to innovate with greater cost-effectiveness than in the past, with enhanced strategic focus, greater development and deployment speed, more coherent decision making, better cross-organizational integration and communication, and with discipline.

* Roadmapping methodologies are continually evolving. A number of different and useful ways to roadmap have already developed, and more are likely.

* Firms need to learn and adapt as they adopt roadmapping. Not only does what is needed and possible change over time, but so, too, may the drivers and constraints of the firm's context and its management, with their varying operational philosophies, etc. Firms will differ in how they progress through an evolutionary pattern in which they establish the culture, trust and knowledge/data bases that can support internal roadmapping. This builds the needed foundation for involving other players (suppliers, customers and partners) and for adopting more programmed systems.

* Returning to and concluding with a message contained in the first part of this report, roadmapping must be recognized as a linchpin management tool that can help support integration with other needed strategic and operational management processes-it does not stand alone. And, bottom line, it is "roadmapping" that delivers results; the focus cannot be on just the "roadmaps."

Other deficiencies and limitations of roadmaps are included in Appendix D. The bibliography of referenced material is also in the appendix.

[19] Excerpted from Michael Radnor, David R. Probert, "Viewing the Future," *Research Technology Management*, Mar/Apr 2004, Vol. 47, Iss. 2, 25-26.

CHAPTER 3: The Complexity Challenge of Industrial Innovation in Semiconductors

"There are many systems for which there is no theory and no team of people who understand the whole thing."

- Joe Weizenbaum, MIT[1]

"When I was a process engineer, you could do everything, you could actually make an integrated circuit. Now, no one person could even come close to making an integrated circuit."

- Mike Splinter, Intel[2]

"Bob Noyce once told me when he was a kid he opened up the hood of his car, he could see the pistons moving and he could understand how it worked and he said today, you know, you open up the hood of a car and you wonder where the engine is... it's that complex."

- Regis McKenna, industry pioneer[3]

"In our industry, difficult things need to get done right away. Impossible takes a little longer."

- Ashok Sinha, Applied Materials[4]

Technological innovation of semiconductors has evolved from the early days of great discoveries by individual inventors like Shockley, Kilby, and Noyce to a global enterprise involving many thousands of people, few of whom will ever become well known. The complexity of today's multimillion- and now billion-circuit chips is mirrored only by the complexity of today's innovation system of organizational networks. The purpose of this chapter is to begin to provide the

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[1] Quoted in Michael Orme, *MICROS: A Pervasive Force, A study of the impact of microelectronics on business and society 1946-90*, London: Associated Business Press, 1979, 118.
[2] Quoted in *Micro Magazine* interview http://www.micromagazine.com/archive/00/03/microinterview.html
[3] Quoted in "Silicon Genesis: Oral Histories of Semiconductor Industry Pioneers," Interview with Regis McKenna, Hosted by Rob Walker, Palo Alto, California, August 22, 1995, http://www.stanford.edu/group/mmdd/SiliconValley/SiliconGenesis/RegisMcKenna/Mckenna.html
[4] Ashok Sinha, President of Applied Materials' Metal Deposition Product business group, quoted in Dylan Mcgrath, "Challenges to Moore's Law Cited," *Electronic News*, Sep 21, 1998.

conceptual framework for the research into the Roadmap and the Roadmap process. Important concepts from Complexity Science have been selected to inform this study. This chapter and the next chapter provide the theoretical context for analysis of the Roadmap process. The chapter begins with a brief discussion of the importance of the Roadmap to sustained industrial innovation. Following this is a detailed description and application of complexity science concepts that draws heavily from *The Complexity Challenge: Technological Innovation for the 21st Century* by Rycroft and Kash (1999).[5] Additional sources are referenced throughout this analysis including excerpts of findings from this study discussed in greater detail in later chapters. The chapter ends with a brief assessment of complexity science concepts as they pertain to this analysis of the Roadmap's creation, evolution, and future development.

The Roadmap and Industrial Innovation

Innovation is usually anything but organized. As has been said, "One should recognize and manage innovation as it really is—a tumultuous, somewhat random, interactive learning process linking a worldwide network of knowledge sources to the subtle unpredictability of customers' end uses."[6] However, this dissertation will demonstrate that technological innovation in semiconductors has become a very organized endeavor. The creative process of turning ideas into new products and processes has been highly refined through institutions including coordinating mechanisms and management tools embodied in technology roadmapping methods and practices. Roadmapping offers a new dimension to innovation by bringing together a broad base of participants whose collective knowledge is applied to the question "Where are we headed and how are we going to get there?" Roadmapping is a collaborative planning exercise that helps align and organize knowledge essential to innovation, thus the notion *organized innovation*. The uses and benefits of roadmapping are many as previously discussed, but in this chapter the role that the Roadmap plays in the semiconductor industry's international innovation system will be

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[5] Rycroft and Kash, *The Complexity Challenge*, op. cit.
[6] James Brian Quinn, quoted in Richard N. Foster, *Innovation: The Attacker's Advantage*, New York: Summit Books, 1985, 239.

considered. If one can imagine the benefits accrued from organizing knowledge through use of knowledge management systems, roadmapping adds value to this process by providing the collaborative process element with the express goal of planning a technology path to the future. Thus, roadmapping also becomes a key source of information into the semiconductor community's knowledge management system.

The semiconductor industry's Roadmap is a document that captures the most current technical information available regarding pre-competitive process technologies. In this sense it is a kind of semiconductor technology almanac. More importantly though, the Roadmap is a process that distills knowledge from the international semiconductor community critical to sustained innovation of the technology. To remain credible, the Roadmap process must continue to be more inclusive and comprehensive while not becoming unwieldy. Although labeled a 'technology roadmap' the Roadmap incorporates economic, political, even cultural variables through such broad participation (the 2003 ITRS involved more than 900 participants). The universality of the Roadmap's appeal is reflected in its continued, expanded involvement from individual firm to industry to international scope. A few comments from informants emphasize the important coordinating role of the Roadmap:

> The Roadmap has catalyzed the continued orderly advancement of the integrated circuit... The Roadmap process may be the most important product of semiconductor industry cooperation. (Bob Burger)
>
> This Roadmap provides a realistic, globally synchronized approach to what we can expect technically for our industry in the future. (Paolo Gargini)
>
> The ITRS represents an up-to-date, global industry consensus on the technical challenges that our industry will address. Each challenge is also an opportunity for the semiconductor community to add to the history of breakthrough achievements upon which the growth of our industry has been based. (Bob Doering)

A major Roadmap ingredient is the evolution of industry collaboration as will be revealed in subsequent chapters. For example, the semiconductor industry was originally vertically integrated; IBM, TI, Fairchild, Motorola, and other chip makers all did everything in-house in the

1950s, 1960s, and even into the 1970s.[7] By the 1970s this approached was no longer appropriate for many chip makers. Developing every tool and process for each new design revealed that individual firms just did not have enough knowledge and typically insufficient market to recoup such a large investment. It was in this time period that the semiconductor materials and equipment (SM&E) industry began to firmly establish itself. Outsourcing manufacturing equipment and materials—and later entire manufacturing or fabrication processes—necessitated greater industry collaboration. This collaboration manifested itself in many ways including research consortia such as the SRC and Sematech. It was also the impetus for the Roadmap. Thus the increased complexity of the organizational arrangements charged with technological innovation—including the Roadmap—in many ways mirrors the increased complexity of semiconductor technology and industrial structure.

Management of innovation is critical in today's fast-paced, competitive environment. The pace of innovation must quicken as product life cycles continue to shorten. The resultant constant state of flux is the pinnacle of Schumpeter's "gales of creative destruction" view of innovation and entrepreneurial spirit. The challenge to participants in this new industrial game is—at a minimum—to maintain parity with the rest of the pack (i.e., adopt so-called best practices). The bigger challenge is to be the benchmark, to set the pace, to lead the business environment and influence its direction. Driven by continuously seeking competitive advantage, today's organizations have come to accept innovation as a given, while a growing number embrace innovation as a core attribute and have implemented processes to manage innovation in the same fashion as management of other critical factors of production such as human and physical capital. Contemporary innovation management goes well beyond the traditional linear or pipeline model of innovation springing forth from research and development activities (i.e., research → development → commercialization). Today's innovation practices involve access to knowledge

[7] The author worked for Digital Equipment Corporation (DEC) in the 1970s and 1980s during which the company built its own chip fabrication facility in Hudson, MA for microprocessors (including later the powerful 64-bit *Alpha* chip) and other special purpose chips used in the firm's minicomputer product lines. Intel now owns and operates the facility.

throughout the enterprise and externally into the network and broader technology complex of which it is a part. Coordination, cooperation, collaboration, sharing, and similar terms are all part of the common vocabulary in contemporary organizational strategic planning and operations.

As mentioned, billion-circuit semiconductor chips are certainly complex in both design and fabrication. But increasing complexity is not solely a technology concern. The competitive context especially is increasingly complex. Complexity comes from the point that competition is played out on a wider and wider variety of dimensions.[8] Organizations continue to evolve from traditional vertical designs to horizontal and network structures that reach throughout the supply chain. This is where roadmaps enter the picture. A roadmap is the culmination of a comprehensive assessment and forward-looking process that becomes a vital tool to innovation managers. Done properly, roadmapping represents an important component of a coordinated or organized innovation process that enables an organization to maintain and exploit its competitive advantage. This thesis delves into the Roadmap process and illustrates the crucial role it plays in sustaining international industrial innovation. To begin, a conceptual framework offered by Complexity Science provides a basis for this analysis.

Complexity Science and the Roadmap

Complexity Science (or Theory) first appeared in the physical sciences, but increasingly scholars have argued that this set of ideas can also be of great value in understanding the functioning of social systems.[9] In an essay that relates closely to the unique nature of the Roadmap, Innes and Booher use complexity science to help explain the emergence of consensus building and other forms of collaborative planning behavior.[10] As background, the authors refer to

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[8] Vittorio Chiesa & Raffaella Manzini, "Towards a Framework for Dynamic Technology Strategy," *Technology Analysis & Strategic Management*, Vol. 10, No. 1, 1998, 111; see also Michael Porter, *Competitive Advantage*, New York: Free Press, 1985.
[9] Judith E. Innes and David E. Booher, "Consensus Building and Complex Adaptive Systems: A Framework for Evaluating Collaborative Planning," *Journal of the American Planning Association*, Vol. 65, No. 4, Autumn 1999, 416.
[10] Ibid.

the traditional mechanistic view that has dominated Western thought since the age of Enlightenment, quoting Capra's description as 'world as machine':

> Like human-made machines, the cosmic machine was thought to consist of elementary parts. Consequently, it was believed the complex phenomena could always be understood by reducing them to their basic building blocks and by looking for mechanisms through which these interacted. This view has become deeply ingrained in our culture and identified with the scientific method. The other sciences accepted the mechanistic and reductionistic views of the classical physics as the correct description of reality and modeled their own theories accordingly.[11]

Thus, with adequate theory, accurate observations and appropriate inputs, the behavior of a machine or system—small and large—may be understood, predicted, controlled, and even *fixed* through intervention. However, as the authors point out it has become all too obvious that interventions (e.g., public policies or corporate strategies) seldom work as intended. The machine metaphor simply does not accurately describe consensus building and the Roadmap process, much less the social world. Machines can be duplicated, they may react in predictable ways, however they experience entropy over time.

Complexity theory, in contrast, offers a more appropriate explanation of social systems that evolve continuously and unpredictably. They interact with and change their environments while they are at work, and may even gather energy rather than lose it as they move forward. Hence, a complexity theory view of the world fits these characteristics far better than a mechanistic view. Box 3-1 excerpts an overview of major concepts, terminology, and definitions of complexity science.

Box 3-1. Complexity Science Overview

"The World as Organism"[12]

Scholars of complexity contend that complex systems mimic organisms in their behavior in uncertain, changing environments. A machine is designed to do a specific task in a defined context, but an organism can adapt and change in response to information it gathers from its environment. It develops new activities and evolves as it "learns" about that environment. This learning occurs as individual "agents," which might be ants in an ant colony, molecules in the human body, or computer-generated actions in a larger program, randomly move through their

[11] Ibid., see Capra, F., *The Turning Point*, New York: Simon and Schuster, 1982, 47.
[12] Ibid., 417.

environment and respond to feedback by changing their actions. The ants, with their tiny brains and limited sensory capacity, quickly mobilize in large numbers to capture a bit of food left on the kitchen counter. Molecules change in a random way at first, but the most effective forms persist and develop further. A system made up of "dumb" individual agents can, as a whole, show tremendous intelligence, learning capacity, and ability to adapt and even innovate.

The hallmark of complex adaptive systems is "emergence." Much can emerge from little. Emergence is the idea that simple elements that are governed by a few simple rules and operate through trial and error with interaction and feedback can produce persistent and systematic patterns that are quite unlike the original elements. The elements and agents that work best are those capable of collecting resources and generating new variants. Those which cannot do this die out. The interactions among the simpler elements of the system produce higher or more complex levels of component organization, similar to the way atoms interact to form molecules, molecules to form cells, and cells to form organs. The result is increasing competence of the system as a whole in the form of greater productivity, stability, or adaptiveness.

A complex adaptive system emerges in nature when the environment is unstable, but not completely chaotic. Stable environments lead to systems in equilibrium, which are not likely to adapt if major changes occur. In chaotic environments, systems cannot find productive patterns. At the edge of chaos—a good analogy to the current period of social transformation—innovation and dramatic shifts in activity patterns can occur, and systems can move to higher levels of performance. Such innovation, however, depends on information flows through linked networks of agents. Consensus building can provide such links and help participants to do their individual parts in the larger system.

Thus, complexity theory—or more precisely, the science of complexity—is the study of emergent order in what are otherwise very disorderly systems. Whether spirals in whirlpools, funnels in tornadoes, flocks of birds, schools of fish, all are examples of orderly behavior in systems that are neither centrally planned or centrally controlled. In summary, complexity science is the study of complex adaptive systems that exhibit emergent behavior and produce self-organized structures. The Roadmap is such a structure. To better understand how this has occurred, a more in-depth examination of complexity science principles is required.

The Complexity Challenge

The Complexity Challenge is a comprehensive look at innovation policy against the backdrop of complexity science and evolutionary economics. The book investigates the fundamental rethinking required by the transition to an innovation system whose guiding intelligence is no longer the traditional central source such as an industrial R&D organization, but emerging self-organizing networks. Emergence, self-organization, and related concepts offer new insight into

understanding the Roadmap and the semiconductor industry of which it is a part. Concepts will be addressed in the following order: Increasing Complexity; Emergence and Self-Organization; Networks and Network Learning; Tacit versus Explicit Knowledge; and Path Dependence and Increasing Returns. An additional concept—Emerging Innovation Patterns—will be addressed separately in the next chapter. Together, these two chapters form the theoretical foundation for this study. As a set-up to the ensuing discussion of Complexity Science concepts the following paragraphs are offered.

Hiroshi Tasaka has coined the phrase "complexity knowing" and emphasizes that through "knowing" the whole as the unit of analysis, as opposed to our penchant toward the reductionist scientific method, we are offered new insight into a complex object, such as the Roadmap or the semiconductor industry more generally:

> Up until now, whenever we encountered a complex object, in order to understand it we would first break it down into simple components of a readily analyzable size. We would then analyze each component minutely, and finally we would synthesize the results.
>
> It is, of course, precisely analysis of this sort that has supported the present advances in science and technology. But as science and technology have developed, the limitations of the analytical method have become apparent (i.e., the fact that something important is lost when an object is reduced to its component parts). Why is this the case? Because it is a characteristic of the world we live in that, as something becomes more complex, it acquires new properties.[13]

Tasaka argues that something very important could get lost in the process of traditional analytical methods. He continues:

> Thus, the world intrinsically is a living system that cannot be reduced to a collection of its components, because the instant it is broken down into parts it loses its life force. In this sense, it resembles a fish, which, after being cut up, dissected and studied minutely, can be sewn back together and restored to its original shape, but it can never regain its essential form as a living, breathing fish.[14]

Alan Allan, Staff Marketing Engineer at Intel, heads the ITRS Overall Roadmap Technology Characteristics (ORTC) process. This is a critical function that establishes baseline parameters

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[13] Hiroshi Tasaka, "Twenty-first-century Management and the Complexity Paradigm," *Emergence*, Vol. 1, No. 4, 1999, 116.
[14] Ibid., 115-6.

and performance specifications that individual technologies must meet in order for the Roadmap goals to be realized. Allan's Roadmap involvement is extensive and dates back more than ten years. In response to a question on industry R&D trends, Allan considered the bigger picture—in much the same fashion as Tasaka's complex object—by describing industry R&D in the context of a broader "ecosystem." He relates the development of the Roadmap in this larger landscape and uses the term "industry government" to refer to the need for common infrastructure. Similarly, Andrew Grove has referred to the semiconductor industry as an example of a bottoms-up "industrial democracy."[15] Allan suggests that membership in this community implies a self-imposed obligation toward the collective welfare of the industry:

> There is an industry government in this sense. Take the example of wafer size. Intel funded 6" or 150mm wafers, IBM funded 8" or 200mm wafers. The rest of the industry benefited. But the "sugar daddy" approach won't work any longer due to economics, which is now the "holy grail." 12" or 300mm wafers require tens of billions of dollars to develop so a collective approach was taken through a consortium [I300I]. Also, the equipment industry was asked this time to pay more of a share—basically they were asked to pay their own way. A consortium is much like an R&D tax. How much government do you want and how do you pay for it? R&D is not yours today, it's more like savings so you must have a long view. How then do you collect taxes to fund infrastructure? Through big prices and profits. Thus, the industry government imposed a $10B tax for 300mm from the profits of companies that paid for development.
>
> R&D is like a flat tax or one-time lump sum funded on a sales tax basis from the profits from current sales. In this business there's a complex interaction at all levels of the semiconductor ecosystem. Funding mechanisms include labs, universities, and R&D consortia. Companies—both device makers and suppliers—have their own R&D with a product emphasis. All this ensures minimum missteps.

Allan then explains the coordinating role of the Roadmap within this cooperative scheme. He suggests the Roadmap as a "natural extension" of the industry's evolutionary development:

> The Roadmap is not an exact science. Long lead times (1-3 years) plus lots of zeros in investment are guided with the help of the Roadmap. Remember that the Roadmap doesn't cause anything to happen directly—collectively it's a compromise. So far, the Roadmap has helped collectively guide universities, labs, and consortia, and now it's being taken to another level: at the international level. We might naturally move into it without a lot of government involvement. The engineering community just seems to do this without a lot of resistance. These are real people in real companies sharing on real projects—you can't abstract or generalize.

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[15] Andrew Grove, "How Intel Makes Spending Take Off: Interview," *Fortune*, February 22, 1993, 57.

> The ITRS is thus a natural extension of all these things—especially cooperation—happening at the right time. The interdependencies are huge, worldwide change is occurring politically, economic progress is well underway, the industry is structurally ready. For example, IBM, Intel, others are already multinationals. There are also strategic alliances and partnerships, other relationships already there. There's appropriate awareness that you've got to be a cooperative team player.[16]

More will be said later about the industry transition from 200mm to 300mm diameter wafers. Suffice it to say now though that viewing the Roadmap within the context of the broader global semiconductor community offers much more insight than simply seeing it as a component part.

Increasing Complexity

> "All complex, adaptive systems—economies, minds, organisms—build models to allow them to anticipate the future." (John Holland)

This quote captures the evolutionary nature of complex systems: to anticipate the future, to reduce uncertainty, to make decisions today that will influence outcomes tomorrow. The Roadmap is the product of a complex, adaptive system; namely the semiconductor community that has a strong tradition of advancing technology at a relentless, yet regular pace. In the midst of a changing external environment, the Roadmap provides the necessary cadence to help coordinate innovation across a global community. In this sense, the Roadmap is an example of a "model" that Holland refers to above.

Rycroft and Kash examine the increasing role of *complexity* as a major explanatory variable in today's innovation environment. The authors define complexity as the general condition of contemporary processes, products, and entire systems that are gradually becoming more difficult to understand due to increased scale and scope (see earlier Weizenbaum quote). A common—but not the only—measure of complexity is the number of component parts per system (e.g., a modern automobile engine). Dasgupta cites Herbert Simon's 1962 article, "The Architecture of Complexity," that articulates the nature of complexity as it is manifested in both the natural and the artificial worlds. A system, according to Simon, is deemed complex if it is composed of a large

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[16] Alan Allan, telephone interviews, August 20, 1999 and March 15, 2000.

number of parts or components that interact in non-obvious ways. In such systems, even if one knows the properties of the components, it is a far from trivial manner to infer the properties of the whole. In a complex system, the whole is indeed more than the sum of its parts.[17] Rycroft and Kash found literally dozens of varying definitions for complexity, including Simon's. For their purposes, they chose a cognitively-based definition.

In the context of technological innovation, the book distinguishes between simple and complex technologies. A *simple technology* is a process or product that can be understood and communicated fully by *one individual* across time and distance to other experts. In contrast, a *complex technology* is a process or product that *cannot* be understood in full detail by an individual expert sufficiently to communicate all the details of the process or product across time and distance to other experts. Thus, complexity in this context is primarily concerned with the capability of an individual to fully comprehend and articulate technological knowledge. The authors argue the *complexity challenge* faced by today's managers is uneven, unrelenting change in systems that are too complex for them to understand.[18]

Moreover, the transition from simple to complex technologies that is well underway has not resulted from a great conceptual breakthrough or great invention as in previous eras. Rather, it has happened *silently* as technological, economic, and social systems have become incrementally more complex. One illustration of this involves an analysis of the composition of U.S. product exports over a 25-year period. In 1970 products classified as "simple" in both design and production process represented 47% of U.S. exports. An example of a simple product/process is crude oil. By 1995 the simple category had dropped by more than half to 22%. In contrast products classified as "complex" in design and production made up 38% of the total in 1970, but had increased to 56% by 1995. Semiconductor devices are considered complex

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[17] Subrata Dasgupta, *Technology and Creativity*, New York: Oxford University Press, 1996, referencing H.A. Simon, "The Architecture of Complexity," *Proc. Amer. Phil. Soc.*, 106 (Dec. 1962), 467-482. Reprinted in *The Science of the Artificial.*

[18] Ibid., 7, also see Margaret J. Wheatley, *Leadership and the New Science: Learning About Organization from an Orderly Universe*, San Francisco: Berrett-Koehler Publishers, 1992.

products using complex processes.[19] Not only had the product landscape changed significantly, the overall success rate—as measured by trade balances comparatively with Japan—had not been favorable for the U.S. in the growing complex product/process category. Between 1980 and 1995, Japan had more than doubled its trade surplus in this category (to $174 billion) while the U.S. watched a surplus reverse into a sizable deficit ($52 billion). Over the intervening period, the value of the yen against the dollar had doubled, which made Japanese exports relatively more expensive. And at the end of the period, Japan was in the midst of its worst recession since WWII.[20]

Nothing better supports the trend toward increased complexity than the semiconductor industry. In terms of the chip fabrication process, Steinmueller states, "Integrated circuit production processes are among the most complicated manufacturing techniques ever devised and utilize knowledge from almost every discipline of the physical sciences."[21] For example, the number of manufacturing steps doubled between 1980 and 1990. It tripled between 1990 and 1995 and was expected to triple again before 2001.[22] Fabricating semiconductor devices requires a unique combination of both capital- and research-intensity that has few corollaries. For example, a chip fabrication facility or "fab" cost about $100 million in the mid 1980s and had an expected life span of nearly 10 years. Today, similar fabs cost upwards of $3 billion and have a life span of only five years. On the research side, R&D budgets have traditionally averaged 15% of revenues, far above the national average and most other industries. Ham, Linden, and Appleyard briefly describe the complexity in semiconductor manufacturing:

> Semiconductor manufacturing processes … are among the most complex in any industry. The fabrication of an integrated circuit (also known as a "chip" or "device") requires more than a hundred steps (such as patterning, coating, baking, etching) across a range of specialized tool sets. An average fabrication facility in 1997 utilized about 40 different types of equipment, with individual tools ranging in price from $100,000 to $7 million. The

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[19] Standard Industrial Code (SIC) No. 3674 represents Semiconductors and Related Devices.
[20] Ibid., 10.
[21] William Edward Steinmueller, *Microeconomics and Microelectronics: Economic Studies of Integrated Circuit Technology*, Ph.D. Dissertation, Stanford University, March 1987, 1.
[22] Douglas Scott and Robert Pisa, "Can overall factory effectiveness prolong Moore's Law?" *Solid State Technology*, March 1998, 75.

> individual manufacturing steps are often mastered in an experimental rather than a scientific level and are difficult to replicate on different tools or in different facilities. Such complexity has historically required manufacturers to work closely with equipment suppliers to improver the performance of each tool.[23]

Note that today's state-of-the-art photolithography exposure tool that transfers the device image pattern onto the wafer, is the most expensive individual tool in a fab. In 1970 a photolithography machine could be purchased for about $15,000. Fifteen years later the cost had reached $700,000 per unit. A current 193-nanometer-wavelength stepper costs about $15 million. That is a thousand-fold increase in price in a little more than three decades. Furthermore, it is estimated that the Extreme Ultraviolet (EUV) lithography tool, slated to replace conventional lithography equipment, may cost in excess of $50 million by the time it reaches the market in 2009 or so.[24] At the device level, the three-decade evolution of the family of Intel microprocessors clearly demonstrates the increased complexity of semiconductor devices as shown in Figure 3-1:

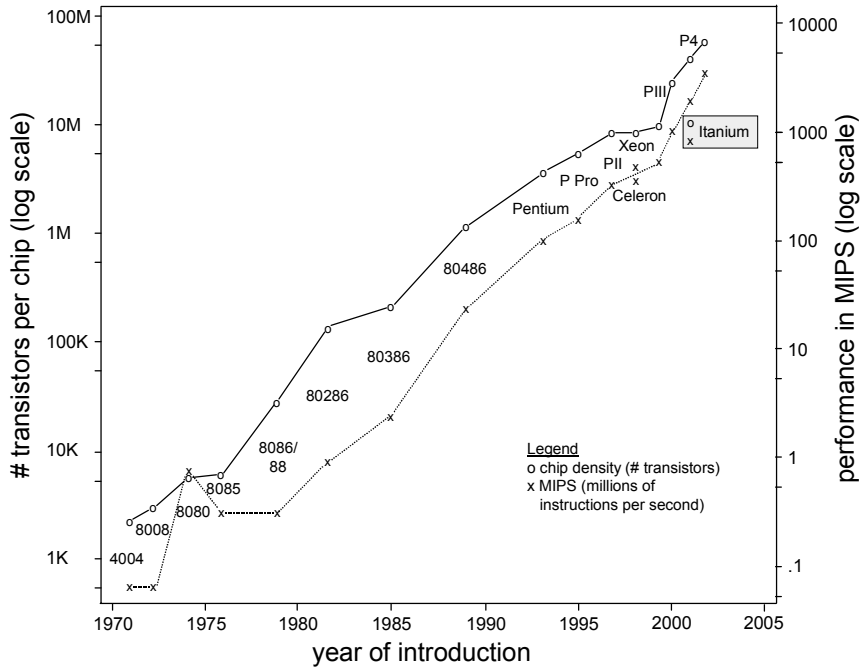

Figure 3-1. Intel Microprocessor Evolution (1971-2002)

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[23] Rose Marie Ham, Greg Linden, and Melissa M. Appleyard, "The Evolving Role of Semiconductor Consortia in the United States and Japan," *California Management Review*, Vol. 41, No. 1, Fall 1998, 139.
[24] Mark LaPedus, "Moore's Law Recast ad Defining Transistor Shrinks, Not Their Scaling," *Electronic Engineering Times*, March 3, 2003, 24.

Source: Intel Microprocessor Quick Reference Guide http://www.intel.com/pressroom/kits/quickreffam.htm and Steve Gilheany, Archive Builders http://www.archivebuilders.com/whitepapers/22016v010h.html

Table 3-1 shows a sample of five microprocessors, separated approximately every eight years apart. Included in the table are key performance measures.

Table 3-1. Key Performance Measures of Selected Intel Microprocessors (by year introduced)

	1971	**1979**	**1985**	**1993**	**2000**
Intel microprocessor	4004	8088	386DX	Pentium	Pentium 4*
Transistor count	2.3 thousand	29 thousand	275 thousand	3.1 million	42 million
Clock speed	108 KHz	5 MHz	16 MHz	60 MHz	1.5 GHz
Instructions per sec.	60 thousand	333 thousand	5-6 million	100 million	1.7 billion
Device feature size	10 microns	3 microns	1.5 microns	0.8 micron	0.18 micron

* note that the current version of the Pentium 4 (February 2004) packs 125 million transistors operating at a clock speed of 3.4 GHz and is fabricated using 0.09 micron (90 nanometer) technology. MIPS estimates are not provided by Intel. Source: http://www.intel.com/pressroom/kits/quickrefyr.htm

The million- and even billion-fold increases in capabilities are hard to imagine at first, as Gordon Moore laments:

> Since I've been in the business the cost of a transistor has gone down some ten million fold. There's no other industry I can identify in the history of mankind where a similar kind of an improvement in cost has been made, particularly over a relatively short period of time.[25]

Note that Intel's company revenues were $9 million in 1971 compared with $26.8 billion in 2002. Effectively microprocessor sales were zero in 1971, while most 2002 sales were derived

[25] Gordon Moore, Extreme Ultraviolet Lithography, Press Conference Call, September 11, 1997, online at http://www.intel.com/pressroom/archive/speeches/euv91197.htm

from microprocessors. Intel's 2002 R&D investment of $4.0 billion or 15% of annual sales was consistent with traditional trends, despite one of the toughest market downturns to date.[26]

The following description contrasts the innovation of Intel microprocessors some two decades apart. It becomes clear that even a complex technology such as a microprocessor has become ever more complex with time. Comparatively, the Intel's first microprocessor, the 4004, could easily be considered a simple technology when judged against the much more complex P6 or Pentium 4 microprocessors. Bob Colwell led the development of both the Pentium Pro and Pentium 4 microprocessors at Intel (discussed in depth in Box 3-2). He contrasts today's state-of-the-art chips with the 4004:

> Well, from my point of view, both the Pentium Pro and Pentium 4 are so far beyond the complexity of the 4004 that it's impossible to even compare them in a useful way. Universities would not even assign the 4004 design as a homework assignment nowadays; it's too simple. I'm exaggerating, but not by much.[27]

Similarly in terms of process, John Kenneth Galbraith's *New Industrial State* (1972) compared the relative simplicity of Model T production engineering to the then-contemporary Ford Mustang.[28] Today's Focus, Ford's "world car," has taken manufacturing and distribution complexity to yet another level. One can only imagine state-of-the-art automobile production thirty years from now. Likewise, the capabilities of microprocessor designed a decade from now stretch our present realm of understanding.

But Colwell, himself an engineer who recognizes that complexity is intrinsically non-quantifiable, reconsiders his assessment:

> But it is nevertheless true that both the 4004 chip and the Pentium 4 chip could be considered complex, and the reasons it's true are themselves interesting and enlightening.[29]

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[26] Intel 2002 Annual Report http://www.intel.com
[27] Bob Colwell, e-mail to the author, June 5, 2002.
[28] Norman Clark, "Some New Approaches to Evolutionary Economics," *Journal of Economic Issues*, Vol. XXII, No. 2, June 1988, 515.
[29] Colwell e-mail.

When reading the following paragraphs, also consider that the IC was commercialized only a decade prior to the introduction of the 4004 microprocessor (in 1961) and contained but 4 transistors, a monumental feat at the time. These devices were essentially hand made as features sizes were measured in millimeters and individual components were distinguishable by the naked eye.

Box 3-2. Increased Complexity in Intel Microprocessor Innovation[30]

To illustrate the point of increased complexity in semiconductor R&D activities over time, contrast the differences between the innovation of Intel's first microprocessor, the 4004 introduced in 1971, and the P6 (Pentium Pro) introduced in 1995. Other factors had also changed markedly over this period, but simply examining the differences in innovation approach, effort, risk, etc. is a very telling example of Rycroft's and Kash's argument for the silent emergence of complexity.

1970 Intel

Innovation in the early days at Intel was concerned with both product architecture and design, and the manufacturing or fabrication process of chips.[31] Gordon Moore, as Director of Research at Fairchild, had been dissatisfied with the linkage between product design and manufacturing at Fairchild. This is one of the chief reasons for his departure to start Intel in 1968. Thus Intel did not establish a separate research organization. Instead, Moore insisted that all process technology research be performed directly on the production line. This approach enabled the company to

[30] Primary sources for this excerpt are Don E. Kash and Robert R. Schaller, "Innovation of the Intel Microprocessor: Revision 1," Working Paper 99:2, School of Public Policy, George Mason University, February 1999, and Robert P. Colwell, "Managing Microprocessor Development at Intel," presentation at PICMET '99, Portland OR, July 29, 1999.

[31] In fact, even today half of Intel's worldwide workforce is involved in manufacturing.

make rapid incremental process changes and to stay ahead of the competition using process technology.[32] Moore reflects on this in the following passage:

> In light of recent experience at Fairchild, it was decided to forestall problems with technology transfer by establishing Intel without a separate R&D laboratory. At some cost of manufacturing and probably to R&D efficiency, development would be conducted in the manufacturing facility... The company continues to follow this course, deeming the time-to-market issues associated with technology transfer to be of paramount importance.[33]

In 1970, semiconductor process (i.e., manufacturing) technology was advanced in comparison with product technology. The design of chips was relatively primitive as available design tools (e.g., computers, software, routines) were limited. Intel was founded on a business

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[32] Robert A. Burgelman, George W. Cogan, and Bruce K. Graham, "Strategic Business Exit and Corporate Transformation: Evolving Links of Technology Strategy and Substantive and Generic Corporate Strategies," Stanford School of Business, Working Paper 1406, September 1996, 42.
[33] Gordon E. Moore, "Some Perspectives on Research in the Semiconductor Industry," in Richard S. Rosenbloom and William J. Spencer, eds., *Engines of Innovation: U.S. Industrial Research at the End of an Era*, Boston: Harvard Business School Press, 1996, 168.
[34] George W. Cogan, "Intel Corporation (A): The DRAM Decision," Stanford University Case BP-256A Rev. 1990, 2.
[35] Gordon E. Moore, "Part 1: The Birth of the Microprocessor," (Interview), *Scientific American*, September 1997.
[36] Fumio Kodama, "The Power of Technology Fusion," Typescript.
[37] Moore, "Part 1: The Birth of the Microprocessor," op. cit..
[38] Ibid.
[39] Carver A. Mead, personal interview, June 15, 1996. Note that Mead and Faggin would later co-found Synaptics (in 1986) to develop technologies to shrink the distance between man and machine such as touchpads, complex pattern recognition, and neural network architecture. See Owen Edwards, "ASAP Legends: Federico Faggin," *Forbes ASAP*, February 26, 1996, 96.
[40] Quoted in Michael S. Malone, *The Microprocessor: A Biography*, New York: Springer-Verlag, 1995, 19.
[41] Robert N. Noyce and Marcian E. Hoff, Jr., "A History of Microprocessor Development at Intel," *IEEE MICRO*, February 1981, 18.
[42] Ibid., 18-19.
[43] Intel made an historic decision in late 1984 to permanently exit the DRAM market, a market they had created.
[44] Interestingly, ZiLOG's Z80 microprocessor was chosen by Tandy Computer Co. for its TRS-80 line of desktop computers introduced in 1977, well before IBM launched its PC. The Z80 used the Intel 8080 instruction set. The Z80 not only outsold the 8080, it is still in production today and is likely the best-selling microprocessor in history. As an aside, Apple Computer had chosen the Motorola M6800 chip, based on a completely different architecture.
[45] Yui Kimura, *The Japanese Semiconductor Industry: Structure, Competitive Strategies, and Performance*, Greenwich, CT: JAI Press Inc., 1988, 63.
[46] Moore, "Part 1: The Birth of the Microprocessor," op. cit..
[47] Colwell was Intel's chief IA-32 architect through the Pentium II, III, and 4 microprocessors. He is now an independent consultant.
[48] The Pentium II is a P6 using a new process technology.
[49] Bob Colwell, "If You Didn't Test It, It Doesn't Work," *IEEE Computer*, Vol. 35, No. 5, May 2002, 11-13, online at http://www.computer.org/computer/homepage/0502/Random/index.htm
[50] Colwell e-mail.

plan to develop complex chips for large volume production. One application that met this requirement with a relatively simple design was computer memories and Intel pursued this technology vigorously. The company had just introduced a new memory chip called dynamic random access memory (DRAM) with its 1K (kilobit) 1103 device. It was hugely successful and by 1972, the 1103 was the largest selling integrated circuit in the world and accounted for 90% of Intel's revenues.[34]

The burgeoning market for electronic calculators was another high-volume, end-use application for chips that had attracted Intel's attention. But the major calculator companies had already secured chip suppliers by that time (including in a few cases a chip maker's downstream entry into the calculator market as in the case of Texas Instruments). In the search process for a calculator company to deal with, Intel came across an unknown firm called Busicom (short for Business Computer). The story of Marcian "Ted" Hoff's elegant 4004 response to the complicated logic design request for the Busicom calculator has been told often and is part of Intel and industry lore. Moore summarizes:

> So we caught up with Busicom, which was a Japanese start-up - a peculiar operation in itself, not very well financed. But they wanted to build a business in scientific calculators, and they were looking for a semiconductor partner. They came in, actually, with all the logic done for their family of calculators, something like 13 chips with considerable complexity.
>
> They had done all the design work on those. We had a small engineering group and most of those people were up to their eyeballs in memory circuits, so we didn't have a lot of engineering to put on something like this. To do 13 different complex circuits was far beyond what we could tackle.
>
> Then one of the guys we had looking at this, Ted Hoff, looked at what they were trying to do and told us that with a general-purpose computer architecture, he thought he could do all of their calculators… His real insight was seeing that this could be done with about the complexity of the MOS memory circuit we were making then… He'd been working with the old DEC PDP-8, which was a relatively hardware-efficient computer, and he knew it very well. So he knew some of the [efficient design] techniques … [a]nd he just recognized that with about the same complexity as the memory chip you could make a simple processing unit.[35]

Thus, the source of innovation of the microprocessor was not planned nor anticipated, but emerged rather serendipitously. Instead of viewing the 4004 as a technological 'breakthrough' or

discontinuity, it might better be described as an outcome of Fumio Kodama's "technology fusion," where existing technologies are combined into a hybrid technology (or design in this particular case).[36]

Hoff's knowledge of minicomputer architecture and Intel's design experience with MOS memory circuitry combined in a way that ultimately produced something fundamentally new and different. But it would take additional time and subsequent incremental innovations to realize this.

Given Intel's situation at the time, total innovation effort for the 4004 was very small. In addition to Hoff there were maybe three others including lead designer Federico Faggin involved in the development. The chief Busicom engineer, Masatoshi Shima, even participated on the project and later joined Intel. Work was completed in nine months. According to Moore, "In those days all chips took about nine months."[37] Due to increased cost pressures in the competitive calculator market, Busicom requested lower prices for Intel's new chips. As is also well known, Intel lowered prices by negotiating in exchange for the rights to sell the chip for other applications. After Busicom's continued financial troubles, Intel returned the $65,000 development funds that Busicom had paid them for complete design rights to the chips for all uses. Again, Moore recalls:

> So the Japanese initially owned all the rights to microprocessors, but sold them for 65 grand. In retrospect, it was kind of like the purchase of Manhattan.[38]

Interestingly, Intel was faced with a similar dilemma: innovative technology with no customer. As interest in microprocessor development waned at Intel, one consequence was that Faggin and Shima soon left to found Zilog to build microprocessors. Most credit Hoff for having the vision of general-purpose microprocessor applications beyond calculators. But according to Carver Mead of CalTech, Faggin and Zilog may have been the true catalysts for subsequent microprocessor development:

> Federico knew right away that this [microprocessor] was a different thing - something irreversible has happened here. And he started acting on that belief system. When I think the real turning point happened is when he left Intel and founded ZiLOG, and there was just enough competitive stuff to push it, because Intel wasn't taking it that seriously -

actually Intel got its act together and started really pursuing it seriously.[39]

Subsequent innovations enhanced the 4004 design including the 8008, an 8-bit version introduced in 1972 that found limited but strategically important application within the electronics hobby community as a building block for what would later be called a *personal* computer. But it was the introduction of the 8080 in 1974 (Faggin had also led the design) that featured a powerful instruction set—enabling users to develop a broader array of software programs—that marked the beginning of a new age in general-purpose computing. As Faggin would later say, "The 8080 really created the microprocessor market. The 4004 and 8008 suggested it, but the 8080 made it real."[40] With this, microprocessors gradually found their way into a wide variety of applications. The biggest of these, of course, was the personal computer (PC).

1980s Intel

The late 1970s witnessed tremendous growth in microprocessor sales, averaging an annual compounded growth rate of 188 percent between 1975 and 1979, according to Noyce and Hoff (1981).[41] In terms of design complexity, by 1980 Intel microprocessor designs had also advanced considerably. One factor, bit-width architecture, had progressed from the 4-bit 4004 to the 32-bit iAPX 432 in less than a decade. In terms of total involvement, the authors compare the two projects:

> The 4004 microprocessor was designed by one man in nine months [Federico Faggin]. Intel's new iAPX432, by contrast, has required 100 man-years of engineering time. To date, Intel has spent over $100 million to design its next generation of processors.[42]

Overall though, the 1980s brought much instability to the semiconductor industry. The Japanese competitive crisis essentially arrested DRAM production from U.S. manufacturers including Intel.[43] At the same time, microprocessor design wars were in full force as Intel, Zilog, Motorola, Mostek, and other producers were vying for key design wins, especially with computer manufacturers. Again, as well known, the biggest design win for Intel was the adoption of the 8086/88 chip by IBM for their PC introduced in 1981.[44] The 8086/88 firmly established the x86

instruction set (derived from the 8080 design) as the *de facto* industry standard and a process of path dependence and increasing returns began to form. This factor along with continued erosion of the DRAM market by Japanese producers would dramatically change Intel's strategic direction. By 1990, Intel had been transformed from a memory company into a microprocessor company (see Figure 3-2).

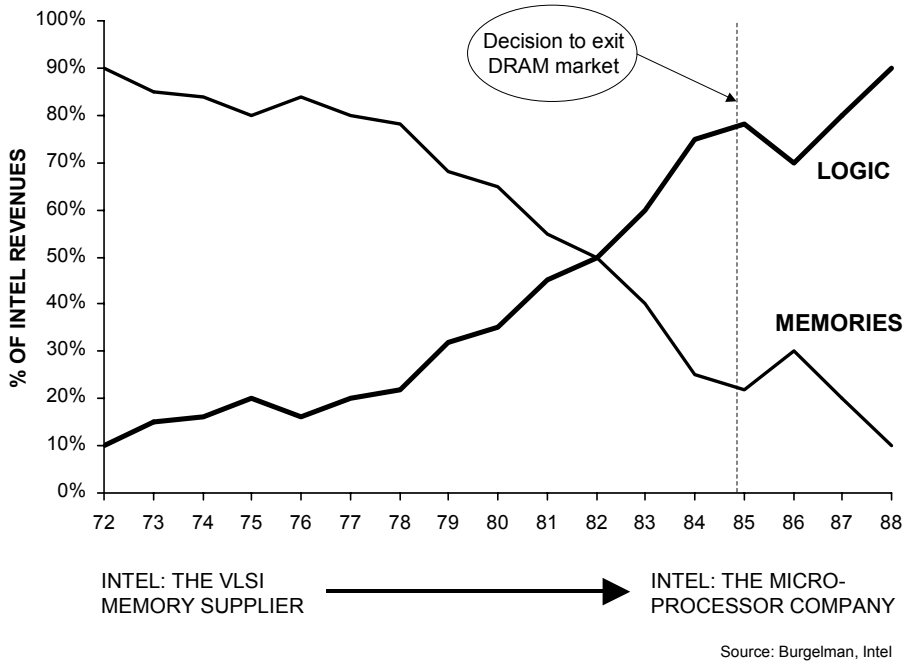

Figure 3-2. Intel: From VLSI Memory Supplier to Microprocessor Company

Design of microprocessors (and other logic devices) is far more complex than memories. Thus, the cost of microprocessor innovation had increased exponentially along with the complexity of design. It has been reported that it cost Intel $1 million to develop a microprocessor in the early 1970s. This figure had grown to more than $100 million by the early 1980s, and continued to escalate.[45]

1990s Intel

As Intel entered the 1990s they had successfully introduced a family of microprocessors that

trace their origin to the 4004 and particularly the 8008. The popular 80486 had just been introduced in 1989 and its successor, the 80586 or P5 (later officially named the Pentium) was well under development for release in 1993. A deliberate and sustained program of product innovation had become critical to the continued success of the firm. In 1997, Moore contrasted the differences in manpower and time commitments between the developments of the 4004 and the Pentium II microprocessors, a span of about 25 years:

> My recollection is that about four engineers worked on the 4004… Now to design one of our chips we have more like 400 engineers, often spread around different sites. And today it takes more like four years. It's a much bigger deal.[46]

Bob Colwell, former Intel Fellow and IA-32 Architecture Director,[47] was the Principal Architect for the P6 (code name for the Pentium Pro), the successor design to the Pentium.[48] He states that the P6 required a total development effort of about 450 people, confirming this estimate. Colwell also led the development of Willamette (code name for the Pentium 4) involving a team size of almost twice this number. Overlapping these efforts, Intel had an estimated 900 people involved in the development of Merced (code name for Itanium), the first 64-bit microprocessor chip in a new IA-64 product architecture co-developed with Hewlett-Packard. Presumably HP also employed a development team of significant size. The steady and significant buildup of development effort over subsequent generations of Intel microprocessors is shown in Table 3-2:

Table 3-2. Estimated Engineering Effort of Selected Intel Microprocessors

Processor	Year Introduced	Estimated team size*
4004	1971	4
80486	1989	80
Pentium	1993	250
P6 (Pentium Pro)	1995	450
Willamette (Pentium 4)	2000	850
Merced (IA-64)	2001	900

* includes validation personnel

Source: Bob Colwell, e-mail to the author, June 5, 2002.

In microprocessor development, architecture leads design. Some sample numbers for project organization include: architecture alone had 50 people for the P6 while Willamette had 80 people. In design, the P6 had 170 people compared with 300 people on Willamette. But the largest single number of people—as much as one-third of total development effort—is in validation (testing). One of the consequences of increased chip density is a corresponding increase in the number of defects or bugs to find and fix. In the beginning of a project, validation is 1 for 1 against RTL (writing code). Total validation effort on the P6 was 300 engineer-years and Willamette was expected to exceed this number by as much as 15 times. Colwell summarizes the overall approach to successful development as "prevent, detect, survive." His philosophy is simple: "If you didn't test it, it doesn't work."[49]

In addition to the immensity of team size, the design complexity required much longer development time than earlier, simpler chips. The P6 would have more than 5 million transistors on board. Development would span some four and one-half years from concept to silicon debug. Merced would require five and one-half years.

There are numerous reasons for the increased complexity in microprocessor development. Colwell offers a few specific reasons in more sophisticated design tools and cumulative experience:

> 1) Design tools. The 4004 was designed with no computer support. Its designers had to keep everything in their heads, from architecture to microarchitecture to circuits to layout. Keeping multiple layers of abstraction of a design in one's head is one of the hardest things there is to do in this field. Seymour Cray was perhaps the most famous of the computer designers who was extremely good at this. He did it because it allowed him to make tradeoffs across unlikely boundaries, thus boosting performance. But the intellectual horsepower required to pull this off taxed even his genius; witness the success of the Cray-1 but the debacles of the Cray-2, -3, and -4.
>
> We could not have designed the Pentium Pro, much less the Pentium 4, without very powerful computers. There are many reasons, among them the fact that maybe Ted Hoff could keep all 2000 transistors in his head at once, but I guarantee you I could not have kept all 43,000,000 transistors of the Pentium 4 in my head at once.
>
> 2) Experience. We learn as we go. When NASA went to the moon, they didn't just build a sequence of huge rockets until one of them worked. They started small, learned what worked and what didn't, kept what did and replaced what didn't, and over time they incrementally got to their goal.

> Well, our industry doesn't have that clear goal, but the method is the same. And it really is true that what was of mind-bending complexity only a few years ago is now commonplace, with grad students expected to have absorbed it during their studies. The history of physics is much like this, too—the ideas come first, and then lots of people try to learn those ideas, and the best ways of representing/understanding them displace the complicated poorly-understood ways that were initially used. (Newton invented calculus, but it's Leibnitz' notation we all use.)[50]

Complexity can also be found in engineering trade-offs, where there are an increasing number of factors. Performance is most important, but validation is almost of equal value (recall the public relations embarrassment Intel suffered following discovery of the rare but unmistakable floating point instruction flaw in the first release of Pentium chips). Other important factors include schedule, die size, and cost; the list goes on. One particular consideration that is unwavering is x86 instruction compatibility. This is absolutely required. In Colwell's words, there is no "close enough" here.

Another aspect of design that is not obvious but an extremely critical success factor is risk management. The sheer size of these innovation efforts is now measured in the billions of dollars, and this does not include the more costly fabrication process to actually build the chips once they are developed. Given the very short product life cycles, multi-billion dollar fabs must be ready simultaneously with new product launches in order to achieve competitive advantage. So in a very real sense these are "bet the company" scale decisions left to design engineers and other technologists on the design team. Engineers push boundaries in their constant quest for better, faster, and cheaper solutions, but they also push risk in the process. Some of this is part of basic engineering, but how much risk is enough? Colwell states, "If you shoot too low, competition kills you. If you shoot too high, you kill yourself." So who judges risk? According to Colwell, the design team must be the judge of risk for reasons of complexity. These design projects involve an extremely subtle synthesis of hundreds of indicators, technical understanding, management directions, capabilities of design staff, state-of-the-art, schedule, tools; again the list goes on. The team—or innovation network as we'll soon see—is the only entity with the knowledge and skill to make these decisions. Thus, management must solicit and abide by the team's judgment.

Colwell summarizes the lessons learned from his P6 and Willamette experiences. One must anticipate and plan for complex issues: "surprises never work in your favor, they almost always make performance go down." You must also propagate a consistent design philosophy that provides structure and guidance over the life of the project. One very interesting, but unsuccessful approach at implementing this philosophy was an attempt to lay out the Intel development facility floor plan in the same design as the chip layout. The idea was to get an optimal floor plan to increase the efficiency of the team, much like a designer attempts to maximize performance with a clever circuit design. Since designers could clearly identify functions and throughputs on the chip, it stood to reason that the people involved in those functions could be co-located with others who they'd have most interaction with. Initially, this action seemed to be working, but over the longer term the logistics of moving people around proved much more difficult than moving functions around on a chip.

Considering future trends affecting microprocessor innovation, exponential trends abound (e.g., Moore's Law) in performance, thermal power (fundamental physics), even team sizes. Colwell asks whether a thousand-person team can truly be nimble. One thing he insists: you can't decentralize teams just like you can't compartmentalize a chip. Lastly, he wonders whether 4-year projects can continue to hit the right targets. He comments that roadmap planning has become very complicated because of many factors and drivers but concludes that roadmap coordination is essential in the midst of increased complexity, now more than ever.

Colwell offers a very interesting account of increasing complexity in microprocessor development projects called "The 101st Benchmark." It is included as Appendix D.

This example underscores the suggestion by Rycroft and Kash of the silent emergence of complexity. Development team sizes have grown gradually from a handful to dozens to hundreds and eventually will top a thousand, mirroring the increased complexity of the technology. Walking into the middle of a development project at any given point along the microprocessor trajectory—if it were possible—would not reveal the same insight as viewing it over time.

Looking ahead, Ashok Sinha's earlier quote, "impossible takes a little longer," seems more believable than at first blush. The demanding technology characteristics forecasted in the latest Roadmap no longer seem as unlikely when viewed in context with past performance. Going forward, the 2003 ITRS projects for node year 2018 that MPU (microprocessor unit) logic chips will contain almost 10 billion transistors with physical gate lengths (feature sizes) of only 7 nanometers (.007 microns). The total cost to build and equip a single fab facility will top $10 billion over this time. Considering this amount is more than 5% of the entire global industry's revenues today, this will be a formidable challenge (as it has always been).

Complexity Science and Sociotechnical Systems

Mitchell Waldrop's 1992 book, *Complexity: The Emerging Science at the Edge of Order and Chaos*, offered valuable insight into the Science of Complexity, a new interdisciplinary study based at the Santa Fe Institute in New Mexico.[51] Referring again to the Holland quote, complexity may be viewed as the ability of autonomous elements to interact in relatively simple ways to produce complex behavior. Under certain conditions, through variation and selection, elements coevolve into systems of increasing structures and complexity. Thus, it is possible that organization, structure, or certain patterns result from simple, small, unpredictable, sometimes irrational (even lucky) events, elements, or pieces that when combined produce a complex *system* well adapted to its environment. Moreover, this process may occur at practically any level in society. As previously stated, examples abound including the evolution of molecules into living cells, cells into increasingly complex organisms and ecosystems, simple economies into complex economies, and simple computers and software into more complex ones.

Complexity theory is contrasted with traditional 'reductionist' theory founded in linear approaches such as Newtonian physics that has dominated scientific thought for the past three centuries. These linear approaches have provided for the requisite predictable order (e.g., laws of nature) to enable

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[51] M. Mitchell Waldrop, *Complexity: The Emerging Science at the Edge of Order and Chaos*, New York: Simon and Schuster, 1992; see also http://www.santafe.edu/ for the homepage of Santa Fe Institute.

empirical, mathematically-based, modern scientific research. Waldrop suggests that this method of research tends to be conducted in a controlled 'laboratory' environment so that outcomes may be isolated, quantified, and 'proven'. Moreover, this basic scientific, reductionist approach has permeated into many disciplines, organizations, and other aspects of society, giving way to optimal methodologies in how we are structured and organized.

Rycroft and Kash assert that existing explanations of technological innovation fall short of the mark and through use of the language and principles of complexity science one may better understand contemporary technological innovation processes:

> The science of complexity offers a useful conceptual framework and vision of technological innovation. Especially, it provides a set of ideas and concepts that are useful in the search for insights into how complex organizational systems carry out the innovation of complex technologies. Certainly in the United States and in western societies generally, there appears to be a powerful inclination to formulate "universal lawlike" rules that purport to provide understanding and guidance... In a complex society general rules won't take one very far towards management success. [52]

There is little question that increasing complexity of semiconductor technology has been a powerful force in the origin and evolution of the Roadmap process. As previously discussed, some have referred to the fabrication of semiconductors as one of the most complex production processes ever performed. More instructive to the Roadmap process, though, is the relationship between process and product technologies and the organizational systems that innovate them. This perspective highlights the idea of *sociotechnical systems*. Sociotechnical systems feature "coupled social and technical parts which humans erect and operate primarily to control our environment and perform tasks we cannot do without such systems."[53] Using this concept it can be seen that there are many types of sociotechnical systems in addition to the network organizations that are the focus of *The Complexity Challenge*. National Innovation Systems (NIS), complexes (i.e., integrated networks such as the U.S. military-industrial complex), individual organizations (i.e., a modern firm or government agency) and cross-functional teams or work

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[52] Ibid., 11.
[53] Ibid., 55-6, see also Stephen J. Kline, *Conceptual Foundations for Multidisciplinary Thinking*, Stanford, CA: Stanford University Press, 1995, 60.

groups are all sociotechnical systems. In their most advanced and complex form, sociotechnical systems may involve thousands of highly trained people, very complicated equipment and facilities, and numerous feedback loops. Edward Wenk has said of these systems that they combine hardware, software, and "socialware" in ways that "the term system is a metaphor for comprehensiveness."[54] Certainly the Roadmap represents a community of collective knowledge organized around the common technological goal of sustaining Moore's Law. Gordon Moore, himself, underscores the sociotechnical nature of semiconductor innovation: "The closer you are to the limits [of the technology], the closer you have to be integrated."[55]

In reference to Complexity Science, *complexity* arises when complex systems approach what's referred to as "the edge of chaos." This is when emergent system-level phenomena generate patterns in time and space that have neither too much nor too little form, and are neither static nor chaotic but are instead interesting due to the coupling of individual and global behaviors.[56] This and other precepts of complexity science are discussed in the sections that follow. A final comment before the discussion and application of complexity science concepts regards the tradition of evolutionary studies and specifically the field of evolutionary economics. *The Complexity Challenge* refers to this growing body of literature as it is complementary to the study of complexity science. Evolutionary economics will be discussed in Chapter 4 as it applies to the idea of technological trajectories.

Emergence and Self-Organization

In the study of complex systems, the idea of emergence is used to indicate the arising of patterns, structures, or properties that do not seem adequately explained by referring only to the system's pre-existing components and their interaction. Emergence becomes of increasing

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[54] Ibid., 56, see also Edward Wenk, Jr., *Making Waves: Engineering, Politics, and the Social Management of Technology*, Chicago: University of Illinois Press, 1995, 11.
[55] Gordon Moore, interview with Ed Korczynski, *Solid State Technology*, July 1997, 359.
[56] Steve Maguire and Bill McKelvey, "Complexity and Management: Moving from Fad to Firm Foundations," *Emergence*, Vol. 1, Iss. 2, 1999, 13.

importance as an explanatory construct when the system is characterized by the following features:

- when the organization of the system (i.e., its global order) appears to be more salient and of a different kind than the components alone;
- when the components can be replaced without an accompanying decommissioning of the whole system;
- when the new global patterns or properties are radically novel with respect to the pre-existing components; thus, the emergent patterns seem to be unpredictable and nondeducible from the components as well as irreducible to those components.[57]

Basically, emergence is an overall systems behavior that comes out of the interaction of many participants. This behavior cannot be predicted, nor envisioned from understanding what each component does in isolation. The research lineage of the study of emergence in self-organizing systems is shown in Figure 3-3.

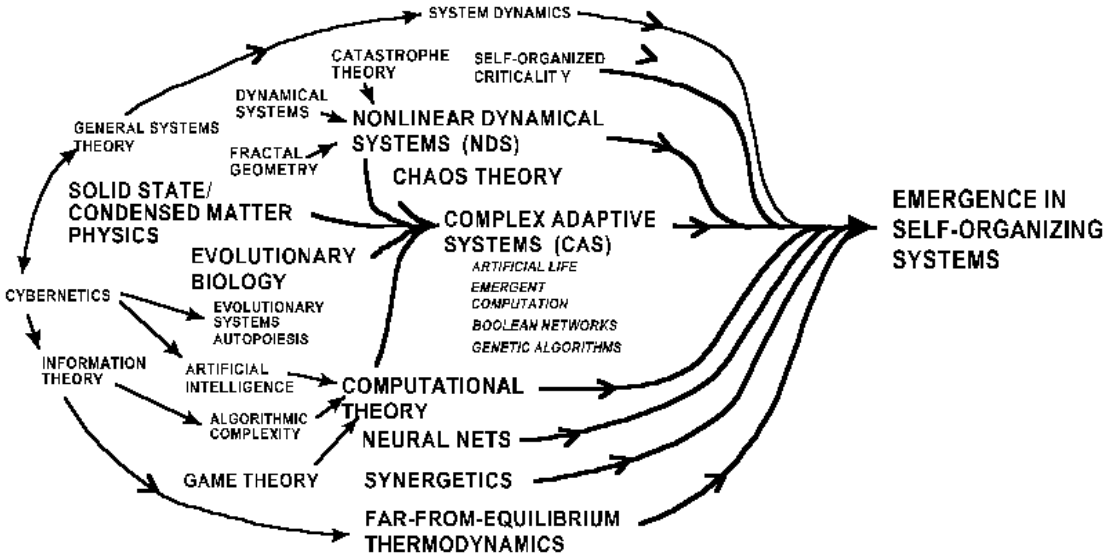

Figure 3-3. Emergence in Self-Organizing Systems

Source: Jeffrey Goldstein, http://www.emergence.org/, adapted from William Bechtel and Robert Richardson, *Discovering Complexity: Decomposition and Localization as Strategies in Scientific Research*, Princeton: Princeton University Press, 1993.

[57] "Emergence as an Explanatory Construct," online at http://www.emergence.org/

Emergent properties are essential to self-organization, which refers to the capability of adaptive systems to reorder themselves into ever more complex structures.[58] John Holland's earlier quote relating to a complex adaptive system (CAS) building models to allow it to anticipate the future captures the idea behind the origin and evolution of the Roadmap. Chapter 9 will detail how elements of the Roadmap formed early in the industry's history but it would take time for important events to unfold before roadmapping practices were employed for broader and more strategic purposes. Similarly, Rycroft and Kash connect the uncertainty that stems from complexity with the increased need for organizational or network learning. They argue that uncertainty becomes an asset, not a liability, in a network structure. When faced with uncertainty, individuals (like single firms) have little recourse other than employing their own knowledge. No matter the individual's skills, knowledge, or abilities, there are discernable limits to learning. But in the case of organizational networks like the semiconductor industry there is an additional factor or natural force that seeks knowledge from all members when confronted with uncertainty:

> In the unpredictable manner of complex systems, the vulnerability conventionally associated with uncertainty frequently becomes a network strength. Faced with uncertainty, the organizational members of networks find the pursuit of fitness requires a reciprocal learning process... Critical to appreciating what takes place in learning organizations is recognition that increasingly individual learning is not enough. Rather, continuous learning must occur across the organization... As complexity increases, the critical knowledge increasingly resides in groups. Maximizing the flow of knowledge and information depends on eliminating fear, fostering a common vision, sense of direction.[59]

Roadmapping not only takes advantage of, but greatly assists in the process of organizational learning. Roadmapping is a form of self-organization reflecting today's need to connect parts of an increasingly complex web of knowledge holders that is central to complex technological innovation. David Teece states that this unique coordinating role fills a void left by the traditional behavior of markets:

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[58] Waldrop, op. cit., 102.
[59] Ibid., 63-4.

> Successful technological innovation requires complex forms of business organization. To be successful innovating organizations must form linkages, upstream and downstream, lateral and horizontal. Advanced technological systems do not and cannot get created in splendid isolation. The communication and coordination requirements are often quite stupendous, and in practice the price system does not suffice to achieve the necessary coordination.[60]

Organizations that are continuously successful in innovating complex technologies are dependent on a capacity for reordering themselves into more complex structures and for using more complex processes. The Roadmap as a network coordinating mechanism that guides a sociotechnical system that is now truly international serves as a vivid example of this self-organizing behavior. A central planning assumption of the Roadmap is Moore's Law (see Chapter 8). In fact, a main aim of the Roadmap is to sustain Moore's Law for the common benefit of the entire semiconductor community. The authors cite the importance of Moore's Law in the semiconductor industry as a powerful benchmark for coordinating learning, but also indicate one potential consequence, path dependence:

> Acceptance of Moore's Law by the network has provided selection criteria for the information and knowledge that has been sought, created, accessed, and used in the innovation process. As such, Moore's Law has helped structure network organizational learning. And the network's success has been dazzling. Yet network members worry that the dominant pattern of learning may keep them from acquiring the knowledge necessary to adapt to a new technological trajectory in the future.[61]

The authors refer to the creation of the Semiconductor Industry Association (SIA) in 1977 and initiatives that followed that helped move U.S. companies toward closer collaboration among themselves and with government (e.g., the Semiconductor Trade Arrangement, the Sematech consortium). These activities gave the industry a forum capable of undertaking intelligence gathering and coordination (e.g., the generation of the Roadmap). Thus, initiatives that improved the capability of, and the opportunities for, participants to interact in mutually beneficial ways led to this industry network becoming more adaptive.

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[60] Ibid., 64-5, see also David J. Teece, "Competition, Cooperation, and Innovation: Organizational Arrangements for Regimes of Rapid Technological Progress," *Journal of Economic Behavior and Organization*, Vol. 18, June 1992, 22.
[61] Ibid., 96.

It is the simultaneous evolution of technology and organization that creates novelty, variety, and performance in products and processes *and networks*. The ultimate success of innovation is as much the 'selection' of organizational characteristics as is technological ones. As a generic concept *coevolution* involves the interaction of a technological community and an evolving technology moving along a path. The technological community is comprised of those individuals, groups, and organizations that share a particular model of problem-solving for a specific technology path. That is, the members of the community share a common, experienced-based, body of heuristics (i.e., how to do things, where to search) and have broad agreement on the key technological and organizational obstacles and opportunities likely to be encountered in the future evolution of the trajectory. The community will have some consensus regarding how to advance the state of the art.[62]

Consistent with the authors' definition, most complex technologies combine components that draw from different knowledge bases. Indeed, the Roadmap represents the collective knowledge of a broad technology network that comprises several technological communities referred to as Technology Working Groups (TWGs). The TWG model has been used by the Roadmap since its inception and dates back to the Sematech workshops and possibly to the SRC's formation (see Chapter 9). The complexity of semiconductor design must consider a multitude of factors (see earlier description of Intel microprocessor innovation) that must ultimately be brought together and reconciled. Stuart Kauffman, a leading complexity science scholar, uses a quilt metaphor to describe an ecosystem model. He describes the role of individual patches while equally stressing the coupling ("knitting" if you will) of these patches into an interactive whole:

> The basic idea of patch procedure is simple: take a hard, conflict-laden task in which many parts interact, and divide it into a quilt of non-overlapping patches. Try to optimize within each patch. As this occurs, the couplings between parts in two patches across patch boundaries will mean that finding a "good" solution in one patch will change the problem to be solved by the parts in adjacent patches. Since changes in each patch will alter the problems confronted by neighboring patches, and the adaptive moves by those

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[62] Ibid., 98.

> patches in turn will alter the problem faced by yet other patches, the system is just like our model of co-evolving ecosystems.[63]

For the 2003 ITRS, these groups are called ITWGs indicating the *international* participation in the specific technology working groups. ITWGs are of two types: *Focus* ITWGS and *Crosscut* ITWGs. The Focus ITWGs correspond to typical sub-activities that sequentially span the Design/Process/Test/Package product flow for integrated circuits. The Crosscut ITWGs represent important supporting activities that tend to individually overlap with the "product flow" at multiple critical points. Table 3-3 shows the 2003 ITRS ITWGs.

Table 3-3. ITRS International Technology Working Groups

Focus ITWGs	Design
	System Drivers
	Test and Test Equipment
	Process Integration, Devices, and Structures (includes RF and Analog/mixed-signal Technologies, and Emerging Research Devices)
	Front End Processes
	Lithography
	Interconnect
	Factory Integration
	Assembly and Packaging
Crosscut ITWGs	Environment, Safety, and Health
	Yield Enhancement
	Metrology
	Modeling and Simulation

Source: 2003 ITRS, 5.

Further description of the Roadmap TWG process and structure is provided in the following excerpt from the 2003 ITRS. It is evident that this arrangement of subdividing the complex task of overall semiconductor innovation into its contributing process technologies enables the large and

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[63] Stuart A. Kauffman, *At Home in the Universe: The Search for Laws of Self-Organization and Complexity*, New York: Oxford University Press, 1995, 252-3; quoted in Michael R. Lissack, "Complexity: the Science, its Vocabulary, and its Relation to Organizations," *Emergence*, Vol. 1, No. 1, 1999, 116.

diverse community of experts to share a particular model or consensus of the future within both their individual working groups and within the broader Roadmap community:

> Each ITWG receives inputs from the regional Technology Working Groups (TWGs). Regional TWGs send one to two representatives to participate on their corresponding ITWG and to attend ITRS meetings. The regional TWGs are composed of experts from industry (chip-makers as well as their equipment and materials suppliers), government research organizations, and universities. In 2003, a total of 936 experts volunteered their support and expertise (an increase from 2001 of 839 participants). The composition of the total TWG membership is analyzed in Figure 1.
>
> It is important to note that per region, particular sectors of the industry are more predominant and the demographics for that region indicate this in the composition by affiliation. For example, there are not many supplier companies in Taiwan, therefore the percentage of participants from suppliers is low. In the United States and Japan, the supplier participation reflects the fact there are more supplier companies in those regions. Likewise, the demographics per ITWG also reflect the affiliations that populate the technology domains. For Emerging Research Devices, a longer-term focus area, the percentage of research participants is 42%, while suppliers is only 8%. In the process technologies of Front End Processes (43%), Lithography (27%), and Interconnect (58%), the percentages of suppliers reflect the equipment/materials suppliers' participation as much higher due to the near-term requirements that must be addressed.[64]

Note that the producing regions referred to are Europe, Japan, Korea, Taiwan, and the United States. Figure 3-4 illustrates the composition of ITWG membership by region and affiliation (i.e., functional representation).

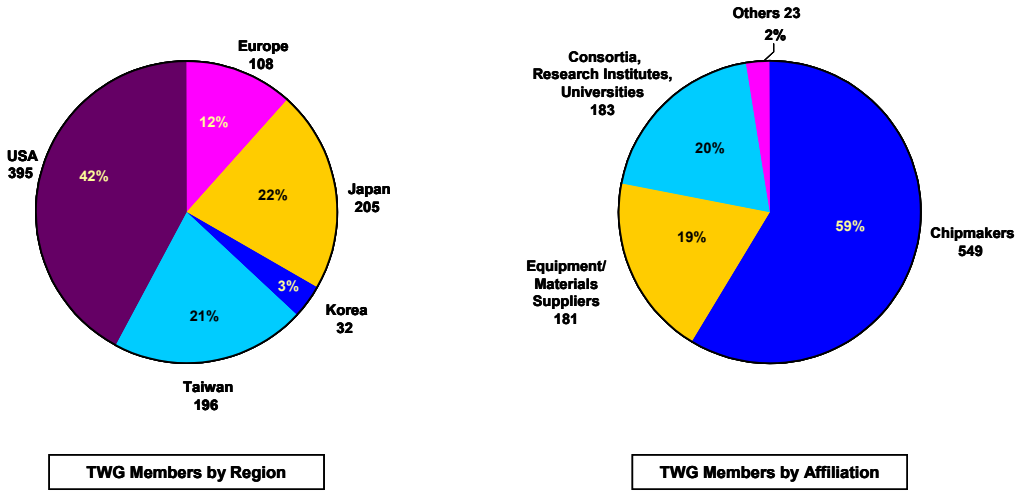

Figure 3-4. Composition of Technology Working Group Members

Source: 2003 ITRS, Figure 1, 6.

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[64] SIA, *The International Roadmap for Semiconductors: 2003 Edition*, 5-6.

Moreover, *The Complexity Challenge* reminds us that networks moving along a trajectory will often self-organize by obtaining new resources (e.g., engaging in new learning activities, acquiring new complementary assets) in order to overcome technological barriers. The formation of technology working groups has been a hallmark of the SIA Roadmap process that officially began in 1992 (see Chapter 10) but is evident in the Sematech strategic planning workshops in 1987/8 (see Chapter 9) and, in fact, is reflected in the organizational structures of both SRC and Sematech research consortia. Semiconductor technology experts have learned that structuring for innovation in this manner has been one of the keys to the continued advance of the state-of-the-art. As the process technologies and innovation communities have coevolved so have the makeup and representation of the working groups. For example, early on the major challenge (some estimates attributed as much as 80%) in advancing the technology through finer and finer feature sizes was through lithography, the key technology that writes the microscopic circuit patterns on chips. So lithography garnered much of the attention of the broader community. With time though what became more important was not the performance of any single technology, but the *coordination* of advances in several related technologies. Karen Brown, NIST Deputy Director, and formerly from IBM Microelectronics including a key assignment at Sematech as Director of Lithography (1994-1998), chaired the National Lithography Committee that preceded the Roadmap Lithography TWG. She describes the creation of the Lithography TWG as the formality of an existing structure:

> The Litho TWG is made up of world experts in lithography and meets four times a year. The group also does regular reviews of litho programs, assessing each potential solution. Two days per quarter are Roadmap related. When the Roadmap was created in the early 1990s, the DARPA budget had a litho line item of $60-70M/yr. So with that level of research commitment by government, there was already a litho structure in place, meeting regularly (quarterly). So when the litho TWG was formed for the first Roadmap it was a lot more convoluted than the rest—some of the other TWGs met around the litho TWG meetings.[65]

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[65] Karen Brown, telephone interview, August 27, 1999.

Brown states that the Lithography TWG was already doing gap analysis and other important activities while some of the other TWGs were grappling with organization, assembling the right mix of participants, etc. The structure of the Lithography TWG provided a model for other groups to look toward. She further describes the real advantage of the Roadmap as a coordinating vehicle for the industry using lithography development as an historical example:

> The semiconductor industry has unique aspects that created a need for the Roadmap. It also made it what it is: you can't make any changes in this industry without integration of disparate companies. For example, i-line to 248nm DUV wavelength requires an exposure tool (6 companies), resist technology (3 companies), and mask technologies (2-3 other industries) to pull off this change. In 1988 IBM worked with exposure [lithography] tool suppliers (Canon, Nikon, SVGL, GCA) and i-line was used longer. IBM was the only photoresist supplier then, but really needed 248nm capability. By 1994/5, 4 or 5 companies were selling 248 resists and IBM was no longer a sole supplier. Thus, the Litho machine tool existed 6yrs before resist capability. By then 248 was capable past .25 microns. Thus, the Roadmap pulls everyone together (resist, mask, exposure tools, calcium fluoride, other materials), integrates timing of supplier availability. Look at IBM and 200mm compared with 5 inch [125mm] tools, 75 different tool families were needed. The Catch 22 is that no one wants to invest until the market is there.[66]

On the other hand the recent transition to 300mm (12 inch diameter) wafer sizes following the 1994 and 1997 NTRS projections proved anything but smooth as new tools were developed ahead of market needs. The supplier community had expended a great amount of resources (estimates range as high as $15 billion) and some came to "blame the Roadmap" for missing the target. This misstep in rhythm or industrial coordination provided a sense of reality that the Roadmap, as thorough as it is, is still a *technology* roadmap and thus limited in considering economic factors such as future market conditions. The positive side of this story is that after a fairly tense and sometimes strained relationship between equipment suppliers and device makers, both groups have worked together in a variety of arrangements to better consider economic factors in future endeavors of such consequence to the industry.

Rycroft and Kash state that self-organization is not a new phenomenon in technological innovation. It is clear that "planned coordination" may be easily substituted for *organized innovation*, so characteristic of the Roadmap process:

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[66] Ibid.

> [W]hen the conceptual "lens" of self-organization is used to view U.S. history from about 1800 to the 1970s, it is evident *there has always been self-organization associated with technological innovation, and in recent years both have been increasing rapidly*... This was especially the case as the benefits of the Japanese pattern of industrial cooperation attracted attention. The evolution from markets to "planned coordination" by cooperating business firms and other organizations ... self-organizing networks are the sources of complex commercial technological innovation around the world.[67]

Extending the discussion of self-organization and network evolution, the authors begin to address network learning using a diagram that shows important linkages within a supply chain. Adapting this concept to the Roadmap process portrays the interplay between Focus ITWGs, each playing a critical part in the overall innovation of semiconductors:

> If one uses an image of a network as a spider's web, the core capabilities would be located in the middle of the web, while the complementary assets would be located in nodes distributed along the web's filaments... Everything represented in Figure 7.1 [3-5] (Core capabilities and complementary assets), then, is subject to change through the process of self-organization.

[67] Ibid., 99, italics in original.

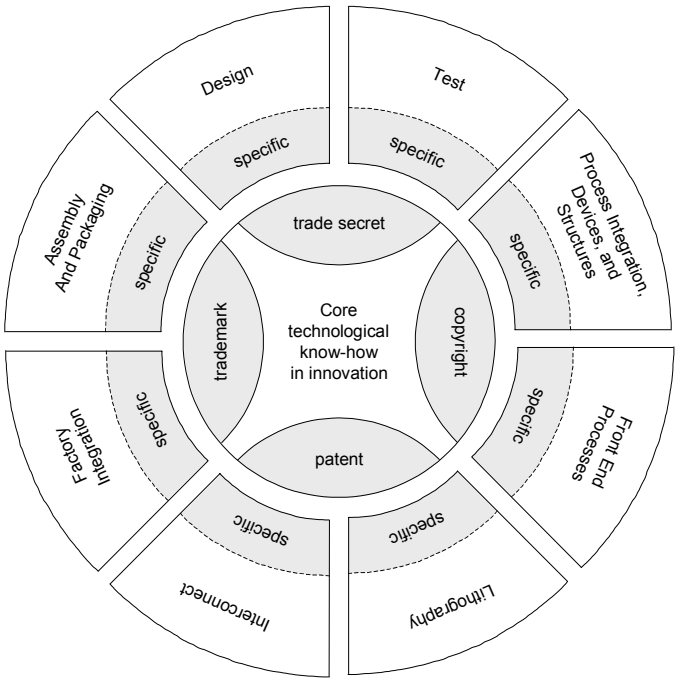

Figure 3-5. Core Capabilities and Complementary Assets

Source: Adapted from Rycroft and Kash, *The Complexity Challenge*, Figure 7.1, 114, taken from David J. Teece, "Strategies for Capturing the Financial Benefits from Technological Innovation," 184 in Nathan Rosenberg, Ralph Landau and David C. Mowery, eds., *Technology and the Wealth of Nations*, Stanford, CA: Stanford University Press, 1992.[68]

It is important to note that the Roadmap structure (i.e., TWG types and makeup, overall scope and purpose) has changed over time (see Chapter 10). Some of these changes are minor, but some have been pivotal (e.g., the transition from U.S. domestic to international roadmap). One of the strengths of the Roadmap process has been its ability to adapt to the changing needs of its users. Another point regarding the adaptation of Figure 3-5 to the Roadmap involves a slightly different interpretation of core capabilities and complementary assets in the context of pre-competitive technologies. The shaded areas of Figure 3-5 would normally represent "less

[68] Ibid., 113-4.

imitatable" or proprietary knowledge, skills, competencies, etc. In theory this type of information is proprietary and thus not shared in the Roadmap process since most participants are from industry and often technologists from rival firms work together on specific Roadmap challenges. While it is very true that proprietary information is closely held by participants, the proportion of total knowledge that is considered pre-competitive (white areas) has grown over time, thus successive Roadmaps have become more complete (increased specificity and granularity of technology requirements). This is the result of two factors. The first is that the semiconductor community has become much more comfortable sharing common knowledge. This process began in earnest with the creation of research consortia, especially with Sematech, and continues today as the limits of technological progress fast approach. So imagine the 'waterline' or dotted line surrounding the shaded areas contracting over time. The second reason is related and accentuates the effect. As the Roadmap has become more widely accepted and used, participation has broadened significantly. As previously mentioned the 2003 ITRS is the product of more than 900 participants located around the globe. Considering that participants in the Micro Tech 2000 Workshop from a decade earlier involved roughly 10% of this number, and those were mostly from the research community, the innovation 'pie' has greatly expanded. The result is that pre-competitive Roadmap knowledge is now a greater share of a growing pool of technological knowledge. This is one key reason that the Roadmap has attained a considerable level of legitimacy within the global semiconductor community.

This development underscores the argument that networks must continually self-organize to stay viable. Rycroft and Kash then apply the concept to strategy, referring specifically to the role of the Roadmap to industry strategy:

> Strategy is composed of a network's objectives and the shared views of its members about how to pursue them. Strategy thus requires deciding what core capabilities to create and maintain over the long term, what complementary assets to access, and what learning processes to undertake ... through the shared vision of the broader technological

> community (e.g., the assumptions underpinning the semiconductor industry's roadmaps) or the common intelligence of the network's participants.[69]

Dynamic organizational routines are embodied in the Roadmap process at both the individual working group (TWG) and overall Roadmap levels:

> At the heart of networks are what Nelson and Winter have called *organizational routines*. It is roughly accurate to say that routines hold key elements of the "core technological know-how in innovation," that Teece has located at the center of Figure 7.1 [2-5]... Faced with solving problems in the process of carrying out innovations, networks learn and incorporate part of what they learn in routines—in "patterns of interactions which represent successful solutions to particular problems and which are resident in group behavior."[70]

Networks and Network Learning

A central focus of *The Complexity Challenge* is the role of organizations—specifically networks of knowledge referred to as network organizational systems—in the innovation process. In fact, the innovation network is the unit of analysis in the authors' research. It is the self-organizing ability of these networks that is a key driving force in innovation. The Roadmap is above all the product of an organizational network of a broad and diverse set of experts representing a dozen key technology areas located throughout the globe. As previously discussed, Roadmap participants hail from the chip-making and materials and equipment industries, research institutes and consortia, universities, government labs and agencies, and other key members of the semiconductor community. Amazingly, the hard work of the Roadmap process carried out by the individual TWGs (or networks) is completely voluntary.

According to Rycroft and Kash, all complex technologies manifest a process of coevolution between the technologies and the organizational networks that produce and use them.[71] They

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[69] Ibid., 114-5.
[70] Ibid., 116-7, see also David J. Teece, Richard Rumelt, Giovanni Dosi, and Sidney Winter, "Understanding Corporate Coherence: Theory and Evidence," *Journal of Economic Behavior and Organization*, Vol. 23, No. 1, January 1994, 15.
[71] Ibid., 5, see also Vincent Mangematin, "The Simultaneous Shaping of Organization and Technology Within Cooperative Agreements," 119-141 in Rod Coombs, Albert Richards, Pier P. Saviotti and Vivien Walsh, eds., *Technological Collaboration: The Dynamics of Cooperation in Industrial Innovation*, Brookfield, VT: Edward Elgar, 1996; Richard R. Nelson, "The Coevolution of Technologies and Institutions," 139-56 in Richard W. England, ed., *Evolutionary Concepts in Contemporary Economics*, Ann Arbor, MI: University of Michigan Press, 1994.

emphasize that technological innovation comes about through adaptations of both technology and the innovation network. The self-organizing nature of these networks is the force that drives innovativeness. The result is that management at every level, from a company to a nation, is increasingly carried out on a day-to-day basis by self-organizing systems that both defy centralized management and have changed the meaning of individual accountability.[72] The Roadmap is the institutional arrangement or network that evolved out of the U.S. industry's competitive crisis in the 1980s, and almost two decades later continues to self-organize to reflect the evolving needs of an increasingly diverse and global semiconductor community.

Network Learning

Peter Senge's 1990 publication, *The Fifth Discipline* brought credence to the then-emerging field of learning organizations.[73] More recently, scholars have paid greater attention to networks as the dominant type of learning organization. In a chapter devoted to network learning, the Rycroft and Kash point out that networks have proven especially capable of know-how learning (e.g., tacit appreciation of how sets of technologies might be made to work together). Networks are not only synergistic learners (i.e., they continuously learn more than the sum of their constituent parts), networks also learn faster than their constituent parts: *the greatest advantage a network can have is the ability to learn quickly.* Much network learning is unplanned and serendipitous, but a critical part results from purposefully "learning how to organize to learn."[74] Further, network learning is a social and collective activity. Although individual expertise is necessary, it is the collaborative nature of learning that distinguishes networks.

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[72] Ibid., see also Robert Jervis, "Complexity and the Analysis of Political and Social Life," *Political Science Quarterly*, Vol. 112, No. 4, Winter 1997-98, 569-93; Paul R. Krugman, *The Self-Organizing Economy*, Cambridge, MA: Blackwell Publishers, 1996; Woody van Olffen and A. Georges L. Romme, "The Role of Hierarchy in Self-Organizing Systems," *Human Systems Management*, Vol. 14, No. 3, 1995, 199-206.
[73] Peter M. Senge, *The Fifth Discipline: The Art & Practice of The Learning Organization*, New York: Doubleday/Currency, 1990.
[74] *The Complexity Challenge*, op. cit., 135, emphasis in original, see also Andreas Pyka, "Informal Networking," *Technovation*, Vol. 17, No. 4, April 1997, 207-10.

These critical points—tacit and quick learning ability, synergy, collectiveness, collaborative nature, and especially the purposeful "organize to learn" aspect—embody important features and benefits of the Roadmap process. Referring back to the TWG process, this is where the real work takes place. Specialists are organized into key technology areas (e.g., assembly & packaging as discussed above) and thus constitute an innovation network for that particular discipline. There are guidelines for TWG membership to ensure balanced participation (i.e., so many device maker reps, so many supplier reps, academic, consortia, etc.), but there are few limitations on participation. In other words, for U.S. regional TWGs at least, most any organization, whether a Sematech, SRC, or SIA member or not, may be a member of the TWG provided the right expertise is supplied. In this way, TWGs are self-organizing networks that have—and will continue to—change their composition as needed. When asked to respond to the statement, "The Semiconductor Technology Roadmap workshops, conferences, and TWG meetings are a good way to communicate technology needs and work key issues." respondents gave priority to the smaller and less-structured TWG meetings over the more formal workshops and conferences. According to respondents, TWG meetings:

- "bring up points on the table, then you can agree on what issues to be worked on, then action."
- "not on their own, TWG sessions are usually a way of initiating things, must follow-up to work issues (e-mail, etc), but social impact important!"
- "are excellent for technology communication. Workshops and conferences are far from ideal."

Changes in Science & Technology Monitoring

The authors note that one of the most striking adaptations in many sectors is the extent to which organizations have moved away from the 'not invented here' syndrome. Monitoring and forecasting science and technology (S&T) usually entails paying attention to more than just explicit knowledge, such as scientific breakthroughs or emerging process and product technologies. It demands a capacity to participate in largely tacit trends, such as the ability to

assimilate research techniques and equipment, and to gain experience with new engineering design or prototyping methods.[75]

Network learning directed toward monitoring the evolving S&T landscape must also be concerned with organizational factors; there is abundant evidence that progress in science has, over time, created an international pool of knowledge that has been a significant source of technological opportunities. A number of studies have documented that, for the most part, scientists and engineers engaged in industrial R&D employ science as a set of tools and stock of knowledge to be tapped in problem-solving. *Used this way, old science may be as useful as more recent developments, and the relation between technological advance and the current scientific frontier may be remote*. The evidence is overwhelming that most applied R&D efforts start with a need or objective and then reach back to science to enable the goal to be achieved.[76]

Increasing complexity demands a much broader reconnaissance using more sophisticated techniques, which may be both costly and time-consuming. The authors point out that some sectors have responded by creating networks whose central tasks are monitoring and trend analysis. The Roadmap is such a network for the global semiconductor community. We are reminded that the Japanese have led the way in advanced monitoring of S&T. Networks comprising firms, industry associations, government agencies, and other organizations have developed a reconnaissance capability that is cited by some observers as a major element in the innovation success of Japanese industries. Central to successful organizational monitoring is the ability to clarify technological trajectories and to realize that the knowledge acquired is fraught with uncertainties. Some observers believe many Japanese networks are successful because they follow a 'learning to learn' approach to monitoring; they are particularly adept at learning from

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[75] Ibid., 141, see also Wendy Faulkner and Jacqueline Senker, *Knowledge Frontiers: Public Sector Research and Industrial Innovation in Biotechnology, Engineering Ceramics, and Parallel Computing*, New York: Oxford University Press, 1995, 218-9.

[76] Ibid., 142-3, emphasis in original, see also Alvin K. Klevorick, Richard C. Levin, Richard R. Nelson, and Sidney G. Winter, "On the Sources and Significance of Interindustry Differences in Technological Opportunities," *Research Policy*, Vol. 24, No. 2, March 1995, 189.

others' earlier mistakes.[77] Despite a decade-long economic downturn in Japan, innovation practices remain strong.

Recall that the Japanese competitive crisis of the 1980s, spurred by their ability to strategically leapfrog the U.S. in the global DRAM race, resulted in many new organizational arrangements. The SRC, Sematech, and the Roadmap, among other measures, were all the direct result of the Japanese crisis and as some have argued, various attempts to mimic a Japanese-style consortia approach to a national challenge. The Japanese are traditionally more akin culturally, politically, and organizationally to a cooperative approach than the fragmented nature of the U.S. semiconductor industry. This belief was confirmed by many informants of this research. The account in Box 3-3 is but one example.

Box 3-3. Industrial Innovation in Japan: One Observation

Turner Hasty, who headed Texas Instruments (TI)'s Semiconductor R&D and later served as COO and acting CEO at Sematech, had spent time in Japan while at TI. He became increasingly concerned as he observed and perceived their ultimate goal as a pretty clear attempt "to get his job." The 1975-1985 era saw continuous improvements to reduce semiconductor device feature size, but the Japanese worked it better than the U.S., according to Hasty. For example, they didn't have divisions between manufacturing and engineering. In other words, there was little evidence of an elitist or *prima dona* attitude characteristic in many U.S. engineering organizations. Later he had to work through similar impediments in the early years at Sematech.

He had witnessed Japan's earlier rapid success in the home entertainment sector of consumer electronics (i.e., TV, VCR, stereo, etc.). The U.S. essentially had 100% of this market in the 1960s, but by a decade later (1970s) Japan dominated the market. Japan's next focus was on computers (especially IBM). They could take it over through capturing the lead in

[77] Ibid., 114, see also B. Bowonder and T. Miyake, "Technology Forecasting in Japan," *Futures*, Vol. 25, No. 7, September 1993, 757-75.

semiconductors first. MITI had published a strategic plan with the goal to dominate computers by 1995. The VLSI consortium was formed in the mid 1970s as the first step. Japan would systematically accomplish semiconductor dominance through a focus on making their equipment suppliers competitive. Traditionally, Japanese passive and active components (vacuum tubes) were always the best quality; they used cheaper but higher-quality components. Applying this experience would give them the advantage in an all-out program on semiconductors.[78]

Regarding the MITI VLSI program, some have argued (Gordon Moore among them) that the Japanese 'figured out' Moore's Law early (by the mid 1970s) and were able to use it to their advantage in DRAM devices especially as the CMOS process technology used was much more stable than other processes at the time. It would take almost a decade later (mid 1980s) before Moore's Law became accepted more generally. In fact, Gordon Moore himself believes that the Japanese' early collective understanding of this allowed them to strategically leapfrog the U.S. semiconductor industry in the ensuing DRAM race of the 1980s.[79]

Sam Harrell, also formerly from TI, is VP at KLA-Tencor and was the first Director of SEMI/Sematech, the supplier industry's research consortium co-located with Sematech.[80] Harrell recalls that in the late 1960s at TI the learning curve was new and device makers were figuring out how to get yields to some target output level. He describes the era as "technology-centric," more accurately "yield-centric." In those days 35% IC yield was in his words, "sensational." Harrell feels that for about two and a half decades the domestic industry remained yield-centric until about the early 1990s. However during the 1980s a new focus emerged: the ability to accelerate the roadmap. (He refers to the roadmap as the normal pace of innovation or Moore's Law.) Up until the late 70s/early 80s a 4yr cycle time existed, but by the early-mid 1980s Toshiba

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[78] Turner Hasty, telephone interviews, May 10 and June 1, 2000.
[79] Ethan R. Mollick, "Foundations of Sand: Moore's Law and the Semiconductor Industry," Senior thesis, Harvard University, March 1997, 45.
[80] The SEMI/Sematech name has since been changed to SISA for *Semiconductor Industry Suppliers Association*.

had permanently changed this to 3yrs and others followed. Echoing the views of Hasty and others, he referenced the VLSI Program—the cooperative effort to develop the 64K and later 256K DRAM—as the means to develop common infrastructure tooling (e.g., Nikon and Canon lithography tools) and in the process improve the overall efficiency and speed of innovation. It was Toshiba first (and then other VLSI firms) to say "we can speed it up," thus "Japan can learn faster than the U.S." The result was a $3B loss in DRAMs for the U.S. including well-known departures such as Intel from the industry.[81]

Methods of Learning

Spillover learning has always pervaded technological innovation, but as networks have moved away from the 'not invented here' syndrome, the rate of spillover learning has accelerated. Often patterns of spillovers are quite unpredictable. Informal channels appear to be especially significant for the transfer of tacit knowledge.[82] Other scholars have found similar behavior:

> They are well practised at focusing such discussion on technical areas of common concern—including the largely tacit knowledge related to research and design instrumentalities—at the same time avoiding disclosure of proprietary information. We would therefore suggest that some types of tacit knowledge are quite extensively shared through informal interaction between competitors.[83]

This caption is another good reflection of the Roadmap process. Even though the focus is on pre-competitive technologies, there still is a great amount of critical knowledge sharing that occurs among Roadmap participants. A Roadmap participant from a small firm sees strategic marketing as a key Roadmap benefit. Increased competitive pressures have squeezed profit margins so the increased risk of making a mistake in product development forces standardization in the form of roadmapping. His firm actively participates and uses the Roadmap to know what's coming so they don't have to guess (wrong). His competitors typically do not participate so his firm can be as much as six months ahead of its competitors in strategic knowledge. Moreover, he

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[81] Sam Harrell, telephone interview, May 11, 2000.
[82] *The Complexity Challenge*, op. cit. 143, see also Andreas Pyka, op. cit., 209-10.
[83] Ibid., see also Faulkner and Senker, op. cit., 206.

recommends to firms that aren't even members or participants to buy the Roadmap updates. His rationale: a customer choice on the Roadmap is a more informed choice than not.[84]

The authors point out that learning by interaction, if successful, triggers further cooperation. One of the distinctive traits of the Roadmap process has been the important role of face-to-face workshops. The ability to meet in person has proven costly and logistically challenging over time as the process has truly become global. Alternative means such as teleconferencing, e-mail, even videoconferencing have been used (see Chapter 11 for a summary of preferences). Further, a collaborative website has facilitated interaction among participants.

From a cultural perspective the authors illustrate the benefits from the network compared with the traditional western approach to cooperative problem solving:

> *Anglo-Saxon contracts are typically limited in the sense that partners are not expected to go beyond the contract. In contrast, in a network perspective, the behavior is prescribed for the unknown, each promising to work in a particular manner to resolve future challenges and difficulties as they arise.*[85]

Note that the Roadmap pre-competitive boundaries help focus the search process to those areas considered common to all participants, but are in practice very pliable as discussed above. There is considerable leeway in obtaining potential knowledge that participants find particularly beneficial to them. The authors continually emphasize learning opportunities as a factor in *constraining and focusing* the self-organization of networks. It is fair to say that the overall purpose of the Roadmap is to constrain and focus collective industry efforts toward sustaining technological innovation. This process can be likened to what many children (boys in particular) learned early on: using a magnifying glass to direct the sun's light on a particular spot—if done long enough—can cause a chemical reaction, namely fire. This metaphor is similar to how the Roadmap focuses the attention of the innovation network toward the chosen 'spots' of research.

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[84] U.S. Assembly & Packaging TWG member, personal interview, June 2, 1999.
[85] Ibid., 146, emphasis in original, quoted from Lorenzoni and Baden-Fuller, "Creating a Strategic Center to Manage a Web of Partners," 154-5.

In this sense, the Roadmap is but one piece of a much larger industrial innovation model that comprises a broad network of organizations, each with distinct knowledge attributes as the authors point out:

> Private firms tend to be better sources of tacit technological know-how, while universities are more capable generators and translators of explicit, codifiable knowledge. The increasing need for a variety of knowledge sources and learning capabilities helps explain why network organizations increasingly include corporate, university, and government components. Moreover, the various learning categories are intertwined. Learning from formalized inquiry, for example, can and is combined with learning by interaction when collaborative R&D projects are undertaken.[86]

Again, the process of network self-organization involves searching for new problem-solving knowledge and procedures, experimenting with and redefining problems, modifying technological trajectories and communities. Paolo Gargini, Intel Fellow and Director of Technology Strategy, has been an active Roadmap participant since 1993. He has co-chaired the Roadmap process since 1997. Many credit Gargini with the Roadmap's success, particularly with regard to its transition to an international roadmap beginning in 1998 and continuing. His vision of the Roadmap as a vehicle for increased international collaboration fits within a new, emerging industrial model that he describes:

> The new model consists of three key elements—like 3 legs of a stool—that support sustained industrial progress: 1) the Roadmap, 2) research consortia (e.g., I300I), and 3) standards. This is closer to real-life, reflecting the structural model used internally within Intel and then taken successfully internationally. Today's semiconductor industry was shaped by the 1980s crisis, similar to how the auto industry reacted after the 1970s. Both needed to become more pro-active to be sustainable. In our case, this is where the three components come in. The semiconductor industry is now very global and is reaching maturity. This transition is much more fundamental than most people realize.[87]

Gargini concludes that organizations must take more responsibilities both in their own plans and in participation in related network activities. The next phase is well underway: research consortia such as International Sematech, Selete, and IMEC conduct highly coordinated research *across international boundaries*. This is increasingly the only way to make the necessary large

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[86] Ibid., see also Walter W. Powell and Peter Brantley, "Competitive Cooperation in Biotechnology: Learning Through Networks?" 370-2 in Nitin Nohria and Robert G. Eccles, eds., *Networks and Organizations: Structure, Form and Action*, Boston: Harvard Business School Press, 1992.
[87] Paolo Gargini, telephone interviews, August 2 and 16, 1999.

investments in advanced technologies since no single company can any longer afford to continue innovation on their own—firms and now consortia must jointly collaborate. Further, the Roadmap serves an important role in setting standards for the industry. The 1997 Roadmap, distributed in early 1998, served as the basis for planning at Sematech, I300I, also SRC to a large degree: it was used as a starting document. In contrast, in late 1995 and early 1996, U.S. industry initiated I300I with the goal of accelerating 300mm development while Japan started Selete for the same purpose. Although both consortia shared the same 300mm wafer objective, they had started with different assumptions and roadmaps. The only way to really determine progress is to have the same assumptions from the beginning, thus the argument for a single, *International* Roadmap that subsequently occurred.

Tacit versus Explicit Knowledge

Referring again to Figure 3-5, much of the "less imitatable" proprietary capabilities in the shaded areas within the dotted lines could be referred to as tacit knowledge (i.e., learned through informal methods, thus difficult to transfer and communicate to others). Sobol and Lei have observed that the tacitness of many dynamic routines makes them an especially powerful source of core capabilities:

> Within organizations, tacit knowledge and skills are often the result of sustained learning and accumulated experience by individuals and teams where the skills become so deeply ingrained or embedded that it becomes difficult for outsiders to imitate or copy them... It is these routines that lay the foundation for building new sources of insights, experiences, and competences.[88]

Tacit knowledge is embedded in behavioral traditions, routines, and heuristics, often as a result of trial and error methods of learning. Thus, tacit knowledge, in whatever form, tends to be path dependent in that it is intertwined with the evolution of particular networks and technological

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[88] Ibid., 117-8, see also Marion G. Sobol and David Lei, "Environment, Manufacturing Technology, and Embedded Knowledge," *International Journal of Human Factors in Manufacturing*, Vol. 4, No. 2, April 1994, 168.

trajectories.[89] In his extensive 1981 study, Sahal examined several technologies that exhibited lawlike patterns of technological innovation. The history of steamboat technology offers one of the most perceptive accounts of the importance of tacit learning, especially as it relates to incremental innovation. This caption makes quite apparent that sustained innovation in semiconductor technology follows much the same course:

> The history of the steamboat is also the history of foundry and machine-shop practice, of metalworking techniques and machine tools, and the practical art of steam engineering. The story is not, for the most part, one enlivened by great feats of creative genius, by startling inventions or revolutionary ideas. Rather, it is one of plodding progress in which the invention in the formal sense counted far less than a multitude of minor improvements, adjustments, and adaptations. The heroes of the piece were not so much men as Watt, Nasmyth, and Maudslay, Fulton, Evans, and Shreve—although the role of such men was important—but the anonymous and unheroic craftsmen, shop foremen, and master mechanics in whose hands rested the daily jobs of making things go and making them go a little better. The story of the evolution of steamboat machinery in the end resolves itself in large part into such seemingly small matters as, for instance, machining a shaft to hundredths instead of sixteenths of an inch, or devising a cylinder packing which would increase the effective pressure a few pounds, or altering the design of a boiler so that cleaning could be accomplished in three hours instead of six and would be necessary only every other instead of every trip. Matters such as these do not often get into the historical record, yet they are the stuff of which mechanical progress is made, and they cannot be ignored simply because we know so little about them.[90]

Explicating or making public technological knowledge that is in large part tacit has been one of the major outcomes of the Roadmap process. Participants in the process are predominantly technologists (i.e., scientists, engineers, technicians) and even management level participants often have extensive technical backgrounds. Thus, they are typically of the engineering mindset to solve problems (Kuhn refers to this as puzzle solving), especially difficult problems. The art of engineering is in some sense about defying the laws of nature or 'engineering around' a perceived limit or previously unsolved problem. Don Wolleson, long-time industry roadmapper and Director of Technology & Reliability Engineering at AMD, underscores the engineers' penchant to "get around" boundaries. He uses the analogy that there are "16,750 guitar pickers in

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[89] Ibid., 118.
[90] Louis C. Hunter, *Steamboats on the Western Rivers, An Economic and Technological History*, Cambridge, Mass.: Harvard University Press, 1949, quoted in Devendra Sahal, *Patterns of Technological Innovation*, Reading, MA: Addison-Wesley, 1981, 161-2.

Nashville," yet musicians still head to Nashville despite the odds. In other words, there's always room to be creative as there are still new things to find or "new ways to play."[91]

Henry Petroski, noted professor of civil engineering at Duke University, has written extensively about engineering and culture for the benefit of a broader, less technical audience. His thorough examinations of simple, daily technological artifacts such as the paper clip or pencil reveal valuable insight into the practice of engineering. Petroski describes engineering as institutionalized invention:

> Engineering is invention institutionalized, and engineers engaged in design are inventors who are daily looking for ways to overcome the limitations of what already works, but not quite as well as can be imagined—or hoped.[92]

The historical regularity of technological advance in semiconductors (see Chapter 8 discussion on Moore's Law) is reflected in a trajectory that embodies both the technology and the network of technologists involved in innovation. Gordon Moore 'explained' Moore's Law—or rather performance against the 1965 Moore plot—back in 1975 as the result of three factors: finer dimensions, increased die size, and design cleverness. The first two of these relate directly to the technology (specifically the process technology involved in fabricating chips) while the last one could be described simply as *engineering* or the ability to advance capability by overcoming difficult design challenges and other limitations.

Limits: Real or Imagined?

One of the characteristics of semiconductor technology—like all other technologies—is that there exist physical limits to its ultimate development. For example, device feature sizes can only be made so small while wafer diameters can only be made so large. Beyond these physical limits the technical properties of the technology break down. What is interesting is that these technological limits have consistently come and gone throughout this industry's history. The very

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[91] Don Wolleson, telephone interviews, August 3 and 10, 1999. Note that Wolleson's industry roadmap experience dates back to the mid 1980s with his involvement at the SRC.
[92] Henry Petroski, *The Evolution of Useful Things*, New York: Vintage Books, 1994.

nature of engineering has something to do with this. When informants were asked about confronting technical challenges while conducting this research, all involved in the Roadmap process would respond with confidence that solutions would be found. Some would reiterate the old engineering 'can do' attitude as if this was just part of everyday practice. Asked what the basis of this 'we'll find a way, we'll figure it out' view shared by so many within the industry, Ralph Cavin, VP of Research Operations at the SRC, stated:

> Well, past successes have something to do with it; we've been able to do it before. When I came to work at the SRC, the 1-micron barrier loomed large of course. And there were those prophets of doom who said, "you will never get past 1 micron, it's against the laws of nature." In fact, we did and we went through it and didn't even notice. Today, 100 nanometers sounds like a formidable barrier. But we will get through it. My view is that the bulk planar CMOS device we've been building for so long will probably change in structure in time. It will still be CMOS technology, still be silicon, but it might not look the same. We'll have to re-engineer it. And I think by doing that we can probably go another order of magnitude in shrink with this technology before we have to invent something else.[93]

What is very interesting in this process is the limits themselves: how they are set, by whom, how they are communicated, and how they are broadly accepted. These questions go well beyond the scope of this research, but it's safe to say that these so-called limits are not as much laws of nature as they are socially-constructed boundaries representing the best available knowledge at the time. As Gordon Moore states, "These limits have a habit of receding as you get close to them."[94] They are constructed by the same community of technologists who will ultimately push these boundaries until they break them, and in so doing set new limits in the process. In evaluating technological life cycles, Rebecca Henderson directly examined performance against so-called limits of optical photolithography and determined that social context factored into the explanation:

> The unexpectedly long age of optical lithography suggests that the belief that the limits of a technology are determined by the internal structure of the technology may be fundamentally misleading. In the case of optical photolithography, the 'natural' or 'physical' limits of the technology were relaxed by unanticipated progress on three fronts: by advances in the performance of component technologies, particularly lenses, by

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[93] Ralph Cavin, personal interview, August 1, 2000.
[94] Gordon Moore, "Extreme Ultraviolet Lithography," Press Conference Call.

> significant changes in the needs and capabilities of users, and by unexpected developments in the performance of complementary technologies... The case of optical lithography thus reinforces the results of those who have suggested that technical structure and social context are simultaneously determined.[95]

More will be said about this in the next chapter's discussion of technological trajectories. Returning to the point, some portion of the ability to overcome so-called limits could be called Moore's "cleverness" or the art of engineering or any other label that captures the creative ability of the human mind. The Roadmap process is really a unique sociological design that's helped make this creativity public in a sense. Cavin continues, underscoring the contribution of the SRC:

> In fact they have learned that by sharing their technical challenges that they all commonly face, there's not much loss to any one of them in doing that. And that by collectively thinking about them, challenges can be overcome. And I believe the SRC has had a big role in that.[96]

It could be argued that Sematech, IMEC, Selete, or any one of a number of related research consortia have had the same kind of positive effect from collaborative efforts. The Roadmap process equally shares this benefit, but is distinct from the others in that it is not a formal organization or structure. Participation is completely voluntary. Although it is sponsored out of necessity, the Roadmap is really beholden to no one in particular. Participation is not restricted to research consortia members. For this reason it enjoys a kind of neutral status that increases its credibility within the semiconductor community.

Through a consensus process of collective inputs, tacit knowledge is shared among participants in technology working group sessions. The author participated in a TWG session during the development of the 1999 ITRS.[97] This TWG process was quite involved. There was considerable time spent updating Roadmap figures and tables as divergent views were discussed and debated. Interestingly, cost emerged as a common criterion that factored into most major discussions. Cost was considered a major factor in determining assignment of colors to future

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[95] Rebecca Henderson, "Of life cycles real and imaginary: The unexpectedly long old age of optical lithography," *Research Policy*, Vol. 24, 1995, 641-2.
[96] Ibid.
[97] Assembly & Packaging U.S. TWG Meeting, University of Texas, JJ Pickle Research Campus, Austin, Texas, June 1, 1999.

challenges (i.e., yellow for solutions being pursued, red for no known solutions, see Chapter 10). The TWG could have easily inserted "affordable" or "reasonable" immediately before solutions. The phrase "whole cost" was suggested by one participant and repeated often by others as a more appropriate way of evaluating a system solution and related tradeoffs. Considering the technical complexity of the assembly and packaging challenges facing the industry, the detailed technical discussion by TWG members—often thrashing back and forth a wide range of technical concerns—ultimately drew out consensus from packaging specialists. The overarching issue was consistently cost (i.e., can it be done at a reasonable cost?). Even when cost was not known, participants pushed for some consensus on proposed solutions to challenges (e.g., in System on a Chip (SoC) applications) with their best guess on cost.

Supporting the Roadmap TWG process, Rycroft and Kash expand on problem-solving search processes by referring to the importance of heuristics that emerge from collective experience:

> Successful search processes rely heavily on *heuristics*, the sets of learned "technological guide posts" (e.g., Where do we go from here? Where should we explore? What sort of knowledge should we draw upon?") that emerge from insight gained from collective experience. A set of heuristics exists somewhere on a continuum between a problem that has only vaguely defined boundaries and a problem that has been fully formulated and defined. Heuristics provide enough structure to focus and guide search activities while still allowing enough flexibility to keep open the consideration of a variety of plausible modifications in these activities.[98]

The Roadmap process has evolved to become a continuous assessment and search for new problem solving knowledge and procedures. As has been stated, a successful network such as the Roadmap practitioner community is characterized by patterns of self-organization that enhance its ability to configure and reconfigure its resources (e.g., capabilities, assets, learning), structures, and strategies in ways that deliver technological innovations.[99]

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[98] *The Complexity Challenge*, op. cit., 122; see also Mario Cimoli and Giovanni Dosi, "Technological Paradigms, Patterns of Learning and Development: An Introductory Roadmap," *Journal of Evolutionary Economics*, Vol. 5, No. 3, 1995, 246; Giovanni Dosi, "Sources, Procedures, and Microeconomic Effects of Innovation," *Journal of Economic Literature*, Vol. 26, No. 3, September 1988, 1127, and Sidney G. Winter, "Knowledge and Competence as Strategic Assets," in David J. Teece, ed., *The Competitive Challenge: Strategies for Industrial Innovation and Renewal*, Cambridge, MA: Ballinger Publishing Co., 1987, 166-9.
[99] *The Complexity Challenge*, op. cit., 122.

Importance of Metaphors

Because much network learning involves tacit knowledge, heuristics often make use of *metaphors*. Metaphorical language is especially useful in expressing visions that provide direction but are not too specific.[100] Management is heavily dependent on metaphors, especially in the U.S. The authors state that metaphors are in many ways the currency of complex systems. By way of metaphors, groups of people can put together what they know, both tacitly and explicitly, in new ways and begin to communicate new knowledge. In the backdrop of an increasingly complex environment, metaphors afford the advantage of referencing something familiar to help better understand something new and unfamiliar. In a broader sense this is why many new path-breaking designs resemble the very design they are meant to replace (e.g., the "horseless" carriage). Familiarity is comforting but more importantly helps ensure success when systems and surrounding environments are undergoing rapid change. Lissack summarizes the role of metaphors as a fundamental tool to today's managers:

> The use of metaphor, in as simple a form as in naming a situated activity, is a generative process. Any given label is also an invitation to see an object as if it were something else; through the resonance of possible connotations, new contextual meaning can be created. Word choice is thus a fundamental tool for the manager, whose role is to shape and create contexts in which appropriate forms of self-organization can occur.[101]

Trajectory is a particularly valuable metaphor in the pursuit of insight into the innovation of complex technologies and the structure and behavior of the networks that coevolve with them. A trajectory refers to a pathway of organizational and technological coevolution. The precise character of technological trajectories can only be outlined in hindsight. Nonetheless, a trajectory is a powerful metaphor.[102] More will be said about technological trajectories in the next chapter. In the same fashion, *roadmap* is closely related to trajectory and serves as a powerful metaphor for strategic technological innovation. "Roadmap" is a simple catch phrase that quickly and naturally captures the concept of planning. As much as anything else, the roadmap label has been a key

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[100] Ibid.
[101] Lissack, "Complexity: the Science, its Vocabulary, and its Relation to Organizations," 121.
[102] Ibid., 28-9.

factor of success in this unique process (see Chapter 2). Tamara Broberg writes about how poets have traditionally interpreted roads, often metaphorically. For example, most are quite familiar with Robert Frost's road "less traveled" passage in his classic poem, *The Road Not Taken*. Broberg emphasizes that roads—particularly in a mobile society—have a special meaning to us. With our cultural tendency to correlate roads with exploration and discovery, the term "roadmap" seems a very fitting innovation metaphor:

> The whole basis of American life has been to "move on" and "discover" … [R]oads will continue to be a major part of our lives and will continue to symbolize the essence of our culture.[103]

The Roadmap has its own set of metaphors. The following two examples in Box 3-4 offer some insight into the extent of usage of analogy and metaphor. Part of this occurs in an attempt to prevent misinterpretation of the Roadmap. More will be said about this in Chapter 11, but suffice it to say for now that the term "roadmap" implies some degree of certainty.

Box 3-4. The Roadmap and Metaphors

Don Wolleson, 1992 and 1994 Roadmap Steering Committee member and active TWG participant, stated: "The term 'roadmap' is not a good metaphor, 'trail blazing' is really what we do."[104] Following the release of the 1994 NTRS, Burger, Glaze, Seidel, and Williams cited Wolleson's route analogy as a way of describing the markedly different terrains faced by the semiconductor innovation community:

> An excellent analogy, developed by Don Wolleson of Advanced Micro Devices, compares meeting the near-term needs to driving along well-mapped, limited-access expressways. These routes require massive engineering efforts, and are able to carry our industry smoothly to the next product generation at 0.25 micron. Few, if any, alternative routes are (or can be) under consideration. The end objectives are well characterized, and the target completion dates are known. Development efforts must stay focused on this costly high-speed expressway.
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> As one moves further out in time to the 0.18-micron generation (about the year

[103] Tamara Broberg, "Poetry of the Open Road," *Public Roads*, Summer 1996, 21.
[104] Don Wolleson, telephone interview, August 10, 1999.

> 2001), the roadmap consists of single-lane paved roads, with more grade-level intersections and traffic lights. Technological progress may be blocked on one development route, forcing a stop to regroup and possibly a shift to a side road. Since this trip is less well-defined, we expect to find alternative routes and dead ends; large investments will be delayed until the correct routes to the end product are found.
>
> Unpaved, unmarked, potholed roads, meandering along the contours of the countryside, characterize the 0.13-micron generation (the year 2004). Even more alternative routes are possible. Though these country roads are replete with barriers, exploration is needed to determine which should be upgraded for future development. For example, we must explore enhancements to optical lithography for 0.13-micron production, as well as other patterning techniques. If no advanced patterning technique can be made to work, we will have to detour and achieve performance advances with some method besides linewidth shrinks.
>
> Near the Roadmap's horizon is the 0.1-micron generation, where the technologist is in wild country with only a multitude of footpaths and few clues for guidance. The number of alternatives has mushroomed, while the resources available for exploration have diminished. Knowledge has to be gained through wide-ranging fundamental research, linked with the performance needs as defined in the Roadmap. Beyond the 0.1-micron product generation, in the 2010 time frame, there are no visible paths and few landmarks; the technology is uncharted. Innovative engineers and scientists are free to follow their knowledge, experimental results, and intuition in whatever directions seem promising, with full knowledge of their end goal: IC performance enhancements. The result may be a proposed device structure with little resemblance to integrated circuits as now known.[105]

More recently, Andrew B. Kahng from the University of California, San Diego and Design TWG Co-chair, addresses the all-too-familiar "red brick wall" challenge facing the industry by using a car analogy. Recognizing the interdependencies of the individual parts to the successful functioning of the system, he stresses a more linked approach as a step toward a 'living' roadmap. Kahng labels this approach as "shared red bricks.".[106]

> In *ITRS* parlance, a red brick is a "technology requirement for which no known solution exists." Solving any given red brick is expensive, and requires large R&D investments. The *ITRS* is now full of red bricks, to the extent that these red bricks seem to form a *red brick wall* in the not too distant future. My contention is that many red bricks stem from trying to continue old ways or old trends without seeking synergy with other parts of the semiconductor supply chain. The following metaphor may help to clarify this point.
>
> Think of the *ITRS*—the semiconductor industry's technology foundations—as a car. The supplier industries (packaging, lithography, design, and so on) are the car's parts. The car must continue along the Moore's Law road; for example, four years from now it

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[105] Robert M. Burger, James A. Glaze, Tom Seidel, and Owen Williams, "The SIA's Roadmap: Consensus for Cooperation, *Solid State Technology*, Vol. 38, Iss. 2, February 1995, 40.
[106] Andrew B. Kahng, telephone interview, February 15, 2002.
[107] Andrew B. Kahng, "The Road Ahead: Shared red bricks," *IEEE Design & Test of Computers*, Mar-Apr 2002, 70-1.

> must reach speeds of 600 mph. It is absurd to think that super tires alone, or super seats alone, will make the car go 600 mph. However, the seat industry might specify its requirements—*and the concomitant levels of R&D investment*—from the perspective that super seats *alone* must enable the 600 mph car.
>
> It is economically wasteful and technologically impossible for each supplier industry to attempt to continue Moore's Law all by itself. We need a more globally optimized allocation of R&D investments—that is, shared red bricks. (By the way, in this metaphor I think of design technology as both steering wheel and tires: Application and market drivers such as microprocessor or RF/mixed-signal drive the car using the steering wheel, and the power generated by the lithography "engine" is transferred to the real-world road via the tires.)[107]

Rycroft and Kash also refer to Nonaka's theory on knowledge creation. Nonaka states that converting tacit to explicit knowledge involves finding a way to express the inexpressible. Again, metaphors serve an important purpose in helping to achieve this metamorphosis because they can communicate experiences that cannot be expressed yet in literal description, such as scientific terminology. In contrast, literal language is inherently reductionist, abstracting and segmenting experience in order to identify elements and their relationships as constituent components of a whole.[108]

The six case studies that informed *The Complexity Challenge* found that participants in networks moving along an existing trajectory shared a rough consensus on what the next incremental innovations were likely to be. The validation of Moore's Law and the Roadmap process certainly support this finding. In fact, these factors enable this network to anticipate the next few innovations (i.e., device generations) with a great deal of confidence. Given that much of this confidence is based upon tacit knowledge, it underscores the importance of psychology. In a discussion following the Assembly & Packaging TWG Meeting, the TWG Chair shared some of the reasons for the Roadmap's success. Similar to Ralph Cavin's perspective, psychology plays a significant role:

> There is a type of optimism or "we'll figure it out" attitude needed for the Roadmap to be successful. You can't look at the Roadmap as a one-way street or dead-end, but a

[108] Ibid., 153, see also Ikujiro Nonaka, "The Knowledge-Creating Company," *Harvard Business Review*, Vol. 69, No. 6, November-December 1991, 96-104.

> means to identify needs that the industry must address through R&D. Look at the red spaces in past Roadmaps and see what happened to them [turning from red to yellow to white]. This is evidence that this attitude prevails. Consider industrial R&D changes: Bell Labs and IBM used to do pure research that the industry didn't have to do but benefited from. This no longer exists, so industry roadmapping helps identify the needs, firms address them and then "go to war" trying to address needs, often crudely, but nonetheless starts a bandwagon effect within the competitive community.[109]

Rycroft and Kash reveal an excellent example of internal-tacit learning referred to as 'black art' knowledge from an observation made during a visit to a turbine blade casting factory:

> After touring a production plant that had advanced robots and precision measuring instruments, one of the authors walked by an employee who had a finished turbine blade in a vice. Attached to the thin, curved edge of the blade was a pair of adjustable pliers that had a piece of metal welded to each jaw. After checking a measuring instrument, the employee tapped the metal welded to the jaws of the pliers with a hammer. When asked what he was doing, the man said: "I'm adjusting the shape. Sometimes the blade comes out of production just a little off. I fix them. You have to be careful; you can't hit them too hard or it changes the granular structure of the alloy, and that will cause the blade to fail." This is learning based on internal-tacit search and discovery.[110]

Similarly, Ham, Linden, and Appleyard found this type of learning in the semiconductor equipment industry. A footnote reads: "An engineer interviewed in this study stated that tool 'tweaks' (i.e., minor changes) constitute some of the most valuable intellectual property in the semiconductor equipment industry."[111] An insightful caption from Lorenz (1962) regarding when a system is placed into operation and "begins to groan and creak" in the next chapter also captures the value of this form of learning.

Finally, the very tacit nature of technological knowledge complicates the transfer of knowledge and demands the mobility of engineers. Rycroft and Kash note that even top-notch specialists have to be willing to bring a screwdriver with them into the North Sea to adjust their designs, so that they will function according to specifications.[112]

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[109] Bob Werner, personal interview, June 2, 1999.
[110] *The Complexity Challenge*, op. cit., 148.
[111] Ham, Linden, and Appleyard, "The Evolving Role of Semiconductor Consortia," footnote 45, 61.
[112] *The Complexity Challenge*, op. cit., 151.

Path Dependence and Increasing Returns

The authors remind us that history matters a great deal in the innovation of complex technologies. The research lessons learned today about how to achieve a certain result are typically built upon previous understanding and this accumulated knowledge influences tomorrow's learning. Hargadon argues strongly that technological breakthroughs happen not through revolutionary, radical, or discontinuous innovations but through incremental change "by building the future from what's already at hand."[113] As Cavin previously stated, this pattern is certainly characteristic of innovation in semiconductors. These tiny devices that perform the countless tasks throughout our daily lives are significantly more capable than the very first devices crafted by Kilby and Noyce almost a half-century ago, however it is fundamentally the same design, only much, much smaller. The ability to make these devices smaller and thus pack more transistors on the same amount of physical space was quickly recognized by early researchers in the field. Gordon Moore was the first to broadly articulate this phenomenon in what has since been dubbed "Moore's Law" (see Chapter 8).

Among other things, this thesis attempts to address why this occurs. Further, why does innovation occur with such regularity? One may ask why doesn't semiconductor innovation occur in a more haphazard fashion, indicative of other industries in similar stages of their life-cycles? One possible explanation is in a concept called *path dependence* as espoused by Brian Arthur and others.[114] Paul David's classic paper on the QWERTY keyboard helps explain why the vast majority of us today use this particular keyboard design.[115] David describes that there have actually been numerous competitive keyboard designs, some of which were arguably superior. Through chance historical events the QWERTY design was broadly adopted and thus "locked-in" as a format standard.

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[113] Andrew Hargadon, *How Breakthroughs Happen: The Surprising Truth About How Companies Innovate*, Boston: Harvard Business School Press, 2003, xii.
[114] See for example W. Brian Arthur, *Increasing Returns and Path Dependency in the Economy*, Ann Arbor, MI: University of Michigan Press, 1994.
[115] QWERTY are the first five alpha characters of the top row (l-r) on the vast majority of keyboards today. See Paul A. David, "Clio and the Economics of QWERTY," *American Economic Review*, May 1985, 332-7.

The implication of path dependence is that a seemingly small advantage or inconsequential lead for some technology, product, or standard can have important and sometimes irreversible influences on the ultimate market allocation of resources. This can occur even in free markets characterized by voluntary decisions and individually maximizing behavior.[116] If path dependence does occur, then it is possible that an inferior or less-optimal alternative may be chosen by forces other than the "invisible hand" of competition. Another oft-cited example that allegedly illustrates the significance of path dependence and lock-in is the eventual choice of VHS over Beta in home videotape-recording formats. More recently, the dominance of Microsoft's Windows over the Apple Macintosh operating system has been referred to as a possible case of path dependence and lock-in. In all three cases, it has been argued that possibly inferior technologies were chosen due to chance historical events. Box 3-5 offers more insight on the PC/Windows vs. Macintosh case.

Box 3-5. Lock-In Example:

How Apple, IBM, and Motorola were "locked out" of Long-run PC Market Rewards[117]

With the benefit of hindsight, the early decisions by Apple and IBM regarding intellectual property of PC systems represent a dazzling set of mistakes. First, Apple's decision to keep its operating system closed and thus deny access to competitors has resulted in its Macintosh computer barely surviving as a niche product in the industry it helped create twenty-five years ago. That is the case even though there is a consensus, at least within the more technical user community, that today's PC running on a Microsoft operating system is still not as capable as an equivalent Macintosh. Even after its recently-released Windows XP PC operating system, many in the network believe that Microsoft's software may not catch up to Macintosh in terms of ease of use and capability for another software release or two. In sum, the Apple decision contributed to

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[116] S.J. Liebowitz and Stephen E. Margolis, "Path Dependence, Lock-In, and History," online at http://wwwpub.utdallas.edu/~liebowit/paths.html

[117] Kash and Schaller, "Innovation of the Intel Microprocessor: Revision 1," op. cit., 15-6.

lock-in on a technically inferior format. The clear beneficiary was the inferior operating system's producer, Microsoft.

The second major mistake was IBM's decision to develop the PC in a manner at variance with its traditional approach. Specifically, IBM went outside to complementary asset suppliers for its microprocessor (i.e., to Intel) and its software (i.e., to Microsoft), in addition to all other system components. This decision appears to reflect both IBM's primary focus on mainframe computers and its belief that the core capability was in the ability to design and assemble the system. From hindsight these decisions reflect adaptation failures by IBM. Not recognizing that the PC represented a new technical trajectory for the computer industry turned out to be a major failure. While IBM was making the decisions that would set the format standard for a new computer trajectory it was failing to position itself to take advantage of the trajectory. Much of the explanation appears to lie in a management decision-making system that did not allow for the kind of rapid adaptation that results from flexible self-organizing networks.

Integral to the flawed IBM decision-making was the misreading of where the long-term core capabilities would be located. As the emergence of Compaq, Dell, Gateway, and literally thousands of smaller firms were to illustrate repeatedly, the ability to assemble and distribute PCs was to quickly take on the characteristics of a commodity activity. The winners were to be those who were first to the market with the lowest-priced PCs. The long-term core capabilities in the PC arena turned out to be what IBM assumed were the complementary assets: the microprocessor and the software.

The triggering event for lock-in of the Intel microprocessor x86 format and the beginning of a pattern of increasing returns occurred with IBM's choice of the network's fourth-generation microprocessor, the 8088 (an 8-bit version of the 16-bit 8086 architecture) for its new PC. The choice of the 8088 over the Motorola 6800 has become a classic in the literature on lock-in. It is especially used to illustrate that the choice of technical trajectories frequently is heavily

influenced by non-technical factors. As was the case with the Macintosh versus Microsoft operating system software, it is widely believed that the 6800 microprocessor was technically superior to the 8088. This choice appears to have been influenced not only by the fact that the 8088 allowed usage of all the software and peripherals designed for the 8080 and the ZiLOG Z80, but also by IBM's preference for the smaller more flexible Intel network which had made on-time delivery of its products a key part of its strategy.

With the market entry of IBM PCs, demand exploded and with it the demand for microprocessors and software. At this point one of the continuing strategic themes of Intel provided major pay-off. It was the early and continuing commitment to assuring that any new microprocessors would serve the existing software base. This is commonly referred to as backward software compatibility. Recall that until the IBM decision the microprocessor network didn't know what operating system it was supposed to support, but, even at that time, it was widely recognized within the industry that the real added-value was in the software, not in the microprocessor. Thus, the network started with the notion that whatever the innovation, it had to be able to support the software that previous microprocessors had supported. Thus, the IBM PC decision and its resultant market success ensured explosive growth for Intel and Microsoft, both of whom subscribed to the precept of backward compatibility.

As enhanced software was written, the market for microprocessors grew exponentially. As the capability of microprocessors increased, the market for software reflected a parallel pattern. A positive sum, increasing returns process had been set in motion. By the early 1980s, the Intel network's innovation focus had expanded from DRAMs and EPROMs to include the microprocessor. Thus the Intel network had become intertwined with Microsoft and the rest of the ever-expanding IBM PC network.

At the same time, the network was becoming ever more intimately linked to complementary asset suppliers of semiconductor-based electronics, increasingly a more significant component of

the PC. Hence, advanced semiconductor materials and process technologies integral to the ongoing miniaturization of chips became part of the network. As aligning and synchronizing innovation of product and process technologies became more important, the integration of the device and process activities into the network became a necessity. Thus the need for a Roadmap to focus the innovation dialogue within the innovation network.

As this example suggests, path dependence means that early technology choices tend to be reinforced by bounding not just the technology, but also the organizations directly involved, and the complex relationships established among them and with others affected by them (e.g., research consortia and even the Roadmap process). Similarly, Hargadon suggests that communities involved in innovative activity from collective sources—semiconductor technology as applied here—draw other actors, objects, and ideas together into tightly knit networks, where people's roles become clear and interdependent, where objects adapt to fit their new applications, and where ideas become shared organizing principles.[118]

There is tremendous power in this, however as organizations, firms, or entire industries build more specialized skills that also become institutionalized, it may narrow the potential strategic opportunities and alternatives that are considered. There is a tendency for highly specialized skills to become more stable, which could make the organization(s) less prepared to respond to environmental challenges. Reference Theodore Levitt's classic "Marketing Myopia" which noted that the once-dominant railroad industry had completely missed the opportunities brought about by technological advances in other modes of transportation.[119] More recently, Clayton Christensen's *Innovator's Dilemma* popularizes the idea that dominant leaders in a technology often lose out in successive innovations because they listen too closely to their current customers

[118] Hargadon, op. cit., 27.
[119] Theodore Levitt, "Marketing Myopia," *Harvard Business Review*, July-August 1960, 45-56.

who are biased toward existing capabilities.[120] On the other hand, path dependence can reinforce an organization's pattern of learning through complex social arrangements. Thus, path dependence has both positive and potentially negative implications for firm and industry performance over time.

The exploration of particular technologies and the development of particular problem-solving methods increase the capabilities of firms and industries in these specific directions and thus increase the incentive to do so in the future. These technology-specific forms of increasing returns tend to lock in the processes of technical change into particular trajectories, entailing mutual reinforcement (positive feedback) between a certain pattern of learning and a pattern of allocation of resources into innovative activities where learning has already occurred in the past.

In cases where a particular technological alternative is *presumed to be dominant* by a sufficient number of actors (e.g., consumers, suppliers, producers of competing designs), this expectation may become self-fulfilling.[121] This appears to be the case with semiconductors as the industry has institutionalized Moore's Law—derived from an initial, simple observation—in the process of developing an industry-wide Roadmap. Industry resource allocations in capital and labor (including research) are made based on Roadmap guideposts. Simply, innovation is guided down the path of Moore's Law. This is obviously a good thing, in fact all are betting on it. But history instructs us that possible breakthroughs in other potentially superior technologies (e.g., carbon-based devices) may be neglected due to lack of allocation of needed resources.

The development of an industry-wide *technology roadmap* with the express goal of sustaining the historical pace of innovation acknowledges and perpetuates the idea of path dependence. To repeat though, path dependence is a double-edged sword: on one side there is great potential in

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[120] Clayton M. Christensen, *The Innovator's Dilemma: When New Technologies Cause Great Firms to Fail*, Boston: Harvard Business School Press, 1997. For a more appropriate treatment since it deals specifically with the semiconductor equipment industry see Rebecca Henderson, "Of life cycles real and imaginary," op. cit., and Rebecca M. Henderson, *The Failure of Established Firms in the Face of Technical Change: A Study of Photolithography Equipment*, Ph.D. Dissertation, Harvard University, 1988.
[121] Ibid., 170.

accumulating and focusing learning along a particular path (or "road"); at the same time this learning can become delimiting as the possibility of "lock-in" may occur. As organizations build more specialized skills that also become institutionalized, this may narrow the potential strategic opportunities and alternatives available. This potential risk is evident in a sampling of comments from informants when asked to describe weaknesses in the Roadmap process (see answers to Question #31 in Appendix B for the complete list of responses). These comments are confined to the narrow focus of the Roadmap as perceived by some participants:

- It can be binding for researchers. The word "roadmap" carries with it implicit belief that you know where you're going and how to get there. In fact, for many of the technologies we have to invent, we don't know. And so I have always felt that it somewhat overstates the state of our knowledge. And faculty sometimes chafe at it because you know 'it's hard to get students interested because, see there's a roadmap, that means you don't have to do anything'.
- It tends to focus our research on a straight line extrapolation and discourage so called disruptive branches as being diversionary.
- Reference Christensen's "Innovator's Dilemma" - the Roadmap is very good at evolutionary, not "disruptive" innovations.
- You might miss something through risk avoidance: if $100 million to spend, where to spend it? On what you know best.
- Leads to short- vs. long-term focus (as opposed to on- vs. off-roadmap choices). For example, litho as a silo: people devoting all this effort to which litho option (out of 4 or 5 alternatives).
- Conventional approach frames the question (e.g., litho): "how to *print* .1 micron features?" begs a litho answer (or Moore's Law answer). But if question is addressed in terms of price/performance parameters, then opens up other possible answers, e.g., quantum computing.
- Historical pitfall or danger is "railroad" effect or narrowing bias - must make sure there is balance in participation (through Delphi). Also make sure roadmap used properly: to define needs and potential solutions, but not the only "route" to take.
- The most serious criticism heard is possibility of squelching innovation, but roadmap process tries very hard to avoid this (curtailing innovation) by leaving open goals as long as possible, but at some point you have to decide on options.

Other related comments include:

- reduced discovery and learning about alternate approaches
- stifles desire to do fundamental research - grants earmarked for on-roadmap research
- can develop a lemming-like mentality
- too predictive

Upon reading these comments (and many others later), consider Wolleson's practical advice that "a roadmap is more than a semi-log plot on a piece of paper."[122]

Moore's Law and Path Dependence

The four-decade run of exponential progress in semiconductors is the envy of every other industry. But there is increasing doubt about how long Moore's Law can go on before this exponential rate reaches, in Gordon Moore's own words, an *asymptote*, or leveling out.[123] Proverbial "roadblocks" in physics and economics loom large along the industry's strategic path. The latest Roadmap states that the so-called "red brick wall" will appear within only a few years as the fundamental limits of the technology are reached. But these doubts are not new—the literature reveals similar skepticism along the way. As previously discussed, each time, though that a formidable obstacle surfaced (e.g., limitations in wavelength of visible light), researchers devised the means to solve these problems to move the technology forward. Perpetual incremental innovation is a hallmark of this industry. Indeed, this is a major factor in the oft-used explanation of Moore's Law as a *self-fulfilling prophecy*.

Perhaps the most striking outcome of Moore's Law is the research implications of the Roadmap. Not that the semiconductor industry is the first nor the last to produce such a document, but clearly this one is unique in its definitive targets of continued, regular exponential performance based on the expectation that Moore's Law will hold for the next decade and a half. By driving hard stakes in the path, researchers and developers throughout the complex network of semiconductor manufacturers, suppliers, and users all share a common view on the prize: smaller—thus faster, better, cheaper ICs. Plans are set, investments are made, resources are allocated, markets bustle in competition, and Moore's Law continues.

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[122] Wolleson interview.
[123] Andrew P. Madden, "The Lawgiver" (interview with Gordon Moore) *The Red Herring Online*, April 1998, online at http://www.herring.com/mag/issue53/lawgiver.html

Thus, innovations in semiconductor technology continue at the pace of Moore's Law. The basic ingredients (e.g., silicon, lithography, clean rooms, even R&D) seem to become more self-reinforcing factors. If anything, an innovation path-dependent Roadmap assures more regularity, possibly at the expense of faster innovation cycles. The result is that, as one research executive has referred, the sheer combined momentum of resources—especially in research—applied to this industry may be the chief driving factor behind Moore's Law.[124] It is safe to say that a 'bandwagon' effect to make things smaller and smaller has taken hold from basic to applied research, to design and manufacturing, to the manufacturing equipment suppliers, to users demanding faster, better, and cheaper end products.

Rebecca Henderson's 1988 Ph.D. thesis was an extensive study of the photolithography industry. Specifically, she examined why established firms in a particular technology (e.g., proximity aligner) failed in the face of technical change to a new technology (e.g., scanning projection aligner).[125] Although not a direct study of path dependence, the author's findings support the view that incumbent firms' previous experience with a technology limits to some extent its ability to successfully introduce new or "generational" innovations, despite having typically invested more in new development projects than new entrants:

> This analysis suggested that established firms have been significantly less able to bring development projects based upon generational innovation to technically successful conclusions... [T]he difference in capabilities between incumbents and entrants was at least partially the result of the communication channels, information filters and problem solving strategies that each firm had developed through its experience with incremental innovation in the previous generation.[126]

Rycroft and Kash cite the work of Bettis and Prahalad in their analysis of institutional impediments to development of the IBM PC, namely unlearning the assumption of the supremacy of mainframes:

> The need to unlearn may suggest why new competitors often displace experienced incumbents in an industry when major structural change occurs (e.g., the personal

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[124] Erich Bloch, personal interview, March 25, 1996.
[125] Hendersen, "The failure of established firms in the face of technical change," op. cit..
[126] Ibid., 245-6.

> computer revolution). The new entrants are starting with a clean sheet of paper and do not have the problem of having to run down an unlearning curve in order to be able to run up a learning curve.[127]

Indeed, the author worked eleven years for Digital Equipment Corporation (DEC) during its heyday (1976-1987) and observed a great deal of organizational learning that enabled the firm to achieve considerable success in a rapidly expanding minicomputer industry (see Box 3-6). However, continued success in minicomputers became an institutional impediment to the learning necessary to recognize and participate in the major structural change underway with the emergence of the personal computer (PC).

Box 3-6. Path Dependence Example:
The Rise and Fall of Digital Equipment Corporation (DEC)

Digital Equipment Corporation (DEC) of Maynard, Massachusetts was founded in 1957 by a bright young engineer and initially made computer modules (digital equipment). By 1960 the new company had produced the PDP-1, the world's first "minicomputer" and within a decade had launched a multibillion dollar minicomputer industry. Digital grew rapidly in the 1970s and early 1980s and ultimately achieved the rank of No. 2 computer manufacturer (behind IBM of course). Digital received wide recognition for its many accomplishments, in both technical and business arenas. Technically, their products were always innovative, high quality (many are still operating today), and often served as industry benchmarks. On the business side, Digital received similar praise. Their stock was the darling of the NYSE well into the 1980s. Finally, Digital was cited as one of a handful of "excellent" companies in Peters and Waterman's hugely popular management treatise, *In Search of Excellence* (New York: Harper & Row, 1982).

While Digital and others were aggressively challenging IBM's lock on the computer mainframe market with smaller, more cost-effective minicomputers, another computer revolution

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[127] *The Complexity Challenge*, op. cit., 146, quoted from Richard A. Bettis and C. K. Prahalad, "The Dominant Logic: Retrospective and Extension," *Strategic Management Journal*, Vol. 16, No. 1, January 1995, 10.

had quietly begun: the *personal* computer. This one was started by Apple Computer in the late 1970s and was legitimized by IBM with the introduction of its "PC" in the early 1980s (see Box 3-5). An almost immediate reaction to IBM's first PC was the development of IBM PC "clones"—later called IBM-compatibles or PC-compatibles. Since IBM did not patent its design—to maintain an open architecture—companies literally obtained a PC, reverse-engineered it (i.e., took it apart to see how it worked) and developed their own systems that would run the same software. To many users it didn't really matter who manufactured the PC since they all performed the same functions. The genius of this decision (however unusual it seemed at the time) was that it helped cement IBM's design as the *de facto* industry standard—not because it was necessarily better (see Box 3-5), but it provided a common platform for everyone to shoot for. One of the first companies to successfully enter the PC-compatible fray was a start-up company in Houston, Texas, that incorporated in early 1982. That company was Compaq Computer who began by concentrating on developing a portable ("compact") computer—the forerunner to today's laptop. Compaq announced the first industry-standard portable computer in 1983 to a very receptive market. They achieved sales of $1 billion five years later (a record). By 2000 Compaq had reached #20 on the Fortune 500 list. (Since then Compaq has been acquired by Hewlett-Packard in a landmark industry merger.)

By 1988 Digital employed 120,000 people around the globe, had annual revenues of $10 billion, and an R&D budget that exceeded Compaq's annual revenues, as impressive as they were at the time. *Fortune* magazine had dubbed Ken Olsen, Digital's founder, CEO and Chairman, "America's Most Successful Entrepreneur," (ahead of Sam Walton, Ross Perot, and others) while a biographical book on Olsen followed shortly after with the title *The Ultimate Entrepreneur*. Unfortunately, this was the beginning of the end for both Olsen and Digital. In 1992

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[128] Adam Gaffin, "Digital: The revolution overtook it," *Network World Fusion*, January 26, 1998, online at http://www.nwfusion.com/news/0126digital2.html
[129] Clayton M. Christensen, op. cit., 109.
[130] Ibid.

Ken Olsen would be forced to resign from the firm and in 1998, after almost a decade of disappointing sales and profits along with unsuccessful restructuring, organizational upheaval, massive layoffs, etc., Digital was acquired by who other than Compaq. The acquisition marked the end of a dark era in Digital's rich history when they seemed desperate to reinvent themselves. Unfortunately it was too late; the PC revolution had passed them by, despite repeated but failed attempts to participate. For all his brilliance and countless contributions, founder Ken Olsen is probably more associated with his now-infamous quote:

> "There is no reason why anyone would want a computer in their home."[128]

As Clayton Christensen points out, just as the emergence of the minicomputer represented a disruptive technology to IBM and its competitors in the 1970s, the PC would have a similar and even more pronounced effect on Digital and its competitors in the 1980s. Despite four attempts between 1983 and 1995 to introduce lines of PCs targeted at consumers, Digital failed to establish a market presence. Similarly, none of the major minicomputer makers became a significant factor in the desktop PC market.[129] Christensen sums up Digital's rise and fall as particularly noteworthy:

> Probably none of these [minicomputer] firms has been so deeply wounded by disruptive technology as Digital Equipment. DEC fell from fortune to folly in just a few years, as stand-alone workstations and networked desktop computers obviated most customers' needs for minicomputers almost overnight.[130]

This story is but one of countless examples of undesirable consequences of path dependency in economic history. Foster's *Attacker's Advantage* and Christensen's *Innovator's Dilemma* enumerate other very good examples. As one reads these accounts the pattern that becomes clear is a kind of 'good news, bad news' story. Path dependency can bless an innovator with economic surplus, while simultaneously sowing the seeds for subsequent economic demise. Pogo's insight is instructive: "We have met the enemy and he is us." In fast-paced industries such as semiconductor manufacturing equipment, magnetic storage, and computers, this likelihood is

particularly acute as shortened product life cycles allow very little time to recover. Common in contemporary management literature is the emphasis on flexibility in the face of uncertainty. It is not surprising that mantras like *Only the Paranoid Survive*[131] have become popular in today's environment. Interestingly, one of the themes of the 1994 Roadmap was "urgency without crisis" as the Japanese competitive crisis—the original impetus for the Roadmap—had subsided:

> The Roadmap also provides a framework for guiding R&D; all relevant segments of the national R&D base can be efficiently enlisted to meet the increasingly complex technology needs of the semiconductor industry. It demands a growing urgency to effectively fund R&D in search of innovative solutions; it is designed to build a culture of "urgency without crisis."[132]

Since path dependency refers to the idiosyncratic patterns of learning and application of competences resulting from the evolution of skills and historical investments and development, the Roadmap is in many ways a formalization of this process. The Roadmap establishes a path for innovation as represented by a 15-year trajectory of increasing capabilities. Moore's early insight of the regularity of empirical performance improvements served an important descriptive function. However, with continued validation, Moore's Law has long since become predictive, thus embodying path dependence. The Roadmap is about sustaining Moore's Law. In other words, ensuring a particular road, route,[133] or path of innovation is taken. Court Skinner of the SRC states its use in guiding research, both private and public:

> The Roadmap is a way of getting the industry to think about what they need to have available if they are going to continue to make progress along the path they are currently on, and thence to guide research funders, in both government and industry, as to where the most useful place to put their money, for whatever their purpose, (e.g., defense or profit).[134]

The Complexity Challenge emphasizes the benefits of network coordination to innovation. Among the many aspects of coordination that produce increasing returns are common standards,

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[131] Andrew S. Grove, *Only The Paranoid Survive: How To Exploit The Crisis Points That Challenge Every Company And Career*, New York: Doubleday, 1996.
[132] Semiconductor Industry Association, *The National Technology Roadmap for Semiconductors*, San Jose, CA, 1994, ix.
[133] According to Rob Phaal, Centre for Technology Management at Cambridge University, the term "Route Map" preceded "Roadmap" in England and possibly in other parts of Europe where it is more commonly referred to by the acronym "TRM" for technology roadmapping.
[134] Court Skinner, e-mail to the author, August 4, 2000.

languages, or infrastructures and the technical compatibility of interconnected systems. In all these instances, the successful performance of any individual technology is contingent on effective linkages with other technological and organizational elements. Traditionally, success of competing 'dominant designs' or technological standards was explained largely in terms of efficiency or some aspect of technological superiority. Organization was typically not an important factor in these assessments. That has changed dramatically, however, with studies of the organizational dynamics that generate coordination benefits from networks. This thesis is an attempt to contribute to this tradition.

Standards and Standards Setting

A technological standard is a set of specifications adhered to either informally or as the result of a formal agreement. Informal, or *de facto*, standards may be created through market dominance by one standard over competing options (e.g., silicon substrate). Formal, or *de jure*, standards are arrived at through agreements reached by voluntary standards-setting organizations or by government regulatory agency mandate.[135] Wafer diameter, feature size, and other scaling parameters are all examples of *de jure* standards.

The benefits of path dependence include increasing returns and positive feedback. Chapter 11 lays out the argument that the Roadmap process has accelerated the pace of innovation. This has endowed the industry with increasing returns, but it also means that the limits to progress—the "red brick wall"—are approaching faster than otherwise. Extending the performance of bulk planar CMOS technology over several decades is a testament to the power of path dependence. Regarding industry strategy and public policy, path dependence means that early technology choices tend to be reinforced. Thus, path dependence bounds not just the technology and organizations directly involved; it also bounds the broader environment of national—now

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[135] Ibid., 166, see also Paul A. David and Shane Greenstein, "The Economics of Compatibility Standards: An Introduction to Recent Research," *Economics of Innovation and New Technologies*, Vol. 1, 1990, 4-5.

international—innovation systems. The role of establishing and maintaining standards becomes increasingly important:

> As technology-based systems become increasingly important and the "windows of opportunity" for making successful investments in the associated markets continues to shrink, *the relevant standards will have to be "managed."* If a standard is fixed, even if it is competitively neutral (an interface standard, for example, rather than a proprietary product element standard), it will eventually act to stifle the introduction of new technology into the system.[136]

To underscore the increased importance of standards the trade association, SEMI (Semiconductor Equipment and Materials International), establishes standards for the collective benefit of the SM&E industry to stay ahead of implementation. The SM&E industry is much more fragmented than the device maker sector that it serves so standards-setting greatly assists in reducing uncertainty. One example of industry-wide standards setting is the transition to 300mm diameter wafers. In response to the 1994 Roadmap, a research consortium called the International 300mm Initiative (I300I), made up of 13 leading device makers from the U.S., Europe, South Korea, and Taiwan was established as Sematech's first subsidiary. Shortly after its formation I300I asked SEMI about standards before implementation. Traditionally, tool development has been haphazard and reactionary. For example, the industry's transition to 300mm wafers would require a different approach than the previous wafer transitions (i.e., 150mm or 6 inch, and 200mm or 8 inch wafers). Ultimately everyone followed but the process was not organized or rational, thus the transition proved very expensive. Ham, Linden, and Appleyard detail the reasons behind this:

> In contrast to previous wafer transitions, the shift from 200mm to 300mm wafers will not be orchestrated by any single firm in the industry, for two reasons. First, experts estimate the costs and technical challenges associated with the shift to 300mm wafers to be in the order of magnitude greater than those of previous wafer transitions… The total development costs of 300mm tools are likely to exceed $10 billion, far higher than the roughly $1 billion cost of developing 200mm tools in the early 1980s. A second and related reason for the lack of single-firm leadership in the 300mm wafer transition is the experiences of Intel and IBM in leading previous wafer transitions. In each of these transitions, the "lead company" (Intel for the 100-150mm transition; IBM led the 150-

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[136] Ibid., 167, see also Gregory Tassey, "The Roles of Standards as Technology Infrastructure," 169, in Hawkins, Mansell, and Skea, eds., *Standards, Innovation and Competitiveness*.

> 200mm transition) purchased or produced test wafers, subsidized equipment development, and guaranteed procurement contracts for production-worthy tools. Representatives of Intel and IBM report that the costs of individually leading these transitions (especially the need to subsidize the development of new equipment whether or not it was eventually purchased) outweighed the benefits of having first access to the new capabilities. Intel took two years longer than expected to reach full volume production in its first 150mm fab, and IBM faced similar problems improving the reliability of its new 200mm tools. Such production delays and unanticipated tool development costs undermined the profitability of being first to manufacture chips on the new wafers.[137]

Ham, Linden, and Appleyard continue:

> Since the costs of "going it alone" with the current wafer transition are so high and no single firm can fully appropriate the returns from that investment, a strategy of sharing some of the costs and risks across a large number of firms has emerged. For the first time in the history of the industry, leading international device makers developed a uniform set of standards in advance of a major wafer transition. In setting these standards, device makers hoped to speed tool development and to reduce the costs of obtaining a compatible 300mm tool set for next-generation fabs. For example… ten different carrier systems were used for 200mm wafers, whereas device makers in the two 300mm consortia have agreed to accept only two carrier systems.[138]

The two consortia referred to in the above passage are I300I initiated by Sematech, and Semiconductor Leading Edge Technologies (Selete) established by ten leading Japanese semiconductor firms. Despite the creation of these two structures, an unexpected economic downturn exacerbated by the Asian currency crisis had set in firmly by 1998 creating 300mm excess capacity. The earlier forecast assumptions based on the 1994 Roadmap turned out to be too aggressive and since this was a *technology* roadmap it had not considered changing market conditions. Ham, Linden, and Appleyard point out that the Roadmap may have served to increase collective risks in this particular case:

> The consequences of the industry downturn on the 300mm transition have been more severe for supplier firms… The chip makers [have] shifted virtually all risks to suppliers… This sudden change in the market outlook for 300mm technologies illustrates an insufficiently appreciated risk of industry-wide collaboration in environments characterized by fundamental uncertainty, which accurately describes

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[137] Ham, Linden, and Appleyard, "The Evolving Role of Semiconductor Consortia," op. cit.., 140.

[138] Ibid., quotes in original, a footnote reads: A variety of standards-setting organizations have been involved in orchestrating dialogue among international device makers and between these manufacturers and their suppliers of semiconductor materials and equipment. Foremost among these are SEMI, an international organization for semiconductor equipment and materials suppliers, and J300, a voluntary industry roundtable in Japan that includes device, equipment, and materials companies. I300I has also taken an active role in standards development.

> most high-technology industries. The formulation of an industry-wide "vision" or technology "roadmap" may increase, rather than reduce, the risks that unforeseen developments will render the best-laid plans irrelevant… Timing is difficult in any rapidly changing environment. But the tendency of such industry-wide collaboration to concentrate technological or economic bets may increase the collective exposure of firms to unexpected developments.[139]

In addition to the industry downturn, another unexpected factor delayed the 300mm conversion efforts. All else equal, a 300mm wafer yields 2.5 times the number of devices as a 200mm wafer, adding capacity and driving unit cost down. But faster-than-expected reductions in the line widths of circuit patterns permitted more, but smaller chips to fit onto each 200mm wafer, extending the productive life of 200mm labs and equipment. Timing acceleration is also attributable to the Roadmap process (see Chapters 10 and 11). In sum, this combination of economic and technical factors delayed the transition to 300mm wafers. Ham, Linden, and Appleyard illustrate the impact:

> As recently as November 1997, chip makers were predicting that seven 300mm pilot lines would be operational in 1998 and that the first high-volume fabs would appear in 2000. As of 1998, however, no 300mm pilot lines are running and high-volume production is not expected until 2002.[140]

As an update, Gartner Dataquest reported that six production fabs are using 300mm wafers in 2002 and there will be eight pilot lines and eleven production fabs using 300mm by the end of the year, but 200mm wafers will still dominate the sales of fab equipment until 2005. Gartner Dataquest reports that over 20 percent of all wafer-fab equipment shipped in 2001 was 300mm.[141]

Whether the Roadmap deserves some degree of 'blame' for the delayed and thus costly transition to 300mm wafers is open to debate. As previously mentioned, the transition to 300mm diameter wafers produced a great deal of discussion between device makers and the supplier communities. Some of these exchanges were heated, but the end result was a much closer

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[139] Ibid., 148.
[140] Ibid., 147.
[141] Kendra Wall, "Bouncing Back," *UpsideToday*, April 23, 2002, http://www.upside.com/

relationship between the two groups along with a revision in the Roadmap process to better accommodate the supplier community.

In summary, the role of standards and standard setting is part of the self-reinforcing regime of path dependency. As such there are both potential positive and negative effects. More will be said about standards later.

Complexity Science and the Roadmap: An Assessment

After discussion and application of many of the concepts, this last section is a general assessment of complexity science as a conceptual framework for this study of the Roadmap process. It is included here in part because the increasing popularity in complexity science over the last decade or so does raise some concerns over its applicability as a 'general theory for everything' or latest management fad that will soon disappear like so many others. The research tradition at the Santa Fe Institute has rightfully earned the due respect of scholars and practitioners alike. This author believes that complexity science has much to offer in the study of this very unique aspect of semiconductor innovation. However, previous concerns over possible misuse have been raised.[142] Thus, it makes sense to pause briefly and consider the advantages and limitations to its use here.

Part of the increased popularity of complexity science (or complexity theory) is attributed to Mitchell Waldrop's 1992 book, *Complexity: The Emerging Science at the Edge of Order and Chaos*. Like Rachel Carson's book, *Silent Spring*, from three decades earlier[143] that reached out beyond the scientific community to awaken the public to the potential dangers of DDT and other pesticides, Waldrop's book found a very broad and receptive audience. Unlike Carson's book, this was not a warning but a generally positive story. Waldrop was able to capture the salient points of a nascent body of new and different research, but as important was his perceptive look at the unique personalities of the few, key people that comprised the discipline at the Santa Fe Institute.

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[142] J. Horgan, “From Complexity to Perplexity,” *Scientific American*, June 1995, 104-9.
[143] Rachel Carson, *Silent Spring*, Boston: Houghton Mifflin, 1962.

Perhaps most importantly, it is a very readable book for practically any audience. Since Waldrop's book—not necessarily because of it—Complexity Science has gained prominence in a wide range of disciplines from health care to banking. A plethora of books now contain the word "complexity" in the title. In May 2002 the author performed a search of book titles at Amazon.com that resulted in a total of 730 matches, of which 193 matches were classified in the Professional & Technical category.[144] In 1999, for its second issue the editors at *Emergence*, a "journal of complexity issues in organizations and management," commissioned a series of book reviews on complexity and management titles. In all, 34 books were reviewed.[145] The majority of these they classified as popular or "trade" books and the reviews are quite insightful. The editors consolidated the reviews (a kind of review of reviews), which is also very informative.[146] Their summary is confined to the trade book category and includes some "Chaos Theory" titles. They refer collectively to complexity science and chaos theory as "New Science."

The *Emergence* editors emphasize at the outset that "The record is clear over the past several decades—management ideas that do not become legitimized by resting on a foundation of quality research are quickly replaced by the next fad coming down the pike."[147] They go on to dispel some of this concern, but still conclude:

> From what the reviews indicate, as well as our own reading of the trade books, New Science is well on its way toward short-lived faddism unless serious research shows there is more than metaphor to chaos theory and complexity science applications and that CEOs using New Science produce more competitively advantaged firms than CEOs who do not.[148]

Relating these findings to an assessment of advantages and limitations in using complexity science as a conceptual framework for this Roadmap case study, one particular aspect has been selected. The empirical example of the Roadmap story attempts to provide context to the broader

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[144] Amazon.com search conducted on May 29, 2002.
[145] Steve Maguire and Bill McKelvey (guest editors), "Special Issue: A Review of Complexity Books," *Emergence*, Vol. 1, Iss. 2, 1999, online at http://www.emergence.org/Emergence/Contents1_2.html
[146] Maguire and McKelvey, "Complexity and Management: Moving from Fad to Firm Foundations," online at http://www.emergence.org/Emergence/Archive/Issue1_2/Issue1_2_1.pdf
[147] Ibid., 5.
[148] Ibid., 43.

evolutionary nature of the semiconductor industry as a complex system. Maguire's and McKelvey's summary of associated book reviewers' findings are instructive:

> *What reviewers applauded*: [T]he empirical examples, case studies and illustrations of concepts that draw on real organizational experiences are almost universally appreciated. Even reviewers who complain of a lack of rigor in the use of complexity concepts congratulate authors for attempting to apply them and for recounting these case histories … bringing structure and order to the chaotic world that they describe. Indeed, just attempting to order the business world within complexity-inspired frameworks is appreciated, as it stimulates thinking and forces readers to reflect on and perhaps struggle with their own ideas. Authors' use of metaphors is singled out as particularly insightful.[149]
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> *What reviewers would like improved*: [S]ome complaints do reappear, especially that of authors' "loose," "less than rigorous," "oversimplified," and even sometimes "incorrect" use of concepts. And while metaphors are applauded, a number of reviewers feel that authors' over-reliance on metaphors contributes to these "superficial" treatments… [T]he full toolkit of complexity has not been put on display for practitioners. Finally, although empirical examples are much appreciated, a number of reviewers feel that these are mere retellings of old tales using complexity terminology tacked on retrospectively, gratuitously and, in many cases, quite awkwardly.[150]

To conclude, all attempts have been made in the course of this research to ensure comprehensiveness and validity. This study follows the tradition of Richard Nelson's "appreciative stories" (i.e., told by those who appreciate the details).[151] If this case is done properly, it should provide an added richness to our understanding of this unique case of technological innovation. On the other hand, if concepts of complexity science are misapplied, we are no better for the exercise.

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[149] Ibid., 8.
[150] Ibid., 9.
[151] Richard R. Nelson, "Recent Evolutionary Theorizing About Economic Change," *Journal of Economic Literature*, Vol. 33, No. 1, March 1995, 85-6.

CHAPTER 4: Emerging Pattern of Organized Innovation

"A hen is only an egg's way of making another egg."

- Samuel Butler[1]

"The linear model is not the way this industry developed. It's not science becomes technology becomes products. It's technology that gets the science to come along behind it."

- Gordon Moore[2]

"[S]emiconductor manufacturing companies have become especially skillful at pinpointing subjects that need to be researched, determining what is and what is not "precompetitive" and then closely working together to develop a solution to common problems."

- Peter Singer[3]

Chapter 3 set up the conceptual framework for this study using major concepts, themes, and language from *Complexity Science*. The purpose of Chapter 4 is partly to continue this line of analysis, more closely examining *Evolutionary Theory* as it pertains to studying particular and appropriate patterns of innovations. The process of innovation will also be examined within an evolutionary framework. Finally, the ideas developed in these two chapters are then considered in advancing a theory of industrial innovation in semiconductors involving the Roadmap which will be referred to as "Organized Innovation."

Studying the Roadmap affords many new and unique insights into the industrial innovation process. The Roadmap is analyzed here in terms of its role in the development of industry

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[1] Samuel Butler, 1885, quoted in Michael Rothschild, *Bionomics: Economy as Ecosystem*, New York: Henry Holt and Company, 1990, 1.
[2] Gordon Moore, in interview by Lillian Hoddeson and Michael Riordan, 11 January 1996, in Michael Riordan and Lillian Hoddeson, *Crystal Fire: The Birth of the Information Age*, New York: W.W. Norton & Co., 1997, 282.
[3] Peter Singer, "International Cooperation Helps Reduce Risks and Costs of R&D," *Semiconductor International*, March 1, 1998.

strategies and public policies. Upon closer examination the Roadmap process offers deeper understanding of other processes affecting technological innovation of semiconductors. Having discussed the increasing complexity of the semiconductor innovation enterprise in the previous chapter, this chapter turns to how the semiconductor community has collectively dealt with this situation through efforts that effectively organize innovation activities with the help of a coordination mechanism such as the Roadmap. Concepts such as technological paradigms, trajectories, regimes, guideposts, among others embody this view of structured or organized technological change.

The chapter begins with a review of the evolutionary literature as it pertains to innovation and technical change. This is followed by a discussion of the process of technological innovation. Finally, a theory of organized innovation is proposed.

Evolutionary Theories of Technological Change

The *Complexity Challenge* refers heavily to the field of evolutionary economics, of which many of the concepts complement complexity science. Before delving into the economic interpretation of evolutionary theory, a broader review of the field will be attempted. Like Complexity Science, Evolution Theory casts a broad net across the literature. Since the interest here is technological change and innovation, this review will be limited to but a few key pertinent sources. Nieto (2002) summarizes the evolutionary idea in this particular context:

> The theory of biological evolution employs three key concepts to explain the dynamics of evolution: diversity, selection, and inherited characteristics. The diversity of organic species has its origin in the processes of genetic mutation (equated to the processes of creation of new technological knowledge). The success of each of the genetic varieties or species (parallel to technological knowledge) is determined by its degree of adaptation to the environment (the industry), which acts as a selection mechanism. Genetic varieties spread through inherited features (equivalent to the diffusion and accumulation of new knowledge). This scheme can serve as a framework of reference adequate for setting up analogies allowing study of technological evolution.[4]

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[4] Mariano Nieto, "From R&D management to knowledge management: An overview of studies of innovation management," *Technological Forecasting & Social Change* 70, 2002, 9 (*uncorrected proof)*.

A recent compilation of essays on this topic, edited by John Ziman (2000), is entitled *Technological Innovation as an Evolutionary Process*.[5] This book is dedicated to the late psychologist Donald T. Campbell, whose research and publications in the 1960s and 1970s were instrumental in developing the field of *Evolutionary Epistemology*, which argues that the growth of knowledge can best be understood as occurring through a process akin to a Darwinian process of natural selection. Hence, the very process of evolution is viewed as the evolution of knowledge.[6] This view interprets the whole story of human social, intellectual and material development as the continuation of organic evolution by other (non-biological) means.[7] In other words, it is an attempt at studying *cultural* change including technological innovation, a social process, using the tools and concepts of biological evolution.

Campbell employed the VSR (Variation, Selection, and Retention) formulation as briefly described above by Nieto. The idea of retention (i.e., inherited characteristics) holds the fundamental evolutionary building block: the *genotype* or simply *gene*. In biology, the gene is the elemental unit that encodes and replicates an organism's vital information. Genes are the carriers of life's unique identity in all things living. In evolutionary theory, the term 'meme' is used to correspond to the biological term, *gene*. In an essay on evolutionary phenomena in technological change, Mokyr draws the parallel:

> In biology, the underlying structure is the genotype, while the manifested entity is the phenotype. In evolutionary epistemology the underlying structure is the knowledge base whose elements determine the traits of cultural entities such as words, artistic forms, ideas, customs, and the like. These elements thus correspond closely to what Dawkins termed 'memes'.[8]

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[5] John Ziman (ed.), *Technological Innovation as an Evolutionary Process*, Cambridge, UK: Cambridge University Press, 2000.
[6] Jon D. Wisman, "Economic Knowledge, Evolutionary Epistemology, and Human Interests," *Journal of Economic Issues*, Vol. XXIII, No. 2, June 1989, 648.
[7] Ziman (ed.), op. cit., 3-4.
[8] Ibid., 52-3, see R. Dawkins, *The Selfish Gene*, Oxford: Oxford University Press, 1976, for the origin of 'memes'.

In this respect "memes" are the elementary concepts that endure over long periods, replicate themselves and shape the actual artifacts.[9] The artifact is in fact the corollary to a biological phenotype, the "manifested entity" or actual organism subject to environmental selection. In this case technical artifacts like a tool, manufacturing process, or semiconductor device are subjected to "fitness" criteria established by such forces as the market. The process of natural selection brings about changes in artifacts which, in turn, influence memes. Thus, artifacts are temporal whereas memes are not. Dosi and Nelson (1993) further clarify the differences between biological genotype and phenotype:

> [Evolutionary] theory is concerned with two actual populations as contrasted with potential ones. One is the population of genotypes, defined as the genetic inheritance of living creatures. The second is the population of phenotypes, defined in terms of a set of variables that happen to be of interest to the analyst, but which include those that influence the "fitness" of each living creature. These might include physical aspects like size, or sight, behavioral patterns like song, responses to particular contingencies like something that can be eaten and is within reach, or a potential mate, or a member of one's own "group" selecting help.
>
> Phenotypic characteristics are presumed to be influenced by genotypic ones, but not uniquely determined by them. Modern evolutionary theory recognizes that the development of a living creature from its origins to its phenotypic characteristics at any time can be influenced by the environment it passes through. Modern evolutionary theory also recognizes a variety of learning experiences which shape the behavior of a phenotype… However … the hallmark of standard biological evolutionary theory is that only the genes, not any acquired characteristics of behavior [phenotypes], get passed on across the generations.
>
> The notion of "generations" is basic to biological evolutionary theory. The phenotypes get born, live, reproduce (at least some of them do), and die (all of them do). On the other hand, the genes get carried over to their offspring, who follow the same generational lifecycle. Thus, the genes provide the continuity of the evolutionary system, with the actual living creatures acting, from one point of view, as their transporters from generation to generation…
>
> In the generally held interpretation of this theory … selection operates directly on the phenotypes. It is they, not their genes per se, that are more or less fit. To repeat what was stressed above, phenotypes are not uniquely determined by genotypes. However, the theory assumes a strong enough relationship between genotypes and phenotypes so that systematic selection on phenotypes results in systematic selection on genotypes.[10]

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[9] Ibid., 5.
[10] Giovanni Dosi and Richard R. Nelson, "Evolutionary Theories in Economics: Assessment and Prospects," Typescript, June 1993, 10-11, quotes in original.

Thus, genotypes (memes) or rather, the genetic code, are passed on to subsequent generations, while phenotypes (artifacts) represent the temporal characteristics of the species at any given point in time. In technological change, the notion of semiconductor device "generations" fits this description well with DRAMs probably the best historical example of this. The long trail of DRAM artifacts starting with the first 1Kbit (one thousand bit) DRAM in 1970 and continuing relentlessly *million*-fold to a 1Gbit (one billion bit) chip thirty years later is undeniable evidence that a generational description is quite appropriate. In an interesting application of evolutionary theory to technological change, Victor and Ausubel (2002) liken the DRAM to a fruit fly in that both exhibit very short life-cycle properties:

> Biologists overcome problems of studying evolution by working with fruit flies and other short-lived animals and plants. The fruit fly *Drosophila melanogaster* is born, matures, and dies in a few weeks. In front of an individual biologist's eyes, fruit flies are tested by the environment and the fit ones reproduce, passing on their tested inheritance through many cycles.
>
> A student of the evolution of technologies, in contrast, generally lacks documented subjects that present several cycles. During a lifetime, a technology researcher will see few cycles of technology from birth through testing to birth of successors... Industries such as autos, pharmaceuticals, and electric power measure the time of many of their products and processes in decades.
>
> Happily, the semiconductor industry has given birth to a fruit fly, a model organism for study of technological evolution. Dynamic random access memory (DRAM) chips cycle quickly from birth through testing by the market to new invention. A generation of, say, 128M DRAM dominates the market for only a few years. Because generations persist only briefly, their well-documented history now extends over eight generations, making precise tests of classic hypotheses of technological evolution possible.[11]

The authors present a series of graphs to support their argument.[12] Figure 4-1 presents one of the charts and clearly demonstrates the life-cycles of each of eight DRAM generations from the 4K device introduced in 1974 to the then-current 64M device introduced in 1994.

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[11] Nadejda M. Victor, Jesse H. Ausubel, "DRAMs as model organisms for study of technological evolution," *Technological Forecasting & Social Change*, 69, 2002, 243-4.
[12] Data used in the Victor and Ausubel (2002) paper are posted at http://phe.rockefeller.edu/LogletLab/DRAM

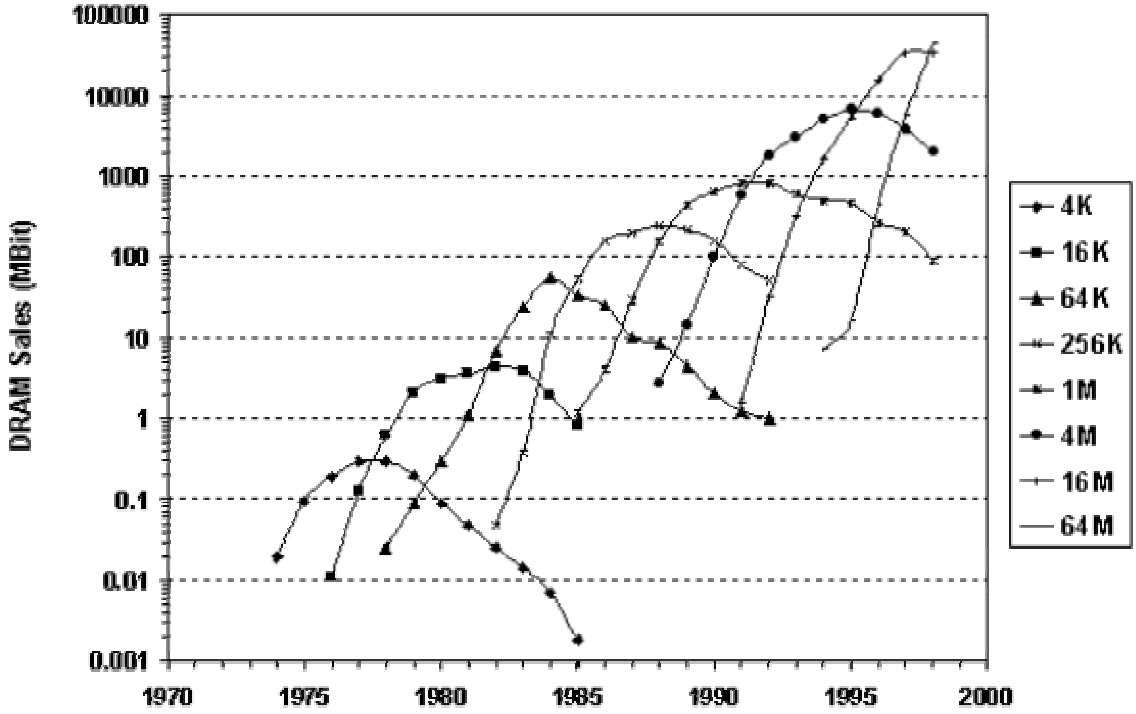

Figure 4-1. DRAM Sales in Megabits by IC Density

Source: Figure 4 of Nadejda M. Victor, Jesse H. Ausubel, "DRAMs as model organisms for study of technological evolution," *Technological Forecasting & Social Change*, 69, 2002, 249.

But what exactly are the *memes* within the successive generations of DRAMs and other semiconductor technologies? What gets transmitted to the 'offspring' that sustains the 'species'? Very simply, what evolves? Mokyr earlier called memes the 'knowledge base' where knowledge is encoded not genetically but in theories, practices, and similar forms. Indeed, technological knowledge embedded in the design and manufacturing of today's chip is greatly a product of history that could be traced back in part to the first DRAM. However, knowledge is a cognitive term, the result of learning. Learning also produces affective and behavioral traits.

One of many contributions of Nelson and Winter's (1982) seminal work, *An Evolutionary Theory of Economic Change* was the idea of "organizational genetics." The authors would more

precisely refer to "routine" as the 'regular and predictable behavior patterns' that play the role of genes in evolutionary theory. Although not fully transferable concepts, habits and routines do have a sufficient degree of durability to be regarded as having quasi-generic qualities:[13]

> We have already referred to one borrowed [from biology] idea that is central in our scheme—the idea of economic "natural selection."… Supporting our analytical emphasis on this sort of evolution by natural selection is a view of "organizational genetics"—the processes by which traits of organizations, including those traits underlying the ability to produce output and make profits, are transmitted through time.[14]
>
> Our general term for all regular and predictable behavior patterns of firms is "routine." We use this term to include characteristics of firms that range from well-specified technical routines for producing things, through procedures for hiring and firing, ordering new inventory, or stepping up production of items in high demand, to policies regarding investment, research and development (R&D), or advertising, and business strategies about product diversification and overseas investment. In our evolutionary theory, these routines play the role that genes play in biological evolutionary theory.[15]

Thus, according to Nelson and Winter, it is these *routines* that serve as the *memes* that transcend technology generations. Under this definition, routines certainly include the complex manufacturing processes employed in CMOS production. As has been discussed, this process has not essentially changed since the 1970s, while the planar method—the foundational production technique—dates back to the first commercial ICs a decade before this. Hodgson (1993) points out that selection goes on as ill-adapted routines fall out of use and ones associated with higher profit levels—or lower cost levels—are adopted.[16] So although photolithography, as one example, has been an essential routine in the production of planar ICs from the beginning, the industry has continually adapted the routine through a series of different types of alignment techniques including contact, proximity, scanning projection, and step-and-repeat (Henderson, 1988). Interestingly, Henderson uses the phrase 'generational innovation' to

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[13] Geoffrey M. Hodgson, "Theories of Economic Evolution: A Preliminary Taxonomy," *The Manchester School*, Vol. LXI, No. 2, June 1993, 139.
[14] Richard R. Nelson and Sidney G. Winter, *An Evolutionary Theory of Economic Change*, Cambridge, MA: Harvard University Press, 1982, 9, quotes in original.
[15] Ibid., 14, quotes in original.
[16] Hodgson, op. cit., 135.

describe innovation rooted in the structure of the technology itself, considering each successive "generation" of alignment technology was distinct and displaced the previous one.[17]

Constant (2000) directly asks the questions, "What is it that evolves? What is the unit of heredity?" His view of 'techniques' and 'science itself' as the fundamental element of evolution combines qualities of both information (reliable knowledge) and Nelson and Winter's 'routines':

> I have chosen to focus on the evolution of technological knowledge or information. This harmonizes with the neo-Darwinian principle that what counts in the evolution of living systems is ancestor-descendant lineages of information—genes metaphorical if not genes literal.
>
> What in technology evolves then—in the very specific and demanding sense of 'becomes better fit'—is information, the fit between phenomena and noumena, that is, reliable knowledge… [W]hat matters is inheritance, not superficial morphological similarities. Thus, on this view, the evolution of technology becomes the descent and modification, or recombination or mutation or saltation, of fabrication techniques, designs, design techniques, and, more recently, engineering science and science itself—information.[18]

Nelson and Winter use the term 'search' to denote all organizational activities associated with the evolution of current routines, and which may lead to their modification, to more drastic change, or to their replacement. They state, "Search routines stochastically generate mutations."[19] In their conclusion, the authors emphasize the importance of genetic routines over firms (i.e., the phenotypes or temporal structures):

> [I]n particular, it is important to remember that it is ultimately the fates of populations or genotypes (routines) that are the focus of concern, not the fates of individuals (firms).[20]

Another conjecture of genetic information that underlies technological change is offered by Dasgupta (1996) as "knowledge of operational principles," common among all practitioners of technology:

> The craftsman of old, laboring in his shop, and the modern engineer sitting at her computer workstation seem worlds apart; and yet they share this one central thing: they

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[17] Rebecca M. Henderson, *The Failure of Established Firms in the Face of Technical Change: A Study of Photolithographic Alignment Equipment*, Ph.D. Dissertation, Harvard University, 1988, 9-10.
[18] Edward Constant, Recursive Practice and the Evolution of Technological Knowledge," in Ziman (ed.), 2000, 223.
[19] Ibid., 400.
[20] Ibid., 401.

> are both concerned with the *creation of artifacts*. They are both, in this particular sense, practitioners of technology.[21]
>
> But above all, the knowledge that most distinguishes the technologist from other knowing beings and that has been common to all creators of artifacts from the dawn of humankind to the age of space and the computer is the knowledge of operational principles.[22]

Dasgupta further argues that technological creativity is conditioned by evolutionary history. He invokes biological concepts of *ontogeny* (i.e., the course of development of a single organism) and *phylogeny* (i.e., evolutionary development of a species) and uses the phrase "phylogenic history" to imply lineage:

> Thus, history is present in one way or another in acts of technological creation. Artifacts, even the most innovative kind, possess evolutionary pasts. The nature of this evolutionary history is not ontogenic. It is a longer-term phenomenon, involving years, decades, even in some cases, centuries. It entails a historically linked network of mature artifactual forms, the end product of which is the newly invented form. In sum, technological creativity is conditioned by the evolutionary past. Every act of invention or design has a phylogenic history. This, of course, is the *phylogenic law*.[23]

Similarly, Sahal (1985, 1981) offers a 'metaevolutionary explanation' of innovation viewing invariance in design as the underpinning factor. He refers to this function as a *technological guidepost* that operates along an *innovation avenue*:

> [T]he innovation process in a wide variety of fields is governed by a common system of evolution. Typically, the process of technological development within any given field leads to the formation of a certain pattern of design. The pattern in turn guides the subsequent steps in the process of technological development. Thus innovations generally depend upon bit-by-bit modification of an essentially invariant pattern of design. This basic design is in the nature of a *technological guidepost* charting the course of innovative activity.
>
> There is an important corollary to the above proposition. It is that technical advances do not take place in a haphazard fashion. Rather, they are expected to occur in a systematic manner on what may be called *innovation avenues* that designate various distinct pathways of evolution. We may say that the technological guideposts point to the innovation avenues just as the innovation avenues lead to technological guideposts.
>
> [I]t can be justifiably concluded that technical progress is governed by an *inner* logic or law of its own.[24]

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[21] Subrata Dasgupta, *Technology and Creativity*, New York: Oxford University Press, 1996, 9, italics in original.
[22] Ibid., 181, italics in original.
[23] Ibid., 185, italics in original.
[24] Devendra Sahal, "Technological guideposts and innovation avenues," *Research Policy*, Vol. 14, No. 2, 1985, 71, italics in original.

Though Sahal does not specify a basic genetic element in technical progress, the last sentence of the above caption implies a comparable self-determined character. Similar concepts including paradigms, regimes, and trajectories will be discussed in a subsequent section of this chapter.

Finally, Rothschild (1990) coined the term 'bionomics' as a hybrid method of studying biology and economics; he put forward, "By way of analogy, bionomics argues that, on a day in-day out basis, biological and economic life are organized and operate in much the same way."[25] He suggests that economic development is not shaped by a society's genes, but its accumulated technical knowledge. Specifically, it is the technological information, captured in books, blueprints, scientific journals, databases, and the know-how of millions of individuals, that is tantamount to the genetic information recorded in the biological DNA molecule. "Technology, not people, holds center stage in this view of economic life… the ultimate source of all economic life."[26]

Thus, from this review a more apt description of memes in technological change is twofold. First, there is a strong cognitive element grounded in technological knowledge. This aspect includes Mokyr's knowledge base elements, Dasgupta's knowledge of operational principles, Sahal's invariant pattern of design, Constant's reliable knowledge, and Rothschild's technological information. Secondly, there is also a behavioral component embodied in Nelson and Winter's routines and Constant's techniques. Technological knowledge and techniques—the *how*—comprise the broader definition of technology, and are of increasing interest to research into the innovation process. Understanding this within the framework of evolutionary theory makes this more evident.

As important, evolutionary theory also informs us what does *not* evolve is the technological artifact—the *what*—or the narrowest definition of technology. Equivalent to phenotypes in

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[25] Michael Rothschild, *Bionomics: Economy as Ecosystem*, New York: Henry Holt and Company, 1990, xiii.
[26] Ibid., xi.

biological evolutionary theory, artifacts embody temporal characteristics that must cope with specific needs or problems brought by an ever-changing user community. Thus, the study of technological artifacts in isolation—as one would study a series of museum exhibits—is not revealing of the forces behind evolutionary technological change. Nor would an isolated examination of technological knowledge and techniques independent of their end-uses be revealing. However, an inquiry into the interactive (i.e., evolutionary) nature of technological innovation that considers both meme and phenotype is instructive. Constant underscores this view with an insightful quote from Lorenz (1962), briefly mentioned in Chapter 3, on how the evolutionary process, in action, furthers knowledge, hence furthers evolution:

> Only when the system is expected to work, that is, to achieve something in relation to the external world in which the real and species-preserving meaning of its whole existence does indeed consist, then the thing begins to groan and creak: when the shovels of the dredging-machine dig into the soil, the teeth of the band saw dig into the wood, or the assumptions of the theory dig into the material of the empirical facts ..., then develop the undesirable side-noises that come from the inevitable imperfection of every naturally developed system ... But these noises are just what does indeed represent the coping of the system with the real external world. In this sense they are the door through which the thing-in-itself peeps into our world of phenomena, the door through which the road to further knowledge continues to lead.[27]

The next section is a closer examination of evolutionary economics, from which *The Complexity Challenge* derives concepts relating to the process of technological innovation.

Evolutionary Economics

Like most fields, there is not one interpretation of evolutionary economics. Schools of thought include Marxism, institutionalism, the Schumpeterian tradition, and others. For the purpose of this study, the Schumpetarian tradition is the starting-off point. With his thesis on economic development resulting from spontaneous and discontinuous change, Schumpeter challenged the traditional (classical) view of an economic system's tendency toward equilibrium. His view of

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[27] K. Lorenz, "Kant's Doctrine of the *A Priori* in the Light of Contemporary Biology," *General Systems*, 7, 1962, 23-35, quoted in Constant, Ziman (ed.), 2000, op. cit., 233. The phrase 'thing-in-itself' is also referred to as 'noumena' and represent an otherwise unknowable world-as-it-is. *Noumena* are contrasted with *phenomena*, our perceptions of, or our beliefs about, the world. Constant states that Donald Campbell's original quest of evolutionary epistemology—still valid nearly 40 years later—is to understand, in Campbell's memorable phrase, the progressively better 'fit of phenomena to noumena'. (220)

change was distinct and central to what he first referred to as a process of 'dynamics'.[28] He called such change 'innovation' and assigned primary responsibility for innovation to the entrepreneur. Schumpeter saw the entrepreneurial function as *the* vehicle of continual reorganization of the economic system. Although he did not use the term *per se*, some scholars who followed him have called this process 'evolutionary'.[29] In his later work he refined this idea of continual reorganization and coined the oft-cited phrase 'perennial gale of creative destruction' which he attributed to the inherent forces of capitalism. He would also reconcile with the evolutionary concept:

> The essential point to grasp is that in dealing with capitalism we are dealing with an evolutionary process… Capitalism, then, is by nature a form or method of economic change and not only never is but never can be stationary… The fundamental impulse that sets and keeps the capitalist engine in motion comes from the new consumers' goods, the new methods of production or transportation, the new markets, the new forms of industrial organization that capitalist enterprise creates.[30]

Since Schumpeter, many authors have contributed to this field of research. This area of inquiry would later be referred to as *neo-Schumpeterian*.[31] Within this tradition, Dosi and Nelson (1993) underscore the importance of evolutionary analysis:

> Most scholars interested in this issue—be they from biology, economics, sociology, or whatever—would agree that the term "evolutionary" ought to be reserved for theories about dynamic time paths, that is ones that aim to explain how things change over time, or to explain why things are what they are in a manner that places weight on "how they got there."[32]

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[28] Schumpeter later dropped the use of 'dynamic(s)' because of its variety of meanings, preferring to call his unique concept of endogenous economic change simply *development*. See Joseph A. Schumpeter, *The Theory of Economic Development: An Inquiry into Profits, Capital, Credit, Interest, and the Business Cycle*, translated by Redvers Opie, New York: Oxford University Press, 1961 (originally published 1934), 64.
[29] It is interesting to note that Schumpeter initially avoided use of the evolutionary concept, noting that the idea had lost credibility. See Ibid., 57-8: "…the evolutionary idea is now discredited in our field, especially with historians and ethnologists... To the reproach of unscientific and extra-scientific mysticism that now surrounds the "evolutionary" ideas, is added that of dilettantism. With all the hasty generalisations in which the word "evolution" plays a part, many of us have lost patience."
[30] Joseph A. Schumpeter, *Capitalism, Socialism, and Democracy (Third Edition)*, New York: Harper & Brothers Publishers, 1950 (originally published 1942), 82.
[31] Nelson and Winter, 1982, op. cit., 39.
[32] Giovanni Dosi and Richard R. Nelson, "Evolutionary Theories in Economics: Assessment and Prospects," Typescript, June 1993, 3, quotes in original.

Dosi describes the purpose of evolutionary theories in the field economics, where a rich literature has amassed:

> I consider under the label of 'evolutionary theories' a rather heterogeneous set of modeling efforts which share the emphasis on the dynamic properties of economies characterized by repeated emergence of various forms of innovation, decentralized processes of discovery and historical persistence of particular patterns of change… [E]volutionary theories attempt to model economic systems rich in positive feedbacks (that is, self-reinforcing mechanisms such as dynamic increasing returns in innovation). Relatedly, such systems tend to exhibit non-linear dynamics and multiple dynamic paths also dependent on their history.[33]

Returning to Schumpeter's thesis on economic development (1934) as a dynamic process that, by definition, does not seek equilibrium, his unique description is worth noting:

> Development in our sense is a distinct phenomenon, entirely foreign to what may be observed in the circular flow or in the tendency towards equilibrium. It is spontaneous and discontinuous change in the channels of the flow, disturbance of equilibrium, which forever alters and displaces the equilibrium state previously existing. Our theory of development is nothing but a treatment of this phenomenon and the processes incident to it. [footnote: …what we are about to consider is that kind of change arising from within the system *which so displaces its equilibrium point that the new one cannot be reached from the old one by infinitesimal steps*. Add successively as many mail coaches as you please, you will never get a railway thereby.][34]

The point of the railway footnote is instructive. Schumpeter uses it as a follow-up to an earlier reference. It is meant to contrast what he calls 'static' analysis in the equilibrium context where he uses an example of a small retailer gradually growing to a large department store, but never changing its form through discontinuous change. A railway, on the other hand, cannot be transformed (i.e., undergo development) solely through continuous change to only one small component such as a mail coach:

> The building of a railway may serve as an example. Continuous changes, which may in time, by continual adaptation through innumerable small steps, make a great department store out of a small retail business, come under the "static" analysis. But "static" analysis is not only unable to predict the consequences of discontinuous changes in the traditional way of doing things; it can neither explain the occurrence of such productive revolutions nor the phenomena which accompany them. It can only investigate the new equilibrium position after the changes have occurred.[35]

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[33] Giovanni Dosi, "Perspectives on Evolutionary Theory," *Science and Public Policy*, December 1991, 354.
[34] Schumpeter, 1961, op. cit., 64, italics in original.
[35] Ibid., 62-3.

Ziman (2000) points out that the units of analysis in evolutionary economics are industrial firms, "treating them as social institutions driven by market forces to adapt to changing technological regimes."[36] Adding theoretical elements to this, Metcalf (1994) asserts that the principal themes of evolutionary economics are *variety* and *selection*: variety as the processes which determine the range of actual innovations introduced into the economy, and selection as the processes which alter the relative economic importance of the competing alternatives. The relation between variety and selection is two-way; variety drives selection while positive and negative feedback processes through market competition mean that the development of variety is shaped by the process of selection.[37] Thus, one of the features of technological innovation in an evolutionary context is that it involves co-evolution of artifacts and institutions. *Sociotechnical* systems, discussed shortly, best embodies this idea. Table 4-1 provides a quick review of other aspects of evolutionary economics by comparing conventional (Old) and evolutionary (New) concepts in economic theories.

Table 4-1. Old vs. New Concepts in Economic Theories

Concept	*Old*	*New*
(i) Technology	Unit capital/labor rations	Systems/paradigms/trajectories
(ii) Equilibrium	Identifiable point of convergence and reference	Does not exist. Far from equilibrium behavior/complex cycles.
(iii) Information	Perfect knowledge/risk	Uncertainty/ignorance
(iv) Analytical Units	Homogenous	Complex
(v) Determinacy	Complete/closed systems/uncreative	Weak/open systems/creative
(vi) Morphogenesis	None	Permitted
(vii) Analytical Style	Deductive	Inductive
(viii) Institutions	Barriers to market forces	Enablers of technical change

Source: Norman Clark, "Some New Approaches to Evolutionary Economics," *Journal of Economic Issues*, Vol. XXII, No. 2, June 1988, Table 1, 518.

[36] John Ziman, "Evolutionary Models for Technological Change," in Ziman (ed), 2000, op. cit., 9.
[37] J. S. Metcalfe, "Evolutionary Economics and Technology Policy," *The Economic Journal*, 104 (July), 933.

Perhaps the most authoritative treatises of neo-Schumpeterian evolutionary theories are offered by Nelson and Winter (1982, 1977). A brief review of these two pieces follows. In Nelson and Winter's classical article, "In Search of Useful Theory of Innovation," they state that prevailing 'production function' theory of innovation has neither the breadth nor the strength to provide much guidance regarding the variables that are plausible to change, or to predict with much confidence the effect of significant changes.[38] The authors propose a new approach to the study of innovation, emphasizing the importance of recognizing uncertainty and institutional roles. They argue that uncertainty and institutional complexity and diversity are salient attributes of innovation which have been "ignored in much of the literature concerned with policy towards innovation."[39] Interestingly, the semiconductor industry Roadmap is an institutional process that recognizes within its design both factors:

> The first of these facts is that innovation involves uncertainty in an essential way. The implicit process characterization of the 'production function' models would appear to be not only rudimentary, but fundamentally misleading… Rather, a theoretical structure must encompass an essential diversity and disequilibrium of choices… Explicit recognition of uncertainty is important in thinking about policy.
>
> A second fact that the microcosmic studies have illuminated is that the institutional structure for innovation often is quite complex within the economic sector, and varies significantly between economic sectors.[40]

The authors begin to depart from the original Schumpeterian view of development in discussing Rosenberg's concept of 'technological imperatives' as guiding the evolution of certain technologies.[41] The authors introduce the concept of natural trajectories and technological regimes as concepts that would soon receive much research interest. This and related ideas of technological change will be discussed in detail shortly under the topic of *consensus paradigms*. It is within this rubric that is the main focus of this study. The authors cited an oft-used example of incremental development—the Douglas DC3 aircraft:

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[38] Richard R. Nelson and Sidney G. Winter, "In Search of Useful Theory of Innovation, *Research Policy* 6, 1977, 38.
[39] Ibid., 71.
[40] Ibid., 47.
[41] Nathan Rosenberg, "The Direction of Technological Change: Inducement Mechanisms and Focusing Devices," *Economic Development and Cultural Change*, Vol. 18, No. 1, pt1, October 1969, 1-24.

> For example, the advent of the DC3 aircraft in the 1930's defined a particular technological regime; metal skin, low wing, piston powered planes. Engineers had some strong notions regarding the potential of this regime. For more than two decades innovation in aircraft design essentially involved better exploitation of this potential; improving the engines, enlarging the planes, making them more efficient… In other words, a regime not only defines boundaries, but also trajectories to those boundaries. Indeed these concepts are integral, the boundaries being defined as the limits of following various design trajectories.

The authors conclude with a proposition that natural trajectories are more observable in industries experiencing rapid growth, like semiconductors, but that trajectories are not necessarily inevitable. Rather, the role of scientific and technological knowledge (i.e., *memes*) seems to be the underlying factor:

> In particular, the discussion of natural trajectories, which we conjectured (interpreting the conjectures of others) were associated with sectors where technological advance has been most rapid, may have given the flavor of 'innate' differences. However, we suggest that it is an open question whether it is inevitable that natural trajectories exist for certain technologies but not for others. We have put forth the proposition that underlying natural trajectories there is a certain body of knowledge that makes the traverse relatively easy, and that in the recent half century formal science has been an important part of that knowledge.[42]

While Nelson and Winter's article begged the question of evolutionary factors underlying innovation, it was their comprehensive book, *An Evolutionary Theory of Economic Change,* that provided the real impetus for a whole new approach to the study of innovation.[43] In the Schumpeterian tradition, the emphasis is the unfolding of economic events over time as opposed to rigid adherence to conventional general equilibrium theory's austere description of the institutions of capitalism. The authors begin with a discussion of contrasting positions referred to as "orthodox" and "evolutionary." Note some similarity with Table 4-1 comparisons.

> Throughout this book, we distinguish our own stance on various issues from the "orthodox" position… We should note, first of all, that the orthodoxy referred to represents a modern formalization and interpretation of the broader tradition of Western economic thought whose line of intellectual descent can be traced from Smith and Ricardo through Mill, Marshall, and Walras. Further it is a *theoretical* orthodoxy, concerned directly with the methods of economic analysis and only indirectly with any specific questions of

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[42] Ibid., 73.
[43] Nelson and Winter, 1982, op. cit.

> substance. It is centered in microeconomics, although its influence is pervasive in the discipline.[44]
>
> The broader connotations of "evolutionary" include a concern with processes of long-term and progressive change. The regularities observable in present reality are interpreted not as a solution to a static problem, but as a result that understandable dynamic processes have produced from known or plausibly conjectured conditions in the past—and also as features of the stage from which a quite different future will emerge by those same dynamic processes.[45]

The authors stress the significance of Joseph Schumpeter's influence on their work and, as previously mentioned, suggest the term "neo-Schumpeterian" as an appropriate designation for their entire evolutionary approach.[46] They remark on the extent to which the influence of the Schumpeterian vision has been limited over the years for want of adequate development (particularly *formal* theoretical development) of constitutive or complementary ideas. They cite an incisive passage from Schumpeter's *The Theory of Economic Development*:

> The assumption that conduct is prompt and rational is in all cases a fiction. But it proves to be sufficiently near reality, if things have time to hammer logic into men. Where this has happened, and within the limits in which it has happened, one may rest content with this fiction and build theories upon it... Outside of these limits our fiction loses its closeness to reality. To cling to it there also, as the traditional theory does, is to hide an essential thing and to ignore a fact which, in contrast with other deviations of our assumptions from reality, is theoretically important and the source of the explanation of phenomena which would not exist without it. (Schumpeter, 1934, 80)[47]

Indeed, the book is in many ways an attempt to operationalize Schumpeter's theories through use of evolutionary models.

Expanding further on the idea of organizational routines, much attention is paid to the importance of skills, knowledge, and in particular, tacit knowledge. They cite driving an automobile as prominent among their own examples of the exercise of individual skill and acknowledge Machlup's earlier treatment of the topic by quoting at some length from his well-known analogy between the theory of the maximizing firm and the "theory of overtaking":

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[44] Ibid., 6, emphasis in original.
[45] Ibid., 10, quotes in original.
[46] Ibid., 39.
[47] Ibid., 40.

Box 4-1. Machlup's "theory of overtaking"[48]

What sort of considerations are behind the routine decision of the driver of an automobile to overtake a truck proceeding ahead of him at slower speed? What factors influence his decision? Assume that he is faced with the alternative of either slowing down and staying behind the truck or of passing it before a car which is approaching from the opposite direction will have reached the spot. As an experienced driver he somehow takes into account (a) the speed at which the truck is going, (b) the remaining distance between himself and the truck, (c) the speed at which he is proceeding, (d) the possible acceleration of his speed, (e) the distance between him and the car approaching from the opposite direction, (f) the speed at which that car is approaching, and probably also the condition of the road (concrete or dirt, wet or dry, straight or winding, level or uphill), the degree of visibility (light or dark, clear or foggy), and the condition of the tires and brakes of the car, and—let us hope—his own condition (fresh or tired, sober or alcoholized) permitting him to judge the enumerated factors. Clearly, the driver of the automobile will not "measure" the variables; he will not "calculate" the time needed for the vehicles to cover the estimated distances at the estimated rates of speed; and, of course, none of the "estimates" will be expressed in numerical values. Even so, without measurements, numerical estimates or calculations, he will in a routine way do the indicated "sizing-up" of the total situation. He will not break it down into its elements. Yet a "theory of overtaking" would have to include all these elements (and perhaps others besides) and would have to state how changes in any of the factors were likely to affect the decisions or actions of the driver. The "extreme difficulty of calculating," the fact that "it would be utterly impractical" to attempt to work out and ascertain the exact magnitudes of the variables which the theorist alleges to be significant, show merely that the *explanation* of an action must often include steps of reasoning which the acting individual himself does not *consciously* perform (because the action has become routine) and which perhaps he would never be *able* to perform in scientific exactness (because such exactness is not necessary in everyday life).

The businessman who equates marginal net revenue productivity and marginal factor cost when he decides how many to employ need not engage in higher mathematics, geometry, or clairvoyance. Ordinarily he would not even consult with his accountant or efficiency expert in order to arrive at his decision; he would not make any tests or formal calculations; he would simply rely on his sense or his "feel" of the situation. There is nothing very exact about this sort of estimate. On the basis of hundreds of previous experiences of a similar nature the businessman would "just know," in a vague and rough way, whether or not it would pay him to hire more men.[49]

The review of relevant concepts from evolutionary theory and evolutionary economics round out the coverage of complexity science concepts examined in Chapter 3. With this foundational understanding it is now possible to begin to advance a theory of industrial innovation for

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[48] F. Machlup, 1946. "Marginal Analysis and Empirical Research." *American Economic Review* 36: 534-5. Note that the English driver "overtakes" a proceeding vehicle whereas an American "passes" one. Similarly, early technology roadmaps in the United Kingdom were referred to as "route maps" (source: Rob Phaal, Cambridge University).

[49] Nelson and Winter, 1982, op. cit.., 93.

semiconductors, of which the Roadmap is instrumental. Before this can be done, there is a need for additional discussion on the accumulation of knowledge, with emphasis on *collective* knowledge in an increasingly-complex environment, and how that knowledge becomes structured within an evolutionary framework.

Collective Learning and Heuristics

Organizational learning and more precisely, *network* learning, were discussed in Chapter 3. As previously stated, although individual expertise is necessary, it is the collaborative nature of learning that distinguishes networks such as the semiconductor innovation network. Organizational learning is defined as the process by which organizations increase their knowledge, skills, and capabilities through the collective and cumulative learning of individual members, characterized as local learning. What is learned is in part unique to those involved because it is based on previous accumulated learning that is partly tacit. Accumulated learning and knowledge play such a major role in the Machlup overtaking example above as in any other complex problem-solving process. Much of this knowledge would be considered 'know-how' or artisanal skills.[50] It is generally tacit and incorporates ideas of training and practice to achieve proficiency. This type of learning could be referred to as *heuristics*, also mentioned in Chapter 3. Nelson and Winter define a heuristic as "any principle or device that contributes to the reduction in the average search to solution."[51] As Rycroft and Kash have argued, heuristics provide enough structure to focus and guide search activities while still allowing enough flexibility to keep open the consideration of a variety of plausible modifications in these activities. Baba and Imai (1993) state that the emergent network organization should be viewed firstly as a dynamic framework, since "*the essence of a network … inheres in its dynamic properties rather than static ones*." The authors elaborate on the importance of 'context':

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[50] Stanley R. Carpenter, "Modes of Knowing and Technological Action," *Philosophy Today*, Summer 1974, 163.
[51] Ibid., 132-3.

> [W]e will use the term 'context' to refer to the *heuristic information core* shared among the network participants which does not provide a unique set of solutions whose structure is concretely specified, but certainly leads the participants' problem-solving activities in the right direction. Put differently, under a given technological trajectory, it is the 'context' that provides the participants with the kind of guidance that indicates the direction their normal technical progress should take, and helps to decide which characteristics of a particular technology users will eventually come to value most highly.[52]

Indeed, the Roadmap process serves this purpose: it may be viewed as embodying industry-level heuristics, as the outcome is the continued advancement of semiconductor technology through the collective knowledge and capabilities of its participants.

Every field of specialized competence contains a wide range of heuristics that are particularly appropriate to that field. Nelson and Winter point out that inventors and research and development engineers operate under a higher order objective to look for inventions and design chances that will reduce costs and improve performance.[53] Engineers, through training and experience, apparently acquire heuristics that assist the design of technologies. But when collectively addressing a technological problem, as is the case in the Roadmap, Rycroft and Kash point out that a community of practitioners (referred to as a technological community) comprised of those individuals, groups, and organizations share a particular model of problem-solving for a specific technology path. That is, the members of the community share a common, experienced-based, body of heuristics (i.e., how to do things, where to search) and have broad agreement on the key technological and organizational obstacles and opportunities likely to be encountered in the future evolution of the trajectory. The community will have some consensus regarding how to advance the state of the art.[54]

According to Linda Wilson, ITRS Information Manager and Roadmap Managing Editor at International Sematech, one of the reasons the Roadmap was developed (and continues) is to focus effort on increasingly difficult chip-making challenges facing the industry. Today's chips and

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[52] Yasunori Baba and Ken-ichi Imai, "A network view of innovation and entrepreneurship: The case of the evolution of the VCR systems," *International Social Science Journal*, February 1993, 25, emphasis in original.
[53] Nelson and Winter, 1977, op. cit., 59.
[54] Rycroft and Kash, 1999, op. cit., 98.

the fabrication processes needed to produce them are far more complex than previously. Simpler designs and architectures (i.e., larger feature sizes and fewer metal layers) in earlier times meant a lot more 'wiggle room' for improvement.[55] Today, however, these advances must come within much tighter technical and economic constraints. This situation necessitates increased dependencies on related technologies as trade-offs (e.g., performance and speed vs. power and heat) have to be addresses collectively. Economically, research, development, and manufacturing costs escalate exponentially while timestamps on technologies become ever shorter. This combination of factors underscores the need for the Roadmap and the collective heuristics that it brings.

Behavior in the semiconductor industry's innovation enterprise is consistent with broader trends in technological innovation. One such trend is the increasing recognition that innovation is more a collective endeavor that draws from many sources rather than the 'lone inventor' theories that popularized an earlier era. Of course this is not necessarily a new finding as Usher (1959/1929) was also critical of what he called the "great-man theory of history."[56] Nonetheless, Van de Poel (2002) writes:

> The days that technical innovation and invention were seen as creative acts of some lonesome genius seem long gone. In the literature on innovation and technology dynamics, there is now widespread recognition that invention and innovation are conditioned by such factors as earlier innovations, the search heuristics of engineers in an industry, available technical knowledge, market demand and industrial structure. As a result, innovation is often incremental and cumulative.[57]

Similarly, Hargadon's analysis (2003) of the innovative activities of Thomas Edison, who is commonly recognized as the model lone inventor, is corroborated with other breakthrough technological developments that were more the result of a recombinant or incremental innovation process:

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[55] Linda Wilson, telephone interview, December 28, 1998.
[56] Abbot Payton Usher, *A History of Mechanical Invention*. Boston: Beacon Press, 1959, 60; first published by Cambridge, MA: Harvard University Press, 1929.
[57] Ibo van de Poel, "The Transformation of Technological Regimes," *Research Policy* 1374 (2002) 1-20, *uncorrected proof*: *article is based on Ph.D. thesis* (van de Poel, 1998).

> Indeed, Edison did more than perhaps anyone else to fix in our minds the notion that innovation is the province of the creative genius and his or her inventions. Yet those who worked alongside him tell a different story, as does closer examination of the technological marvels that emerged from his Menlo Park lab. Instead, Edison owed his success to his ability to build his inventions from the previous work of others—work that spanned markets, continents, and decades. Edison took elements of these existing technologies and recombined them in ways that had never existed before and for markets that had never seen them before. The origins of other technological revolutions—the development of mass production, the transistor, the personal computer—reveal similar hidden histories. These backstage stories do not detract from the revolutionary impact of these technologies, but they do require dramatic changes in how we perceive and, in turn, pursue the innovation process.[58]

Van de Poel also cites Nelson and Winter (1977, 1982) and their use of the term *technological regime* to refer to the search heuristics of engineers in an industry. According to the authors, "the sense of potential, of constraints, and of not yet exploited opportunities, implicit in a regime focuses the attention of engineers on certain directions in which progress is possible, and provides strong guidance as to the tactics likely to be fruitful for probing in that direction. In other words, a regime not only defines boundaries, but also trajectories to those boundaries." (Nelson and Winter, 1977:57)[59]

Technological regimes have a broader reach than simply among the immediate innovation community (e.g., design engineers) and ultimately influence stakeholders some steps removed from the pure technical aspects of innovation. This is consistent with the Rip and Kemp (1998) interpretation of technological regime which they define as the rule-set or grammar that is characteristic for the development of a technology and that guides not only the search activities of engineers, but also the actions and interactions of the other actors involved in technical development.[60]

In keeping with the evolutionary view of technology, heuristic knowledge embedded within a technological community provides the genetic character and thus replication and continuance of a technological regime. In analyzing the microelectronics industry, Perez (1985) asserts that a

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[58] Andrew Hargadon, *How Breakthroughs Happen: The Surprising Truth About How Companies Innovate*, Boston: Harvard Business School Press, 2003, xii-xiii.
[59] van de Poel, op. cit.
[60] Ibid.

techno-economic paradigm serves as a general guiding model for productive behavior. She suggests that these behaviors follow more or less predictable trends for relatively long periods as techno-economic paradigms provide a general 'rule-of- thumb' guide for investment and technological decisions. As a paradigm generalizes, it introduces a strong bias in both technical and organizational innovation so that eventually the range of choice in technique is itself contained within a relatively narrow spectrum as the supply of capital equipment increasingly embodies the new principles. Perez draws an evolutionary comparison:

> The process can be seen as analogous to the appearance of a new genetic pool, which contains the blueprint for a great variety of organisms (products and processes) and their forms of interrelation. It diffuses through hybridization, cross-breeding, evolution and new entrants. Its increasingly obvious advantages inevitably destine it to transform most and substitute many of the old 'species' and create a new 'eco-system.'[61]

With the idea of regularity in innovation through search heuristics, regimes, trajectories, and paradigms we now probe deeper into the broader literature on consensus paradigms, a seemingly essential element of the Roadmap.

The Role of Consensus Paradigms

Perez's use of the concept 'paradigm' is but one of numerous authors' generalized interpretations of Kuhn's central argument from his seminal work, *The Structure of Scientific Revolutions*.[62] According to Kuhn, paradigms are described as universally recognized scientific achievements that for a time provide model problems and solutions to a community of practitioners. This could be understood as something accepted at face value, taken for granted, second nature, conventional wisdom, or even 'truth', albeit temporarily. As an illustration, Kuhn cites a card experiment involving red spades. One is conditioned to the convention of black spades (like red diamonds), and when confronted with an *anomaly* such as red spades, initially they are ignored. Only after repeated exposures to red spades is the difference realized. Likewise, repeated

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[61] Carlota Perez, "Microelectronics, Long Waves and World Structural Change: New Perspectives for Developing Countries," *World Development,* Vol. 13, No. 3, 443-4, 1985.
[62] Thomas S. Kuhn, *The Structure of Scientific Revolutions*, Chicago: University of Chicago Press, 1970.

challenges (or anomalies) of an accepted paradigm can produce *crisis*, which according to Kuhn brings to the forefront the fragility of the existing paradigm. New answers are offered, eventually formulating a new paradigm based on different values, assumptions, etc. Drawing a parallel with major political change, Kuhn describes this process of shifting of paradigms as 'scientific revolution'. Among other examples, Kuhn cites the emergence of the Copernican theory of the universe as scientific revolution, displacing the Ptolemaic view or paradigm that prevailed for well over a dozen centuries.

By *consensus paradigm* what is briefly meant is some broad idea, theory, model, or other organizing principle that is commonly recognized and accepted by an innovation community (this definition will be expanded shortly). The addition of the term *consensus* to this concept may at first seem redundant as a paradigm is, by definition, universally recognized. However, consensus deals with opinions, ideas, and less tangible items than models, designs, or illustrative examples. Consensus is certainly shaped by a paradigm, as much so as a paradigm is greatly influenced by consensus. Neither is complete without the other, yet they are different concepts. Thus, they are two sides of the same coin in much the same way that *sociotechnical* systems better describe both the social and technical components of technology as described in Chapter 3. By combining the terms the intent is to explicitly recognize the role of consensus, of expectations, of even belief that institutions such as Moore's Law and the Roadmap bring forth.

A key dimension in the historical success of the semiconductor industry is the role played by consensus paradigms in guiding the process of technological innovation. Following the tradition of Kuhn (1970, 1962), subsequent works examining the history of several technologies (Bijker et al, 1990; Vincenti, 1990, 1984; Constant, 1980, 1973) have built upon this concept. Constant's *Origins of the Turbojet Revolution*, in fact, uses Kuhn's conceptual framework as the basis for his analysis. Constant's *presumptive anomaly* involving the limitation of propeller-driven engines was commonly recognized and helped guide the aircraft engine community to a new paradigm—the turbojet. Similarly, Vincenti's assessment that a design consensus requiring the use of flush rivets

to decrease drag and increase performance of aircraft involved an almost simultaneous recognition of the problem among the aircraft design community.

Gordon Moore's observation almost four decades ago that the circuit density of semiconductor devices had doubled on a regular basis and would continue to do so was also commonly understood within the semiconductor design community. Each of these examples illustrates the significance of consensus paradigms. At the same time, consensus paradigms produce path dependency behavior, as previously discussed, that limits innovative activities to some degree. Overall, the role of consensus paradigms is to simplify, guide, coordinate, and even control the efforts of large and diverse networks involved in technological innovation. But the origin, development, and widespread acceptance (i.e., consensus) of these paradigms is very subtle and complex.

Relating this to the rapidly changing semiconductor industry, one wins by literally making products obsolete. In a very real sense, a timestamp or 'use-by-date' mentality is increasingly recognized and accepted as new capabilities replace old with the regularity of Moore's Law—in so doing, setting the very pace of technical progress. The next section will examine the guiding/organizing principle of consensus paradigms in general and the Roadmap in particular.

Recall from Chapter 1 Hypothesis 3: Existence of a consensus paradigm increases the success rate of S&T roadmaps. This hypothesis was tested during the research and it was generally found that the unique pattern of technological change in semiconductors following "Moore's Law" is a key factor in the success of the SIA Roadmap (see Chapter 11 for summary findings).

Technology Paradigms, Trajectories, Traditions, Focusing Devices, Guideposts

More broadly, the role of consensus paradigms in guiding the process of technological innovation seems a very important factor in many historical cases. For example, scholars in economics, economic history, history of technology, philosophies of science and technology, and

innovation studies have argued that organizing principles under a variety of labels bound the process of technological innovation. Cimoli and Dosi (1995) state that the notions of technological paradigms, trajectories (and largely overlapping ones such as dominant designs) entail a representation of technologies centered on the cognitive and problem-solving procedures which they involve.[63] The authors elaborate on the role of local and cumulative learning:

> A general property, by now widely acknowledged in the innovation literature, is that learning is local and cumulative. Local means that the exploration and development of new techniques is likely to occur in the neighborhood of the techniques already in use. Cumulative means that current technological development – at least at the level of individual business units – often builds upon past experiences of production and innovation, and it proceeds via sequences of specific problem-solving junctures. Clearly, this goes very well together with the ideas of paradigmatic knowledge and the ensuing trajectories.[64]

In an earlier work, Dosi (1991) referred to the variety of names that have been suggested for overlapping empirical invariances in the dynamics of specific groups of product and process innovation. These terms include "dominant designs," "technological paradigms," "regimes," "technological trajectories," and "techno-economic paradigms." All capture some features of relatively ordered patterns of innovation whereby:

- technological competences build incrementally upon past experiences of both successes and failures;
- learning capacities are imbedded within specific organisations, such as firms and public laboratories, and communities of practitioners such as engineers;
- some forms of increasing returns to learning often induce self-producing mechanisms of advancement; it is possible generally to identify rather ordered patterns of technical change in the technical and economic characteristics specific to each paradigm.[65]

A closer review of this literature reveals the following descriptors attributed to particular authors (some of these have already been mentioned):

- paradigms (Kuhn, Constant, Dosi)
- regimes (Nelson and Winter)

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[63] Mario Cimoli and Giovanni Dosi, "Technological paradigms, patterns of learning and development: an introductory roadmap," *Journal of Evolutionary Economics*, Vol. 5, No 3, 1995, 244.
[64] Ibid.
[65] Giovanni Dosi, "Perspectives on evolutionary theory," *Science and Public Policy*, December 1991, 355.

- trajectories (Nelson and Winter, Dosi, Rycroft and Kash)
- focusing devices, imperatives (Rosenberg)
- traditions of practice (Constant)
- guideposts (Sahal)
- dominant designs (Abernathy and Utterback)

With this background, more definition of consensus paradigm is required. This definition is derived from the works of Kuhn, Constant, Dosi, Nelson, Sahal, and Rycroft and Kash. Each author's use of the term is briefly described followed by a summary of the salient points that apply in the case of semiconductor innovations. From this analysis an expanded definition will be offered.

In examining the history of science, *Kuhn* refers to a *paradigm* as a term that relates closely to 'normal science', the genesis and continuation of a particular research tradition. Accepted examples of actual scientific practice including law, theory, application, and instrumentation together provide models from which spring particular coherent traditions of scientific research. A paradigm is what mainly prepares a student for membership into a particular scientific community where (s)he will later practice. Because (s)he joins others who learned the bases of their field from the same concrete models, his/her subsequent practice will seldom evoke overt disagreement over fundamentals. Those whose research is based on shared paradigms are committed to the same rules and standards for scientific practice. That commitment and the apparent consensus it produces are prerequisites for normal science."[66]

In examining the history of turbojet technology, *Constant* avoids using Kuhn's term 'paradigm' *per se* because of difficulties in definition. Instead he used 'traditions of practice' and 'conventional system' as corollaries. According to Constant, technological traditions of practice comprise complex information physically embodied in a community of practitioners and in the hardware and software of which they are masters. Such traditions define an accepted mode of

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[66] Thomas S. Kuhn. *The Structure of Scientific Revolutions*, Chicago: University of Chicago Press, 1970, 10-11.

technical operation, the conventional system for accomplishing a specified technical task and encompass aspects of relevant scientific theory, engineering design formulae, accepted procedures and methods, specialized instrumentation, and, often, elements of ideological rationale. Constant emphasizes the cognitive element of a paradigm: "It is a cognition: ask anyone before 1950 to make the sound of an airplane and he will buzz; ask someone born after 1950 and he will whistle—to the older an airplane has a propeller, to the younger it is a jet."[67]

Dosi refers to both 'technological paradigms' and 'technological trajectories' in his essay concerning the determinants and effects of innovative activities in contemporary market economies. Dosi's definition is a bit more esoteric. He observes that a crucial implication of the general paradigmatic form of technological knowledge is that innovative activities are strongly selective, finalized in quite precise directions, cumulative in the acquisition of problem-solving capabilities. He likens this to the relatively ordered patterns of innovation as shown in the study of technological forecasting.[68] He suggests that innovative search is characterized by strong uncertainty which applies primarily to those phases of technical change that could be called *pre-paradigmatic*. During these highly exploratory periods one faces a double uncertainty regarding both the practical outcomes of the innovative search and also the scientific and technical principles and the problem solving procedures on which technological advances could be based. When a technological paradigm is established, it brings with it a reduction of uncertainty, in the sense that it focuses the directions of search and forms the grounds for formatting technological and market expectations more surely."[69]

In an essay on evolutionary economics, *Dosi and Nelson* discuss the concept of a technological paradigm as the set of understandings about particular technologies that are shared by firms and engineering communities about the technology's present and innate limitations.

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[67] Edward W. Constant II. *The Origins of the Turbojet Revolution* (Baltimore: The Johns Hopkins University Press, 1980), 10, and Edward W. Constant II, "A Model for Technological Change Applied to the Turbojet Revolution," *Technology and Culture*, Vol. 14, No. 4, October 1973, 554.
[68] Giovanni Dosi. "Sources, Procedures, and Microeconomic Effects of Innovation" *Journal of Economic Literature*, XXVI:3, September 1988, 1128.
[69] Ibid., 1134.

Secondly and relatedly, it embodies the prevailing views and heuristics on "how to make things better." And thirdly, it is often associated with shared ideas or 'artifacts' which are there to be improved in their performances and made cheaper in their production. They also use the term technological trajectory to refer to the path of improvement taken by that technology, given technologists' perceptions of opportunities, and the market and other evaluation mechanisms that determined what kinds of improvements would be profitable.[70]

In explaining lawlike patterns of technological change, *Sahal* suggests a principle of 'technological guideposts'. He states that very often there emerges a pattern of machine design as an outcome of prolonged development effort that in turn continues to influence the character of subsequent technological advances long after its conception. Thus innovations generally depend on "bit-by-bit modifications" of a design that remains unchanged in its essential aspects over extended periods of time. This basic design is in the nature of a technological "guidepost charting the course of innovative activity." The notion of a technological guidepost is evidenced by the fact that very often one or two early models of a technique stand out above all others in the history of an industry. Their design becomes the foundation of a great many innovations via a process of gradual evolution. In consequence, they leave a distinct mark on a whole series of observed advances in technology. Examples include the farm tractor, steamboat, DC-3 airplane, and electric motors.[71] Sahal further argues that technical progress is best characterized as a process of learning by scaling. The origin of a wide variety of innovations lies in *learning* to overcome the constraints that arise from the process of *scaling* the technology under consideration.[72]

In a similar interpretation, Abernathy and Utterback (1978) use the term *dominant design* to describe related behavior. The authors argue that intriguing regularities in the course of technological progress appear throughout the history of incandescent light bulbs, paper, steel,

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[70] Giovanni Dosi and Richard R. Nelson. "Evolutionary Theories in Economics: Assessment and Prospects" Second Draft, June 1993, 29-30.
[71] Devendra Sahal, *Patterns of Technological Innovation*, Reading, MA: Addison-Wesley, 1981, 33.
[72] Devendra Sahal, "Technological Guideposts and Innovation Avenues," *Research Policy*, Vol. 14, No. 2, 1985, 61.

standard chemicals, internal-combustion engines, as well as aircraft and automobile industries: "superior designs of products like the DC-3 and the Model T Ford seem to mark turning points in the development of their respective productive units." These designs were synthesized from individual technological innovations that had been introduced independently in prior products. The important economic effects of a dominant design provide a benchmark for functional performance competition. In this environment innovation is typically incremental in nature, and it has a gradual, cumulative effect on productivity. In all these examples, major systems innovations have been followed by countless minor product and systems improvements. Such incremental innovation typically results in an increasingly specialized system of resource allocation.[73]

Rycroft and Kash refer to *technological trajectories* as evolutionary guideposts for innovative activities within a technological community or network. A technological trajectory traces the activity of technological advance according to the organizational and technological trade-offs made in the process of their coevolution. Trajectory evolution is the consequence of carrying out, in a particular way, the shared views of the technological community. Two common patterns emerged in their conduct of six separate cases studies of incremental innovations along technology trajectories. One is that the participants in the communities concerned with the technologies generally share a consensus view of what innovations will come next, through a common understanding of the performance characteristics to be developed. The other is that this shared consensus is empirically—not theoretically—based. The view of what would or will come next along each trajectory reflects a body of community knowledge derived from syntheses of potentially available technology enhancements and latent (potential, but unidentified market) needs. Further, all of the technologies experienced patterns of innovation along trajectories that reflect accumulated learning and technical expectations. Incremental innovations in all of the

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[73] William J. Abernathy, "General Model: Innovation and Process Change in a Productive Unit (James M. Utterback co-author) in William J. Abernathy, *The Productivity Dilemma: Roadblock to Innovation in the Automobile Industry*, Baltimore: The Johns Hopkins University Press, 1978, 68, and William J. Abernathy and James M. Utterback, "Patterns of Industrial Innovation," *Technology Review*, June/July 1978, Vol. 80, 40-47.

cases are significantly characterized by an interplay between technological advancement and network adaptation.[74]

The expanded definition of a consensus paradigm offered here draws from each of the above descriptions *but in the reverse order as to importance*. Drawing first from Rycroft and Kash, participants in the technological communities generally share a consensus view of what innovations will come next, through a common view of the performance characteristics to be developed. Also, this shared consensus is empirically—not theoretically—based. Finally, technological trajectories reflect accumulated learning and technical expectations. From Abernathy and Utterback, the important economic effects of a dominant design provide a benchmark for functional performance competition. From Sahal, lawlike patterns in innovativeness emerge from prolonged development effort that in turn continues to influence the character of subsequent technological advances. A self-reinforcing innovation system perpetuates a successful design which acts as a guidepost or broader architecture for further development. From Dosi and Nelson, technological paradigms embody the prevailing views and heuristics on "how to make things better" and often are associated with shared ideas or "artifacts" which are there to be improved in their performances and made cheaper in their production. From Dosi, a technological paradigm brings with it a reduction of uncertainty, thus focuses the directions of search and forms the grounds for formatting technological and market expectations more surely. From Constant, technological traditions of practice define an accepted mode of technical operation, the conventional system for accomplishing a specified technical task. Finally, from Kuhn, those whose research is based on shared paradigms are committed to the same rules and standards for scientific practice. That commitment produces in a word, *consensus*.

To summarize, the salient characteristics of a consensus paradigm include:

- a consensus view of what comes next
- that it is empirically, not theoretically, based

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[74] Rycroft and Kash. op. cit.

- a self-reinforcing innovation system that perpetuates a successful design
- accumulated learning (of the past) and technical expectations (of the future)
- the embodiment of heuristics on "how to make things better"
- the presence of "artifacts" to improve upon
- the reduction of uncertainty and risk
- the effect of focusing direction of technological search and market expectations
- traditions of practice that define an accepted mode of technical operation
- a shared commitment (consensus) to the rules and standards of scientific/innovative practice

In the unique case of semiconductor technology, one more characteristic can be added: *the consensus paradigm is explicit and openly articulated (i.e., Moore's Law publicly communicated through the Roadmap)*. Thus, a definition for a consensus paradigm for semiconductor technological innovation would include acceptance of Moore's Law as a benchmark for technical progress, along with the foundation of this premise: dependence upon silicon-based bulk planar CMOS technology which has been the tradition or 'dominant design'[75] of the industry since the 1970s.

So what is the role of a possible consensus paradigm in semiconductor industry innovations? Some authors have already speculated an answer to this question. Dosi's 1984 case study of the industry observed the unique effect of Moore's Law on technical change. Dosi asks, "What are the factors which shape the directions of the innovative activity when powerful external factors [e.g., early defense and space contracts] cease to exert their 'pulling' or 'pushing' influence?"[76] Without citing Moore's Law by name, his answer certainly supports this view by dubbing it a 'natural law' of the industry. He also notes both micro- and macro-economic effects that stem from the cumulative effects of this factor.

> '[N]ormal' technical progress maintains a momentum of its own which defines the broad orientation of the innovative activities. This in-built heuristic is particularly clear in the semiconductor case. Take, for example, the fundamental trend in the industry towards

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[75] Abernathy and Utterback, op. cit.
[76] Giovanni Dosi, *Technical Change and Industrial Transformation: The Theory and an Application to the Semiconductor Industry*, London: The MacMillan Press, 1984, 68.

> increasing density of the circuits: the doubling of the number of components per chip every year (in the late 1970s every two-three years) is almost a 'natural law' of the industry. After 1K memories one progressed to 4K, 16K, 64K and further increases in integration are expected. The same applies to microprocessors, from 4 to 8, 16, 32 bit devices. This *cumulative process* has an important role in the competitive process of the industry, by continuously creating asymmetries between firms and countries in their relative technological success.[77]

In his 1988 essay, in addition to aircraft technology, he cited microelectronics as an example of technical progress within a technological trajectory:

> In microelectronics, technical change is accurately represented by an exponential trajectory of improvement in the relationship between density of electronic chips, speed of computation, and cost per bit of information.[78]

More recently, Rycroft and Kash observe both the positive and limiting effects of consensus around Moore's Law as discussed in Chapter 3, underscoring the point that paradigms or trajectories imply path-dependence and possibly lock-in. Randall Isaac, IBM's Research Division Vice President of Systems, Technology, and Science, has discussed the future of silicon-based ICs, the basis of Moore's Law. He notes that the industry has recognized for 20 years the impending limitations of silicon and embarked on ambitious research programs in search of alternatives from gallium arsenide to Josephson junctions. He argues that today we are closer to reaching the supposed limits of silicon, and "ironically, there is virtually no major investment in alternative technologies." He concludes with a classic path-dependent observation reminiscent of Paul David's QWERTY keyboard story:

> Any potential replacement for silicon would need to supercede … the impressive economic base supporting silicon that is in place today. For example, a company using a new semiconductor would need to account for the incremental cost of improving silicon technology versus the non-incremental costs of creating an entirely new manufacturing tool base required for non-silicon technology production. In other words, it is highly unlikely that the present worldwide silicon infrastructure will be regenerated to support a silicon successor.[79]

He goes on to discuss that IBM has achieved recent breakthroughs in silicon research, further extending IC capability and thus, Moore's Law. Further, by noting the present "worldwide

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[77] Ibid., quotes and italics in original.
[78] Dosi. (1989), op. cit., 1129.
[79] Randall Isaac. "Viewpoint: Beyond Silicon...And Back Again" *IEEE Spectrum*, January 1997, 58.

silicon infrastructure," he lends more credence to the existence and influence of a silicon-based consensus paradigm.

Finally, Moore's Law and silicon-based technology both underpin the Roadmap, where a central planning assumption is an extension of the industry's historical productivity curve according to Moore's Law."[80] Further, 'semiconductor' has become synonymous with 'silicon' in the minds of industry technology planners:

> One underlying assumption of the "Semiconductor" Technology Roadmap is that it refers to mainstream silicon ... (CMOS) technology and does not include non-silicon technologies.[81]

For the first time, the 2001 ITRS (and expanded in the 2003 ITRS) addressed alternative "advanced non-classical CMOS structures" with an entire chapter entitled *Emerging Research Devices*,[82] however most of these are not expected to be available until the latter part of the present 15yr Roadmap horizon (2018). Nonetheless, through the Roadmap, the consensus paradigm of Moore's Law has been institutionalized within the technological community's (i.e., industry, suppliers, consortia, government, and others) research and development infrastructure.

The next section delves into the process of technological innovation, particularly within an evolutionary framework.

Technological Innovation

According to Hill (1979), the process of technological innovation involves the creation, design, production, first use, and diffusion of a new technological product, process, or system.[83] More broadly, innovation is concerned with ideas, practices, or objects that are perceived as new and introduced to a market or a community. The interest here is primarily in the innovation of

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[80] Semiconductor Industry Association, *The National Technology Roadmap for Semiconductors*, San Jose, CA, 1994, ix.
[81] W.J. Spencer and T.E. Seidel. "National Technology Roadmaps: The U.S. Semiconductor Experience," Austin, TX: Sematech, undated typescript (est. 1995), quotation in original.
[82] *The International Technology Roadmap for Semiconductors: 2001*, 177-195.
[83] Christopher T. Hill in Christopher T. Hill and James M. Utterback, *Technological Innovation for a Dynamic Economy*, New York: Pergamon Press, 1979, 2.

semiconductor technologies. However, innovative ideas and practices such as management systems or manufacturing processes may help drive and even define the technological artifact that is most often studied as the unit of analysis. For example, restructuring of the organization often occurs during the innovation process and continues to shape and be shaped by stages of technological innovation. Invention, development, and diffusion (commercial implementation) are the basic stages that comprise the process of innovation. Thus, innovation can be simply defined as the *process* of moving creative solutions to the market place.

As discussed in Chapter 3, one point that is increasingly more evident is that the process of technological innovation has become ever more complex. The factors contributing to innovation are wide and diverse, and include technical, social, economic, and political (public policy) factors. Kline and Rosenberg (1985) argue that the operating systems of concern in innovation are not purely technical in nature; they are rather strongly intertwined combinations of the social and the technical, or "sociotechnical systems" as a more useful descriptor to think about such institutions.[84] The authors expand on this more complete view:

> Models that depict innovation as a smooth, well-behaved linear process badly misspecify the nature and direction of the causal factors at work. Innovation is complex, uncertain, somewhat disorderly, and subject to changes of many sorts. Innovation is also difficult to measure and demands close coordination of adequate technical knowledge and excellent market judgment in order to satisfy economic, technological, and other types of constraints—all simultaneously. The process of innovation must be viewed as a series of changes in a complete system not only of hardware, but also of market environment, production facilities and knowledge, and the social contexts of the innovation organization.[85]

Parayil (1993) conceptualizes innovation as essentially a historical process that takes place within particular economic, political, and cultural contexts.[86] Thus to fully understand innovation, one must understand the role played by these contributing factors. In Layton's (1974) classic

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[84] Stephen J. Kline and Nathan Rosenberg, "An Overview of Innovation," in Ralph Landau and Nathan Rosenberg, eds., *The Positive Sum Strategy* (Washington, DC: National Academy Press, 1986), 278.
[85] Ibid., 275.
[86] Govindan Parayil, "Models of Technological Change: A Critical Review of Current Knowledge," *History and Technology*, 1993, Vol. 10, 121.

article, "Technology as Knowledge," he asserts the importance of understanding innovation within a social context:

> Innovation suggests consideration of the role of technology in social change. In either case, the ideas of technologists cannot be understood in isolation; they must be seen in the context of a community of technologists and of the relations of this community to other social agencies.[87]

Therefore, the innovation process is not, as a rule, the simple product of science (i.e., the search for truth) producing technology (i.e., practical tools that solve life's problems). Rather, the innovation of complex technologies has become more uncertain and disorderly. At the same time (and perhaps in response), innovation has also become more structured and organized around domains of knowledge, expertise, and economic resources. Another characteristic about innovation in today's complex world is that the operating systems of concern are no longer purely technical in nature; they are strongly intertwined combinations of the social and the technical, proving extremely difficult—if not impossible—to understand and model. As a result, the crafting of effective public policies to foster technological innovation has become high art.

A quick look at traditional explanations of innovation offers little insight anymore in today's complex environment. The popular post-WWII 'technology push', 'pipeline', or 'linear' model (i.e., research → development → production → marketing) as well as 'market pull' descriptions bound to the Schumpeterian heritage of the charismatic entrepreneur as the single, exogenous source of innovation are no longer satisfactory, especially in the innovation of semiconductor technologies.[88]

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[87] Edwin T. Layton, Jr., "Technology as Knowledge," *Technology and Culture*, Vol 15, No 1, January 1974, 38.

[88] Note that Schumpeter distinguished clearly between invention, innovation, and imitation (diffusion) as separate but related acts. His delineation between invention as the inventor's task and innovation as the entrepreneur's task is most evident in Joseph A. Schumpeter, *The Theory of Economic Development: An Inquiry into Profits, Capital, Credit, Interest, and the Business Cycle*, translated by Redvers Opie, New York: Oxford University Press, 1961 (originally published 1934), 88-89: "Economic leadership in particular must hence be distinguished from "invention." As long as they are not carried into practice, inventions are economically irrelevant. And to carry any improvement into effect [innovation] is a task entirely different from the invention of it, and a task, moreover, requiring entirely different kinds of aptitudes. Although entrepreneurs of course *may* be inventors just as they may be capitalists, they are inventors not by nature of their function but by coincidence and vice versa. Besides, the innovations which it is the function of

Most striking is the simplistic economists' view of innovation as a "black box" (Rosenberg, 1982) containing unknown components and processes. This view attempts to identify and measure the main inputs that enter and the outputs that emanate from the black box, largely neglecting the highly complex process through which certain inputs are transformed into certain outputs. Further, a myriad of factors contribute to the innovation process. These factors are both endogenous and exogenous and include the role of science, R&D, production processes, market forces, organizational learning and networks, and public policies among others. Also, the influence of standards in the form of technological paradigms, trajectories, and possible path dependencies and market 'lock-in' play a larger role in the increasingly organized innovation systems that occupy today's commercial environment. Therefore, more appropriate explanations must incorporate all of these factors to some degree implying that there are few, if any, generalizable 'models' of the innovation process. Today's innovation process is emergent and dynamic, involving tightly intertwined, complex networks of organizations that self-organize and co-evolve with the technology. Understanding of this process requires both broader and deeper investigation into the intimate relationships and feedback loops among all contributing factors (e.g., see Kline's "chain-linked" model, Figure 4-3). Finally, the process of innovation must be viewed within the context of a complete system of not only hardware, but also market environment, production facilities and knowledge, and the social contexts of the innovating organization(s). This requires an inter- or multi-disciplinary approach to understanding.

A better understanding of technological innovation is particularly useful since the pace of innovation is quickening in many technologies, most notably in semiconductors (e.g., microprocessor and DRAM chips) where a very rapid yet regular pace of innovation is characteristic. Since semiconductors are in such widespread use in modern consumer and industrial electronic products, this has spawned considerable rates of technological advances in these and related information technologies.

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entrepreneurs to carry out need not necessarily be any inventions at all. It is, therefore, not advisable, and it may be downright misleading, to stress the element of invention as much as many writers do."

Models of Technological Innovation

A rich literature has emerged over the past twenty-five years or so that examines the process of technological innovation. Some have labeled this field "Innovation Studies," which reaches across many disciplines including economics, sociology, history of technology, engineering, public policy, and others. It is beyond the scope of this study to review this entire literature, however a sampling of some of the more pertinent work is instructive. Thus, three authors'—an engineer (along with an economic historian co-author), an economist, and a physicist—interpretations of the innovation process will be presented as a representative sample of the prevailing approaches or explanatory models of technological innovation.

In an essay simply called "An Overview of Innovation" (1986), the late Steven Kline, Professor Emeritus of Science, Technology and Values and of Mechanical Engineering at Stanford University, spoke for many when he criticized the linear model as portraying the major activities of innovation "implicitly visualized as flowing smoothly down a one-way street, much as if they were the 'begats' of the Bible" (Figure 4-2).[89]

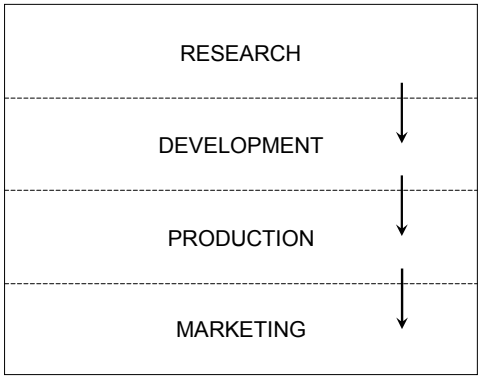

Figure 4-2. Kline/Rosenberg Linear Model of Innovation

Source: Stephen J. Kline and Nathan Rosenberg, "An Overview of Innovation," in Ralph Landau and Nathan Rosenberg (eds.), *The Positive Sum Strategy: Harnessing Technology for Economic Growth*, Washington, DC: National Academy Press, 1986, 286.

[89] Stephen J. Kline and Nathan Rosenberg, "An Overview of Innovation," in Ralph Landau and Nathan Rosenberg (eds.), *The Positive Sum Strategy: Harnessing Technology for Economic Growth*, Washington, DC: National Academy Press, 1986, 285-6.

The authors found several limitations with the linear model. For example, they pointed out that there were no feedback loops, which are inherent in the development process. Further, their view was that design, not science, was the central process of innovation. Their overall critique: "Thus, the notion that innovation is initiated by research is wrong most of the time."[90]

This assessment led the authors (Kline in particular) to propose the "chain-linked model" as shown in Figure 4-3. Although a central chain of innovation (CCOI) generally follows the direction of the linear model, the chain-linked model is a much richer portrayal of the innovation process. It features many enhancements including extensive incorporation of feedback loops, and perhaps most importantly, it reflects research (or scientific knowledge) as not the driver, but a common resource available throughout the innovation process. The authors conclude:

> In sum, the use of accumulated knowledge called modern science is essential to modern innovation; it is a necessary and often crucial part of technical innovation, but it is not usually the initiating step. It is rather employed at all points along the central-chain-of-innovation, as needed. It is only when this knowledge fails, from all known sources, that we resort to the much more costly and time-consuming process of mission-oriented research to solve the problems of a specific development task.[91]

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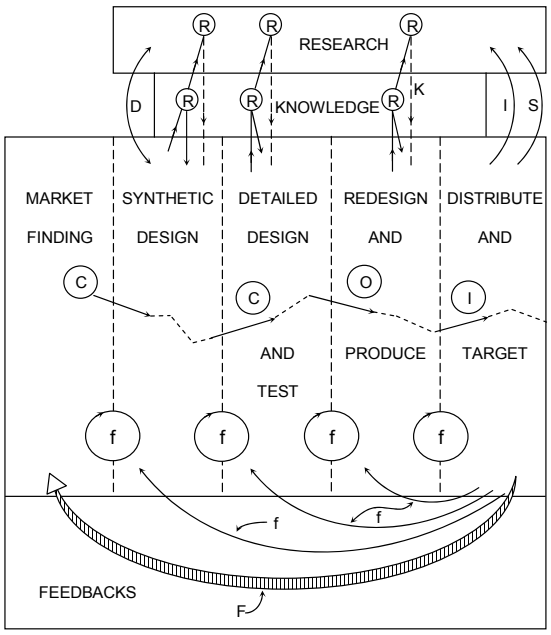
[90] Ibid., 288.
[91] Ibid., 291.



Chain-linked model showing flow paths of information and co-operation.
Symbols on arrows:
CCOI = central-chain-of innovation;
f = feedback loops;
F = particularly important feedback.

K-R: Links through knowledge to research and return paths. If problem solved at node K, link 3 to R not activated. Return from research (link 4) is problematic -- therefore dashed line.
D: Direct link to and from research from problems in invention and design.
I: Support of scientific research by instruments, machines, tools, and procedures of technology.
S: Support of research in sciences underlying product area to gain information directly and by monitoring outside work. The information obtained may apply anywhere along the chain.

Figure 4-3. Kline's Chain-Linked Model of Innovation

Source: Stephen J. Kline and Nathan Rosenberg, "An Overview of Innovation," in Ralph Landau and Nathan Rosenberg (eds.), *The Positive Sum Strategy: Harnessing Technology for Economic Growth*, Washington, DC: National Academy Press, 1986, 290.

In an essay on evolutionary economics, Norman Clark (1988), honorary professor of the Science Policy Research Unit (SPRU) at the University of Sussex, examined the role of technology in economic change and offered a similar contrasting view as Kline/Rosenberg. Clark

started with a version of the conventional "pipeline" model (Figure 4-4). Note that it is essentially the Kline/Rosenberg linear model, however knowledge flows are not solely uni-directional, except with respect to science (to and not from technology).

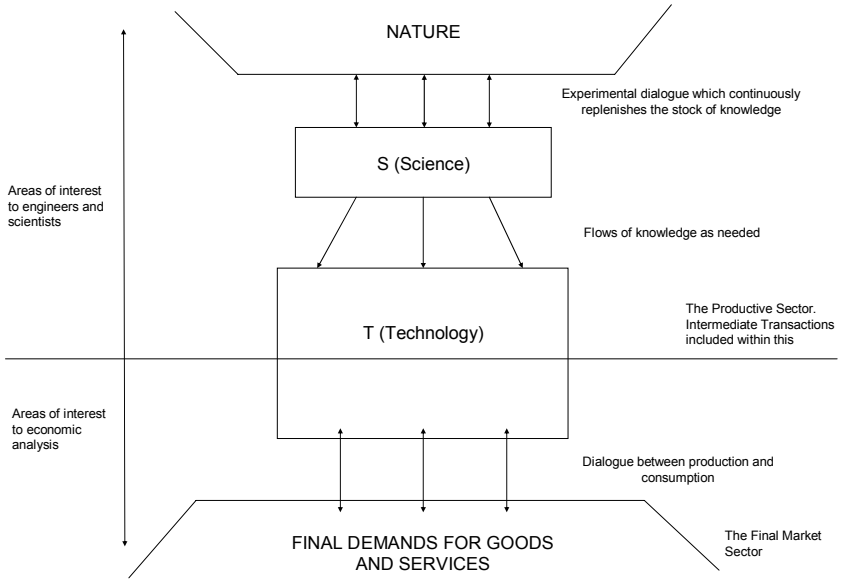


Figure 4-4. Clark's Pipeline Model

Source: Norman Clark, "Some New Approaches to Evolutionary Economics," *Journal of Economic Issues*, Vol. XXII, No. 2, June 1988, Figure 3, 525.

Like Kline and Rosenberg, Clark found limitations in the pipeline (linear) model and argued for a rather different metaphor as a more accurate depiction. He offered a stylized view of a set of relations that are at once both more complex and more continuous and referred to this as an 'interactive' model (Figure 4-5).

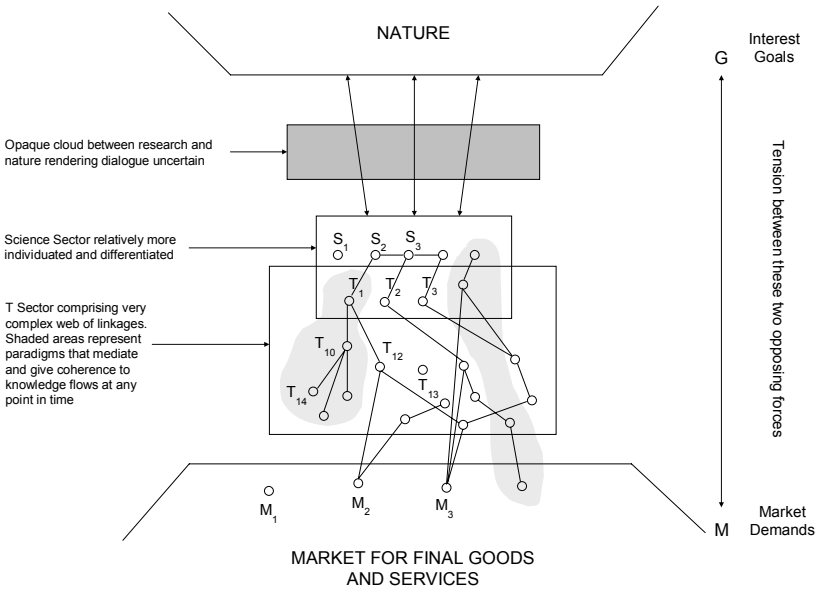


Figure 4-5. Clark's Interactive Model

Source: Norman Clark, "Some New Approaches to Evolutionary Economics," *Journal of Economic Issues*, Vol. XXII, No. 2, June 1988, Figure 4, 527.

Again, there are similarities between this interactive model and the chain-linked model. For example, knowledge flows are multi-directional and can traverse all major activities (Clark calls these sectors). However, there are significant differences. Most notable is the web of linkages (i.e., connections between numbered S, T, and M dots representing specific domains of knowledge). Moreover, Clark indicates that the "shaded areas represent paradigms that mediate and give coherence to knowledge flows at any point in time." Thus, the interactive model reveals actual as well as potential outcomes of the innovation process. The author speculates on the role of a technological paradigm—as previously discussed—within this model:

> A third point portrayed vividly in Figure 4 [4-5, the interactive model] is the complexity and uncertainty characteristic of relations between science and production. Indeed, so great are these that ways must be found to ensure an adequate rate of technical change, and the technological "paradigm" is precisely such a social device, since its heuristic

properties provide, as it were, a pathway of relative certainty in the midst of considerable ignorance.[92]

Finally, John Ziman, Emeritus Professor of Physics at the University of Bristol, offers perhaps the most extensive review of innovation models. In an essay on the strategic importance of technological innovation (1991), Ziman asks the question, "what sort of mental model of the whole process of technological innovation is required for strategic thinking in that field?" To answer this, the author reviews several models of innovation in a progressive fashion, beginning with the familiar linear model (Figure 4-6a)"which time's moving finger writes inexorably from left to right."[93]

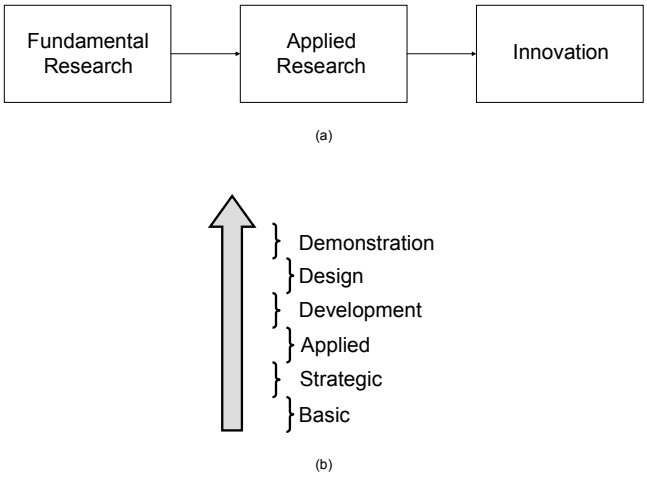


Figure 4-6. Two of Ziman's versions of the linear model

Source: John Ziman, "A Neural Net Model of Innovation," *Science and Public Policy*, Vol. 18, No. 1, February 1991, 66.

[92] Norman Clark, "Some New Approaches to Evolutionary Economics," *Journal of Economic Issues*, Vol. XXII, No. 2, June 1988, 526, quotes in original.
[93] John Ziman, "A Neural Net Model of Innovation," *Science and Public Policy*, Vol. 18, No. 1, February 191, 66.

He argues further: "The linear metaphor is so firmly entrenched in the language of public speeches, editorials, and official reports that we must assume that it relates to a widely shared mental model."[94] Like the other authors, he also questions whether such a simple and single model could ever fully explain the true nature of technological innovation.

Although he states that the linear model represents the innovation process "much too naively, as if it were carried out by a very simple sequential computer," Ziman defends the linear model arguing that it does approximate an abstract level of reality. He then uses this notion to describe a series of progressively more complex models. He begins by changing the direction of flow from the traditionally Western left to right movement to one where technology flows upward from a base of science (Figure 4-6b). Note that this is the reverse direction of the Kline/Rosenberg and Clark models.

The first enhancement he refers to as the 'cyclic' model (Figure 4-7a) which incorporates a multi-directional flow between market, discovery, technology, and science. He states: "the historical record reminds us … that the relationship between a scientific discovery and a technological invention is not always causative in that direction."[95] One limitation of the cyclic model is that it is still one-dimensional. In arguing for more dimensions to better incorporate the paths along which a variety of specific academic research findings actually get transferred and transformed into a range of specific industrial products, he suggests a more elaborate cyclic model "with, say, a chain of many stages which may be connected back and forth over several steps" reminiscent of the chain-linked model. He states:

> The mental image that this evokes is a very complex whole with many different interconnected elements. Whether concretely elaborated or abstractly simplified, it cannot be linear. Of mathematical necessity, this image must span a space of more than one dimension.[96]

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[94] Ibid.
[95] Ibid.
[96] Ibid., 67.

He then states that to keep the useful features of the linear model one may "unpack" each of the spectral regions along it into several more dimensions. He offers a metaphorical 'department store' model traversed by a vertical elevator. Although not shown here, the idea is that each floor or 'department' represents a social institution (e.g., universities and fundamental research institutes in the basement, national laboratories and Fraunhofer institutes on the ground floor, the central corporate laboratories of multinational firms at first floor level, and so on). In effect, the linear model is unpacked into a three-dimensional institutional space, where the 'linkages' represent normal social interactions such as transfers of information, or of goods. The elevator enables vertical movement between departments, one level at a time. From the department store model the author emphasizes the importance of cognitive space and offers a more refined 'knowledge domains' model (Figure 4-7b). In this rendering, the innovation process is unpacked into three planes labeled *ideas*, *techniques*, and *commodities* and stacked up in successive domains of scientific and technological knowledge. Again, the basic elements of the linear model remain intact.

The next step is to incorporate the linkages that exist not only within each plane of knowledge domain, but across separate domains (Figure 4-7c). For example, scientific ideas may be linked to techniques where they have contributed, and these techniques in turn may be linked to the commodities where they have been used. The author relates the resulting image as similar to the roots of a tree, stretching down into the domain of fundamental research, stating "For at least the past century, a 'broad-based cone of finely-divided roots' would be a more appropriate image of the cognitive linkages in technological innovation."[97]

He then points out that the cognitive elements of technological innovation are rapidly becoming more and more interconnected in every direction, including 'sideways' (Figure 4-7d). Quite disparate techniques are linked indirectly by the scientific ideas that they share, and that apparently quite different commodities rely on the same techniques. He states that these

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[97] Ibid., 72, quotes in original.

relationships are not simply causal, from the root-tips upwards. The ideas that are current in one scientific specialty are suddenly discovered to be enormously fruitful in another very distant area (e.g., photolithography for printing and for chip-making). Further, he offers biotechnology as a field where two unrelated techniques may be married to produce a commercially valuable technical process, without either having previously become commodities.

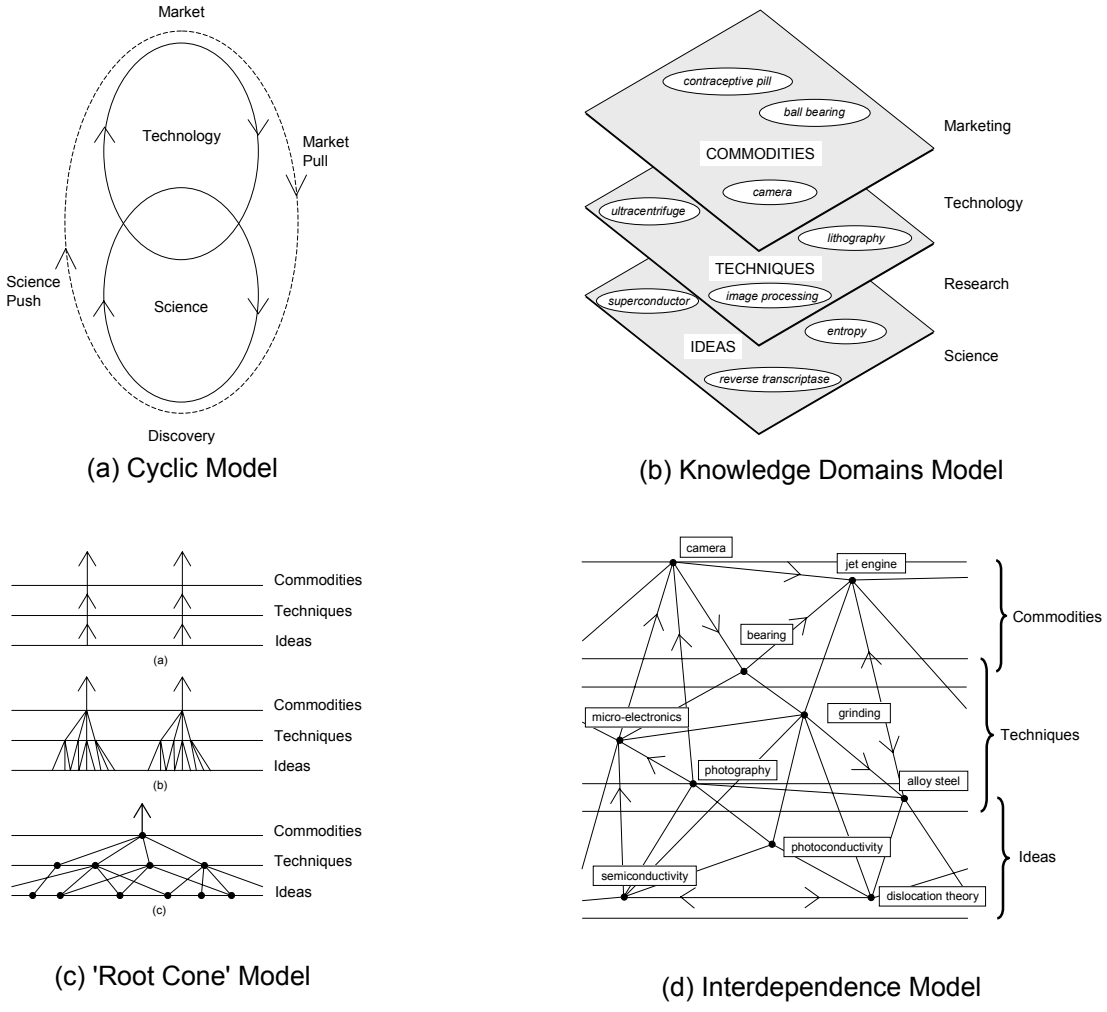

Figure 4-7. Ziman Innovation Models

Source: John Ziman, "A Neural Net Model of Innovation," *Science and Public Policy*, Vol. 18, No. 1, February 1991, 65-75.

Finally, Ziman suggests that a network structure, specifically a 'neural net' model, best describes the contemporary innovation process (Figure 4-8):

> Think of it, however, as a layered structure, connected both within each layer, and also from layer to layer, in both directions… Surely we have something here very like a neural net, of the kind to be found in a living brain. The nodes are neurons—nerve cells—connected both locally and over large distances by fibrous dendrites and axons. In some parts of the brain, such as the cerebral cortex, such networks often show a pronounced layer structure, corresponding in many cases to the successive transformations of incoming signals to achieve various physiological functions.[98]

He further states that this depiction, although much more sophisticated than the simple linear model described at the outset, produces similar results: "Metaphorically speaking, technological innovation is a process of this kind, where knowledge derived from the study of the natural world is transformed into the design of useful artifacts."[99]

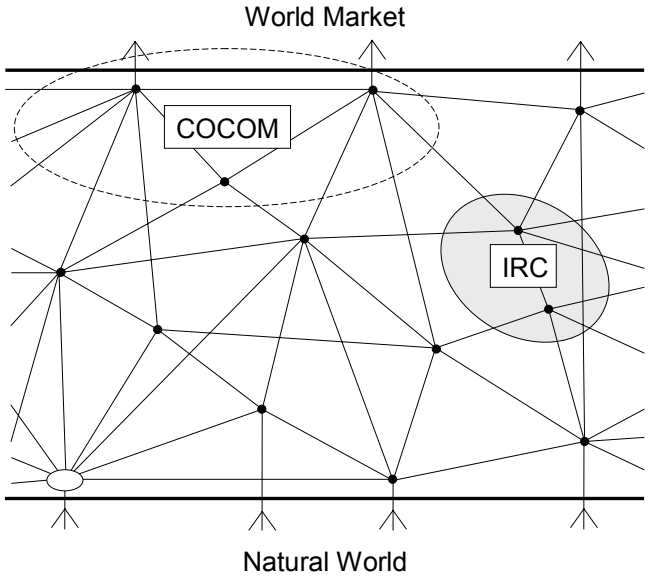

Figure 4-8. Ziman Neural Net Model

Source: John Ziman, "A Neural Net Model of Innovation," *Science and Public Policy*, Vol. 18, No. 1, February 1991, 74.

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[98] Ibid., 74.
[99] Ibid.

In summary, the three authors' models reviewed here represent a set of constructs from varying perspectives on the innovation process. While there are noticeable differences among the interpretations, there are a few clear underlying themes common among them: 1) innovation is much more complex than the linear/pipeline model implies, 2) multi-directional as well as multi-dimensional knowledge flows are essential to innovation, and 3) the process of innovation provides the critical linkages between innovating agents charged with producing specific outputs such as research programs or new products and the external forces (e.g., the market, society) requiring such outputs.

It is interesting to note that the review of these authors covered a snapshot period (1986-1991) that coincided with the crisis faced by many American industries, including especially semiconductors, in international competitiveness. It was during this time that notions such as *industrial competitiveness*, *critical technologies*, and similar descriptors helped foster a closer examination of the process of innovation. Much of this research has since been incorporated into contemporary innovation practices. The semiconductor industry, along with the development of the Roadmap in particular, provides an excellent example of this. Furthermore, the technology roadmapping practices that emerged in the 1990s, as discussed in Chapter 2, seem to pattern closely the innovation models that preceded them. This possible relationship is beyond the scope of this study, nonetheless it is worth noting for possible future research.

Before moving on, two more models of innovation will be presented briefly. They may be treated, at least chronologically, as "bookends" to the previous three authors' models. Both interpretations are important to this study. The first of these two is the Abernathy-Utterback patterns of innovation model previously mentioned. This model appeared in several publications in the 1970s and early 1980s (Figure 4-9) and is one of several from the product life-cycle tradition (S-curve models will be discussed in more detail shortly). The importance of this particular model is the role that a *dominant design* plays in shifting the emphasis of innovation from product to process. It will be shown that the semiconductor industry has generally followed

this model, while the Roadmap has played an important role in extending the technology life-cycle.

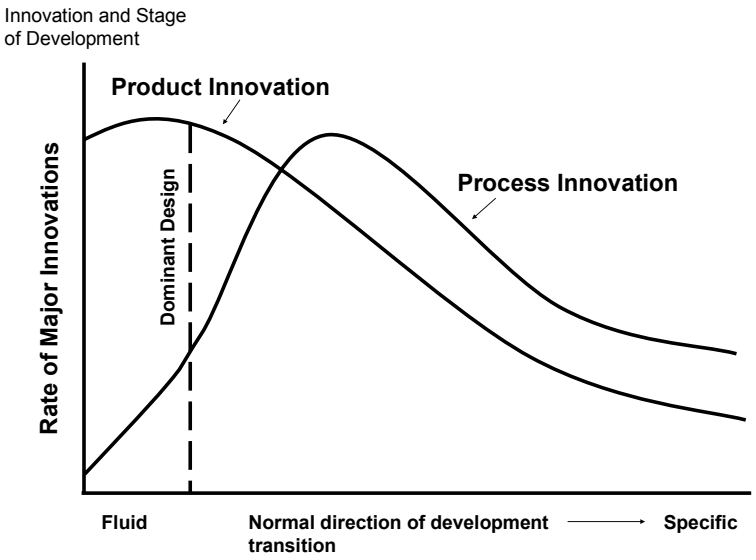

Figure 4-9. Abernathy-Utterback Patterns of Innovation Model

Source: William J. Abernathy (James M. Utterback co-author), "A General Model: Innovation and Process Change in a Productive Unit," Chapter 4 in *The Productivity Dilemma: Roadblock to Innovation in the Automobile Industry*, Baltimore: The Johns Hopkins University Press, 1978, 72.

According to Abernathy and Utterback, as a unit moves toward large-scale production, the goals of its innovations change from ill-defined and uncertain targets to well-articulated design objectives. In the early stages there is a proliferation of product performance requirements and design criteria which frequently cannot be stated quantitatively, and their relative importance or ranking may be quite unstable. The stimulus for innovation changes as a unit matures. In the initial fluid stage, market needs are ill-defined and can be stated only with broad uncertainty; and the relevant technologies are as yet little explored. As the technology develops, however, uncertainty about markets and appropriate targets is reduced, and larger research and development investments are justified. At some point before the increasing specialization of the

unit makes the cost of implementing technological innovations prohibitively high and before increasing cost competition erodes profits with which to fund large indirect expenses, the benefits of research and development efforts would reach a maximum. Technological opportunities for improvements and additions to existing product lines will then be clear, and a strong commitment to research and development will be characteristic of productive units in the middle stages of development. Such firms will be seen as "science based" because they invest heavily in formal research and engineering departments, with emphasis on process innovation and product differentiation through functional improvements.[100]

The other model is one taken from a plethora of new approaches to innovation emerging in the 1990s in new fields called the *Management of Technology* (MOT), *Innovation Management* (IM), and similar descriptors (Figure 4-10). This particular model reflects the more contemporary thinking about innovation as a more-or-less on-going process that connects technology endogenous to a firm with exogenous market requirements. This depiction reveals many aspects of the aforementioned models, but with even greater specificity. It will be shown that the roadmapping process has become an integral management tool to help innovators operationalize models such as these. For example, one popular method of innovation management employed by many large companies is called the "stage gate process." Each major activity along the path of innovation (e.g., conceptual design, prototype, full-scale development) is considered a stage and innovators must sequentially pass through "gates" at each stage by meeting established criteria such as return on investment before proceeding to the next stage. Given the increasingly competitive environment that firms and entire industries face today, optimal usage of financial, capital, and human resources are best allocated through methods such as these while still remaining innovative in a fast-changing market.

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[100] Abernathy and Utterback, op. cit., 44-5.

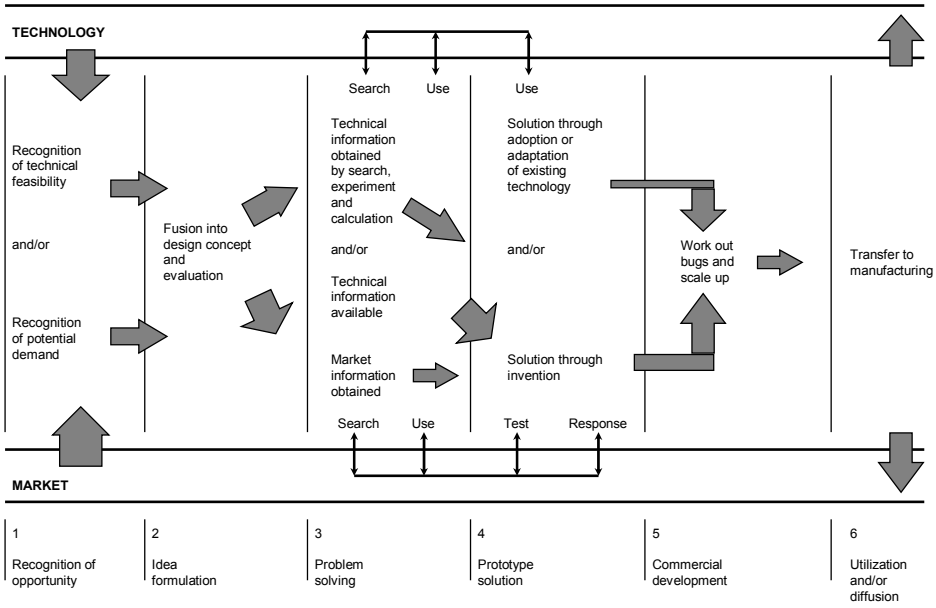

Figure 4-10. Innovation as Process

Source: K. Debackere, K.U. Leuven, "Innovation management: process, models, organization," (PowerPoint presentation, Slide 4, created August 6, 1999)

The next section explores one particular model of explaining technological innovation that borrows heavily from the tradition of evolutionary theory as it pertains specifically to the semiconductor industry and the Roadmap.

Rycroft/Kash Innovation Patterns Framework

Chapter 10 of *The Complexity Challenge* thoroughly presents a conceptual framework of technological innovation patterns that builds upon earlier work by one of the authors (e.g., Kash, 1989). The innovation patterns framework offers valuable insight into a variety of behaviors involved in today's complex innovation environment.

Rycroft and Kash examine the increasing role of complexity in the process of technological innovation. They emphasize that technological innovation comes about through adaptations of

both technology and the innovation network. To help explain the innovation of semiconductor technology, the Rycroft/Kash framework of innovation patterns is described.[101] Innovation patterns are useful conceptual references that help describe the origin and development of complex technologies. The learning necessary for the innovation of complex technologies requires organizational *networks* that involve multiple firms and often other participants (e.g., suppliers, universities, government agencies or laboratories). Strategies and policies that successfully facilitate innovation must reflect the fact that technologies and networks *co-evolve*. The paths traced by co-evolving technologies and networks are labeled *trajectories*. Three distinct innovation patterns are evident when trajectories are used to analyze the co-evolution of technologies and networks: *normal*, *transition*, and *transformation.* The three patterns and their relationships are shown in Figure 4-11.

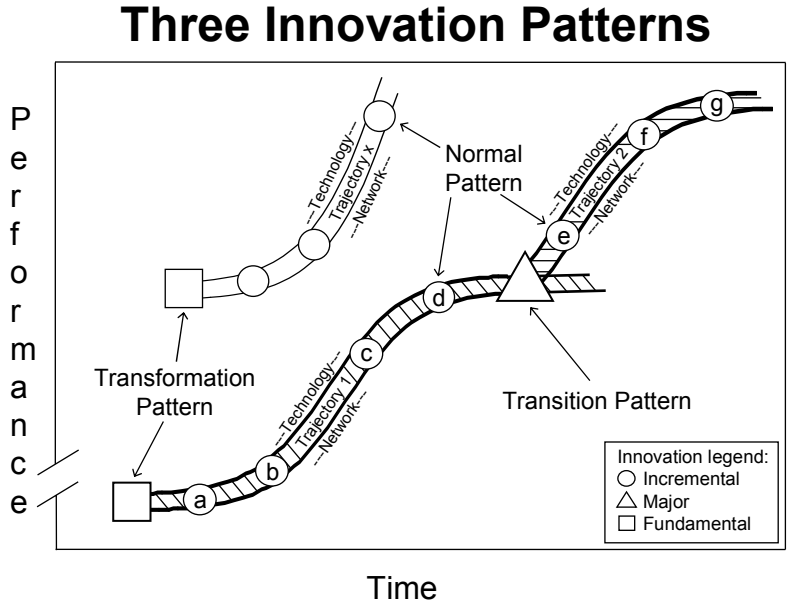

Figure 4-11. Three Innovation Patterns

Source: Rycroft and Kash, *The Complexity Challenge*, 1999.

[101] Adapted from Rycroft and Kash, 1999, op. cit.

The box symbol at the lower left of Figure 4-11 illustrates the fundamental innovations that characterize the transformation pattern. Innovations in a transformation pattern produce dramatically different technologies; they have fundamentally different characteristics than other technologies. A transforming innovation launches a trajectory, a co-evolving technology and network that then goes through the incremental innovations associated with the normal pattern. Once established, a transformation pattern settles into a normal pattern as illustrated in Figure 4-11 by the incremental innovations at points "a" through "d."

For complex technologies, the normal pattern is at some point replaced by a transition pattern, illustrated in Figure 4-11 by the triangle symbol. The transition pattern involves an innovation that produces a major change and improvement in the technology. Like the transformation pattern, a transition launches a new trajectory and then settles into the normal pattern, illustrated in Figure 4-11 by the incremental innovations at points "e" through "g."

Pattern Characteristics

The normal pattern, consistent with incremental innovations, is distinguished by the existence of a relatively stable network and a technology that has the same basic design before and after an innovation. In contrast, both the transition and transformation patterns, consistent with radical, disruptive, or revolutionary innovations, are associated with establishing new technology designs and networks. The new technologies may result from either major modifications in established technologies (i.e., transition) or from the creation of fundamentally new designs (i.e., transformation). Similarly, new networks may have either the same participant organizations or new ones, but they always include new knowledge, core capabilities, and complementary assets.

Most historical studies of innovation are treated in this order (i.e., starting from stability or a normal pattern to instability of either the transition or transformation variety). Rycroft and Kash also present the innovation patterns in this order: normal, transition, and transformation. They

further argue that following completion of either transition or transformation patterns, the innovation process migrates back to a normal pattern.

While semiconductor innovations follow this general order, in this case the order will be reversed so that the normal pattern *ends* the process. The reason for this is to emphasize the incremental nature that so dominates semiconductor innovations as evidenced by institutions like Moore's Law and the Roadmap.

The Transformation Pattern

The transformation pattern is the most chaotic of the three. Its innovations involve fundamental changes in technology and the creation of new networks. In this pattern major surprises and discontinuities are frequently encountered, and everything is subject to change. Thus, it is useful to think of transformational innovations as doing more than overcoming existing boundary constraints. Fundamental innovations establish previously unavailable technology paths.

Transformational innovations require creating new core capabilities. This often involves merging previously existing core capabilities, but sometimes it means creating them from whole cloth. In the arena of complex technologies, commercial opportunities seldom flow directly and immediately from scientific breakthroughs. Thus, the identification and development of entirely new core capabilities is a risky trial-and-error process. The learning critical to transformational innovations may be unrelated to the past learning of a network or company. Learning boundaries expand and become blurred. Thus, it is essential within this pattern that firms and networks learn to 'be at home anywhere'. No potential source of usable knowledge can be ruled out. Success is usually associated with a general openness to redefining organizational strategy and structure, as well as existing routines and decision-making procedures. For any particular firm or other organization, undertaking such broad learning may require memberships in multiple networks cutting across different industries, sectors, and economies.

The Transition Pattern

Innovations that occur within the transition pattern create new technology designs and networks as a result of major changes in what previously existed. Transitional innovations commonly deliver major advances in performance and qualitative changes in design by modifying established technologies in ways that overcome previously constraining boundary conditions. This often happens when a new subsystem is integrated into the complex technology. When transitional innovations occur, networks face significant uncertainty about the design characteristics of the technology and about what the innovation will cost and when it will take place. Nonetheless, transitional innovations can usually rely—at least in part—on a reservoir of knowledge that has been accumulated while carrying out the incremental innovations associated with previous trajectories. Transitions may be generated by problems, opportunities, or a combination of both. When impending transitions are widely anticipated, there are substantial incentives for previously competing networks to cooperate. The great uncertainty associated with transitions is a powerful inducement to establish strategic alliances and other forms of cooperation. As part of the transition to a new trajectory, even the most entrenched competitor networks are increasingly engaging in collaborative activities. One factor that encourages cooperation is the belief that limiting the number of transition pathways through the use of voluntary standards setting has advantages for all the networks involved.

Networks that carry out transitions become new networks because they must integrate new core capabilities to carry out the innovation. The most common occurrence is to integrate established core capabilities with core capabilities developed in other sectors. Because of the benefits of rapid innovation and because of the need to use significant amounts of tacit knowledge, new core capabilities are increasingly being accessed by adding new members to the network. That is because tacit knowledge takes too long to develop internally.

The Normal Pattern

The greatest profits from complex technologies are usually produced within the normal pattern. Specifically, it is the ability to incrementally innovate ahead of or in parallel with competitors that produce success in the arena of complex technologies. The normal pattern is characterized by continuity. Incremental innovations occur within a network's current problem-solving model. Within the normal pattern, high levels of confidence exist regarding what the performance characteristics of the next increment will be, what problems demand priority, and what procedures should be followed in solving them. The dominant short-term uncertainties are about how long the problem-solving process will take and how much it will cost. Company and network strategies and structures are usually modified in small steps as each incremental technological advance takes place. In the normal pattern, as technologies evolve along an established trajectory, network core capabilities tend to become more fixed. These capabilities commonly include increasing mastery of systems integration and architectural knowledge, and thus the growing capability to synthesize previously separate knowledge and complementary assets.

Organizational learning in the normal pattern is predominantly internal to the network and normally becomes more focused with each incremental advance. As network routines become well-developed, learning becomes ever more dependent upon what has been done in the past. Thus, as problems emerge, established networks know where to go for solutions. This makes problem-solving a less-risky process than it is when more wide-ranging exploratory learning is required.

Application to Semiconductor Technology

Braun & Macdonald (1982) reinforce the importance of accumulated learning in their assessment of semiconductor innovation:

> There are several special features to the innovation which we call semiconductor electronics. First of all, it is not really a single innovation at all, but consists of a long series of linked innovations.[102]

While this view is true in a broad sense, there are some notable points throughout the history of semiconductors that can be fitted within the Rycroft/Kash framework. The *transformation pattern* occurred initially with the discovery and early development of the transistor in the late 1940s and early 1950s at Bell Laboratories. The transistor, truly an innovation based on science, was a fundamentally different technology than the then-dominant design, the receiving/vacuum tube (valve) used for amplification, switching, and other electronics functions. The promise of 'solid-state' components afforded the electronics industry tremendous advantages in performance, reliability, power usage, and most importantly size. Further, it was not just the technology that was different, but an entirely new organizational network began to emerge to exploit the new transistor technology. For example, a geophysical company involved in oil well services (Texas Instruments) was the first to innovate a transistor made from silicon (Bell Labs' first transistors used germanium as a substrate material). Silicon would ultimately become the substrate of choice by semiconductor manufacturers.

In the context of this study, it was more accurately the invention and commercialization of the integrated circuit (IC)[103] almost a decade later that launched the fledgling semiconductor industry along a distinct technological trajectory. By connecting or *integrating* discreet components (i.e., transistors, diodes, resistors, and other components) *on the same substrate* it was now possible to increase circuit functionality to a level only limited by the ability to integrate. The development of planar process technology by a new division of an aerial survey company (Fairchild) made the manufacture of the IC possible and helped to guide the trajectory in a particular direction. Both innovations (IC and planar process) combined in a manner that would be considered within the *transition pattern*. The IC was a different kind of invention than the transistor. Whereas the transistor was borne from science, the IC involved little (if any) science. Instead, existing

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[102] Braun & Macdonald, op. cit. 1.
[103] Texas Instruments and Fairchild Semiconductors share the IC patent (see Chapter 6).

technologies and organizations combined knowledge, skills, and abilities from established innovation networks to launch the new trajectory where new capabilities and networks would form and become part of the innovation system.

Since the 1960s innovations have followed the *normal pattern*, which is characterized by 'bit-by-bit' incremental innovations, thus movement of the technology along the locked-in trajectory. Braun & Macdonald's earlier "long series of linked innovations" definition better describes the normal pattern. Within this pattern, a number of very significant advances have occurred including MOS (then CMOS) technology; DRAM, microprocessor, SoC, and other product types; step-and-repeat photolithography; new materials such as copper interconnects just to name a few. However, all have advanced the bulk planar CMOS device towards ever greater density, performance, and reduced unit cost characteristics. The consensus paradigm of Moore's Law captures the regularity of the industry's ability to perpetually innovate. Research consortia such as the SRC and Sematech in the U.S., but also Selete and ASET in Japan, IMEC in Europe, among others have emerged as key participants in the industry's innovation system. Interestingly, most of these organizations had started to solely support domestic industries (e.g., SRC and Sematech), but have since become international organizations. This adaptation reflects the increased globalization of semiconductor technology, markets, and innovation network. The Roadmap, in fact, followed a similar route and is another manifestation of this behavior. As stated previously, Moore's Law and the Roadmap are like two sides of the same coin within the industry's innovation system. Together, they serve to reinforce the normal innovation pattern. Figure 4-12 summarizes the three innovation patterns relative to semiconductor technology.

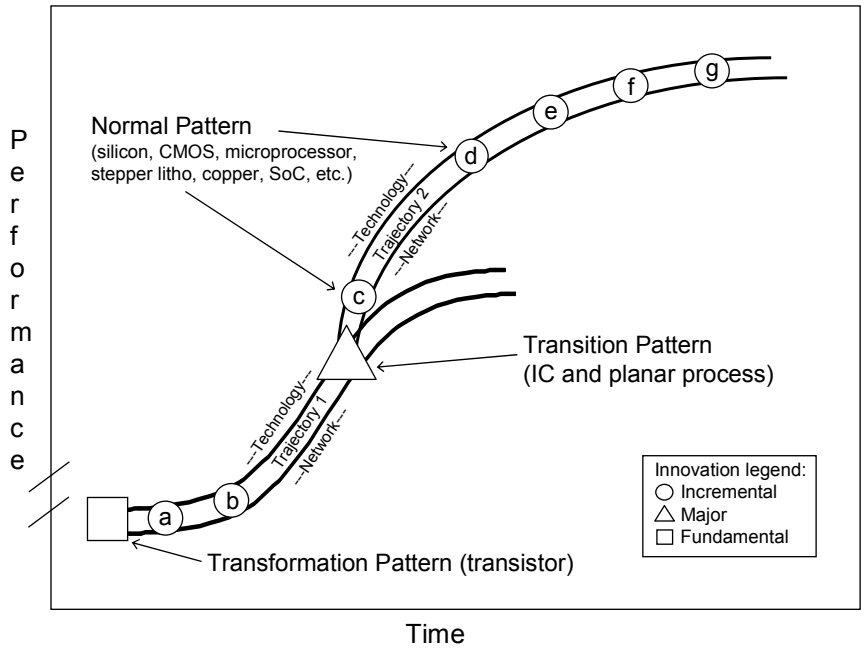

Figure 4-12. Three Semiconductor Innovation Patterns

At the same time it is widely acknowledged that the bulk planar CMOS device faces technological and economic limits within the window of the current Roadmap (next 15 years). The U.S. industry has responded by establishing five research focus centers at universities to address 'beyond the Roadmap' or 'post-CMOS' challenges (see Chapter 12). Further, as previously mentioned the *2003 ITRS* contains an entire chapter called *Emerging Research Devices* that explores novel structures and materials in anticipating a so-called "red brick wall" that marks the end of traditional productivity gains from advances in bulk planar CMOS devices.[104] Exactly which route the industry chooses to take will determine whether future innovations will follow the transition (major change) or transformation (fundamental change) pattern. Note that the focus center innovation networks charged with this task are separate and apart from the current

[104] Red-colored blocks in the Roadmap indicate "Manufacturable Solutions are NOT Known." Since many red-colored blocks now populate the Roadmap with a distinct concentration appearing by as early as 2007, the phrase "red brick wall" was coined as a metaphorical way of describing the impending challenges facing the semiconductor innovation community.

industry innovation system. Given that the lead time to commercialization of much of this research is probably a decade away, the industry will continue to employ the normal pattern using the Roadmap as its guide.

The next section considers the previous discussion on evolutionary theory and attempts to advance a theory offered by this author that better describes the unique nature of technological innovation within the semiconductor industry.

Performance Possibilities Frontier of Semiconductors

Continuing the discussion from Chapter 3 on the 'limits' of semiconductor technology, this section revisits these so-called limits and offers a theoretical explanation for why the industry has and continues to extend these technological limits, thus perpetuate Moore's Law. The question that has dogged the industry for decades as one of the great historical debates in the industry has been, "When will Moore's Law end?" Early predictions of its demise date back to the late 1970s and early 1980s, but none have come to pass as semiconductor devices have continued to advance, now boasting billion-fold improvements in circuit density covering four decades. Thus Moore's Law lives and will continue to do so for the foreseeable future (conservatively estimated as at least another 10 years). Then what are the ultimate limits of technological advance? Every time a 'physical' limit is set it gets broken. The reasons are complex, but suffice it to say that knowledge advance has much to do with it. Henderson's (1995) treatment of the 'imaginary' limits in photolithography is instructive. She argues that so-called technological limits may be as much socially constructed as they are natural. Almost two decades of roadmapping have produced similar results. Why? Basically it is the problem-solving (engineering) nature of advancing semiconductor—or really any—technology. Vincenti (1990) describes in detail the creation, accumulation, and dissemination of engineering knowledge. One of the striking points is the on-going 'day-in, day-out' process of the engineering enterprise. As argued here, the normal act of discovery is not the 'eureka' kind of event that is popularized (sometimes romanticized) in the

literature, but a continual task of solving mostly small, yet important, technical challenges. According to Moore, R&D is all about solving problems:

> We thrive on problems and like to find them so we can solve them. That's an old R&D view—there's nothing to do unless you've got a problem.[105]

Hwa-Nien Yu, noted research scientist at IBM, elaborates further that the spirit of R&D also entails a competitive mentality with regard to so-called limits:

> If someone says 'that's the limit' then maybe I can break that. That's really the spirit of R&D to push in that direction. Eventually it will hit the limit someplace, right? But before that, everybody thinks that way so I can compete, I can stay on top. That's a mentality.[106]

The result of this problem-solving is two-fold: (1) advance of capability as problems are solved, and (2) increased knowledge base for use in solving future problems. Thus, so-called limits represent whatever state-of-knowledge exists at any point. Certainly other considerations such as economics come into play, but the technical dimension of these limits is, in a sense, socially-constructed by the current knowledge of engineers and other technologists charged with advancing the technology.

Again then, what are the limits of technological advance in semiconductors? Perhaps science will ultimately tell us, but in the meantime the technology itself is the best teacher through daily engineering practice. There is current debate on the correct stage of the industry life cycle. The industry shows many signs of maturity, yet the technology continues to advance exponentially (which would argue for growth stage). For our purposes the industry is still growing as new applications are found almost daily. The technology continues to advance—assisted by an industry roadmap—thus capability or performance will continue its ever-increasing process. To better understand this particular behavior we will examine the applicability of the "S-shaped" curve used by many scholars in explaining the history of technologies, including semiconductors.

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[105] Gordon Moore, quoted in John Morkes, "Success Likes to Follow Intel's Gordon Moore," (interview with Gordon Moore) *R&D Magazine*, July 1993, 34.
[106] Hwa-Nien Yu, personal interview, July 18, 2000.

Utility of S-Curves

Several models of technological advance (and diffusion) have been offered. The logistic or "S" curve has been a popular method of portraying a three-phased pattern of a slow start (Phase 1) followed by exponential growth (Phase 2) and ending or leveling-off as the technology matures and reaches its 'limits' (Phase 3). Klein (1977) used S-curves to help explain economic behavior as 'dynamic' versus the traditional static view generally accepted within classical economic theory. About a decade later, Foster (1986) argued that the S-curve revealed both great competitive potential and vulnerability. Market leaders could be left at a disadvantage to a new entrant or 'attacker' who could exploit his position. Several authors, particularly in the strategic management tradition, followed Foster's reasoning, offering all kinds of additional insight and 'advice'. Christensen and Rosenbloom (1995) and Christensen (1997) argued that following too closely to one's S-curve could eventually prove fatal as discontinuities or new S-curves are launched, usually from outside of familiar 'value networks', disrupting the established technological trajectory. As previously illustrated, Rycroft and Kash (1999) use S-curves to demonstrate emerging patterns of innovation, distinguishing between normal, transitional, and transformational patterns.

As already mentioned, several authors have used semiconductor (or microelectronics)[107] technology as a contemporary example that displays S-curve behavior (Meindl, 1987; Foster, 1986). While semiconductor technical advance may seem to exhibit S-curve behavior, it is argued that any attempt to 'fit' this technology to a life-cycle model such as an S-curve is premature because of the unique ability of the semiconductor community to continue to push the so-called limits of this technology. Thus, in this particular case the S-curve method, or rather a *singular* S-curve, is not very instructive. In Chapter 6 the history of the technology (and industry) will be examined in more depth, but for now the proposition offered here is that there is a unique

[107] The terms *chips*, *semiconductors*, and *microelectronics* are used interchangeably throughout this document.

regularity of technical progress—described as Moore's Law (see chapter 8)—that has enabled the industry to continue its rapid climb up the growth segment of the S-curve. It is argued that semiconductor technology has been able to 'defy' the diminishing returns (second half) portion of the S-curve—at least so far. This has occurred with the regularity of Moore's Law through the help of a focusing device like the industry Roadmap. There is no doubt that progress will slow (there are already signs that this has begun) but one of the advantages of having a more far-sighted industrial view from tools like Moore's Law and the Roadmap is that the future can be anticipated with some degree of certainty. Ironically, this has yet to happen as the 'limits' to growth keep getting pushed further as has been discussed. Thus, proposed is a *series of shifting* S-curves model for this industry as a more useful means for analysis.

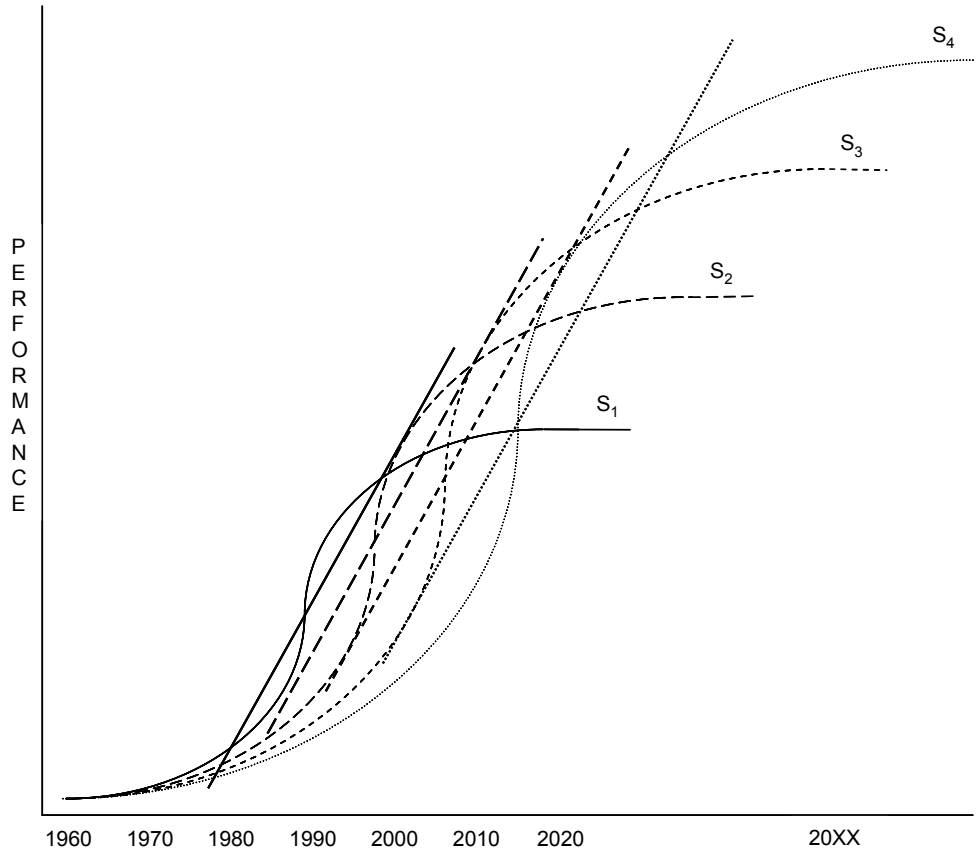

Figure 4-13. Series of Shifting S-Curves of Semiconductor Technology

Figure 4-13 shows a series of four S-curves (S_1 through S_4). S_1 represents the 'first' observation of this kind of behavior. One could argue that Gordon Moore's 1965 forecast underpins this initial curve (although he really didn't speak to the diminishing portion of the curve, see Chapter 8). Over time Moore's initial forecast was validated and adjusted reflecting new knowledge, pushing the performance frontier upward to S_2. As previously mentioned, continual upward revisions of the limits could be shown as S_3, S_4, and continuing. This pattern of an expanding performance frontier has become an industry trademark similar to other technologies in other industries such as aircraft (Constant, 1980, 1973). In terms of this study, the problem with most of these *ex post* examinations of technologies is that 'progress' is treated in an evolutionary way along some form of performance curve, often where S-curve behavior is demonstrated. Authors even argue—particularly when using the 'old' technology as a basis for a revolutionary or discontinuous 'new' technology—that the competitive threat from a replacement technology forces greater levels of performance out of the existing technology that is targeted to be replaced. Stories abound in the economic history, history and sociology of technology, philosophy of science, and related traditions. What is *not* considered in most of these analyses is the process that goes on 'in the meantime'. In other words, the never-ending 'day-in, day-out' pattern of sustained, incremental innovation. With his experience and keen insight as a practicing engineer, Vincenti (1990:206) as scholar makes this point:

> Even when resolution of a new problem is achieved, the problem does not disappear—after our stories were finished, propellers and airfoils still had to be selected for particular aircraft and flush-riveted joints proportioned and detailed. Developments and refinements continue.

In contrasting innovative imitation practices between Japan and the U.S. (during a time when the Japanese competitive threat loomed large), Rosenberg and Steinmueller (1988) best articulate the significant and yet mostly invisible role of incremental innovation, or *development* as they refer to it below. Having respectively chaired and authored a Ph.D. thesis on the microeconomics of the semiconductor industry, the authors offer semiconductors as a supporting case:

> R&D is, in fact, overwhelmingly D. Yet we know more about the 12 percent of R&D that constitutes basic research than of the 68 percent that constitutes development… American thinking about the innovation process has focused excessively upon the earliest stages—the kinds of new products or technologies that occasionally emerge out of basic research, the creative leaps that sometimes establish entirely new product lines, the activities of the "upstream" inventor or scientist rather than the "downstream" engineer. American discussions of technical change are more likely to be presented in terms of major innovations and pioneering firms, rather than in terms of the success of particular sectors or firms at catching up and overtaking other organizations through sustained effort and small improvements. In this respect, the dominant view of the innovative process is still overly Schumpetarian, in its preoccupation with discontinuities and creative destruction, and its neglect of the cumulative power of numerous small, incremental changes…
>
> Their [minor modifications and small improvements] cumulative effects may, however, be immense, as when the semiconductor industry moves, through a multitude of small steps, from a handful of transistors on a chip to a million such transistors…
>
> A continual stream of small improvements is often the essence of success in the competitive process. In industries such as those that currently account for the bulk of Japanese exports to the U.S., development is a never-ending activity. They are not, from some points of view, very exciting activities. They are activities that do not win Nobel Prizes; nor, for the most part, do they even win recognition at the Patent Office. This low visibility accounts for the very limited awareness of their economic importance.[108]

Sahal (1981) also reminds us that the history of technology reveals numerous examples of the significance of incremental innovations (see caption in Chapter 3). Returning to Figure 4-13, there is a series of parallel, upward-sloping lines associated with the series of S-curves. These are meant to represent the exponential growth stage of the curves (Phase 2). They are a conceptual rendering only, but sufficient to argue both the reality and theoretical hypotheses here. Note that the parallel lines (or curves) shift upward and to the right consistent with the series of S-curve shifts. It is this pattern of continual expansion of performance limits that is of concern. Simply labeling this process as 'dynamic' (Klein, 1977) by ascending points on a single, static S-curve fails to capture the real innovation pattern at work.

This study is about technical change and thus must consider discontinuities, radical or fundamental innovations—Schumpeterian technical change if you will. However, consistent with the comments above, revolutionary change is *not* the major concern here. Instead, the focus of this study is the steady, cumulative, incremental, 'normal' technical advance so characteristic of

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[108] Nathan Rosenberg and W. Edward Steinmueller, "Why are Americans Such Poor Imitators?" *AEA Papers and Proceedings*, May 1988, 230-1.

semiconductor technology. Several authors—with empirical data—have validated this exponential trend (Moore, 1965, 1975; Noyce, 1977; Dosi, 1984; Meindl, 1987; Schaller, 1997; SIA Roadmaps, 1992, 1994, 1997, 1999, 2001). Thus, most would agree that this trend continues to hold (see Chapter 8 for more detail). Further, insight into the 'stretching' S-curves behavior while semiconductor technology still exhibits exponential advance is helpful in explaining this unique innovation pattern.

In fact, Rosenberg (1976) argues that the Schumpeterian heritage has so shaped our thinking that it provides a bias which leads to the neglect of the analysis of small improvements.[109] The author further elaborates that the process of innovation was never really part of Schumpeter's analysis:

> Within the sequence of (1) invention, (2) innovation, and (3) imitation, Schumpeter's theory had the result of focusing attention upon the circumstances surrounding and influencing the act of innovation. Inventive activity stood as an exogenous factor outside of his framework… inventive activity itself is never examined as a continuing activity whose nature, timing, and special problems are relevant to the subsequent Schumpeterian stages of innovation and imitation. It is an activity carried on offstage and out of sight. Inventions come onto the Schumpeterian stage already fully grown, and not as objects or processes the development of which is a matter of explicit interest; nor are subsequent improvements or modifications of the invention typically treated as significant.[110]

It is noteworthy that semiconductor fabrication has not fundamentally changed in the four and a half decades since the planar process was introduced in 1959. Today's process that produces billion-circuit chips is one—if not the best—contemporary example of the immense benefits of incremental innovation. Given the size of the industry along with the broad and diverse supply chain supporting and supported by it, one could easily argue that this well-established pattern of incremental innovation has contributed trillions (plural) of dollars into the world economy. Within the semiconductor community Moore's Law is seen as a kind of 'meta law' that literally dictates incremental innovation as the means to ensuring its validity. Moreover, the Roadmap process helps guarantee that the historical rate of progress will continue well into the future.

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[109] Nathan Rosenberg, *Perspectives on Technology*, Cambridge: Cambridge University Press, 1976, 66.
[110] Ibid., 67.

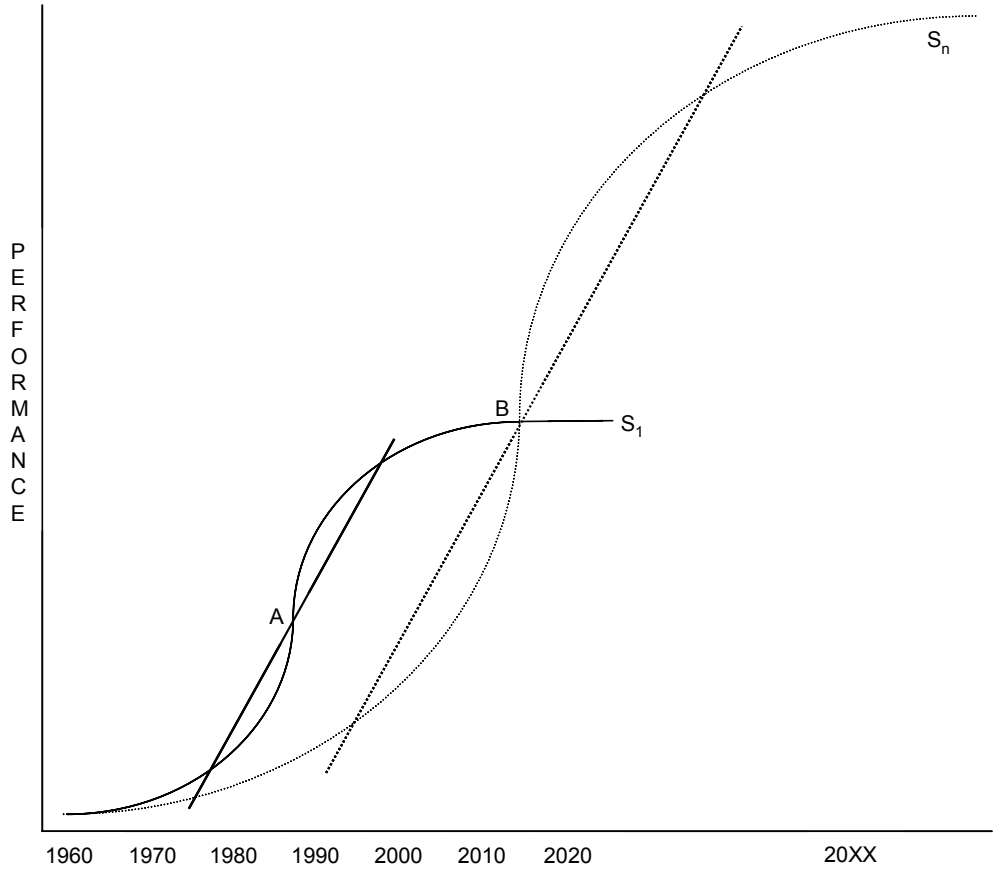

Figure 4-14. Simplified Shifting S-Curves

Figure 4-14 simplifies Figure 4-13 showing the beginning (S_1) curve and a possible ending (S_n) curve. Again, if and when an *ex post* technology history is written about this technology these curves will likely be combined into one, connecting points A and B (the points where diminishing returns set in or as the layperson would say, "when the technology slows down"). The interest here is in the innovation that goes on 'in the meantime' between points A and B. It is not an *ex ante* speculation nor an *ex post* report, but rather an analysis 'as it happens' (within some boundaries). Therefore, the more pertinent question is why the industry continues to advance against the 'logic' of the logistic or S-curve. To help address this, a concept called a *performance possibilities frontier* that combines Dosi's (1982, 1984) notion of a "technological frontier" with

basic economics principle of production possibilities frontier is proposed. Dosi describes a *technological frontier* as:

> ...the highest level reached upon a technological path with respect to the relevant technological and economic dimensions.[111] … By that we mean the highest (or lowest, according to the direction of change) values of the above technological parameters achieved at any point in time, together with the highest levels of knowledge, experience, expertise, design and manufacturing capabilities.[112]

Every first-year economics student is familiar with the principle of *opportunity cost*: given scarcity, the amount of other products that must be foregone or sacrificed to produce a unit of a product. In lay terms this is known as a 'trade-off' (one cannot have his proverbial cake and eat it too). To illustrate opportunity cost, a simple inversely-related curve comparing two products (e.g., guns [A] or butter [B], see Figure 4-15) captures the possible production choices.[113] Note that the opportunity cost of the maximum production level of either product is production of the alternative product (again, one either eats his/her cake or doesn't), thus it is not possible to achieve maximum production of both products, at least not in the present. Given the state of current resources (factors of production) and technology, short-run production choices (resource allocation) then are made along the curve, while long-run changes in resources enable new production possibility sets and thus, economic growth. This is shown by the entire curve shifting out.

Likewise, a *performance* possibilities curve (PPC') reveals the choice (trade-off) between an existing technology (e.g., *on*-Roadmap) and new (e.g., *off*-Roadmap) technologies as shown in

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[111] Giovanni Dosi, "Technological paradigms and technological trajectories: A suggested interpretation of the determinants and directions of technical change," *Research Policy* 11, 1982, 154. A footnote reads: "One may figure that "frontier" as a set of points in a multidimensional space."
[112] Giovanni Dosi, *Technical Change and Industrial Transformation: The Theory and an Application to the Semiconductor Industry*, New York: St. Martin's Press, 1984, 40.
[113] The choice between *guns* or *butter* is the classic application of the production possibilities curve (PPC) concept. Briefly, in the late 1930s the American economy was still in the throes of the Great Depression while Europe prepared for war. Although idle, U.S. national resources were still scarce and the strong likelihood of engaging in war, either indirectly or directly, meant that tough economic choices needed to be made regarding national production and thus the very way of life. Policy choices were made in favor of defense (guns) over normal consumption goods (butter). These choices were intensified following the invasion of Pearl Harbor and industry was transformed (e.g., car manufacturing ceased) while many consumption goods were rationed (including butter). Anyone who has ever held a 1943 'steel' penny is reminded of the necessary sacrifices made to assist in the war effort.

Figures 3-16 and 3-17. In the semiconductor case, the one who 'chooses' is obviously not an individual or even a single company or even country. This is an industry-level choice that is carried out through a complex (or value) network (Rycroft and Kash, 1999; Christensen and Rosenbloom, 1995) of device makers, equipment and material suppliers, research consortia, government labs and agencies, increasingly at an international level. The Roadmap assists in focusing (Rosenberg, 1969) through coordination of this complex network of the semiconductor innovation community. With each incremental innovation, the frontier is pushed outward.

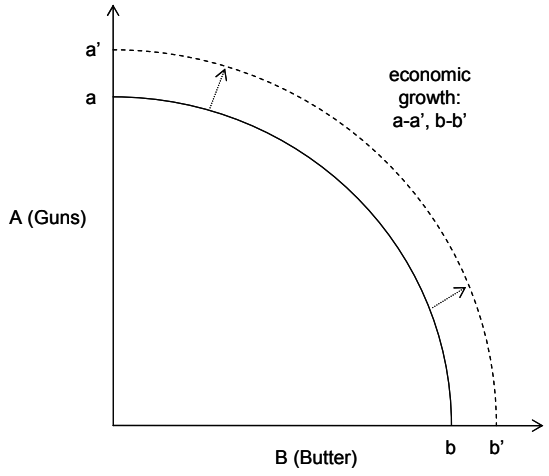

Figure 4-15. Classic Production Possibilities Curve showing economic growth

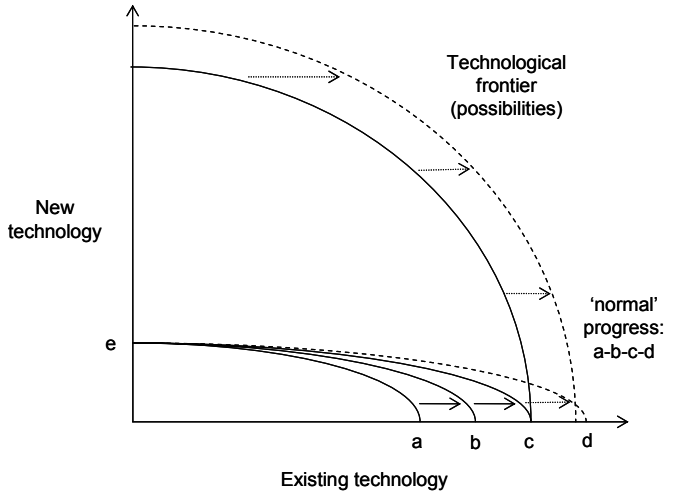

Figure 4-16. Performance Possibilities Curve PPC', showing 'normal' technical progress (a-b-c-d via Roadmap, Moore's Law)

The overall "performance objective" remains the same: increased capability (pushing curve/frontier outward). This is presently (and has been for four decades) measured in terms of Moore's Law (increased circuit density), but does not necessarily have to be. A real variable is the term "new" since this is an unknown. The current definition from the vantage point of existing capability (Roadmap) is "not on Roadmap."

Note that in reality Figures 4-16 and 4-17 should be a 3-demensional (spherical) portrayal since "New" could be just about anything. For simplicity purposes a 2-dimensional graph is used here recognizing this limitation. But if the fullness of the performance possibilities frontier could be portrayed, imagine a suspended sphere representing current capability or performance of a given technology. The accumulated technological knowledge with this technology determines its size (diameter). With each incremental innovation the sphere expands uniformly. Thus, bigger spheres imply longer traditions of incremental innovation. Since the frontier sets the performance benchmark for all future innovations, alternative or 'new' technological choices face increasingly higher opportunity costs. In other words, they become that much harder to do. Hence, incremental innovation reinforces a pattern of continued incremental innovation.

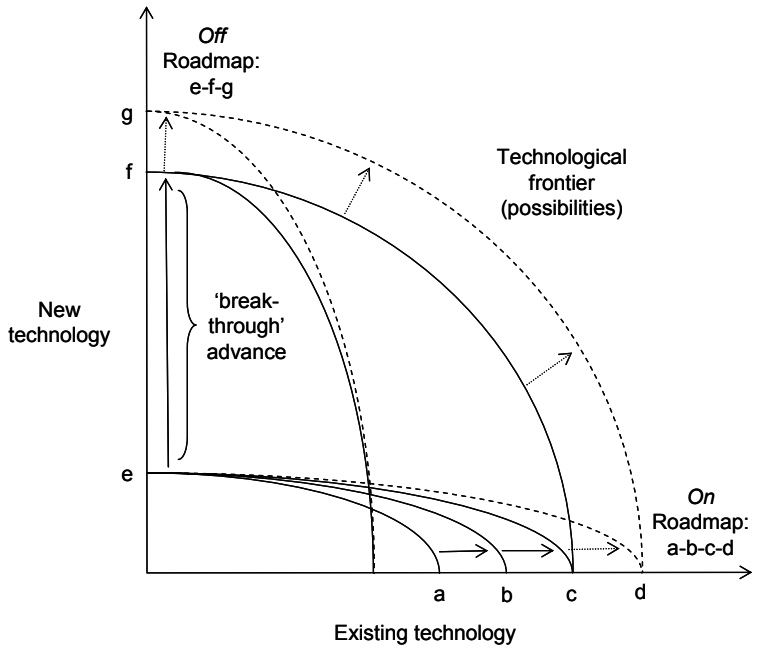

Figure 4-17. Performance Possibilities Curve PPC', showing normal (on Roadmap) advance and possible off-Roadmap advance (e-f-g)

A few caveats or assumptions related to the preceding PPC' graphs include:

- PPC' determinants include accumulated knowledge as the most important factor, along with capital, labor, and other innovation resources.
- The overall goal is increased capability or an ever-increasing technological frontier (e.g., increased device density as presently defined by Moore's Law, but this is not the only way to increased capability, see Appendix C).
- PPC' model also applies to semiconductor materials (e.g., aluminum vs. copper conducting material), manufacturing equipment and processes such as lithography choices (e.g., optical vs. NGL), and related SM&E tools and other technologies.
- Limitation note: many innovation studies are microeconomic, not macroeconomic, thus it is hard to directly apply general principles. The production possibilities curve (PPC) concept is also a microeconomic principle dealing with the production function so this may limit its use here.

Various authors have attempted to describe the limiting factors to innovations. According to Metcalfe (1994), "innovation possibilities" set constraints on what can be achieved. Elements of

these constraints are faced by all technologists working within the relevant institutions and communities of practitioners. The idea of technologies as paradigmatic frameworks which shape the evolution of design problems, guiding and simultaneously limiting advances, is one of the central themes of current thinking on technological change (see earlier discussion on consensus paradigms).[114] Sahal (1981) views the critical role of scaling:

> As in the case of learning, the process of scaling plays an important role in innovative activity not only at the level of a single unit of physical equipment, but also at the plant level… Once technological evolution is considered in its entirety, a much more interesting phenomenon emerges: The extent to which a system can be mechanized depends on the scope for utilization of its scale, whether large or small.[115]

Finally, Rosenberg (1976) sees complex technologies creating internal compulsions and pressures which, in turn, initiate exploratory activity in particular directions. The notion of imbalances in the relation *between machines* is virtually *de rigueur* in any treatment of the English cotton textile industry in the eighteenth century (Kay's flying shuttle leading to the need for speeding up spinning operations, etc.). Rosenberg suggests that, *within a single complex machine or operation*, even more important imbalances frequently exist among its component parts. A concept of technological equilibrium at the system level may be instructive. Thus single improvements tend to *create* their own future problems, which compel further modification and revision.[116]

This is not to say that some radical or breakthrough innovation cannot or does not occur. This type of 'new' innovation is necessary and thus frequent. In fact it may be more frequent than a simple incremental (existing) vs. radical (new) choice set reveals (e.g., copper vs. aluminum conducting materials or 300mm vs. 200mm wafer sizes—this particular innovation is referred to as an architectural innovation by Henderson and Clark, 1990). Community members are well aware of the disruptive nature of these changes. In fact, the transition to 300mm wafer sizes proved very difficult for the industry, despite its anticipation (see Chapter 11). By definition these

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[114] J. S. Metcalfe, "Evolutionary Economics and Technology Policy," *The Economic Journal*, 104, July 1994, 935.
[115] Sahal, 1981, op. cit., 308.
[116] Rosenberg, 1976, op. cit., 28-9, italics in original.

types of major innovations are irregular, take longer, carry higher risk, and often do not work (at least initially)—all the elements of a more Schumpeterian view of technical change. Most importantly, they can come from anywhere since 'new' represents a much greater part of the dimensional space of the sphere than 'existing' as shown in Figure 4-17. However, in the semiconductor industry—and perhaps as well in some other industries—these 'new' innovations are not totally destructive of the given regime, but in fact are compatible and self-supporting relative to the overall objective of pushing the frontier ever farther out. In this industry it is the meta-function of Moore's Law that all share (i.e., as a consensus paradigm) in the innovation process. Whether a front-line technician who tweaks the new equipment to increase productivity (existing axis), or the university scientist experimenting with novel substrate materials ('very' new), both are engaged in pushing the performance envelope.

Vincenti's (1984) historical account of the simultaneous pattern of production of flush-riveted joints that appeared in aircraft skins in the 1930s is an excellent example of employing incremental innovation to push the performance envelope to the right and outward:

> The widespread, simultaneous nature of flush-riveting development is unmistakable. By the end of the basic stage of development, which occupied the second half of the 1930s, at least fifteen manufacturers were using the new type of riveting. That they worked largely independently is indicated by the wide range of head angles from one company to another (78-130 degrees) and the diversity of head dimensions even among companies using the same angle. The need for flush riveting was apparently felt more or less simultaneously everywhere and once it was, work on such riveting welled up from below, so to speak, throughout the industry. This widespread simultaneity is the most striking characteristic of the activity we are examining.[117]

Interestingly, a parallel can be drawn in the earlier days of the U.S. semiconductor industry. In the mid 1980s when Japanese chipmakers overtook the U.S. in DRAM worldwide market share, a call came from within the industry to establish a collective response to the competitive crisis. The creation of Sematech in 1987 was one of the measures undertaken. Although all U.S. chipmakers used basically the same production methods, there was wide variation in techniques used. An

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[117] Walter G. Vincenti, "Technological Knowledge without Science: The Innovation of Flush Riveting in American Airplanes, ca. 1930-ca. 1950," *Technology and Culture*, Vol. 25, 1984, pp. 548-9.

illustrative example of this was the variance of 'gifts' of production processes provided to Sematech by the two largest producers, AT&T and IBM. AT&T, the organization that started the industry some 25 years earlier, contributed a production process that was significantly inferior—approximately two device generations behind—to IBM's process (see Chapter 6).

On the other axis, one example of a discontinuous innovation is Extreme Ultraviolet Lithography (EUV). EUV is one among a handful of candidate technologies considered possible Next Generation Lithography (NGL) technologies expected to replace traditional photolithography techniques. How EUV has gained in importance as a replacement technology is revealing. Stix (2001) states that the unique approach Intel took in co-developing EUV with the Federal Government's National Laboratories stands in marked contrast to the large centralized laboratories built by AT&T, IBM, Xerox and others. "The classical research model never worked," laments G. Dan Hutcheson of VLSI Research. In 1997, at the beginning of Intel's stepped-up involvement, looming technical difficulties caused EUV to be rated last out of four lithography technologies in a straw vote taken at an industry conference. But by late 1998, at another industry session, solutions to many of these problems—such as how to make super-smooth mirrors—had been found, propelling EUV into first place when it came time to vote. "The group went from having an attitude of 'Sure, sure, tell us you can do that' to placing us up front," stated one lithography researcher.[118] In other words, as limits to the technology were overcome, innovation possibilities were expanded and the PPC' shifted upward and outward.

The Roadmap process with its long view (i.e., a 15 year outlook in this industry is a very long time), consensus nature, and broad tent of participation (both geographically and functionally) is all about expanding this sphere in lithography and other supporting technologies in a manner that is aggressive yet practical. Should another 'destructive' sphere come along ('really' new) with performance objectives that depart from the existing regime, this would be considered a revolution in the tradition of Constant's (1980) turbojet revolution. Always wary of this possibility—

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[118] Gary Stix, "Getting More from Moore's," *Scientific American*, Vol. 284, No. 4, April 2001, 32.

and eventuality—the semiconductor community continues its quest toward an ever-expanding performance frontier.

The last section of this chapter considers the PPC' proposition offered here along with evolutionary theory literature previously described. From this a theory of *Organized Innovation* is proposed to more fully explain the evolutionary nature of technical advance that is so characteristic of semiconductor technology.

Toward a Theory of *Organized Innovation*

Considering the path and regularity of historical development of semiconductor technology, it seems that some theoretical explanation can be offered that goes beyond a single variable attribute such as complexity, globalization, research consortia, or even Moore's Law. Realistically, a complete explanation involves all these variables and more. However, what has emerged is an organizing principle for innovativeness that appears unique among other industries, at least presently. That principle is in fact the dynamic ability to innovate without rest. Jan duPreez, president of Infineon's North American operations, says "The only way to stay competitive in this business is to innovate at all times."[119] Don Kash's 1989 book title *Perpetual Innovation*[120] captures the very essence of innovativeness in semiconductors. This tradition, practiced for decades within the semiconductor industry, has only recently been broadly adopted within other industrial sectors. How and why this has occurred for semiconductor technology is now considered. Chapter 6 will provide more background on the development of the industry, but some salient points can be made here regarding the theoretical basis for such development.

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[119] Jan duPreez, quoted in Will Wade, "Turning Dollars Into Development: R&D remains crucial, but leaner budgets are forcing chipmakers to hone their strategies," *Electronic Business News*, Iss. 1295, January 14, 2002.
[120] Don E. Kash, *Perpetual Innovation: The New World of Competition*, New York: Basic Books, 1989.

First and foremost, making chips is a research-intensive endeavor. Gordon Moore calls it "an industry predicated on R&D."[121] The industry was born out of a major scientific breakthrough followed by a spate of equally-important technological advances necessary to manufacture and commercialize semiconductor devices. Important innovations such as the integrated circuit also were the product of research. The industry routinely invests 10 to 15 percent of revenues in R&D, even during periods of downturn.[122] Note that this is well above the national average of 5 percent for all industry. Finally, the industry was an early initiator of industry-funded research consortia and now boasts one of the largest research consortia portfolios around the globe. At the same time, a very small amount of the total R&D budget is devoted to basic research, the very type of research that brought the industry into existence. This point was emphasized in the earlier Rosenberg and Steinmueller reference. Thus the research focus is intensely on shorter-term development efforts, those involving the next product generation or two. The horizon of R&D activities has over time become shorter for a variety of reasons (this will be discussed more in Chapters 11 and 12). In an attempt to determine the possible influence of the Roadmap on this trend, survey respondents for this study were asked whether the Roadmap has qualitatively affected R&D expenditure patterns of the U.S. semiconductor industry (emphasizing more "D" than "R"). In other words, has the Roadmap shortened the research agenda horizon? The answers were mixed (see answers to Question #20 in Appendix B) but a few pointed out that the Roadmap was NOT the primary cause of this:

- Disagree, there is very little R in this industry anyway.
- Agree/Disagree… In fact, more “D” than “R” happens, because that is directly funded by IC producers, and the sources of true “R” funds are scarce. Remember, we don’t have Bell Labs anymore, and IBM is not the altruistic think tank that it once was.
- That's true, but I don't blame the Roadmap for that. I think it's more the environment this industry lives in. Today market life cycles for products are very short, and they've got to hit those windows or they don't make any money. And so that drives the behavior which is afar from papers on fundamental understanding. So what's happened in industry at

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[121] Gordon E. Moore, "Some Personal Perspectives on Research in the Semiconductor Industry," Chapter 7 in Richard S. Rosenbloom and William J. Spencer (eds.), *Engines of Innovation: U.S. Industrial Research at the End of an Era*, Boston: Harvard Business School Press, 1996, 165.
[122] Ibid., 166.

> large is that horizons are shortened for research. They've got to deal with that. That's actually made places like the SRC more important.

Price competition is another powerful ingredient that helps compress time in this industry. According to *Investopedia.com*, "The semiconductor industry lives—and dies—by a simple creed: smaller, faster, and cheaper."[123] The driving force is miniaturization: the relentless pursuit of smaller geometries (finer line widths) enabling more components per chip. Smaller and more devices on a chip operate faster and deliver greater performance. Finally—and most importantly—the unit cost per device (i.e., transistor) decreases accordingly. Thus, lower marginal costs of production are achieved with each 'shrink' so it is no surprise that within a matter of months, the price of a new chip can drop sometimes by half. As a consequence, there is constant pressure on chip makers to innovate.

To further complicate the picture, the semiconductor industry is highly cyclical: semiconductor companies face constant booms and busts in demand for products. Chips are not consumer goods. Their demand is largely derived from end-market demand for personal computers, cell phones, and other electronic equipment. When these sectors fluctuate due to changing macroeconomic conditions, they send a ripple effect through the entire semiconductor supply chain. Good times such as the late 1990s when Microsoft *Windows* and Internet applications, along with the flurry of investment surrounding Y2K, produced a boom for PC and higher-end computer makers. Chip companies were hard pressed to produce enough output to keep up with this demand. But harder times such as the recent (2001-2003) industry downturn have seen flat and even falling PC and other consumer electronics sales combined with weaker industrial demand for telecomm equipment and network systems. Thus chip production has been reduced drastically. After industry revenues peaked in 2000 at over $200 billion, revenues fell by almost one-third in 2001 and was essentially flat in 2002. In fact, the industry does not expect to reach 2000 level revenues until 2004 or possibly 2005 (see Figure 4-18).

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[123] Investopedia.com, "The Industry Handbook—The Semiconductor Industry," http://www.investopedia.com

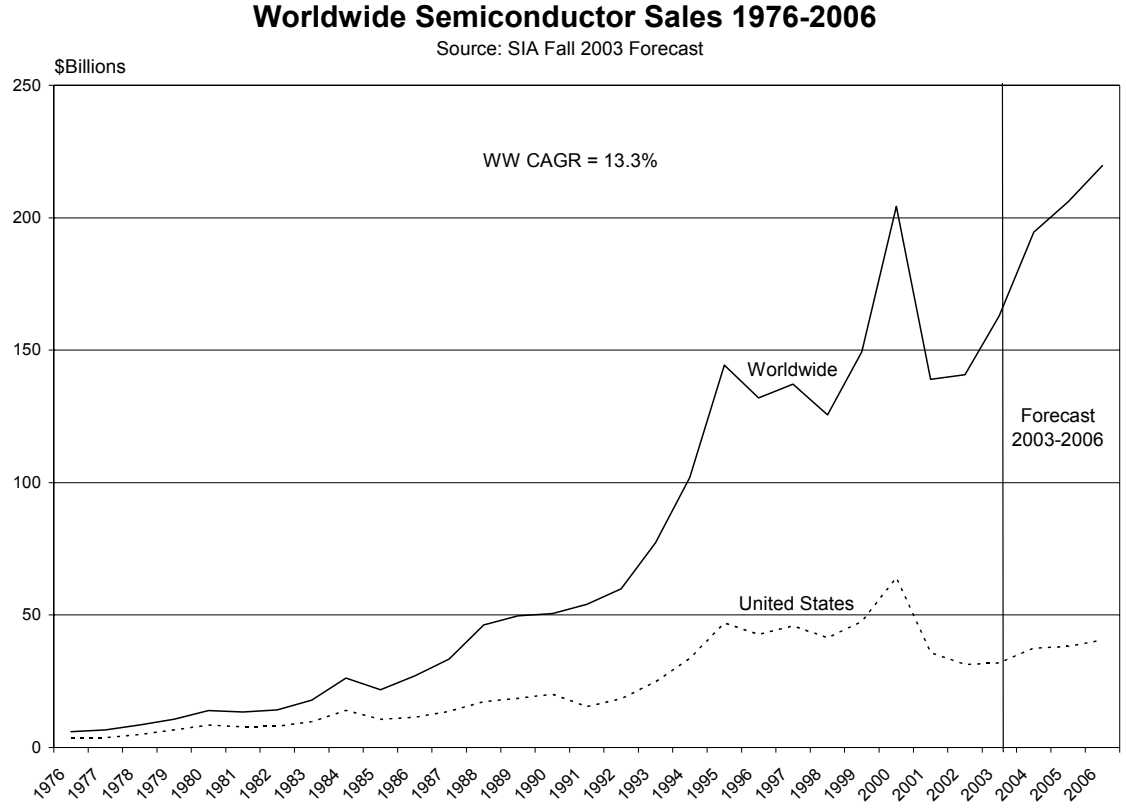

Figure 4-18. Semiconductor Sales, Worldwide and United States, 1976-2006[124]

A look back is instructive. The industry reached the $1 billion revenue milestone by 1964. Fifteen years later (1979) industry revenues topped $10 billion. Another 15 years passed and by 1994 the industry achieved the $100 billion revenue milestone. Based on the historical compound annual growth rates of almost 18% the industry projected $250 billion in revenues by 2000. The industry fell short of this target, but hitting the $200 billion mark in 2000 was still a major milestone.[125] However the real possibility of NO net growth in sales for the next five years is something the industry has never faced. Ray Burgess, corporate vice president and director of strategy for Motorola Semiconductor remarks that the present downturn is historical:

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[124] SIA Semiconductor Forecast was made in November 2003. Actual 2003 sales beat forecast slightly ($166.4B).

[125] Some argue the 2000 sales level was an anomaly because the in-between years 1995-1999 saw little net growth: 1995 $144B; 1996 $132B; 1997 $137B; 1998 $126B, 1999 $149B, 2000 $204B (Source: SIA).

> I have been in this industry since 1980 and I have seen a lot of ups and downs, and this is the worst downturn that the industry has ever had, both psychologically and from the standpoint of the numbers. If you take a rolling 5-year average growth rate, this year [2002] we are at the lowest 5-year compound growth rate in the history of the semiconductor industry.[126]

Despite this cyclicality, chipmakers know from experience that innovation must continue since competitive advantage rests on the next advance in technology. Moore (1996) underscores this point:

> One thing that has always been true in this industry is that recovery after a down cycle never occurs with old products. Technology evolves so rapidly that the market moves to the next generation or beyond. Thus, to be successful it is necessary to continue investing in new products even during these down periods.[127]

Thus chip makers must routinely take part in a form of high stakes gambling. Linda Wilson refers to this as 'placing bets'.[128] The big risk comes from the fact that it can take many months, or even years, after a major development project for companies to find out whether they have hit the jackpot—or blown it all. The pressure extends to chip makers, foundries, design labs and distributors—everyone connected to the business of bringing chips from R&D into high-tech equipment. The result is an industry that continually produces cutting-edge technology while riding volatile business conditions.

It is precisely this tension from the relentless pace of innovation and increased levels of expenditures for research and production capacity within an industry where demand is wildly cyclical that has invoked the need for the Roadmap. It is important to note that the Roadmap is primarily concerned with advancing process technology, the cornerstone of the semiconductor industry's exponential growth. A constant move to smaller process geometries and larger wafers is part of the industry's history. In the economics of chip production wafer size refers to the quantity of raw material. In this case larger wafer size is better—the world's highest semiconductor returns in history occur when it moved to larger wafer sizes. Recently, the move to

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[126] Ray Burgess, quoted in Linda Geppert, "Semiconductors: Rough economic seas pound chipmakers as they steam ahead to advance technologies," *IEEE Spectrum*, January 2003 (forthcoming).
[127] Gordon E. Moore, "Intel—Memories and the Microprocessor," *Daedalus*, Vol. 125, Issue 2, Spring 1996, 78.
[128] Linda Wilson, personal interview.

300mm wafers allows chip makers to manufacture cheaper chips while continuing to make process improvements. For example, the new 300mm wafers are 50% larger in diameter than the 200mm wafers that preceded them. However, the larger wafers yield 2.25 times as much surface area for etching chips, yet costs only about 20% more to process, further ensuring a continuing drop in chip prices and hence everything else that depends on silicon. Yet the cost of a chip factory (or fab) that can handle 300mm platters is at least $2.5 billion and as much as $3.5 billion. Thus only a handful of traditional chipmakers can justify such an investment because earning a return on one of these 'megafabs' requires annual sales of at least $6 billion.[129]

Self-Organization

The semiconductor innovation community has adapted to this turbulent environment through a process of self-organization (see Chapter 3) involving the formation of a variety of structures such as strategic partnerships, research consortia, and the Roadmap. An added point is that this process has become increasingly global (e.g., the *International* Technology Roadmap for Semiconductors).

We now examine this process in more detail. Kash (1989) introduced the notion of organizational *complexes* and *networks*. A complex is composed of all the organizations involved in a general area of activity or product sector. To be part of a complex minimally requires that the organization be involved in the innovation process of a sector. The worldwide semiconductor community is considered an organizational complex. A network, on the other hand, is organized around a discreet activity, product, or process. Networks are subsets of an organizational complex, composed of that specialized expertise and capability needed to carry on a specific product or process. The lithography community (or any of the Roadmap ITWGs) would be considered an organizational network.

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[129] Author unknown, "Chips on Monster Wafers: How the shift to larger wafers and thin circuits will transform the industry," *Business Week Online, International Edition (Asian Cover Story)*, November 11, 2002.

In semiconductor innovation, the underlying factor for these organizational arrangements is the relentless capacity toward miniaturization of device feature sizes. That these devices have approached feature sizes of molecular geometries (i.e., measured in nanometers or billionths of a meter) necessitates an organizational approach to further advance semiconductor technology. As will be discussed in more detail in succeeding chapters, this process has, in fact, been underway in earnest for at least two decades. National cooperative research and development efforts beginning with Japan's VLSI Program in the late 1970s were followed (countered) by the U.S. in the 1980s with the creation of the SRC and Sematech, the latter made possible by the National Cooperative Research Act (NCRA) passed by the U.S. Congress in 1984. A variety of other formal cooperative arrangements including the creation of standards development organizations, strategic alliances and partnerships, even mergers and acquisitions are commonplace throughout the semiconductor community. As important though is the vast amount of much less formal arrangements that have emerged and are integral to the furthering of technological innovation. Many of these are of the typical nature such as shared membership in engineering or other technical societies or associations.

But a few—most notably the Roadmap—are truly unique to semiconductors. The Roadmap falls somewhere in the middle of a range that spans informal to formal organizational structures. It is quite formal in that it is officially sponsored by national industrial trade organizations (e.g., the SIA in the U.S.) and carries a significant budget and modest full-time staff to manage it. There is a formal governance structure that establishes policy and provides guidance and oversight to the dozen official technology working groups charged with the actual development of the Roadmap. On the other hand, Roadmap membership is entirely on a volunteer basis. With membership now totaling close to a thousand and spanning the globe this has become a daunting task, but one that most feel is worthwhile (as evidenced by its growing membership). The next section explains the requisite pattern of innovation from which the Roadmap emerged and within continues to evolve.

Normal Innovation

What all these organizational forms share is a common purpose to advance the technology to ever finer geometries, thereby increasing performance, capability, and thus demand, profits, and continued growth. As stressed in this thesis, the innovation model employed is one of sustained, incremental innovation (i.e., continuous improvement). Traditionally a feature of the Japanese industrial regime, this capability has become imbedded within the semiconductor innovation network. This form of innovation is referred to as *normal* as contrasted with *revolutionary* or *disruptive* innovation. The previously discussed Rycroft and Kash *normal pattern of innovation* best captures this. Antecedents may be found from several scholars including *normal science* (Kuhn, 1963), *normal technology* (Constant, 1973), *normal technical progress* (Dosi, 1982 and 1984), *normal design* (Vincenti, 1990), and simply *normal progress* (Christensen and Rosenbloom, 1995). Dosi, as already discussed, uses the *normal* descriptor to define the broad orientation of innovative activities in which a momentum of its own is maintained. He refers to this as an in-built heuristic that is particularly clear in the semiconductor case.[130]

Vincenti (1990) uses the term "normal design" consistent with Kuhn's and Constant's usage. According to Vincenti, though less conspicuous than radical design, normal design makes up by far the bulk of day-to-day engineering enterprise. The vast design offices at firms like Boeing, General Motors, and Bechtel engage mainly in such activity. In the words of one reader of this material, "For every Kelly Johnson (a highly innovative American airplane designer) there are thousands of useful and productive engineers designing from combinations of off-the-shelf technologies that are then tested, adjusted, and refined until they work satisfactorily." In addition, knowledge for normal design is more circumscribed and easier to deal with. Though it may entail novelty and invention in considerable degree, it is not crucially identified with originality in the

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[130] Dosi, *Technical Change and Industrial Transformation,* op. cit., 68.

same way as knowledge for radical design.[131] Carlson (2000) offers a similar perspective in demystifying the process of invention:

> For some people, invention and evolution are polar opposites. The invention of new technology is typically viewed as a sudden, discontinuous, and revolutionary process through which an inventor stumbles into a new machine or process by accident, not by planned effort… Biological evolution, in contrast, is commonly viewed as a process characterized by small, continuous changes: new species are not supposed to burst suddenly into being. Evolution, moreover, is a process which can be analysed… I would argue, however, that revolution and discontinuity do not describe how inventors actually work. An examination of their notebooks, artefacts and letters reveals that inventors work methodically and purposefully.[132]

Similarly, another reference to semiconductors (actually microelectronics) is made by Vincenti (1984) in his historical analysis of flush riveting in American airplanes previously discussed. The author foresaw a similar pattern that would come to dominate semiconductor technology in a footnote:

> The divorce from science, though a historical fact here, is not essential in principle for widespread innovative activity. If a high degree of scientific aptitude and training were present throughout an industry, widespread science-based innovation could occur when needed provided the essential ideas about the way to proceed were well known or obvious. Perhaps this may already have happened in the microelectronics industry.[133]

Indeed, the way to proceed in semiconductor innovation (i.e., miniaturization of device feature sizes) is now well understood, despite the fact that pure scientific understanding of semiconductor behavior is far removed from the day-to-day practice of engineering, especially process engineering. Recall the Moore quote at the beginning of this chapter: "It's technology that gets the science to come along behind it." A key point in Vincenti's writings is his emphasis on the vital role of the engineer, and in particular the collective effort of the engineering community on the overall innovation process. In the tradition of Kuhn, Constant, and others, his thesis on the community of practitioners as a key variable in advancing technological progress in aircraft design fits well with the semiconductor case. Like the collective interest in continually advancing performance and capability

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[131] Walter G. Vincenti, *What Engineers Know and How They Know It: Analytical Studies from Aeronautical History*, Baltimore: The Johns Hopkins University Press, 1990.
[132] W. Bernard Carlson, "Invention and Evolution: the Case of Edison's Sketches of the Telephone," in Ziman (ed.), 2000, op. cit., 138.
[133] Vincenti, 1984, op. cit., 571.

in aircraft technology including the crucial but 'not so interesting' development of flush vs. protruding rivets, semiconductor technology progresses through the combined efforts of a similar type of fraternity of practitioners. The existence of an industry-wide Roadmap greatly assists the semiconductor innovation community by broadly communicating important technical knowledge, much of which was traditionally tacit in nature. It is this particular feature—explicating tacit knowledge—combined with the public availability of the Roadmap that makes it such a beneficial tool to the semiconductor innovation community.

This process of explicating tacit knowledge has roots that predate the Roadmap. Again, the success of research consortia hinges on the willingness and ability of participants to share needed knowledge. The creation of Sematech provides a rich example of how this process evolves. Also, since the creation of the SIA in 1977 (by a handful of merchant IC companies) its membership grew ten-fold by 1985 and included the all-important captive chipmakers (i.e., IBM and AT&T). Although international trade concerns brought about the formation of the SIA, improving industrial competitiveness would become a priority of the trade association. SIA recognized early on the importance of research (and supply of researchers) to the future of the U.S. semiconductor industry; this was the basis for the Semiconductor Research Corporation (SRC) in 1982. This new model for research departed from the traditional industrial research model whereby larger organizations such as AT&T, IBM, and even TI would develop technologies in their central research labs. Through technical publications and conferences, as well as through profitable license agreements, these technologies would transfer to other, often smaller firms and eventually diffuse throughout the industry. This process is, in fact, how the industry initially was created and had served it well for almost three decades.

But by the late 1970s several factors began to seriously affect the international competitiveness of American manufacturers in several industries. The lifting of price ceilings and the Arab oil crisis fueled a decade-long spate of inflation that contributed to a growing macroeconomic 'malaise'. This was accompanied by stagnant growth and high rates of unemployment, thus the term *stagflation* was

dubbed by economists to help describe this period of unique macroeconomic conditions. At the same time, central industrial labs became harder and harder to maintain as profits were squeezed from the combination of increasing costs due to inflation and falling unit prices due to a stagnant economy and increased foreign competition.

Precompetitive Cooperation

In a review of the literature on cooperation, Smith, Carroll, and Ashford (1995) state that it is rich in theory and diverse in its academic roots, noting that cooperation is a topic of interest in disciplines such as economics, sociology, anthropology, psychology, and political science as well as organizational behavior, organization theory, and strategic management.[134] The authors indicate that two types of cooperative relationships can occur: the formal and the informal. Formal cooperation comes about through official agreement whereas informal cooperation involves adaptable arrangements in which behavioral norms rather than contractual obligations determine the contributions of parties. Eric von Hippel's (1987) essay, "Cooperation between rivals: Informal know-how trading," explores a novel type of informal cooperative behavior: the trading of proprietary know-how between rival (and non-rival) firms:

> The informal proprietary know-how trading behavior I have observed to date appears to involve informal trading "networks" which develop between engineers having common professional interests. Network formation begins when, at conferences and elsewhere,... an engineer … meets, and builds his personal informal list of possibly useful expert contacts.[135]

There is a long history of both types of cooperation within the semiconductor industry, especially among members of the innovation network. With increased complexity, cooperation has become an increasingly important means of addressing growing technical and economic challenges. As has been discussed, informal cooperation was manifest within the practitioner communities of technicians, engineers, and researchers. Further, the high rate of spin-off

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[134] Ken G. Smith, Stephen J. Carroll, and Susan Ashford, "Intra- and Interorganizational Cooperation: Toward a Research Agenda," *Academy of Management Journal*, Vol. 38, No. 1, 1995, 9.
[135] Eric von Hippel, "Cooperation between rivals: Informal know-how trading," *Research Policy* 16, 1987, 292.

company creation (e.g., 'Fairchildren') and excessive employee turnover rates ensured a steady flow of knowledge throughout the industry. Throughout the early stage of the industry life-cycle—until about 1980—informal forms of cooperation were dominant. However, formal cooperation was limited to license agreements, acquisitions, and the like which were not conducive to any lasting relationship beneficial to all parties. In the U.S. in particular, long-standing antitrust laws precluded organizations from cooperative behavior of this sort. This was not the case in Europe and Japan where formal cooperative arrangements had first appeared in the 1970s.

By the 1980s the U.S. semiconductor and broader electronics industries were being rivaled by foreign producers. The pace of technological change was accelerating, thus to remain competitive U.S. companies saw the need to increase research investment. The substantial costs and risks, along with the sheer complexity associated with this type of research, made it increasingly harder for any individual firm to succeed. The SRC was formed in 1982 as an industry-led cooperative research initiative. But the stakes had been raised by international competition to a level beyond which the industry could handle alone. It was now very clear that foreign competition—from Japan in particular—would significantly affect American producers' markets both domestically and abroad. Industrial 'competitiveness' emerged as a national priority that begat a variety of public policy discussions and proposals. Following the lead of Japan and Europe, U.S. industry became interested in amending the antitrust laws to permit for-profit R&D consortia. One important policy initiative that resulted from this was the National Cooperative Research Act of 1984.[136] The SIA had helped lobby for its passage, but a key catalyst for this change was the formation of the Microelectronic and Computer Technology Corporation (MCC) in 1983. This consortium of microcomputer and electronic firms recognized the potential legal hazards in pooling their resources for R&D. During its formation and after its establishment, MCC proposed to Congress a change in the antitrust laws. U.S. lawmakers, concerned over the decline in corporate R&D spending and recognizing that U.S. companies were falling behind those in

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[136] Public Law 98-462.

Japan and Europe, unanimously passed the NCRA. The NCRA encourages cooperative R&D efforts at the precompetitive stage of production by limiting the antitrust exposure of consortia that file with the Department of Justice. Precompetitive research encompasses experimentation and study of phenomena and observable facts, development or testing of engineering techniques, development of prototypes and models, and collection and exchange of research information. In effect, precompetitive cooperative research limited collaboration to such areas as basic research or to its applications in such areas as establishing standards or formulating processes rather than focusing on developing marketable products.[137]

Congress designed the act to give American firms the same research capability enjoyed in other nations. The NCRA lifted industry barriers to communication and cooperation, at least in basic research, by exempting registered R&D consortia from the treble damages provision of antitrust law. The NCRA requires that "joint research and development venture(s) shall not be deemed illegal per se," and that such ventures instead shall be "judged on the basis of [their] reasonableness, taking into account all relevant factors affecting competition, including, but not limited to, effects on competition in properly defined, relevant research and development markets." Thus, Congress made clear that any antitrust litigation concerning cooperative research efforts should be judged under the rule of reason. The U.S. government retains the right to adjudicate the legality of R&D consortia.[138]

One area that proved very helpful to the semiconductor industry was the definition of the term *precompetitive*, an area that would be common territory for cooperation. It was now allowable to work in areas common throughout the industry. Most importantly in semiconductors was the complex chip fabrication process. Sematech's formation came about to address this area that all chipmakers shared an interest in. Now that the once-proprietary process (black art) of chip-

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[137] Larry D. Browning and Judy C. Shetler, *Sematech: Saving the U.S. Semiconductor Industry*, College Station, TX: Texas A&M University Press, unpublished manuscript, 11-12, and William M. Evan and Paul Olk, "R&D Consortia: A New U.S. Organizational Form," *Sloan Management Review*, Spring 1990, 39.
[138] Evan and Olk, "R&D Consortia," op. cit., and Thomas M. Jorde and David J. Teece, "Competition and Cooperation: Striking the Right Balance," *California Management Review*, Spring 1989, 31.

making was considered precompetitive, the gap between leading-edge and less-advanced producers began to narrow as the collective knowledge of all producers was openly shared, as previously discussed.

Reflecting the broad concern that U.S. manufacturing capability had lagged other nations, by the late 1980s various national competitiveness reports were released (e.g., the 1988 MIT report: *Made in America: Regaining the Productive Edge*) identifying the antitrust exclusion of production joint ventures in the NCRA as a competitive barrier for American industry.[139] The National Cooperative Research and Production ACT (NCRPA, 15 U.S.C. 4301-06) of 1993 amended the NCRA to include cooperative *production* ventures. Interestingly, while almost 300 new registrations were made in the first three years following the amended law's passage, only three of these (1%) were production joint ventures.[140] Nonetheless, the NCRA and NCRPA have had profound effects on cooperative initiatives—including the rapid growth of research and other consortia in particular—within U.S. industry.

Moving from informal to formal types of cooperation, another form of cooperative behavior that has gradually taken place is now discussed. This is the evolution of research capability regarding process technology moving 'upstream' from the semiconductor device industry to the semiconductor equipment industry. Eric von Hippel's (1988) *The Sources of Innovation* provides a detailed historical account of fifteen major innovations in silicon semiconductors (among other technologies) and strongly argues the dominant role of the user (i.e., chip maker) in the innovation process. In many cases (e.g., mask alignment using split field optics), Fairchild or another user firm initially developed the technique in-house which was later offered commercially by an equipment manufacturer.[141]

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[139] Thomas A. Hemphill, "U.S. Technology Policy, Intraindustry Joint Ventures, and the National Cooperative Research and Production Act of 1993," *Business Economics*, Vol. 32, Iss. 4, October 1997.
[140] Ibid.
[141] Eric von Hippel, *The Sources of Innovation*, New York: Oxford University Press, 1988. Von Hippel also points out that the equipment manufacturer's "developer" in this particular case was formerly an employee at Fairchild and may have been in a position to have previous knowledge of it. The free movement of skilled

Gordon Moore recalls one experience of his early days at Fairchild involving Art Lash, a technician who was paid for work on nights and weekends at home to make capillary tubes used in a critical gold-bonding process. Lash also developed diffusion furnaces that were essential to device fabrication:

> At Fairchild we were talking about these gold balls that you stick on that [form a bond]. I had a technician working for me. We made the first little capillary tubes to put the gold wire through. We used to draw glass down to get a very narrow hole and poke this 2 mil gold wire through it, and you have to cut the capillary off at just the right place so the hole was the right size, and then that was the thing that you used to push the gold ball on to make it bond, then it come up like a sewing machine, you'd cut it off and make another ball, put the next one on. And these things got plugged fairly often, so the guy who was setting up our production started paying my technician to do this nights and weekends to make these capillaries at home and pretty soon that business got so big that he quit and set up Electroglas, which was the first one of these equipment companies.
>
> That was the first one that I know of. And he started making those, and he'd also been helping me build furnaces—we had to build our own furnaces in those days. So he took the basic furnace design and started building furnaces, first for us, then for the industry. Then, we were still building our own furnaces. I guess we bought one from him pretty much from the beginning, but he kept developing furnaces and selling them to everybody and pretty soon his furnaces were a lot better than the designs we had. And we discovered that eventually epitaxial growth, which was a new process, [was developed by this new] commercial source. The ones that were being done as a product to sell rapidly became a lot better than what we were doing internally. So it was decided it didn't make any sense at all to try to do these internally.[142]

Over time Electroglas would shift its emphasis from glass capillaries and diffusion furnaces to wafer probing technology. Today, Electroglas is a leading provider of automated probing technologies with an installed base of more than 15,000 systems.[143]

Upstream Capability (Research) Transfer: precompetitive evolution

As evident by Moore's quote, semiconductor production was a turnkey process in the industry's early days. The entire fabrication of chips was the responsibility of the chip maker,

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personnel is characteristic of the semiconductor industry, especially in its earlier stages. Gordon Moore's career is an apt example. Moore's early collaboration with William Shockley (co-inventor of the transistor) at Shockley Labs allowed him to meet Robert Noyce; the pair then co-founded Fairchild Semiconductor in 1957. As will be discussed, Fairchild would spawn some 150 companies, including Intel which Moore and Noyce co-founded in 1968. Moore served as Intel's CEO, then Chairman until retirement in 1997, upon which he was appointed Chairman Emeritus.

[142] Gordon Moore, personal interview, June 13, 1996.

[143] Electroglas, Inc. website http://www.electroglas.com

including 'growing' the silicon ingots. All of the complex front-end processes from material and chemical handling to wafer slicing, polishing, preparation, etch, ionization, etc. to testing and other critical steps were developed by the chip maker. Even early lithographic tools and processes were developed by chip makers. Gradually these capabilities were transferred 'upstream' creating the SM&E industry.

In parallel, U.S. manufacturers had begun the process of transferring the labor intensive back-end processes (i.e., assembly, packaging, and final test) to several overseas locations where unit labor costs were significantly cheaper. With time these steps became increasingly automated and overseas chip assembly facilities steadily declined in usage by U.S. chip makers. Additionally, the nascent SM&E industry began to provide chip makers with better and less costly process tools as they could market to multiple customers. Equipment suppliers also became more skilled in developing the procedural 'recipes' that would accompany the new tools.

An interesting phenomenon took place regarding knowledge transfer. When the fab process was completely turnkey, there was little knowledge transfer external to the chip maker (with the exception of new equipment requirements and other specifications to toolmakers). In fact, the fiercely competitive market environment caused producers to closely guard all production-related information since competitive advantage usually went to the first to implement a new process. As an independent SM&E industry became established, external knowledge transfer necessarily had to increase between chip maker and supplier firms. For competitive reasons, chip makers naturally insisted that suppliers not divulge any of this information to any of their other customers (i.e., the chip maker's competitors). Some chip makers even held exclusive supplier agreements to protect the potential transfer of knowledge to competitors. But it was in the suppliers' economic interests (i.e., scale economies) to find multiple customers for their tools. Thus it was only a matter of time before information sharing became more widespread between suppliers and manufacturers. By the mid 1980s this had become common practice. Intel's Mike Splinter's more recent perspective summarizes the changing role between Intel and its suppliers:

> [T]he sophistication of the suppliers has become dramatically higher. The level of technology that they have to deal with has increased dramatically so their technical capability has increased… I think the collaboration between the semiconductor companies and the equipment companies has changed a lot. We're doing many more joint projects than we ever did in the past. That's where I see a big difference. The whole move for process equipment companies to do their cell or total module development is coming from a different location.[144]

Since there was also a tendency to standardize process tools and recipes, this led indirectly to fabrication processes having less and less uniqueness, thus containing less proprietary knowledge. It was partly this growing influence of the supplier industry that coincided with international competitiveness pressures that facilitated information/knowledge sharing (e.g., NCRA) that helped the industry come to a consensus on a precompetitive definition.

By the late 1980s a less fragmented semiconductor equipment industry began the development of needed compatibility standards. Citing well-studied cases such as the QWERTY keyboard, VHS videocassette recorder, IBM-compatible PC, and 33rpm LP record, Langlois (1998) describes the process whereby cluster-tool equipment standards emerged in 1989:

> In all of those cases, standards emerged through a competition or "battle of the standards" among alternatives originally offered as proprietary schemes. A standards battle did once threaten in the cluster-tool industry, and such a battle may yet take place. But the origins of the standards in this case were, if not exactly "spontaneous," then at least far more grass-roots and collaborative in character. The Modular Equipment Standards Architecture (MESA) was the result of the work of an *ad hoc* organization comprising the bulk of firms in the cluster-tool and related industries. …the MESA committee was folded into Semiconductor Equipment and Materials International (SEMI), the equipment makers' trade group, becoming the Modular Equipment Standards Committee (MESC)… And … it appears that MESC has indeed been established as *the* industry standard. [145]

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[144] Mike Splinter, *Micro Magazine* interview
http://www.micromagazine.com/archive/00/03/microinterview.html

[145] Richard N. Langlois, "Capabilities and Vertical Disintegration in Process Technology: The Case of Semiconductor Fabrication Equipment," Draft typescript, January 1998, 27, emphasis in original. The author uses an interesting footnote to describe the significance of standards setting. Footnote 17 states: "A better historical analogy for the MESA/MESC standards might be the efforts of the Society of Automotive Engineers, led at first by Howard E. Coffin of the Hudson Motor Car Company, to standardize numerous parts used in the early automobile industry. Between 1910 and 1920, the S.A.E. reduced the number of types of steel tubing from 1,600 to 210 and the number of standards of lock washer from 800 to 16." Original citation from Epstein, 1928, 41-3.

captures his historical perspective on the gradual transfer of IC tool-making from IBM to external equipment suppliers, necessitating the increased importance of an industry roadmap.

Box 4-2. Industry Evolution and the Roadmap: A Perspective from Randy Isaac[146]

[F]rom a provider point of view, one of the real values of a roadmap is you need other people to *invest* in a timely way so that they are there with the support structure that you need. You can't go and hold their hands one by one - you need a global roadmap - that's tremendously valuable. Since I joined the company in the mid '70s until now there's been fascinating change. In the mid '70s, IBM built almost every piece of its process equipment … I guess maybe eighty percent. We designed and built ion implanters. We designed and built air handling systems. We designed and built our wafer cleaning - our chem hoods. We designed and built our deposition systems, our etch chambers.

But as the industry matures it's not cost effective. The volume is too small, and you get specialists who can do it better. So now we're evolved to a very large set of the equipment - we are basically dependent upon the infrastructure. So you see in copper that one of the first things we did was to work with one or two equipment vendors to ensure that they could produce tools that would run this process. Now you see it's not economically viable for them to produce tools only for IBM. So in order to keep them healthy we have to insure that the rest of the industry also does copper. So there's a sense in which we cannot keep copper to ourselves very long, because we want to be able to sustain it. So that's why I tell my team that we have to step out and be leaders and to be a technical leader means you have to get the rest of the industry to follow. If they don't follow you're a loner, you're not a leader - because they are not following you. You've got to get them to follow you so that there will be a market for the equipment for other people so they can stay in business, so they can sustain it, so you want this whole thing.

Now, to me this is where a roadmap is important. See now copper wasn't - depending on your point of view - necessarily a roadmap: it's not like scaling aluminum. And so copper is a discontinuity - so that's why we had to work especially with equipment suppliers so that they'd be ready in time. A roadmap provides that function in a non-proprietary fashion: the entire industry can see, anybody can jump in because he knows that there's a good probability that there will be equipment needed in this time frame. You now can make that investment and start thinking about that ahead of time. So the roadmap is a very important economic necessity, rather than just an interesting self-fulfilling prophecy - let's all try to do it. It's really an economic necessity.

So what it means is that you have to keep moving - and that's partly what keeps this whole industry accelerating, because - let's stick with copper - we couldn't keep it to ourselves. We need the equipment vendors to be viable and everything else, you know etching, other suppliers, and all that. But what does that mean then? Where's our advantage? Well it means we can't sit still - we have to move on to another parameter. So in the case of copper it means being more productive, being more effective, implementing it more appropriately. Not just having the raw capability, but being able to do it in a better way. But then at some point, you have to recognize that, well there are other parameters that you're going to have to - you can't just stick to copper, you have to move on to something else. There's our SOI - there's another parameter: silicon on insulator. Or silicon germanium - you look for others - you cannot sit still!

[146] Randy Isaac, personal interview, July 18, 2000.

The SM&E industry has grown significantly in scale and scope as shown in Table 4-2. After losing the leadership spot in the 1980s, the U.S. has reclaimed this position. Applied Materials, now the industry's largest semiconductor tool maker by a wide margin, also ranked *second* largest in the broader semiconductor industry in 2000.[147]

Table 4-2. Top 10 Semiconductor-Equipment Manufacturers, 1979, 1989, 1995, 2000

1979		1989		1995		2000	
Company	**Rev**	**Company**	**Rev**	**Company**	**Rev**	**Company**	**Rev**
Fairchild TSG (US)	$111	Tokyo Electron (J)	$634	Applied Materials (US)	$3500	Applied Materials (US)	$10410
Perkin-Elmer (US)	101	Nikon (J)	582	Tokyo Electron (J)	2872	Tokyo Electron (J)	5142
Applied Materials (US)	54	Applied Materials (US)	523	Nikon (J)	1820	Nikon (J)	2432
GCA (US)	54	Advantest (J)	399	Canon (J)	1215	Teradyne (US)	2044
Teradyne (US)	53	Canon (J)	384	Lam Research (US)	1030	ASM Lithography (E)	2016
Varian (US)	51	General Signal-GCA (US)	354	Advantest (J)	1027	KLA-Tencor (US)	2003
Tektronix (US)	39	Varian (US)	335	Hitachi (J)	791	Advantest (J)	1865
Eaton (US)	38	Hitachi (J)	210	Teradyne (US)	675	Lam Research (US)	1627
Kulicke & Soffa (US)	37	Teradyne (US)	200	Dainippon Screen (J)	617	Canon (J)	1418
Balzers A.G. (E)	34	Silicon Valley Group (US)	187	Varian (US)	606	Dainippon Screen (J)	1390

Notes: Dollars in millions. Legend: US = U. S. firm; J = Japanese; E = European.

Source: VLSI Research, "Executive Advisory: Top Ten Semiconductor Equipment Manufacturers," April 15, 2002, http://www.vlsiresearch.com/

On the other hand, the increasing sophistication, capability, and complexity of semiconductor supplier equipment have placed additional challenges on innovation within this new industrial sector. New "plug-and-play" requirements are also pushing previously discussed higher investment trends in the device maker industry upstream to equipment makers:

> This is very significant problem for the industry because it puts a constraint on innovation. Twenty years ago, there was greater R&D partnership on the part of equipment and semiconductor companies. If you wanted to develop a new piece of equipment, you'd build a couple and put them with customers and work with them to develop it further, and

[147] Court Skinner, telephone interview, July 21, 2000. Note that at the time Texas Instruments' total revenues were greater than those of Applied, but TI's semiconductor division revenues did not match Applied's total revenues that would exceed $10 billion that year.

> then market it. The environment has now shifted, and customers require that equipment come into the factory plug-and-play.
>
> There's nothing wrong with this, except that we must recognize that there is a learning curve involved, and that to get a plug-and-play piece of equipment you must build a number of them. The cost of that development—from prototype to plug-and-play—is significant. This puts constraints on innovation in our industry and stifles new companies due to the $50M investment it takes to bring each new product out. The stakes get bigger as we go through each of these transitions, and I am unsure of what the solution might be.[148]

This caption captures one important trade-off of moving to a new stage of relationship between device maker and supplier communities. It further supports the need for increased coordination across the supply chain at a level that substitutes for 'R&D partnerships' no longer feasible between individual suppliers and customers.

ORGANIZED INNOVATION

Similar Concepts

As background, some authors have offered similar terms to describe concepts likened to *organized innovation*. Von Hippel (1987) discusses empirical evidence contrary to his thesis on know-how trading that relates here. Specifically, he cites Allen's (1983) research of nineteenth-century English steel industry where a phenomenon the author called "collective invention" was reported.[149] Von Hippel summarizes Allen's work:

> Allen explored progressive changes in two important attributes during 1850-1875 in England's Cleveland district: an increase in the height of furnace chimneys, and an increase in the temperature of the "blast" air pumped into an iron furnace during operation. Both types of technical change resulted in a significant and progressive improvement… Next, he examined technical writings of the time, and found … publicly revealed data on their furnace design… Thus, it appeared that some firms revealed data of apparent competitive value to both existing and potential rivals, a phenomenon he called *collective invention*… In contrast [with know-how trading], collective invention

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[148] Court Wozniak, in Alexander E. Braun, "Interview with Court Wozniak, Electroglas Chairman and CEO," *Semiconductor International*, January 1, 2003.
[149] Robert C. Allen, "Collective Invention," *Journal of Economic Behavior and Organization* 4 (1), 1983, 1-24.

> requires that all competitors and potential competitors be given free access to proprietary know-how.[150]

Allen's *collective invention* can be likened to Vincenti's *simultaneous pattern* of flush riveting innovation, or more recently to today's *Linux* operating system development model where open source code enables shared development. It is also an appropriate corollary to this theory of *organized innovation* within the semiconductor industry. There are, no doubt, other similar examples. One difference worth noting between the innovation patterns of late 19th century British steel and contemporary semiconductor technology (and *Linux* development) is the overt public nature of technical knowledge.

Another example is *systemic innovation* used in a variety of ways. Langlois (1998) sees systemic innovation as becoming the norm, at least in process innovations:

> [T]he systemic or autonomous nature of innovation is neither entirely exogenous nor driven solely by technology. The structure of organization helps shape the pattern of innovation, which in turn influences the subsequent structure of organization. In short, a theory of organizational structure is properly part of an evolutionary theory of social institutions… [T]he literature on the learning curve often implies that in the realm of manufacturing and process technology, *systemic innovation*—fine tuning the production process—is the norm.[151]

Baba and Imai (1993) emphasize the network view of innovation, where "a group of network participants becomes directly responsible for the management of innovations… Furthermore, network participants such as equipment suppliers to joint firms or marketers for licensing firms seem to deserve the status of network-type entrepreneurs because of the critical, if inconspicuous, role they play in the coordination process." [152] The authors also use the term *systemic innovation* in a similar context, drawing the relationship with innovation networks:

> The systemic nature of innovation has recently been highlighted… We might term an innovation brought about by the broader systemic sequence, a *systemic innovation*… Network organization is a basic institutional arrangement to cope with systemic innovation… We emphasize the importance of co-operative relationships among firms as a key linkage mechanism of network configurations. Networks take not only the joint-

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[150] Eric von Hippel, "Cooperation between rivals: Informal know-how trading," op. cit., 296-7, italics added.
[151] Langlois, 1998, op. cit., 2, emphasis added.
[152] Baba and Imai, 1993, op. cit., 25.

> venture form, but also that of long-term collaboration or co-operation (e.g. OEM, subcontracting and cross-licensing).[153]

The authors illustrate the significance of network innovation by asserting that "the *de facto* world standard, i.e. VHS, has persisted partly due to the VHS format network."[154]

In explaining innovation in the telecommunications industry, Godoe (2000) offers the term *innovation regimes* as a conceptual framework for how innovations in telecom are created, particularly explanation of radical, yet *intentional*, innovations. She states:

> The global innovation system which constitute the innovation regimes in telecom may be of a type that van den Belt and Rip (1987) term a ‘‘cultural matrix’’ which creates an ‘‘exemplar’’, i.e., new technological paradigms. However, its formalized institutional characteristics makes the term ‘‘innovation regime’’ more apt and precise, because the sector, due to its innovation regimes, was (until recently) capable of continuously creating a broad range of innovations, many of these radical innovations. Furthermore, these innovations were outcomes of *intentions*: These were made on purpose—for a purpose, and not as results of serendipity. Thus, their degree of success, their ability to qualify as innovations, is also a measurement of the rationality of the innovation regime.[155]

While not using an innovation term *per se*, Henderson and Clark (1990) observe the importance of *architectural knowledge* imbedded within organizations, and how the communication channels between organizations build this architectural knowledge. The room fan example and the related subtask organizations that are created mark a parallel with much of the material presented in this chapter:

> An organization's communication channels … are the relationships around which the organization builds architectural knowledge. Thus an organization’s communication channels will come to embody its architectural knowledge of the linkages between components that are critical to effective design. For example, as a dominant design for room fans emerges, an effective organization in the industry will organize itself around its conception of the product’s primary components, since these are the key subtasks of the organization’s design problem. The organization may create a fan-blade group, a motor group, and so on. The communication channels that are created between these groups will reflect the organization’s knowledge of the critical interactions between them.[156]

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[153] Ibid., italics in original.
[154] Ibid., 31.
[155] Helge Godoe, "Innovation regimes, R&D and radical innovations in telecommunications," *Research Policy*, 29, 2000, 1039-40, quotes in original.
[156] Rebecca M. Henderson and Kim B. Clark, "Architectural innovation: the reconfiguration of existing product technologies and the failure of established firms," *Administrative Science Quarterly*, March 1990, v35, n1, p9(22).

Towards a Definition

Given these related concepts and the material presented in this chapter, the final step is to synthesize a definition for *organized innovation*. Before doing this it is important to note some general trends in the innovation process that have influence. One key trend is the routinization of the innovation process. Sahal (1983) observed this as he referenced Schumpeter:

> It is much easier now than it has been in the past to do things that lie outside familiar routine—innovation itself is being reduced to routine. Technological progress is increasingly becoming the business of teams of trained specialists who turn out what is required and make it work in predictable ways. The romance of earlier commercial adventure is rapidly wearing away, because so many more things can be strictly calculated that had of old to be visualized in a flash of genius.[157]

In a similar vein, John Kenneth Galbraith observes, "It is a commonplace of modern technology that there is a high measure of certainty that problems have solutions before there is knowledge of how they are to be solved." while Dalton states, "Technological innovation is no longer the haphazard result of occasional discovery. It has become institutionalized through corporate, university and governmental research."[158]

Similarly, Fairtlough (2000) points out that during the course of his writing Schumpeter assumed two models of innovation (the author referred to these as Mark I and Mark II). In his earlier work (Mark I), innovation is the result of the constant formation of new entrepreneurial firms, each of which introduces some new product or process. Schumpeter derived this model from the sort of innovation he saw as prevalent in the late nineteenth century.[159] In contrast, Mark II innovation emerges from the R&D laboratories of large corporations and was suggested to Schumpeter by the innovation typical of the first half of the twentieth century. The author generalizes from Schumpeter's two models and classifies innovation into two types: *individualist* and *collaborative*. Individualist innovation includes entrepreneurial firms, but also individual innovators and small academic groups, and even unauthorized 'skunk works' within large firms.

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[157] Devendra Sahal, "Invention, Innovation, and Economic Evolution," *Technological Forecasting and Social Change* 12, 1983, 213-4, Schumpeter quote taken from *Capitalism, Socialism, and Democracy*, 1942, 132.
[158] Ibid.
[159] Gerard Fairtlough, "The Organization of Innovative Enterprises," in Ziman (ed.), 2000, op. cit., 267.

Collaborative innovation includes corporate R&D laboratories, but also large government laboratories and perhaps a few large, well-coordinated academic research laboratories. Collaborative innovation benefits from sustained interaction within a group of people, who develop shared tacit knowledge, shared mental models and 'shared literacy'.[160] By adding a dimension for the major driver of innovation (i.e., discovery vs. design), he suggests a typology of innovation to help contrast the two models (see Figure 4-19):

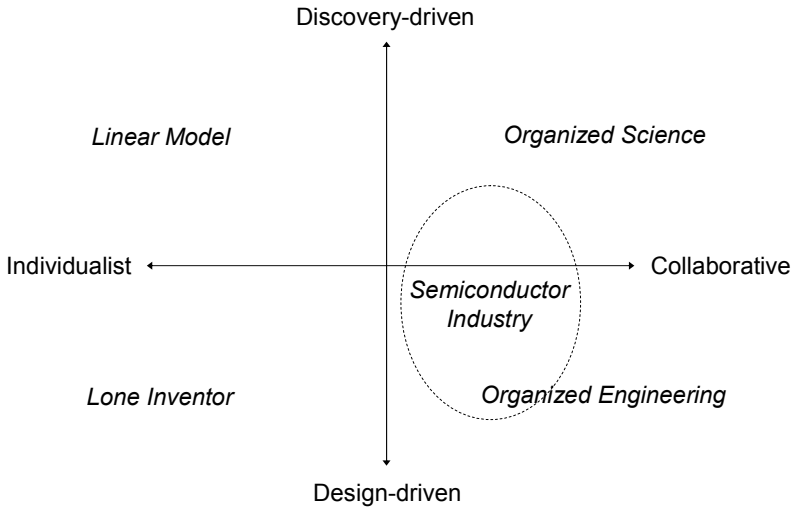

Figure 4-19. Fairtlough Innovation Matrix

Source: Adapted from Gerard Fairtlough, "The Organization of Innovative Enterprises," in Ziman (ed.), 2000, op. cit., Figure 19.1, 269.

Fairtlough classified each quadrant of the matrix and used the terms *organized science* and *organized engineering* for the top right and bottom right quadrants respectively. Today's semiconductor industry fits in the right half of this matrix. Following life-cycle theory (and Schumpeter's observation) the industry has gradually shifted to the right from an individualist

[160] Ibid., quotes in original.

model (e.g., Shockley, Kilby, Noyce, etc.) to a collaborative model (e.g., SRC, Sematech and other research consortia, the Roadmap, etc.). Regarding the other axis, with the exception of the initial discovery of the transistor the industry has never been a practitioner of the linear model. However, R&D spending is significant and blends shorter-term process improvements with longer-term needs such as NGL and novel materials and device structures. Thus, the semiconductor industry is classified as occupying both right quadrants with more emphasis on the bottom right (i.e., design-driven/collaborative). Indeed the author noted that in this particular study, pharmaceuticals, semiconductor devices, plastics materials and materials and medical instruments emerged as the industries with the greatest proximity to a science.[161] Consistent with the material presented in this chapter, the author states that the large majority of technological innovation today depends less on leaps of the imagination than on skilful choice and disciplined development of the right ideas. This is increasingly a social process, a process of group learning.[162] He also draws the connection between organization and technological evolution:

> Technologies and technologically innovative organizations must be expected to evolve together… When coevolution of technologies and organization styles is a gradual process, the likely result is a trend towards the bottom right of the matrix, a trend to design-driven innovation and towards large, highly collaborative organizations.[163]

This is precisely the case with the semiconductor industry and its Roadmap, which provides an industry-wide 'shared literacy' for innovation. The placement of the industry's innovation model toward the lower right quadrant is referred to as *organized innovation*, bridging both design *and* discovery elements into the domain. Fairtlough also notes that this trend can be reversed by unexpected discoveries in basic science, or drastic cost reductions in the products of other industries. Sahal too points out that innovative systems are *inherently untidy* systems and any attempt to routinize the course of research and development activity is doomed to failure. Thus, the only essential condition of a dynamic organization is the property of self-organization.[164]

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[161] Ibid., 271.
[162] Ibid., 274-5.
[163] Ibid., 277.
[164] Sahal, 1983, op. cit., 233.

On the contrary, it is argued that organized innovation is not only possible, but is actually the product of self-organization, reinforced by the Roadmap and other collaborative institutions. Within this context has emerged the concept called *organized innovation*: in simplest terms the structured approach to innovation (i.e., directed efforts at some specific end). But this simple definition is not adequate as systematic industrial R&D has been practiced successfully for almost 80 years, though industrial R&D does not constitute innovation in the broader context. Horwitz (1979) noted that R&D is neither a necessary nor sufficient condition for technological innovation, yet there is still a body of opinion, both within the scientific community and, for example, in the Congress, which appears to treat the terms "R&D" and "innovation" as practically synonymous.[165]

In semiconductor innovation it has been argued that several organizational forms are operating—from university researchers working at the edge of scientific knowledge to the practitioner community of front-line technicians fine-tuning or 'tweaking' process recipes. Both groups, and everyone in between, share the same objective: to advance the technology ever farther by packing more and more capability on the same space of substrate. Achieving this feat with such regularity and hence predictability does not occur by chance. It happens as a result of an orchestrated effort that has Moore's Law as its conductor. Past performance has much to do with it. The way has been shown through the heuristics of previous device generations carried forward through continual engineering practice into successive device generations.

As will be discussed in Chapter 8, Moore's Law is not a physical law like Newton's law of gravity or other laws of physics. It is not considered a behavioral law such as the laws of demand or supply in microeconomic theory. There is no theoretical foundation behind Moore's Law. The original 'plot' was derived from a simple observation. The 'law' is an outcome of numerous forces at play that all have in common the goal of achieving increased performance and capability at reduced unit cost.

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[165] Paul Horwitz, "Direct Government Funding of Research and Development: Intended and Unintended Effects of Industrial Innovation," in Hill and Utterback, 1979, op. cit., 255, quotes in original.

Though this is the objective of any enterprise, the unique arrangement within the semiconductor innovation network (or complex) provides an implicit structure that directs innovative efforts in a more coordinated fashion than in other industries. Thus, from an innovation standpoint, Moore's Law is really a manifestation of many factors. These include heuristics, knowledge—both explicit and tacit, an R&D investment pattern that remains true during economic downturns, and a fairly open exchange of information—both vertically and laterally. Open communication is greatly assisted by a widely accepted definition of precompetitive activities along with enabling institutions and organizations such as research consortia (e.g., SRC, Sematech) to help reinforce it.

Thus it is the meta-property of Moore's Law (earlier referred to it as a meta-law)—more precisely the regularity of technical advance—that underpins innovation efforts in semiconductors. As repeatedly stated, everyone within the semiconductor community understands their heritage and in some degree (in both large and small organizations, English-speaking or not, practical or theoretical) fashion their work toward advancing capability to the next level, thus validating again this phenomenon. This is the 'self-fulfilling prophecy' that is so often used to explain Moore's Law.

It is this variable—the public knowledge and acceptance of Moore's Law, the *consensus paradigm* for state-of-the-art semiconductor design and technology—that serves as the guiding principle or mission to be collectively sought. As will be shown, it is the institution of the industry Roadmap (i.e., ITRS) that accompanies Moore's Law and the innovation complex that helps *organize* innovation.

Although not theoretically addressed here, there is anecdotal evidence (much of it based on inputs from personal interviews with semiconductor industry members) that the pace established by Moore's Law (present capacity doubling every 18-24mos) is determined not only by the technology (physics), but by social forces such as the human capacity to acquire, learn, and

communicate new knowledge; the rate at which R&D investment is made; and probably most importantly the coordination or alignment requirements to bring any given change about.

As in any production process, fashioning and installing new tools (physical capital) provides the means to increase output more productively. Tool-making has become a highly coordinated activity in semiconductors due to all the dependencies involved. Required investment levels now in the billions of dollars to produce each new device generation in essence requires entire new facilities of which each must be equipped with *all* of the necessary tooling. Missing one small tool runs the risk of idling the entire facility.[166]

Timing becomes critical. Having tools available precisely when needed—not too early, not too late (some refer to this as the 'Goldilocks' principle)—is essential to success. Here is where the Roadmap comes in. Specifically, the 15yr timing window attempts to portray the most practical route (and schedule) to take, given the best knowledge available while considering technical and economic limitations of the industry. Hence, the Roadmap is *always wrong in retrospect* as old problems are solved and new problems continue to emerge.[167] New knowledge alters the Roadmap in the same fashion as a map of an area becomes much more granular with time as travelers' understanding (knowledge) is increased.

Thus organized innovation, to a great extent a decentralized process, does have at its core a common purpose to which participants subscribe. This helps explain the gradual globalization of the industry, where such coordination is more complex, yet more necessary. Interestingly, Angel (1994), in studying the aftermath of the 1980s international competitive crisis, observed an important trend almost in anticipation of the *International* Roadmap and the globalization of many research consortia:

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[166] Turner Hasty, telephone interview, May 10, 2000. Hasty recalls as a prime example a new Intel fab that had cost close to three-quarters of a billion dollars and sat idle for 18 months because of unavailable equipment.

[167] Andrew Kahng, telephone interview, February 15, 2002. Kahng also points out that the sociology of the Roadmap inherently causes it to be beaten, "thus it's always wrong!"

> It has become clear that emergent manufacturing forms are characterized by a profoundly different mix of global competition and cooperation than that which characterized semiconductor production through the mid-1980s. The new institutional structure of innovation and technology development in semiconductors involves a complex array of international cooperative alliances and research agreements among U.S., Japanese, and European firms.[168]

A Proposed Model for Semiconductor Innovation

Numerous elements contribute to the pattern of organized innovation offered here. From Chapter 3, increasing complexity, self-organization, emerging standards are but a few factors. From this chapter, the evolutionary nature of both the technology and economics supporting it, learning and accumulated knowledge, so-called limits, globalization, and Moore's Law round out this list. Subsequent chapters will elaborate on these factors, however for now Figure 4-20 presents a model that embodies the key functions and organizations that collectively contribute to continuous innovation. Note that the Roadmap (ITRS) serves as a central institution to such *organized innovation*.

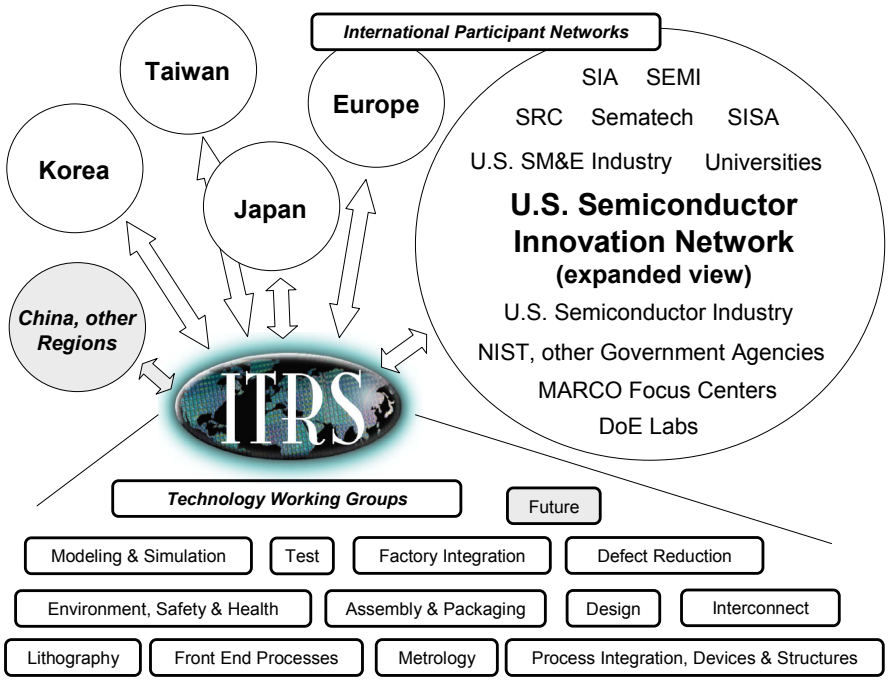

Figure 4-20: Organized Innovation Model

[168] David P. Angel, Restructuring for Innovation: The Remaking of the U.S. Semiconductor Industry, New York: The Guilford Press, 1994, 7.

In closing, to bring the subject full circle Ziman and contributors (2000) remind us that "technological change is, above all, a social phenomenon… Indeed, the same holds true for any evolutionary system."[169] The authors further elaborate, emphasizing an earlier point about evolutionary epistemology—that 'memes' are the hereditary carrier of technological change, but require examination within a cognitive and social context:

> What we have found, indeed, is that 'memes' are major players—perhaps *the* major players—in technological change. From an evolutionary point of view, material artefacts cannot be considered in isolation from their cognitive and social correlates… The collectivization and institutionalization of invention in the twentieth century is only the latest in a sequence of transitions to new technological regimes, where artefacts, knowledge, organizations and individuals take on new configurations and where even the basic evolutionary processes identified by Donald Campbell enter into new relations.[170]

Studying the Roadmap and the broader semiconductor innovation network is such an attempt toward a better understanding of this unique form of technological innovation.

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[169] Ziman (ed.), 2000, op. cit., 312, italics in original.
[170] Ibid., 314-5.

CHAPTER 5: Research Design

"If we knew what it was we were doing, it would not be called research, would it?"

- Albert Einstein

"If scientific reasoning were limited to the logical processes of arithmetic, we should not get very far in our understanding of the physical world. One might as well attempt to grasp the game of poker entirely by the use of the mathematics of probability."

- Vannevar Bush

This is a comprehensive study of a unique aspect of technological innovation in the semiconductor industry. The unit of analysis is the International Technology Roadmap for Semiconductors (ITRS). For this examination, a qualitative research design is used. The research design is a two-pronged strategy: (1) historiography and (2) case study method. The research type is inductive within the tradition of grounded theory (Glaser and Strauss, 1967), which affords an opportunity to build theory that offers significant explanatory power from the evidence gathered. Each of these three approaches—historiography (the past), case study (the present), and grounded theory (implications for the future)—is complementary to the overall research design and intended to help establish face validity of the study. All three methods are briefly discussed below.

Historiography

Preliminary research into this field by the author affirms that in the semiconductor industry, "history matters." *Historiography* is the method of doing historical research or of gathering and analyzing historical evidence. (Neuman, 2000:395) There have been numerous retrospective examinations of both semiconductor technology and the semiconductor industry. (Kleiman, 1966;

Golding, 1971; Braun and Macdonald, 1978; Hazewindus and Tooker, 1982; Dosi, 1984; Gilder, 1989; Morris, 1990; Riordan and Hoddeson, 1997) All of these (and more) historical studies cover at least one of the most celebrated historical events that so clearly define this industry: the paradigmatic "Big 3" inventions, of which the first two garnered Nobel prizes, while the third endowed the inventing firm with enduring economic rewards:

1. the transistor at Bell Labs in 1947-48
2. the integrated circuit (IC) at TI and Fairchild in 1958-59
3. the DRAM and microprocessor at Intel in 1970-71

Each treatise is a deserving work in its own right. Although each takes a distinctive historical approach based on the particular research angle, there is a common theme that these breakthrough products helped spawn a broader *revolution* or *transformation* that is so characteristic of the Schumpeterian (1950, 1934) tradition of innovation and technical change, as well as Kuhn's (1970) and subsequently Constant's (1973, 1980) respective interpretations of scientific and technological revolutions.

There is varying coverage of less-recognized *process innovations* in semiconductor production, but these are not featured as major themes by any of the aforementioned authors. A complete listing of process innovations would be considerably longer and in fact could not really be fully documented because of the less visible nature of these advancements. As previously mentioned, Nobel prizes do not apply here. A few of the most notable process innovations have been examined by academic authors (Tilton, 1971; Steinmueller, 1987; Henderson, 1988; Bassett, 1998). These include: the selection of silicon over germanium as a substrate material by Texas Instruments and Bell Labs and in the early 1950s, the diffusion and oxide masking processes pioneered by Bell Labs that led to the planar process developed by Fairchild in the late 1950s, CMOS technology introduced by RCA in the 1960s (again, based on earlier MOS research at Bell Labs and at other firms), silicon gate technology introduced by upstarts Mostek and Intel in the late 1960s, and the numerous advances in photolithography scanner and stepper

technologies that occurred in the 1970s by an entirely new semiconductor *equipment* industry. There is little debate that each of these has had a significant impact—both technically and economically—perhaps more so than any of the three product innovations previously mentioned. It could be argued that in semiconductors, process innovations contribute far more to technological progress than product innovations. It is from these process innovations that Moore's Law and later the Roadmap emerged as important institutions within the semiconductor community.

Thus, this study concerns itself with process innovations in semiconductors. More precisely this research examines as its major focus one particular *process* of process innovation, namely the industry Roadmap. It will be illustrated that the Roadmap grew out of an industry that recognized early on the unique economic benefits of semiconductor technology that could be advanced in a relatively regular pattern through intensive application of process innovations. Moreover, the design characteristics of the base technology—bulk planar CMOS (Complementary Metal-Oxide-Semiconductor)—that came to dominate the industry, demonstrated an exponential rate of performance enhancement, dubbed "Moore's Law," that was clearly unprecedented.

To suitably explain this phenomenon several historical sources have been investigated. As mentioned, the origin and evolution of Moore's Law as a *consensus paradigm* is thoroughly examined. Likewise, the origin and evolution of technology roadmaps and roadmapping practices including extensive research into Motorola's practices is also attempted. Further, a detailed historical review of the Roadmap process including a longitudinal thematic survey of the series of five SIA Roadmap editions (1992, 1994, 1997, 1999, and 2001) has been conducted. These have been supplemented by pertinent literature and other archival review to aggregate pertinent characteristics. For example the SRC, Sematech, and the general role of research consortia are briefly examined within this framework.

Finally, the fact that semiconductor histories seem to be appearing less frequently may suggest something about the life-cycle of the industry and/or the changing nature of technological innovation. The Roadmap might have a role in this as incremental process innovations become increasingly diffused throughout the global semiconductor community. Interestingly, the industry is long due for another "big" invention. It has now been 30 years (which is several life times in semiconductor years) since the DRAM or microprocessor—the last big invention—was introduced. This fact underscores the importance of process innovations to the semiconductor industry's continued success. Writing in 1977, Lester Hogan underscored the importance of one of the crucial process innovations, the planar process:

> The planar process introduced in 1959 [has] become the pillar of the entire industry since that time.[1]

Twenty-five years later, planar remains the dominant fabrication process that supports a much larger and diversified global semiconductor industry.

Case Study Methodology

For this examination, a qualitative research design using a case study strategy following the tradition of Yin (1994, 1981) is employed. Yin defines the case study as a research *strategy* likened to alternative research strategies such as an experiment, a history, or a simulation:

> As a research strategy, *the distinguishing characteristic of the case study is that it attempts to examine*: (a) a contemporary phenomenon in its real-life context, especially when (b) the boundaries between phenomenon and context are not clearly evident.[2]

This study examines the Roadmap as a single, comprehensive case in the belief that an in-depth examination of one industry roadmap—considered by many as the *model* roadmap—can yield more insights than a less detailed study of a number of industry roadmaps. The researcher followed Yin's expanded definition of the case study as combining multiple data sources of

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[1] C. Lester Hogan, "Reflections on the Past and Thoughts About the Future of Semiconductor Technology," *Interface Age*, March 1977, 29.
[2] Robert K. Yin, "The Case Study Crisis: Some Answers," *Administrative Science Quarterly*, Vol. 26, Iss. 1, March 1981, 59, emphasis in original.

evidence. Indeed, numerous sources of data were used in this research including an extensive review of pertinent literature, archival records, personal interviews (telephone and face-to-face), and some observation. Each of the data sources is briefly discussed.

- *Literature and archive review:* The researcher obtained or had access to a wide variety of sources including: all SIA Roadmap editions and updates (1992-2001); Micro Tech 2000 Technology Workshop Report (1991) and related NACS documents; Sematech archives dating back to 1987; SRC newsletters (1983-1996) and other archival records; press coverage of the Roadmap dating from 1991; and numerous reports, studies, and other dissertations dating back into the 1960s. These sources are identified throughout this study.
- *Personal interviews:* Since interviews are the key source of primary data, an extended explanation is offered below for more information.
- *Observation:* The researcher attended three ITRS-related meetings (1998 ITRS Update Workshop, December 1998; 1999 ITRS Domestic Assembly & Packaging TWG Meeting and Domestic Workshop, June 1999; 1999 ITRS Roadmap Workshop, July 1999) along with the NEMI 2000 Roadmap Workshop, June 2000.

In sum, the case study method along with the variety of data sources enabled the researcher to examine the Roadmap process *in situ* or 'as it happens'. The timing for the start of field work (Spring 1999) was advantageous as it coincided with the development cycle of the 1999 ITRS, the first full-fledged *international* roadmap. This turned out to be a very useful entry point into a dynamic and adaptive roadmapping process that emerged in small organizations (within individual firms) and broadened its scope evolving from firm level, then to industry level, and ultimately to international level.

Grounded Theory

In *grounded theory*, a qualitative researcher begins with a research question and little else, approaching the object of study free from any theory or preconceptions. Theory actually develops during the process of field study and data collection and is shaped with comparisons to existing theory. As more empirical data is gathered, theory emerges iteratively until it is saturated. This more inductive method means that theory is built from data or "grounded in the data." (Neuman, 2000:145-6) Glaser and Strauss (1967) argue that it is the intimate connection with empirical reality that permits the development of a testable, relevant and valid theory. Eisenhardt (1989) describes how theories are built specifically from case studies, stating:

> The central idea is that researchers constantly compare theory and data—iterating toward a theory which closely fits the data. (1989:541)

This research is such an attempt. One example of grounded theory application in this research is the interesting phenomenon expressed by interviewees as 'beat the roadmap' behavior. This unique behavior, shared by individual semiconductor community members, underpins the technology acceleration phenomenon, thus helps explain why the industry continues to sustain Moore's Law. As one 1999 ITRS participant states:

> Some companies, interestingly enough, use the Roadmap as a stalking horse. It's sort of a target that they can surpass, the 'beat the roadmap' behavior—an interesting sociological phenomenon.[3]

Within grounded theory the researcher sees micro-level events—such as this comment, also shared by most interviewees—as the foundation for a more macro-level explanation (i.e., technology acceleration). This methodology can be likened to the development of Sir Isaac Newton's theory of gravity, or Adam Smith's "invisible hand" theory of competitive markets, or perhaps the best example, Alexis De Tocqueville's interpretation of the institution of democracy in American society. Tocqueville's 1835 remarks are revealing:

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[3] ITRS survey respondent.

> I confess that in America I saw more than America; I sought there the image of democracy itself, with its inclinations, its character, its prejudices, and its passions, in order to learn what we have to fear or to hope from its progress.[4]

All three of these scholars, although from different disciplines (i.e., physics, economics, and sociology), induced their theories from unique observations and insights derived from relatively few and quite ordinary circumstances. Yet their theories carry almost universal acceptance after centuries of testing and validation. The theory of *organized innovation* attempted here is considerably modest by comparison, however the principles used to derive it are probably not that much different than in other applications of grounded theory. The remainder of this chapter addresses personal interview methods, classification, and data.

Primary Data Source: Personal Interviews

Personal interviews were a primary source of research data. At least eighty-five formal interviews were conducted over the course of this study, of which seventy-five were documented. Some candidates were interviewed more than once. There were also at least another twenty informal interviews or related discussions that were held but not documented. Thus the researcher spoke with more than one hundred people during the course of this study. Note that some paraphrasing and elaboration of personal interviews were necessary and are the responsibility of the author. In addition, the researcher had access through Sematech archives to sixteen in-depth interviews conducted by Larry Browning and Judy Shetler of the University of Texas in preparation for their book, *Sematech: Saving the U.S. Semiconductor Industry*, College Station, TX: Texas A&M University Press, 2000. Findings in these records along with other data sources were triangulated with the researcher's interview findings.

The nature and type of interviews changed over the course of the study consistent with the evolution and increased clarity of the research. Six unstructured exploratory interviews were conducted in 1996-97 in preparation for a paper by the author on Moore's Law that appeared in

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[4] Alexis De Tocqueville (translated by Henry Reeve), *Democracy in America*, New York: D. Appleton and Company, 1901, Author's Introduction.

the June 1997 issue of *IEEE Spectrum* of which a version reappears here as Chapter 8. As the dissertation topic formulated into a study of technology roadmaps, about ten roadmapping process-related interviews were conducted in 1998 and early 1999 including attendance at the *Technology Roadmap Workshop*, moderated by the U.S. Office of Naval Research (ONR) in Washington, DC on October 29-30, 1998. Another paper, co-authored with Ronald Kostoff of ONR in the May 2001 issue of *IEEE Transactions on Engineering Management* was to come from that—a summary version also reappears here as Chapter 2. This second set of interviews was more structured but still largely exploratory in nature. The remaining seventy-five interviews representing the bulk of the field work concerned semiconductor industry roadmapping practices in particular and were conducted between 1999 and 2002 with the most concentration between the Summer of 1999 and the Spring of 2000 coincident with the publication of 1999 ITRS (December 1999).

About two-thirds of these interviews were structured interviews guided by a survey instrument that was developed incorporating all nine hypotheses (and some sub-hypotheses) questions (see Appendix). The survey was co-developed, reviewed, and revised by Sematech in an iterative process until the final questions were approved for use. The iterative process between the researcher and Sematech helped increase face validity of the research instrument. The first instrument contained 36 questions of which ten questions related directly to hypothesis questions. There were another dozen or so questions that were evaluative of the Roadmap process (recommended by Sematech), and the remainder were background or demographic in nature.

Following the first few interviews—which also served as a field test of the instrument—a few questions were modified while a few were consolidated. Additionally it became clear that different user communities (e.g., research vs. supplier) had different needs, thus different perspectives of the Roadmap. So about six additional questions were added at the end and asked of three groups, where applicable. Three surveys, distinguished only by the last six questions were developed; they were for R&D, semiconductor materials and equipment (SM&E), and

international participants. The 30 or so core questions were not changed again and thus were common to all respondents.

Sematech provided a list of about twenty possible interview candidates to begin the field work. All but two from this prospective list were interviewed. Another thirty were interviewed as suggested by the first group of interviewees. In total, 50 people were interviewed with the assistance of the survey instrument. Of the 50 surveyed, not all answered all questions. Thus, finished surveys were categorized by level of completion. A survey was classified *complete* if the major components of the survey (i.e., Roadmap process evaluation questions and four research hypotheses) along with all but four (4) or less remaining questions (out of about 40) were answered. In some cases, not every remaining question was asked or answered due to time constraints and other factors (further discussed below). Twenty-five or 50% of surveys were considered complete. A *partial* survey meant that more than four questions were not answered; there were twelve or 24% partial surveys. Finally, some interviews of industry executives or former participants where the exact survey flow and line of questioning was inappropriate were labeled *context* surveys; there were also thirteen or 26% context surveys. (It would be appropriate to label these context surveys as *semi-structured interviews*.) In all cases, the survey instrument was used to guide these interviews in the same fashion as with any other Roadmap participant. The researcher made all contacts directly with the interviewees. Sematech was copied on all e-mail correspondence with the interviewees including any interview notes.

The length of responses ranged considerably. Twelve respondents elected to answer in writing (via e-mail); some providing very detailed answers while others gave one- or two-word answers. It quickly became apparent that time was critical to these respondents, so the researcher made the best use of each respondent's time, sometimes skipping selected questions or entire sections of the survey when necessary. The result is that 30 of the 50 respondents were able to provide statistical data, while the number of answers to the ten core hypothesis questions ranged from 21 to 33 with the average being 27 (see Appendix for detailed results).

One limitation of the instrument was the time needed to complete all questions. Completion of all questions was estimated at between 60 to 90 minutes depending on the depth of responses. Most respondents kept very busy schedules and when contacted, especially at work, could not devote this length of time to the survey.[5] When possible, a second or third follow-up call was made. When this proved infeasible, the researcher chose which questions to focus on given the allotted time. This is one reason the number of responses to questions varies. In terms of actual time involved, the shortest survey lasted about thirty minutes while the longest was more than three hours (spanning multiple phone calls). The average of all interviews was easily more than one hour.

Recognizing time limitations, respondents were asked to e-mail answers either before or after the interviews. As indicated, this was successful in a dozen cases. Additionally, when possible the researcher attempted to document interviews soon after completion. The draft transcript was e-mailed to the respondent (Sematech was copied) requesting review and comment. In most cases there was little to no reply. In a few cases the respondents provided changes and additional information including replies to previously unanswered questions. In sum, every reasonable attempt was made to obtain survey data to better inform this study, however the reality of *in situ* organizational research is very challenging.[6]

Selection of Survey Respondents

As previously mentioned Sematech provided an initial list of potential candidates as shown in Table 5-1.

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[5] Time zone differences also had to be accommodated, most notably with calls to Europe and East Asia.
[6] Typical of this type of research, there were numerous (about twenty) cases when the author attempted to contact potential survey candidates via telephone or e-mail only to not hear back. In these cases, the author attempted follow-up contact. After three attempted calls and/or e-mails to a candidate with no reply the author moved on to make other contacts. One particular case is worth noting. After two unsuccessful calls to an engineer at a major semiconductor equipment manufacturer, the researcher was finally able to reach the person. After a brief exchange the engineer stated that she had received previous messages and fully understood (and supported) the research, but said that the pressures of the then-current project packed her day so tightly that she apologetically said she had to go, wished me luck, and proceed to hang up.

Table 5-1. Sematech List of Interview Candidates

Name	Organization	Roadmap Function
Alan Allan	Intel	ORTC (Overall Roadmap Technology Characteristics) Coordinator
Karen Brown	NIST	Former Lithography TWG (Technology Working Group) Co-chair
Bob Burger	SRC (retired)	Former Roadmap Co-chair
Ralph Cavin	SRC	RCG (Roadmap Coordinating Group) member
Alain Diebold	Sematech	Metrology TWG Co-chair
Bob Doering	Texas Instruments	RCG and IRC (International Roadmap Committee) Co-chair
Paolo Gargini	Intel	RCG and IRC Co-chair
Jim Glaze	Lawrence Livermore Lab	Former VP, SIA Technology Programs (oversight)
Juri Matisoo	SIA	RCG member, SIA VP Technology Programs
Jim Meindl	Georgia Tech	RCG member
Larry Novak	Radian	ESH TWG Co-chair
Paul Peercy	Semi/Sematech (SISA)	RCG member
Bob Scace	NIST	RCG member
Steve Schulz	Texas Instruments	Design TWG Co-chair
Tom Seidel	Genus	Former Roadmap Co-chair
Court Skinner	SRC	Factory Automation TWG Co-chair
Bill Spencer	Sematech	Chairman of the Board, former CEO (oversight)
Larry Sumney	SRC	President (oversight)
Peter Verhofstadt	SRC	Former Design & Test TWG Co-chair
Werner Weber	Infineon	IRC member
Don Wollesen	AMD	RCG member

Source: Linda Wilson e-mail to author, July 22, 1999.

The rationale behind this list was to interview a representative sample that covered a variety of Roadmap leadership and technical functions. Note the large share of candidates with IRC, RCG, or TWG assignments; five separate TWGs were included in the list to ensure variety of perspectives. Further examination of this list reveals the following demographic distribution by

type of organization: 8 consortium, 7 chipmakers (including SIA), 3 government, 2 suppliers, and 1 university. Part of the reason for the large share of consortium candidates was the practical consideration of access; consortia personnel might be more accessible for this research than industry (chipmaker and supplier) personnel. As the interviews got underway it became evident that more representatives from industry, especially from the supplier community, needed to be included. An implicit goal was to try to approach a sample distribution that resembled the 1999 ITRS Membership demographics (the 1999 ITRS was then in progress): 45% chipmaker, 27% supplier, 14% consortium, 8% university, and 6% government. (Sematech, 2002)

At the request of the author, Sematech provided additional possible interview candidates from the international community while Semi/Sematech (now SISA) furnished potential names from the supplier community. As the interviews proceeded the researcher made a conscious attempt to bring this distribution as close to the 1999 ITRS membership distribution to increase the validity of the sample. In the end, the distribution of the 50 interviews seemed to correlate fairly closely (see Table 5-2). This is even more the case when the category 'Analyst' is excluded from the total.[7] Excluding the 'Analyst' category, note that the large share of Research Consortium was really the only anomaly when comparing against 1999 ITRS Membership demographics, and this is because this category made up the leading share of the initial interviews.

[7] 'Analyst' refers to a respondent who did not directly participate in the Roadmap process, but was a Roadmap user and provided some analytical insight regarding the Roadmap (e.g., industry analyst or technical journalist).

Table 5-2. Demographic Comparison of Survey Respondents and 1999 ITRS Membership

Function	# surveys (n=50)	% of total	% of total w/o Analyst	1999 ITRS Membership*
Chipmaker (including 5 international respondents)	15	30%	35%	45%
Research Consortium (SRC, Sematech, and international consortia)	12	24%	28%	14%
Supplier (including 1 international)	9	18%	21%	27%
Analyst (including consultants)	7	14%	excluded	0%**
University	4	8%	9%	8%
Government (agencies and labs)	3	6%	7%	6%

* Source: Excel attachment from Linda Wilson e-mail dated February 27, 2002.

** referred to as "Other" in 1999 ITRS Membership demographics

Responses from international members should be pointed out. The researcher's six international interviews represent 12% of the total and include input from each 1999 ITRS participating region outside of the U.S.: Europe, Japan, Korea, and Taiwan.

One final point on demographics of the sample is the extensive experience level of the survey participants. The 28 respondents who furnished statistical data claimed a grand total of 173 total years' involvement in semiconductor industry roadmaps. The average involvement for all respondents was 6.9yrs. While one respondent had only been involved for 1yr, another had been involved for 14yrs.[8]

Sample Size and Validity

Since this is a qualitative study, the determination of sample size as a statistical means of establishing validity does not apply in the same way as it would in a quantitative study where some form of random sampling technique were used. However, validity was affected positively by the sample size of interviews conducted by the researcher. Since the survey was aimed primarily

[8] See Q2 detailed results in Appendix.

at Roadmap participants, the study population would be the total number of participants in the 1999 ITRS, of which there were approximately 325[9] technical contributors acknowledged in the front of the Roadmap. Given this population, or even a more realistic population of 275-300,[10] a sample of 50 represents is at least a 15% sample size.

This must be weighed against the fact that not all surveyed for this study participated in the 1999 ITRS. Three-quarters of the respondents (38 of 50) did participate in the 1999 ITRS. Further, 100% of the respondents who provided statistical data claimed their involvement as *active* or *very active*.[11] *Active* meaning they attended TWG meetings and the annual roadmap workshops, and often presented as TWG Chairs or in some other capacity. In all cases, the survey respondents claimed that the Roadmap was an important part of their professional life (note that all Roadmap activity is voluntary). Respondents claimed that involvement in the Roadmap process outside of the formal workshops was significant, ranging from 5% to 75% of their time, with an overall average of 18%.[12] The author also attended a U.S. TWG workshop (Assembly & Packaging) and both the U.S. and International Roadmap Workshops in the summer of 1999 where he counted approximately 150 attendees at most; these could be considered "active." Thus a sample size of at least 20% of active 1999 ITRS participants seems a reasonable estimate.

Moreover, validity is also affected positively by the nonprobability sampling technique chosen for the interviews. The sampling technique used could best be described as a combination of purposive and convenience sampling as defined by Sekaran (1992:235-6):

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[9] This is an estimate since several contributors appear in two (or even more) cases.
[10] Note that more than 100 (almost one-third of the total) are listed as International Technology Working Group (ITWG) representatives. ITWGs were formed expressly for the 1999 ITRS, the first full-fledged *international* industry Roadmap. It is probably safe to say that many of these ITWG members were not yet truly active in the process, but this could not be identified by the researcher. In any case this group (ITWG representatives) was not seriously considered when selecting interview candidates.
[11] 61% claimed very active, 32% active, and 7% in between. See Q4 detailed results in Appendix.
[12] See Q6 detailed results in Appendix.

- *Purposive sampling* is used to obtain information from specific targets—that is, specific types of people who will be able to provide the desired information, either because they are the only ones who can give the needed information, or because they conform to some criteria set by the researcher. Two types of purposive sampling offer further definition. *Judgment sampling* involves the choice of subjects who are in the best position to provide the information required based on their unique knowledge, skills, and experiences in the subject being investigated. *Quota sampling* is a form of proportionate stratified sampling, in which a predetermined proportion of people are sampled from different groups, but on a convenience basis.
- *Convenience sampling* involves collecting information from members of the population who are conveniently available to provide this information.

Applying these methods to the Roadmap interviews, the initial list of interview candidates as determined by Linda Wilson, the ITRS Information Manager, would be considered purposive sampling while incorporating elements of both judgment and quota sampling. The researcher then used convenience sampling to expand the list of candidate interviewees, however within the implicit demographic boundaries discussed earlier. The resultant interview list thus reflects a deliberate attempt at proportioning the sample according to the broader population, albeit with some limitations as previously discussed. In sum, every reasonable attempt was made by the researcher to obtain as complete and valid a picture about the Roadmap process as possible.

This concludes Part One. With this basis for both a theoretical understanding and research design for this study, we now turn to the historical basis for these key ingredients in an attempt to show how this has occurred and thus suggest how this might continue. The next part of the dissertation (Part Two) is a substantial historical coverage of the evolution of the IC industry, the microprocessor, Moore's Law, and the antecedents of the Roadmap. Mostly descriptive in content, the information is presented in a manner that helps give added meaning and context to the theoretical concepts advanced in Chapters 3 and 4 of Part One.

PART TWO: HISTORY

CHAPTER 6: History and Evolution of Integrated Circuit Innovation

> "In contrast to the invention of the transistor, this [integrated circuit] was an invention with relatively few scientific implications… Certainly in those years, by and large, you could say that it contributed very little to scientific thought."
>
> - Jack Kilby[1]

> "This was the first planar transistor. This gave us something that was very important, and [Bob] Noyce recognized this. In fact, what happened interestingly enough, when we were patenting this we recognized it was a significant change, and the patent attorney asked us if we really thought through all the ramifications of it. And, we hadn't.
>
> So Noyce got a group together to see what they could come up with and right away he saw that this gave us a reason now you could run the metal up over the top here without shorting out the junctions, so you could actually connect this one to the next-door neighbor or some other thing. And then he also came up with the idea of how you could put extra junctions in here to electrically isolate the thing."
>
> - Gordon Moore[2]

The two opening quotes emphasize the importance of technology—more than science—that contributed to the invention of the integrated circuit (IC). The invention of the IC stands taller than any other that followed the transistor a decade earlier and in recognition of its importance, Jack Kilby, the co-inventor of the IC, was awarded the Nobel Prize in Physics in 2000. Remarkably, Bob Noyce, the other co-inventor, and his staff had not realized the full significance of their development until a patent attorney asked them to reconsider their application. The invention of the microprocessor, the industry's other seminal discovery, also involved no science and included a strong element of serendipity as Busicom's calculator design request of Intel certainly wasn't for a general purpose microprocessor. Moreover, it wasn't even patented (see Box 3-2 and Chapter

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[1] Jack Kilby, quoted in Ernest Braun & Stuart Macdonald, *Revolution in Miniature: The history and impact of semiconductor electronics re-explored in an updated and revised second edition*, Cambridge: Cambridge University Press, 1982, 90.
[2] Gordon E. Moore, personal interview, June 13, 1996.

7). These stories are typical of many in industry lore, however as discussed in Chapter 4 this is an industry that relies more on advances through incremental rather than radical innovation. Most of these small (and some large like the microprocessor) improvements are not patented, and those that are may follow a similar process as the discovery of the IC.

The purpose of Part Two of this study is to provide essential historical background and context to help support the concepts put forth in Part One. Chapters 6, 7 and 8 review important elements of industrial history that have shaped the innovation process while Chapter 9 examines the parallel development of technology roadmaps as a strategic planning tool. As will become more evident the current Roadmap is derived from innovation practices and patterns that formed early on. In many ways the ITRS—the subject of Part Three—continues this heritage. The material in Part Two is organized as follows. Chapter 6 provides a brief history of innovation in the IC industry as background. This is by no means an exhaustive historical treatment of the IC industry. The literature is rich in historical studies (see the historiography reference list at the beginning in Chapter 5). Instead, particular elements that would become critical to the success of the industry are highlighted and discussed (e.g., MOS technology). With this background Chapter 7 revisits the all-important invention of the microprocessor as a mini-case study that examines the broader context of IC innovation in the late 1960s and early 1970s. The result is a more complete rendering that demonstrates the collective nature of innovation. Chapter 8 studies Moore's Law as a phenomenon that emerged early and gradually enabled this industry to operate on a time-based cadence, eventually becoming the chief planning assumption for the Roadmap. One theme that runs through this early history is that an implicit time-based roadmap emerged (later dubbed Moore's Law) around which innovation occurred. Finally, Chapter 9 examines early technology roadmaps and roadmapping practices in semiconductors where this implicit innovation pattern was captured and codified with increasing frequency and scope. Together Chapters 6 through 9 form the historical basis of this dissertation.

Brief History of Semiconductor Industry Innovation

To place this research in context, the following paragraphs provide a brief account of the industry's history through the 1990s, highlighting key events and milestones. Note the high risk of missing something important in summarizing in this fashion. This section is followed by a discussion of a few of the more appropriate inventions or innovations that concern this research. Again, the two chapters that follow expand on the invention of the microprocessor and Moore's Law in far greater detail.

1950s

The decade of the 1950s was the early, experimental, discreet transistor era where innovation occurred by trail-blazing individuals utilizing scientific knowledge furnished by large, vertically-integrated electronic equipment manufacturers, especially AT&T's Bell Labs but also RCA, GE, Sylvania, and others. Many of these large electronic systems houses were also leading manufacturers of receiving/vacuum tubes (valves), the antecedent technology. Newly discovered solid-state technology launched the U.S. semiconductor industry, consisting of but four firms in 1951 and growing rapidly to twenty-six by 1956. By 1957 the new firms—firms with no experience in the receiving tube industry—had captured 64% of the total semiconductor market.[3]

As expected, both the technology and the young industry could best be described as unstable. This was a time when rudimentary, trial-and-error manufacturing methods were developed in a true form of "black art" as the development lab and production facility were often one in the same. Semiconductor production was empirically determined by engineers, chemists, physicists, technicians, and the like working in very crude environments compared with today's ultra clean rooms. All this experimentation resulted in very unpredictable production runs with

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[3] Ernest Braun, "Transistor to Microprocessor," in Tom Forester (ed.), *The Microelectronics Revolution: The Complete Guide to the New Technology and Its Impact on Society*, Cambridge, MA: The MIT Press, 1983 (first published 1980), 74.

single-digit production yields as the norm.[4] The science underlying semiconductor technology was not well understood, so advances in technology, specifically process technology, were needed to improve production methods and, in turn, develop a viable semiconductor industry. A wide gap existed between semiconductor theory and manufacturing practice; mastering the fabrication process became a critical skill. This view is captured by John Tilton:

> I think it's very important in this industry to differentiate between the ability to produce a new device in the laboratory and the ability to produce the thing in scale at competitive prices. Now the former was really much easier. The people who made money really did the difficult task which was producing these things in large quantities at very low prices. I think you have to look at that as two different problems.[5]

Thus, the direction of semiconductor development during the 1950s was determined not so much by the desire to make better devices as by the desire to find better ways of making them. It was the power of process over product which has since determined so much of the course of semiconductor electronics.[6] Gordon Moore, who started in the industry during this time, recalls the important and unique role of technology in the early stages, "Indeed, the technology led the science in a sort of inverse linear model."[7] As for materials, germanium first dominated as the *semi*conducting material of choice, but by the mid to late 1950s silicon became increasingly used, especially in high-performance applications. As the industry searched for the right business model, profits were mostly non-existent as most output was produced by newly-created divisions within large electronic systems houses.[8]

Important background events occurred in the late 1940s—both involving AT&T—that would profoundly shape the direction of the nascent semiconductor industry in the 1950s. The first was

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[4] Production yield refers to the percentage of good output from a process step. Since chip fabrication involves multiple processes, final device yields can be (and indeed were in the early days) very low.
[5] John Tilton, quoted in Braun & Macdonald, op. cit., 54.
[6] Ibid., 73.
[7] Moore interview, op. cit.
[8] RCA, Sylvania, GE and Raytheon, who represented roughly three-fourths of the receiving tube industry sales at the time, were among the first companies to produce transistors. However, in their attempt to switch to semiconductors, the burden of the huge technology commitment to the device the transistor would ultimately replace, none ultimately succeeded in the transition. Note that the Bell Labs researchers who discovered the transistor effect were working on a viable replacement for the receiving tube; recall that AT&T (Western Electric) was a user rather than a producer of receiving tubes.

the 1947 discovery—and 1948 demonstration and publication—of the transistor by three scientists at Bell Labs.[9] They were later awarded the Nobel Prize in 1956. The other critical event was an antitrust case brought against AT&T in 1949 that resulted in a 1956 consent decree preventing AT&T (including Bell Laboratories, Western Electric, and its other subsidiaries) from competing outside its basic telecommunications markets.[10] Thus they were barred from commercially selling semiconductor technology products. They were further directed to license all existing patents to domestic firms royalty-free, and to foreign firms for a nominal fee. The Bell Labs' patent licensing practice set an early tone for a more open attitude toward licensing and fostered a common practice of licensing and cross-licensing among manufacturers. One drawback of this was that individual firms' intellectual property was not easily protected, however the industry more broadly established a pattern of knowledge sharing that was vital to continued innovation.

The first license takers were not solely the large electronics systems houses. One of the new players was Texas Instruments (TI), a small geophysical firm in Dallas that provided oil well services.[11] TI would rapidly absorb the technology and contribute significantly to its early advance (e.g., proving silicon as a more suitable substrate material). Another early taker was a then-unknown, Japanese equipment company called the Sony Corporation[12] that succeeded in the first widespread commercial application of the semiconductor, introducing a pocket transistor radio by the mid 1950s. The hearing aid was another early consumer product application that took advantage of the transistor's small size. By the late 1950s the seeds of a new *merchant* industry were being sowed with start-up firms like Fairchild Semiconductor in California. By and large, the

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[9] The transistor grew out of work in solid-state physics that had produced semiconducting point-contact diodes in the late 1930s, but was partially suspended due to World War II.
[10] In exchange, AT&T retained its natural monopoly status and was not broken apart.
[11] TI was first known as Geophysical Services Inc. when incorporated in 1930. In 1951 Gordon Teal was hired away from Bell Labs to set up semiconductor operations and the company name was changed to Texas Instruments reflecting the company's new mission.
[12] Sony was first known as Tokyo Telecommunications Engineering when formed in 1946 just after the end of WWII.

1950s represented the great experiment to commercially 'make a go' of a promising new technology.

The late 1950s also brought two pivotal developments that carried great influence. The first was technological, and perhaps the single most important contribution ever to the industry. This, of course, was the invention of the *integrated circuit* (IC) by Jack Kilby at TI and Robert Noyce at Fairchild.[13] The IC was fundamentally different than its discreet component predecessor; ICs encompassed entire circuit functions such as signal amplification, logic, and memory, thus becoming a much larger building block than the discreet transistor. With greater density and more complexity, the IC could now represent a larger portion of the total value of the end products into which it was incorporated.[14] The IC was made possible through significant advances in process technologies (e.g., the oxide masking and diffusion method and most importantly, the planar process) that enabled batch processing, thus mass-manufacturing of semiconductors. The introduction of the IC and improved process technologies changed the basic economics of the industry, enabling merchant semiconductor manufacturers to develop capability both forward and backward.[15]

The second major event was the Soviet Union's successful launch of Sputnik in 1957 which served to heighten Cold War tensions and thus increase U.S. Government spending on national security interests. Miniaturization in weapons systems had been a priority by the U.S. military throughout the decade including such programs as the Navy's Tinkertoy (1950, based on receiving tubes), Army Signal Corps' micromodule plan (1957), Diamond Ordnance Fuze

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[13] Kilby's 1958 discovery actually preceded Noyce's by a few months (in 1959), however Noyce's device design proved much more practical, and thus was adopted for manufacture. After years of dispute, both were awarded the patent and are recognized as co-inventors of the IC; see Braun & Macdonald, op. cit.
[14] U.S. Department of Commerce, Industry and Trade Administration Office of Producer Goods, *A Report on the U.S. Semiconductor Industry*, Washington DC: USGPO, September 1979, 11.
[15] The industry's largest producers of chips were so-called *captive* manufacturers (i.e., Western Electric, IBM, and later others) who saw the importance of the new devices to their end-use applications (i.e., communications, computing, etc.). Further, in the late 1960s and early 1970s as broader acceptance of IC-based consumer goods took place, some *merchant* chip makers (e.g., TI and Intel) jumped into full-scale development of pocket calculators, digital watches, and other consumer products. The IC expanded the scope of chip design that enabled this evolution to occur.

Laboratories' (DOFL) microcircuits program (1957), and the Air Force molecular electronics program (1959).[16] Follow-on efforts would continue well into the 1960s, thus most of the initial demand for U.S. semiconductor products came from the military and later NASA.[17] Performance, not price, was the chief concern. This guaranteed market, albeit short-lived,[18] gave the fledgling industry the financial means to invest and grow. This point, among others, is acknowledged in Box 6-1.

Box 6-1. *Business Week* Special Report on Semiconductors, 1960[19]

The March 26, 1960 issue of *Business Week* contains a 21-page special report on "Semiconductors" that represents one of the first broad assessments outside of the electronics trade press concerning the new technology and young industry. The article opens with a statement, "The industry's story is an exciting drama of breakthrough after breakthrough—by perhaps the fanciest assembly of brains any business has ever known." The 'breakthrough after breakthrough' assertion summarizes the normal innovation pattern that continues to define this industry. The following article excerpts provide an important glimpse of the major challenges facing the industry at the time. While the industry has certainly changed in many ways over the four decades since, some of the same factors—including 'breakthrough after breakthrough' innovation—still apply more than forty years later.

- This year [1960], transistors and kindred devices are selling at an annual $500-million clip, and there are predictions of a $1-billion rate by 1963… making semiconductors the dominant force in the $10-billion electronics industry…
    - The military now gives the new industry about half its sales volume…

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[16] Herbert S. Kleiman, *The Integrated Circuit: A Case Study of Product Innovation in the Electronics Industry*, D.B.A. Dissertation, Washington, DC: George Washington University, 1966.
[17] Federal Trade Commission, *Staff Report on the Semiconductor Industry: A Survey of Structure, Conduct, and Performance*, Bureau of Economics, January 1977, Table III-3, 60. Note that almost one-half of all U.S.-produced semiconductors (including discreet components) were purchased by the U.S. Government in 1960. All IC production in 1962 was consumed by the U.S. military; in 1965 over 70% of U.S.-manufactured ICs went into defense and space applications.
[18] By 1973 overall U.S. Government purchases of semiconductors had dropped dramatically to less than 10% of total U.S. production, although military IC demand share remained in double-digits through the mid 1980s.
[19] "Special Report on Semiconductors," *Business Week*, March 26, 1960, 74-121 (21pp).

- This pattern of innovation, profit, imitation has made continuing innovation all the more vital to the young industry…
- [U]nit prices in any established line tend to fall a disconcerting 30% a year…
- The most promising new type of diffused base transistor … a mesa. An etching process during production leaves little mounds that look, under a microscope, something like the flattened hills of the Western deserts. The name caught on.
    - The first diffused base transistor was manufactured by Western Electric. The first to be generally marketed was … introduced by Texas Instruments in the spring of 1958.
    - The first silicon transistors of the new sort came from Fairchild Semiconductor Corp… which, largely on this one product, built sales from less than $500,000 in 1958 to about $7-million in 1959…
- Turning out a transistor with most present techniques takes much delicate handwork of a sort to which women seem best adapted. Currently, more than 80% of the industry's 40,000 employees are women.
- When technology changes as fast as it does in semiconductors, it's much cheaper to retrain workers than to rebuild expensive automatic machinery. This is a patent argument against extensive mechanizing…
- It's nothing new for a new product to bring a high price at first and a low one later. The first ball-point pens, for instance, cost the customer $15; now you can buy a ball-point—and a better one, at that—for a quarter. In just the same way, junction transistors dropped from $100 to about 50¢.
- Two Flourishing Independents:
    - Texas Instruments leads the industry in sales, and in technology it's considered second only to Bell. In 1959 it scored net sales of $193 million, about half attributable to its broad product line of semiconductors… This compares with 1947 sales of less than $5-million, almost all of it from performing geophysical services—the business in which the company started.
        - TI, typical of the industry, has spent lavishly for research and development—$30 million in 1959, half from its own funds and the other half contributed by the federal government for special projects. All in all, 1,400 of the Semiconductor-Components Div.'s 6,000 employees devote full time to research, product development, engineering support, and patents.
        - The company also has a unique production engineering group numbering nearly 500, which builds almost all TI's production equipment…
        - Texas Instruments has built an extensive silicon plant to supply its own needs and also, it hopes, to supply others.
    - Transitron was founded in 1952 by the brothers Leo, and David Bakalar… By 1954, the new company was in the black… In the fiscal year ended last June [1959], Transitron's sales were $30.9-million, net income after taxes nearly $6.5-million. In sales, it's second only to TI among independents and in a neck-and-neck race with General Electric for the No. 2 spot in the industry over-all.
- The Richest Promise … Wrapping Packages—Probably the most important of all developments is the work in circuit function packages—wrapping the entire works of something like a radio into one tiny, utterly dependable chunk…

- The Army Signal Corps microminiature module, for which RCA holds the prime contract.
- "molectronics," demonstrated by Texas Instruments and Westinghouse and under development in many other labs…
- Doubts and Rebuttals—Many engineers still doubt that circuit function packages will ever be economically practical. But most in the industry disagree. A Texas Instruments engineer [possibly Jack Kilby] describes how his company can use a single crystal of silicon for a device that would have formerly been made up of more than a dozen components costing $100 in all. "It's not only more reliable," he says, "eventually it will be considerably cheaper." …That single silicon crystal is no bigger than a match head, but it contains the guts of a two-tube radio.

1960s

Still in the introductory stages of the industry's life cycle, the 1960s are remembered as a time of rapid growth along with the emergence of some industrial definition and stability. By 1963 more than 100 companies had plunged into the U.S. semiconductor industry with total shipments valued at $687 million (an industry downturn in 1961-2 kept total revenues from reaching the $1 billion *Business Week* projection). By 1972 there were 325 firms involved in semiconductors with total industry sales of almost $2.7 billion.[20] One lesson the industry learned early on was its cyclical nature during economic swings, especially downturns. Since the demand for semiconductors is derived from the overall demand for end-use industrial and consumer goods, changes in the general business cycle would be amplified in changing semiconductor demand. As the decade progressed, U.S. Government demand for semiconductors fell considerably, causing greater exposure to fluctuating market conditions. Some companies, heavily dependent upon government contracts, would not survive (e.g., Transitron).

Semiconductor devices were increasingly replacing receiving tubes in both consumer and industrial electronics systems. The transistor radio beget transistor-based televisions, hi-fi equipment, and most-importantly in the U.S., computer systems. IBM would become the largest single producer of semiconductors to fuel the circuit needs of its popular mainframe computers. In

[20] Robert N. Noyce, "Microelectronics," *Scientific American*, Vol. 237, No. 3, September 1977.

1968, U.S. manufacturers dominated worldwide production of both consumer electronics (62%) and semiconductors (80%).[21]

In terms of manufacturing, new batch processes, especially the planar method, enabled the industry's growth, prompting both a rapid increase in the number of components produced and an even more rapid decline in unit prices. By the early 1960s Fairchild and others had overcome many of the technological hurdles and developed much of the equipment necessary to mass produce semiconductors.[22] By the mid 1960s as semiconductor production processes began to stabilize, a new semiconductor supplier industry was being formed as many chip makers allowed this function to be spun-off from their operations. While semiconductor device makers began to concentrate more heavily on product innovations, process technology would gradually become the domain of this emerging semiconductor materials and equipment (SM&E) industry.

The IC was commercialized in 1961 and would transform the industry, comprising 90% of semiconductor shipments by decade's end. Even more than its predecessor device, the transistor, the IC was almost entirely dependent upon U.S. Government contracts for the first few years of sales as shown in Table 6-1. This percentage would steadily decrease each year throughout the 1960s.

Table 6-1. Percentage of ICs Consumed by the U.S. Military

Year	% of Total IC Output
1962	100
1963	94
1964	85
1965	72
1966	53
1967	43
1968	37

[21] Golding, *The Semiconductor Industry in Britain and the United States*, 134.
[22] Ross A. Young, *Silicon Sumo: U.S.-Japan Competition and Industrial Policy in the Semiconductor Equipment Industry*, Texas: University of Texas at Austin, 1994, 62.

Source: John E. Tilton, *International Diffusion of Technology: The Case of Semiconductors*, Washington, DC: The Brookings Institution, 1971, Table 4-8, 91.

From President John F. Kennedy's first inaugural challenge of landing a man on the moon and returning him safely to earth by decade's end, the IC received a huge boost from NASA and followed a similar fast-track of achievement, producing a one-chip calculator by 1970 (see Chapter 7). However, realizing this goal was not at all easy nor initially expected by the IC community as Jack Kilby (1982) admits:

> Certainly at the time [1961] I did not visualise anything comparable to a one-chip calculator or that level of complexity in the foreseeable future.[23]

By the mid 1960s a noticeable pattern of increased IC device integration was underway, and reflected in a short, obscure article published in a 1965 *Electronics* magazine issue by Gordon Moore, then head of research at Fairchild. In the article Moore predicted an annual doubling of circuits per chip based upon a simple extrapolation of the brief history of the IC.[24] Later dubbed "Moore's Law" based on its forecast accuracy, the most amazing aspect is that Moore based his prediction on only three (3) data points, one of which was still in the lab! Chapter 8 discusses Moore's Law in detail.

As manufacturing process technologies began to stabilize, firms attempted to produce ICs with ever greater levels of integration. Starting with a handful of circuits per chip in the early 1960s, integration levels progressed into the hundreds of circuits by the mid 1960s and surpassed the thousand circuit level by 1970. The primary reason for this was the adoption of the metal-oxide semiconductor field-effect transistor (MOSFET or simply MOS), a new chip-making method that enabled integration levels of as much as four times over conventional bipolar (junction) technology. The trade-off was that MOS gates switched considerably slower than bipolar. A major MOS vs. bipolar debate ensued among technologists. Both methods would be

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[23] Jack Kilby, quoted in Braun & Macdonald, op. cit., 97.
[24] Gordon E. Moore, "Cramming More Components Onto Integrated Circuits," *Electronics*, Vol. 38, No. 8, April 19, 1965, 114-117.

employed, and neither was easy to make at first, but with time MOS proved to be the choice by chip makers seeking greater density ICs.

By the late 1960s MOS technology combined with more stable chip-making processes allowed IC producers to turn increasingly to product development. New applications such as the portable calculator (see Chapter 7), semiconductor memories and later the microprocessor would replace the dwindling demand from U.S. Government contracts. Seeing the promise in large scale integration (LSI) applications, a whole flurry of merchant start-ups including National Semiconductor, Intel, Mostek, and AMD—each of these spin-offs from Fairchild or TI—soon stood alongside the large captive device makers such as AT&T and IBM.

The great reliance on basic research that characterized the 1950s and early 1960s gradually gave way to process engineering and the ability to quickly master production capability. For example, although RCA and Fairchild are credited with most of the early work in MOS technology, they were unable or unwilling to introduce the technology to the marketplace. Generally smaller firms such as GMe, AMI, and General Instrument, which conducted less basic research, were the first to exploit MOS technology commercially.[25]

At decade's end the leading firms were TI, Fairchild, and Motorola (TI and Motorola produced for both internal and external users). Worldwide industry revenues exceeded $2 billion of which American manufacturers represented a commanding 70% global market share as shown in Figure 6-1.

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[25] Robert W. Wilson, Peter K. Ashton, and Thomas P. Egan, *Innovation, Competition, and Government Policy in the Semiconductor Industry*, A Charles River Associates Research Study, Lexington, MA: Lexington Books, 1980, 65.

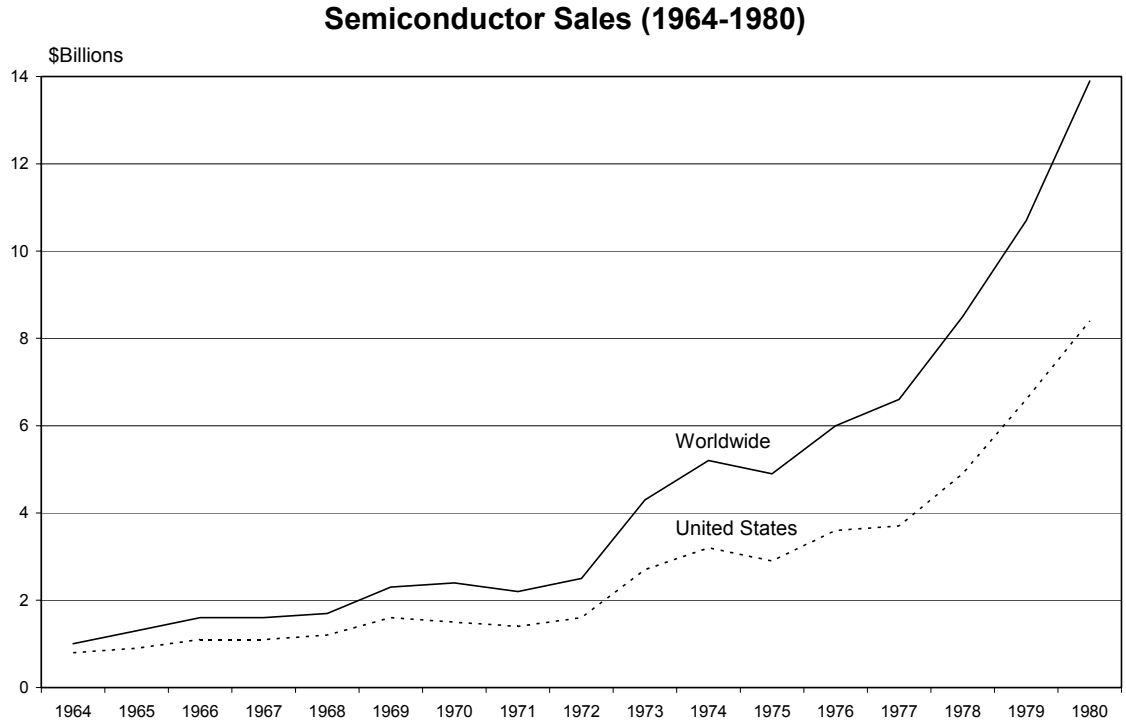

Figure 6-1. Semiconductor Sales (1964-1980)

Source: Various sources (note that these are recorded sales and do not include production by captive manufacturers).

1970s

Rapid expansion of the industry was concentrated in Northern California's Santa Clara Valley, giving rise to the title "Silicon Valley" aptly describing this new regional center of high-technology. By 1975 Silicon Valley employment rivaled employment levels of Massachusetts' Route 128 corridor.[26] Although Texas Instruments was based in Texas and Motorola's semiconductor operations in Arizona, the hub of a rapidly growing semiconductor innovation network had been firmly established in Silicon Valley. Over time, literally dozens of other regions around the globe would attempt to replicate this phenomenon with names like "Silicon Forest" or "Silicon Plains" or

[26] Annalee Saxenian, "Lessons from Silicon Valley," *Technology Review*, July 1994, 45, 47.

some similar variant. At the same time, overseas manufacturing expansion continued so by 1973, U.S.-based companies operated 128 offshore plants.[27]

Braun & Macdonald (1982) also point out that, due to dramatic unit price decreases, the industry had actually contracted during the 1960s and while there were also many new entrants, by 1972 there were about 120 semiconductor companies, approximately the same number as a decade before.[28] The spate of new start-up companies in the late 1960s came mostly from spin-offs from larger IC firms. A primary driver for this wave of new entrants was to develop semiconductor memories, the first real opportunity for a standard IC product to be produced in volume. Although Intel's formation exemplifies this, several other companies such as Mostek, American Memory Systems, Computer Microtechnology, Semiconductor Electronic Memories Incorporated (SEMI), and Cogar Corporation also had appeared. By early 1970, at least eighteen companies were making or planning some form of semiconductor memory.[29] Following serial shift-register memories, the first major product was the random access memory (RAM), in both *dynamic* (*D*RAM, meaning the cells need to be periodically refreshed) and *static* (*S*RAM, meaning no refresh circuitry required) designs. RAM was a vastly less-expensive alternative to the then-dominant ferrite core memories used in computer systems so a huge demand for these products made many of these new firms short-term success stories. Recall from Box 3-2 that Intel's 1103 1K-bit DRAM quickly became the largest selling IC in the world in 1972, accounting for 90% of Intel's revenues that year. However, Intel's dominance in DRAMs would be short-lived as fierce competition and product innovation flourished. By the next product generation Mostek's 4K DRAM used a less-costly 16-pin package that emerged as the standard for most of the industry, while their follow-on 16K DRAM design employed but a single transistor per bit vs. the conventional three transistors per bit.[30] Other new memory products included ROM (read only

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[27] Braun & Macdonald, op. cit., 150.
[28] Ibid., 122.
[29] Wilson, Ashton, and Egan, op. cit., 91.
[30] Ibid., 93; Gordon E. Moore, "Intel—Memories and the Microprocessor," *Daedalus*, Vol. 125, Iss. 2, Spring 1996, 71.

memory), *P*ROM (*programmable* ROM), and *E*PROM (*erasable* PROM). Between 1971 and 1979 the U.S. market for digital semiconductor memories grew at an extraordinary pace: from a base of $60 million in 1971, sales of semiconductor memories exceeded $500 million in 1976 and reached almost $1.3 billion in 1979.[31]

Another major product that helped propel the industry was the introduction of the microprocessor in 1971 by Intel (see Chapter 7). Within a few years, rapid developments in microprocessors spawned the microcomputer or 'personal computer' (PC), first by start-ups like Altair and Apple,[32] but by decade's-end IBM would commit to an all-out crash development effort to enter the market in grand fashion. Much of the rapid growth of the late 1970s shown in Figure 6-1 was derived from RAM and microprocessor sales.

The 1970s also saw semiconductors move pervasively into all kinds of consumer and industrial applications, literally by creating new capabilities from the chip's distinctive size, cost, and performance benefits. As a result, pocket calculators, digital watches, VCRs and many other consumer electronics fields experienced exponential growth rates. At the same time, microcontrollers and microprocessors were finding their way into automobiles and other consumer durables, as well as manufacturing control systems. Interestingly, these end-use industries, once dominant mainstays of American post-WWII manufacturing, were experiencing steady declines in market share to foreign producers, particularly the Japanese. At the same time the role of the U.S. Government had diminished as the primary users (i.e., DoD and NASA) experienced significant budget cutbacks.

By the mid to late 1970s, the semiconductor industry was two decades old and no longer viewed as a lark. Total annual sales would top $10 billion with an average annual growth rate of 13%. U.S. domestic employment would exceed 100,000 workers, with almost that many more

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[31] Michael Borrus, James Millstein, John Zysman, *U.S.-Japanese Competition in the Semiconductor Industry: A Study in International Trade and Technological Development*, Berkeley: Institute of International Studies, University of California, 1982, 29.

[32] A small start-up named Microsoft began in 1975 to develop software for the PC. Five years later IBM chose Microsoft to provide the operating system software (MS-DOS) for their new line of PCs.

working in offshore locations. More importantly, IC output was critical to the production of more that $200 billion worth of goods and services in manufacturing and communications industries.[33] Accompanying this tremendous growth was increased attention paid to issues such as international trade, thus the Semiconductor Industry Association (SIA) was formed in 1977 by five merchant chip makers to represent the interests of the industry in Washington.[34]

Finally, a few government reports had appeared by the late 1970s with 'heads-up' warnings based on observations of potential international competitive threats such as from Japan's Very Large Scale Integration (VLSI) program.[35] National security was also at risk. After recovering a Soviet sonobuoy and discovering an array of ICs that were direct copies of off-the-shelf chips made by TI in the U.S., the U.S. defense department hurriedly initiated the VHSIC (Very High Speed Integrated Circuit) program in 1979.[36] Reduced international competitiveness, intensified Cold War national security threats, and lower levels of federal support would have ramifications on the future of the increasingly important U.S. semiconductor industry.

In 1977, the Federal Trade Commission concluded, "Overall, by any reasonable standard, one must conclude that the performance of this industry is excellent."[37] A few years later, the U.S. Department of Commerce was not as confident of the industry's future, concluding, "The future of the U.S. semiconductor industry appears optimistic in the near term, but less clear in the long view... In the longer view, the U.S. semiconductor industry stands at an important crossroad."[38] Citing increased global competition, particularly from the Japanese, the report cautioned that marketing and management skills, and a "heightened concern for research and development programs" were becoming more important to the U.S. industry's viability as an effective

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[33] USDOC, op cit, 1.
[34] These were LSI Logic, Intel, Advanced Micro Devices (AMD), National Semiconductor (NSC), and Motorola.
[35] See for example USDOC, op cit.
[36] Tobias Neagele, "Ten Years and $1 Billion Later, What Did We Get from VHSIC?" *Electronics*, June 1989, 97. Note that the technical goal for VHSIC was a chip with a million logic gates using 0.5 micron technology.
[37] Douglas Webbink, Staff Report on The Semiconductor Industry: A Survey of Structure, Conduct, and Performance, Washington, DC: Federal Trade Commission, January 1977, 143.
[38] U.S. Department of Commerce, Industry and Trade Administration, *A Report on the U.S. Semiconductor Industry*, Washington, DC: USGPO, September 1979.

competitor in world markets. In other words, the traditional U.S. strength of technological dominance (e.g., the best designs) was no longer enough to carry the day. Other capabilities, most especially in manufacturing process engineering, began to emerge as important factors.

In terms of technology, by the mid 1970s Moore's 1965 prediction had not only proved true, but with the adoption of MOS (metal-oxide semiconductor) silicon-gate process technology, extreme packing densities along with low power consumption enabled the idea of continual capacity (and feature/performance) doubling to perpetuate well into the future. Although the doubling rate would not continue on an annual basis, the consensus rate of every 18-24 months that constituted "Moore's Law" would ultimately be universally accepted (see Chapter 8).

MOS technology underpinned the era of large-scale integration (LSI), making it possible to put more than one thousand components on a chip in 1970; by decade's end this number would exceed 100,000. The promise of MOS had significant effects on industrial structure. According to Borrus, Millstein, and Zysman (1982), between 1966 and 1972 thirty new companies specializing primarily in MOS ICs entered the U.S. industry. By 1973 approximately 85 percent of the sales of these newly established IC firms were concentrated in MOS technology, whereas among those firms established before 1966 only 35 percent of sales were in MOS devices. Spurred by its use in hand-held calculators, digital watches, and computer main memory, sales of MOS IC products rapidly expanded between 1970 and 1975.In 1970 sales of digital MOS integrated circuits were only some $45 million; by 1975, however, MOS sales had reached $428 million and had surpassed the total value of digital bipolar sales.[39]

Bipolar was the other major technology used in IC designs. There were various types of bipolar, but the most popular was transistor-transistor logic (TTL) invented by Fairchild in the mid 1960s. The biggest advantage of TTL over MOS was its fast switching speed, thus most high-end applications such as computers employed bipolar technology. However, compared with MOS, bipolar required much more power, did not scale in increased packing density at the same rate,

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[39] Borrus, Millstein and Zysman, op. cit., 28.

and was more difficult to manufacture. Thus, the gap between MOS and bipolar gradually narrowed until MOS won out as indicated above.

Finally, it was during the 1970s that silicon solidified its place as the dominant substrate material. Braun & Macdonald (1982) capture this sentiment in selected quotes as follows:

> Silicon is it. I see no reason to go in any other direction for a long, long period of time. In fact, I personally killed all the gallium arsenide power diode programmes in Westinghouse… (William Winter)
>
> There hasn't been a whole lot of search for a replacement for silicon for years now . . . I would say rather that there is a wide-eyed recognition in the industry that we haven't begun to apply the technology we have. (Floyd Kvamme)[40]

By decade's end the international industrial landscape began to change markedly. A wave of acquisitions of U.S. IC makers by larger firms—including foreign enterprises—had occurred or was underway. Fairchild was absorbed by Schlumberger (France); Signetics by Philips (Netherlands); Mostek by United Technologies (U.S.); American Microsystems Inc., first partially by Bosch (Germany), then later completely by Gould (U.S.); and Electronic Arrays by Nippon Electric (Japan). Furthermore, leading Japanese IC makers, aided in part by a government-sponsored initiative to catch up and ultimately surpass U.S. firms in technological capability, began to make significant progress. After consistently following U.S. manufacturers in introducing the 1K and 4K RAM generations, a Japanese manufacturer, Fujitsu[41] was the first to introduce a 16K RAM chip in 1978 and by 1979, Japanese firms had grabbed 42% of the 16K RAM market.

1980s

The 1980s are best remembered in the industry as a watershed era dominated by international competitiveness threats, particularly from Japan. As shown in Figure 6-1, the U.S. had been steadily losing semiconductor market share to Japan since the mid 1970s (correlated

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[40] Braun & Macdonald, op. cit., 141.

[41] Although Fujitsu is acknowledged as the first to introduce the 16K DRAM it should be noted that this chip was actually a copy of a Mostek design. According to informants, a Japanese company called Topan obtained the Mostek design around 1976, photographed each layer and sold the photo masks to anyone for $50K. Fujitsu apparently had been one of the purchasers. At the time Mostek had difficulty manufacturing the part. See for example, e-mail from Turner Hasty to the author, August 16, 2000.

with steady U.S. market share losses in 'downstream' electronics and manufacturing industries) but this had gone largely unnoticed by the public. A flurry of industry consortia and major legislative initiatives illustrate the dual challenges of international competitiveness and national security that faced the U.S. semiconductor industry. The SIA formed the SRC (Semiconductor Research Corporation) in 1982 to address not only collaborative research needs, but the more immediate high-skilled U.S. worker shortage in the science and technology fields. The National Cooperative Research Act of 1984 exempted joint R&D projects from treble damages and *per se* rules of antitrust law and helped legitimize the term, *pre-competitive research*. By 1985 several Federal agencies, Congress, and most importantly, industry began to collectively realize that the continual erosion of market share, primarily to the Japanese, had far-reaching implications for the nation. As a result, Sematech was formed in 1987 by the SIA to address semiconductor manufacturing technology needs, an area that the U.S. had clearly become lax in. DoD shared in the funding of Sematech (along with 14 industry members), a proposed 5-year program to regain U.S. leadership in worldwide market share. A related development was the Semiconductor Trade Agreement, ratified in 1986 to address opening up access to Japanese markets and dumping by Japanese firms in the US market. Finally, a National Advisory Committee on Semiconductors (NACS), fashioned after the NACA model in aeronautics, was established by Congress in 1988 with the charge of "devising and promulgating a national semiconductor strategy." By the end of the 1980s a whole new set of concerns had captured the collective attention of all parties, private and public, involved in the U.S. semiconductor enterprise.

It is important to note that within the federal government this view was extensive as evidenced by the number and sources of major reports or studies including from the Commerce Department,[42] Defense Science Board,[43] White House,[44] as well as Congressional staff briefs and

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[42] U.S. Department of Commerce, Office of Microelectronics and Instrumentation, *A Competitive Assessment of the U.S. Semiconductor Manufacturing Equipment Industry*, Washington, DC: USGPO, March 1985.

[43] Defense Science Board, *Report of the Defense Science Board Task Force on Defense Semiconductor Dependency*, Washington, DC: Office of the Under Secretary of Defense for Acquisition, February 1987.

reports. The SIA also commissioned studies. A central theme of these reports was the purported decline of U.S. leadership, both economically and technologically, against international rivals, especially Japan. In total world market share, Table 6-2 shows the ranking of the top 20 semiconductor manufacturers in 1985, including major U.S. captive producers IBM and AT&T. This list comprised almost three-fourths of global production.

Table 6-2. Principal Semiconductor Manufacturers Shares of 1985 Total World Markets

'85 Rank	Company	HQ	'85 Total Share
1	IBM	U.S.	9.1%
2	NEC	Japan	7.0%
3	Motorola	U.S.	6.4%
4	Texas Instruments	U.S.	6.1%
5	Hitachi	Japan	5.9%
6	Toshiba	Japan	5.2%
7	Philips-Signetics	Europe	3.8%
8	Intel	U.S.	3.6%
9	Fujitsu	Japan	3.6%
10	National Semiconductor	U.S.	3.3%
11	Matsushita	Japan	3.2%
12	Mitsubishi	Japan	2.3%
13	Advanced Micro Devices	U.S.	2.2%
14	AT&T	U.S.	2.1%
15	Fairchild[45]	U.S.	1.7%
16	Sanyo	Japan	1.6%
17	Siemens	Europe	1.5%
18	Hewlett-Packard	U.S.	1.5%
19	Sharp	Japan	1.2%
20	Thomson	Europe	1.1%

Source: Dataquest, as reported in *The Semiconductor Industry: Report of a Federal Interagency Staff Working Group*, November 16, 1987, Chart 4, 7.

While a U.S. firm retained overall leadership, there were more firms outside the U.S (11 total) than in the U.S (9) making up this list. A related concern was the slippage of technology

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(Note that the draft title of this report was "Assurance of Continuing U.S. Capability for Designing and Producing Critical Integrated Circuits: A Defense Semiconductor Initiative").

[44] *Report of the White House Science Council Panel on Semiconductors*, September 1987.

[45] Note that Fairchild had been earlier acquired by Schlumberger, a French company, thus assignment to U.S. as headquarters country may be incorrect.

leadership in key products, materials, and manufacturing equipment. Figure 6-2 was published by the National Research Council's Materials Advisory Board and received widespread attention.

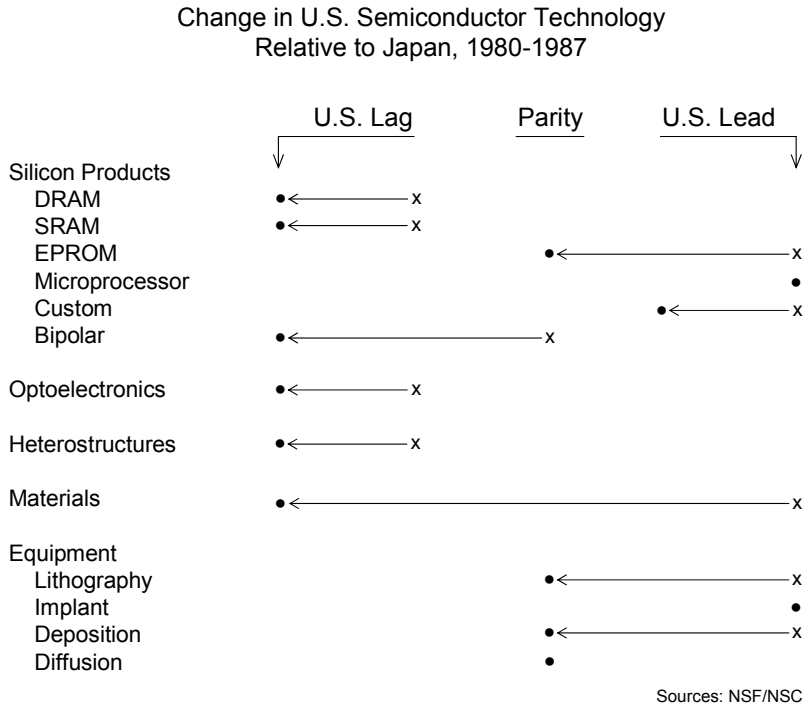

Figure 6-2. Change in U.S. Semiconductor Technology Relative to Japan, 1980-1987

Source: *Report of the White House Science Council Panel on Semiconductors*, September 1987, Figure 3, 4.

The industry had undergone consolidation in the 1970s. It is estimated that there were between 15 and 20 percent fewer firms in the U.S. semiconductor industry in 1980 than a decade earlier.[46] Much of this came about through corporate takeovers or mergers with other semiconductor firms or large corporations wishing to enter the industry. Of 36 U.S. semiconductor companies started between 1966 and 1975, only seven remained independent in 1980, and no fewer than 17 merchant semiconductor companies were then owned by conglomerates with

[46] Braun & Macdonald, op. cit., 124.

primary interests outside semiconductors. Economic barriers to entry had grown to the point that it was no longer possible to establish a small semiconductor facility for a few million dollars.[47]

In terms of product innovation, the industry continued to contribute 'breakthrough after breakthrough', the pattern set more than twenty years earlier. The PC industry became mainstream following IBM's entry (see Box 3-5). The desktop computer application intensified the memory bit density race while a microprocessor performance race ensued as new manufacturers appeared almost overnight attempting to grab a piece of a rapidly-expanding market. A few of the more well-known entrants include Compaq, one of the first to offer a 'compact' PC in 1982, along with Dell in 1984 and Gateway in 1985, both of which offered innovative toll-free ordering and a 'direct' distribution method enabling users easy and quick access to PCs. Industry sales boomed; all three of these firms' revenues would eventually exceed $1 billion with Compaq setting a new record (i.e., the first new company to achieve the sales milestone in its first five years). Ironically, desktop computing made possible by the IC would have serious ramifications on many of the captive computer systems manufacturers (including IBM and Digital Equipment Corporation) involved in mainframes and minicomputers. Moore's Law continued at an unrelenting pace and as ICs became increasingly more powerful a gradual and permanent shift of knowledge and capability from traditional computer system companies to the semiconductor industry resulted.

There were more ramifications. The standard, high-volume IC products that emerged in the 1970s such as DRAMs and microprocessors/microcontrollers sparked major structural changes within the industry throughout the 1980s. For example, many of the firms that had specialized in custom chips when it first appeared that this would be the trajectory to follow (e.g., AMI discussed in Chapter 7) found themselves in an economic dilemma as unit prices continued to fall at a 30% per annum rate and set-up costs proved far too expensive.

A definitive pattern was underway that transferred economic fortune from electronics and computer systems houses to IC suppliers, which Gilder (1989) aptly calls collapsing into the

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[47] Ibid.

'microcosm',[48] is now referred to as moving capability up the supply or value chain or simply "upstream." As ICs incorporated progressively more complex user needs from custom design experience—greatly assisted by ever-capable processes that packed more functionality per IC—chip makers turned out designs not in response, but in *anticipation* of user needs, thus helping create them. The case of the electronic calculator was one of the first important examples of this (see Chapter 7), but semiconductor memories, microprocessors, microcontrollers, and numerous other device types all followed this 'custom-to-standard' pattern. Of course *standard* does not mean universal as competition forced players to continually innovate new design features and capabilities. The microprocessor 'wars' of the 1980s between Intel (who supplied the IBM PC and PC-compatible architectures) and Motorola (who supplied the Apple Macintosh architecture, and ultimately IBM itself) best illustrates this. In terms of complexity, the Intel 8086/88 microprocessor that was selected to power the IBM PC in 1980 contained 29 thousand transistors, more than a tenfold increase from its first microprocessor, the 4004 introduced in 1971. During the 1980s Intel introduced three follow-on generation microprocessors (i.e., 286, 386, and 486) the last of which containing more than one *million* transistors. Motorola's 68000 family underwent similar advances.

This also meant that as the competitive stakes increased and profit margins were squeezed, chip makers had to become even more specialized in what they produced and how they produced it. One landmark example of this is Intel's strategic decision to exit the DRAM market (see Box 3-2), a market they essentially created with the launching of the 1K 1103 DRAM in 1970. Intel initially dominating this product sector and drew most of their sales and profits from DRAMs during the early 1970s, however by late 1984, Intel's market share in 256K DRAMs had fallen to 4%, and it had lost its position entirely in 64K DRAMs.[49] Interestingly, when Intel chose to

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[48] George Gilder, *Microcosm: The Quantum Revolution in Economics and Technology*, New York: Simon and Schuster, 1989.
[49] Robert Burgelman, "Intel Corporation: The Evolution of an Adaptive Organization," Academy of Management Chicago 1999 Conference, August 6-11, 1999, http://www.aom.pace.edu/meetings/1999/INTEL1.htm

exit the market they had just developed the first CMOS 1M DRAM (which they never commercially introduced).[50]

Brugleman (1999) points out that by 1984 DRAMs had taken on the characteristics of a mature product such as standardized product features which favored the manufacturing oriented players. Equipment suppliers had become more important in process innovation, which led to a leveling of process capabilities. As a result, both design and fabrication technologies were well understood by all major players in the industry. Moreover, the primary buyer of DRAMs changed from engineers to procurement officers, who were more concerned with cost, quality, and reliability than product features. The competitive nature of this market made low manufacturing costs a key competitive advantage. This was an area where Japanese manufacturers had the advantage.[51] Maturity also brought other forms of specialization such as the rapid growth of the SM&E industry as discussed in Chapter 4.

A related issue was quality which had at its source manufacturing processes. As had been done successfully in consumer electronics, automobiles, steel, and other product sectors, Japanese-made semiconductors were increasingly recognized as higher quality products than those made by American chipmakers. A well-publicized report by Hewlett-Packard (HP) in 1980 demonstrated a significant difference in quality in 16K DRAMs between three leading U.S. manufacturers and three leading Japanese manufacturers. The results of the study were astounding: the best American supplier had a failure rate approximately six times as many failures as the best Japanese supplier, and the worst American supplier had about 27 times as many failures per thousand hours. Although later studies by Hewlett-Packard showed significant improvement by the U.S. companies, this early report had a dramatic effect in drawing attention

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[50] The 1Mbit CMOS DRAM prototype would be ready March 1985 and was based on advanced (at the time) 1 micron process technology. The product would be 18-24 months ahead of everyone else, fully intended to leapfrog the competition. Intel had already invested $50 million in development, but another $150 million was required to manufacture the chip.

[51] Ibid.

to the issue of Japanese superior quality.[52] Okimoto et al (1984) attributed Japan's ascendancy in large part to their emphasis on process technology over product design, where U.S. manufacturers had traditionally concentrated. The authors argued that Japanese companies had been able to advance rapidly from positions far behind largely because of their concentration on, and successes in, incremental improvements in process technology.[53]

Another important factor was the industry's so-called business cycle. The cyclical nature of product demand was not new but the extent of the effects also played a major role in the 1980s. After averaging better than 17% annual growth in the early 1980s and 52% in 1984, the worldwide semiconductor industry suffered a major cyclical reverse of 15% decline in 1985.[54] The resultant fall in unit prices was unprecedented, falling in some cases more than tenfold to cents per chip.

1990s

In November 1989 NACS issued its first report to then-President Bush entitled *A Strategic Industry at Risk*.[55] The threat of compromised economic and national security posed by further erosion of the semiconductor industry loomed large in the public eye. But looking closer, the U.S. industry had already begun to turn the corner with a small increase in world market share gains. What had resulted from a decade of semiconductor industry 'crisis' was a different approach, model, and even attitude towards cooperative behavior. 'Beating the Japanese' had served as a rallying cry of sorts that enabled a fiercely competitive industry to come together—now legally in a pre-competitive environment—to cooperate and collaborate on design and manufacturing processes all shared in some way. This set of issues had a broad reach, particularly *upstream* with the critical manufacturing equipment and materials industry that supplies the chipmakers.

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[52] Daniel I. Okimoto, Takuo Sugano, and Franklin B. Weinstein (eds.), *Competitive Edge: The Semiconductor Industry in the U.S. and Japan*, Stanford, CA: Stanford University Press, 1984, 53.
[53] Ibid., 180-1.
[54] *The Semiconductor Industry*, Report of a Federal Interagency Staff Working Group, November 16, 1987, 1.
[55] National Advisory Committee on Semiconductors (Ian Ross, Chairman), *A Strategic Industry at Risk*, Washington, DC: USGPO, November 1989.

The U.S. semiconductor industry led most other U.S. manufacturing industries in the adoption of technology management practices that fostered cooperation and collaboration. By 1990, the early vertically-integrated chip making industry had outsourced much of the fabrication process technology to the SM&E industry. At the same time, chipmaking became more and more "vertically-specialized," providing vast growth opportunities for novel new approaches or business models including *fabless* (i.e., design only) and *foundry* (i.e., manufacturing only) firms.

Another milestone is the creation of the industry's technology strategy or "roadmap," loosely initiated during the strategic technology workshops held in the formation of Sematech and more formally with MicroTech 2000 in 1991, one of NACS final projects. The purpose of these early roadmap exercises was expressly to regain U.S. leadership by looking out over a longer time horizon and aligning all the necessary elements (i.e., lithography, design, test, interconnect, etc.) so that a more orchestrated approach was possible. With the acceptance of responsibility for the MicroTech 2000 report, the SIA decided to continue the collaborative planning effort and subsequent industry technology roadmaps were produced in 1992, 1994, and 1997. Starting in 1998/9 the process became *international*, and the first International Technology Roadmap for Semiconductors (ITRS) was published in 1999.

New regional players emerged across the global landscape. The persistent Japanese economic recession, an aggressive low-cost push from other Asian countries such as Taiwan, Korea, and Singapore, and resultant downward trend in prices (and profits) as DRAM devices matured fully into commodity products, caused continual erosion of Japanese market share. Meanwhile, the U.S. had all but departed from the DRAM business during the 1980s, save for TI and the much smaller firm Micron in Idaho.[56] The traditional strength of U.S. chipmakers in the area of product innovation brought new capabilities to the much more profitable logic device sector. This is no more evident than in the area of microprocessors, where Intel, Motorola, AMD,

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[56] Micron has since purchased Texas Instruments' memory operations in 1998 and now is one of the industry's leading suppliers of semiconductor memories.

and others were able to fuel the rapidly-growing PC market that had achieved widespread adoption due to reduced prices, software advances (e.g. Microsoft *Windows*), and perhaps most importantly, easy and inexpensive Internet accessibility. Further, TI's dominance in Digital Signal Processors (DSPs) and other U.S. firms' strength in ASIC (application-specific IC) devices, where there is significantly more value-added (and profit) than in DRAMs, helped reinforce the "reversal of fortune"[57] experienced by the U.S. semiconductor industry as illustrated in Figure 6-3.

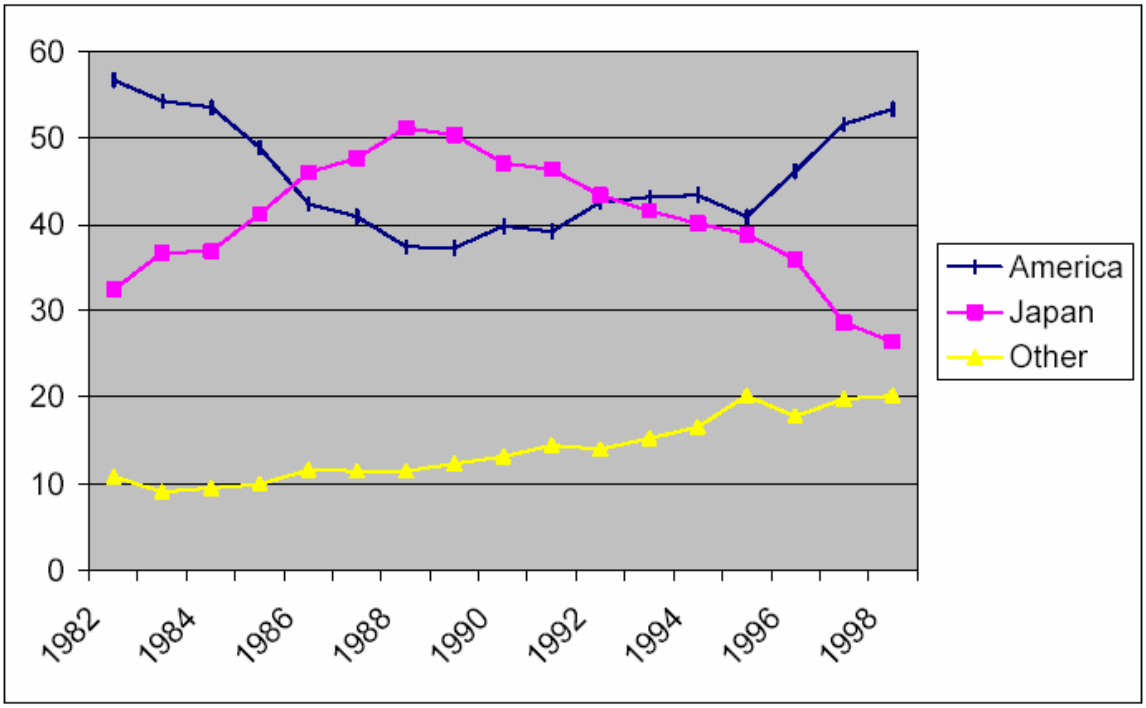

Figure 6-3. Worldwide Semiconductor Market Shares (in percent), 1982-1998

Source: Semiconductor Industry Association, as reported in Richard N. Langlois and W. Edward Steinmueller, "Strategy and Circumstance: the Response of American Firms to Japanese Competition in Semiconductors, 1980-1995," Paper presented at the Tuck/CCC Conference on the “Evolution of Capabilities: Emergence, Development, and Change,” September 24-25, 1999, Hanover, New Hampshire, December 1999, Figure 1, 2.

[57] Jeffrey T. Macher, David C. Mowery and David A. Hodges, "Reversal of Fortune? The Recovery of the U.S. Semiconductor Industry," *California Management Review*, Vol. 41, No. 1, Fall 1998.

Also noteworthy is that Sematech, initially a U.S.-only consortium (to counter the Japanese threat), underwent two significant strategic changes. In 1994 it gave notice to the Federal Government that it would no longer accept matching government funds (effective 1996), and in 1999 Sematech fully transitioned into *International Sematech* expanding its membership to include European and Asian regions. As Turner Hasty, a member of the Sematech start-up team, stated, "The laws of physics are the same in Massachusetts as in Dallas as in Tokyo."[58] The purpose of Sematech had evolved from a strategy *against* international competitors to one where those same competitors would become Sematech members with the new goal of perpetuating the industry's historical productivity curve or what one long-time Roadmap participant refers to as the industry's 'common good'.[59] Reflecting the globalization of the industry in both *upstream* suppliers and *downstream* users, International Sematech better fits the reality of today's daunting technological and economic challenges. In parallel the industry's Roadmap has evolved from a *National* Technology Roadmap for Semiconductors (NTRS) to an *International* Technology Roadmap for Semiconductors (ITRS) as previously mentioned. This does not include the many international consortia established to address specific technical issues such as I300I, the international 300mm (12") wafer initiate. Additionally, strategic industry alliances, both horizontal and vertical, are clearly on the increase in response to both technological and economic factors.

Technologically, the pace of innovation continued to advance as 1Gbit DRAMs and 1GHz microprocessors were demonstrated. Moore's Law in semiconductors has spawned similar scaling phenomenon in mass data storage, telecommunications bandwidth, and optoelectronics.[60]

The 1990s did bring the traditional cyclical swings in demand, however the decade would end with a strong upswing: in 2000 the global industry achieved $200 billion in sales, a remarkable

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[58] Turner Hasty, telephone interview, May 10, 2000.
[59] Alan Allan, personal interview, July 1999.
[60] National Electronics Manufacturing Initiative (NEMI), NEMI Roadmap Workshop, June 14-15, 2000.

four-fold increase from $50 billion in 1990 sales. The industry entered the 21st Century stronger and more global than ever.

The future of the industry looks very promising technologically. New sources of demand include the wireless revolution brought on by the widespread adoption of pagers, cellular phones, and other portable telecommunications devices that are redefining the information appliance in the consumer market. The lines separating telecommunications (e.g., cell phone) and information tool (e.g., Palm Pilot) are rapidly blurring. This convergence gives rise to semiconductor devices such as the SoC (system-on-a-chip), analog and compound (non-silicon only substrate) semiconductors, even MEMS (micro-electromechanical systems). These same product types are also finding more uses in industrial applications. The trend in device miniaturization has brought forth MEMS and related technologies under the broader are referred to as *nanotechnology* where considerable research, both privately and publicly funded, is underway.

Further, economic challenges (e.g., $3 billion fab costs) will bring to bear additional hurdles to overcome. Perhaps the biggest challenge the industry faces, with both technical and economic factors, is continuing along the industry's historic productivity curve (i.e., Moore's Law). The miniaturization of circuits using the present design regime (i.e., silicon substrate, CMOS process, etc.) will soon reach atomic levels or the physical limits of nature. Analysts estimate that this will occur within a decade or so. In the meantime, research into new materials and device structures is well underway.

The more immediate concern has been the dramatic cyclical downturn since the peak in 2000. It may take until 2004 or possibly 2005 before the industry attains the $200 billion sales level again (see Chapter 10, Table 2).

Summary of Major Factors

The next section draws from this brief history and examines the major factors that have contributed to the industry's unique pattern of technological innovation. While certainly not an

exhaustive examination of all possible factors, these factors are considered the most significant. The technical factors include the planar process, the IC, Moore's Law, and MOS/CMOS technology and device scaling, while institutional factors include research consortia, standards, and the ITRS.

Planar Process

According to Braun & Macdonald (1982), one of the major innovations of the 1950s, "perhaps *the* major innovation," was the planar technique.[61] As previously mentioned, the planar process was the triumph of newcomer Fairchild Semiconductor which had been successful manufacturing the mesa transistor. The planar technique was similar to that used for the production of mesa transistors, but with important advantages. As with the mesa transistor, the planar technique allowed much of the fabrication to be accomplished from one side of the wafer, making for production economies. Unlike the mesa, though, the planar transistor was flat. This meant that electrical connections no longer had to be made laboriously by hand, but could be achieved by depositing an evaporated metal film on appropriate portions of the wafer.[62] The planar technique allowed producers to make multiple transistors at a time versus individually. The era of batch processing was born with the planar transistor. As Dummer aptly states, "The planar process is the key to the whole of semiconductor work."[63]

The Integrated Circuit

The planar transistor was the forbearer of the integrated circuit (IC), a device which the functions of several discrete components are performed within a single chip of semiconductor material. Batch processing made possible by the planar technique pointed in the direction of the IC. Since it was now feasible to make several identical components on one wafer and then cut the wafer into separate components, then it was also feasible to make a suitable selection of

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[61] Braun & Macdonald, op. cit., 73, emphasis added.
[62] Ibid., 74-5.
[63] G.W.A. Dummer, as quoted in Ibid., 74.

components on the wafer, to connect them in the same way that connections were made to form circuits from individual transistors, and to sell whole integrated circuits.[64] As Moore's opening quote reveals, this was basically how the IC was invented. With electrical connections between circuits accomplished internally to the device the economic impact of this discovery quickly became obvious and would be significant. By making multiple devices in the same space formerly occupied by a single device, not only do these devices perform better individually, but the entire IC package (or chip) containing these *integrated circuits* demonstrate far greater synergistic performance benefits. They perform better while consuming less power.

Initially a novelty, ICs were not in the mainstream of production (and even research). They were harder to make, thus more costly and less profitable. "This [integrated circuit] only replaces two transistors and three resistors and costs $100. Aren't they crazy!" stated one industry executive in the early days of the IC.[65] Turner Hasty, former head of research at TI and an early Sematech COO, remembers that the IC, like most things new, met with a lot of initial resistance:

> Most of the 1960s was spent defending the IC as a good idea. It was problematic since early performance wasn't that good. Bipolar technology used off-chip was very good at the time and the best semiconductor makers like AT&T were against the IC. In the early 1960s there was a *Business Week* article that discussed the IC versus discreet industry argument. IBM stayed neutral at first, but when they decided to start using ICs in the late 1960s in computers things changed.[66]

As Hasty's last comment suggests, probably as important as any factor is that there was no clear commercial demand for the device at first. Moore (1996) also recalls this early period when supply led commercial demand, "By the late 1960s … [t]he industry was caught on the horns of a dilemma. We were capable of manufacturing circuit functions more complex than those that could be defined."[67] Another major factor concerned traditional circuit design practices. The designers of electronics systems at the time assembled circuits using discreet components—first vacuum

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[64] Ibid., 88.
[65] Attributed to a Philips director by P. W. Haayman in Braun & Macdonald, Ibid., 98.
[66] Turner Hasty, telephone interview, May 10, 2000. Hasty had the unique experience of working for both Jack Kilby (at TI) and Bob Noyce (at Sematech) during his career.
[67] Gordon E. Moore, "Intel—Memories and the Microprocessor," *Daedalus*, Vol. 125, Issue 2, Spring 1996, 56.

tubes, then transistors—to meet the functional requirements of end-use systems. Due to the experience amassed in discreet devices, their performance exceeded that of the IC for several years; even cost/function ratios were better. Jack Kilby, co-inventor of the IC, acknowledges a related impediment to adoption by discreet component designers:

> [T]he true transistor people did not want to see their elegant devices messed up with all the other stuff on the chip.[68]

The following account of design ingenuity by Jack Avins at RCA as described by Goldstein (1997) provides insight into the lengths taken to initially adopt the IC into commercial applications. Following the successful innovation and introduction of color television in the early 1960s, the company embarked on an all-out effort to incorporate ICs into receiver and other important television circuits. This challenge proved much more difficult than simply substituting ICs for discrete components:

> These [technical challenges] were many. The team's strategy was first to develop a circuit in discrete components and then recreate it on a chip. Unfortunately, the procedure was not so straightforward. ICs were still new and details of their use were not well established. For example, Avins hoped to use strings of diodes to supply the power for several of the transistors on his chip, a routine technique called 'biasing'… In his discrete component prototype, Avins was able to reach into a bin he kept near his bench, pull out a handful of diodes and put them in place. When he fabricated the circuit on a chip, however, he found the diodes were not working. Although diodes, unlike inductors, had been successfully integrated on chips in the past, some unexpected production difficulties forced Avins to look for a new way to realize diodes in his particular situation. Working with his team, he replaced diodes with transistors that had their base and collector shorted.[69] This solution was unimaginable with discrete component [sic] because transistors were more costly than diodes. On the integrated circuit, however, a transistor was just as easy to implement as a diode. Thus Avins' team had countered a problem raised by the special properties of the IC by exploiting another of its special properties.[70]

One of the underlying themes of this study is the crucial importance of engineering to technological innovation that is so well reflected in the Jack Avins account above. This author offers a similar account in Box 6-2.

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[68] Jack S. Kilby, "Turning Potential Into Realities: The Invention of the Integrated Circuit," Nobel Lecture, December 8, 2000, 482.
[69] The 'base' and 'collector' are two of the transistor's three leads. The third is called the 'emitter'.
[70] Andrew Goldstein, "Jack Avins: The Essence of Engineering," Chapter 4 of Andrew Goldstein & William Aspray (eds.), *Facets: New Perspectives On the History of Semiconductors*, New Brunswick, NJ: IEEE Center for the History of Electrical Engineering, 1997, 171.

Box 6-2. Personal "Engineering" Story

The author was formerly a computer service technician, involved in the installation, preventive and remedial maintenance of a wide variety of computer systems and peripheral equipment including mainframe, minicomputer, and desktop computer families. His troubleshooting career highlight was fault isolating a single defective ferrite core in a 4K (thousand) word bank of core memory. Repair entailed replacement of the entire memory bank, but the challenge was in the troubleshooting, as any service person will attest. As memorable as this accomplishment is, it was a correction of a previously-working (and engineered) system function. Thus, this is not the engineering story. One that better fits this description (i.e., given a set of parameters, how do you solve this particular problem?) occurred during extensive system training for a mainframe system.[71]

Brief overview of computer design: Digital computer systems at bottom operate on "ones" and zeros" or basically the changed electrical states of circuits, whether they be relays, vacuum tubes, discreet components, or integrated circuits as featured in this thesis. This is known simply as binary logic: the circuit is either turned on (one) or off (zero). Designing these circuits in arrays—and lots of them running very fast—allows a computer architect to organize and then manipulate binary data into comprehensible information (e.g., a person's name, address, etc.). This is done by arranging individual binary digits or "bits" of data into binary coded decimal arithmetic that represents alphanumeric characters (i.e., bytes) or combinations of these called words. The actual manipulation of data is done through the computer's pre-coded instructions (e.g., Intel's x-86 instruction set) that, when accessed, tell the computer what operation to perform. These instructions are also at bottom binary code, but are organized into a higher-level

[71] The computer system discussed here is a Burroughs B5500 mainframe designed primarily for large appliocations such as banking, but used in this case at a U.S. Navy base for payroll and other large administrative functions. Introduced in 1964, the B5500 employed a unique circuitry packaging scheme of discrete components. Thus, it was one of the few systems where the author had the opportunity to isolate and replace a defective transistor. The author was also trained on the B3500 mid-range system which was first introduced in 1967 and employed integrated circuits.

"machine language" that enables programmers to write instructions for programs at even higher-level programming languages (e.g., assembly language) so ultimately end users may perform useful functions such as word processing, e-mail, and a whole plethora of software applications. So basically a single keystroke or mouse click sets off hundreds and even thousands of individual computer operations that ultimately reset ones to zeros or vice versa to achieve a desired outcome. Current desktop machines operating at Gigahertz speeds accessing Gigabytes of data make this simple operation seem effortless, but it is really quite involved.

The engineering story: One of the things service personnel need to learn is diagnostic procedures. Known commonly as "diagnostics," these are programs written expressly to test and verify functionality of various computer operations (e.g., the Scan Disk operation performed on PCs upon startup that checks the integrity of the hard drive). Diagnostic programs are simply another computer application, but since they are not end-user programs often are not written beyond machine language level. One particular situation occurred when diagnostics were being covered during mainframe system training. As a method of teaching the instruction set and the associated machine language, the instructor assigned students to write a simple machine language program to have the machine store an assigned value in a certain memory address and then stop. This was a straightforward task involving only a handful of the simpler instructions, but he further challenged each student (including the author) to see *who could do it with the least lines of code*. He then stated that *the record was 29 lines* and had stood for several classes (years).

Although none of us was an engineer, being technicians was not much different especially when it came to meeting a technical challenge such as this. At first the challenge seemed

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[72] Op. cit., Rumelt.
[73] Gordon Moore, personal interview with the author, Intel, Santa Clara, CA, June 13, 1996. Moore retired in 1997 (he still serves as Chairman Emeritus) and has since contributed heavily to many causes including education and the environment. Moore was ranked #5 of *Forbes* "400 Richest in America" in 2000 behind Warren Buffett, Paul Allen, Larry Ellison, and Bill Gates http://www.forbes.com/400richest/
[74] Gordon Moore, in an interview with *Ingenuity* editor, Laura Schmitt, March 2, 2000, http://www.ece.uiuc.edu/ingenuity/500/mooreint.html

impossible since text book programming techniques that we had learned required at least 40 lines of code. After learning some of the workarounds many were able to get the number down to the mid thirties and the author was able to reach 32 successfully. But anything lower seemed unreachable. How a previous student was able to achieve 29 baffled everyone (except, of course, the instructor). After many hours studying the problem (staring at the machine in a cold basement one very early morning), an inspiration came. It involved the order and placement of the lines of code. Each line of code contained a "word" of either *instruction* that directed the machine what to do, or *data* that was to be manipulated by the (typically preceding) instruction. Therein laid a potential workaround: it was possible that the "word" could be the same code whether it be data or instruction. In fact, this was the case in more than a few lines of code. So the challenge was how to use one line of code (vs. two or three) of a distinct word and reduce redundancy. After several attempts at reorganizing the order of instructions and reassigning memory addresses so that the same word was used as both instruction and data, the author was able to whittle the lines down to 26, three fewer than the standing record! Later that morning the author presented the 80-column punched card (that's how old this story is) to the instructor who proceeded to run it through the card reader and witness that it performed successfully. At that point the author asked the instructor to note how many columns had been punched. With amazement the instructor offered congratulations.

The class quickly moved on to other important system functions and the excitement was short-lived. Much of engineering life is similar—new problems continually arise that need attention. The efforts and excitement of the previous student who was the first to break 30 was probably not much different. The subsequent student who beat the author's mark was equally inventive and his/her efforts rewarding. In fact, anyone engaged in a creative endeavor has a similar story to tell. A former student of the author's who happened to be an engineer once stated that good engineers learn to "fool mother nature." He used optical lithography as an example. With a pencil and paper (an engineer's tools of the trade) he described how the edges of a very

small object, when projected, become distorted or blurred at very low wavelengths. The reason for this is diffraction, a fundamental principle in optical theory. Recognizing this, photolithography designers could build a mask with a non-rectangular pattern (e.g., including scattering bars on sides and serifs on corners) which, when projecting a very small image, would "blur" into a rectangle.[72] Thus, engineers have compensated by designing into the device a means of correcting for the natural occurrence of diffraction, thereby extending the use of optical lithography equipment to ever shorter wavelengths. This practice is officially called *optical proximity correction* (OPC) and is one of several engineering 'tricks' employed. Of course, this type of inventive behavior can be found in all technologies from tap drinking water to manned flight to perennial rice.

When the author had the opportunity to personally interview Gordon Moore, he was then Chairman of Intel and would later be ranked 5th by *Forbes* in terms of wealth in the U.S.[73] Remarkably, his office was an unassuming cubicle with enough space for a desk, small round table, and a few chairs. I learned quickly that this was part of Intel's egalitarian corporate culture that Moore himself worked very hard to instill. Perhaps most notable was Moore's technical explanations. Again, with pencil and paper, he meticulously described the design of an early 'mesa' transistor and its significance as a predecessor to the planar transistor, from which everything else follows. While viewing a diagram of the planar transistor, Moore proudly and with much laughter stated, "I designed that thing myself. It's probably about the only device I ever designed that went into production." Of all the things that were discussed in that interview (predominantly about Moore's Law), Moore seemed most comfortable as an engineer, with pencil and paper, describing the workings of the technology with both modesty and earnestness. Though formally trained as a chemist and self-trained as a successful entrepreneur, "once an engineer always an engineer" as the saying goes. Moore offers an apt description: "Engineering is a series of failures with an occasional success."[74]

The concluding point is that the art of engineering is practiced widely and comes more from

the common desire and ability to solve problems that to the layperson may not seem significant or even important. But as repeatedly stated, this is the source of most progress in semiconductor technology.

Returning to the IC, as Hasty points out both AT&T and IBM, the two largest captive device makers, had initially decided against a monolithic[75] chip design, opting instead for miniaturized packaging architectures. Since these were both based on discreet components, there were foreseeable limitations. It was the promise of miniaturization that the monolithic IC brought that attracted the attention of the U.S. Government. Size, weight, and reliability considerations were critical in defense weapons systems such as missiles as well as in the rapidly growing space program. This resulted in the U.S. Government consuming practically all IC production for the first few years. This guaranteed demand subsidized not only research but costly production equipment and facilities. Kleiman (1966) catalogs the U.S. Department of Defense (DoD) and NASA requirements, stating that it was not until 1964 when Fairchild, supplier of the major share of Apollo program ICs, was the first to offer an off-the-shelf IC product line directly aimed at non-military, non-space markets.[76]

Over time, commercial demand for industrial controllers and computers along with new consumer products such as portable calculators and digital watches would displace military and space demand. But the infrastructure of IC production was greatly enhanced by early government consumption. As Michiyuki Uenohara et al (1984) point out:

> The integrated circuit was invented at precisely the time when an American response to Sputnik required new technology, and the needs of U.S. space and defense programs provided a unique opportunity for the development of these devices. The Minuteman missile program was committed in the early 1960s to the use of ICs, and this provided a base for development of ICs at high reliability levels and in large quantities. The

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[75] Monolithic refers to a single substrate material that all devices share. Kilby's lab notebook description would come to be known as "The Monolithic Idea." Source: Kilby, 2000, op. cit., 480.
[76] Herbert S. Kleiman, *The Integrated Circuit: A Case Study of Product Innovation in the Electronics Industry*, D.B.A. Dissertation, Washington, DC: George Washington University, 1966, 129.

> development of the semiconductor industry was significantly accelerated by the Minuteman program.[77]

Similarly, John Linvill and Lester Hogan, both Bell Labs alumni and key contributors during the early IC era, reflect on the significance of the Minuteman missile program to IC development:

> This [Minuteman] missile system poured hundreds of millions of dollars into the semiconductor industry at a very important time in its history. This money went into diffused transistors and integrated circuits; in particular, it provided funds necessary for the refinements to achieve a high level of reliability for semiconductor devices. All subsequent semiconductor systems benefited from the technological advances with the new levels of electronic reliability.[78]

Sam Harrell, VP at KLA-Tencor and former executive at Sematech and SEMI/Sematech, recalls with specificity the environment for ICs in the 1960s and briefly traces the changes in emphasis over three decades. According to Harrell the early to mid 1960s is best described as "government-centric," reflecting the emphasis on programs like the Minuteman missile just discussed. He underscores the large amount of defense funding prevalent at the time. He also states that early production processes were experimental, "In 1964 we had 0.6% yields."[79] The emphasis was to push performance at the expense of economics: proof of concept was the objective. The question at the time was: 'what could you do?' The fact was if you could make a technically better product, there was a market (i.e., government need). It was capability (technology) oriented with little reference to cost. Harrell sums up that era, "If you could make any, you could make money."[80] Then came the first commercial requirements in the 1967 timeframe in TV tuners, seat belt sensors, automotive electronics, and similar applications. For the first time economics was an important consideration. In consumer products like handheld calculators and digital watches, leverage came from higher yields. By this time TI had also

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[77] Michiyuki Uenohara, Tukuo Sugano, John G. Linvill, and Franklin B. Weinstein, "Background," in Okimoto, Sugano, and Weinstein (eds), op. cit., 10.
[78] John G. Linvill and C. Lester Hogan, "Intellectual and Economic Fuel for the Electronics Revolution," *Science*, New Series, Vol. 195, No. 4283, Electronics Issue, March 18, 1977, 1109-10.
[79] Sam Harrell, telephone interview, May 11, 2000.
[80] Ibid.

discovered learning curve behavior.[81] Firms worked harder to improve yields and achieve some target yield level. Harrell regards this period as "yield-centric" referring to 35% IC yields of the late 1960s as "sensational." This emphasis would continue for two and a half decades until the early 1990s. By this time yields had achieved 90% levels and thus gave way to other factors such as product design as areas for leverage.

By the mid 1960s IC production was becoming more widespread and a distinct pattern of innovation began to emerge. This pattern was a time-based regularity of circuit density doubling, first articulated by Gordon Moore in a famous log-linear plot extrapolating three historical data points ten years into the future. What Moore said in 1964/5 has become industry lore to the point where "Moore's Law"—as it later came to be known—embodied the very nature and essence of this industry. Sustaining Moore's Law has become so important to the industry that several hundreds of technical experts collectively work on an international industry Roadmap to maintain the historical cadence of density doubling. The process of how this cadence evolved from casual observation to strategic significance is complex and goes as follows.

Moore's Law

In 1965 Gordon Moore, then head of research at Fairchild, contributed a short, obscure article in *Electronics* magazine entitled "Cramming More Components Onto Integrated Circuits."[82] The magazine was publishing a 35th anniversary issue and had asked him me to predict what would happen in the semiconductor components industry over the next ten years. In the article he plotted on a log-scale (Figure 6-4) the few historical data points of Fairchild IC density and extrapolated a straight-line projection to 1975 based on continued annual density doubling.

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[81] Michael Rothschild, *Bionomics: Economy as Ecosystem*, New York: Henry Holt and Company, 1990, 180. According to Rothschild, the learning curve had languished in obscurity since World War II until 1966, when the Boston Consulting Group (BCG)—a recently formed consulting firm specializing in corporate strategic planning—conducted a study for a client in the semiconductor industry, presumably TI. BCG analysts found that, after adjusting for inflation, the unit costs for integrated circuits were dropping 25 percent with each doubling of experience. This cost erosion could not be attributed solely to improving labor productivity.

[82] Gordon E. Moore, "Cramming More Components Onto Integrated Circuits," *Electronics*, Vol. 38, No. 8, April 19, 1965, 114-117.

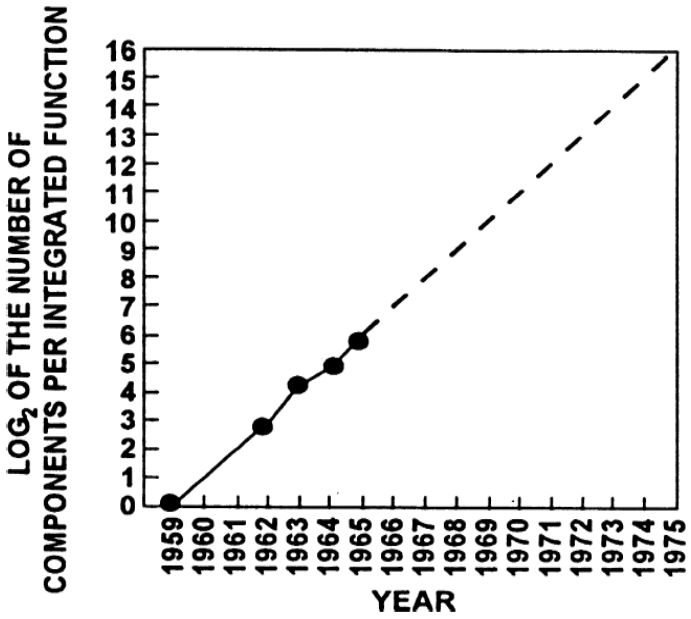

Figure 6-4. Original Moore plot from 1965 *Electronics* article

Source: Gordon E. Moore, "Cramming More Components Onto Integrated Circuits," *Electronics*, Vol. 38, No. 8, April 19, 1965, 116.

From this he predicted the possibility of 65,000 components per integrated circuit by 1975 (2^{10} times 1965 starting value). He joked later about the simplicity of his forecast method, "I really only had this much data: 3 data points."[83] He continued:

> I counted the one down here [1959], you see this was the first planar transistor which I consider the origin of all of this. And then the first few integrated circuits [1962, '63, '64], and I knew the one we were working on was the next point [1965]. So I just happened to look at those and they were about doubling. So the point I wanted to make was this trend was going to continue without thinking there was a heck of a lot of likelihood we would follow it. But it makes a fairly significant prediction. Here we're talking 32 components total [1964], and 10 years doubling every year is another thousand-fold, so this is a very long extrapolation, and it followed amazingly well.[84]

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[83] Moore interview, June 13, 1996. Note that the "3 data points" Moore refers to are the 1962, '63, and '64 points; he discounts the 1959 starting point and the 1965 point that was then still under development.
[84] Ibid.

Not as concerned then about the accuracy of his forecast, Moore wanted to emphasize the long-term ramifications of IC technology. "The big thing I was trying to push was that this integration was driving a major change."[85]

Although Moore is acknowledged as the one who best articulated it, many in the industry recognized the peculiar pattern of IC component density doubling.[86] However, as just discussed ICs in this timeframe were still in their infancy stage, used primarily for special-purpose defense and space applications. R&D was a critical variable and thus very costly. So long as demand from government contracts for high-priced chips supported industry R&D as well as the necessary learning for fabrication processes, advances that occurred were reflected in ever more complex chips. In time, fabrication processes began to improve as Harrell previously stated, but commercial demand for a high-volume product that could fully utilize the capability that these new devices offered was lacking. It's as if the technology (supply) led demand, most notably in a high-volume market segment where profits would be sufficient to fund subsequent development. Moore explains this situation as the primary impetus for leaving Fairchild to help start Intel in 1968:

> We got to the point in the late '60s where the processes were getting clean enough and the yields were getting high enough that we could make bigger things. The problem was nobody knew what to make. When we were making simple gates, or just a few gates, they tended to be fairly general purpose functions, but once you got into big blocks they tended to become unique; you only used them once in a computer or something. And the world was only making 10,000 computers total a year, so if you got one in every computer—which was very unlikely—the volume was so low that you couldn't amortize the design cost.[87]

In today's terms, what was missing was a 'killer application', some undeniable need that could justify expansion of development and production of ICs. New applications had appeared, and indeed were enabled by the IC (e.g., portable calculators, see Chapter 7) but these still tended to

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[85] Ibid.
[86] Erich Bloch, personal interview, March 25, 1996.
[87] Moore interview.

result in special-purpose development programs. Moore continues with the volume enabler that emerged: semiconductor memory.

> The opportunity we saw was that semiconductor memory could possibly replace magnetic cores in a lot of these applications if we could get the cost down enough, and that was a standard function that could use high complexity.[88]

With this vision of a high-volume, general-purpose product business model, Intel went on to introduce the first semiconductor memories, including the dynamic random access memory (DRAM). This product would later become the 'killer app' that the industry was searching for earlier. It would serve many purposes, not the least of which was the industry's 'technology driver'. Thus, the actual pattern of what came to be known as "Moore's Law" was still at least a decade away. Chapter 8 expands on Moore's Law.

MOSFET (MOS), CMOS, and Device Scaling

> "It is likely that the course of technological development depends more on the capability of MOS technology than on any other technical factor." (Carver Mead)[89]

Similar to the junction transistors that preceded them the first ICs were bipolar (short for bipolar-junction), built on layers of silicon with different electrical characteristics (see Figure 6-5a). In 1962 a *unipolar* IC was developed known as the MOSFET, which stands for metal-oxide semiconductor field-effect transistor; it is also simply referred to as MOS. The 'field effect' is key to the operation of a MOS transistor because, unlike in a bipolar design where current flows from collector to emitter through the base of the transistor when activated, in a MOS IC only the surface is active. Hence, no current flows through the MOS 'gate' but instead through a conducting 'channel' (i.e., within the dotted line area, referred to as the *depletion region*, of Figure 5-5b) that is insulated from the gate terminal by a layer of metal whose surface is oxidized.[90] Interestingly, MOSFET operates on the same principle as the original 'point contact' transistor,

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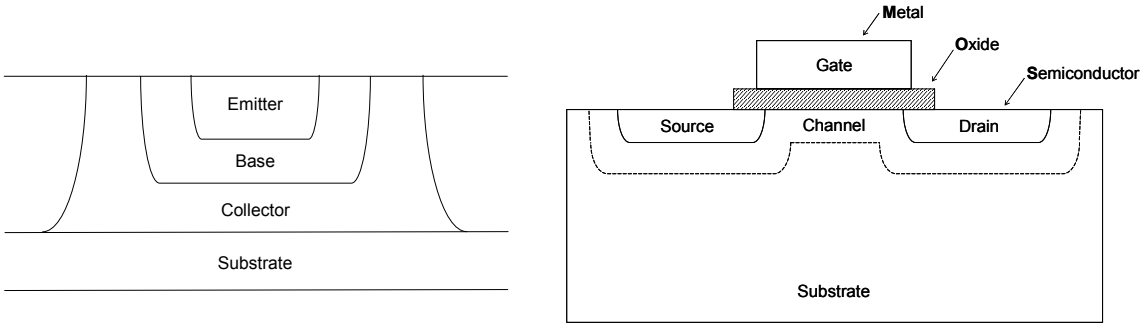
[88] Ibid.
[89] Carver A. Mead, "Scaling of MOS Technology to Submicrometer Feature Sizes," *Journal of VLSI Signal Processing*, 8, 1994, 9.
[90] This technical discussion draws heavily from Andres G. Fortino, *Workbench Guide to Microelectronics*, Reston, VA: Reston Publishing Co., Inc., 1985.

discovered by Bell Labs in late 1947, that also operated by field-effect. But the original transistor, although worthy of a Nobel prize, was an experimental design and would not be successfully commercialized. It would take roughly 15 years to fully understand and overcome inherent design problems such as surface effects that plagued these devices.[91]



(a) Simplified Bipolar Transistor Section (b) Simplified MOS Transistor

Figure 6-5. Bipolar and MOS Transistors

Visualizing a cross-section of a MOS transistor in a planar design (see Figure 6-5b) shows the metal gate (M) on top of an oxide insulation layer (O) which is on top of the semiconductor substrate (S), thus the 'MOS' acronym. The most basic function of a MOSFET is as a switch with the gate serving to open or close the current flow between source and drain junctions that have been formed within the semiconductor substrate. When the gate is activated a connection is made by electrical 'field effect' whereby a channel is created in the region just beneath the gate without actually making contact with it. As a basic electronics device, the gate of a MOS transistor acts as a capacitor, whereas the base in a bipolar transistor serves more as one side of two diodes, the other sides being the collector and emitter.

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[91] See, for example, Ross Knox Bassett, *New Technology, New People, New Organizations: The Rise of the MOS Transistor, 1945-1975*, Ph.D. Dissertation, Princeton University, January 1998, for a thorough analysis of 'surface effects' and other early MOSFET technology challenges.

This last point is important. Because no current (except a minute leakage current) flows through the gate, MOSFETs can be used to make circuits with very low power consumption. Another related advantage of MOS over bipolar technology is its much greater packing density as the basic device design also entails fewer elements (Figure 6-5a reveals only part of a bipolar transistor). Therefore, MOS devices require fewer production process steps and are less costly to make. The major disadvantage is that a MOS transistor performs significantly slower than a bipolar transistor, in part because of its more horizontal design. That is partly why, as Bassett's (1998) extensive study of the technology points out, it would take close to a decade from its first discovery before the widespread adoption of the technology.[92] Hasty concurs that MOSFET in the mid 1960s represented a major change and that a "big argument ensued over MOS vs. bipolar."[93] While the performance gap between MOS and bipolar was significant in the mid 1960s, by the mid 1970s the gap had narrowed significantly, hence MOS had proved the better product for all but the most high-performance applications.

There are two basic types of MOS technology based on how the substrate is charged (i.e., doped with impurities): *p*-type or *p*-channel (PMOS) and *n*-type or *n*-channel (NMOS) where 'P' refers to a positively-charged substrate and 'N' refers to a negatively-charged substrate.[94] Initially PMOS technology was used because it was easier and cheaper to work with as Ning, IBM research scientist, states:

> The reason is that p-channel is very immune to sloppiness in the process. You can do anything, there's lots of tolerance, and you don't need a super clean room. That's why everybody preferred it.[95]

With time, though, IBM switched to NMOS because it was intrinsically faster than PMOS—several times faster. Other computer manufacturers, then merchant chipmakers producers soon followed. In 1964 RCA invented CMOS (complementary MOS) technology specifically for avionics

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[92] Bassett, op. cit.
[93] Hasty interview, op. cit.
[94] There are variations of PMOS and NMOS technologies, but this level of explanation is not necessary here.
[95] Tak Ning, personal interview, July 18, 2000.

and aerospace applications because it had very low power consumption and excellent noise immunity. By 'complementary', CMOS technology uses a combination of a p-channel transistor and an n-channel transistor, combining both transistors within a single circuit. By using both n- and p-channel transistors in a normally-off state, it is possible to make circuits that only use significant power when switching. In this way CMOS offered considerable power-saving advantages. Performance of CMOS technology was also faster than PMOS but slower than NMOS.

As will be discussed in Chapter 7, these advantages were soon discovered to be ideal in portable electronics applications such as calculators, watches, and other consumer IC-based products. But it was the thousand-plus gate density requirements for DRAMs and microprocessors where MOS generally, and CMOS specifically, would bring the most promise. Although CMOS was invented and first used by American firms, Japanese IC makers embraced the early adoption of CMOS in consumer IC applications where low power was a greater consideration than performance. Leading U.S. chipmakers were more focused on improved performance for computer applications, thus bipolar and NMOS designs received more attention (e.g., IBM). This would later prove a critical advantage to Japanese chipmakers when DRAM chips would emerge as the industry's technology driver, based on CMOS process technology.

Estimates vary somewhat on the downstream uses of semiconductors between Japanese and U.S. manufacturers but there is little question that U.S. drew heavily on the computer and government defense and space sectors whereas Japan's primary demand was from the consumer sector. The U.S. concentration on performance-related applications helps explain why adoption of MOS (and especially CMOS) technology lagged Japan, where consumer demand for calculators, watches, radios, TV tuners and related items made up half of all semiconductor demand (see Table 6-3).

Table 6-3. Demand Sector Comparison of U.S. vs. Japan, 1982

End-use	United States	Japan
Computer	40%	22%
Telecommunications	21%	10%
Industrial	11%	17%
Military and aerospace	17%	0%
Consumer	11%	51%

Source: Yui Kimura, *The Japanese Semiconductor Industry: Structure, Competitive Strategies, and Performance*, Greenwich, CT: JAI Press Inc., 1988, Table III.7. Demand for Integrated Circuits by End-use Market, United States, Japan, and Western Europe, 1982 (includes captive consumption), 57, citing OECD, 1985.

By 1983-1984, the cost of CMOS had fallen below that of NMOS, and CMOS quickly became the clear technological choice for almost all applications.[96] By 1988, CMOS represented about 40% of the value of all IC production, and by 1994, CMOS was responsible for 80% of total production value.[97] Even in mainframe computing applications, where bipolar technology was used exclusively because of its superior performance qualities, CMOS has won out as Ning (2000) acknowledges:

> Every technology has its limits. For silicon, a vivid example is the limitation of bipolar technology for logic application. For more than twenty years, silicon bipolar was used in mainframe computers because of its raw circuit speed. However, the number of bipolar circuits that can be put on a chip is severely limited by their large standby power dissipation. This limitation is the main reason that mainframe computers are now made mostly using CMOS circuits which, although slower than bipolar circuits, allow a huge number of circuits to be integrated on a chip.[98]

Randy Isaac, VP of Systems, Technology, and Science for IBM Research, further explains the higher integration benefits as the factor that gave CMOS the edge over bipolar technology:

> [B]y the early 1990s, it was becoming clear that a large number of components on a chip could lead to superior system performance as well as lower cost per component. At high integration levels, functions that otherwise required many chips and complex system

---

[96] Richard N. Langlois and W. Edward Steinmueller, "The Evolution of Competitive Advantage in the Worldwide Semiconductor Industry, 1947-1996," Chapter 2 in David C. Mowery and Richard R. Nelson (eds.), *Sources of Industrial Leadership: Studies of Seven Industries*, Cambridge University Press, 1999, 44.
[97] Ibid., 48, primary source: ICE, 1995.
[98] Tak H. Ning, "CMOS in the New Millennium," IEEE Custom Integrated Circuits Conference, 2000, 49.

connections could be combined onto one chip. The net effect was improved chip performance as well as significant reduction in cost. Despite the raw transistor speed advantage, bipolar circuits had much greater power dissipation, and hence lower density, than CMOS circuits. Eventually, CMOS technology was able to achieve greater system-level performance, thanks to high integration levels, despite its inherently slower transistors.[99]

Isaac provides two comparisons between technologies that well illustrate how the overall performance of CMOS surpassed bipolar over time. Figure 6-6 plots the historical and future server performance trends using bipolar and CMOS circuits. The straight, dotted lines represent the time-averaged exponential improvement in the performance of the technology.

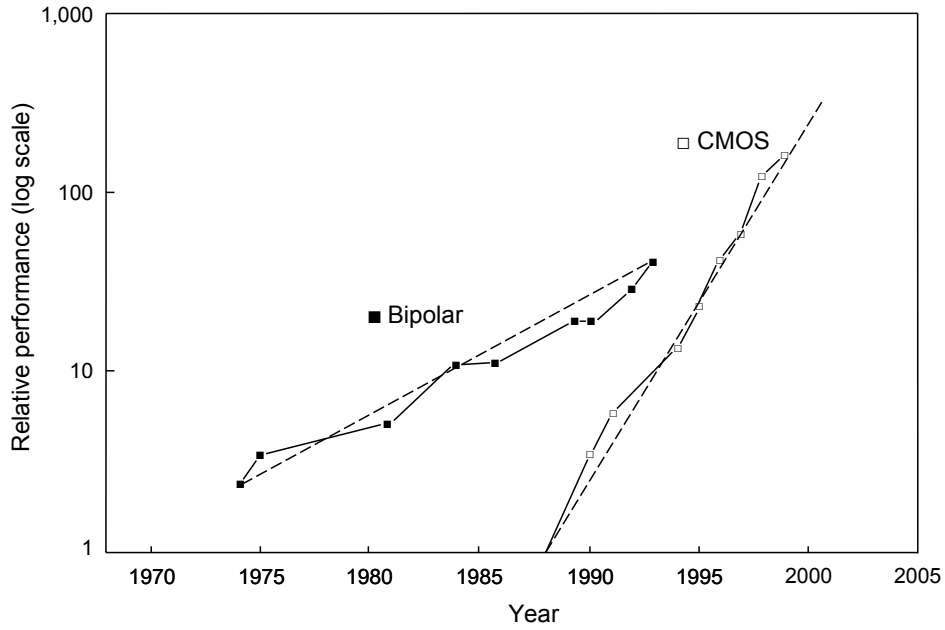

Figure 6-6. CMOS vs. Bipolar Server Performance

Source: R.D. Isaac, "The future of CMOS technology," *IBM J. Res. Develop.*, Vol. 44, No. 3, May 2000, 372, Figure 6, 375.

Table 6-4 compares physical characteristics of bipolar and CMOS-based IBM S/390 mainframe systems. According to Isaac, the G6 system, first shipped in 1999, offers more than

[99] R.D. Isaac, "The future of CMOS technology," *IBM J. Res. Develop.*, Vol. 44, No. 3, May 2000, 372.

double the performance of the fastest bipolar system shipped, and yet it contains dramatically fewer components and had much lower space and power requirements.

Table 6-4. Bipolar and CMOS-based IBM S/390 mainframe

	ES/9000 9X2*	*S/390* G6*
Technology	Bipolar	CMOS
Total no. of chips	5000	31
Total no. of parts	6659	92
Weight (lb)	31,145	2057
Power requirements (kVA)	153	5.5
Chips per processor	390	1
Maximum memory (GB)	10	32
Space (sq ft)	671.6	51.9

* Trademark or registered trademark of International Business Machines Corporation

Source: Source: R.D. Isaac, "The future of CMOS technology," *IBM J. Res. Develop.*, Vol. 44, No. 3, May 2000, 372, Table 1, 376.

The steady progress shown in Figure 6-6 is attributed in large part to device 'scaling', the ability of IC device feature sizes to be scaled down to smaller and smaller physical dimensions. According to Solomon and Tang (1979), also IBM researchers, bipolar scaling is considerably more complicated than MOSFET scaling "since the device itself is more complicated," thus the widening performance gap between technologies over time.[100]

Device Scaling Theory

Carver Mead, noted computer scientist, recalls the beginnings of scaling theory at the University of California at Berkeley:

> The thing that really got us started … I was sitting in Gordon's [Moore] office at Fairchild and he said you really should work out what happens as these things get smaller, how

[100] Paul M. Solomon and Danny D. Tang (IBM Corporation), "Bipolar Circuit Scaling," 1979 IEEE International Solid-State Circuits Conference, 1979, 86.

> they're going to scale. And so I did and I presented that in I think '68 in a little conference down at Lake of the Ozarks [Missouri]. And there were a bunch of good people there, some IBM people, some AT&T people there. And the IBM guys got on it, and they started doing work on it, and we did some work on it. And then there was enough going that people could see that these were correct calculations, that everything got better.
>
> So The IBM guys started working out a bunch of scaling stuff and that helped a lot because I wasn't the only one pushing it. And these other guys could be seen as from the industry; even though they weren't, they were from the research lab. But that research lab was more academic than at our university.
>
> And I had a student who was in the very first VLSI class in '71 whose name was Dick Pashley, and he went to work at Intel. And he was given the assignment to redo one of their little RAMs. And he figured out—he had been exposed to all this stuff—if he made the transistor smaller, and sized it down, then it would run a lot faster. And it did run a lot faster.[101]

Shortly after this Mead co-authored a paper with another of his students, Bruce Hoeneisen, that articulated the scaling assumptions and principal physical limitations of MOS transistors. The authors declared the possibility of ICs with up to 100 million transistors before reaching the limits of MOS technology:

> The channel length of a minimum size MOS transistor is a factor of 10 smaller than that of the smallest present day devices… It is thus possible to envision fully dynamic silicon chips with up to 10^7 to 10^8 MOS transistors per cm^2.[102]

This projection was plotted as a continuation of the original Moore plot (see Figure 6.4) as shown in Figure 6-7. This projection is significant in that—different than Moore's original extrapolation seven years earlier—there was now a theoretical understanding behind the future forecast (dotted line).

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[101] Carver Mead, personal interview, June 15, 1996.
[102] B. Hoeneisen and C.A. Mead, "Fundamental limitations in microelectronics. I. MOS Technology," *Solid-State Electronics*, Vol. 15, 1972, 819.

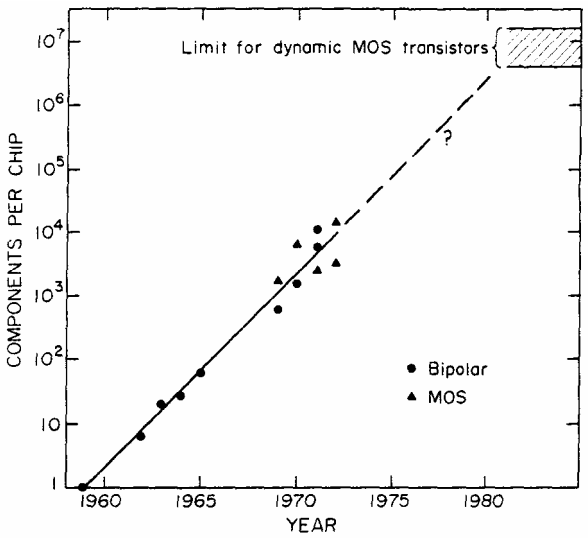

Figure 6-7. History of IC Complexity, circa 1972

Source: B. Hoeneisen and C.A. Mead, "Fundamental limitations in microelectronics. I. MOS Technology," *Solid-State Electronics*, Vol. 15, 1972, 819, Fig. 1 which reads "History of integrated circuit complexity. Line corresponds to a two-fold increase in the number of components per chip per year. This figure is due to Gordon E. Moore."

Meanwhile, work at the IBM Thomas J. Watson Research Center continued in earnest. The idea to develop scaling principles came out of an IBM project started in 1970 to develop an n-channel MOS chip at 1 micron dimension. Representing a manifold reduction in then-present feature sizes, 1 micron was a formidable technological challenge, and many believed the feat not possible as stated by Yu:

> As a matter fact, at that time in the early to mid '70s, people think 1 micron is a barrier - you can't go beyond that.[103]

This is consistent with the earlier quote by Ralph Cavin in Chapter 3's discussion on limits, "there were those prophets of doom who said, 'you will never get past 1 micron, it's against the laws of nature'." At the IEEE International Electron Devices Meeting (IEDM) in December 1972, IBM researchers first presented a set of scaling relationships that showed how a conventional device could be reduced in size to 1 micron dimensions. Then in October 1974 the classic paper

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[103] Hwa-Nien Yu interview, op. cit.

on scaling MOS integrated circuits appeared in the *Journal of Solid-State Circuits* that considered "the design, fabrication, and characterization of very small MOSFET switching devices suitable for digital integrated circuits using dimensions of the order of 1 μ."[104] In order to design such a device suitable for smaller channel lengths, the device was scaled by a transformation in three variables: dimension, voltage, and doping.[105] Rumelt (2003) summarizes the paper's key findings:

> Their surprising result was that if the electric field strength over the gate were held constant, simple reduction in scale of a MOSFET would work, and would produce improved performance on almost every dimension. In particular, if the linear dimension of the transistor were cut in half, then the voltage necessary was cut in half and the current flowing was cut in half. The power consumed was cut by a factor of four. The transistor density (number per unit area) was increased by a factor of four. Furthermore, the frequency of operation was doubled. (In addition, the doping concentration needed to make the device work doubled.)[106]

Written by Robert Dennard, Fritz Gaensslen, Hwa-Nien Yu, Leo Rideout, Ernest Bassous, and Andre LeBlanc, all IBM research scientists, the paper is frequently referenced and in fact, is the most often cited article in the history of *JSSC* because it contains the first publication of a unified set of principles for scaling MOS transistors and integrated circuits to increasingly smaller dimensions.[107]

According to lead author Robert Dennard, "The idea of scaling all physical dimensions of a MOS device along with proportional changes of voltage and substrate doping is remarkably simple and concise, yet very powerful. It predicts significant improvement in speed and reduction of power consumption along with the profound cost advantage of fabricating many more transistors on each silicon chip."[108] Ning, who was later involved in the 1 micron project, states that this research was based on n-channel MOS, a technology IBM would pioneer as a superior

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[104] Robert H. Dennard, Fritz H. Gaensslen, Hwa-Nien Yu, V. Leo Rideout, Ernest Bassous, and Andre R. LeBlanc, "Design of Ion-Implanted MOSFET's with Very Small Physical Dimensions," *IEEE Journal of Solid-State Circuits*, Vol. SC-9, No. 5, October 1974, 256.
[105] Ibid., 258.
[106] Richard P. Rumelt, "Gordon Moore's Law (A Case Study)," The Anderson School at UCLA, POL-2003-03, 2003.
[107] JSSC Classic Paper: Scaling Enabled Moore's Law http://www.ieee.org/organizations/pubs/newsletters/sscs/oct02/jssc.html
[108] Ibid.

alternative to PMOS and even CMOS in terms of performance. He describes the basic questions addressed through scaling research:

> You make something in large dimension, you optimize it until you like it. Now when you make them small, how do they behave? What is it that you need to do to preserve the behavior the way you want?[109]

As chip designers better understood that there was an underpinning *theory* behind scaling, this knowledge would be incorporated in new designs and a distinct pattern of technical advance that had emerged in the 1960s became even more pronounced in the 1970s and 1980s. A type of cadence or regularity emerged as shown in Table 6.5.

Table 6-5. Progress in IC Minimum Feature Size

Year	Minimum Feature Size (microns)	Size of Memory Chip Possible
1959	100.0	
1962	25.0	
1964	12.0	1K
1972	6.0	4K
1974	5.0	16K
1977	4.0	64K
1983	2.0	256K
1987	1.3	1M
1990	.8	4M
1995	.5	16M

Source: William Edward Steinmueller, *Microeconomics and Microelectronics: Economic Studies of Integrated Circuit Technology*, Ph.D. Dissertation, Stanford University, March 1987, Table 4.6.1, 221; citing (1959-1977) George Marr, "Perspectives on MOS Directions," in *Fifteenth IEEE Computer Society International Conference* (Washington, D.C., September 6-9, 1977): 243; and (1983-1995) William J. McClean (ed.), *Status 1986: A Report on the Integrated Circuit Industry* (Scottsdale, AZ: Integrated Circuit Engineering, Inc., 1986), 76.

[109] Ning interview, op. cit.

It will be shown in Chapter 8 that this cadence would be labeled "Moore's Law" as a type of validation of the crude scaling projection referred to in Figure 6-4 as the original Moore plot.

Viewed individually, the planar process, the IC, and MOS/CMOS technology were crucial innovations to the success of the semiconductor industry. But considering them collectively, the overall impact is immeasurable. These three innovations from the 1960s underpin the technological trajectory that has defined the industry ever since. Chapter 7 that follows examines another important technological innovation, the microprocessor, in detail as an attempt to demonstrate some of the prevailing knowledge, skills, and context that existed at the time. By considering these aspects, the invention (and innovation) of the microprocessor is not as straightforward as the popular description implies.

CHAPTER 7: The *Invention* of the Microprocessor, *Revisited*

"Facts are stubborn things; and whatever may be our wishes, our inclinations, or the dictates of our passions, they cannot alter the state of facts and evidence."

- John Quincy Adams

Table 7-1. Selected Quotes Involving Invention of the Microprocessor

"The 4004, invented by Intel, was the world's first commercially available microprocessor." (Intel website)[1]	"TI invents the single-chip microcomputer and receives the first patent for the single-chip microprocessor, ushering in the personal computer era." (Texas Instruments website)[2]
"The first microprocessor in a commercial product was Lee Boysel's AL1, which was designed and built at Four-Phase for use in a terminal application in 1969." (Nick Tredennick)[3]	"Alongside to the IC, the invention of the 'micro-processor' (MPU - Micro Processing Unit) is the greatest invention of the 20th century in the field of electronics." (Busicom Corp.)[4]
"[T]he idea of putting the computer on a chip was a fairly obvious thing to do. People had been talking about it in the literature for some time, it's just... I don't think at that point anybody realized that the technology had advanced to the point where if you made a simple enough processor, it was now feasible." (Ted Hoff)[5]	"Having been involved with integrated electronics when I was at Intel, we never conceived of patenting a computer on a chip or CPU on a chip, because the idea was patently obvious. That is you worked on a processor with 25 chips, then 8 chips, and by-God eventually you get one chip so where's 'the invention'." (Stan Mazor)[6]
Such inventions don't come from new scientific principles but from the synthesis of existing principles… Because these inventions have a certain inevitability about them, the real contribution lies in making them work. (Federico	"[A]t the time in the early 1970s, late 1960s, the industry was ripe for the invention of the microprocessor. With the industry being ready for it, I think the microprocessor would have been born in 1971 or 1972, just because the

[1] "Intel Consumer Desktop PC Microprocessor History Timeline," http://www.intel.com/pressroom/archive/backgrnd/30thann_timeline.pdf
[2] "History of Innovation: 1970s," http://www.ti.com/corp/docs/company/history/1970s.shtml
[3] Nick Tredennick, "Technology and Business: Forces Driving Microprocessor Evolution," *Proceedings of the IEEE*, Vol. 83, No. 12, December 1995, 1647.
[4] "Innovation: The World's first MPU 4004," http://www.dotpoint.com/xnumber/agreement0.htm
[5] Ted Hoff as quoted in Rob Walker, "Silicon Genesis: Oral Histories of Semiconductor Industry Pioneers, Interview with Marcian (Ted) Hoff, Los Altos Hills, California," Stanford University, March 3, 1995.
[6] Stan Mazor, Stanford University Online Lecture, May 15, 2002, 020515-ee380-100, http://www.stanford.edu/class/ee380/

Faggin)[7]	technology and the processing capability were there." (Hal Feeney)[8]
"I don't think anyone 'invented' the microprocessor. Having lived through it, this [claim] sounds so silly." (Victor Poor)[9]	"It is problematic to call the microprocessor an 'invention' when every invention rides on the shoulders of past inventions." (Ted Hoff)[10]
"Most of us who have studied the question of the origin of the microprocessor have concluded that it was simply an idea whose time had come. Throughout the 1960's there was an increasing count of the number of transistors that could be fabricated on one substrate, and were several programs in existence, both commercial and government funded, to fabricate increasingly complex systems in a monolithic fashion." (Robert McClure)[11]	"The question of 'who invented the microprocessor?' is, in fact, a meaningless one in any non-legal sense. The microprocessor is not really an invention at all; it is an evolutionary development, combining functions previously implemented on separate devices into one chip. Furthermore, no one individual was responsible for coming up with this idea or making it practical. There were multiple, concurrent efforts at several companies, and each was a team effort that relied on the contributions of several people." (*Microprocessor Report*)[12]
"The emergence of microprocessors is not due to foresight, astute design or advanced planning. It has been accidental." (Rodnay Zaks)[13]	"The only thing that was significant about the microprocessor was that it was cheap! People now miss this point entirely." (Stan Mazor)[14]

Each of the statements in Table 7-1 is backed by the credibility of the individuals and/or organizations that made them. Most were key contributors in the early inventive activities that brought forth the microprocessor, "the greatest invention of the 20th century in the field of electronics," as Busicom claims. Box 3-2 in Chapter 3 briefly discussed the innovation of Intel's first microprocessor (i.e., the 4004) as the start of a technological trajectory of a since-strategic

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[7] Federico Faggin, "The Birth Of The Microprocessor: An invention of major social and technological impact reaches its twentieth birthday," *Byte*, Volume 2, 1992, 145, http://www.uib.es/c-calculo/scimgs/fc/tc1/html/MicroProcBirth.html

[8] "Microprocessor pioneers reminisce: looking back on the world of 16-pin, 2000-transistor microprocessors," *Microprocessor Report*, Vol. 5, No. 24, December 26, 1991, 13(6). Hal Feeney helped design the 8008 at Intel.

[9] Vic Poor, former vice president of research R&D for Datapoint, telephone interview with the author, June 5, 2003.

[10] Dean Takahashi, "Yet Another 'Father' of the Microprocessor Wants Recognition From the Chip Industry," *Wall Street Journal*, September 22, 1998, http://www.microcomputerhistory.com/f14wsj1.htm

[11] See e-mail/newsgroup posting to Dave Farber's IP list dated May 12, 2002 to Dave Farber dave@farber.net McClure was formerly with TI and helped found CTC; he also was an expert witness in the Boone patent case.

[12] Microprocessor Report, op. cit.

[13] Rodnay Zaks, *Microprocessors: from chips to systems*, 3/e, SYBEX Inc., 1980, First Edition Published 1977, 29.

[14] Stan Mazor, telephone interview with the author, June 10, 2003.

product family that has witnessed astonishing increases in overall capability and complexity. Intel proudly asserts—and it is generally accepted—that the 4004 was the *first* microprocessor in the industry, thus they claim priority in this important invention. While this author has neither the evidence nor desire to dispute this claim, what is pointed out is that the "invention" of the microprocessor, although celebrated since as a major historical event by Intel and others, was really viewed at the time as an evolutionary—even expected—improvement within the industry as the last several quotes indicate. In contrast, the first set of quotes reveals how widely views are (were) held about the discovery and its significance. An interesting point worth noting here is that Intel did *not* file a patent for the 4004 as a microprocessor as the development did not seem that significant to them at the time.[15] Moore reflects:

> [F]rankly, we didn't think the microprocessor *per se* was that patentable. What we had done was take a computer architecture and make it all on one chip instead of on several chips. And that was kind of the direction that the integrated circuit technology was pushing in anyhow, always putting more and more of the system on a chip.[16]

Furthermore, it is quite possible that others "got there first" and for reasons clear and not so clear did not disclose of their discovery. A fuller account reveals that there were many others involved, from organizations large and small and from a variety of industrial sectors. While it is not possible to recount every contribution, it does seem reasonable and necessary to cite some of these contributions, at least as footnotes, in the complex story of the invention of the microprocessor. Hence, the purpose of this analysis is to underscore the incremental (or normal) innovation pattern built upon accumulated knowledge that so characterizes this industry, in contrast with what many (most) have since referred to as a revolutionary or discontinuous

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[15] Note that U.S. Patent 3,821,715, "Memory System for a Multi-chip Digital Computer," filed January 22, 1973 by Marcian Edward Hoff, Jr., Stanley Mazor, and Federico Faggin of Intel Corporation, was issued June 28, 1974 and described the 4004 chip set, but not the embodiment of single-chip CPU. Rather, the emphasis was on "how we did it," in 16 pin packages, a major feat at the time. Source: Stan Major telephone interview, op. cit.; see also Stanley Mazor, "The History of the Microcomputer - Invention and Evolution," *Proceedings of the IEEE*, Vol. 83, No. 12, 1600-1608, December 1995, http://www.dotpoint.com/xnumber/Microcomputer_invention.htm "The Intel patent on the MCS-4 (Hoff, Faggin, Mazor) has 17 claims, but the single chip processor is not claimed as an invention."

[16] Gordon Moore, in interview at Stanford University, "Silicon Genesis: Oral Histories of Semiconductor Industry Pioneers," March 3, 1995, online at http://www.stanford.edu/group/mmdd/SiliconValley/SiliconGenesis/GordonMoore/Moore.html

innovation. In this way, the innovation practices employed today under the guise of an industry roadmap and collaborative research programs are not that much different than in the late 1960s and early 1970s era, except perhaps in the nature of knowledge sharing.

In writing about the fruitful, yet widely unknown, engineering career of Jack Avins at RCA, Goldstein (1997) cautions, "History, as the word reminds us, is a story, and dramatic stories are always the most popular."[17] An early excerpt from Malone's (1995) book with the clever title, "The Microprocessor: A Biography," also takes issue with the bias of popular histories:

> Not that the text diverges from the facts—on the contrary—but it certainly doesn't fit with the received view as presented in corporate brochures and "official" histories. High technology rarely looks back; and when it does, it usually has a selective memory. The engineering mind would much rather see history as the stately advance of technology by brilliant minds. But the world doesn't work that way. It is far more messy than any blueprint.[18]

Consistent with a key theme of this research that the great advances in semiconductor technology have come from day-in, day-out engineering work, Goldstein states:

> But this tendency to focus only on the engineering stories that spill out of their technological domain into the courts of law or the corporate executive suites shortchanges the inventors whom it drives out of the limelight, and interferes with a correct understanding of the nature of technological progress. More meaningful and more revealing are the longer sagas of steady research, punctuated by regular triumphs, that characterize the bulk of engineering work.[19]

Indeed, there have been court battles over the invention of the microprocessor. At least two other individuals have sought legal action for recognition while another has been acknowledged by industrial historians as developing an 8-bit chip before Intel's 4-bit 4004. Still another account of the organization that brought Intel the request for their second chip, the 8-bit 8008, raises questions as to who should be credited with the original "idea." Moreover, continuous innovations within firms that designed and manufactured calculators, data terminals, computers and related

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[17] Andrew Goldstein, "Jack Avins: The Essence of Engineering," in Andrew Goldstein & William Aspray (eds.), *Facets: New Perspectives On the History of Semiconductors*, New Brunswick, NJ: IEEE Center for the History of Electrical Engineering, 1997, 133.
[18] Mike Malone, *The Microprocessor: A Biography*, Santa Clara, CA: Telos, 1995, xii.
[19] Goldstein, op. cit., 133.

products brought forth advances in large-scale integration (LSI) technologies, which at the very least suggested the microprocessor as an eventual outcome.

Invention vs. Innovation

The process of technological innovation, along with a variety of models of innovation, was discussed in depth in Chapter 4. Recall that innovation involves the introduction or commercialization of an invention, thus other factors must be considered in analyzing the innovation process. Like innovation the process of invention is also complex, however by examining a subset of the broader process—through a reexamination of a very important semiconductor invention—new insights can be revealed about what factors contribute to technological advance. While many of the above claims refer to the *invention* of the microprocessor (and generally most attribution is given to Intel), this examination shows that priority claims are not that clear and, in fact, it is most likely that no *one* can rightfully claim the invention. What is more clear though is that Intel was probably the first successful *innovator* of the microprocessor, finding application in a variety of industrial and commercial products such as the PC.

The early work of Usher (1959/1929) provides some basis to guide this analysis of microprocessor invention. Usher starts by stating the obvious, "A theory of invention must address itself to the basic question: how do new things happen?"[20] He then challenges the idea that historical development is attributed solely to the inspiration of genius or what he refers to as the "great-man theory of history," as previously discussed.[21] He acknowledges that while some inventions may have occurred in this way, most inventions occur more as a cumulative process involving the synthesis of many previous inventions. The incremental or normal pattern of semiconductor innovation underpinning this research is consistent with Usher's view. The microprocessor, as a distinct artifact, is no exception and will be featured here, to use Usher's

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[20] Abbott Payson Usher, *A History of Mechanical Inventions*, Boston: Beacon Press, 1959, 60.
[21] Ibid., see Chapter 3.

words, as a *strategic invention*. To begin Usher offers a general theory of invention, labeled as Gestalt analysis that places the role of inventor in new light. The following passage is revealing:

> The Gestalt analysis presents the achievements of great men as a special class of acts of insight, which involve synthesis of many items derived from other acts of insight. In its entirety, the social process of innovation thus consists of acts of insight of different degrees of importance and at many levels of perception and thought. These acts converge in the course of time toward massive syntheses. Insight is not a rare, unusual phenomenon as presumed by the transcendentalist; nor is it a relatively simple response to need that can be assumed to occur without resistance and delay. The Gestalt analysis thus presents an essentially new concept of the place of the individual in society. He is neither the romantic leader or reformer that frees people from paralyzing traditions, nor the passive instrument of cosmic forces that is implied by so many deterministic sociologies.[22]

Next, he provides a model that incorporates a genetic process involving four steps as shown in Figure 7-1 and briefly described here.[23] The first step is the perception of a problem, conceived as an incomplete or unsatisfactory pattern symbolized by an incomplete circle that typically stems from an unfulfilled want. Usher calls the second step 'setting of the stage' represented by an almost-complete circle (i.e., an offset arc of a circle separated slightly from the gap in the incomplete pattern). For the general process of invention this step is dependent upon pure chance, or upon the mediated contingency of a systematic effort to find a solution by trial and error. The third step, shown by a completed circle, is referred to as the 'act of insight' where the essential solution of the problem is found. Step 3, however, does not end the process as a solution must be studied critically, understood in its fullness, and learned as a technique of thought or action. He describes this fourth and final step as 'critical revision', represented by a complete, but more massive (bolded), circle.

Furthermore, his idea of progressive synthesis is shown by arrows leading in toward the various steps in the process. Usher emphasizes that the process is legitimately conceived as a whole, because it rests upon a sequence that is explicitly genetic, however he acknowledges that discontinuities in time and indeterminate resistances do occur.

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[22] Ibid., 61.
[23] This section draws heavily on ibid., 65-69.

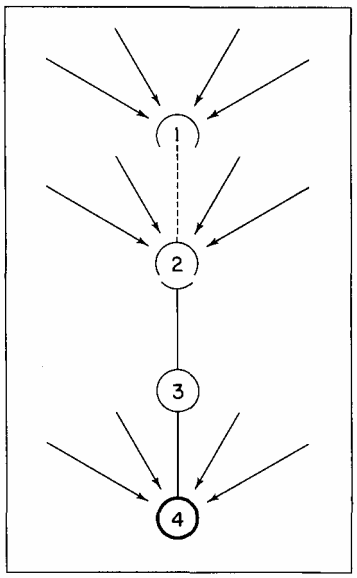

Fig. 7. The emergence of novelty in the act of insight: synthesis of familiar items: 1, perception of an incomplete pattern; 2, the setting of the stage; 3, the act of in sight; 4, critical revision and full mastery of the new pattern.

Figure 7-1. Usher's Emergence of Novelty

Source: Abbott Payson Usher, *A History of Mechanical Inventions*, Boston: Beacon Press, 1959, Figure 7, 66.

Usher states that emergent novelty becomes truly significant only through cumulation (i.e., cumulative synthesis of preceding inventions). He extends his generalized model to describe the achievement of *strategic* invention, which involves all the separate steps found in the emergence of a single item of novelty (Figure 7-1). However, a strategic invention involves synthesis on a high level, comprising both new and old elements. In challenging conventional descriptions of significant industrial age inventions, he cites the history of printing, the steam engine in various forms, and the power-driven airplane as examples that were generally mischaracterized. These and other popular historical accounts rest upon the false assumption that the particular achievement was so simple and specific that it could properly be identified with the work of a single person at a given moment. Usher argues the impossibility of attributing any one person with a particular strategic invention:

> These popular attitudes are justified in their emphasis upon the special importance of some inventions. The position is not really inconsistent with the concept of a massive social process of cumulative synthesis. The social process as a whole may be described as a sequence of strategic inventions which draw together many individual items of

> novelty as well as many familiar elements. The history of the reciprocating steam engine involves at least five strategic inventions: the atmospheric engine of Newcomen; the low-pressure engine of Watt; the high-pressure engine of Trevithick and Evans; the steam locomotive of Hackworth and Robert Stephenson; the compound engines. In many instances, it is not possible to cite a single inventor even for a particular stage in this long development. There are quantitative differences in the achievement which admit, and really require, differentiation in the description of the accomplishment.[24]

Usher then describes the process of cumulative synthesis with an enhanced model shown in Figure 7-2. In the diagram, the development of the strategic invention is symbolized by the large arcs or circles, marked with Roman numerals. Arrows converging toward the focal points of synthesis are designed to suggest the incorporation of familiar items in the new synthesis. The number of items involved at each step is purely arbitrary. The diagram merely indicates the combination of “several” or “many” items, familiar and novel, at each stage in the process. This particular diagram shows one complete sequence in strategic invention (I-IV), and part of another (second I-II). Finally, he states: "In historical analysis, it would be unusual *not* to find that several strategic inventions were involved in any achievement of large social importance."[25] Indeed, the microprocessor easily fits as a (*the?*) contemporary example of strategic invention. As will be shown, numerous advances in semiconductor design and manufacture, calculator and computer architectures, software development, and system integration paved the way to the invention of the microprocessor. With Usher's theory of invention as a guide, this important achievement may be better understood.

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[24] Ibid, 68.
[25] Ibid., 69, emphasis added.

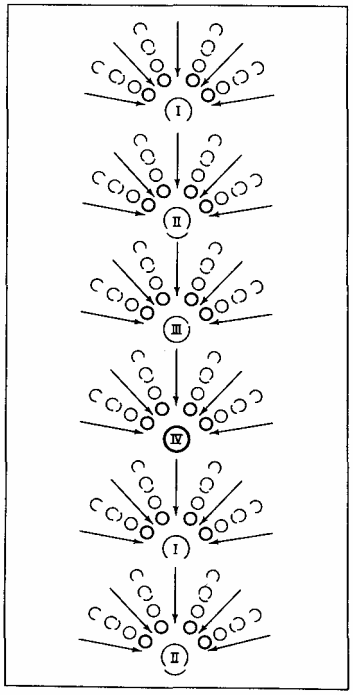

Fig. 8. The process of cumulative synthesis. A full cycle of strategic invention, and part of a second cycle. Large figures I-IV represents steps in the development of a strategic invention. Small figures represent individual elements of novelty. Arrows represent familiar elements included in the new synthesis.

Figure 7-2. Usher's Process of Cumulative Synthesis

Source: Abbott Payson Usher, *A History of Mechanical Inventions*, Boston: Beacon Press, 1959, Figure 7, 69.

This analysis looks back to the late 1960s and early 1970s with a perspective that draws on a variety of sources. What will be demonstrated is that the combined efforts of many talented engineers, scientists, and others brought forth a particular artifact that, in retrospect has been distorted somewhat by time and fortune. Furthermore, what guided their efforts towards the outcome of a so-called microprocessor was an implicit roadmap that all understood and in their own way helped contribute to its realization. As has been argued elsewhere in this thesis, a roadmap combines accumulated knowledge of past achievements along with the incorporation of novelty through a shared consensus process within an innovation community. This has been the heritage of semiconductor technology from almost the start, at least a decade before formal roadmapping practices came into being. Usher's *cumulative synthesis* and *strategic invention* explanations seems to anticipate a roadmapping process, particularly an industry-level roadmap.

The analysis begins with a summary of a few of the more publicized claims of invention. Following this is a detailed historical account of the Datapoint 2200 and the Intel 8008. The next section addresses the significant role of calculator applications with a particular emphasis on early HP calculators. The section concludes with a brief examination of the multiple microprocessor-related patents that were filed before Intel's 8080 patent to illustrate the kind of thinking that was going on during the era when the "invention" occurred. The introduction of the 8080 is a defining point in the history of the microprocessor as it represents the beginning of the *general purpose* microprocessor era that continues to the present, thus usually garners most of the attention.

I. Alternative Claims to the Invention

Raymond Holt claims that in 1969 he and a team of 25 engineers created the first microprocessor, for the U.S. Navy's F-14A "Tomcat" fighter jet, at a time when Intel's effort was just beginning. The first F-14A took off on December 21, 1970 with Holt's system operational. Holt, who directed the F-14A flight-computer-chip design team with another engineer, Steven Geller, kept the nature of his achievement quiet all these years because the work was classified by the U.S. Navy. "We were thrilled [at the discovery], but we couldn't tell anyone," Mr. Holt says.[26] Holt's design was actually three processor chips (supported by three other chips) since the application involved calculating air speed, wing position, and altitude simultaneously, a much harder task than supporting calculator functions as in the case of the 4004. A team of six engineers at American Microsystems, Inc. (AMI) of Santa Clara, CA, did all the chip circuit design and layout for the MP944 microprocessor chip set. (AMI will figure in later in this chapter as a key supplier of ICs for HP scientific calculators.) Holt has likened the MP944 design to a high-priced Cadillac in comparison to a Ford (i.e., Intel's 4004).[27] Intel disagrees. Speaking for the 4004 development team, Ted Hoff states, "I still consider the 4004 as the first microprocessor. [It was]

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[26] Takahashi, 1998, op. cit.
[27] Dean Takahashi, "Paternity Suit," Electronic Business, January 1, 1999, http://www.e-insite.net/eb-mag/index.asp?layout=article&articleid=CA66397

the first computer central processor on a chip. In our view, it had to be a single chip."[28] But this "view" of what constituted a microprocessor did not exist at the time and in fact was not defined for years. Recall that the 4004 was one of a four chip set.[29] According to a microprocessor patent filed by the RCA Corporation in 1974 (and referencing a patent application by the same inventor and assignee from 1972), a definition of a microprocessor was offered:

> A microprocessor is a device capable of performing arithmetic, logical, and decision making operations under the control of a set of stored instructions, but of small size, capable of being manufactured on a few (not more than four) integrated circuits.[30]

Even the Intel 8008, a concurrent 8-bit microprocessor project (that will be discussed soon in detail) required a number of support chips to operate in a minimum configuration as Noyce and Hoff describe, "Requiring a minimum of 20 TTL packages for memory and I/O interface, the 8008 could address 16K bytes of memory."[31]

Circa 1970 most competing processor designs (e.g., in popular minicomputers) comprised several MSI (medium scale integration) chips, such as the TTL packages just referenced, usually residing on a single (or few) printed circuit board(s). In fact, when DEC introduced its LSI-11 in 1975, the first 16-bit microprocessor-based minicomputer employing the PDP-11 instruction set, the LSI-11 "chip set" as it was called, consisted of four 40-pin chips (of which one was the control chip).[32] Conceptually at least, a microprocessor was not synonymous with a single chip until the mid to late 1970s. In fact, it would take Intel 5 years and three designs after the 4004 to produce the 8085, its first true single-chip microprocessor in 1976.

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[28] Ibid.
[29] According to Stan Mazor, only two chips of the four chip set were needed for a minimum system (i.e., 4004 CPU and 4001 ROM). The 4002 RAM was needed if there was user data and the 4003 I/O port shift register was incidental. Stan Mazor, e-mail to the author, July 30, 2003.
[30] Joseph A. Weisbecker, "Microprocessor Architecture," U.S. Patent 3,970,998; assignee: RCA Corporation, New York, NY; filed October 15, 1974, issued July 20, 1976; relates to U.S. Patent 3,798,615, filed October 2, 1972, issued March 19, 1974 by the same inventor and assigned to the same assignee as this application.
[31] Robert N. Noyce and Marcian E. Hoff, Jr., "A History of Microprocessor Development at Intel," *IEEE MICRO*, February 1981, 13. TTL stands for transistor-transistor logic, a popular bipolar logic design at the time.
[32] The LSI-11 was initially manufactured by Western Digital as the MCP 1600. In 1977 the author developed the maintenance plan and conducted the first field service training on the DEC Datasystem 320, a desk-enclosed business system that employed the PDP-11/03 (LSI-11 chip set) processor. By 1980 DEC was manufacturing the LSI-11 chip set at a special facility in Hudson, MA.

Gilbert Hyatt is a largely unknown systems designer, electronics engineer, and aerospace consultant who was granted patent #4,942,516 for a "Single Chip Integrated Circuit Computer Architecture" in 1990 after a 20-year battle with the U.S. Patent Office. According to Hyatt, the patent established him as the one who invented the microprocessor.[33]

In 1968, according to Hyatt, he built the first breadboard for a new type of small computer in his home. "I trademarked the name microcomputer, because it was a computer smaller and more efficient than the minicomputer." Hyatt formed a company called *Micro Computer* and built his first working computer later that year. He obtained venture capital financing from several sources, including Robert Noyce and Gordon Moore, both of whom were to play important parts in the creation of the microprocessor. "We had brought in—or I should say, the finder for the financing brought in—Dr. Noyce and Dr. Moore, the Intel founders," says Hyatt. "Essentially, we needed access to a chip-making capability so that we could put my computer on a chip." The "effective date" of Hyatt's patent filing is December 28, 1970, for a computer on a chip—the microcomputer having a CPU, operand memory, and ROM on an IC chip. In 1971, after a dispute over Hyatt's refusal to assign the financial backers rights to his patents, the firm went out of business.[34]

Hyatt's patent was invalidated in 1996 (and upheld on appeal in 1998) in a patent interference case brought forth by Texas Instruments, on account that the device it described was never implemented and was not implementable with the technology available at the time of the invention.[35] According to Richard Donaldson, senior vice president and general patent counsel for TI:

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[33] Author unknown, "Micro, Micro: Who Made The Micro?" *Byte*, January 1991, http://www.uib.es/c-calculo/scimgs/fc/tc1/html/WhoMadeTheMicro.html
[34] Ibid.
[35] "The Gilbert Hyatt Patent," http://www.intel4004.com/hyatt.htm and "TI Invented Famous 'Computer on a Chip' Before Gilbert Hyatt -- Hyatt v. Boone 96-1514, 1515," June 1998, http://www.ipo.org/2001/fedcirsum1998.htm

> This ruling rightfully establishes Gary Boone and TI as the inventor of the single-chip microcontroller, settling the broad speculation that followed after Mr. Hyatt received a patent. Gilbert Hyatt has absolutely no claim on the invention.[36]

Gary Boone, who successfully overturned the Hyatt patent, is a former Texas Instruments engineer. In 1971 he was involved in the invention of TI's first microprocessor and received the first patent for one:

> After months of work, Boone and his coworkers completed building the first working computer-on-a-chip in the early morning hours of July 4, 1971. Two weeks later, TI filed a patent application, which resulted in the series of patents issued, beginning in 1978, naming Boone as the inventor.[37]

The first patent was actually granted in 1973 which allows TI to claim "TI invents the single-chip microcomputer and receives the first patent for the single-chip microprocessor," as quoted at the very beginning.[38] The "computer-on-a-chip" referred to in the above statement is actually an alternatively designed chip (part of a chip set) for the Datapoint 2200 single-chip design request of Intel. As is well known, TI's chip did not work properly and Datapoint did not accept it. The chip was advertised but was never sold. This will be discussed in more detail shortly.

Also important is that TI had been actively seeking commercial applications in order to stimulate demand for the fledgling IC. Recall that U.S. military and space programs were practically the sole sponsors of IC manufacturers including especially TI well into the 1960s. Realizing government demand would not be sustaining, hand-held calculators were selected as one of the first applications for commercial IC use. Challenged by the CEO and Chairman of TI, Jack Kilby himself was requested to design a calculator as powerful as the large, electro-mechanical desktop models of the day, but small enough to fit in a coat pocket. In 1967 Kilby and two colleagues completed a prototype of the first hand-held calculator and filed a patent application shortly thereafter. The U.S. Patent Office issued patent number 3,819,921 on June

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[36] Richard Donaldson, "Texas Instruments: They invented the Microcontroller - U.S. Patent Office Rules TI Engineer Invented Computer-On-A-Chip," http://www.datamath.org/Story/Intel.htm#Texas%20Instruments:%20They%20invented%20the%20Microcontroller

[37] Ibid.

[38] Gary W. Boone, "Computing Systems CPU," U.S. Patent 3,757,306; assignee: Texas Instruments Incorporated, Dallas, TX; filed August 31, 1971, issued September 4, 1973.

25, 1974.[39] Kilby's calculator design work would be refined and TI ultimately introduced a single MOS IC "calculator-on-a-chip" in September 1971. Boone was also involved in this project. This chip became the basis for the TMS100 microcontroller, a very successful chip for which TI holds several patents.[40]

It is important to note the distinction here between a *microcontroller* and *microprocessor*. Neither term was actually used then, however *microcomputer* does appear in the historical record (e.g., see Hyatt's earlier reference). A microcontroller would later be defined as a chip for *special* purpose applications (e.g., for calculators or other commercial or industrial uses), whereas a microprocessor would typically connote a chip with *general* purpose capabilities. Both were programmable and thus to many it is a matter of degree as to which category was appropriate for these early chips. Again, the historical record reveals that these labels were not generally applied until years later, indicating that the issue—at least from the technologist's view—was not that important. The drivers for these products were not obvious. If anything this was another case of a new semiconductor technology searching for a market. The predominant motivation was the technical challenge of increasing the density and thus reducing the unit cost of IC technology. Consider the assertion by Goldstein & Aspray (1997) that general technological conditions were favorable for the development of the microprocessor in the mid-to-late 1960s. Continual increases in scale of integration had made it possible to place ever more elements of a computer circuit into a single chip, leading engineers to speculate about building a computer on a chip. Federico Faggin, who led the engineering work on the 4004 project at Intel, acknowledged this fact:

> By the mid-1960s people were building single-board microcomputers, using MSI [medium-scale integration] as a side function. It didn't take geniuses to figure out that this pattern of continuing integration and combining functions was going to happen. To people

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[39] Joerg Woerner, "The Story of the Datamath Calculator," http://www.dotpoint.com/xnumber/Datamath_history.htm
[40] Ibid.

> in the art and inside the industry, it was the natural thing to do. The question was, 'When will we have the technology that will allow it economically.'[41]

In dismissing Gilbert Hyatt's claim to the microprocessor invention previously discussed, Carver Mead from Cal Tech echoes Faggin's sentiment:

> It was a time of ferment. If you put yourself back into that time, you know that everybody was talking about putting a computer on a chip. We obviously would have done it if we had the technology. It was a no-brainer. It was a matter of when you could do it.[42]

Having been there, Poor's 'I don't think anyone invented the microprocessor' assertion sums up this view reflected by many in the other selected quotes at the beginning of this chapter. Today, of course, distinctions are much clearer as definitive markets for ICs have formed and evolved. But then it was anyone's guess as to where applications for these new devices would be. What seemed evident, though, is that there was consensus that continuation of circuit density increases would eventually lead to embodiment on a single chip. Important to this study is that a technological trajectory leading toward a single-chip solution—an implicit microprocessor *roadmap* if you will—was already established that helped guide the day-in, day-out *art* of engineering.

Lee Boysel left Fairchild to co-found Four-Phase Systems in 1969 (shortly after Noyce and Moore left to form Intel), and his design of the 8-bit AL1 chip is recognized by more than a few industry analysts as the first microprocessor. In his historical analysis of MOS IC technology, Bassett (1998) concurs with Faggin's and Mead's previous statements while offering other important background and context to argue that the invention of the microprocessor is more complicated than commonly understood:

> …Intel has a large stake in promoting that history [of microprocessor invention]. But things are more complicated than Intel lets on. As one looks at the organizations involved in MOS work in the late 1960s, one finds that the idea that it would be possible to put a computer on a chip was widespread at the time. Furthermore in the particular case of

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[41] Federico Faggin, as quoted in Andrew Goldstein & William Aspray (eds.), *Facets: New Perspectives On the History of Semiconductors*, New Brunswick, NJ: IEEE Center for the History of Electrical Engineering, 1997, 218.
[42] Carver Mead, as quoted in Joyce Gemperlein and Pete Carey, "If Hyatt Didn't Invent the Microprocessor, Who Did?" *The San Jose Mercury-News*, December 2, 1990.

> Fairchild, there were two distinct groups working on MOS. One group had a background in physics and chemistry and was skilled in the processes of making integrated circuits. The other was made up of electrical engineers who understood how to design things with MOS integrated circuits. The core of the first group left Fairchild to form Intel, while the second left to form a computer company, Four-Phase Systems. Four-Phase actually built a chip [AL1] that could have been called a microprocessor prior to Intel's work. It did not see what it had done as a microprocessor, a computer on a chip or even a discrete invention. To the engineers at Four-Phase their chip represented merely an evolutionary extension of previous ideas. Because they were in a computer company, they did not want to publicize their chip for fear others would copy it. Although the chip was technically similar to Intel's early microprocessors (and in many ways superior), its location in a computer company led to a vastly different trajectory for it.[43]

Rob Walker, co-founder of LSI Logic Ltd., another Fairchild spin-off, and formerly with Intel, has done historical research on the subject and states, "a guy that never gets any credit for his contributions is Lee Boysel … [who] in fact, developed the first microprocessor. It was never commercially sold but it was, essentially, an 8080 and it came before the 4004!"[44] During an interview with Gordon Moore (1995) when asked by Walker whether Boysel had developed the AL1 before the 4004, Moore replied:

> Ah, I didn't realize *that*. Lee had done some complex circuits at Fairchild… When he went off to set up Four Phase, he extended some of the stuff he was doing and, you know, I couldn't confirm that he did something before the 4004. The timing would have been pretty tough on that… How early was it?[45]

Walker responded, "His essentially 8080 was '69 and is still in use today by the IRS."[46] As Moore acknowledged, Boysel had conceived and designed the AL1 chip while still at Fairchild. Bassett (1998) provides evidence that in September 1967 Boysel wrote a single page proposal consisting mostly of a schematic diagram of a computer implemented entirely in MOS technology. Six different MOS chips, a ROM, a RAM, a "basic CPU element," and three different types of register chips, would make up the bulk of the computer. According to Bassett, Boysel described

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[43] Ross Bassett, "New Technology, New People, New Organizations: The Rise of the MOS Transistor, 1945-1975," *Business and Economic History*, Vol. 27, No. 1, Fall 1998, 6-7.
[44] Interview with Gordon E. Moore, Silicon Genesis: Oral Histories of Semiconductor Industry Pioneers, March 3, 1995.
[45] .Ibid., emphasis in original.
[46] Ibid.

the CPU element as a "4 bit wide slice with all op code decoding and branch instruction control built in."[47] The 'bit slice' design would later appear in the AL1 chip.

Tredennick (1996) also points out that "By 1967, the complexity of logic macro functions had risen to the point that Fairchild introduced the 3800, an 8-bit ALU chip with an on-board accumulator. By 1969, Four Phase had introduced a terminal product containing Lee Boysel's AL1."[48] In early 1970 Boysel had co-authored a paper that described design concepts of Four-Phase Systems' 8-bit AL1 microprocessor.[49] The AL1 was the heart of newly-developed Four-Phase computer system. The AL1 contained an 8-bit arithmetic unit and was an extremely complex chip as described below:

> Adding six lines of power, ground, and a 4Φ clock gives a total pin count of 42 and a complexity level of approximately 1500 to 1600 MOS gates for a 16-bit word. The resulting 40-to-1 gate-to-pin ratio is exceptional, but this complexity level would presently require a 200 x 200-mil LSI chip which is not practicable. For this reason and to make this device more universal, an 8-bit section was selected and designed to allow any number of these circuits to be connected to form a parallel 8-, 16-, or 32-bit word.[50]

When the article was published the Four-Phase system was already operating at an engineering-level and was publicly introduced that fall of 1970. By June of 1971, Four-Phase systems were in operation at Eastern Airlines, United Airlines, Bankers Trust, and McDonnell-Douglas. By March 1973, Four-Phase had shipped 347 systems with 3,929 terminals to 131 different customers.

For purposes of comparison the AL1 was roughly the size of Intel's 4004 while packing approximately the same number of transistors as Intel's 8008.[51] Both Intel chips would follow the AL1 by 1 and 2 years, respectively. It should be pointed out that there were *three* 8-bit AL1 chips in the Four-Phase System to support its 24-bit word architecture. At first blush, this appears a

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[47] Ross Knox Bassett, *New Technology, New People, New Organizations: The Rise of the MOS Transistor, 1945-1975*, Ph.D. Dissertation, Princeton University, January 1998, 247, Figure 2, 248.
[48] Tredennick, 1996, op. cit., 28.
[49] Lee L. Boysel and Joseph P. Murphy, "Four-Phase LSI Logic Offers New Approach to Computer Designers," *Computer Design*, April 1970, 141-146.
[50] Ibid., 144.
[51] Bassett, op. cit., 462-3 and footnote 17.

case similar to Holt's three "chip set" design discussed earlier. For this reason, some "single-chip" proponents dismiss Boysel's design as a true microprocessor embodiment. However, others see it differently. One big difference between the AL1 design and Holt's design was the consideration toward device *partitioning*. The 8-bit AL1 represented an entire parallel byte CPU 'slice' that could be arranged to accommodate a variety of computer architectures. The following caption describes Figure 7 of the Boysel/Murphy article:

> Fig. 6. The final 8-bit computer slice, complete with logic, registers and control, may be serially connected to form any word length. The circuit required 40 pins, which is the largest standard package available.[52]

One technical assessment of the AL1 is offered by Nick Tredennick, a recognized engineer and microprocessor designer. Tredennick holds nine patents, has written a textbook on microprocessor design (Microprocessor Logic Design), and was involved in the logic design and microcode development for Motorola's MC6800 and for IBM's Micro/370 microprocessors.[53] Reflecting on previous analysis as an expert witness in the Boone/Hyatt patent case previously discussed, his comparison between the AL1 and 4004 chips follows:

> I was an expert in a lawsuit some years ago when TI was beating companies over the head with its "Boone" patents. The Boone patents are the TI patents on the 8008… I have looked at the AL1 design from the papers written about it through the circuit diagrams and discussions with Lee Boysel and I believe it to be the first microprocessor in a commercial system… I have studied the papers, patents, and file histories for the early history of the microprocessor... Here are my opinions from that study. The first microprocessor in a commercial product was Four Phase Systems' AL1. The first commercially available (sold as a component) microprocessor was the 4004 from Intel. The reason that TI had such difficulty with its 8008 was that its designers adopted ideas from Lee Boysel's Computer Design article without understanding how four-phase logic works. Motorola bought and eventually destroyed Four Phase Systems, so there's no PR department to defend the AL1, leaving popular belief for the invention of the microprocessor up for grabs by a surviving company.[54]

In contrast with the three previous individuals discussed, Boysel himself did not seek a possible claim of priority to the microprocessor. It has been others who have made the assertion

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[52] Ibid.
[53] http://www.quickflex.com/news010523.html
[54] Nick Tredennick, online message posted 12 May 2002, Subject: The 8008 and the AL1, http://www.interesting-people.org/archives/interesting-people/ Note that Lee Boysel was also an expert witness in the same case.

that Boysel deserves at least some mention in the invention of the microprocessor. Bassett (1998b) characterizes Boysel's attitude about putting a computer on a chip as "nonchalant" from his statements in an article published in *Electronic Design* in February 1970 when Four-Phase already had a working computer system built around the AL1 chip. Boysel asserts in the article:

> The computer on a chip is no big deal. It's almost here now. We're down to nine chips and we're not even pushing the state of the art. I've no doubt that the whole computer will be on one chip within five years.[55]

Boysel's prediction proved remarkably accurate as the early microprocessor chip set designs of the era with separate ROM, RAM, clock, I/O and other support chips would eventually be reduced to a single chip by the mid 1970s by several manufacturers including Intel's 8085 as already stated, but more importantly Zilog's Z80, both in 1976.[56]

A final comment on the AL1 that will become even more evident in subsequent accounts has to do with *motivation*. Of course one major reason for keeping the AL1 low-key was that it was a key component of the computer system from which Four-Phase derived sales and profits. Protecting this intellectual property for competitive reasons was far more important than seeking a technical patent. A related factor concerned the type of business that Four-Phase along with other computer companies was in. This was also true of calculator, adding machine, even programmable terminal companies who were seeking similar technical and cost advantages from LSI technology. For the most part, companies that embedded microprocessors into their systems did not seek to manufacture or market the devices separately. Even the larger computer companies like RCA and Burroughs that manufactured their own chips did so only on a captive basis.

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[55] Ross Knox Bassett, *New Technology, New People, New Organizations: The Rise of the MOS Transistor, 1945-1975*, Ph.D. Dissertation, Princeton University, January 1998, 464-5; Boysel quoted in Elizabeth de Atley, "LSI Poses Dilemma for Systems Designers," *Electronic Design*, 1 February 1970, 44-52.

[56] Note that TI's TMS1000, first introduced in 1974, was a 4bit single chip embodiment as a *microcontroller*, while Rockwell's PPS4/1, one of the first complete microcomputers-on-a-chip, was introduced in 1976. Source: Rodnay Zaks, *Microprocessors: from chips to systems*, 3/e, SYBEX Inc., 1980, First Edition Published 1977, 170.

The relatively-young IC makers, on the other hand, made and sold chips. Competitive forces at the chip level played a much stronger role than at the end-device level. This factor will be explored in more detail later.

II. The Datapoint 2200 and the Intel 8008

CTC and the Datapoint 2200 programmable desktop terminal have already figured into this story. The Boone patent filed in 1971 that stands—at least legally—as the "first" microprocessor is based on a design in response to Computer Terminal Corporation's (CTC's) request for a programmable chip that would allow its new terminal product, the Datapoint 2200, to emulate terminals from a variety of different computer manufacturers. Important background about the Datapoint 2200 and the Intel 8008 microprocessor follows.[57]

Recall that the Busicom request that resulted in the 4004 was after all a calculator application. Although the embodiment included general-purpose features, the simple 4-bit design was quite limited in application. The real contribution of the 4004 was not the general-purpose microprocessor that is often touted, but rather the much larger field of microcontrollers, mostly commodity chips used in special applications such as industrial controllers (e.g., digital scales, taxi meters, gas pumps, traffic lights, elevator controls, vending machines, medical instruments, etc.) and a whole range of emerging 'smart' products where the microprocessor is a low-cost embedded device. Mazor summarizes the impact of these chips:

> The MCS-4 [4004 chip set] evolved into the single chip microcomputers 8048/8051. These chips emphasized small size and low cost. These, along with a variety of other manufacturer's parts have evolved into the under $1 computer on a chip used in toys, automobiles, and appliances. These chips are very pervasive - almost invisible.[58]

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[57] Much of this taken from separate telephone interviews with Vic Poor, June 5, 2003, and Stan Mazor, June 10, 2003 with the author along with corroborating e-mails and archival materials. Every attempt has been made to reconcile the historical accounts between Datapoint and Intel sources. In cases where these accounts differ greatly, this is simply acknowledged as "according to [source]" without offering additional interpretation.

[58] Mazor, 1995, op. cit.

On the other hand, the history of the 8008, typically described as the *second-generation* microprocessor (following the 4004), is not as well documented. Gordon Peterson, who was a software developer for Datapoint, the desktop terminal manufacturer that originally made the single-chip request (the organization was then known as CTC), comments on the lack of historical coverage:

> [I]nteresting, isn't it!? I think Intel (while not lying) would prefer to let the public think that the 8008 was a natural evolution from the 4004.[59]

In fact, the 8008 was a completely different project that was initiated only a few months after beginning the 4004. At the most basic level, since the 8008 addressed a terminal application, 8 bits were needed for alphanumeric ASCII character string handling, whereas 4 bits were all that were needed for the BCD arithmetic (10 numeric digits 0-9) used in a calculator operation.[60] It is widely known that the 4004 project suffered from a lack of dedicated resources; likewise the 8008 (then called the 1201 within Intel) project was often interrupted by other, pressing priority projects, especially in memory products, the young firm's specialty. At one point it appeared that the 8008 would be finished before the 4004 but Hal Feeney, an engineer recently hired from General Instruments to work on the 8008 design, was reassigned to work on the company's new DRAM product line. Federico Faggin was assigned to manage both logic projects, but was almost completely devoted to the 4004. While Mazor and Hoff worked briefly on the 8008 project, Feeney returned as the chip's primary developer. Thus, some information exchange did occur between the projects, but the project assignments as brief as they were meant that essentially the projects were quite different in type and approach. So each chip project is best described as having occurred independently while almost concurrently.

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[59] Gordon Peterson, e-mail with the author, June 3, 2003.

[60] Noyce and Hoff, op. cit., 1981, 10, 13. ASCII is an acronym for American Standard Code for Information Interchange, a 7-bit character code (2^7 = 128 code points) commonly used throughout the telecommunications and computer industries. When an eighth bit is used as a 'parity bit' to verify whether or not data has been transmitted properly then ASCII becomes an 8-bit, or one-byte (8 bits = 1 byte), character code. This is the typical usage in ASCII data transmission. A true 8-bit character code allows for up to 256 items to be encoded (2^8 = 256 code points). Numeric digits 0-9 require only 4-bit BCD or hexadecimal (base 16) coding.

Like the 4004, the 8008 also came as a special chip request from an outside firm. While much is written about the Busicom calculator chip request, often featuring the design genius of Intel's Marcian "Ted" Hoff or the assertive role of Busicom's Masatoshi Shima, the personalities involved in the CTC chip request were much more low-key. Usually CTC is mentioned as a small footnote in the 8008 story. One important factor in both chip requests is that the architecture and basic design were already completed by the users when presented to Intel. Different than Busicom's dozen-chip request,[61] CTC specified a *single-chip* design, according to Victor Poor, former vice president of R&D for Datapoint and the one who made the original chip request of Intel. Both Busicom and CTC were not in the chip business and were seeking a component manufacturer to "reduce the design to silicon." Unlike the 4004 though, the significance of the 8008 would be far-reaching as this product housed the *CTC-developed* basic instruction set that would become the basis of the 8080, 8086, and subsequent microprocessors that transformed Intel and helped spawn the PC revolution. All x86-based Intel (and other code-compatible) microprocessors trace their ancestry to the 8008, thus to CTC/Datapoint. Interestingly, like the 4004 *Intel did not file a patent claim for the 8008 either*.[62] But another organization did (i.e., TI as a kind of second-source for the 8008)[63] as has been previously discussed.

The origin of the 8008 idea is recounted by Poor and Jonathan Schmidt who worked directly for Poor. Both played important roles at CTC, based in San Antonio, Texas, particularly with regard to this project. According to them, the single-chip idea started while they worked at Frederick Electronics in Maryland, a company Poor earlier helped co-found. During the Thanksgiving weekend in 1969 Poor, Jonathan Schmidt, Stan Kline, and Harry Pyle, then a student at Case Western University, participated in the effort and would all shortly become CTC

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[61] Accounts vary from 10 to 13 as to the exact number of custom chips requested by Busicom. In any case, Busicom's multichip specification was very complex.
[62] Mazor points out that the 8008 ISA (instruction set architecture) was 95% Datapoint's, and it was also a custom chip like the 4004, Stan Mazor interview, op. cit.; see also Mazor, 1995, op. cit.
[63] Gordon Peterson e-mail, op. cit., "Normally a 'second source' for a complex chip set uses the same internal architectures and often even the same masks. The primary goal is an 'alternate foundry' should the original producer go bust. TI developed their 8008-compatible microprocessor, as I understand things, separately from and in competition with Intel."

employees to head up a project to put a programmable controller into the existing Datapoint 3300 terminal.[64]

Like Intel, CTC was formed in 1968. Its main business was ‘glass’ teletypes which were video terminal versions of the Model 33 Teletype (TTY) then in common use. The CTC Model 3300 emulated the popular Model 33 TTY protocol, used semiconductor vs. acoustic delay line shift register memory, and employed cassette vs. paper tape as its I/O device. The 3300 was well received by the market; no sooner was it introduced, all kinds of inquiries came in from customers about unique (non-TTY) terminals: could a terminal be made to simulate this or that manufacturer's terminal? Many terminals had special control functions and protocol-handling was done through sophisticated hard-wired designs.[65] None of the individual requests represented enough market demand to warrant a new product, but collectively there was a definite need for a different type of product; one that could accommodate several terminal protocols through software vs. hardware. So the group of four was hired by CTC in December 1969 specifically to develop a new product that could emulate other manufacturers’ terminals. They brought with them significant experience with a similar serial controller using recirculating memory built for several years at Frederick Electronics. The new CTC product was called the Datapoint 2200 and is shown in Figure 7.3.

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[64] Poor had 'met' Pyle years earlier during an amateur radio session involving HF receivers when Pyle was still in high school in Delaware. Poor asked Pyle to work for Frederick during summers and school breaks, a practice that Pyle continued at college.

[65] As one example, DEC was a large manufacturer of its own video terminals. In the early 1970s the VT52 offered standard ASCII keyboard functions, but also included special control functions that only DEC machines could recognize. This had become common practice among other computer manufacturers that also made proprietary video terminal devices. By the 1980s video terminals (and other computer peripheral products) would gravitate toward more open designs, enabling standards for interface protocols, keyboard layout, and overall physical design that are evidenced in most of the PC monitors and keyboards in use today.

Figure 7-3. Datapoint 2200 Programmable Terminal (1970)

The Datapoint 2200's appearance closely resembled the 3300 but with a 12-line, 80-character width green phosphorous screen, cassette I/O devices integrated into the top right of the unit, and a more conventional typewriter-like keyboard. The 2200 also contained an 8-bit serial CPU implemented on a single circuit board consisting of roughly 100 MSI TTL chips.

CTC had hired Poor (he had also helped raise capital to start CTC in 1968) as its V.P. of R&D with the 2200 as his priority project. While at Frederick, Poor had wrestled with the programmable terminal idea (as a consultant as he was not yet on the CTC payroll) and helped decide on the *single* terminal design to emulate multiple vendors. Additionally, Poor envisioned that the CPU MSI implementation could be implemented in LSI to cut costs and hence increase the 2200's marketability. As previously mentioned, with increased circuit densities on chips it had become feasible to achieve this with LSI technology coupled with microcode (software) for emulation. Poor states that the objective was not to build a replacement for the PDP-8 or other

computer; CTC was not thinking about general purpose computing: they were a *terminal* company.[66]

During that Thanksgiving 1969 holiday Poor presented the LSI idea to Pyle who had returned to Frederick to work over the holiday break. Pyle was a gifted, self-taught computer designer familiar with the architecture of the PDP-8 and similar systems. Responding to Poor, Pyle sketched out a schematic and functional specification for a processor that could be implemented in LSI as a *single chip*. These were not detailed semiconductor designs as CTC wasn't interested in making chips, but they did emphasize efficient chip design techniques especially keeping gate counts down (i.e., the design tried to keep data flows to a reasonable number of gates). These sketches were later made public in a *Datamation* article that featured Poor as “co-designer of the Datapoint 2200 [LSI CPU] … of what later became [the] 8008 microprocessor."[67] Poor and Pyle also developed the basic instruction set of about 50 instructions for the chip with Schmidt working along side.

Immediately upon joining CTC Poor visited Intel in December 1969 to meet with several people including Bob Noyce, Gordon Moore, Andy Grove, Ted Hoff, and Stan Mazor. Poor was following up with Intel on chip orders while requesting additional MSI parts to help implement the immediate design (in TTL) of the 2200. At the time CTC was Intel's biggest customer of MOS shift registers. Used as recirculating serial memories, Model 3300s required a lot of MOS shift registers to refresh CRT screens. Intel also produced a custom 512-bit shift register memory chip for use in the Datapoint 2200. Shift registers were one of the first standard MOS IC parts. Because they were serial devices, chipmakers could increase the number of transistors (or the number of bits) inside a chip without increasing pin count (i.e., number of external leads) on a chip package. Referred to as the 'gate-to-pin ratio', this factor frequently turned out to be the

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[66] Poor interview, op. cit.
[67] W. David Gardner, "Microprocessors Are "Old Stuff" to Him," *Datamation*, January 1976, 1 of 2pg reprint.

limiting factor in chip design.[68] Mazor notes that shift registers were successful as early LSI devices because the gate-to-pin ratio was very good for a small package: "there were few I/O's handling lots of bits."[69] Also note that *there was no Random Access Memory (RAM) commercially available at the time*.

At the same time, Intel was also CTC's biggest chip supplier. Both companies had started about the same time, were about the same size, and were very important to each other. According to Poor, a good relationship existed among the leadership of both companies.[70]

During a meeting with Intel leadership and following the discussion on shift registers, Poor mentioned to the Intel team the 'single-chip' idea that he and Pyle had conceived. According to Poor, their response was discouraging, stating the idea was not economically feasible since there was inadequate volume. They reminded Poor that Intel was in the *memory* business because that was the sector where sufficient volumes existed. Stan Mazor, former Intel development engineer, does not recall a 'single-chip' request from Poor, but it is possible that he was not in attendance when the initial request was made. Mazor states that Poor had asked Andy Grove, then production manager, for a 16x8 'push-down stack' by adding a counter to a small 16x4 bipolar RAM Intel had begun manufacturing. Grove couldn't answer him so he asked Mazor to address the issue with Poor directly. Mazor had left Fairchild in September 1969 to join Intel and was assigned immediately to work on the 4004 architecture for Ted Hoff. So he had been working heavily on the 4004 for three months. With this knowledge Mazor suggested three alternatives as follows:

1. a chip to hold 8 registers (and a stack),
2. a chip to hold 8 registers, stack, and an 8-bit ALU,
3. a CPU chip to integrate the entire CPU on the condition that the ISA wasn't too exotic.[71]

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[68] Bassett, op. cit., 298.
[69] Mazor interview, op. cit.
[70] Poor interview, op. cit.
[71] Stan Mazor, e-mail to Gordon Peterson, Subject: old 8008 (1201) history stuff 12/02, December 6, 2002.

According to Mazor the single-chip CPU idea took Poor by surprise. Mazor's account is contrary to Poor's earlier interpretation that CTC/Datapoint brought the idea to Intel. Hoff (1995) comments that this difference of opinion on whether it was Datapoint or Intel that originated the single-chip CPU design idea is an old debate:

> Victor Poor has said that he brought the idea for the microprocessor to Intel and that it was his intention all along to do it as a single chip. But considering that the 4004 had already been defined, and we considered the 4004 to be the first microprocessor ... my firm belief is that the original [Datapoint] request was for registers and it was our counterproposal to do … what was ultimately known as the 8008.[72]

Reconciling this long-standing debate is well beyond the scope of this research. One possible explanation is that the Datapoint 2200 was originally a bit-serial design based on recirculating shift register memory, and the claimed single-chip design from CTC was bit-serial. The Intel 8008 design (like the 4004) was a parallel architecture using newer dynamic *random access* memory (DRAM), soon to become Intel's most important product. Intel may have felt the older, bit-serial design infeasible with newer memory architectures, an area CTC was not as familiar with. Nonetheless, the important point is that a shared exchange between a few key individuals of two young companies brought forth the 8008 concept that would ultimately have far-reaching effects.

While the single-chip CPU project was being considered, CTC had proceeded with development of the 2200 using an immediate MSI design (CPU on a single board), including the instruction set, op-codes, and all supporting functions. According to Poor in early 1970 Phil Ray, the CEO of CTC, met with Bob Noyce, CEO of Intel, and expressed concern that the CTC single-chip request was not taken seriously by Intel. CTC considered the single-chip design very important to reducing the production cost of the 2200. So Ray used customer leverage with Noyce, reminding him that CTC's memory business could be taken elsewhere if Intel did not reconsider the single-chip request. As a result, Intel agreed to develop the chip for $100K (a figure arrived at mutually between Ray and Noyce). According to Mazor, the 8008 agreement involved 100,000 *units* and was more of a conventional contract between the firms. At an

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[72] Ted Hoff as quoted in Rob Walker, op. cit.

estimated order rate of between 5,000 and 8,000 terminals per year Mazor states that Datapoint could never have satisfied the 100,000 unit contract terms anyway.

Once an agreement was struck, CTC provided all 2200 technical and programming specs to Intel. Mazor was assigned as Intel liaison on the project. His manager, Ted Hoff, also worked on the project along with another recently-hired engineer, Hal Feeney, previously mentioned. According to Mazor, Poor sent the *Datapoint 2200 Programmer's Manual* which defined the symbolic and machine code ISA in January 1970.[73] From this Mazor states that he wrote, with inputs from Hoff, a handwritten proposal for the 1201 chip (Intel code name for the chip); the 1201 would later be renamed the 8008 by Intel's marketing department (8008 = twice 4004). Mazor and Pyle communicated regularly on the 8008 project according to both individuals. Furthermore, after completion of the 8008 both continued to collaborate on product improvements resulting in follow-on projects (i.e., Intel's 8080 and Datapoint 2200 v2). Mazor contributed significantly to the 8080 instruction set and is part-holder of the 8080 patent.[74]

Sometime after Intel initiated work on the 8008 TI approached CTC and requested to do chip design at no cost (they were also interested in CTC's memory business). It is generally believed that TI obtained Intel's proprietary 1201/8008 design information to speed up the development. Mazor, Tredennick, and McClure have closely examined the TI 'Boone' patent and noted both the unique Datapoint and Intel design features (including ones that did not work in the initial Intel design). Many speculate that the Intel information was leaked to TI through Datapoint, however Poor insists that this was not done. Nonetheless, TI delivered a 212 x 224-mil eight-bit chip to CTC in March 1971 well before Intel.[75] However, the chip was barely operational and was certainly not commercially viable, so CTC did not accept the design. Soon after, TI ran an

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[73] According to Gordon Peterson, the *Datapoint 2200 Programmer's Manual* incorporates a "Reference Manual" completely describing the CPU hardware, instruction set, and built-in I/O facilities of the 2200. See e-mail/newsgroup posting to Dave Farber's IP list dated May 11, 2002 to John Wharton wharton@shasta.Stanford.edu

[74] Federico Faggin, Masatoshi Shima, and Stanley Mazor, "MOS Computer Employing a Plurality of Separate Chips," U.S. Patent 4,101,449, Assignee: Intel Corporation, Santa Clara, CA, Filed December 31, 1974, Issued March 1, 1977.

[75] Noyce and Hoff, op. cit., 13.

advertisement of a single-chip design for a customer (CTC) and proceeded to apply for a patent (see earlier discussion on Gary Boone patent). After "puttering around for two years" according to Poor, Intel finally delivered the 8008 chip in late 1971. The chip worked but significantly lacked in performance compared with MSI implementation. One analyst estimates the Intel chip "executed instructions approximately ten times as slowly as Datapoint had specified."[76] The Datapoint 2200 systems (using MSI design) had already been shipping for about a year so CTC decided against using the 8008.

Ted Hoff, who headed applications research at Intel and was instrumental in developing both the 4004 and 8008, comments on the limitations posed on early microprocessors by other devices—in this case memory—when used in applications beyond special-purpose microcontrollers:

> At that time, we weren't really looking to replace the general purpose computer. For one thing, the microprocessors of that first generation were very slow devices and if you were to go to an application that required a large amount of memory, you were going to have to have a big investment in memory, because memory was quite expensive then. So it wouldn't necessarily make sense to use a microprocessor in that environment because you weren't using your memory effectively, you might do better to spend a few dollars more and use a processor that was built out of TTL such as you'd find in a minicomputer of the day. So, for that reason, we tended to limit our imagined use of these devices to applications that could be done with very modest amounts of memory.[77]

Jonathan Schmidt worked directly for Poor at CTC while Pyle reported to Schmidt. All were actively involved in the 2200. As already stated, Schmidt was at Frederick Electronics Thanksgiving '69 with Poor and Pyle when the programmable processor design was developed. Schmidt oversaw development efforts on many of the follow-on Datapoint programmable data terminals. He recounts how quickly development proceeded on the 2200:

> I wrote a simulator for it on an HP 2116, including the I/O bus. Peripherals and early programs were tested on that. It only took until April of '70 to have working units at the American Banker's show in San Francisco, CA, in a case design that looked identical to that of the units shipped through to 1980 or so. I wrote the demo programs for that show,

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[76] Adam Osborne, *An Introduction to Microcomputers: Volume 1, Basic Concepts*, Adam Osborne and Associates, Inc., 1976, 1-4.
[77] Ted Hoff in Rob Walker, op. cit.

> too… However, by [the time Intel delivered the 8008], Datapoint had shipped hundreds, perhaps 1000s, of 8008-based machines implemented in MSI.[78]

When CTC tested the 8008 it was far superior to the TI chip (the TI chip was not actually functional). One factor was that Intel had used newer silicon gate technology (developed at Fairchild by Faggin) on the 8008 whereas TI used conventional metal gate technology. Intel's chip was 60% smaller than TI's, while performing much more reliably.

According to Poor, following delivery of the 8008 Noyce contacted Ray and requested the $100K development cost from CTC. Ray's reply was that the 8008 chip was "a year late and a dollar short" so CTC did not pay Intel anything for development. In exchange CTC agreed to allow Intel full rights to the chip, including the instruction set and all other functions supplied by CTC. Noyce agreed with the proposal and in April 1972 Intel officially announced the 8008 (MCS-8) as a standard product without mention of CTC's involvement.

Although CTC rejected the 8008, CTC was pleased that the 2200 I/Os and instruction set were both fully intact in the Intel 8008: "that's all we cared about" says Poor. Thus, the Datapoint 2200 CPU architecture and instruction set formed the basis of the 8008, as verified by CTC. Different than the simpler Busicom calculator application for the 4004, the 2200 CPU was much more demanding and its MSI design, based on bipolar technology, easily outperformed MOS technology employed in the 8008. Both bipolar and MOS technologies were relatively new, so either choice meant some degree of risk. Previous coverage of why CTC chose to stay with bipolar (TTL) technology usually deals with economics: bipolar devices were cheaper than MOS and recessionary pressures in 1970 brought prices down even further. While cost was an important factor, the fact that bipolar was superior to MOS in terms of speed and performance also weighed heavily in the decision. Moore (1976) summarizes the technical trade-offs between the two technologies at the time:

> Bipolar transistors employed in modern integrated circuits are relatively high-speed devices. Even minimum-sized transistors have the ability to switch relatively large

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[78] Ibid.

> currents rapidly, resulting in the possibility of high-speed circuits… Thus high-speed systems can be made by interconnecting many separately packaged circuit functions, each of modest complexity. This accounts for the broad use and popularity of circuit families such as TTL that depend upon the integrated bipolar transistor.
>
> On the other hand, the MOS transistor of the same vintage is a relatively slow device with generally limited drive capability… Performance of MOS was adequate for calculators… the pressure on the evolution of MOS technology supplied by the calculator was toward high density and low cost. It exerted little pressure toward higher speed.
>
> Bipolar, on the other hand, had evolved toward increasingly high-performance logic families…The level of complexity required to realize a complete processing unit existed only in MOS; so the first microprocessors were MOS.[79]

Moore's last statement helps explain the situation facing CTC at this juncture. The major advantage of MOS technology to single-chip applications was increased density: MOS designs feature symmetrical electrical characteristics that, among other things, minimize required device sizes increasing the amount of functions per unit area. The trade-off was slower performance. So although MOS made feasible single-chip capability, the initial applications were limited to relatively simple operations such as the 4-bit functions of the Busicom calculator. In contrast, the 8-bit 2200 CPU was *not* one of these simple applications. CTC continued to use MSI CPU designs in subsequent systems including the 2200 v2, 5500, 8800, and other systems that spanned into the early 1980s. What they discovered was—like the initial 8008—Datapoint MSI designs were always one generation ahead of single-chip CPU designs in terms of processing power. Thus, although they continued to evaluate microprocessors for possible use, CTC *never substituted an Intel microprocessor for their MSI CPU design*. Schmidt describes this cycle:

> Datapoint made prototypes of 8080-based compatible machines using an 8080 and a small amount of external logic to reconcile the difference but it wasn't used because, by that time, Datapoint needed the power of a 286, and the cycle of one-behind-the-chip-curve went on for 13 years before they finally merged.[80]

The 2200 became so successful that the company officially changed its name from CTC to Datapoint. Following the 8008, Datapoint continued to use Intel as a chip supplier but also bought semiconductors from Mostek and TI. Like Intel, all Datapoint systems had to be backward-

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[79] Gordon E. Moore, "Microprocessors and Integrated Electronic Technology," *Proceedings of the IEEE*, Vol. 64, No. 6, June 1976, 849.
[80] Schmidt e-mail, op. cit.

compatible so 8008 follow-on chips and 2200 follow-on systems remained fairly software-compatible. As previously mentioned Mazor and Pyle continued their collaboration, sharing ideas on the immediate follow-on products, the Intel 8080 and Datapoint 2200 v2. The 2200 v2, introduced about a year after the bit-serial 2200, incorporated an 8-bit *parallel* processor (but not the 8008) while replacing serial shift register memory with Intel's new RAM chips and doubling the main memory capacity. Along with other hardware performance improvements and more applications, the 2200 v2 was a legitimate general-purpose small data system that would help redirect the company's strategic focus. Schmidt compares the two closely-related products:

> The 8008 was EXACTLY the Datapoint 2200 instruction set. The 8080 was almost but not exactly the same as the Datapoint 2200 Version 2 instruction set.[81]

With time though the Datapoint instruction set diverged slightly as follow-on machines became more sophisticated. A similar process occurred with subsequent Intel microprocessor generations. However, review of internet newsgroup postings reveals software compatibility between later Datapoint and Intel-based systems as described by the examples below:

> A friend worked for a while setting up business systems on Datapoint 2200s and their follow-ons. As for programming, I got hold of the source code for their cute little "man and dog" screen hack. This almost-8008 assembly code was close enough to 8080 that I was able to translate it to run on my IMSAI.[82]

> At Datapoint we took assembly source code for the Datapoint 2200 (instruction-set compatible with the 8008) and assembled it for Z80s all the time. When Datapoint made the 1500 using a Z80 instead of a proprietary processor, that's how the OS and utilities were ported.[83]

The reference to the Zilog Z80-based 1500 contains an interesting twist of irony. Recall that in 1976 Zilog, co-founded by Federico Faggin as a spin-off from Intel to develop microprocessors, introduced the Z80, a code-compatible but more powerful *single-chip* version of the Intel 8080 three chip set. That same year Datapoint decided to incorporate the Z80 into its follow-on model

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[81] Jonathan Schmidt, e-mail to the author, June 3, 2003, emphasis in original.
[82] Joe Pfeiffer, message posted February 28, 2002 16:54:53 -0700 to Newsgroup *alt.folklore.computers*, Subj: Re: Intel 4004. Note that the IMSAI was an early 8080-based microcomputer.
[83] Robert Teisberg, message posted May 28, 1992 06:42:24 PST to Newsgroup *comp.arch*, Subj: Re: TI '486 clone? Note that the Zilog Z80 was code-compatible with the Intel 8080; Federico Faggin led the development of both chips.

1500, making them one of Zilog's first customers. The 1500 reached mass production in less than a year, a record at the time, and priced at $6,000, ultimately sold well.[84] So although Datapoint never employed an Intel microprocessor, it did indeed see its ISA implemented in a microprocessor (i.e., Z80) whose antecedent was the 8008.

Datapoint grew rapidly in the 1970s and early 1980s. The company was successfully transformed from first a 'dumb' then 'smart' terminal company into one that could be better described as a small business computer system firm in large part because of the success of the 2200 design. Intel similarly grew and underwent a transformation from a memory company to a logic/microprocessor firm as follow-on products to the 8008 were introduced. The most notable of these, of course, was the 8086/88 that was accepted by IBM and used in their PC introduced in 1981. That year alone IBM accounted for 13% of Intel's total sales. Gordon Moore later recalled the IBM PC design win as very important, but could not see its strategic value:

> Any design win at IBM was a big deal, but I certainly didn't recognize that this was more important than the others. And I don't think anyone else did either.[85]

The economic fate of both firms would be challenged in the early 1980s. Starting in late 1984, Datapoint became a target of a successful hostile takeover bid that broke up the company, sold off parts of the firm while simply dropping other parts such as R&D. Poor had recently retired, but all the other key players involved in the 2200 and follow-on systems were let go in the acquisition. The impact was devastating: of the 9,000 total Datapoint employees (6,000 in San Antonio) before the takeover; only 200 remained in San Antonio 24 months later.

Interestingly, Intel also faced a similar fate as Moore describes:

> We were also concerned about the potential for a hostile takeover, and we figured that if IBM owned 20 percent of us, we wouldn't be a likely candidate. So it worked out well for us.[86]

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[84] Datapoint 1500 sales estimate according to Jonathan Schmidt: "many thousands were sold if not 5 figures." Jonathan Schmidt, e-mail to the author, July 30, 2003. "Thousands" estimate also by John Cole in e-mail to Gordon Peterson, August 1, 2003.

[85] Author unknown, "Intel Corporation: The Evolution of an Adaptive Organization," http://www.aom.pace.edu/meetings/1999/INTEL1.htm

What Moore is referring to in this statement is that in 1982 IBM had announced plans to purchase 12% of Intel for stock for $250 million, and by 1984 this amount had increased to 20% and $400 million. Recall from Box 3-2 the increased international competition in the DRAM market from primarily Japanese producers. The DRAM, developed by Intel in 1970, had been all but arrested from U.S. producers by the late 1970s; Intel had become a minor player while others began to abandon the market altogether. IBM, now a strategic partner of Intel's for its successful PC, saw its ownership stake in Intel as good insurance.

Decades later, Mazor laments about Datapoint's contributions to the 8008, thus to Intel's and the industry's success, stating "the original instruction set was theirs, and the original motivation was theirs."[87] He also describes the 8008 instruction set as "admirable," noting specifically that there was good symmetry in the microcode, much more than in the 4004.[88] Many of the original Datapoint 2200/8008 design features such as the 8-register architecture continue to this day in x86-based microprocessors through the popular Pentium IV. He also finds irony in Datapoint's fortune as the 8008 successor chips, the 8080 and especially the 8086/8 sold to IBM and PC-compatible makers, went head-to-head with Datapoint:

> It is ironic that Datapoint ultimately competed in the marketplace with PC products based upon *their own*, Datapoint defined, architecture![89]

Likewise, Schmidt has reconciled Datapoint's accomplishments with the passage of time. Even if the public record may not completely reflect Datapoint's contributions to the 8008, he acknowledges personal satisfaction as reward enough:

> None of us have any agenda to set anything straight. 'Stuff' happens. We were blessed with having had the best damned time you could imagine. We did the above.[90]

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[86] Anthony B. Perkins, "The Accidental Entrepreneur: An interview with Dr. Gordon E. Moore, Chairman and Co-founder, Intel Corp.," Red Herring, September 1995, http://www.redherring.com/mag/issue23/accidental.html
[87] Michael Kanellos, "Intel's Accidental Revolution," *CNET News.com*, November 14, 2001, http://www.dotpoint.com/xnumber/accidental_revolution.htm
[88] Mazor interview, op. cit.
[89] Mazor, 1995, op. cit., emphasis in original.
[90] Schmidt e-mail to author, op. cit.

III. Calculators Bring Forth the Microprocessor[91]

The next section discusses the important role of calculators as the LSI application most associated with the development of the microprocessor. As previously discussed, the crucial role of the user in innovation is stressed by von Hippel (1977).[92] Consistent with this, Chuck Peddle, a recognized innovator of early microprocessors, emphasizes that "This industry was built by customers."[93] In the Intel case, both the Busicom and especially the Datapoint examples best illustrate this. The emphasis here is on one key user—the electronic calculator industry—in serving as an early catalyst for volume production of LSI ICs, culminating in the microprocessor. Briefly, what is described is that both IC and electronic calculator technologies emerged and co-evolved in the 1960s, each affecting the other in important ways. The most striking evidence of this is the progressive reductions in size, weight, and price demonstrated by both industries. Within a decade of the first fully-electronic calculator (based on vacuum tubes) a product featuring a complete "calculator-on-a-chip" was available; in fact, many single-chip calculators had been (or would soon be) introduced. U.S. chipmakers in particular would dominate as suppliers of calculator ICs from the mid 1960s through the early 1970s. Writing shortly after this era, Zaks (1977, 1980) provides a simple flowchart showing the evolution of LSI applications to the microprocessor with *calculator* as an immediate, preceding step:

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[91] This section draws heavily upon several excellent websites that catalog the history of the electronic calculator. The author is grateful to those who freely share pictures, physical descriptions, technical specifications, prices, and in some cases sales data on these products. Every attempt has been made to acknowledge sources of information on calculator artifacts.

[92] Eric von Hippel, "The Dominant Role of the User in Semiconductor and Electronic Subassembly Process Innovation," *IEEE Transactions on Engineering Management*, Vol. EM-24, No. 2, May 1977, 60-71.

[93] Microprocessor Report, op. cit., Peddle worked at Motorola on the 6800, and led the team that went to MOS Technology to create the 6502, the microprocessor used in the popular Apple II Computer.

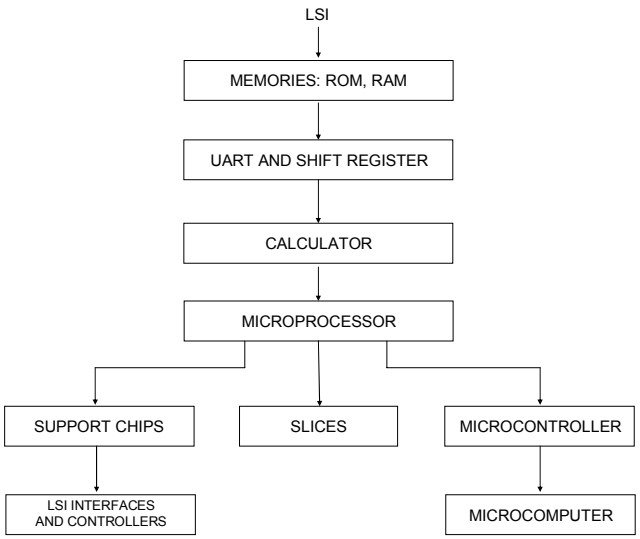

Figure 7-4 The Evolution of LSI

Source: Rodnay Zaks, *Microprocessors: from chips to systems*, 3/e, SYBEX Inc., 1980, First Edition Published 1977, Fig. 1-19: The evolution of LSI, 30.

In Braun & Macdonald's treatise on the history of semiconductor electronics (1978, 1982), a similar lineage culminating in a single chip calculator is described:

> The two most crucial factors in determining the path electronics was to take in the seventies were the invention of semiconductor memories and the success of the single chip calculator… As far as the history of the microprocessor is concerned, the important feature of the calculator is that it contains most of the features of a computer – input, output, memory, arrays of logic gates for the performance of arithmetic operations – but all possible operations are permanently wired… The fundamental difference between a 'dedicated' calculator chip and a programmable microprocessor chip is the facility for software wiring."[94]

[94] Ernest Braun & Stuart Macdonald, *Revolution in Miniature: The history and impact of semiconductor electronics re-explored in an updated and revised second edition*, Cambridge: Cambridge University Press, 1982 (first published 1978), 105-7, emphasis in original.

The authors note programmability (i.e., "software wiring") as the key difference between calculator and microprocessor technologies. However, they also state that even this difference fades when considering progressively more powerful calculators:

> The calculator is a computer. The most basic and the cheapest calculators do little more than add, subtract, multiply and divide, and there is a hierarchy above the basic model capable of more elaborate functions. Somewhat more expensive is the scientific calculator and more expensive still the desktop calculator… At the top of the hierarchy, and almost indistinguishable from what is normally regarded as a computer, is the programmable calculator.[95]

As discussed in Chapter 6, the emergence of the IC in the early 1960s was a significant technical breakthrough, so much so that a transition in the semiconductor technological trajectory resulted (see Chapter 4). Industrial fortunes were rearranged as new names like Fairchild, Texas Industries, and Motorola came to replace the firms that had commercially exploited the transistor that Bell Labs had brought forth a decade earlier. True to the Rycroft/Kash *normal* innovation pattern, steady and rapid increases in IC circuit density (i.e., Moore's Law) helped create chips with more and more advanced capabilities. Throughout the 1960s *scale* of integration on a single chip moved relentlessly from small-scale integration (SSI) to medium-scale integration (MSI) to large-scale integration (LSI) as shown in Table 7-2.

Table 7-2. Scale of IC Integration

Scale	**# Logic Gates**[96]	**Application (in calculator)**	**Timeframe**
SSI	up to 12 gates	simple circuits like flip-flops	early to mid 1960s
MSI	up to 100 gates	building blocks like counters, adders	mid to late 1960s
LSI	up to 1000 gates	subsystem such as calculator adder-subtractor	late 1960s
VLSI	more than 1000 gates	complete system such as calculator-on-a-chip	early 1970s

[95] Ibid., 187-8.
[96] A logic gate in semiconductor electronics is an array of switches or transistors.

In many cases the technology outpaced the perceived need for the increasingly powerful devices. IC makers faced a new economic reality with greater associated risks concerning product development—exactly what to make. Recall Moore's description of this dilemma when Intel was formed in 1968: "the problem was nobody knew what to make." Moore expands on this 'product definition crisis' in the following passage, noting the strategic importance of the calculator and semiconductor memory:

> In general, the semiconductor industry's efforts to solve its problems in the 1965-1968 era were not successful. The product definition crisis persisted and limited IC complexity through the mid-60s. Two things broke the crisis for [the] semiconductor component manufacturer, though not necessarily for the mainframe computer manufacturer: the development of the calculator and the advent of semiconductor memory devices.[97]

It is important to note that Intel was founded upon a strategy to manufacture LSI ICs for high volume, thus the initial development of semiconductor memories to replace acoustic delay lines and magnetic cores was seen as a chief opportunity. But at the time there were few other industrial uses for ICs outside of DoD and NASA, even though federal government requirements were dwindling considerably by the late 1960s. Given this situation IC makers had increasingly turned to the consumer market. Just as the hearing aid or 'transistor radio' is most associated with early commercial application of discreet transistors, the electronic calculator held a similar role for ICs.

Recall that it was a special chip request from Busicom that resulted in the Intel 4004 (Figure 7-5a). The 4004 chip, along with ten additional LSI support chips (e.g., ROM, RAM, I/O) from Intel, was successfully implemented in Busicom's desktop printing calculator, model 141-PF (Figure 7-3b) in 1971.[98]

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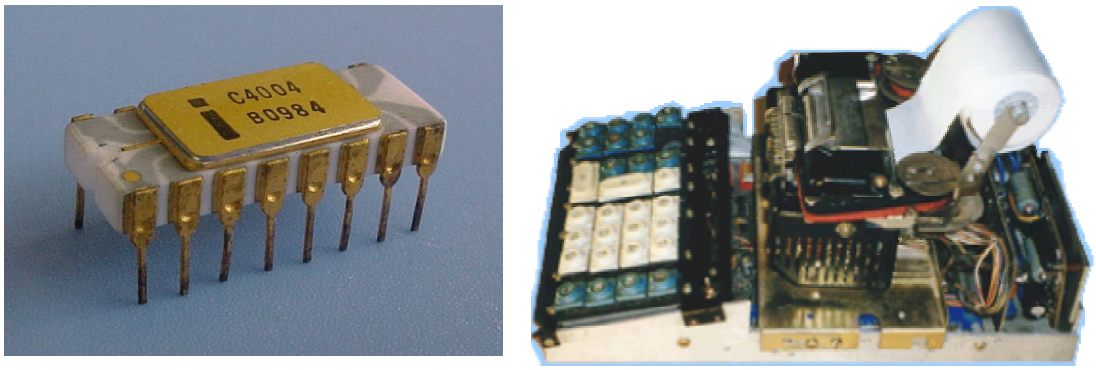
[97] G.E. Moore, "VLSI: Some Fundamental Challenges," *IEEE Spectrum*, Vol. 16, No. 4, April 1979, 33.
[98] The Busicom 141-PF sold for 159,800 yen (about U.S. $695).



(a) **(b)**

Figure 7-5. Intel 4004 and Busicom 141-PF Desktop Printing Calculator (1971)

Photos courtesy http://www.intel4004.com and http://www.antiquetech.com/chips/4004.htm

Also, the TI 'Boone' patent discussed earlier may have been for the Datapoint 2200 programmable terminal microprocessor (as a potential second source to Intel), but the resultant chip never worked satisfactorily, thus was not produced. Interestingly, when Datapoint did not accept Intel's version of the chip, Intel branded it the 8008 and their first customer was Seiko for a calculator application.

By 1972 TI was very active in developing both a calculator product line *and the semiconductor chips that drove them*. As previously discussed, Jack Kilby himself was asked to lead an early effort to develop the first hand-held calculator for which he succeeded.[99] Within a few years TI was acknowledged as a leader in microcontrollers, including the TMS1802, claimed to be the first commercially available 'calculator-on-a-chip' announced September 17, 1971, of which Boone was also involved.

Regarding the oft-cited Busicom-Intel project, what is usually not reported is that Busicom's parent company, Nippon Calculating Machine Company, had also requested a *single-chip calculator solution* for a portable unit from a different young start-up firm called Mostek. In May 1970, almost a year after Busicom approached Intel, Mostek, a 1969 spin-off from TI with barely

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[99] http://www.ti.com/corp/docs/company/history/calc.shtml

50 employees, agreed to develop what would become the first 'calculator-on-a-chip'. Developed in just six months, the MK 6010 (Figure 7-6) was designed specifically for Busicom's new line of small calculators. According to Mostek, Nippon Calculating Machine Company agreed to purchase 60,000 copies of the chip at $30 each. "The company needed that money, and it [Nippon] needed that product. That fact had a very strong influence on our work," said Mostek's Dave Leonard, member of the four-person design team.[100]

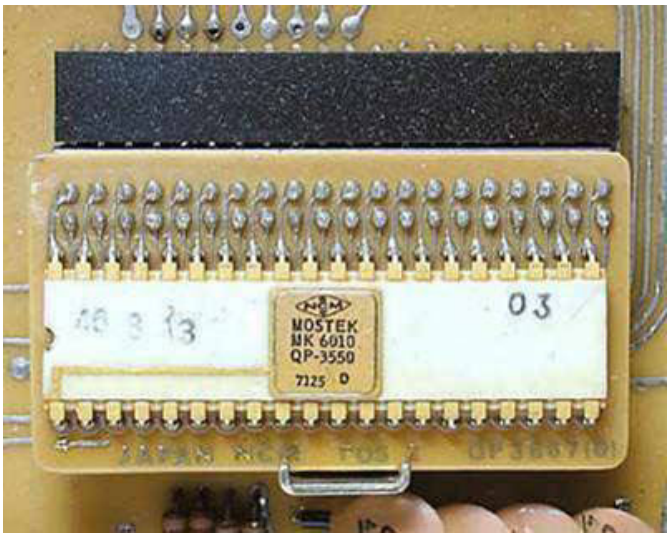

Figure 7-6. Mostek MK 6010 (January 1971)

The 180-mil-square chip contained the logic for a four function 12-digit calculator with more than 2,100 transistors. Note the NCM (Nippon Calculating Machine) marking just above the Mostek name stamped on the chip. The first application of the chip was in an existing desktop machine called the Busicom *Junior* (Figure 7-7a).The single chip replaced 22 chips in the *Junior* calculator and reduced the number of circuit boards from two to one. The MK 6010 would also power Busicom's first "pocket" calculator, the Handy LE-120 (Figure 7-7b). Sold in 1971, the Busicom Handy was the world's smallest handheld calculator for at least a year and was even

[100] Author and date unknown, "The Chip: Mostek engineers had to make history," http://www.mindspring.com/~mary.hall/mosteklives/history/10Ann/thechip.html

advertised as a "palmtop computer." Mostek would go on to develop microprocessors based, in part, on this early accomplishment. Busicom's fate was not as fortunate. It is reported that in 1974 Busicom became the first major Japanese calculator company to succumb to the ensuing calculator price wars, discussed later.

(a) **(b)**

Figure 7-7. NCR 18-16 (Busicom *Junior*), and Busicom Handy LE-120 (1971)[101]

Photos courtesy http://www.vintagecalculators.com/html/integrated_circuits.html

The MK 6010 chip was introduced in January 1971, prior to both TI's TMS1802 and Intel's 4004. More than any other commercial application, calculators represented the single most important driver for early microprocessor/microcontroller development. In 1972 the journal *New Scientist* stated: "Electronic calculators today provide the largest market for LSI, which is mostly of the metal oxide semiconductor (MOS) type."[102]

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[101] The price of the NCR 18-16 (Busicom *Junior*) was £168 Sterling in the U.K. (about U.S. $400) whereas the Busicom Handy LE-120 price was 89,800 yen (about U.S. $390).

[102] Vintage Calculators Web Museum Calculator Technology, Calculator Electronics: Integrated Circuits, http://www.vintagecalculators.com/html/integrated_circuits.html

The three single-chip calculator achievements introduced in 1971 by Mostek, Intel, and TI represented a decade of accumulated learning in both IC and electronic calculator technologies. A brief review of technological progress in electronic calculators with an emphasis on co-evolving IC technology is informative. The calculator was a natural extension of the mechanical 'adding' machine that dates back to the late 19th century. These devices were called *calculators* because they not only performed addition, but also subtraction and most importantly multiplication and division (through repetitive addition and subtraction operations), including in some cases, square root. By the 1950s electro-mechanical calculators performed calculations using relays combined with complex gear systems; some were called *comptometers*. The promise of electronics as a substitute technology brought about a true desktop electronic calculator by the early 1960s. Introduced in 1961 and equipped with vacuum tubes, the *ANITA* (*A N*ew *I*nspiration *T*o *A*rithmetic) Mark 7 and Mark 8 (Figure 7-8), made by the Bell Punch Co. and distributed by Sumlock Comptometer LTD (both in the U.K.), is claimed to be the world's first fully-electronic desktop calculator. ANITA was marketed as an "Electronic Desk Computer" and cost about £355 Sterling (roughly $1000).

Figure 7-8. ANITA Mark 8 (1961)

Photo courtesy http://www.vintagecalculators.com/html/anita_mk_8.html

The ANITA, considered a landmark achievement in the history of calculators, fostered increased attention by U.S. and Japanese calculator manufacturers. The next notable innovation was the Friden EC-130 introduced in 1964 and sold for about $2100 (Figure 7-9). The EC-130 was also a breakthrough product as the first semiconductor-based electronic calculator.[103] Although ICs were available when the EC-130 was designed, they were deemed too expensive so the design used all discrete devices. Other EC-130 innovations included a 10-key serial-entry keyboard, much like today's calculators, and the first calculator to use Reverse Polish Notation (RPN), preceding the HP 9100A, Hewlett-Packard's first calculator, discussed shortly.

Figure 7-9. Friden EC-130 (1964)

Photo courtesy http://www.oldcalculatormuseum.com/f130proto.html

Just as the Friden EC-130 was introduced, the Victor Comptometer Corp. contracted General Micro-Electronics (GME) to supply advanced MOS chips for a new calculator, the Victor 3900.

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[103] At least four Japanese manufacturers also introduced transistor-based electronic calculator models in 1964 including the Sharp (then Hayakawa Electoric) CS-10A, Sony Sobax, Oi-Electric Alpha-Zero, and Canon Canola 130.

The new model was announced as the world's first IC-based calculator. A 1965 print advertisement features a picture of a chip, roughly 15mm square, and reads:

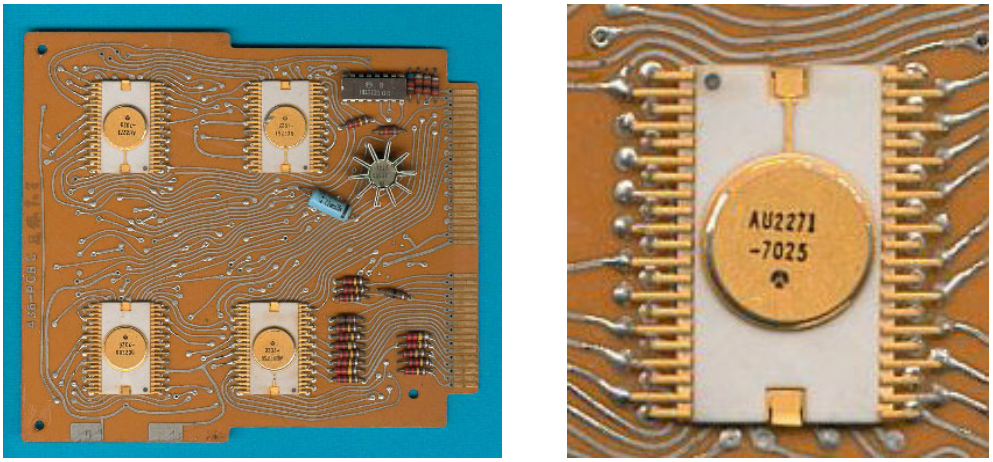
> Victor's incredible little chip (shown here 25 times actual size) ushers in the era of the desk-top electronic calculator! Space-age micro-circuitry, applied with traditional Victor logic, makes it the fastest and easiest to use—as well as the most compact!

The 3900 contained 29 MOS chips, each containing up to 250 transistors, and a very complicated circuit design for the time. GME, the chipmaker, was a 1963 spin-off of Fairchild where MOS had recently been invented. But production problems resulted in poor yields while many chips that did pass initial test later failed in operation. These early LSI ICs made by GME stretched MOS technology too far, proving to be very prone to failure. This meant that very few calculators were produced; it is estimated that about 100 calculators were sold. It is reported that in many cases the machine wouldn't function brand new out of the box. Victor had to scramble to placate frustrated customers by providing high-end loaner (or in some cases, free replacement) electro-mechanical calculators to keep customers from revolting. In the end, most of the machines sold were taken out of service soon after sale. Victor suffered tremendous losses, both financially and in market reputation. After repeated attempts to correct chip reliability problems, Philco-Ford (who had since acquired GME) finally abandoned the program in 1968.

Although the Victor 3900 was a commercial failure, the way was shown that the increasingly popular calculator represented an application for the IC with sufficient volume that chipmakers had been seeking. The GME-Victor supply agreement was also an early model of the collaborative calculator/chipmaker arrangements to follow. The continued reduction in calculator size and cost was led by Japanese calculator makers who witnessed strong domestic demand for these products. Lacking MOS IC production capability, these firms turned exclusively to the U.S. IC industry and key supply relationships were forged. These included Sharp and North American

Rockwell, Canon and Texas Instruments, General Instrument and Sanyo, Fairchild and Casio, and Ricoh and AMI.[104] As previously discussed, Busicom contracted with both Mostek and Intel.

The Rockwell-Sharp agreement resulted in the first true LSI-based MOS calculator, the Sharp QT-8D in 1969. Sharp, formerly Hayakawa Electoric, was an early innovator of electronic calculators in Japan. Tadashi Sasaki, Sharp managing director, saw great potential in the new devices and aggressively planned a new LSI-based calculator. Sasaki traveled to the U.S. to seek out a chip supplier. The requirement called for three million parts totaling $30 million. This was the largest single commercial IC request to date, however Sasaki had great difficulty finding a chipmaker that would agree to take on the project (see Box 7-1). A deal was eventually struck with North American Rockwell's Autonetics Division to develop the advanced chip set (Figure 7-10).[105]



The Rockwell LSI chip set has four MOS LSI chips and a clock generator (round device with star-shaped heat-sink clipped on). Each of the 42-pin DIP ICs contains 900 transistors.

Figure 7-10. Rockwell LSI chip set for Sharp QT-8D (1969)

Photos courtesy http://osaki.cool.ne.jp.information/history/3-rocket/3-rocket.html

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[104] Kenneth Flamm, *Mismanaged Trade? Strategic Policy and the Semiconductor Industry*, Washington, D.C.: Brookings Institution Press, 1996, 72; Robert W. Wilson, Peter K. Ashton, and Thomas P. Egan, *Innovation, Competition, and Government Policy in the Semiconductor Industry*, A Charles River Associates Research Study, Lexington, MA: Lexington Books, 1980, 99.

[105] From the mid 1960s Rockwell had been working on techniques to build large size integrated circuits for NASA projects. Knowledge from this work helped Rockwell develop the calculator chip set and subsequent microprocessors such as the PPS4 and PPS8.

When the Sharp QT-8D calculator (Figure 7-11 middle) was introduced in 1969 it weighed only 3 lbs. and was the first calculator priced under 100,000 yen. The product drew immediate attention. Masatoshi Shima, the Busicom engineer involved in the development of the Intel 4004 (and later the 8080), comments on the reaction to the Rockwell chip set:

> Sharp designed the logic and provided logic schematics to Rockwell. Then Rockwell did a circuit design. It was implemented with only four chips--including a clock. Everybody in desktop calculator companies were (*sic*) shocked.[106]

Box 7-1. Tadashi Sasaki, Sharp and Busicom Calculator Chips

A famous story often told in Japan relates how the chief executive of Sharp [Sasaki] visited the United States in 1968 to work out an arrangement for an American chip company to supply MOS LSI chips needed in its new calculator designs. He visited eleven manufacturers, including Fairchild, TI, Motorola, AMI, National Semiconductor, RCA, Philco, and Sylvania. All rejected his proposal, because the volumes he required were too high for their current capacity, which was largely tied up with defense production. Finally, just as he was leaving the United States, executives at North American Rockwell had him paged at the Los Angeles airport, to tell him they had reconsidered their initial decision to reject the request and would work with him.[107]

[Later] Sasaki asked Rockwell to produce [single functional unit] four-division chips, but Rockwell refused—according to Sasaki because Rockwell was already earning high profits with its other semiconductor devices and did not want this distraction.

In 1968, in the first several months after Intel was founded, [Robert] Noyce visited Sasaki at the Sharp offices in Nara, Japan, hoping to sell Intel's manufacturing semiconductor devices to Sharp. Sasaki felt beholden to Noyce because of the important use he had made of Noyce's earlier results at Fairchild on planar-type semiconductor devices; so he asked Rockwell if it would

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[106] Masatoshi Shima, in interview with William Aspray, IEEE History Center Oral History Program, Rutgers University, New Brunswick, NJ, May 17, 1994, http://www.ieee.org/organizations/history_center/oral_histories/transcripts/shima.html

[107] Ibid., 72, footnote 99.

allow Intel, a new and struggling firm, to produce a small percentage of Sharp's semiconductors. Rockwell refused, pointing to its exclusivity agreement with Sharp. Sasaki had previously given technical advice to Busicom, which is permissible in Japanese business culture since Busicom was small and posed no serious threat to Sharp. Thus he decided surreptitiously to provide 40 million yen to [Yoshio] Kojima [Busicom president], with the stipulation that Busicom would front a contract with Intel to manufacture the four-division chip. This funding was used to pay for the development contract with Intel that led to the development of the 4004 microprocessor.[108]

Sharp continued to exploit the size and cost advantages of MOS LSI technology, introducing the EL-801 *ELSIMINI* (Figure 7-11 right), the first CMOS-based calculator powered with a single IC chip made by Toshiba.[109] After a period of about six years of U.S. dominance in MOS production, Japanese IC makers began to make inroads into this market, especially in CMOS where low power consumption was ideal for calculators that were now truly portable. CMOS knowledge and skills would soon be applied to other IC device types, the most notable being DRAMs.

In summary, the Sharp calculators shown in Figure 7-11 illustrate the size reduction achieved over about four years made possible by developments in MOS IC technology. All three models are basic four function calculators: from left to right are the Compet 22 of 1968, QT-8D of 1969, and EL-801 *ELSIMINI* of 1972. Similar progress was also achieved by literally dozens of companies that entered the calculator field; likewise concomitant price decreases also ensued. As an example, the Compet 22 shown below sold for about 270,000 yen ($1175), while the QT-8D at 99,800 yen ($434) was considered low-priced when introduced one year later. In three more years the EL-801 sold for 39,000 yen ($170), less than half of the QT-8D.

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[108] Aspray, op. cit., 6.
[109] TI was also a supplier of the EL-801 calculator chip.

Figure 7-11. Sharp Calculators: 1968-1972

Photo courtesy http://www.vintagecalculators.com/html/integrated_circuits.html

Sharp Model	Compet 22	QT-8D	EL-801 ELSIMINI
Year Introduced	1968	1969	1972
IC technology (supplier)	83 MSI (Hitachi)	4 MOS LSI (Rockwell)	1 CMOS LSI (Toshiba)
Power source	AC	AC	Battery (4 AA)
Price in yen ($U.S.)*	270,000 ($1175)	99,800 ($434)	39,000 ($170)

* based on exchange rate of 230 yen per dollar

Later in 1972 Casio introduced its one-chip *Mini* priced at 12,800 yen ($55), two-thirds less than the Sharp EL-801 and a bitter price war was underway. The Casio Mini sold one million units within 10 months and six million within 3 years after release.[110] The Casio Mini had opened a new era of family-use pocket calculators. Within a few years calculator prices would half again. In 1971, there were about forty Japanese calculator companies, but by the late 1970s half of these either went bankrupt or exited the market. By decade's end only two firms, Sharp and Casio, together served roughly 80% of the Japanese calculator market. The U.S. calculator market followed a similar path. Many early manufacturers (e.g., Bowmar) did not survive the price war

[110] "Casio Mini Sensation," http://osaki.cool.ne.jp/information/history/7-casiomini/7-casiomini.html

that began in Japan. According to one source, twenty-nine North American and Japanese companies left the calculator business in 1973 and 1974 alone.[111]

Several chipmakers that had designed and supplied calculator chips also integrated forward to develop calculator products. TI has already been mentioned, but others including Rockwell, AMI, and National Semiconductor followed suit. Most of these ventures were short-lived; TI was the only notable one to survive providing a very successful line of increasingly advanced calculators that continue to this day. The other U.S. manufacturer of advanced calculators was Hewlett-Packard (HP). By most measures HP outpaced TI in total offerings and overall quality, but a definite pattern between HP and TI—much in the same manner as the Sharp-Casio duopoly in Japan—would bring forth a continual stream of innovations in calculator technology throughout the 1970s and early 1980s. All firms were sensitive to equally-continual price reductions, however demand for advanced calculators (i.e., scientific, financial, programmable), the niche that HP had carved out, was far less price-elastic. The story of HP's entry into calculators is unique among the others for many reasons. Perhaps the most pertinent to this research is that HP was a *captive* chipmaker; they produced chips in-house for a wide variety of instruments and other products sold to customers. Compared with IBM and AT&T, HP was a small captive producer. However, their entry into the calculator market affords a look into how users—in the von Hippel sense—but internal to the firm helped catalyze microprocessor development efforts, almost by default. Further, by focusing on *programmable* calculators, a distinct computing application, early HP calculator programs reveal how innovation leading toward the microprocessor might have occurred within other computer firms.[112]

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[111] Wilson, Ashton, and Egan, op. cit., 99.

[112] An interesting footnote of industry lore is that the prototype for what would be called the Apple computer was built in 1975 at HP's Advance Products Division (where calculators were made) by then-employee Steve Wozniak. The prototype employed ICs from the lab stock at HP (the company had a written rule that any engineer could take chips from lab stock without cost for a project of their own design if their supervisor approved). Upon completion Wozniak suggested to HP management that they manufacture and sell the device for $800, about the same price as HP's top-end handheld calculators. After weeks of serious consideration HP finally said no. See "Stephen Wozniak: The Making of an Engineer and a Computer," *The*

HP was not unlike most companies engaged in the rapidly-growing electronics field in the mid to late 1960s—all held in common the promise of IC technology advances as a strategic tool. Companies already in the nascent calculator industry, along with tabulator, cash register, and related industries naturally sought the cost and space advantages offered by ICs, particularly employing LSI technology. For HP, the decade of the 1960s witnessed great expansion of HP's capabilities through both acquisitions and internal developments. One example of the latter is that by 1970 HP had started development of their first consumer product, the handheld programmable calculator. This industry first necessitated more powerful calculator logic chip capability than what was available in the conventional 4-function arithmetic calculators at the time. The effort would result in a microprocessor chip set, co-developed by two young, yet-unknown chip companies and rapidly incorporated into what would be HP's most successful new product launch up until that time. A brief background is helpful.

HP was a company with a legacy producing sophisticated instruments, measurement and test equipment for highly technical and scientific users. In 1966 HP was a 27 year-old Fortune 500 company with revenues of $203 million and 11,309 employees.[113] That year HP Laboratories was established where the primary areas of research would include solid state physics, physical electronics, electronics, and medical and electronics instruments. The new lab was instrumental in developing HP's first computer, the HP 2116A, a versatile instrument controller for HP's growing family of programmable test and measurement products. The HP 2116A represented HP's first use of ICs and was capable of interfacing with a wide number of standard laboratory instruments allowing customers to computerize their instrument systems. By this time, automating measurement systems through programmable instruments had become a key HP strategy. The HP 2116A would find many laboratory applications, but it would also pave the way for more

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Computer Museum Report, Volume 17, Fall 1986, http://ed-thelen.org/comp-hist/TheCompMusRep/TCMR-V17.html#Woz

[113] http://www.hp.com/hpinfo/abouthp/histnfacts/imeline/hist_60s.htm

general-purpose computing applications that HP would exploit in the 1970s and 1980s in the rapidly-growing minicomputer industry.

One offshoot of the programmable controller work was the development of the 9100A Desktop Calculator in 1968, also a product of HP Labs. HP marketed the 9100A as a calculator because at the time the perception was that a computer had to be big to be credible. Note that the 2116A computer was the largest single mechanical package HP had built to date while the 9100A was a desktop machine about the size of a typewriter. Bill Hewlett said "If we had called it a computer, it would have been rejected by our customers' computer gurus because it didn't look like an IBM. We, therefore, decided to call it a calculator and all such nonsense disappeared."[114] The 9100A is now recognized by some as the first desktop computer. For example, a phrase in a 1968 ad in *Science* magazine announcing the product reads "The new Hewlett-Packard 9100A personal computer." More than three decades later, *Wired Magazine* named the 9100A the first personal computer.[115]

The 9100A holds the distinction of being the first monolithic desktop scientific stored-program programmable solid-state electronic calculator.[116] The machine provided built-in high-level math functions including trigonometric functions, logarithmic and exponential functions, rectangular to polar conversions, among others. The 9100A used a new language called HPL, described as very much like BASIC language. Programs were written through keyboard entry and a built-in magnetic card reader/writer was used for program and data storage. The desktop machine also used a CRT (cathode ray tube) for display of three data registers (Figure 7-12).

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[114] Ibid., see *Wired Magazine*, December 2000.
[115] http://www.hp.com/hpinfo/abouthp/histnfacts/museum/personalsystems/0021/index.html
[116] http://www.oldcalculatormuseum.com/a-hp9100a.html

Figure 7-12. HP 9100A Programmable Desktop Calculator (1968)
Photo courtesy http://www.oldcalculatormuseum.com/a-hp9100a.html

The 9100A introduced many calculator innovations that were tailored to the scientific user. A most familiar feature in successive HP handheld models is the use of Reverse Polish Notation (RPN), introduced in the Friden EC-130 discussed earlier. RPN is a system for representing mathematical expressions without the use of parentheses (i.e., left-to-right display entry and no 'equals' key on the keypad). Combined with a special 'cordic' algorithm, the 9100A could also handle transcendental functions (i.e., trigonometric, logarithmic, exponentials, hyperbolics and circular functions) with a single algorithm, which naturally produced an internal economy.[117] In 1971 HP was issued a patent for the embodiment of the 9100A.[118]

Interestingly, there were no ICs used in the 9100A. The 9100B, upgraded with more memory and I/O capabilities, soon followed and did employ a few ICs. The reason given for not using ICs in the 9100A is that new LSI devices such as ROMs were unproven at the time so designers chose to use more reliable discreet components (including magnetic core memory).

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[117] Kip Crosby, "The Analytical Engine," (An Interview with Barney Oliver), *Journal of the Computer History Association of California*, Vol. 2, No. 3, May 1995, http://www.chac.org/engine-ascii/engv2n3.txt
[118] Thomas E. Osborne, Calculator Employing Multiple Registers and Feedback Paths for Flexible Subroutine Control, U.S. Patent 3,623,156, Assignee: Hewlett-Packard Company, Filed May 26, 1969, Issued November 23, 1971.

Based on the success of the 9100 series, HP developed the more powerful 9800 series that made use of new technologies including IC chips for RAM, ROM, and logic. The 9810A, the first of these machines, was introduced in 1971 and was equipped with an 8MHz 16-bit processor that used an instruction set designed to resemble the HP 2100 series computers. HP actually produced the 4k-bit ROM chips while purchasing the 1k-bit 1103 RAM chips from Intel. Perhaps the most interesting feature relevant to this research is the many specific references to a *microprocessor* in the patent documentation.[119] The 9800 series would consist of several models (i.e., 9810, 9820, 9830, 9805, 9815 and 9825) over a span of five years that incorporated a number of innovations such as an expanded instruction set, full programming support for languages such as BASIC, and support of numerous I/O devices including a full QWERTY keyboard. By 1975 the 9800 series had evolved into a powerful line of desktop computing systems, but calculator development at HP had since shifted its focus to handheld devices starting with the HP-35 in 1972.

"The HP-35, the world's first scientific handheld calculator," was introduced in February 1972.[120] Coincidental with the development of the 9800 series (at a separate facility in Loveland, CO), Bill Hewlett himself initiated the development of a "shirt pocket-sized HP-9100" on an accelerated schedule. Company lore has it that upon witnessing the capability of the 9100 desktop, Hewlett declared that this capability should be more accessible to users, especially engineers. A former employee recounts:

> In March 1968, Hewlett-Packard introduced the HP-9100A table-top programmable calculator. At that time, Bill Hewlett wondered if the next calculator would not be a tenth the size and cost of the 9100A. Later the goal was formalized to be a series of ten machines to be handheld, battery operated, and capable of being carried in his shirt

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[119] Emil Edward Olander, Jr., et. al., "Programmable Calculator Employing Algabraic Language," U.S. Patent 3,839,630, Assignee Hewlett-Packard Co., Filed December 27, 1971, Issued October 1, 1974. See also near identical patent in Robert E. Watson, Jack M. Walden, Charles W. Near, "Programmable Calculator," U.S. Patent 3,859,635, Assignee: None, Filed June 15, 1971, Issued July 7, 1975.

[120] HP Timeline—1970s http://www.hp.com

> pocket -- which was measured on the spot. Thus the HP-35, HP-80, HP-65, HP-55 were born, along with machines yet to be announced.[121]

The size of the handheld 9100 calculator (later called the 35 because it had 35 keys) was dictated by Hewlett's shirt pocket. In fact, HP originally developed the HP-35 for internal use and later decided to try selling it.[122] The HP-35 went on to produce the highest sales growth of any product the company had ever seen, $100 million in the first year.[123]

The HP-35 was a risky project involving several immature technologies including LSI ICs. Although HP had IC production capability, two chipmakers were sought out to design, develop, and supply the logic ICs for the HP-35: Mostek and American Microsystems, Inc. (AMI). Both companies were previously mentioned: Mostek was the first to introduce a 'calculator-on-a-chip' for Busicom while AMI had developed the MP944 microprocessor chip set for the F-14A. Some brief background on both companies is important. Mostek was founded in 1969 as a spin-off of TI to specialize in MOS LSI ICs. Within its first year, Mostek developed the first 1K-bit DRAM and began development of the Busicom single-chip calculator. When HP approached them with the HP-35 request, Mostek was barely a year old. Characteristic of most start-ups at the time, Mostek was hungry for work, thus involved in many requests for custom chips.

Tracing its lineage to Fairchild, AMI was formed in 1966 just as the infant MOS market was beginning to surface.[124] Formed by personnel who left General Micro-Electronics (GME), the chipmaker that could not get early MOS chips to work for the Victor 3900 first IC-based calculator, AMI was successful in setting up a trouble-free production process. AMI discovered a large MOS market awaiting them:

> AMI President Howard S. Bobb explains simply that he wanted his company to do well at the job—manufacturing—that General Micro did worst. His determination paid off. Sales

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[121] Gene Wright, "PH or HP?" http://www.dotpoint.com/xnumber/hp_or_ph.htm "This article first appeared in the V2N1 issue of 65-Notes (January 1975), published by Richard Nelson. Gene Wright made additions to the article."
[122] http://www.hpmuseum.org/hp35.htm
[123] http://www.danderby.com/hp35_c.htm
[124] Business Week, "An integrated circuit that is catching up: A $1-billion market may await MOS devices by the mid-1970s," April 25, 1970, 136.

> have climbed from $1-million in 1967 to $3.5-million in 1968 and to $7.65 million last year [1969]; every penny came from MOS.[125]

AMI's business strategy, however, was unique among the dozens of new chip companies (like Intel and Mostek) attempting to develop standard products for high-volume production. Recall, for example, Intel's initial reluctance to Datapoint's special request that became the 8008. In contrast to most chipmakers, AMI's specialty was in *custom* ICs. AMI would be a pioneer in the field later called application-specific ICs (ASICs). Wilf Corrigan, former CEO of Fairchild, would associate ASICs as "the business nobody wanted," but go on to co-found an ASIC design-only firm called LSI Logic Corp. in 1981, thus launching a new business model of *fabless* semiconductor operations that specialize in supporting today's burgeoning ASIC field.[126] Prior to all this, AMI stood alone while others abandoned the resource-intensive custom-chip business in the 1970s:

> The only major company that continued to pursue custom design was American Microsystems Inc., which had lots of experience in calculator chips. AMI engineers knew how to handcraft custom designs.[127]

AMI's custom-chip strategy was initially very successful. In fact, AMI rapidly became the leading MOS chipmaker. Table 7-3 reveals that AMI maintained a strong leadership position through 1975 among the more notable start-ups of the late 1960s.[128]

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[125] Ibid.
[126] George Rostky, "ASICs: the business nobody wanted," *EE Times*, in "The Century of the Engineer: Misunderstood Milestones," 2000, http://www.eetimes.com/special/special_issues/millennium/milestones/corrigan.html
[127] Ibid.
[128] AMI also achieved the rank as the tenth leading U.S. merchant IC manufacturer in 1975. However, disappointing financial performance resulted in a major management shake-up in 1976. By this time almost all the large chipmakers had dropped out of the custom chip market, leaving this business to the small houses. Mostek's success would soon outpace AMI. Both companies would eventually be acquired. Mostek merged with United Technologies in 1979 and was later bought by SGS-Thompson in 1987, whereupon 80% of its workforce was dismissed. AMI was purchased by Gould/Japan Energy in 1982. The remnants of AMI still exist as AMI Semiconductor (AMIS) employing 2,400 worldwide on 2002 sales of $345 million. http://www.amis.com

Table 7-3. Semiconductor Company Sales for Selected Companies 1970-1975
(all companies were 100% semiconductor sales)[129]

	Started	1970	1971	1972	1973	1974	1975
Advanced Micro Devices, Inc.	1969	---	1.3	4.6	11.2	26.4	25.8
American Microsystems, Inc.	1966	28.5	24.2	28.9	58.1	75.3	66.1
Intel Corp.	1968	4.2	9.4	23.4	66.2	134.5	136.8
Intersil, Inc.	1967	3.7	8.4	12.5	24.2	28.8	25.5
Mostek Corp.	1969	1.0	3.6	17.7	41.9	60.1	47.1

Source: Federal Trade Commission, *Staff Report on the Semiconductor Industry: A Survey of Structure, Conduct, and Performance*, Bureau of Economics, January 1977, Tables C-8 and C-16, 177 and 185.

Given this background and from the experience both chipmakers had accumulated with Japanese calculator programs, it is not surprising that HP chose them to develop the logic ICs for their handheld calculator. HP designed the logic while AMI and Mostek manufactured the chips. It is also reported that AMI assisted in algorithm development. When introduced in February 1972 the HP-35 (Figure 7-13a) had one microprocessor chip, one I/O control chip, three ROM chips, and one clock chip.[130] Logic IC technology used in the HP-35 is shown in Figure 7-13b. The microprocessor is the 16-pin ceramic arithmetic & registers chip in the lower right. The larger 28-pin ceramic chip on the left was for I/O control & timing. Both chips are embodied in dual in-line packages (DIP). Support chips include the 8-pin plastic clock driver chip (upper right) and three 10-pin cylinder ROM "cans" (center). AMI supplied all chips shown here, with the exception of the 8-pin clock chip made by HP. Later calculator versions would feature Mostek chips in combination with AMI chips or as sole supplier. It is reported that Mostek would become HP's largest supplier of calculator chips by the mid 1970s.

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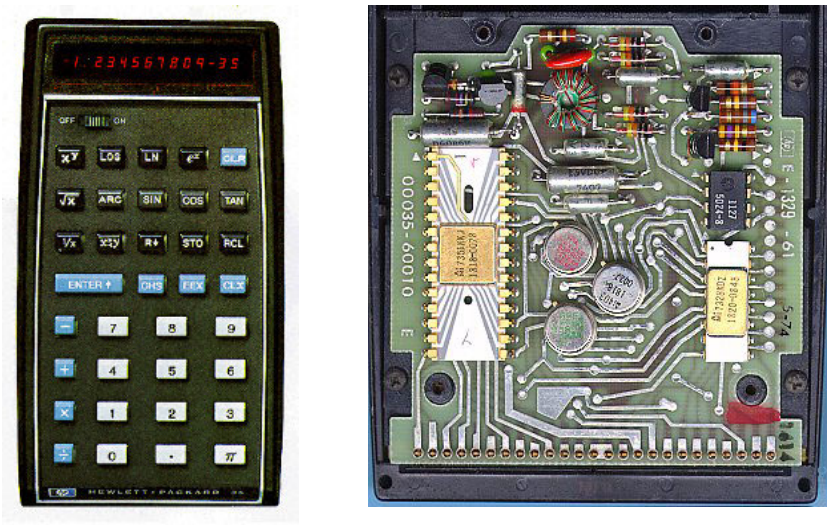
[129] Leading IC makers like TI, Motorola, Fairchild along with some smaller companies such as National Semiconductor also sold other products.
[130] James Redin, "The Death of the Slide Rule," http://www.dotpoint.com/xnumber/hp.htm



(a) **(b)**

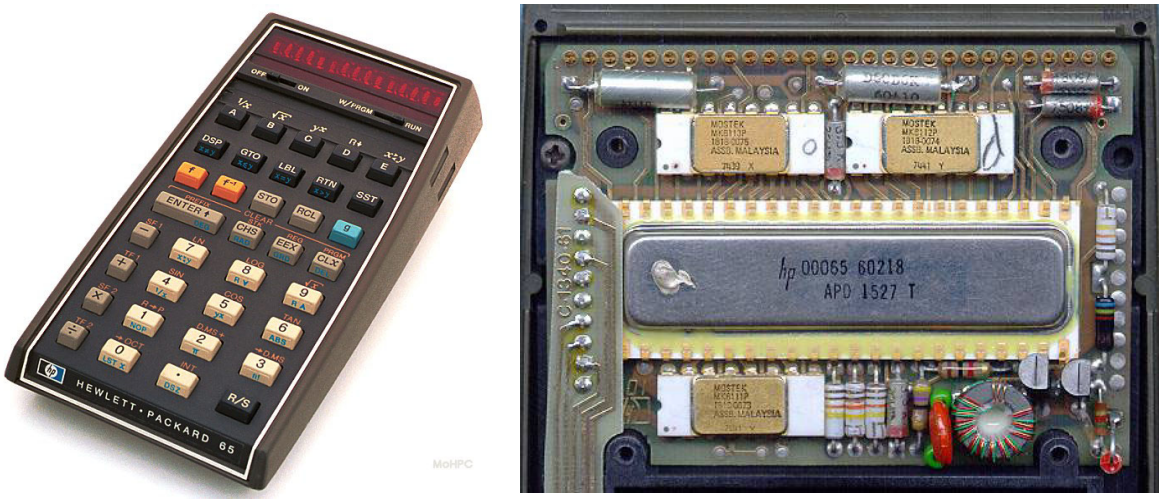
Figure 7-13. HP-35 and internal logic PCB (1972)

Photos courtesy
http://www.computerhistory.org/timeline/timeline.php?timeline_year=1972 and
http://www.hpmuseum.org/

As previously discussed, there were at least three single calculator chips that preceded the HP-35 embodiment. Coincidentally, the first one of these introduced a full year earlier was the Mostek MK 6010 for Busicom handheld calculators. Why the HP-35 calculator chips deserve recognition is that they were the first to provide *scientific and other advanced calculator functions*, capabilities far beyond the operations of (an) arithmetic 4-function calculator chip(s). HP, as a captive IC maker, was not in the business of selling chips so the efforts involved in the design and manufacture of these most-important calculator components was largely hidden from public view.

Within 18 months of the HP-35 introduction, HP would introduce the HP-80 (financial calculator with a shift key), HP-45 (first scientific calculator to have a shift key, nearly doubling the computational power of the calculator), and most importantly, the HP-65, the first *programmable* handheld calculator (with a magnetic card reader/writer, Figure 7-14a). The HP-65 was the calculator Bill Hewlett had originally envisioned as the 'handheld 9100'. Two other models

followed through 1975 (i.e., HP-70, HP-55); all used what is now labeled "Classic Series Technology" based upon AMI/Mostek logic chips.[131]



(a) (b)

Figure 7-14. HP-65 Programmable Calculator (1974) and Logic PCB with Hybrid CPU (1973)

Photos courtesy http://www.hpmuseum.org/

The HP-65 was controlled by a hybrid CPU (Figure 7-14b), a 44-pin hybrid circuit containing six chips believed to be: arithmetic and registers, control and timing, (2) RAMs, clock driver and init, and card reader controller.[132] The package is marked with an HP part number but is also claimed to be manufactured by Mostek.[133] Comparing the HP-35 logic chip arrangement (Figure 7-13b) with the HP-65 single logic module reveals the progress made in IC packaging over an 18-month period. Consider also that the functionality of the programmable HP-65 was so much greater than the HP-35. Essentially the number of logic chips had doubled (the three ceramic DIP ICs in the HP-65 are ROMs like the three cylinder chips in the center of the HP-35 PCB), yet all was consolidated within a single package.

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[131] The Museum of HP Calculators, "Classic Series Technology," http://www.hpmuseum.org/techclas.htm
[132] Tony Duell, "HP65 Internals," Lecture at Cambridge University Computer Preservation Society, February 26, 2002, http://www.cam.ac.uk/societies/cucps/20012002/hp65.txt
[133] "MOSTEK Calculator Integrated Circuits," Datamath Calculator Museum, http://datamath.org/Mostek_IC.htm

By 1974, HP had begun development of its second generation of handheld calculators, known commonly as the 20 series (e.g., HP-21, HP-25, etc.). The heart of the 20 series calculators as well as many pocket calculators that followed was the Arithmetic, Control and Timing (ACT) chip. This chip integrated the earlier generation's register, arithmetic, control, and clock driver circuit into a single package reducing size and cost.[134] In the course of about six years, HP's calculator technology had advanced from several hundreds (or thousands if ferrite cores are counted) of discrete components on the 9100A to advanced MOS LSI ICs culminating in a single calculator (ACT) chip. By every conventional measure HP lagged the broader calculator industry in semiconductor technology when it entered the market in 1968. But with the knowledge accumulated from introducing one new model after another while focusing on more advanced products enabled HP to catch up and in some cases surpass others in the use of LSI IC technology. While HP may not have figured directly into the microprocessor development story, the kind of technology advances demonstrated by its calculator IC requirements illustrates that they, and probably many others, truly affected the process indirectly. Through engaging in a consumer market where cost, size, and speed to market were stronger factors than in industrial markets, HP's calculator families evolved rapidly, bringing with them increased integration of the control circuitry. With each new product the control circuitry absorbed more functionality until eventually a single chip was sufficient.

In summary, technological advance in calculators co-evolved with similar advances in ICs. The evolution from SSI to MSI to LSI (and ultimately to VLSI) is most evident in calculator applications. In this sense, the calculator brought forth the microprocessor. Finally, the emergence and widespread diffusion of the electronic calculator is a great early success story for IC technology in its own right. The benefits afforded the industry are reflected in the following quotes from Braun & Macdonald (1982):

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[134] "20 Series Technology and Packaging," The Museum of HP Calculators, http://www.hpmuseum.org/tech20.htm

> Tell somebody to divide 12 by 12 and they pull a calculator out.[135]
>
> It has been very difficult to come up with another hand-held calculator … There is no readily apparent product like that that is the next candidate that one could essentially execute as an integrated product to open up a new market without engaging somehow or other with other industries.[136]

IV. Microprocessor-related Patents

This final section considers a sample of U.S. patents filed prior to the patent filing for the Intel 8080, considered the first general-purpose microprocessor. Table 7.4 lists two dozen patents in chronological order by date originally filed. The last entry is the Intel 8080 patent (filed December 31, 1974). The appendix provides an abstract of each patent. While it is beyond the scope of this research to examine individual patents, the main purpose of this section is to demonstrate the breadth of similar inventive activity that is available through public record. It is understood that patent information alone does not present the full picture, and may even provide an incorrect one (e.g., the Hyatt and Boone patents discussed earlier). Nonetheless, these records do offer a glimpse at the kind of related activities that spanned a variety of industries that included calculators as previously discussed, but also mainframe computers, cash registers, programmable terminals, industrial controllers, and others. A more extensive review of patent information may demonstrate that others preceded Intel with a microprocessor embodiment. For now, the purpose is to reinforce previous analysis that supports the idea that the invention of the microprocessor was more of an evolutionary process than a revolutionary event.

Table 7-4. Early Microprocessor-related Patents[137]

Date Filed*	Patent	Title	Assignee
1966-12-21	3,462,742	Computer System Adapted to be Constructed of Large Scale Integrated Circuit Arrays	RCA Corporation
1969-06-13*	3,760,375	Source Data Entry Terminal	Sycor, Inc.
1969-09-27	3,579,201	Method of Performing Digital Computations Using Multipurpose Integrated Circuits…	Raytheon Company

[135] Suhael Ahmed, quoted in Braun & Macdonald, op. cit., 192.
[136] Dean Toombs, quoted in Ibid., 202.
[137] U.S. patents filed prior to and including Intel's 8080 patent (filed December 31, 1974).

1970-09-14	3,702,988	Digital Processor	National Cash Register
1970-10-01	3,654,617	Microprogrammable I/O Controller	IBM Corporation
1970-12-28*	4,942,516	Single Chip Integrated Circuit Computer Architecture	None [Hyatt]
1971-06-15	3,859,635	Programmable Calculator	None [Hewlett-Packard]
1971-08-31	3,757,306	Computing Systems CPU [Boone]	Texas Instruments
1971-08-31	4,037,094	Multi-functional Arithmetic and Logical Unit	Texas Instruments
1971-09-03	3,757,308	Data Processor	Texas Instruments
1971-11-17	3,748,452	Electronic Cash Register	Alan M. Vorhee
1972-09-22	3,793,631	Digital Computer Apparatus Operative with Jump Instructions	Westinghouse Electric
1972-11-20	3,878,514	LSI Programmable Processor	Burroughs Corporation
1972-12-26	3,943,495	Microprocessor with Immediate and Indirect Addressing	Xerox Corporation
1973-01-22	3,821,715	Memory System for a Multi-chip Digital Computer [4004 memory]	Intel Corporation
1973-08-27	3,999,165	Interrupt Information Interface System	Hitachi, Ltd.
1974-01-02	4,087,852	Microprocessor for an Automatic Word-Processing System	Xerox Corporation
1974-05-30	3,986,170	Modular Control System Design With Microprocessors	GTE Automatic Electric Labs, Inc.
1974-09-04	4,177,511	Port Select Unit for a Programmable Serial-bit Microprocessor	Burroughs Corporation
1974-10-07	3,984,813	Microprocessor System	Fairchild Camera and Instrument Corp.
1974-10-15	3,970,998	Microprocessor Architecture	RCA Corporation
1974-10-30	3,987,418	Chip Topography for MOS Integrated Circuitry Microprocessor Chip	Motorola, Inc.
1974-11-26	3,980,992	Multi-microprocessing Unit on a Single Semiconductor Chip	Burroughs Corporation
1974-12-31	4,101,449	MOS Computer Employing a Plurality of Separate Chips [8080]	Intel Corporation

* date originally filed

Limitations and caveats

Before proceeding a few notes on patents should be pointed out. First, recall the sentiment expressed in Moore's quote (and echoed by others) at the very beginning: "Frankly, we didn't think the microprocessor *per se* was that patentable." This was conventional thinking as most others did not seek to claim the microprocessor a unique embodiment. Noyce and Hoff (1981) state that as of mid 1974, nineteen microprocessors were either available or announced, and one year later the number had grown to 40; by 1976 the total had risen to 54.[138] Appendix 6A lists at least 24 firms that were producing or were about to produce microprocessors in late 1975 (FTC, 1977). Of these, only seven appear in Table 7-4 as assignees including the "big 3" IC makers at the time (i.e., Fairchild, Motorola, and TI) along with a fourth, Intel. From a practical standpoint, Table 7-4 is not a complete list of all possible microprocessor-related patents but a sample of the more probable ones based on the author's review of keywords and diagrams. Since the term *microprocessor* was not used commonly until the mid 1970s, terms like *micro-computer*, *LSI* or *IC* combined with *computer* or *processor*, and variations thereof were used in searching online patent databases.[139]

Even if it were possible to list all patents, not all inventions are ever patented. Some inventions, like the first microprocessors, were simply not considered patentable as just discussed. This is probably true in many other cases, but another unique aspect of early semiconductor innovations should be noted. Beginning with the historic precedent set by AT&T in the early to mid 1950s of selling licenses for their transistor designs and process technologies, it had become common industrial practice to openly sell or exchange the use of patents through licensing arrangements. Among other effects, this tradition reduced the normal incentive to use a patent to protect intellectual property. Based upon extensive field research of industry officials in the late 1970s, Wilson, Ashton, and Egan (1980) argue that cross-licensing practices (i.e.,

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[138] Noyce and Hoff, op. cit., 14.
[139] Delphion Research http://www.delphion.com and U.S. Patent and Trademark Office http://www.uspto.gov/ both have search engines that access their online patent databases.

exchanging patent rights) and the rapid pace of innovation combined as limiting factors for patent activity in semiconductor technologies, minimizing the traditional incentive for innovation:

> The overwhelming view among industry executives is that patents provide little incentive for innovation in the semiconductor industry. Two main reasons for the failure of patents to provide an incentive exist. One reason is that semiconductor patents are so numerous that firms have to cross license each other. Without cross licensing and of several firms could block others from producing, and wasteful legal confrontations would result. Second, the time required to obtain a patent is long in relation to the speed with which semiconductor technology changes. As one executive put it, "the payoff comes from charging ahead with the innovation. Patents may provide some protection later."[140]

Further, some scholars have argued that a key motivation to early semiconductor patents was in order to license extensively, and derive revenues from selling these rights. Some firms collected a significant portion of their total revenues from licensing fees. A related factor is the early practice of second (and sometimes third) sourcing required by many users of semiconductor devices to insure a ready supply of needed components. Recall that the time period examined here (late 1960s to early 1970s) was in today's vernacular a very "fluid" time in the semiconductor industry. Characterized by spin-offs and start-ups, this is the era when "Fairchildren" were spawned and when the phrase "Silicon Valley" was coined. The unstable nature of these times underscored the necessity of second source practices.

Most of these small start-up firms typically had little to no formal research (R&D) programs, the traditional source of patent applications. Recall that in Intel's case in particular, the founders intentionally set up the organization *without* a separate R&D group.

Most of these small start-up firms typically had little to no formal research (R&D) programs, the traditional source of patent applications. Recall that in Intel's case in particular, the founders intentionally set up the organization *without* a separate R&D group. Writing from this era and consistent with the discussion on engineering knowledge in Chapter 3, Orme (1979) points out that the industry’s tradition had been for frequent and informal contacts, by word of mouth,

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[140] Wilson, Ashton, and Egan, op. cit., 62.

between design engineers in competing firms and for top engineers to be permanently and potentially ‘on the hoof', rendering patents almost academic.[141]

Also, the resources and filing costs involved prohibited small firms especially from seeking patents that might otherwise have been sought by more established organizations. Finally, patent filing typically followed embodiment (i.e., reduction to practice) so that in most cases a patent was a lagging indicator of invention. Masatoshi Shima, the Busicom engineer involved in the Intel 4004 and who also shares the patent on the Intel 8080, reinforces the 'patent last' philosophy but explains that this patent filing pattern gradually underwent change as patents became more of a competitive tool:

> …at that time [circa 1970], in the case of the United States, rather than writing a patent, companies found it better to develop a functional product as soon as possible. That is a much stronger way compared with patenting. Many times I was told by Intel that if an idea came out you should develop the product first, then bring the paper to the IEEE, then write the patent. Therefore, product, paper, and then patent. That was the priority. But after 1975 or 1976, this pattern changed: write patent first, then write the paper, and afterward make the product. Motorola did it in such a way for 6800. Thus the paper was written two years before the real 6800 sample.[142]

Despite these shortcomings, the patents listed in Table 7-5 do offer useful insight and at least beg for additional research. As one example, four of the first five patents filed (all filed prior to the infamous 'Hyatt' patent application discussed earlier) are from large firms primarily in the computer field. Also, the computer firms listed as assignees are mainly mainframe companies; absent are minicomputer manufacturers. This point is interesting because many involved in the invention of the microprocessor had been influenced by simple minicomputer architectures such as the DEC PDP-8. Table 7-5 summarizes the entire list by broad industry sector.

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[141] Michael Orme, *MICROS: a pervasive force, A study of the impact of microelectronics on business and society 1946-90*, London: Associated Business Press, 1979, 123.
[142] Masatoshi Shima interview, op. cit.

Table 7-5. Summary of Early Microprocessor-related Patents

Industry Sector	#	% of total
Computers	10	42%
Merchant Integrated Circuits	7	29%
Special Purpose Applications	5	21%
Industrial Control	2	8%

An important point about this categorization is that there is considerable overlap. Several companies were also *captive* IC makers, namely RCA, IBM, Burroughs, Westinghouse, even HP as previously discussed. While these companies felt compelled to protect their inventions, by definition they would not have marketed their embodiments as stand-alone products as merchant IC makers would have. Thus knowledge of these activities would not have been commonly shared, except of course through the patent literature. As an example of this kind of work one patent will be examined in more detail; it is the first one listed, U.S. Patent 3,462,742: Computer System Adapted to be Constructed of Large Scale Integrated Circuit Arrays, filed by Miller, Linhardt, and Sidnam of RCA Corporation on December 21, 1966 and published August 19, 1969.

U.S. Patent 3,462,742 [excerpted by page number, column number]

[p6, Col 5] *A review will now be made of the architectural construction of the computer system illustrated in FIGS. 1 through 3. The computer system includes a plurality of units necessary for performing the functions inherent in a general-purpose, stored-program computer…*

[p6, Col 6] *In the system of FIG. 1, each of the five units is constructed of a very large number of elemental circuits or gates… each of the four units [MCU, AMU, MU, and IOU] is geometrically feasible of fabrication in the form of a single integrated circuit array including 300 gates, necessary interconnections, and less than 100 peripheral terminals for connection with the system buses.*

However, the present state of development of the art of constructing integrated circuit arrays has not yet reached the point at which 300 good and operable gates can be constructed as a single integrated circuit array under factory production conditions. Therefore, the four listed main units in the system of FIG. 1 are shown as each divided into two units in the system of FIG. 1 are shown as each divided into two units with the partitions represented by dashed lines…

It is therefore seen that the system architecture of the invention is adaptable to being fabricated using integrated [p7, Col 7] *circuit arrays of various sizes. That is, the designer will normally use integrated circuit arrays of as large a size (containing as many gates) as is available for production purposes. However, if the available arrays cannot be made to have as many gates as are needed to constitute a complete unit, the unit may be partitioned into a plurality of smaller arrays that are designed to be partially autonomous in operation.*

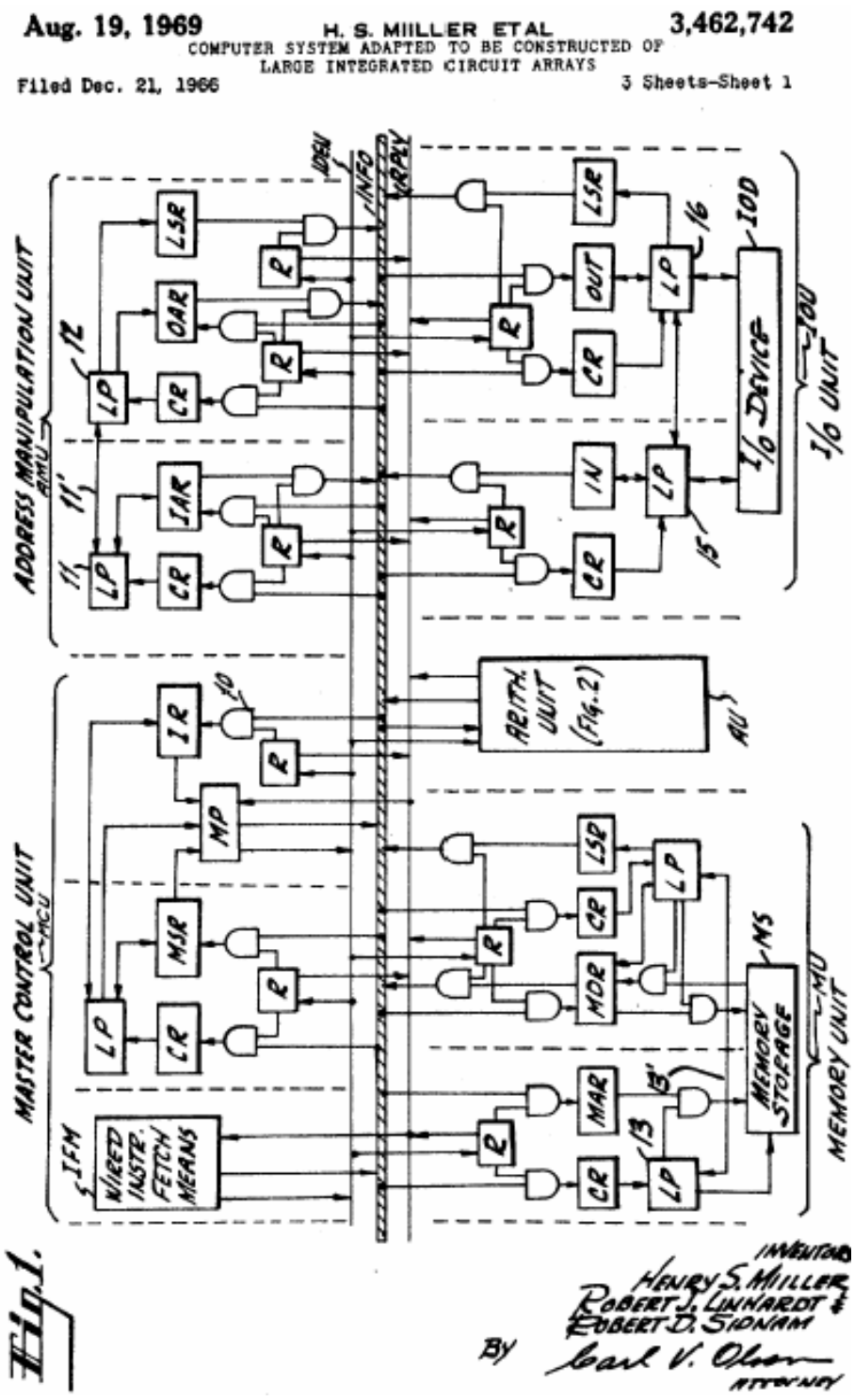

Figure 7-15. U.S. Patent 3,462,742 Figure 1

Source: H.S. Miller et al, "Computer System Adapted to be Constructed of Large Scale Integrated Circuit Arrays," U.S. Patent 3,462,742, RCA Corporation, August 19, 1969, 1.

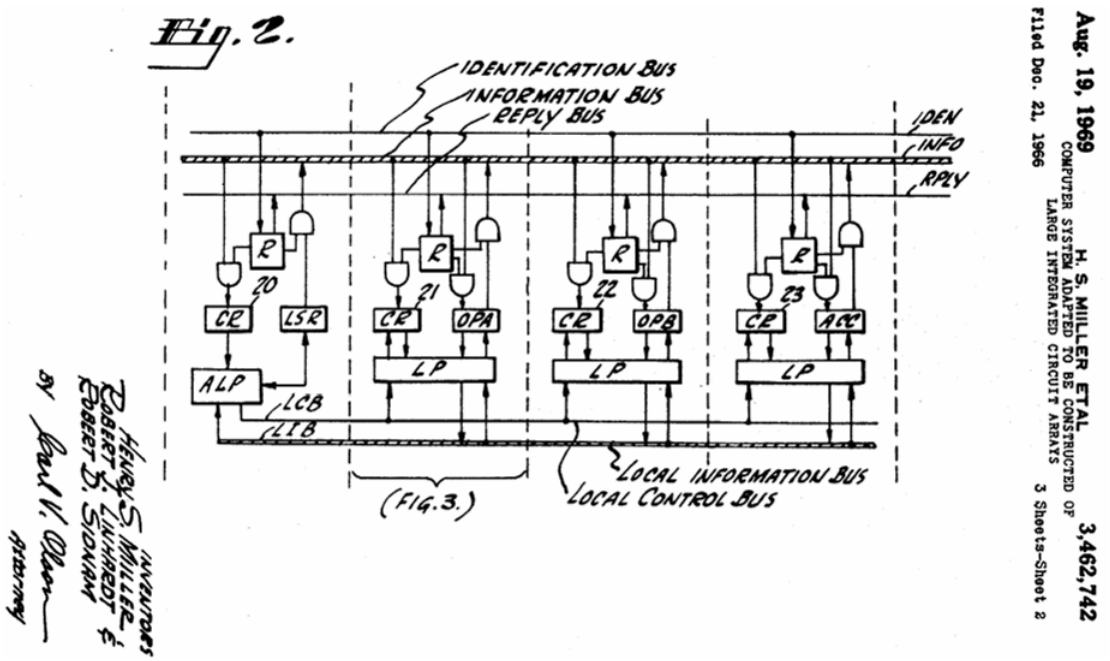

Figure 7-16. U.S. Patent 3,462,742 Figure 2

Source: ibid, 2.

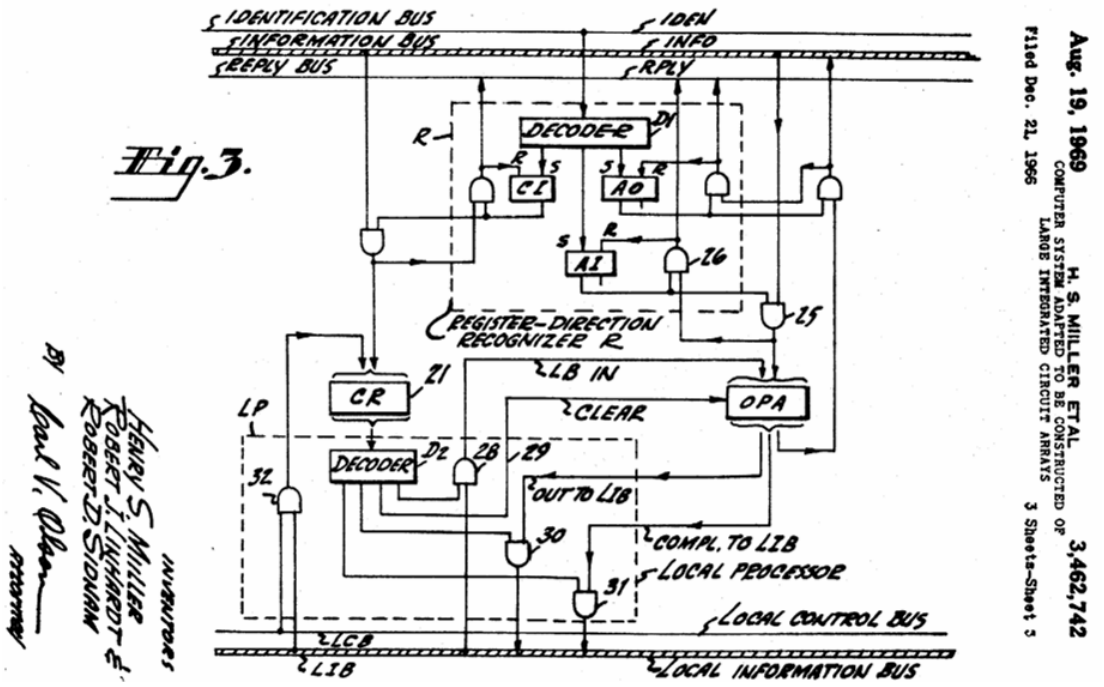

Figure 7-17. U.S. Patent 3,462,742 Figure 3

Source: ibid, 3.

[p7, Col 8] …*The concept of using the described system buses and connecting substantially autonomous integrated circuit array units to the buses permits the construction of a whole family of easily enlargeable or contractable computers according to the changing need of the user.*

Analysis

Figure 1 (7-15) reveals as few as five and as many as ten IC arrays. Figure 2 (7-16) is an expanded view of the Arithmetic Unit of Figure 1 apparently because the "arithmetic unit AU may constitute about sixty percent of the hardware of the entire computer system." Figure 3 (7-17) is a similar breakout of one of the register blocks from Figure 2. Thus, Figures 2 and 3 represent as few as one (already counted as the AU in Figure 1) or as many as eight IC arrays (depending on the number of registers, four are shown here). Hence, the total number of IC arrays could be as high as 17 or possibly more. According to Stan Mazor *IC array* meant an integrated circuit:

> "IC array" means chips. One reason is that we were using chip designs known as gate arrays, which were a general array of gates that allowed a separate metal layer of on-chip connections to define the chip (array's) functions. So I think it is safe to say this means separate chip.[143]

In fact, several firms were making IC arrays at the time. Captive array makers included RCA, IBM, even Raytheon (see U.S. Patent US 3,579,201), while leading merchant producers Texas Instruments and Fairchild even called their approaches "Discretionary Wiring" and "Micromatrix" respectively.[144] The motive for this technology was anticipated demand for custom circuits; in this case a kind of off-the-shelf approach to meeting unique needs. By building wafers for inventory containing ICs with different standard logic gate designs—but not completely interconnected—then pulled and processed through final masking to connect the logic gates on the wafer into the customer's unique circuit requirements, a custom circuit could be made in relatively large volumes.

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[143] Mazor e-mail, July 30, 2003, op. cit.
[144] Michael Borrus, James Millstein, John Zysman, *U.S.-Japanese Competition in the Semiconductor Industry: A Study in International Trade and Technological Development*, Berkeley: Institute of International Studies, University of California, 1982, 23.

In this particular case IC arrays provided the basis for a CPU design using but a handful of neatly partitioned chips. This idea precedes all others yet stated by about three years, but it is clear from patent excerpts that the state of development of IC fabrication was not capable at the time to produce such chips with reliability. Recall GME's failed attempt to reliably produce the 29 MOS chips for the first IC-based calculator, the Victor 3900, around the same time. The more important point is the fact this 1966 design—from RCA, then a computer *and* chip maker—incorporated partitioning of processor functions so that it would be possible to reduce the chip count as fabrication state-of-the-art would allow. Partitioning of CPU functions for the purpose of IC fabrication was a key contribution of this early RCA patent. The last excerpt is worth noting again: "The concept … permits the construction of a whole family of easily enlargeable or contractable computers according to the changing need of the user." The idea of a universal computer design that could be easily enlarged or contracted to fit the needs of the user through the use of IC array technology seems to anticipate both the microprocessor and the supercomputer (via parallel processing). This is an example of the custom IC approach taken well beyond calculators, one of the major custom IC applications at the time.

Regarding process technology, RCA was the first company to pursue MOS technology vigorously, with much of its work done under government contract, according to Bassett.[145] In 1965 RCA won a large contract from the U.S. Air Force for R&D on CMOS that devoted almost its entire MOS program to CMOS. It was referred to as the "CMOS array effort."[146] There is no specific reference to MOS or CMOS in this patent, but the levels of integration indicated strongly suggest MOS technology, capable of chip densities by factors of up to four over bipolar technologies. According to Cserhalmi, Lowenschuss, and Scheff (1968), RCA was also developing around this time the LIMAC (Large Integrated Monolithic Array Computer), a 16-bit

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[145] Bassett, op. cit., 313.
[146] Ibid., 316.

machine grouped into functional execution units, and governed by micro-instructions.[147] The authors state that although this concept favors large arrays,

> [LIMAC] is not restricted to any specific size. As semiconductor technology improves, more circuits can be included in a package which leads to increased gate-to-pin ratio and decreased unique parts in this particular system organization.[148]

Note the similarities between this design concept and rationale provided in a Burroughs patent referencing work from a patent filed several years later in 1972 when the state-of-the-art for single chip LSI fabrication had been achieved:

> 2. Description of the Prior Art
>
> Advances in the field of integrated circuits have led to an increase in the number of transistor gates which a circuit chip can accommodate from a very few up to hundreds and even in excess of a thousand gates. Such advances have made it possible to begin considering placing an entire small data processor on a single integrated circuit chip. This, in turn, provides the economic advantage of mass production in that, once the circuit masks for fabrication of the chip have been designed, the entire processor can be automatically manufactured much more cheaply than when a number of such chips are required to accommodate the processor, and certainly more cheaply than when a processor is formed of discrete components. A particular example of a small processor being placed on a single integrated circuit chip is illustrated in the Faber Patent Application No. 307,863, filed Nov. 20, 1972, now U.S. Pat. No. 3,878,514, which application is assigned to the assignee of the present application.[149]

V. Discussion

This chapter has explored the invention of the microprocessor considering surrounding factors in more depth than typical treatments of this important "event." The factors considered here include:

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[147] N. Cserhalmi, O. Lowenschuss and B. Scheff, "Efficient partitioning for the batch-fabricated fourth generation computer," *Joint Computer Conference*, Fall 1968, 858. Also see Howard R. Beelitz, et al, "System architecture for large-scale integration," Proceedings of Fall Joint Computer Conference, 1967, and Howard R. Beelitz, "Electrical System and LSI Standard Cells," U.S. Patent 3,573,488, Assignee: RCA Corporation, filed September 5, 1967, published April 6, 1971.

[148] Ibid.

[149] : Bernardo Navarro Levy and David Chin-Chung Lee, "Multi-microprocessing Unit on a Single Semiconductor Chip," U.S. Patent No. 3,980,992, Burroughs Corporation, Detroit, MI, filed 11-26-1974, published 09-14-1976, p12, Col 1.

Expected achievement

The microprocessor (or any single-chip embodiment) was an expected achievement by technologists. The question was not whether but when. An implicit roadmap toward increased integration had formed as ICs transitioned from SSI to MSI to LSI levels throughout the 1960s. Moore's Law would later describe this phenomenon. A consensus gradually emerged that MOS technology, with its high-density advantages, would make the single-chip idea an ultimate reality. Numerous accounts suggest this eventuality, although most in retrospect. But a few lead the invention such as Hoff's assertion in a 1970 article:

> [A]n entirely new approach to the design of very small computers is made possible by the vast circuit complexity possible with MOS technology. With 1,000 to 6,000 MOS devices per chip, an entire central processor may be fabricated on a single chip.[150]

Most convincing though is the RCA patent for a computer system constructed of large IC arrays (chips) that when filed in 1966 led all claims discussed here by almost three years.

Differing motivations

Another consideration was that different members of the innovation network defined the problem or goal from their own perspective which meant that certain applications would serve to define the microprocessor more than others. For example, chipmakers saw increased integration as a technical challenge and actively sought new uses for devices that often ran ahead of the apparent need for them. The microprocessor, first called a "micro-computer" by Intel, is a great example of a product in search of a market. Cost seemed to be the chief driver. As Mazor emphasizes, the real significance of the microprocessor was that "it was cheap!"

Small system designers also envisioned the possibility of reducing the size of CPU capability to fewer and fewer devices. This behavior is most visible in low-end computing applications like calculator products (e.g., Sharp, HP, Busicom) and is also evident in special-purpose applications (e.g., Datapoint 2200). In many ways, though, larger computer systems were the exception. A

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[150] Hoff interview with Walker, op. cit.

contemporary computer was a much more complex and expensive industrial product where the CPU represented a small fraction of the overall system so microprocessor designs were not as cost-sensitive. For example, pin count, a major cost factor, was a key constraint in Intel's 4004 and 8008 designs—the 4004 patent is more about pin count economy than anything else. These were custom chips that Intel, as a memory company, was hoping to sell lots of and very cheap. Contrast this with the Four-Phase AL1 8-bit CPU slice on a 40-pin chip that predated both Intel chips. Also a MOS device, Mazor estimates the AL1 unit cost as approaching $1000, well above the $100 (or less) cost of Intel chips.

A second consideration related to higher-end computer usage of the microprocessor was the trade-off between bipolar and MOS technology: computers required much higher speed and performance capabilities than initial microprocessors could deliver. Thus, computer firms generally stayed with bipolar technology, delaying adoption of MOS. Although much faster, bipolar technology did not scale like MOS, necessitating several more chips than a comparable MOS design. The Datapoint 2200 example readily illustrates this point. It would take several years before MOS technology approached bipolar in speed and performance capabilities. On the other hand early adopters of MOS realized single-chip solutions well in advance of those using bipolar designs.

Finally, motivation toward innovation, defined by the type of business/industry a firm was in, was also a factor. For example, one major reason for keeping the AL1 low-key was that it was a key component of the computer system from which Four-Phase derived sales and profits. Protecting this intellectual property for competitive reasons was far more important than seeking a technical patent. This was also true of calculator, adding machine, even programmable terminal companies who were seeking similar technical and cost advantages from LSI technology. For the most part, companies that embedded microprocessors into their systems did not seek to manufacture or market the devices separately. Even the larger computer companies like RCA and Burroughs that manufactured their own chips did so only on a captive basis. The relatively-

young IC makers, on the other hand, made and sold chips. Competitive forces at the chip level played a much stronger role than at the end-device level. Chip makers like Intel, TI, Fairchild, Motorola and others were in an intense innovation race to develop new IC products and processes. The incentives to innovate, patent, and publish IC advances were significantly greater for these firms than for those who were effectively customers of these firms.

Role of user in innovation

The all-important role of the user—both external and internal—in innovation is demonstrated repeatedly, from calculators to programmable terminals to industrial controllers. Every IC maker is beholden to some customer that brought not simply a problem to be solved, but often a solution to be implemented or at least modified in the process of developing a solution. The rapid evolution of electronic calculators from large desktop (sometimes inclusive of the desk) machines to increasingly portable designs until pocket (and eventually wallet) dimensions were achieved demonstrates the symbiotic relationship established between chip suppliers and calculator manufacturers. This was not the case as much in the more arms-length supply relationships between computer manufacturers and chipmakers. Calculator applications were ideal for MOS applications where high density and low power consumption were key drivers, while low-speed was not a factor. In fact, this application helped to foster CMOS development which had languished after early U.S. Government research contracts expired. As integration reached the level of a 'calculator-on-a-chip', many MOS IC makers integrated forward into the calculator (user) market. Note that a 'calculator-on-a-chip' became a standard product only after doing it for others (e.g., TI, Rockwell, National, even Intel's 4004).

Regarding the general-purpose microprocessor, this would take Intel three attempts to achieve. Despite Intel's intentions of making standard parts in volume, initially all work was custom. Both the 4004 and 8008 came about this way. Intel helped build user interest and demand for these products with the MCS-4 and MCS-8 kits and associated development systems. Users contributed willingly to improving Intel's first two microprocessors which

culminated in the 8080, their first true off-the-shelf part. Along the way, the hobbyist sector and others helped evolve standards for the microprocessor.

More needs to be said about the crucial role of custom chips to the growth of ICs and to MOS technology in particular. Wilson, Ashton, and Egan (1980) have referred to the 1964 to 1974 era as "the era of custom LSI" in the sense that many firms believed that custom LSI products would constitute the largest portion of the next generation of digital integrated-circuit sales dollars.[151] This projection would not come to pass, but firms like AMI did realize early success in custom ICs. Even in Intel's case, the standard device in volume strategy was only possible after repeated custom work. Bassett (1998) likened Intel's approach as one to "use custom to create standard," referencing Noyce (1970):

> Intel is actively soliciting business. We're doing this because we want to learn by working very closely with customers what they need to do their job. Hopefully by working with several customers in the same area, we can find the commonality that everybody seems to need, and then we can build that as a standard part. And once it exists as a standard part, the cheapest way for a guy to go will be to use it, because he will have all the advantages of a production-line flow that is already established.[152]

Braun & Macdonald (1982) note that the microprocessor (along with semiconductor memory) represented a mass market opportunity that broke from the preceding custom chip tradition that had emerged with MOS LSI technology:

> Before the days of the microprocessor, a fundamental problem was that the more integrated the chip, the more specialised its function. It was unlikely to find a mass market and such a market was absolutely essential for the batch production methods and long runs which seemed to be the only economic way of manufacturing such integrated circuits… MOS was the cheapest form of integrated circuitry and LSI the most exhaustive exploitation of that form.[153]

Cumulative Synthesis

Referring back to Usher's theory of cumulation, the invention of the microprocessor involved the cumulative synthesis of many skills and capabilities, some new but most existing. Closer

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[151] Wilson, Ashton, and Egan, op. cit., 89.
[152] Basset, op. cit., 471-2; Noyce quoted in Elizabeth de Atley, "Can You Build a System with Off-the-Shelf LSI?" *Electronic Design*, 1 March 1970, 50.
[153] Braun & Macdonald, op. cit., 104.

examination of the Intel case reveals that Intel's greatest asset at the time was its chip fabrication process. Regis McKenna has said, "Intel wasn't exactly the greatest architectural design firm in the world, they were much more a process company."[154] Hoff underscores, stating "we figured our process was probably good for maybe twice the transistor count of any other MOS process around and, of course, the MOS process had about a four-to-one advantage on logic density."[155] Intel was an early adopter of silicon-gate technology—actually "borrowed" from Fairchild—that enabled them to make these chips much more reliably than others at the time. The TI 8008 chip (for which they received the first patent) employed conventional metal-gate technology that was not as well-suited for the increased level of integration. The result was a much bigger chip that did not operate reliably (and was never commercially produced).

The more recent accounts describe Faggin's role in the 4004 *innovation* (in the true sense of the word) as arguably the most important as his process (chip-making) knowledge coupled with his dogged-persistence made the idea a commercial reality. With this capability it is easier to understand Intel's success in producing successive chips such as the 8008, 8080 and others. Hoff's computer design knowledge (influenced by the PDP-8) allowed him to conceptualize the problem differently than the customer (Busicom) had envisioned as a calculator design (several individual chips for separate functions like adder, printer, screen, etc). Mazor's previous experience with IBM and DEC mainframe designs also was a factor. Finally was the active role of the user (see earlier discussion) by Shima in specifying in great detail the layout and later living with the project to assure its completion. Bringing a design/template enabled Intel with scant design resources to skip the traditional "research" phase (of which Intel initially ignored) and critique and adapt a specification to make it operational.

Datapoint's specification that became the 8008 followed a similar path, however since it was also a young organization it only committed a young engineer to interface via phone.

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[154] McKenna interview with Walker, op. cit.
[155] Hoff interview with Walker, op. cit.

Software/firmware contribution as evidenced by the almost-literal use (95% in Mazor's estimation) of the Datapoint 2200 ISA (and thus the 8008, 8080, and x86) is probably the most lasting artifact of the invention as design and process innovations have advanced well beyond initial ones. Again, the role of the user in specifying the requirement enabled a much quicker development cycle.

Summary and Conclusions

If this analysis tells us anything it is that the microprocessor was not simply invented in isolation lab by a lone, heroic individual at Intel or anywhere else. It could even be argued that the microprocessor was *not* a deliberate outcome before its creation—an end in itself; like most things it just sort of happened. In retrospect it has truly created a revolution in technical, economic, and societal change. But these are consequences; they tell us little to nothing about the invention and the innovation process. This chapter has attempted to describe that it was a combination of many factors that helped bring about the microprocessor. Of all the factors the most important is perhaps the inventors themselves, of which their contributions may be long forgotten. Unfortunately, most of the firms that played key roles in this story including Busicom, Datapoint, Four-Phase Systems, Mostek, and American Microsystems were effectively all gone by the mid-1980s. By that time the IBM PC architecture, thus the Intel microprocessor, was well on its way to capturing the lion's share of the microprocessor market, again another (considerable) consequence.

In conclusion, since the microprocessor is a complex product that is better described as a system that comprises a network of skills and capabilities, it is difficult if not impossible to assign sole responsibility for its discovery. If the embodiment of the microprocessor invention is outcomes-oriented—in other words “making it” successfully—then Intel has a reasonable claim. A more apt claim is that Intel deserves acknowledgement for the *innovation* of the microprocessor since they successfully envisioned and marketed the product as a separate part. Many have attributed marketing skill as another competitive asset of Intel's. However, if embodiment of an

invention captures important inputs (in this case design, instruction set architecture, application, and all the accumulated process knowledge that had come before), then Intel's (or anyone's) individual claim is clearly not so strong. In the end this invention was very much a collective endeavor.

CHAPTER 8: Moore's Law: Basis for Industrial Cadence[1]

"When discussing the roadmaps of [the] semiconductor industry, it is almost unavoidable to refer to the famous Moore's Law."

- L. Baldi[2]

"The Roadmap is just Moore's Law, heavily decorated."

- Sonny Maynard[3]

"We don't adhere to Moore's Law for the hell of it. It's a fundamental expectation that everybody at Intel buys into… We simply don't accept the growing complexity of the challenge as an excuse not to keep it going."

- Craig Barrett[4]

"Moore's Law is more of an economic imperative than anything else."

- Robert Akins[5]

"You don't know if Moore's Law is driving the industry or the industry is driving Moore's Law."

- Hwa-Nien Yu[6]

"Moore's Law is not a law; it is an act of will."

- Chris Mack[7]

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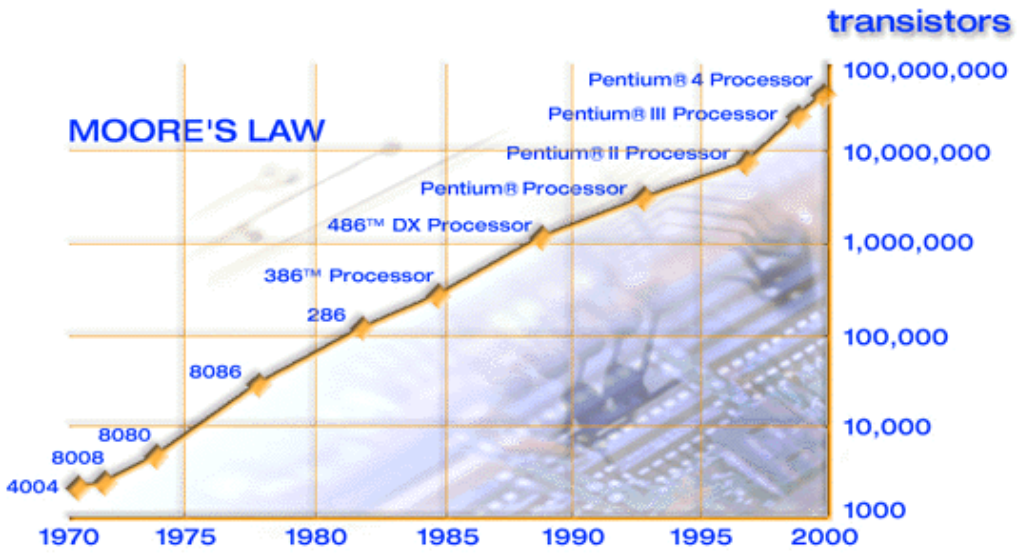
[1] This chapter draws from Robert R. Schaller, "The Origin, Nature, and Implications of 'Moore's Law': The Benchmark of Progress in Semiconductor Electronics," manuscript, September 26, 1996, which was published in abbreviated form in Robert R. Schaller, "Moore's Law: Past, Present, and Future," *IEEE Spectrum*, June 1997, 52-59.
[2] L. Baldi, "Industry Roadmaps: The Challenge of Complexity," *Microelectronics Engineering*, Vol. 34, No. 1, December 1996, 9-26.
[3] E.D. "Sonny" Maynard, personal interview, August 1, 2000.
[4] Craig Barrett, quoted in Brent Schlender, "Intel's $10 billion gamble," *Fortune*, November 11, 2002.
[5] Robert Akins, quoted in Josh McHugh, "Laser Dudes," *Forbes*, February 24, 1997, http://www.forbes.com/forbes/97/0224/5904154a.htm Akins is cofounder and CEO of Cymer Inc.
[6] Hwa-Nien Yu, personal interview, July 18, 2000.
[7] Chris A. Mack, "Using Learning Curve Theory To Redefine Moore's Law," *Solid State Technology*, July 2003, 58.



Microprocessor	Year of Introduction	Transistor Count
4004	1971	2,250
8008	1972	2,500
8080	1974	5,000
8086	1978	29,000
286	1982	120,000
386™ processor	1985	275,000
486™ DX processor	1989	1,180,000
Pentium® processor	1993	3,100,000
Pentium II processor	1997	7,500,000
Pentium III processor	1999	24,000,000
Pentium 4 processor	2000	42,000,000

Figure 8-1. Intel Microprocessors and Moore's Law

Source: Intel http://www.intel.com/research/silicon/mooreslaw.htm

"Moore's Law, the doubling of transistors every couple of years, has been maintained, and still holds true today." states the Intel website. Moore's Law is referred to often throughout this thesis. As the first quote that opens this chapter suggests, it is difficult if not impossible to discuss semiconductor roadmaps without referring to Moore's Law. Indeed, Moore's Law serves as a

basic planning assumption for the ITRS. Many see the Roadmap's purpose as sustaining Moore's Law. Since Gordon Moore's observation some four decades ago that the number of components per IC had and would continue to increase on a regular, exponential rate,[8] this idea has become so ingrained within the semiconductor industry that it is commonly referred to as a self-fulfilling prophecy. Steve Schulz of Texas Instruments expands on this by using the phrase, "Moore's suggestion":

> This industry has followed the density curve of Gordon Moore for so long that it has gone beyond mere conventional wisdom: it has become gospel, a sort of self-fulfilling prophecy. For years, I have referred to "Moore's Law" as "Moore's Suggestion," because our ability to sustain that rate depends upon the power of suggestion, not upon any fundamental laws. We invest at that rate necessary to fulfill our prophecy, because we believe the investment will always provide much greater returns. The laws of physics, however, are even more compelling. As investment costs rise, it's left to design to find better ways to use these investments to increase value, and thus revenue. The rising costs of high-tech fabs are quickly becoming a rich man's game, and only the companies that truly understand the increasingly critical role of design will be able to effectively compete in the coming era.[9]

Over time the definition of Moore's Law has undergone change as will be discussed. Nonetheless, the implications in industry investment in research, development, manufacturing, and the overall innovation enterprise are unmistakable. The consequences of not complying with Moore's Law can be disastrous. Thus, a noticeable innovation rhythm or cadence characterizes the semiconductor industry. Product life cycles must necessarily follow this rhythm. More importantly, all the required supporting materials and technologies must be available in accordance with this rhythm. One of the crucial goals of the ITRS is to help align activities across the various technology areas so that the stated Roadmap targets may be met. As discussed in Chapter 4 this is referred to as *organized innovation*.

Organization of the Chapter

This chapter is taken in large part from a background paper prepared by the author for a

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[8] Gordon E. Moore, "Cramming more components onto integrated circuits," *Electronics*, Vol. 38, No. 8, April 19, 1965, 115.

[9] "Moore's Observation" is courtesy of Steve Schulz, personal interview September 1, 1999 and Steve Schulz, "New ITRS Roadmap Portends Massive Design Changes Ahead," *ISD Magazine*, December 1999. Note that Schulz served as co-chair of the Design TWG for the 1999 ITRS.

public policy course in early 1996, from which an abbreviated version appeared in *IEEE Spectrum* in 1997. While much has changed over the ensuing time, the original article still remains a useful primer for Moore's Law. Thus it is included here without revision except where appropriate redundancies are removed if they appear elsewhere in the thesis.[10] Appendix C provides a detailed retrospective to the base article that serves three purposes, to: 1) correct, amend, and briefly reflect on the original article, 2) discuss important changes in context between the mid 1990s when the original article was prepared and the present period (2003-4), and 3) summarize other interpretations of Moore's Law as they pertain to industrial cadence and the ITRS. Finally, this chapter ends with a brief set of questions and prospective comments for future consideration.

Robert R. Schaller, "The Origin, Nature, and Implications of 'Moore's Law': The Benchmark of Progress in Semiconductor Electronics," paper prepared for PUBP 801 Macro Policy, Spring 1996, for Professor Roger Stough, September 26, 1996.

Introduction

This paper attempts to more completely explain "Moore's Law," a phenomenon unique to the rapid innovation cycles of semiconductor technology and thus the semiconductor industry as a whole. Gordon E. Moore's simple observation almost four decades ago that circuit densities of semiconductors had and would continue to double on a regular basis has not only been validated, but has since been dubbed, "Moore's Law" and now carries with it enormous influence. It is increasingly referred to as a controlling variable—some have referred to it as a "self-fulfilling prophecy." The historical regularity and predictability of "Moore's Law" produce organizing and coordinating effects throughout the semiconductor industry that not only set the pace of innovation, but define the rules and very nature of competition. And since semiconductors increasingly comprise a larger portion of electronics components and systems, either used directly by consumers or incorporated into end-use items purchased by consumers, the impact of

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[10] In some cases whole sections have been moved to other chapters. Some original references are no longer complete (i.e., primarily page numbers) as a few sources are no longer in the author's possession.

"Moore's Law" has led users and consumers to come to expect a continuous stream of faster, better, and cheaper high-technology products. The strategy and policy implications of "Moore's Law" are significant as evidenced by its use as the baseline assumption in the industry's Roadmap for the next decade and a half.

The historical background that led up to Gordon Moore's 1965 observation can be found in Chapter 6. Specifically, the 15-year period spanning from the late 1940s when the transistor was discovered until the early 1960s when the integrated circuit was successfully commercialized provided the backdrop for Moore's insight. Perhaps the most important breakthrough that is pertinent to Moore's Law is better described as a series of incremental process innovations in the manufacturing of semiconductor devices. Work at Bell Labs and General Electric produced most of these innovations. Bell Labs' sharing of these methods in formal symposia made possible rapid process technology diffusion throughout the industry. The two most noteworthy innovations are the diffusion and oxide masking process, and the *planar* process, both becoming the permanent basis for production since. The diffusion process allowed the producer to diffuse impurities (dopants) directly into the semiconductor surface, eliminating the tedious practice of adding conducting and insulating material layers on top of the substrate. The addition of sophisticated photographic techniques permitted the laying of intricate mask patterns on the semiconductor so that diffusion took place only in designated areas. This greatly increased the accuracy of production while improving the reliability of devices. With diffusion, production moved from a craft process of individual assembly to batch processing.

The planar process was a logical outgrowth of the diffusion and oxide masking process. Planarization was the creation of physicist Jean Hoerni of newly-formed Fairchild Semiconductor. Hoerni observed the production limitations of conventional 3-dimensional transistor designs (e.g., the "mesa" transistor[11]). Hoerni reasoned that a design based on a "plain" would be superior.

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[11] The device was called a mesa because its shape resembled a table-topped mountain in cross-section. Electrical contacts were made to the raised structures--the 'mesas' of the transistor.

Thus, the planar transistor, as the name implies, was flat. Flattening the mesa enabled electrical connections to be made, not laboriously by hand, but by depositing an evaporated metal film on appropriate portions of the semiconductor wafer. Using a lithographic process of a series of etched and plated regions on a thin, flat surface or wafer of silicon, the "chip" was born out of the planar transistor. Like the printing process itself, the planar process allowed for significantly greater rates of production output at even higher yields.

More importantly, the planar process enabled the *integration* of circuits on a single substrate since electrical connections between circuits could be accomplished internal to the chip. Robert Noyce of Fairchild quickly recognized this as recounted by Gordon Moore in an opening quote in Chapter 6. Fairchild introduced the first planar transistor in 1959 and the first planar IC in 1961. Moore views the 1959 innovation of the planar transistor as the origin of "Moore's Law." Perhaps more than any other single process innovation, planarization set the industry on its historical exponential pace of progress as Gilder (1989) notes:

> Known as the planar integrated circuit, Fairchild's concept comprised the essential device and process that dominates the industry today... Ultimately it moved the industry deep into the microcosm, and put America on the moon.[12]

With time and experience, *ad hoc* production methods were replaced with more formalized technology-based processes. To underscore the importance of process innovations, Braun and Macdonald (1982) state that much of the early growth in semiconductor electronics "was not only permitted by new processes, but actually precipitated by them, for batch production in general, and planar in particular, prompted both a rapid increase in the numbers of components produced and an even more rapid decline in their price."[13]

Amazingly, the industry has not veered from this course since then. With time, chip manufacturers improved the lithographic process with more precise photographic methods and *photo*lithography thus became the standardized production method for the industry. More

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[12] George Gilder, *Microcosm: The Quantum Revolution in Economics and Technology*, New York: Simon and Schuster, 1989, 77.
[13] Braun & Macdonald, op. cit. 75-76.

pertinent to "Moore's Law," photolithography enabled manufacturers to continue to reduce feature sizes of devices. Commenting on the significance of photolithography within the planar process Malone states, "Thus were planted the seeds of Moore's Law, the very principle that governs the information age." The research focus of the 1950s, moving from laboratory to the production floor, gradually shifted its emphasis from understanding why to learning how. Creating and mastering the art of photolithography is an excellent example of this transition from science to technology.

> "The use of photolithography is yet another example of interdependence of technologies and cross-fertilisation. The method had been developed for printing purposes and had been in use in this area for some time. It is but one outstanding example of the adoption and adaptation of extraneous technologies to improve the manufacture and design of electronic devices." (Braun and Macdonald 1982)

A New Industry from a New Technology

The secondary literature on the development of the semiconductor industry—including the phenomenon called "Silicon Valley"—is extensive and need not be reviewed here. One common theme worth noting is that this industry is qualitatively different as characterized by its base technology which seems to provide a limitless source of performance advancement. From the beginning this was recognized primarily by new firms, not existing electronics device firms as discussed in Chapter 6.

Theodore Levitt's "Marketing Myopia" (1960) noted that the once-dominant railroad industry had completely missed the opportunities brought about by technological advances in other modes of transportation. The railroad industry's narrow definition of its market as the "railroad" business, as opposed to the broader "transportation" business excluded its participation in whole new automobile, truck, and airplane/airline industries. A similar parallel can be drawn regarding the creation of the semiconductor industry—none of the major semiconductor players today bears the name of dominant electronics firms of the 1950s (e.g., General Electric, RCA, Raytheon, Sylvania, Philco-Ford, and Westinghouse). These firms, all heavily engaged in the production of vacuum tubes, did make substantial early investments in semiconductor electronics. But the semiconductor industry that emerged by 1960 is represented by a whole new breed of firms,

some from other seemingly unrelated industries, some entirely new. Texas Instruments, Shockley Laboratories, and Fairchild Semiconductor are three of the many new firms that had emerged. Each had a traceable connection to Bell Labs.

Texas Instruments, a geophysical company that provided oil well services, was one of the first to purchase a license from AT&T and begin semiconductor design and manufacturing operations. Texas Instruments' Gordon Teal, a former Bell Labs researcher, successfully produced the first silicon transistor that would prove significantly easier to manufacture while possessing much improved operating characteristics over the germanium transistor in use at the time. Robert Shockley, also formerly of Bell Labs and Nobel laureate for the co-discovery of the transistor, established Shockley Transistor Laboratories, gathering together some of the best minds at the time, including a young engineer named Gordon Moore. Within a few years, Moore and others at Shockley Labs convinced Fairchild Camera and Instrument, an aerial survey company, to finance a new enterprise, so they left Shockley and formed Fairchild Semiconductor. Moore would head up the research department at Fairchild, where he would later make his circuit density doubling observation. The innovative breakthrough of the IC in the late 1950s as previously discussed actually involved both firms. Jack Kilby at Texas Instruments produced the first germanium IC while Robert Noyce at Fairchild quickly made the concept technically and economically feasible—thus commercially viable—by developing the planar process.[14] Moore recalls the significance of the planar process at Fairchild, "In the planar structure, Fairchild struck a rich vein of technology." (Moore 1996)

Fairchild Semiconductor

The story of Fairchild Semiconductor is a fascinating one and is illustrative of the dynamic nature of this industry, especially in its early days. Fairchild is the subject of much industry lore. The young founders (including Moore), seeking to make good on commercial success in

[14] Although Kilby's discovery preceded Noyce's by six months, both were later awarded the patent for the invention of the IC.

semiconductor production, left Shockley Laboratories in 1957 calling themselves the "Fairchild Eight"[15] and founded Fairchild Semiconductor. Fairchild is thought to have spawned no fewer than 150 companies, including Moore's and Noyce's Intel in 1968. These spin-offs have come to be referred to as "Fairchildren." It was at Fairchild that Gordon Moore, Director of Research, made his profound density-doubling observation and extrapolation.

Gordon Moore's Observation

The April 19, 1965 *Electronics* magazine was the 35th anniversary issue of the publication. Located obscurely between an article on the future of consumer electronics by an executive at Motorola, and one on advances in space technologies by a NASA official is a less than four page (with graphics) article entitled, "Cramming more components onto integrated circuits," by Gordon E. Moore, Director, Research and Development Laboratories, Fairchild Semiconductor. Moore had been asked by *Electronics* to predict what was going to happen in the semiconductor components industry over the next 10 years—to 1975. He speculated that by 1975 it was possible to squeeze as many as 65,000 components on a single silicon chip occupying an area of only about one-quarter square inch. His reasoning was a log-linear relationship between device complexity (higher circuit density at minimum cost) and time:

> "The complexity for minimum component costs has increased at a rate of roughly a factor of two per year. Certainly over the short term this rate can be expected to continue, if not to increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will remain nearly constant for at least 10 years." (Moore 1965)

This was an empirical assertion, although surprisingly it was based on only three data points.[16]

Ten years later, Moore delivered a paper at the 1975 IEEE International Electron Devices

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[15] William Shockley labeled them the "Traitorous Eight."

[16] Gordon E. Moore, personal interview, June 13, 1996. Moore views the first planar transistor in 1959 as the origin to this phenomenon. The planar IC had only been in commercial production since 1961. By 1964 he had data on the first few ICs, the latest containing 32 components (25). He was also aware that the next IC still in the lab to be introduced later in 1965 would contain about twice that many components (26). So looking out 10 years meant another thousand-fold increase to 216 components, so he literally drew a line with a straight-edge on log paper to form his prediction.

Meeting in which he reexamined the annual rate of density-doubling. Amazingly the plot had held through a scatter of different complex bipolar and MOS device types (see Product and Technology Overview) introduced over the 1969-1974 period. A new device to be introduced in 1975, a 16K charge-coupled-device (CCD) memory, indeed contained almost 65,000 components.[17] In this paper, Moore also offered his analysis of the major contributions or causes of the exponential behavior. He cited three reasons. First, die sizes were increasing at an exponential rate—chip dice were getting bigger. As defect densities decreased, chip manufacturers could work with larger areas without sacrificing reductions in yields. Many process changes contributed to this, not the least of which was moving to optical projection rather than contact printing of the patterns on the wafers.

The second reason was a simultaneous evolution to finer minimum dimensions (i.e., feature sizes or line widths). This variable also approximated an exponential rate. Combining the contributions of larger die sizes and finer dimensions clearly helped explain increased chip complexity, but when plotted against the original plot by Moore, roughly one-third of the exponential remained unexplained.

Moore attributed the remaining third to what he calls "circuit and device cleverness."[18] He notes that several features had been added. Newer approaches for device isolation, for example, had squeezed out much of the unused area. The advent of metal oxide semiconductor (MOS) technology in the late 1960s and early 1970s had allowed even tighter packing of components per chip. Interestingly, he also concluded that the end of "cleverness" had arrived with the CCD memory device:

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[17] Moore became President and CEO of Intel in 1975. Presumably all of the more recent data points used were Intel devices (founded in 1968), just as his original "3 points" paper had contained only Fairchild devices.

[18] Gordon E. Moore. 1995. "Lithography and the Future of Moore's Law," also personal interview, June 13, 1996.

> "There is no room left to squeeze anything out by being clever. Going forward from here we have to depend on the two size factors - bigger dice and finer dimensions."[19]

So Moore revised upward his annual rate of circuit density-doubling. Every eighteen months seemed to be a reasonable rate and was supported by his analysis. He redrew the plot from 1975 forward with a less steep slope reflecting a slowdown in the rate, but still behaving in a log-linear fashion. Shortly thereafter someone (not Moore) dubbed this curve, "Moore's Law." Officially, Moore's Law states that circuit density or capacity of semiconductors doubles every eighteen months or quadruples every three years. It even appears in mathematical form:

$$(\text{Circuits per chip}) = 2^{(\text{year}-1975)/1.5}$$

In 1995 Moore compared the actual performance of two device categories (DRAMs and microprocessors) against his revised projection of 1975. Amazingly, both device types tracked the slope of the exponential curve fairly closely, with DRAMs consistently achieving higher densities than microprocessors over the 25 year period since the early 1970s. Die sizes had continued to increase while line widths had continued to decrease at exponential rates consistent with his 1975 analysis.

Moore's early prediction was based on the shared observations by many in the fledgling semiconductor industry.[20] The invention of the transistor had started a miniaturization trajectory in semiconductors which had produced the integrated circuit in the late 1950s, soon followed by medium scale integration (MSI) of the mid 1960s, then large scale integration (LSI) of the early 1970s, very large scale integration (VLSI) of the 1980s, and ULSI (ultra) of the 1990s. Today's Intel Pentium microprocessor contains more than three million transistors, the Motorola PowerPC microprocessor contains almost seven million transistors, and Digital's 64-bit Alpha microprocessor contains almost 10 million transistors on a thin wafer "chip" barely the size of a fingernail. In early 1996 IBM claimed that a *gigabit* (billion bits) memory chip was actively under development and would be commercially available within a few years. Papers presented at a

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[19] Ibid.
[20] Erich Bloch, personal interview, March 1996.

1995 IEEE International Solid-State Circuits Conference contend that *terachips* (capable of handling a trillion bits or instructions) will arrive by the end of the next decade. (Stix 1995)[21]

Implications: Technological Barometer?

The implications of Moore's Law are quite obvious and profound. It is increasingly referred to as a ruler, gauge, benchmark (see title), barometer, or some other form of definitive measurement of innovation and progress within the semiconductor industry. As one industry watcher has recently put it:

> "Moore's Law is important because it is the only stable ruler we have today, . . It's a sort of technological barometer. It very clearly tells you that if you take the information processing power you have today and multiply by two, that will be what your competition will be doing 18 months from now. And that is where you too will have to be." (Malone 1996)

Since semiconductor cost is measured in size and complexity, unit cost is directly related with size. That is, as circuit size has been reduced, so has cost. As a result, virtually all electronics used today incorporate semiconductors. These devices perform a wide range of functions in a variety of end-use products, everything from children's toys, to antilock brakes in automobiles, to satellite and weapon systems, to a variety of sophisticated computer applications. The fact that all these products (and many, many more) are now so accessible to so many users is due in large part to continually declining costs of the core microelectronics made possible by the innovation of the semiconductor.

***Perpetuum Mobile*, Self-Fulfilling Prophecy, or Both?**

Perhaps the broadest implication of Moore's Law is that it has become an almost universal guide for an entire industry that has not broken stride in exponential growth rates for almost four decades now. The repeated predictability and regularity of Moore's Law are characteristics of the

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[21] Note that the title of the article, "Toward 'Point One'," refers to the length of 0.1 microns of a transistor electrical channel or gate required for gigabit chips. A micron or micrometer (μ) is one-millionth of a meter. 'Point One' microns is about the width of a DNA coil, or a thousandth the width of a human hair (see also Figure 2).

elusive *perpetuum mobile* for this industry. Some have referred to Moore's Law as self-reinforcing or a "self-fulfilling prophecy." Moore himself recently stated:

> "More than anything, once something like this gets established, it becomes more or less a self-fulfilling prophecy. The Semiconductor Industry Association puts out a technology road map, which continues this generation [turnover] every three years. Everyone in the industry recognizes that if you don't stay on essentially that curve they will fall behind. So it sort of drives itself." (Moore 1996)

There is intuitive merit to this view. The inherent characteristics of the technology contribute significantly to this "drives itself" tendency. Chip makers have long recognized the combined benefits of miniaturization. As Moore summarizes:

> "By making things smaller, everything gets better simultaneously. There is little need for tradeoffs. The speed of our products goes up, the power consumption goes down, system reliability, as we put more of the system on a chip, improves by leaps and bounds, but especially the cost of doing things electronically drops as a result of the technology." (Moore 1995)

Braun and Macdonald (1982) also refer to the "self-sustaining" nature of miniaturization in semiconductors as "tradeoffs," in Moore's words, don't really enter into the equation. In economic parlance, this is the proverbial "free lunch."

From a different angle, George Gilder (1989) argues that the technology itself possesses an almost natural "microcosmic" force toward integration in smaller and smaller spaces. He refers to this as the "law of the microcosm" and suggests that users and other institutions affected by the technology understand and follow its direction:

> "Rather than pushing decisions up through the hierarchy, the power of microelectronics pulls them remorselessly down to the individual. This is the law of the microcosm... The very physics of computing dictates that complexity and interconnections—and thus computational power—be pushed down from the system into single chips … Above all, the law of the microcosm means the computer will remain chiefly a personal appliance ... Integration will be downward onto the chip, not upward from the chip."

He draws some fairly broad implications by stating that the evolution of chip-related industries "will remorselessly imitate the evolution of the chip." That is smaller, thus cheaper, yet more powerful chip capabilities will redefine entire industries away from larger, oligopolistic structures to smaller structures, more conducive to an entrepreneurial environment. He makes a convincing

case with telecommunications, referencing Peter Huber's post-AT&T break-up analysis of the "geodesic" or horizontal network that evolved within the telephone system. Huber asserts that the traditional pyramidal network model, where all switching was done in the central office, had been made obsolete by decentralized switching systems such as private branch exchanges, local area networks, and related systems. Thus it was only natural to accord an industry a more horizontal competitive landscape consistent with its redefined geodesic network structure.

Expectations Matter

Yet another dimension, involving non-technical or non-physical variables such as user expectations contribute to the dynamic of fulfilling this *law*. In this view, Moore's Law is not based on the physics and chemical properties of semiconductors and their respective production processes, but on other non-technical factors. One hypothesis is that a more complete explanation of Moore's Law has to do with the confluence and aggregation of individuals' expectations manifested in organizational and social systems which serve to self-reinforce the fulfillment of Moore's prediction.

A brief examination of the interplay among only three components of the personal computer (PC) (i.e., microprocessor chip, semiconductor memory, and system software) helps reveal this point. A very common scenario using the IBM-compatible PC equipped with an Intel microprocessor and running Microsoft's Windows software goes something like this. As the Intel microprocessor has evolved from the 8086/88 chip in 1979 to the 286 in 1982, to the 386 in 1985, to the 486 in 1989, to the Pentium in 1993, and the Pentium Pro in 1995, each incremental product has been markedly faster, more powerful, and less costly as a direct result of Moore's Law. At the same time, dynamic random access memory (DRAM) and derivative forms of semiconductor memory have followed a more regular Moore's Law pattern to the present where a new PC comes standard with 8Meg (million bits) to 16Meg of memory as compared to the 480K (thousand bits) standard of a decade ago. Both of these cases reflect the physical or technical aspects of Moore's Law.

However, system software, the third piece of this puzzle, begins to reveal the non-technical dimension of Moore's Law. In the early days of computing when internal memory was costly and scarce,[22] system software practices had to fit this limitation—limited memory meant efficient use of it or "tight" code. With the advent of semiconductor memory—especially with metal oxide semiconductor (MOS) technology—internal memory now obeyed Moore's Law and average PC memory sizes grew at an exponential rate. Thus, system software was no longer constrained to "tight spaces" and the proliferation of thousands, then many thousands, and now millions of "lines of code" have become the norm for complex system software.

Nathan Myhrvold, Director of Microsoft's Advanced Technology Group, conducted a study of a variety of Microsoft products by counting the lines of code for successive releases of the same software package. (Brand 1995) *Basic* had 4,000 lines of code in 1975. Twenty years later it had roughly half a million. Microsoft *Word* consisted of 27,000 lines of code in the first version in 1982. Over the past 20 years it has grown to about 2 million. Myhrvold draws a parallel with Moore's Law:

> "So we have increased the size and complexity of software even faster than Moore's Law. In fact, this is why there is a market for faster processors—software people have always consumed new capability as fast or faster than the chip people could make it available."

As the marginal cost of additional semiconductor processing power and memory literally approaches zero, system software has exponentially evolved to a much larger part of the "system." More complex software requires yet even more memory and more processing capacity, and presumably software designers and programmers have come to expect that this will indeed be the case. Within this scenario a kind of reinforcement multiplier effect is at work.

A "Slipstream" to Software Development?

This network reinforcement multiplier effect is most noticeable in computers and related products. This point is further emphasized since computers represent the single largest user category of

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[22] Bulky magnetic ferrite core memories were primarily used prior to semiconductor memories.

semiconductor devices at 60% of the entire industry demand, primarily for microprocessors and DRAMs. A very distant second is telephones at 10%. After that, nothing else comes close. (Hutcheson and Hutcheson 1996, Economist 1996) Arguably in computer software—as in semiconductors—complexity has also been rising exponentially. As just discussed, though, the rate of increased software complexity appears to be outpacing that of the chips that comprise the hardware that drives the software. One noted software programmer has propounded two new Parkinson's Laws for software: "Software expands to fill the available memory," and "Software is getting slower more rapidly than hardware is getting faster." (Gilder 1995)[23] Indeed, newer programs seem to run more slowly on most systems than their previous releases (e.g., compare WordPerfect 6.0 for Windows with WordPerfect 5.1 for DOS). Microsoft, especially with its Windows development and emergent "Wintel" (Windows-Intel) *de facto* standard, owes much of its success to shrewdly exploiting the advances of microcosmic hardware. (Gilder 1995, 1989)

> "[Bill] Gates travels in the slipstream behind Moore's Law, following a key rule of the microcosm: Waste transistors... 'Every time Andy [Grove] makes a faster chip, Bill uses all of it.' Wasting transistors is the law of thrift in the microcosm, and Gates has been its most brilliant and resourceful exponent." (Gilder 1995)

When asked recently about his view of "Wintel," Moore, Chairman of the Board at Intel, quips, "Our legal department doesn't like it at all."[24] He then expands on the strategic importance of the hardware/software technological alliance, but also acknowledges the independence of architectures made possible by an ever-changing industry.

> "We certainly will try to keep it [Wintel] going that way. We have a tremendous asset in all the compatible software that's out there, so any new processor we introduce has to be able to run that stuff and as long as we keep a very large fraction of the processors, I think Microsoft will be sure that they write things that run well on our processors. And, we both have ideas of being somewhat independent. We're happy to have Java applications, and then Netscape, UNIX and everything else, and also Microsoft ports NT to [Digital's] Alpha, but in fact there is a tremendous advantage to the volume centers business."[25]

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[23] Parkinson's Law states: "Work expands so as to fill the time available for its completion." (Parkinson 1957). The second statement is also referred to as "Wirth's Law."
[24] Gordon E. Moore, personal interview, June 13, 1996.
[25] Ibid. "Volume centers" refers to large scale production of popular microprocessor or DRAM chips such as the Intel Pentium, as opposed to smaller volume or special application chips such as Digital's 64-bit Alpha chip.

It is clear that a type of lock-in (Arthur 1994) has occurred with respect to PC system hardware and software architecture. The history of this particular alliance beginning with IBM's early selection of both Intel and Microsoft as critical component suppliers (microprocessor and operating system, respectively) of their revolutionary PC has ultimately contributed to a decade and a half of mutual learning by the two firms, ironically now without IBM. Had the choice been different, who knows what system architecture would have evolved? What's important is that one has, involving—and producing—two of the most important players in the PC industry today in Intel and Microsoft. And there is no doubt that this alliance affects development and innovation cycles of both firms, thus the industry at large. Whether Moore's Law is the slipstream to software development as George Gilder asserts, or the other way around, may be a kind of "chicken and egg" question. There is little doubt that a significant expectations feedback loop involving Moore's Law is at play. This feedback mechanism is illustrated in Figure 8-2.

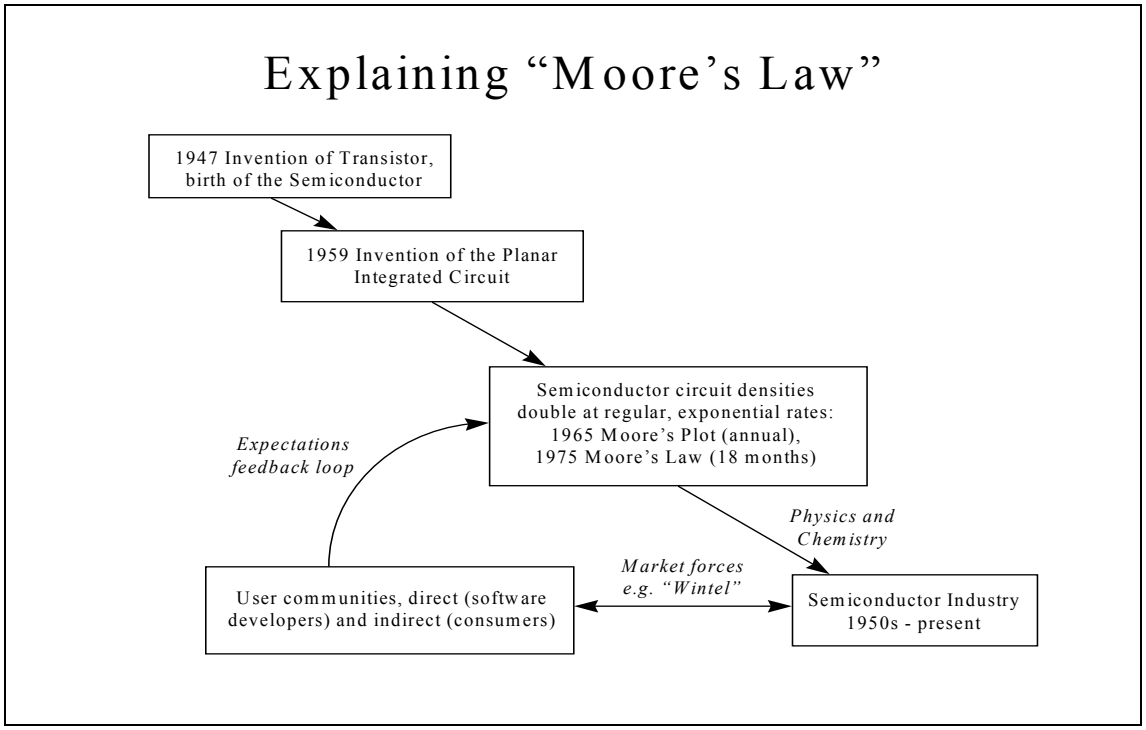

Figure 8-2. Explaining "Moore's Law"

Scaling from J-Shaped to S-Shaped Curves

As stated earlier, the exponential pace of innovation was generally understood within the semiconductor community by the mid 1960s. Erich Bloch credits Gordon Moore as being "the most articulate"[26] of the early group of technologists in communicating this phenomenon. Carver Mead, noted computer scientist at Caltech, did a series of early calculations to determine the precise scaling effects of the technology. This work intensified with the introduction of MOS technology in the late 1960s and by 1972 the first comprehensive scaling analysis was published.[27] Mead's analysis confirmed that Moore's extrapolation was not only possible, but probable, and added academic credence to the assertion. In a more recent study, Mead (1994) reexamined his earlier scaling estimates and then looked ahead:

> "Over the ensuing 22 years, feature sizes have evolved from 6 to 0.6μ, and the trend shows no sign of abating... I shall conclude that we can safely count on at least one more order of magnitude of scaling, with a concomitant increase in both density and performance."

This form of analysis is consistent with technology development along exponential "J-shaped" or "S-shaped" curves. (Rothschild 1990, Foster 1986, and Klein 1984, 1977) In the field of economics, particularly its evolutionary strain in the field of *Complexity Science*, this phenomenon is known as increasing returns. (Arthur 1994, Waldrop 1992) Whatever label is applied, there is little question that there is still considerable "learning" occurring in exploiting the potential physical properties of semiconductors along with the associated production processes. At some point this technology—like all technologies—will reach its limit of exponential growth and begin to experience diminishing marginal returns (at the top hump of the "S"). See Chapter 4 for a detailed discussion of S-curves.

So When Will Moore's Law End? Is This The Right Question?

A 1995 article in the *Economist* is titled, "The End of the Line" and discusses the impending fate

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[26] Erich Bloch, personal interview, March 25, 1996.
[27] B. Hoeneisen, and C.A. Mead. 1972. "Fundamental Limitations in Microelectronics I: MOS Technology," Solid-State Electronics Vol. 15, pp. 819-829.

of Moore's Law. A similar *Forbes* article is titled, "Whither Moore's Law?" while a recent editorial's headline in a Unix Users Group's Internet home page (CUUG 1996) reads, "The End of Moore's Law: Thank God!" Numerous other forecasts have come to similar conclusions. But as discussed earlier, Moore's Law started out as a simple observation and extrapolation. Actual performance and experience have validated Moore's original plot, proving him quite prophetic. An intriguing point about Moore's Law is that throughout its existence, forecasts of its demise have consistently been wrong. For example, in an exhaustive study on the history and impact of the semiconductor, Braun and Macdonald (1982) came to a similar conclusion as Gordon Moore had in his original 1965 article:

> "Unlike the consequences arising from the future use of semiconductor electronics, the technical future of the technology, though still uncertain, can be forecast with a degree of confidence over the very short term. For the time being, trends of increased circuit densities will continue, although no-one expects Moore's Law to hold for very much longer."

The authors go on to say that the microprocessor would probably reach its zenith with a 32-bit[28] architecture and questioned whether the 256K DRAM would become the "ultimate single chip memor[y]." In a decade and a half since, Digital's 64-bit Alpha 21164 microprocessor chip contains almost 10 million transistors, operating at more than 300 MHZ, and the 16 Meg DRAM are now the contemporary state-of-the-art chips, with advanced designs soon to eclipse these capabilities.

In late-1994, The Semiconductor Industry Association (SIA) published the *National Technology Roadmap for Semiconductors*. The *Roadmap* is a consensus view of the industry's technical vision and forecast over the next decade and a half--through 2010. The second paragraph of the document contains the statement, "A central assumption of the Roadmap is an extension of industry history according to Moore's law." (SIA 1994)

A recent survey of some of the best thinkers in the high-tech industry revealed a wide range

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[28] "32-bit" refers to the number of parallel bits of information (length of computer "word") processed at one time.

of responses to the question, "How many more years will Moore's Law play out?" including:

> "With conventional lithography, another three to five [years], max... 10 to 15 years max... At least another 20 years or more... Moore's Law has worked in the past 25 years or so. There's no doubt that it will continue... We'll all be dead when Moore's Law is played out." (Malone 1996)

A very revealing follow-up question, "What will stop it [Moore's Law]—design limits, manufacturing limits or fabrication costs?" has several predictable answers such as, "The fundamental physics of silicon will become a limiting factor." However, one respondent, Dan Lynch, President and CEO of CyberCash, offers a starkly different view by answering, "Moore's Law is about human ingenuity progress, not physics." (Malone 1996)

Along similar lines, Carver Mead states that Moore's Law "is really about people's belief system, it's not a law of physics, it's about human belief, and when people believe in something, they'll put energy behind it to make it come to pass."[29] Mead offers a retrospective, yet philosophical explanation of how Moore's Law has been reinforced within the semiconductor community through "living it":

> "After it's [Moore's Law] happened long enough, people begin to talk about it in retrospect, and in retrospect it's really a curve that goes through some points and so it looks like a physical law and people talk about it that way. But actually if you're living it, which I am, then it doesn't feel like a physical law. It's really a thing about human activity, it's about vision, it's about what you're allowed to believe. Because people are really limited by their beliefs, they limit themselves by what they allow themselves to believe what is possible. So here's an example where Gordon [Moore], when he made this observation early on, he really gave us permission to believe that it would keep going. And so some of us went off and did some calculations about it and said, 'Yes, it can keep going'. And that then gave other people permission to believe it could keep going. And [after believing it] for the last two or three generations, 'maybe I can believe it for a couple more, even though I can't see how to get there'. . . The wonderful thing about [Moore's Law] is that it is not a static law, it forces everyone to live in a dynamic, evolving world." (UVC 1992)

The historical literature reveals a pattern—beginning with Moore's original 1965 prediction—that the longer-term predictions (greater than 10 years) of diminishing marginal complexity increases simply have not yet come to pass. In fact, the latest set of "predictions" in 1996, although collectively more optimistic than previous samples, still peg a future longer-term limit at

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[29] Carver A. Mead, personal interview, June 15, 1996.

less than 15 years. (Malone 1996)[30] In a very recent interview, Moore himself seems to stick to the "about another decade" prediction he originally made in 1965:

> "I think much of the rate of progress can be expected to continue for at least a few more generations. Three generations of technology at three years per generation is about a decade. So I can see us staying on roughly the same curve that long." (Moore 1996)

At the same time, Moore recognizes that history has proven him and mostly everyone else wrong about past predictions. His closing remarks at a Microlithography Symposium in February 1995 challenged the participants to continue to "think smaller":

> "Semiconductor technology made its great strides as a result of ever increasing complexity of the products exploiting higher and higher density to a considerable extent the result of progress in lithography. As you leave this meeting I want to encourage each of you to think smaller. The barriers to staying on our exponential are really formidable, but I continue to be amazed that we can either design or build the products we producing today. I expect you to continue to amaze me for several years to come." (Moore 1995)

Internal and External Sources of Innovation

The transistor and its extensive lineage of semiconductor products are arguably the result of much technology push, intrinsic to the nature of these devices. Arguing against the conventional wisdom that product innovations are typically developed solely by product manufacturers, von Hippel (1986) used the title, *The Sources of Innovation* to explain that:

> ". . . the sources of innovation vary greatly. In some fields, innovation users develop most innovations. In others, suppliers of innovation-related components and materials are the typical sources. In still other fields, conventional wisdom holds and product manufacturers are indeed the typical innovators."

In an exhaustive case study of the semiconductor industry, Dosi (1984) concluded that U.S. public (military and space) policies initially performed an essential external role of selection and guidance of the directions of technical progress, but noted that this role has since decreased. Moore (1996) agrees with this view, noting that defense R&D and particularly the space program of the 1960s had a "negligible impact on the semiconductor industry."

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[30] Pp. 60-61. Note that a diverse sample of eleven industry representatives (CEOs, senior systems and software engineers, industry analysts, industry writer, venture capitalist) were interviewed. A conservative "average" of 13.9 years was derived from the stated answers to, "How many more years will Moore's Law play out?" This average excluded one unlimited ("we'll all be dead") answer.

Dosi then poses the important question, "What are the factors which shape the directions of the innovative activity when powerful external factors cease to exert their 'pulling' and 'pushing' influence?" He goes on to argue three major factors. First, 'normal' technical progress maintains a momentum of its own which defines the broad orientation of the innovative activities. He refers to this "in-built heuristic" in so many words as Moore's Law:

> "Take, for example, the fundamental trend in the industry towards increasing density of the circuits: the doubling of the number of components per chip every year (in the late 1970s every two-three years) is almost a 'natural law' of the industry. After 1K memories one progressed to 4K, 16K, 64K and further increases in integration are expected. The same applies to microprocessors, from 4 to 8, 16, 32 bit devices. This *cumulative process* has an important role in the competitive process of the industry, by continuously creating asymmetries between firms and countries in their relative technological success."[31]

The second factor stems from the mutual relationship between innovation in semiconductors and end-use applications. Technical change in semiconductors defines one of the boundary conditions of possible technical advances in 'downstream' sectors. At the same time, both technological problems and commercial opportunities in these downstream sectors focus and lead the direction of technological advances in semiconductors. As previously discussed, the interplay of the "Wintel" architecture is most evident here. Moore acknowledges this, but continues to emphasize the "pushing" force of semiconductor electronics:

> "There's still a lot of push [going on], we work it on both ends. You look at what Intel does, for example, our thrust in video conferencing. That is driven principally as an application that requires higher performance processing to support, so our business depends on continuing that model where everybody needs more computing power every year, so we're trying to drive as much push as we can."[32]

A third factor Dosi cites is the more traditional economic "market-pull" influence from changes in relative prices and distributive shares. Dosi emphasizes that market factors operate particularly with respect to 'normal' technical progress, and second, that technical progress occurs *within the boundaries* defined by the basic technological trajectory. This suggests that user feedback can be self-reinforcing within the parameters of the technological trajectory of semiconductors.

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[31] P. 68, quotes and italics in original.
[32] Gordon E. Moore, personal interview, June 13, 1996.

Finally, Hutcheson and Hutcheson (1996) offer a more critical view of the regularity typically associated with Moore's Law. They point out that underlying production limitations are becoming increasingly difficult to overcome.

> "In stark contrast to what would seem to be implied by the dependable doubling of transistor densities, the route that led to today's chips was anything but smooth. It was more like a harrowing obstacle course that repeatedly required chipmakers to overcome significant limitations in their equipment and production processes. None of these problems turned out to be the dreaded showstopper whose solution would be so costly that it would slow or even halt the pace of advances in semiconductors and, therefore, the growth of the industry. Successive roadblocks, however, have become increasingly imposing, for reasons tied to the underlying technologies of semiconductor manufacturing."

The physics underlying semiconductor manufacturing steps suggests several potential obstacles to continued technical progress and density doubling. For example, the gigabit chip generation may finally force technologists up against the limits of optical lithography. Lithographers confront the formidable task of building structures smaller than the wavelength of light (see Figure 8-3).

Scale	Diameter/width of	Wavelength of
1 meter	man	audible sound (in air)
1 centimeter	fingernail	
1 millimeter	human hair	
	"typical" cell	
1 micron (μ)	chromosome, bacterium	
0.1 μ (point one)	DNA coil, virus	visible light
	macromolecule	ultraviolet light
1 nanometer	small organic molecule	
1 Angstrom (Å)	atom	x-rays used for crystallography

Figure 8-3. Scale of Approximate Sizes[33]

"Think of it as trying to paint a line that is smaller than the width of the paintbrush," says a researcher at Bell Labs. (Stix 1995) He goes on to say that there are ways of doing it, but the cost

[33] Each step in the scale is a factor of 10.

involved may be prohibitive. Economics may constrain Moore's Law before the limits of physics. The reality is that both are closely intertwined which brings us to "Moore's Second Law."

Moore's Second Law: Economics

In 1977, Robert Noyce, then Chairman of the Board at Intel, wrote:

> "Today, with circuits containing 2^{18} (262,144) elements available, we have not yet seen any significant departure from Moore's law. Nor are there any signs that the process is slowing down, although a deviation from exponential growth is ultimately inevitable. The technology is still far from the fundamental laws of physics: further miniaturization is less likely to be limited by the laws of physics than by the laws of economics."

Almost two decades later, Noyce's foresight of economic limitations has brought about what has been referred to Moore's Second Law.[34] (Ross 1995) "What has come to worry me most recently is the increasing cost... This is another exponential," writes Moore (Economist 1995). In today's dollars, the cost of a new "fab" (fabrication plant) has risen from $14M in 1966 to $1.5B in 1995. By 1998 work will begin on the first $3B fabrication plant. Between 1984 and 1990, the cost of a fab doubled, but chip makers were able to triple the performance of a chip. In contrast, the next generation of fabs will see cost double again by 1998, but this is likely to produce only a 50% improvement in performance. The economic law of diminishing marginal returns appears to be setting in. If this exponential trend continues, by 2005 the cost of a single fab will pass the $10B mark (in 1995 dollars) or 80% of Intel's current net worth. According to Dan Hutcheson, President of VLSI Research, Moore's Law will fall victim to economics before it reaches whatever limitations exist in physics:

> "The price per transistor will bottom out sometime between 2003 and 2005. From that point on, there will be no economic point to making transistors smaller. So Moore's Law ends in seven years." (Ross 1995)

State-of-the-art fabs become obsolete in three to five years; staying ahead in such a business requires a large chip maker to spend vast sums simply to keep up with technology. In 1995 the industry spent $30B in new fab capacity; Intel's share alone was $3B. To recoup its investment, a

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[34] Like the first "Law" Moore states that he did not coin the "Second Law." He refers to the capital cost exponential observation as "Rock's Law" after Arthur Rock, who originally financed the Intel venture.

semiconductor firm will want to run the plant as near to full capacity as possible. When levels of demand change (and supply remains fixed), then wide price swings—much like in farming, another commodity business—cause supply to adjust stickily to demand. The result is an historical pattern of volatile market cycles producing mass surpluses and shortages. (Economist, 1996) These industry-unique cycles are further aggravated by normal business cycle behavior at the macroeconomic level. The U.S. industry crisis of the early-mid 1980s is a vivid reminder of this economic impact.

So what are firms to do? Hutcheson and Hutcheson (1996) suggest that firms collaborate—team up. They cite that increasingly, chip makers are sharing the costs of a new fab with customers, competitors, even countries. IBM and Toshiba are building a plant together, as are Motorola and Siemens. Also state-organized consortia appear to be on the rise in the newer participant countries in semiconductor manufacturing such as Korea and Singapore. Another point is that the role of the suppliers of materials and especially, manufacturing equipment, has become even more vital to the overall success of the industry. The next section takes a broader look at various interpretations and uses of Moore's Law, and its implications including those important to public policy.

Other Interpretations and Uses

Moore's Law is increasingly used as a metaphor or label for anticipated rates of rapid change—not only in semiconductors, but in broader contexts. The source of this change is technological, but the effects of it are economic and social. In this very complex arrangement, Moore acknowledges that Moore's Law "gives us a short-hand to talk about things."[35]

Recently, a software representative was quoted in the *New York Times* as saying, "The length of eternity is 18 months, the length of a product cycle." In some sense, Moore's Law has taken on a life of its own as it finds its way into the broader community of users and other

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[35] Ibid.

institutions impacted by the technology. To assess this impact, an Internet keyword search on "Moore's Law" was recently conducted. Out of well over 100 pertinent references, more than two dozen quality references were obtained. Most references came from direct industry application including the front-end component of the SME industry. The majority of the references were from downstream user communities including software, PC users, and network and Internet applications. It is interesting to note that Moore's Law now has many "spin-offs" such as "Metcalfe's Law."[36] Surprisingly, the fields of education and even marketing have referred to Moore's Law. The following is a sample of the wide range of uses, interpretations, and applications found. Note that processing power, not circuit density, is increasingly becoming the new basis of Moore's Law.

> "Management is not telling a researcher, 'You are the best we could find, here are the tools, please go off and find something that will let us leapfrog the competition.' Instead, the attitude is, 'Either you and your 999 colleagues double the performance of our microprocessors in the next 18 months, to keep up with the competition, or you are fired.'" (Odlyzko 1995)
>
> "'Moore's Law' may one day be as important to marketing as the Four Ps: product, price, place, and promotion... If it is borne out in the future the way it has in the past, the powerful Pentium on your desktop will seem as archaic as a 286 PC in a few years." (Koprowski 1996)
>
> "We have become addicted to speed. Gordon Moore is our pusher. Moore's law, which states that processing power will double every year and a half, has thus far held true. CPU designers, always in search of a better fix, drain every possible ounce of fat from processor cores, squeeze clock cycles, and cram components into smaller and smaller dies." (Joch 1996)
>
> "So holding 'Moore's Law' as the constant, the technology in place in classrooms today will not be anything like the classroom of five years from now!" (Wimauna Elementary School 1996)
>
> "The End of Moore's Law: Thank God!... The End of Moore's Law will mean the end to certain kinds of daydreaming about amazing possibilities for the Next Big Thing; but it will also be the end of a lot of stress, grief, and unwanted work." (CUUG 1996)
>
> "Computer-related gifts must be the only Christmas presents that follow Moore's Law." (Sydney Morning Herald 1995)
>
> "Moore's Law is why ... smart people start saving for the next computer the day after they buy the one they have... Things are changing so fast that everyone's knowledge gets

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[36] Metcalfe's Law is attributed to Robert Metcalfe, former Xerox PARC researcher, inventor of Ethernet, and founder of 3-COM. It states that the network increases in performance exponentially with the addition of each user.

> retreaded almost yearly. Thank you, Mr. Moore... [for] the internet, a creature of Moore's Law..." (Hettinga 1996)

Are There Any Good Analogues?

The examination of Moore's Law would not be complete without drawing analogues to other technologies. This has been done often for various reasons. For example, in arguing the uniqueness of the million-fold cost reductions and performance improvements in semiconductors, Gordon Moore jokingly cites that if similar progress were made in transportation technologies such as air travel, a modern day commercial aircraft would cost $500, circle the earth in 20 minutes, and only use five gallons of fuel. However, it may only be the size of a shoe box. Stephen Kline of Stanford has suggested a bit more appropriate use of the aircraft analogy, suggesting that the earlier era of rapid advances in aircraft speed and performance may offer additional insight.[37]

Carver Mead suggests that magnetic storage, specifically disk drive technology, has followed a similar scaling path as semiconductors. He cites that PC hard drives in particular have evolved from megabyte (million bytes) to gigabyte (billion bytes) capacity in roughly a decade. This thousand-fold capacity improvement approaches Moore's original extrapolation. Mead has done some scaling calculations and continues to be amazed with the phenomenon. He acknowledges, "I still don't understand that."[38]

Mead and Erich Bloch have also suggested the field of biotechnology beginning with Watson's and Crick's discovery of DNA. While there are others that could be examined, some that have been used really miss the point. Take, for example, the following Moore's Law analogy to railways recently offered by the *Economist* (1996).

> "Consider the development of America's railways as an example. In 1830, the industry boasted a mere 37 kilometers (23 miles) of track. Ten years later it had twice as much. Then twice that, and twice again—every decade for 60 years. At that rate 19th-century train buffs might have predicted that the country would have millions of kilometers of track

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[37] Stephen J. Kline, personal interview, June 13, 1996.
[38] Carver A. Mead, personal interview, June 15, 1996.

> by 1995. In fact there are fewer than 400 km. Laying rails were too expensive to justify connecting smaller towns; people simply did not need track everywhere. Exponential growth gave way to something more usual—a leveling off around a stable value at which economic pressures were balanced... Americans stopped building railways, but they did not stop becoming more mobile. As rail's S-curve tailed off, Americans took to driving cars and built roads."

Used as an analogue to describe the limitations of Moore's Law, the railroad analogy is limited in its application. Increasing railroad track area (or roads, sea routes, bandwidth, etc.) really deals with implementation or *diffusion* of technology—transportation infrastructure in this case—not technological innovation. Moore's Law is about the pace of innovation (i.e., ideas).

The next section attempts to summarize and draw together the major findings of this examination. In doing so, implications for future research are discussed.

Moore's Law Reconsidered

Beginning as a simple observation of trends in semiconductor device complexity, Moore's Law has become many things. It is an explanatory variable for the qualitative uniqueness of the semiconductor as a base technology. It is now recognized as a benchmark of progress for the entire semiconductor industry. And increasingly it is becoming a metaphor for technological progress on a broader scale. As to explaining the real causes of Moore's Law, this examination has just begun. For example, the hypothesis that semiconductor device users' expectations feed back and self-reinforce the attainment of Moore's Law (see Figure 8-1) is still far from being validated or disproved. There does appear to be support for this notion primarily in the software industry (e.g., "Wintel" *de facto* architecture). Further research, including survey research and additional interviews, is required to address this possible relationship.

What has been learned from this early investigation is the critical role that *process* innovations in general, and manufacturing equipment innovations in particular play in providing the technological capability to fabricate smaller and smaller semiconductor devices. The most notable of process innovations was the planar diffusion process in 1959—the origin of Moore's Law. Consistent with Thomas Kuhn's (1962) paradigm-shifting view of "scientific revolution,"

many have described the semiconductor era as a "microelectronics revolution." (Forester 1982, Braun and Macdonald 1982, Gilder 1989, Malone 1996, and others) Indeed, the broad applications and pervasive technological, economic, and social impacts that continue to come forth from "that astonishing microchip" (Economist 1996) seem almost endless. However, this phenomenon has also been aptly described by Bessant and Dickson (1982) as *evolutionary*, albeit at an exponential rate.

> "In a definite technical sense there has been no revolution (save, perhaps, for the invention of the transistor in 1947) but rather a steady evolution since the first invention."

Moore's Law is one measure of the pace of this "steady evolution." Its regularity is daunting. The invention of the transistor, and to a lesser degree the integrated circuit a decade later, represented significant scientific and technological breakthroughs, and are both classic examples of the Schumpeterian view of "creative destruction" effects of innovation. This is evidenced by the literal creation of an entire new semiconductor industry at the expense of the large electronics firms that dominated the preceding vacuum tube technological era. This period of transition from old technology to new technology is characterized by instability, and factors that underpin very irregular performance. This would be considered a shift in the economic and technological paradigm (Dosi 1984, 1988) similar to Constant's (1980) account of the "Turbojet Revolution" where the invention of the turbojet, along with co-evolutionary developments including advancements in airframe design and materials, enabled significant performance improvements in air speed and altitude. The turbojet produced a whole new "jet engine" industry and helped redefine both military and commercial aircraft industries and their users (e.g., airlines). Following the early experimental years of the turbojet, these industries settled in on a new technological trajectory (Dosi 1984, 1988) toward the frontier of the "jet age."

Innovations within the boundary limits of this new frontier occurred at a rapid, but more regular rate. The role of accumulated knowledge—both tacit and explicit (Freeman 1994)—and standards (e.g., the role of the Proney brake as the benchmark for performance measurement and testing) are emphasized. Similarly, semiconductor development since the planar process has

followed Klein's (1977) description of "fast history," but is more in line with Pavitt's (1986) application of "creative accumulation" (i.e., the new technology builds on the old). The "new" technology in this case is the accumulated incremental—particularly process-oriented—advancements indicative of the Moore's Law semiconductor "era." As for standards, indeed Moore's Law itself is used throughout the industry as the benchmark of progress, evidenced most strikingly by the kilo- to mega- to gigabit density DRAM chips. Increasingly, regular advances in microprocessor performance measures such as MIPS (millions of instructions per second) and MHZ processing speeds follow—and become part of—Moore's Law.

Preliminary Conclusions and Future Research

Based on a review of the literature (academic, popular business, and computer trade), an Internet keyword search, and a few personal interviews with major semiconductor players including Gordon Moore and Carver Mead, much has been learned. But no firm conclusions can yet be drawn about what "causes" or what is "caused by" Moore's Law. This examination has revealed that there are two major lines of pursuit from this point. The first is based on the user or "downstream" point of view. This analysis would address the "Wintel" and other "demand-pull" innovation arguments including the expectations feedback hypothesis, but requires more extensive and direct research methods. The second avenue is from the supplier or "upstream" perspective. Since much of the literature is concerned with process limitations (e.g., is it possible to reach 'Point One')—reflecting the reality of the industry's everyday challenge--there is a tendency to examine the "physics" limitations of photolithography and other essential fabrication aspects. At this point it is not clear whether this is just another example of the endless technological pursuit of increasing capabilities and performance similar to earlier advances in turbojet technology. Or is Moore's Law, in Carver Mead's terms, "permission to believe that it will keep going," reinforced by human belief systems? (UVC 1992) Or is it some altogether different variable, yet to be determined?

The answers to these questions are probably all "yes, to some degree." Future research will

attempt to better answer these and related questions with more specificity.

Conclusions and Prospective (see also Appendix C)

Many questions have been raised about Moore's Law. In particular several new questions have surfaced since the author's article was first published and answers were attempted here. More questions will likely be asked into the foreseeable future. Most likely some will not be new as they still require answers. A few of these are repeated here for review.

- What is Moore's Law and how is it measured?
- What are the determinants of Moore's Law?
- Is it a self-fulfilling prophecy?
- How much do market pull factors temper technology push factors?
- Is it in danger of slowing down or possibly ending?
- Is it relevant any more? Should it be changed?
- Has it become *dangerous*? Is blind adherence causing more harm than good?
- Why is there such fascination with Moore's Law?

Some of these have been addressed in Appendix C, but certainly not completely. Some others have yet to be addressed in possible future research. For present purposes it has been argued that Moore's Law has played a vital role in semiconductor innovation, growth and development. Much discussion and analysis have ensued on peripheral aspects of Moore's Law such as the continued debate over the actual rate of progress. But a more important debate has begun over the core of Moore's Law: just what is it (i.e., the first question)?

A partial answer is Moore's Law is at once many things. At bottom it is a simple plot on log-linear paper that is both a good descriptor and predictor of technological progress in semiconductors. This plot, over time, has become an ever moving "line in the sand" that challenges participants to cross it, thus pushing the line yet further.[39] In full view Moore's Law is a complete cycle as Randy Isaac suggests that paces (and is paced by) the participants in the

[39] This phrase is borrowed from Paul Peercy, former President of Semi/Sematech (now called SISA). Peercy used the phrase in reference to the ITRS and chipmakers tendency to step over the line and "beat the Roadmap" (see Chapters 10 and 11). Paul Peercy, personal interview, August 30, 1999.

everyday game called the semiconductor industry. In much the same fashion as Adam Smith's "invisible hand of competition" that silently regulates markets toward equilibrium points, Moore's Law silently guides the advance of semiconductor technology. The result has been a distinct pattern of innovation, one of rhythm or cadence. While the exact pace of this rhythm has not always held constant, its presence is unmistakable. It is now institutionalized in the industry's Roadmap and countless individual company roadmaps, large and small, foreign and domestic, tool supplier and chipmaker, etc.

The semiconductor industry is so much different today in 2004 than in 1995, much less 1985, 1975, and 1965 as briefly described here and elsewhere in this thesis. One constant that has remained throughout this long stretch is Moore's Law.

CHAPTER 9: Early History and Evolution of Semiconductor Technology Roadmaps

"In the semiconductor industry, amazingly enough, high-level roadmaps have been followed pretty well for the last 30 years."

- Turner Hasty[1]

"By the time Sematech was formed, IBM was well-versed in the roadmapping process. Other firms were too: Motorola, TI, Intel. Also, Japanese firms like Toshiba and Hitachi had been using roadmaps since the late-1970s; they even called them roadmaps."

- Obi Oberai[2]

"Roadmaps were developed in the mid 1970s at Motorola. The tools were developed in Phoenix (semiconductor sector) over a series of years. It was an evolutionary process, not developed overnight.

- Neil Hagglund[3]

As discussed in Chapter 2, technology roadmaps and roadmapping practices have become essential planning tools within modern industrial organizations, across many sectors, whether private or public, large or small. Usually, the technology (thus the organization) is moving so fast that few ask, "Where did this roadmap come from?" This chapter attempts to answer this question for the semiconductor industry and is specifically concerned with the early history and evolution of semiconductor technology roadmaps. Roadmapping practices date back much earlier than what is commonly understood. Most people familiar with the Roadmap trace its origin to Micro Tech 2000, a comprehensive report published by the U.S. National Advisory Committee on

[1] Turner Hasty, former Sematech COO and research executive at Texas Industries, from personal interview transcript with Larry Browning, 1993.
[2] Obi Oberai, former Sematech Strategy Officer and semiconductor manufacturing executive at IBM, telephone interview, April 29, 2000.
[3] Neil Hagglund, telephone interview, May 27, 2001, Hagglund is VP, Director of Corporate Technology Planning at Motorola.

Semiconductors (NACS) in 1991. This chapter will address the major activities and events that preceded and in many ways contributed to Micro Tech 2000 and the series of Semiconductor Industry Association (SIA) Roadmaps that followed. This covers a fifteen-year span beginning roughly in the mid 1970s and closely coincides with the period when the U.S. semiconductor industry came under serious competitive threat by Japanese rivals, particularly in the area of memory chips. Micro Tech 2000 represents a good break point for this analysis as this was the first legitimate attempt at an industry roadmap exercise involving broad participation from industry, universities, research consortia, and government agencies and labs. A variety of roadmap activities will be examined in detail to help demonstrate that although early roadmaps involved far fewer participants and a much narrower scope than the succeeding SIA Roadmaps, elements of a successful roadmap—long-range view, multi-disciplinary participation, and consensus-based methodology—are evident throughout the progressive expansion of scope and involvement of this emerging technology planning practice.

Foreward

A full historical accounting of the origin and evolution of technology roadmaps and roadmapping practices is not the purpose (if it were even possible) of this chapter. But as in most things, "history matters" in properly examining the changing role of technology roadmaps in the semiconductor industry. What follows is a compilation of material obtained from published sources and personal interviews,[4] roughly in chronological order, documenting one possible (and hopefully probable) historical course for semiconductor technology roadmaps.

Genesis

The exact origin of technology roadmaps in the semiconductor industry is debatable, but many credit Bob Galvin of Motorola with coining the term—in a particular context—in the mid to

[4] Some paraphrasing and elaboration of personal interviews are the responsibility of the author.

late 1970s.[5] However, the use of the generic term 'roadmap' or even 'technology roadmap' probably dates back much farther (e.g., see Turner Hasty's quote above). Thus, the first thing that must be discussed is to distinguish between the use of the term and the process or practice (using the ITRS process as a model).

As discussed in Chapter 2 the term, 'roadmap' is not at all unusual or complex. Most agree it "fits" as a meaningful label for a form of planning. Linda Wilson of Sematech says it is recognized as a good "catch word."[6] Further, the metaphor relates to highway travel, where having a map is much more efficient than not, especially when the journey is new to the traveler. In connection with this, many feel the term originated in the United States where highway travel is a normal part of modern American life. American culture may be more prone to the use of metaphors to help describe concepts in a less theoretical, more practical fashion. Thus, some have suggested the origin of the term within the automotive industry. Charles Lassen states:

> The term "technology roadmap" is believed to have first come into prominent use in Detroit in the late 1980s. Many electronic component suppliers were asked to pitch their technology roadmaps to the big three to show that they had a technology development plan for the road ahead.[7]

Government Role in Roadmaps

Indeed, the oldest published industry-related material the author found that uses the term roadmap (one word, and as a verb) in the title involves the automotive industry, but from a decade earlier (1979) and for a different reason. "Government Roadmaps Basic Auto Research," includes an interview with the deputy administrator of the National Highway Traffic Safety Administration within the U.S. Department of Commerce regarding a cooperative automotive research program. The purpose of the research roadmap was in response to the fuel crisis of the 1970s:

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[5] Bob Galvin, personal interview, June 13, 2000 and confirmed by other informants.
[6] Linda Wilson, Sematech ITRS Information Manager, personal interview, September 1998.
[7] Charles Lassen, "Beyond Technology Roadmaps…to Economic Waypoints," white paper (Bulletin) posted on the company's website, NY: Prismark Partners LLC, January 1996.

> In fuel economy—the principal thrust of this program—the main question is whether the forces of the marketplace aren't providing a pull stronger than any government regulatory pull... We're talking about a socially responsible automobile with good fuel economy, low emission of pollutants, a high level of safety and damageability [and] attractive to satisfy the desires of the public.[8]

This application description does not seem all that much different than similar collaborative measures that were to follow—in particular, the Partnership for a New Generation of Vehicles (PNGV) two decades years later. What is perhaps most interesting about this particular research roadmap was its government-industry cooperative nature, well before this practice became more commonplace. For example, the article states that the White House Science Advisor, one of the chief architects of the program, predicted it would "lay the technology base for the next generation of automobiles" by focusing research on thermodynamics; combustion and fluid dynamics; structures; noise and vibration; materials science and processing; control systems; and friction and wear.[9] Industry and government would share (on approximately a 50-50 basis) an annual research bill estimated at $50 to $100 million for projects assigned to university, industry, and federal laboratories. This research approach certainly resembles similar applications in the semiconductor industry that were to follow: the SRC, Sematech, the SIA Roadmap, and MARCO Focus Centers.

One final note on the automotive industry. There may quite possibly be a roadmapping connection between the semiconductor and automotive industries as the automotive sector has traditionally been a large industrial user of integrated circuits (ICs). When asked about this possible connection, Bill Howard, former semiconductor executive at Motorola, offers the following observation.

> As far as the origin being in the automotive companies, I have no knowledge of that. I do know that when we went to discuss Motorola's roadmap with the GM / Delco people in

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[8] Howard Dugoff, quoted in Paula D. Hodges, "Government Roadmaps Basic Auto Research," *Automotive Industries*, September 1979, 71, 73. Note that Dugoff was referred to as "chief cartographer" in the article.
[9] Ibid., 69.

> the course of keeping them up to date on our technical progress, they thought it was a novel concept.[10]

More research is required to determine the extent of this roadmap connection—if any—between semiconductor and automotive industries.

Department of Defense

Another source for roadmaps that is very apparent is the U.S. Department of Defense (DoD), and in particular the U.S. Air Force. There is strong evidence to suggest that roadmaps, although not applied solely to technology, may have originated within DoD as a metaphor for planning. Again, given its wide interpretation, it is not possible to pinpoint the exact origin of the use of the term 'roadmap'. However, in the context of planning, or anticipating the future in a fairly-long time horizon (i.e., 5yrs or more), roadmaps seem to fit within the missions of defense agencies responsible for acquisition management of large weapons systems programs that span life-cycles measured in decades. It may very well be that the longer-term horizon of DoD interests combined with the naturally shorter planning horizons of industry brought about a consensus on a working definition of technology roadmaps that we are familiar with today. This proposition is open to debate, but it has at least been confirmed by informants that the historical cross-pollination between government and industry—mostly at the program level—has led to a variety of collaborative planning efforts of which technology roadmaps were one result. A sampling of related inputs from informants follows.

Similar planning methods (i.e., roadmaps of a different name) probably date back to military applications during and following World War II according to Sonny Maynard, executive of the Semiconductor Research Corporation (SRC), and formerly from DARPA, OSD, McDonnell Douglas, and the U.S. Air Force:

> If you take the general subject of roadmaps you can go back a long way. When I was a Lieutenant in the Air Force [I remember] if you were running programs for the Air Force, you had to have a "roadmap" ... a program roadmap, which just in those terms predicted

[10] Bill Howard, e-mail to the author, June 19, 2000.

> how much money you were going to spend, in what fiscal year, so they could plan where to put the money in the budget. That was called a roadmap.[11]

Len Weisberg, who managed the Very High Speed Integrated Circuit (VHSIC) program in the Office of the Secretary of Defense (OSD) in the late 1970s, states that the idea of program and resource planning certainly was not introduced with roadmaps. He comments about the significance of technology roadmaps to engineers and scientists:

> While I was at DoD (1975-1979) ... there were clear forerunners [to technology roadmaps]. For example, 5-year business and product plans have been used for many years. In all major programs, going back well before the 1970s, there were detailed program plans, with each milestone given a specific date, with maps drawn to show the convergence of events (a milestone chart). In many cases, program and product plans incorporated technology plans. The key point about technology roadmaps is that engineers and scientists hate to make detailed projections, since the future is so unclear. Creating a separate discipline for engineers and scientists to make detailed predictions about the future was a very important step.[12]

Sonny Maynard, who followed Weisberg in management of the VHSIC program, sees the roadmap lineage in DoD back as far as post-World War II:

> If you say roadmap you can certainly trace it back to the late-forties, fifties, and the whiz kids; they were using the term. The output of your operations analysis is a roadmap on whatever thing it is you're charting. That's because if you do a Gantt or a Pert chart, it looks like a roadmap. So I think you could say that word in essence came from the government, was cycled through the academic and research community. The semiconductor industry was introduced to the notion through the SRC, and they've prospered with it. They've jumped on it "with both feet."[13]

It may be coincidental, but the Air Force had been, along with NASA, the largest supporter of the IC industry in its infancy during the early to mid 1960s (e.g., Minuteman missile program).[14] This support had fallen off considerably by the early 1970s as commercial applications for ICs rapidly developed in consumer devices like hand-held calculators, digital watches, etc. After about a 5yr hiatus, the DoD became a big player again in the industry with the VHSIC program that began to take shape in 1977. As will be discussed shortly, the VHSIC program with its definitive process technology targets may have been an avenue to transfer (or at least share) the

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[11] Sonny Maynard, personal interview, August 1, 2000.
[12] Len Weisberg, e-mail to the author, August 15, 2000.
[13] Maynard interview.
[14] Herbert S. Kleiman, *The Integrated Circuit: A Case Study of Product Innovation in the Electronics Industry*, D.B.A. Dissertation, Washington, DC: George Washington University, 1966.

practice of roadmapping between government and industry. So by a decade later, when Sematech was forming in 1986/87 (and involving many of the same players), roadmapping would have been commonly understood, even to the point of having procedures to guide the process.

Interestingly, a memo dated July 7, 1987 concerns the Sematech workshops (discussed later in this chapter) that had just gotten underway. The memo included suggestions for future workshops. Paragraph C reads as follows:

> C. SEMATECH Road Mapping Approach and Documentation
>
> Sonny Maynard's office (OSD) has offered to provide us with a copy of the DOD documentation procedures on road mapping for use as a guide in SEMATECH planning. These procedures may help us to formulate a standard model for the theory of road mapping that could serve as a technique at the next scheduled workshops. I hope the DOD documentation may serve together with whatever concepts you may have to find an appropriate roadmapping model for SEMATECH. I believe formulating such a standardized model is important to conducting the workshops.[15]

Attached to the memo are copies of selected parts of Air Force instructions that provide guidance on preparing and assessing program plans. These include AFSCR 11-8 dated 14 May 1982 that contains instructions on preparing briefing charts (called "vugraphs") including symbols for indicating milestones and schedule information, AFSC Form 103 Program Schedule includes standard milestone symbols, and AFSC Form 425 Program Financial Review Assessment (includes rating of satisfactory, marginal, and unsatisfactory). None of these documents contains the term 'roadmap' but it is evident that conventional program planning techniques were used (and continue to be) in preparing time-based roadmaps.

Appendix 9-A is a compilation of early 'roadmap' citations in U.S. Government publications and provides further evidence that the roadmap concept in government existed as far back as 1975, and possibly even earlier. Hence it can be asserted that the government was an early user of roadmaps and may have played an important role in promulgating their use in other applications such as within the semiconductor industry.

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[15] Internal Sematech memo from Chuck Minihan, Perkin-Elmer (representing SEMI, the SM&E industry's trade association), to Colin Knight of AMD and fist Sematech co-COO.

Technology Forecasting

Another possible explanation for the emergence of roadmapping within the U.S. Government is the development of technological (or technology) forecasting, a related activity. The purpose of technological forecasting is to project technological capabilities and attempt to predict the invention and spread (diffusion) of technological innovations. A technological forecast typically includes the time period of the forecast or a future date when a new technology will emerge, along with the characteristics of the technology or the functional capabilities of the technology and a probability of the forecast coming true.[16]

The field of technological forecasting within the government can be traced back to 1937, but it was used primarily by military planners from the 1940s through the 1960s in the areas of aeronautics, atomic power, and missile defense.[17] By the late 1960s and early 1970s rapid technological and industrial development brought increasing interest from the commercial community and several publications in the field appeared. A few of these include:

- Jantsch, Erich, *Technological Forecasting in Perspective*, Paris: OECD, 1967.
- Bright, James R., ed., *Technological Forecasting for Industry and Government: Methods and Applications*, New Jersey: Prentice-Hall, 1968.
- Wills, Gordon, David Ashton, and Bernard Taylor, eds., *Technological Forecasting and Corporate Strategy*, New York: Elsevier, 1969.
- Ayers, Robert U., *Technological Forecasting and Long-Range Planning*, New York: McGraw-Hill, 1969.
- Linstone, Harold A., ed., *Technological Forecasting and Social Change*, (Academic Journal), New York: Elsevier, 1969/70.
- Martino, Joseph P., *Technological Forecasting for Decision Making*, New York: McGraw-Hill, 1974.

The timing makes it quite possible that some of this activity bled over into very early roadmapping efforts in government, but this point deserves more research. However a

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[16] Joseph P. Martino, *Technological Forecasting for Decision Making: Third Edition*, New York: McGraw-Hill, 1993.
[17] Joseph P. Martino, "The Future of Technology Forecasting and Assessment," PICMET '01 Panel Discussion, July 30, 2001. Also see James R. Bright, *Practical Technology Forecasting*, Austin, Texas: Technology Futures Inc, 1998.

preliminary conclusion that can be drawn is that roadmapping, as a practice, may not have come solely from industry as is commonly accepted. Rather, government was a major source, in large part in response to a particular public concern or crisis (e.g., national security, adequate energy supplies, international competitiveness, etc). The basic idea of looking beyond the immediate horizon—in the case of semiconductors to the next few product generations, or current demand in the case of energy—was not of foremost interest to these industries in the 1970s prior to crises that invoked such responses. The very nature of the defense department engaged in or preparing for a crisis necessitates this kind of anticipatory behavior. Referring to the ITRS, one long-time participant states:

> "The Roadmap is actually countercultural, it is not a natural industry activity. It began in the U.S. sitting down and looking around at others such as MITI [Japan's Ministry of International Trade and Industry] doing plans, so we had to."

The VHSIC program is very instructive in this regard since it contained all the basic ingredients for a kind of roadmap approach: crisis, significant resources, collaboration of organizations, and a government sponsor interested in a long-term solution, well beyond the immediate planning horizon. VHSIC was not without its critics as total spending approached $1 billion, yet the program was never actually completed in its intended form. But some have argued that its biggest contribution was that it forced the relatively young semiconductor industry to look ahead in a fashion that was not yet familiar to them. Interestingly, it was the close collaboration with industry that allowed the VHSIC program office to set the process technology targets that would serve as the basis for not only this program, but subsequent industry roadmapping efforts. This point is discussed later.

Roadmapping Process Model Emerges in Industry

Most people close to the field share a consensus that industrial roadmapping processes as we know them today probably emerged sometime in the 1970s or early 1980s. Those that have

studied roadmaps cite crisis as a necessary element that fosters the need for roadmapping.[18] Crisis is a galvanizing event that quickly focuses attention. As was just discussed, the energy crisis of the 1970s and heightened international competitiveness that followed in the 1980s may help explain the roots of roadmapping in related U.S. industries such as automobiles and semiconductors. Other less-macro factors also contributed which are examined in other chapters of this study.

One point worth mentioning here is where the need was first derived. It appears that research, traditionally a curiosity-driven enterprise, is where roadmapping started. The need to look beyond the next innovation step (e.g., device "generation" in semiconductors) is the purview of R&D. The quickened pace of technological change, along with related shortened product life cycles, increased technical complexity, expansion into global markets, and rapidly escalating capital expenditures have all contributed to make the researcher's challenge that much harder. Add to this the scaling back of basic research, most notably in industry, makes the idea of an *organized* approach to research more of an economic necessity. One of the central arguments of this thesis is that roadmapping contributes to an *organized innovation* pattern.

Finally and perhaps the most interesting attribute is that industry—with much influence from government—has been the innovator in diffusing technology roadmapping practices. Unlike similar approaches that attempted to project future technological progress that were developed and practiced mostly within the academic or government communities (e.g., technological forecasting, technology assessment), industry developed and used roadmaps. This explains the much wider acceptance and adoption of the practice. However, this presents additional challenges when attempting to study this practice academically. One problem in particular is that there is simply *not* much written about it. The one area where technology roadmaps seem the

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[18] See for example, Dudley Caswell of Enterprise Innovations, "Roadmap Purpose, Next Generation Manufacturing, Integrated Manufacturing Technologies Roadmapping, and Industry Roadmap Examples," PowerPoint presentation at Technology Roadmap Workshop, moderated by Office of Naval Research, October 29, 1998, slide 12.

most pervasive is the semiconductor industry, where the factors mentioned in the previous paragraph are pronounced.

Semiconductor Industry Adoption

This discussion begins with a review of internal company roadmaps where it is widely accepted that roadmaps were used, and progresses to industry level roadmaps. Although many semiconductor firms claim to have used technology roadmaps for some time (e.g., IBM, Texas Instruments, Intel, and others), roadmapping practices at Motorola are reviewed here as a representative case, in large part because there is more historical evidence available for this firm. Also, many credit Motorola with originating the process. The purpose of this discussion is to reveal an evolutionary development of an internal practice that helps explain subsequent adoption at industry, national, and international levels.

Motorola

The earliest documented source of the use of internal technology roadmaps in semiconductors involves Motorola in an account by Morone (1993). In a chapter on Motorola Communications, technology roadmaps are introduced:

> *Technology roadmaps*. General management played a prominent role in this effort to enhance and broaden the individual product lines. William Weisz, former CEO and vice chairman, and John Mitchell, former president and vice chairman, "stuck our noses in the businesses continuously," putting pressure on individual product line management to press for the next generation, for the smaller, lighter, and better performing product. By the mid-1970s, this general managerial encouragement began to evolve into a more formalized review process, spearheaded by Bob Galvin, then the chairman, in which each business was required to develop what eventually became known as "technology roadmaps." By the 1980s, these had become rather detailed technology and product planning exercises, but in essence, they involve three basic steps:
>
> 1. Projects the future evolution of each product line over the course of the next five to ten years. Projections are based on detailed historical analysis of product life cycles and experience curves... "Once you plot these things," Mitchell explains, "you see that the key next generation should arrive *here*..."
> 2. Forecasts the evolution of the technologies required for development of these projected products.

3. Combines the product projections with the technology forecasts ... and the desired timing of these products are placed against forecasts of the technologies needed to develop those products in the time frame desired.

The philosophy underlying this process is that technology is not developed in the abstract, but rather must be driven by a focus on future products ... Mitchell argues the "research program *has* to be looking out a generation or two on a product roadmap." Businesses that are in their pre-emergent state are not subjected to this kind of review. But according to Mitchell, if the business is well established and "if it has an orderly heritage, where you can almost sit there and rattle off all the generations ... then you ought to be able to look to the next five to ten years and say you need that radio at that time."[19]

The strategic context of the metaphor 'roadmap' along with the structure and discipline that the practice provided is discussed:

George Fisher, Motorola's chairman and CEO, explains, "Bob Galvin would always say, 'You can't know what's around the next corner, so construct an organization that is able to adapt. But you have to have a framework [roadmap], or you get too distracted and diversified. You keep your eye on the road.'"[20]

Neil Hagglund, VP and Director of Corporate Technology Planning at Motorola, was an active roadmap user in the Communications Sector prior to moving to the corporate position to oversee company roadmap practices in 1987.[21] He succeeded Charlie Willyard in this unique capacity and has been involved in roadmaps at Motorola probably more than anyone else. Some refer to him as "Mr. Roadmap." Hagglund is particularly proud of the broad application of the roadmapping process throughout the firm. He confirms that roadmaps developed sometime in the mid 1970s at Motorola with the main tools coming from the Semiconductor Product Sector in Phoenix over a series of years. He emphasizes that it was an evolutionary process and was not developed overnight.

Asked if technology roadmapping originated in Motorola he is not certain but has little doubt that Motorola has been on the forefront in technology roadmapping practices. "Roadmaps are a part of Motorola's culture," says Hagglund. Thus, Motorola has been much more involved in company-wide roadmapping application than other firms, and not just in semiconductors. The

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[19] J. Morone, *Winning in High-Tech Markets: The Role of General Management*, Boston: Harvard Business School Press, 1993, 87-9.
[20] op. cit., 119.
[21] Neil Hagglund, telephone interview, May 27, 2001.

process was broadly applied across all sectors. For example, in the Communications Product Sector alone the process started in the 1980s with the first application in 2-way radios, then pagers, then cellular phones, now everything from basic materials and biology to entire satellite communications systems. Further, the process is used in many different applications of technology such as the government electronics group in Scottsdale, Arizona.

Hagglund attributes success of the process to upper management's support in the early days: Bob Galvin, Chairman; Bill Weisz, President; John Mitchell, COO (Weisz and Mitchell were from the Communications Sector). The process developed and evolved with their help, then permeated throughout the company. He says the criticism from Galvin and others was that managers were getting too far away from the technology. Regular Management Technology Reviews (RMTRs)[22] were annual reviews by senior management held between 1976 and 1997/8 timeframe. These served a very important function. As one informant stated, "behavior changes when the CEO is coming to town." This activity developed along with the roadmap process and was a good summation of the process. The annual review process has since been enhanced to include other business reviews.

In summary, Hagglund remarks, "Motorola developed a roadmap *process*, not just a chart." He is also optimistic about the future of roadmaps at Motorola:

> Since roadmaps are part of our culture, the process will continue. New tools will be developed while some old tools will pass. It is an evolving process. The overall strength of the roadmap process is that it forces you to put in motion today actions to evaluate technologies that will be needed in the future (beyond 6mos) to meet your customers' needs. However, the overall weakness is a characteristic of trend analysis and experience curves: trends may NOT stay the same. The process is not foolproof. It's not just about extending the trend line. There's nothing wrong with using it, but when it comes to disruptive technologies you must be willing to plot these. This can and should be done, but you must be willing to acknowledge changes and "bend" trend lines.[23]

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[22] Other informants referred to these as "Routine Management Technology Reviews" or "Road Map Technology Reviews." In any case everyone knew them more by its acronym: RMTR.

[23] Hagglund interview, op. cit. Note that Hagglund challenges the common criticism that roadmaps necessarily limit focus and result in path dependency.

Ken Davis, VP and Research Director in one of Motorola's many labs, concurs: "Roadmaps definitely will continue. They have become part of our corporate language, progressing in a wave throughout the company. Motorola is a large, diverse company. This is not easy to do but roadmaps are everywhere at Motorola."[24]

Ted Lind's career in the Components Products Sector spanned more than thirty years where he advanced from junior engineer to Member of the Technical Staff. He managed the advanced technology development group for a number of years and was essentially the informal chief scientist/ engineer on the crystal side of the operation. He has excellent first-hand information on the day-to-day use of roadmaps. He recalls:

> During my career I participated in many RMTRs for our division. Bob Galvin, John Mitchell, and Marty Cooper were the upper managers reviewing our operations in the early days. We started RMTRs in the mid to late 1970s. When we moved to Franklin Park in 1972 [new group, occupied vacant facility from Quasar division sale] I definitely remember roadmaps being used. I had been a group leader then for five or six years. Our division made frequency sensitive devices such as piezoelectric quartz oscillator crystals and filter crystals for use in Motorola radios. Research organizations used the RMTR extensively. Over time it gradually expanded to include most engineering organizations within the business.
>
> As our technologies became more complex the design and development of a product required many pieces of the puzzle to come together in a timely manner. The Roadmaps spread to most of the engineering organizations. They became a good tool to make sure a degree of coordination existed between a process group developing next generation manufacturing processes and product designers developing next generation radios. They helped to make sure the technologies under development were compatible in a future time frame and also helped to make sure the timing was correct. In our division I found this aspect to be the most useful. It was a long-term product plan that helped to insure each major group within the engineering organization was working in synchronism rather than at cross purposes.
>
> The RMTRs also served an important communication function. The reviews were typically held in the largest conference rooms available and many people were invited from across the organization. Several times a year the company's technologists would gather at one of the RMTRs. This allowed a lot of face-to-face communications between the technology drivers across the company. It also allowed them to compare notes on a very wide scale to make sure their efforts complemented the overall effort and company goals.[25]

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[24] Ken Davis, telephone interview, June 1, 2001.
[25] Ted Lind, e-mail to author, May 22, 2001; follow-up telephone interview, May 26, 2001.

Bill Howard was an executive in charge of Semiconductor Operations in Phoenix, Arizona in the mid to late 1970s where technology roadmapping started in that operation. According to Howard, a confluence of factors contributed to its development.[26] Howard recalls Len Weisberg from OSD in DoD visiting the Motorola Semiconductor sector in that time frame to discuss the upcoming VHSIC program (see earlier discussion) and asking "how do you describe your vision of the future?" Motorola's response was a 5-year technology vision including capabilities, process, design, etc. According to Howard, Bob Galvin had been actively seeking a new strategic technology planning approach, and upon seeing the result of this exercise, coined the term 'roadmap' and insisted it should be used throughout the corporation as a common planning tool. Further—and what begins to define this as a unique planning process—roadmaps were to be looked at or reviewed *systematically*; the roadmap review process involved formal sessions concerned with managing the future. Owen Williams, who worked for Howard at the time and later became very active in the SIA Roadmap process, recalls the comprehensiveness of Galvin's RMTRs based on product/technology roadmaps.[27] Box 9-1 offers more insight on the early use of roadmaps within other sectors of Motorola.

Box 9-1. M68000 Microprocessor Family Roadmap

An example of Motorola's early use of roadmaps in commercial applications is in microprocessor development. Among the first external documents where the term 'roadmap' appears in the title is a 1980 conference paper entitled "The M68000 Family Roadmap Shows the Way."[28] From its abstract it is apparent that at least two important features of roadmapping are discussed: inclusiveness, "the whole system," and a long-term perspective, "what some of the new members of the family will look like."

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[26] William E. Howard is also the co-author with Bruce R. Guile of: *Profiting from Innovation*, a report of a three year study commissioned by The National Academy of Engineering, published by The Free Press (1991).
[27] Owen Williams, telephone interview, August 25, 1999.
[28] J.F. Stockton, "The M68000 Family Roadmap Shows the Way," Conference Paper: Wescon/80 Conference, 16-18 September 1980; Anaheim, CA, USA. Source: Science Citation Index.

Abstract: These days, a systems designer must be more aware of factors affecting his choice of a microprocessor other than just the cost and performance. He must consider the whole system, the development support tools, and he must also be aware of other design efforts under way in his own company. In spite of efforts to make a systems design independent of the microprocessor selection, the trend is still for a company to be tied strongly to a particular semiconductor vendor and his family of processors. It is becoming more important to pick not only a microprocessor, but a microprocessor company as well. To understand this better let us look at what some of the philosophies of the M68000 Family are, and then at what some of the new members of the family will look like.[29]

Galvin himself recalls the genesis at Motorola and agrees with Howard that technology roadmaps, at least within the electronics industry, started at Motorola in the mid to late 1970s time period in the semiconductor sector.[30] He states that he used to spend countless hours in semiconductor labs, "dropping in on people, finding out what they're working on." He came to the realization that he was learning more than his senior managers and concluded that this front-line knowledge was valuable and needed to be shared in a more systematic way. He gathered his executive team (i.e., Bill Weisz, John Mitchell, John Welty) in Phoenix and vented serious concerns about not knowing this essential information. He insisted on a formal process or method emphatically stating, "I want a roadmap of what we're doing and where we're going." He drew a simple chart (i.e., x and y axis) on a single sheet of paper showing what the firm was doing, putting resources into, etc. and directed his team to prepare a detailed roadmap. He then said he would return in six months to attend the roadmap review meeting (presumably the first RMTR). About three weeks later in the company's corporate headquarters in Chicago, John Mitchell from the CEO Office approached Galvin and asked him, 'you really want this?' and he said 'yes, of course'. Mitchell then said that Galvin's approach wouldn't work as suggested; it was not complete enough. Galvin said 'fine, do what makes sense'. Working with Marty Cooper in Research, Mitchell incorporated different factors (e.g., learning and product life-cycle curves, etc) and began to synthesize different considerations into the process. This was the foundation of the

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[29] Ibid.
[30] Bob Galvin, telephone interview, June 12, 2000.

technology roadmapping process that would become a staple in Motorola's strategic planning regimen. Galvin's summarizes the genesis: Roadmaps were my impetus, but their [Mitchell, Cooper, and others] design.[31]

With regard to the connection with the VHSIC program that Howard has suggested, Galvin states, "Nothing comes to my mind on that score. I had known of the VHSIC program, but there was nothing unique about it that prompted me to do what I did in the initiation of the roadmap program. It is possible that those who refined the program put some special attention to the VHSIC roadmap, and were that to be the case, that would legitimately fit into the history of the device." Bill Howard clarifies his understanding of the role the VHSIC program played:

> There is no inconsistency between the recollections of Bob Galvin and others at the top of the Motorola hierarchy and the memories of those who participated in the VHSIC effort. As in many changes, several forces came to bear at about the same time to produce a workable roadmap concept. Bob is right in that he and Bill Weisz were looking for a way to express the Corporation's technical directions. About the time the VHSIC meeting took place, they were asking for some way to present future technology directions.
>
> None of the senior leaders of the corporation were involved in the VHSIC meeting. Nonetheless, that meeting provided the tool that answered the management question of how to display not only the surface level of the technology but the contributing elements as well. When the Chicago leadership came down for their next operations review, we presented the VHSIC charts (they were not labeled VHSIC) and Bob indicated enthusiastically that it was the answer to the more general questions he had been asking.
>
> One other thought - the VHSIC roadmapping connection was not something that was part of DoD's program. It was the basis of the presentation we at Motorola Semiconductor made to visiting VHSIC program people (specifically Len Weisberg) while the program was in its formative stages. I have a copy of the original slide, but it is not dated. To my knowledge, the VHSIC program never picked up roadmapping as part of the program - the format became the basis for Motorola's technology planning system.[32]

VHSIC Connection

The importance of a possible VHSIC connection reappears in the early 1980s as Larry Sumney, who succeeded Len Weisberg as program director, left to head the newly-created

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[31] Ibid.
[32] Bill Howard, e-mail communication, June 19 and 25, 2000.

Semiconductor Research Corporation (SRC), the first research consortium of the SIA,[33] and where the idea of semiconductor *industry* roadmapping started (see following discussion). According to Court Skinner of the SRC, the VHSIC program, set up by OSD and later DARPA, preceded both SRC and Sematech (later a DARPA program) not just in time, but also in approach.[34] The significance of VHSIC was that it represented the first government IC program exclusively based on *silicon* (Si) substrate material. As discussed in Chapter 6 the government's defense and space agencies had significantly funded early IC development in the 1960s, but most of this dealt with germanium devices which eventually did not find significant commercial applications. Except in gallium arsenide (GaAs) devices, government support of silicon ICs had become almost non-existent until VHSIC. More importantly, VHSIC re-established an important government connection with the industry. This helped as much as anything in later obtaining government support for Sematech, where the industry's roadmap flourished.

Technically, VHSIC represented the most advanced semiconductor technologies at the time. This was to the chagrin of many industrial leaders. Bob Noyce, Intel's co-founder and Chairman, was a vocal opponent largely in fear of losing scarce engineering talent to the program. But according to Bob Burger of the SRC, industry stood to gain—not lose—from VHSIC, "Even though VHSIC was focused on defense, from 1980 to 1990 it made important contributions to industrial integrated circuit technology at a very crucial time for the industry."[35] According to Skinner, from a pure knowledge standpoint anyone in industry at that time needing semiconductor research information, including the SRC, went to the VHSIC program. Teams from industry participants such as National Semiconductor, IBM, Westinghouse, AT&T, Motorola, etc. collaborated (very carefully) on technical problems. VHSIC program reviews by participating companies were a public way for individual firms to gauge or benchmark themselves against each other in a form of

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[33] The Semiconductor Industry Association (SIA) was formed in 1977 to represent a unified image of the state of the industry to the federal government and solicit help where needed.
[34] Court Skinner, telephone interview, July 21, 2000.
[35] Robert M. Burger, *Cooperative Research: The New Paradigm, Semiconductor Research Corporation*, unpublished manuscript, 2001, 38-9.

open competition. Driven by definitive technology targets (i.e., "near micron" 1.25 microns for Phase I, and "sub-micron" 0.5 micron for Phase II), the VHSIC program contained some of the key factors that could be interpreted as a technology roadmap exercise, if not explicitly intended as such.

"Motorola's Technology Roadmap Process"[36]

This oft-cited article appeared in 1987 as a descriptive narrative, with sample illustrations, of a practice that had become highly refined at Motorola by this time, roughly a decade after its inception. Charles Willyard was the director of technology planning at Motorola's corporate headquarters. Bill Howard describes Willyard as the "corporate roadmapping guru until his retirement from Motorola." This article articulates the roadmapping process and is, in fact, still cited as one of a handful of "must read" pieces for students of technology roadmapping practices. The rationale for technology roadmaps is explained in the second paragraph:

> Because our [Motorola's] products and processes were becoming much more complex over the years, we realized there was the danger that we would neglect some important element of technology. This potential danger gave rise to corporate-wide processes we call "Technology Roadmaps." The purpose of these documents is to encourage our business managers to give proper attention to their technological future, as well as to provide them a vehicle with which to organize their forecasting process. It also provides a means of communicating to the design and development engineers, and to the marketing personnel, which technologies will be requiring development and application for future products.[37]

Notions such as technological future, organized forecasting, and communicating across disciplines characterize a process that had evolved from application in semiconductor operations to an enterprise-wide usage, presumably for all product lines. Of particular interest to this line of study are several graphics of key data considered. Although these are samples, another dimension of roadmapping, namely *time* as the independent variable or x axis on an x/y graph, is prominent. This temporal variable embodies the idea of Moore's Law (see Chapter 8) as a log-

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[36] C. H. Willyard and C. W. McClees, "Motorola's Technology Roadmap Process." *Research Management*, Sep-Oct 1987, 13-19.
[37] Ibid., 13.

linear forecasting approach that becomes the recognizable structure in subsequent roadmapping practices. Figure 9-1 is taken from the article and shows a ten-year timeframe (1982-1991) of an unidentified product. One of the required technologies included is IC technology progressing from 5 micron to 1 micron CMOS well within that planning horizon. IC technology is one of seven other technological requirements portrayed against time that reveals the degree of comprehensiveness of roadmapping.

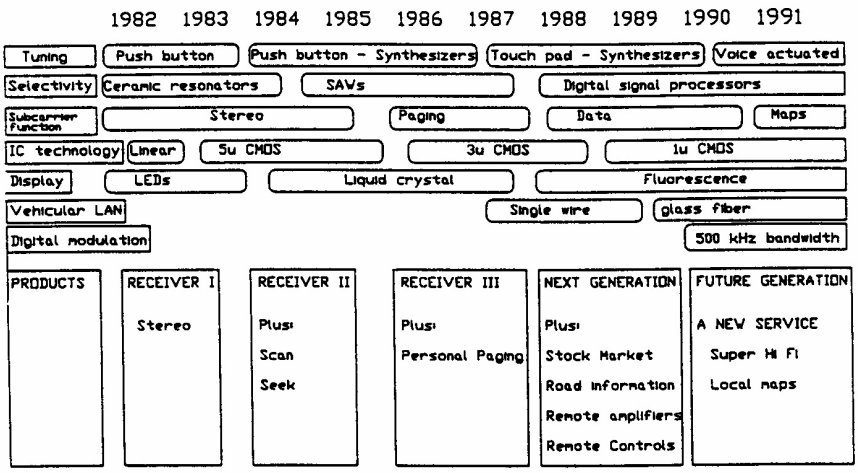

Figure 7.—Technology Roadmap Matrix summarizes technological requirements for future products. This example is for a broadcast automotive FM receiver.

Figure 9-1. Graphical Portrayal of Sample Motorola Technology Roadmap

Source: C. H. Willyard and C. W. McClees, "Motorola's Technology Roadmap Process." *Research Management*, Sep-Oct 1987, Figure 7, 18.

This author has visited Lucent Technologies and collaborated with Philips International, both of which are big practitioners of product-technology roadmaps. Their roadmap processes closely resemble those described in this article. Tom Kappel, who worked at Lucent at the time, had studied Motorola's roadmapping process. His dissertation on Technology Roadmapping includes this abstract of the Willyard/McClees article:

> At Motorola, Inc., managerial tools, called technology roadmaps, are used to give business managers a comprehensive assessment of their technologies and everyone else a long range perspective of future product needs. The product technology roadmap is a compilation of documents providing a complete description of the product line of a division or operating group. The roadmap encourages use of structured tools in the planning and managing of the complex technological environment and furnishes a framework for review of present activities and progress. The product technology roadmap has eight sections... At Motorola, the technology roadmap helps create an environment in which a proper balance is maintained among various management issues.[38]

A final note on the Motorola process: asked why anything had not been published on Motorola's roadmap process since the 1987 Willyard/McClees article, Neil Hagglund offered this explanation:

> The 1987 article was very descriptive, Charlie captured the process, but there's one thing that is somewhat misleading. If read carefully, the message is that if you use these tools and do trend analysis, then that's really all you have to do. The reality is that a roadmap is a living tool that's only as good as the people and their innovative ideas that construct it. The article doesn't capture that all the rules may change. The article was probably good for its time [late 1980s] but look at all the changes just in the last few years. No one anticipated this, including Bill Gates, and he's pretty smart! Motorola has also made some bad calls in this timeframe.[39]

His conclusion: roadmapping is much more complicated than just developing process tools or as another long-time practitioner quips: "A roadmap is more than a semi-log plot on a piece of paper."[40] Organizations must anticipate change and incorporate that knowledge into roadmaps. This is a primary reason that roadmapping has become an iterative process. The rapid pace of innovation in technology is increasingly more important today. According to Hagglund, the reality is that firms don't really talk about how internal roadmaps are used outside the company, yet another reason nothing new has been published. There's only so much time and companies will focus on trying to use it to their best advantage versus constantly trying to improve the process: they're not keen on looking at documentation: "that's the last thing to worry about," according to Hagglund.[41]

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[38] Thomas A. Kappel, *Technology Roadmapping: An Evaluation*, Ph.D. Dissertation, Evanston, IL: Northwestern University, 1998, 274.
[39] Hagglund interview, op. cit.
[40] Don Wolleson, telephone interview, August 3, 1999.
[41] Hagglund interview, op. cit.

Roadmapping in Other Companies

As previously mentioned, other companies were also using roadmaps or similar practices for product or technology strategic planning. Recall Turner Hasty's quote at the beginning of the chapter. Their wide usage is also mentioned in the following statement from the 1992 SIA Roadmap:

> Roadmaps, which are widely used in industry, show the full range of technology needed to meet IC needs of future electronics products. Roadmaps provide the basis for establishing milestones for R&D activities necessary to turn technology plans into reality.[42]

However, except for Motorola, there is very little historical literature that reflects internal company usage. Thus, this section draws on personal interviews. Obi Oberai, formerly of IBM and founding Director of Strategic Planning at Sematech, recalls the practice that emerged within IBM. Note the need for external communications along with an emphasis on consensus:

> By the early 1980s, huge investments were required in semiconductor manufacturing, equipment, and materials, and especially in lithography. Chipmakers had to have a cohesive, defined way of deciding which investments to make. They could have "sat in a corner" and directed [top-down] investment decisions, but realized that due to increased complexity of chip fabrication, everyone had to get together. IBM had several technical experts, including IBM Fellows, to jointly contribute to this effort. The result was a series of roadmaps (10-12 different processes, e.g., applied materials) created by subject-matter experts using a Delphi technique. The purpose was to define *long-term* needs, 10-15 year look at where we are headed versus a short-term view [next generation] which was the typical planning horizon. Paul Low, President of the Division, fostered this activity to go outside, which was unusual for IBM at the time, to include material and equipment suppliers.[43]

Oberai continues, pointing out that industry roadmapping was a logical outgrowth of refined company roadmapping practices:

> By the time Sematech was formed [in 1987], IBM was well versed in roadmapping processes. Other firms were too: Motorola, TI, Intel. Also, Japanese firms had been using roadmaps since the late 1970s (e.g., Toshiba, Hitachi); they even called them roadmaps. The practice was not new by the mid to late 1980s. A 10-15 year horizon was so far-reaching for the semiconductor industry at the time. This is very significant in such a fast-

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[42] Semiconductor Industry Association, *Semiconductor Technology Workshop Conclusions*, San Jose, CA: 1993, 4.
[43] Avtar "Obi" Oberai, telephone interview, April 29, 2000.

> moving industry. Also, the longer-term view helps explain how roadmapping has evolved from single company to industry to national to international scope.[44]

With the apparent widespread usage, this raises the question, "Why has the semiconductor industry in particular embraced roadmapping so enthusiastically?" Galvin attributes (with adequate modesty) some contribution from the priority he placed on roadmaps at Motorola, a major player in semiconductors. In fact, Motorola has traditionally been a strong participant in industry groups such as Sematech, and people like Bill Howard, Owen Williams, and others have had great influence. Further, Galvin has been a strong advocate for the adoption and use of Science Roadmaps with the national labs, Congress, and other groups such as the Santa Fe Institute. Finally, informants for this research offer several additional answers to the question "why the semiconductor industry?" in three general categories as follows (see answers to Question #21 in Appendix B for the complete list of responses):

1. Unique technology and industry, rapid and predictable rate of technological change, Moore's Law:
    - A formal recognition of history 1960-1990s; uses Moore's law as a guide to planning. Other industries do not have such a clear model, nor are they as viciously competitive.
    - Rapid pace of change, if you don't have a willingness to adapt roadmap frequently, you will die. Semi industry unique, without precedence - some similarities, but nothing with same productivity curve, no other industry.
    - I can tell you, everyone knows what the clock frequencies are going to be next year, they are driven by Moore's Law scaling curve. The industry has been driven by technology evolution more than by product evolution alone.
    - Because this industry has Moore's Law as an economic statement of intent.
    - No other industry evolves so quickly, yet so predictably (Moore's Law).
    - History of technology progression (Moore's Law) so clearly documented, rate of advance/pervasiveness astounding.
    - Because industry has a unique technology that has advanced as rapidly for so long.
    - Semi industry economic model very different than other mature industries: chips or computing (use), technical problems revolutionary (e.g., new materials), pace of change very fast. See Dan Hutcheson article in Scientific-American regarding immensity of investment, complexity much greater, very unique industry, yet successful.

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[44] Ibid.

- Driven by the cost and complexity of the technology as well as the rapid rate of change in introducing new technology nodes.
- Moore's Law productivity gains are becoming increasingly difficult and costly to implement, yet these productivity gains are essential to industry growth.

2. Need for structure, commonality in order to reduce risk and gain efficiencies:
   - It has proven to be the best tool we can find; it brings a reasonable degree of order to what could be a chaotic set of options in many technology areas.
   - Because the industry is notoriously bad at planning and this gives a common framework.
   - It gives a standard framework against which to benchmark the whole business enterprise.
   - Because people like standards against which they can measure.
   - Industry needs to restrict R&D expenditures, budget constraints.
   - Greater efficiency needed due to competitiveness.
   - Heavy/expensive manufacturing technology, many elements common to all, suppliers are glue, solutions need to be common (15 companies all doing CMOS process - all multi-billion companies), suppliers feeding industry. Common needs.
   - The problem has gotten too big for one company to pool resources to stay on curve - need to coordinate/ control costs.
3. External use, communication of most important information to supply chain:
   - One purpose of semi roadmaps was to specify requirements and communicate these needs to equipment suppliers (e.g., Applied, KLA). Before this, suppliers were essentially "guessing" customer needs - very inefficient use of industry resources. Roadmaps helped to communicate specific needs, greatly reducing guessing tendency.
   - Semiconductor industry has unique aspects - created a need for Roadmap, also made it what it is: can't make any changes in industry without integration of disparate companies. For example, I-line 248nm to 193 requires exposure tool (6 companies), resist technology (3 companies), mask technologies (2-3 other industries) to pull off this change.
   - It reduced mis-information.
   - A semiconductor manufacturer can no more control the supplier industry.
   - The Roadmap gave them the promise that they wouldn’t be ‘blindsided’ by something that was completely unanticipated.
   - Probably from desire to avoid wrong investments in tools and manufacturing, though this is less the case now with more diverse participation.
   - With the investments being considerable (currently $1-3 billion for new fabs) and materials approaching ultra purity levels, the roadmap in a sense forces a degree of standardization with materials and processes. Not that each chipmaker’s process is a carbon copy of its competitors, but the industry tends to select a “winning” solution that results in a degree of standardization.

Emergence of Semiconductor *Industry* Roadmap

By the 1980s the stage was set for the practice of roadmapping to evolve beyond an individual company's domain. As was previously discussed, by this time some—if not most—companies had roadmaps of some form, even within Japanese firms. They may not have been called 'technology roadmaps', but they served the same purpose as strategic technology planning tools. At the time, though, a company roadmap was closely guarded, considered the competitive "crown jewels," as one informant called them. Sharing them to anyone other than a strategic partner (e.g., major customer or equipment supplier) was just not done.[45] With the development of collaborative R&D programs, especially research consortia, this mindset gradually began to erode and give way to a more cooperative approach to roadmapping. This important transition is examined in the following paragraphs.

Conceptual Framework Forms[46]

As firms developed their individual technology roadmaps, a certain commonality in approach developed. A technology forecast against a time variable that spanned five, ten, or even fifteen years is one example. The other axis was (and still is) future technical capability measured in terms of increased DRAM bit density (Moore's Law), faster logic chip clock rates, reduced device feature size, or the like. The realization of a definitive device scaling pattern that emerged during the 1970s with the broader adoption of CMOS and other factors enabled IC researchers, developers, manufacturers, even marketers to chart a log-linear projection of future capability with increased confidence. Once a future goal or target was seen, the issue became how to reach it; metaphorically, to "map" the route to the destination. Thus, the real purpose of a technology roadmap was not to simply forecast the future, although this was a major component, but to lay out the path to get there. Specifically, this meant a *methodical* and *systematic* approach to

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[45] Ibid.
[46] See Chapter 2 and Ronald N. Kostoff and Robert R. Schaller, "Science and Technology Roadmaps" *IEEE Transactions on Engineering Management*, Vol. 48, No. 2, May 2001.

defining the needs of supporting technologies, materials, and other resources in order to realize technological goals. Bill Howard explains the strategic importance of this change to Motorola:

> My experience before roadmapping became a way of life in Motorola was that companies did try to forecast technical advancements, but did not look too deeply into those that were conceptual as opposed to those that were more or less at hand. What roadmapping did for Motorola was to use the technical forecast - including the supporting technologies required to realize a technical capability - to drive business goals. Prior to roadmapping, technology planning (as opposed to factory planning or financial planning) was much more laissez faire. Roadmapping made the solution of the R&D problem a set of hard business objectives. What was important was the use of the roadmap to mobilize and coordinate the R&D assets of the company to accomplish a mutually supporting set of R&D goals.[47]

Thus, a technology roadmap became a decision tool, *one that integrated Motorola's technology goals with its business goals*. This point deserves emphasis. Technological forecasting and other forms of technology planning were, for the most part, the province of senior technologists. Typically, these exercises approached technology independent of the business enterprise. This partly explains why they were not adopted as a mainstream planning tool. In connection with this, the roadmapping process broadened participation through a framework characterized by cooperation, collaboration, and consensus. Howard continues:

> It's important to understand that roadmapping is a social process. A collegial planning effort is critical to achieving the set of shared goals that makes roadmaps succeed in that it achieves buy-in from the community at large. Prior technology forecasting efforts stemmed from high level thinking about technology and did not actively seek inputs from the technical staff. Lots of organizations engaged in planning. What is new about roadmapping (with the exception of the Manhattan Project) is the active involvement of the technical participants in setting expectations and goals.[48]

It is evident that these benefits could be realized by a wider audience than a single firm. The catalyst for this extended use was the same as at the firm level: *competitive advantage*. The difference was one of scope. International competitiveness emerged as a national priority among industrial nations in the late 1970s and semiconductors were no longer the sole domain of American manufacturers.

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[47] Bill Howard e-mail, August 23, 2000.
[48] Ibid.

Setting Collective Technology Targets: VLSI, VHSIC, and SRC

The need for U.S. semiconductor *industry* attention was precipitated by a national concern (later crisis): the Japanese challenge of the U.S. industry's global market domination as discussed in Chapter 6. Most agree that MITI's Very Large Scale Integration (VLSI) program was a major catalyst. Table 9-1 shows how effective the Japanese were at mounting a formidable challenge against U.S. manufacturers of dynamic random access memory (DRAM) devices, then a vital "technology driver" of new IC process technologies.

Table 9-1. Maximum DRAM Market Share

DRAM Device Type	Volume Production Year	Maximum Market Share U.S.	Maximum Market Share Japan
1K	1971	95%	5%
4K	1974	83%	17%
16K	1977	59%	41%
64K	1979	29%	71%
256K	1982	8%	92%
1M	1985	4%	96%
4M	1990	2%	98%

Source: Jeffrey T. Macher, David C. Mowery, and David A. Hodges, "Reversal of Fortune? The Recovery of the U.S. Semiconductor Industry," *California Management Review*, Vol. 41, No. 1, Fall 1998, Table 1, 111.

The VLSI Program of the late 1970s was in response to an anticipated introduction of advanced IC technology from IBM. Japan's Ministry of International Trade and Industry (MITI) had attempted for more than a decade to directly thwart IBM's dominance in the Japanese computer market with little success. Following IBM's very successful System 360 introduction in 1964, MITI organized a "very high speed computer system project" that helped foster the development of a Japanese computer industry, much of which occurred through partnerships with

American computer makers other than IBM. The introduction of the IBM System 370 in 1970 would force some major U.S. computer makers (e.g., RCA, GE, and TRW) to exit the industry, thus prompting MITI to realign the Japanese computer industry. Two additional national research projects were launched to help Japanese computer companies remain competitive. But when the Japanese learned of IBM's future system plans that included the development of a one-megabit memory chip by the early 1980s, the focus of MITI's efforts shifted from computer design to the underlying IC technology and more specifically, the development of lithography equipment required for the fabrication of chips.[49]

Thus if chip technology could be advanced, computer design would logically be advanced. Further, the drivers to advanced chip technology lie both in design and manufacturing. As device designs became increasingly complex, the ability to manufacture them became more of a bottleneck. Realizing this, the VLSI Program concentrated on improving manufacturability of devices through a collaborative research effort involving Japan's five largest industrial chipmakers. The result was nothing short of amazing. It is widely acknowledged that the VLSI Program was one of the most successful national cooperative research efforts in the history of the industry. Testimony to this is all the "copy-cat" approaches to collaborative research that followed.

The importance of VLSI to technology roadmaps is not apparent at first. Although not by name, the VLSI program represented a "kind of" industry-level technology roadmap exercise, or at a minimum a precursor to one. Definitive technology objectives were set (e.g., targets of lithographic spatial resolution and alignment accuracy; also the 256Kb DRAM, later revised to 1Mb, was a program goal), a deliberate plan that addressed the progressive needs to achieving these targets was developed, and lastly, a collegial environment through a shared lab was provided.

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[49] Wataru Nakayama, William Boulton, and Michael Pecht, *The Japanese Electronics Industry,* Boca Raton: Chapman & Hall/CRC, 1999, 45-6.

By 1980 Japan was well on its way to dominating the worldwide DRAM market; DRAM technology had been developed in the U.S. a decade earlier. A full U.S. response would take the entire decade of the 1980s to unfold. The first major U.S. program, VHSIC, was already underway and dealt exclusively with the defense needs of ICs. It is important to note that by the mid 1970s DoD and other government agencies had become small users relative to the exploding commercial markets for ICs. VHSIC's purpose was to first ensure that DoD's needs were not neglected, and secondly, as a by-product, help advance IC technology for the benefit of the U.S. semiconductor industry and thus respond, in kind, to the MITI VLSI effort. Like VLSI, VHSIC had technology targets based upon device feature sizes as previously mentioned.

The Semiconductor Research Corporation (SRC) was a separate, but related initiative that grew out of the Japanese DRAM onslaught. Analyzing the competitiveness problem revealed structural deficiencies beyond technology, including human resources and basic research. Skilled resources were already scarce (e.g., recall the consternation by Bob Noyce with the VHSIC Program) and the situation was projected to worsen as U.S. colleges and universities simply were not enrolling enough students in engineering, chemistry, physics, and related sciences to meet the burgeoning needs of the industry. In basic research, the U.S. semiconductor industry, realizing that federal government R&D funding was inadequate and perhaps inappropriate to the areas they felt most important, saw the need to "collectivize" a research agenda that would be carried out by the university community. Addressing the two needs of the university system—quantity and quality of skilled personnel along with an increased emphasis on basic research—resulted in the creation of the SRC in 1982.

The SRC was the first research consortium created by the SIA.[50] One of the first initiatives addressed by the SRC was the state of semiconductor manufacturing. As Sonny Maynard recalls:

> One of the first things ... when these guys finally did get into one room together and talked about this business of research and what do we need to work on and so forth, it became clear that just doing academic research wasn't going to be enough, that we

[50] In fact, the SRC originally stood for Semiconductor Research *Cooperative*.

> needed to do a lot more in the area of manufacturing. And by '83 or so, "Project Leapfrog" was proposed.[51]

The basis for "Project Leapfrog" was the "Ceres Project," one of the earliest SRC studies; Ceres considered the cooperative development of a 1Mbit DRAM using a sub-micron CMOS process. Ceres envisioned development of many process technologies including electron beam mask making, x-ray and advanced lithography for patterning, low temperature and dry processing technology, and an automated manufacturing process. Bob Burger points out that this proposal was made at the time when 64Kbit DRAMs were being produced in quantity and were viewed as the technology driver of the semiconductor industry. Ceres' stated purpose was to advance U.S. industry from being one generation behind its Japanese competitors to being one generation ahead.[52] Unfortunately, the effort did not receive adequate funding to proceed. Instead, the planners were asked to change the plan from developing a *product* to developing a *process* and Project Leapfrog resulted in early 1984:

> The objectives of Leapfrog were stated as follows:
>
> - to develop a new generation of fabrication equipment for submicron applications on an accelerated time scale so that the equipment will be available two years earlier than normally expected, and
> - to demonstrate that the new generation of equipment is manufacturing-worthy by implementing a prototype 0.5 micron CMOS demonstration/evaluation facility.[53]

Sonny Maynard was at DoD at the time and was a potential backer of the program. He states: "it was called Leapfrog because the idea was let's all collectively put in enough money and people and effort in one place and get one generation ahead."[54] According to Court Skinner, this was "a response to MITI's VLSI program," as the young SRC decided to do something "really big," namely collaborate to build a memory.[55] Colin Knight, former head of research at AMD,

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[51] Maynard interview, op. cit.
[52] Burger, Cooperative Research, 118.
[53] Ibid. Interestingly, the industry faced a similar dilemma almost a decade later when the product-based Micro Tech 2000 initiative was discarded in favor of a process-based SIA Roadmap approach (see Chapter 10).
[54] Maynard interview.
[55] Skinner interview.

concurs with Skinner that Leapfrog was in response to then-understood timing of Japanese technology. He also stated one shortcoming in the approach: "Industry thought they could 'outsmart' Japan by design only, but manufacturing was neglected."[56] Despite an offer from the DoD to fund as much as half of the initiative, the SIA voted against the proposal.[57] Regardless of the technical feasibility of essentially skipping a technology generation,[58] an important consideration at the time was anti-trust. At that time manufacturers could not collaborate to do *products* such as a DRAM in fear of anti-trust violation.[59] Skinner recalls the heavy discussion surrounding Project Leapfrog and concludes that even though the proposal was rejected, the discussion that ensued around what could be done reminds him of later SIA Roadmap discussions.[60]

It is important to review what had emerged in the late 1970s to early 1980s period relative to *industry* technology roadmapping. International competitiveness and, to a lesser extent, national security collectivized concerns and interests in semiconductor technology progress. The Japanese were primarily concerned about their computer industry, while the U.S. concern centered on semiconductors, primarily memory chips. The two were obviously interrelated. R&D activities that resulted all attempted to achieve some date-certain technology targets. The internal practice of technology roadmapping, at least in terms of common goal setting, had taken hold outside the individual firm. The next step was to legitimize the process.

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[56] Colin Knight, telephone interview, June 6, 2000.

[57] According to Maynard, the industry was not quite ready for such a cooperative approach: "I remember Larry Sumney and I and the President's Science Advisor went to an SIA Board meeting and Sumney made the presentation for Leapfrog. I said the government thinks this is a good idea and we'd be willing to put up halves and they said NO. [Why?] Well, there was Charlie Sporck about 3yrs later when we did Sematech. I asked Charlie Sporck, "why now and not 3yrs ago?" He said "we're a lot more humble now" because meanwhile they had a big downturn in that period - had lost another 5 or 10 percent of marketshare."

[58] Jim Meindl, telephone interview, August 16, 1999. Meindl is Pettit Professor of Microelectronics and Director of the Microelectronics Research Center at Georgia Tech. He states that industry has always been skeptical of a "leapfrog" approach (true also later in Micro Tech 2000) because it violates the learning tradition of using knowledge from the current generation as essential learning for developing the next generation. He states that although an aggressive technology target in and of itself is academically sound, industry is used to day-to-day practice in order to achieve it.

[59] Anti-trust law prevented this type of design cooperation of a particular product. In 1984 anti-trust laws were relaxed by Congress with the passage of the National Cooperative Research Act.

[60] Court Skinner, telephone interview, July 21, 2000.

Setting Industry Goals: the SRC Summer Studies

The germ of industry roadmapping formed in 1984 shortly after the Project Leapfrog decision in an activity called the "SRC Summer Study." According to John Carruthers, former Director of Components Research at Intel and one of the original members of the SRC Technical Advisory Board (TAB) Executive Committee:

> The whole roadmapping process actually started with the Semiconductor Research Corporation (SRC). That is something that I did in the early to mid 1980s (1983-1984) with the SRC. We had a roadmap there that went from 1984 to 1994.[61]

Court Skinner, then a TAB member from National Semiconductor, further explains that the origin of the first semiconductor industry roadmap was the first SRC TAB Summer Study meeting in Colorado in 1984. The meeting's purpose was a review of SRC's research goals and mission (long term issues). Skinner recalls:

> It was a typical summer study: end of a long day, we were sitting around and discussing research strategy. There were four or five of us left in the room: Phil Downing from AMD, Jim Daughton from Honeywell, Bob Burger from SRC, myself from National Semiconductor, and maybe someone else. I think Daughton may have been the first to use the term 'roadmap' since that was a strategic planning practice at Honeywell. We liked the term since it captured where we were and where we were going. We were asking ourselves what would happen in 10 years? So we developed a hand-written, one-page "spreadsheet" on an easel that showed 1984-1994 targets for litho dimensions, voltage, feature size, etc. These turned into the 1994 SRC goal set that was the basis for the first strategic plan. You could say this first set of goals was a precursor to the ORTC [overall roadmap technology characteristics] table in the SIA Roadmap.[62]

Larry Sumney, SRC President, described this summer study and its relationship to roadmapping and strategic planning, emphasizing the importance of an R&D strategy for the industry as a whole:

> [T]he SRC is about to step back from its operational activities and attempt to construct a roadmap that will help us to secure our future. By our, I mean the future of the U.S. semiconductor industry. The vehicle for this planning is the SRC "summer study" during which selected members of the Technical Advisory Board ... join the senior technical staff of the SRC for a three-day, in-depth study of an identified issue. Last year [1984],

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[61] John Carruthers, personal interview, November 19, 1999.
[62] Court Skinner, telephone interviews, August 17, 1999 and July 21, 2000. See Chapter 10 for description of ORTC.

> because it was the first such get-together, the issue was the goals and research priorities of the SRC. This year [1985] the subject is R&D strategy for the industry.
>
> At this stage, it is difficult to predict the results of this exercise. At a minimum, we have to identify a straw-man strategy that has sufficient credibility to lead to action... If a roadmap that defines the roles of universities, industry, and government in maintaining global competitiveness in VLSI is created, it may serve to focus enough resources on the challenge to better assure success.[63]

Bob Burger's treatise on the history of the SRC has a chapter entitled "Goals, Roadmaps, and Objectives" where he describes the connection between industry goals and roadmaps:

> There is a very close relationship between goals, roadmaps, and needs. Goals provide the objectives for the research while roadmaps describe the expected pathways for their achievement... Having learned that barriers become goals, the technical challenges described by the SRC provided the first goal-set for the industry while the 'roadmaps' outlined a reasonably detailed set of needs.[64]
>
> The ten-year 1994 goals were accepted for the purpose of guiding SRC research and disseminated through contract reviews, the SRC Newsletter, and presentations at technical meetings. Particularly in the early years when many university faculty and students began participating in SRC's research, the existence of the goals and their nature was welcomed. The university community that participated in the SRC found the absence of technical goals associated with their research support made the research more difficult.[65]

The basic idea of the summer study is interesting in itself as it reflects the important role that industry played (and continues to) in influencing the goals of semiconductor research. Honeywell was one of the first ten companies to join the SRC. Jim Daughton, the TAB member from Honeywell, was an advocate for the idea and hosted a meeting at Honeywell in Minnesota around "the summer of '83 which then resulted in fleshing out the concept of a summer study for the TAB primarily," according to Bob Burger.[66] Burger says that the summer study evolved out of a desire by industry members to better contribute into the SRC technical planning process:

> [The summer study] actually came out of a TAB discussion. We had a technical advisory board meeting and the early members were gathered together and we were discussing their role with respect to the SRC and how they could become more effective. And they volunteered the comments that coming in one day every several months to work with the SRC really didn't give them the opportunity to make the kind of contributions they wanted to make. Therefore, they felt that having a more intensive 2½ or 3 day discussion in the

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[63] Larry W. Sumney, "Strategic Planning and the SRC," *SRC Newsletter*, Vol. 3, No. 7, July 1985, 1.
[64] Burger, *Cooperative Research*, Chapter 6, 54-5.
[65] Ibid., 60.
[66] Bob Burger, personal interview, August 1, 2000.

> summertime would be a way to get more productivity out of the group and focus their attention a lot more strongly on the SRC, and the challenges, and getting it set up and running. And of course this was the time period when the SRC was still being formed, its modes of operation were being determined. Therefore it seemed particularly appropriate so they suggested it and Jim Daughton was a major spokesman for it.[67]

Ralph Cavin, SRC VP of Research Operations, recalls the first goal-setting exercise: "We were trying to set goals for our organization. We were a research company and research companies need to ask themselves how they're going to change the world."[68] Daughton states that a particular problem the SRC membership was wrestling with at the time was planning university research.[69] He says the question "On what basis do we the industry have to tell universities what to do?" was discussed at length. The solution was a form of research roadmap. The idea was to *organize* university research through a "roadmap" versus the traditional "white space" approach to academic inquiry. Thus, the first summer study in August 1984 dealt specifically with this question (see discussion above) and explored what it would take to meet these targets by 1994. Among the global goals for 1994 were:

Functionality:	250X increase in complexity
Performance:	10,000X increase in gate-hertz/cm^2
Cost:	500X reduction in cost/functional element
Process feature size:	0.25 micron +/- 10%

Achieving these and other goals by 1994 would make possible the development of a 256M DRAM (or 64M SRAM) as compared with the 1M DRAM that was in prototype at the time. The overall benefit reflected the common pattern of technology acceleration that was apparent in the VLSI, VHSIC, and Project Leapfrog programs that had come earlier:

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[67] Ibid.
[68] Ralph Cavin, personal interview, August 1, 2000.
[69] Jim Daughton, telephone interview, August 4, 2000.

> The "1994 Goal Set" projects on a ten-year horizon the results from the SRC research program will enable the U.S. Semiconductor Industry to attain capabilities *two years earlier* than would have been possible without this cooperative effort.[70]

Burger reflects later that these goals represented a break with the SRC's early research program. This is consistent with preceding program approaches.

> Most of these [1984] goals are modified extrapolations of technology trends. The modifications provided an acceleration of the pace. These goals are independent of the research program that was then in place.[71]

Regarding the goal setting environment at the young SRC, Daughton was "astounded to see how people eagerly talked about where things were going. From the very beginning, there was general enthusiasm on talking about forecasting the future."[72] There was such open discussion that consensus on the future was reached easily. He also draws the connection with MITI's VLSI program, while pointing out a key difference in approach:

> The precursor to the SRC Roadmap was the MITI Roadmap [VLSI program] which also was a longer-term plan. SRC brought together actual guys doing it like Phil Downing from AMD. There was an open dialogue. This was different than MITI which was more private and guarded secrets tightly. It was pre-competitive technology that pulled together SRC.[73]

Attendance at the first summer study numbered about 20: eight from the SRC staff including all the research program managers and the executive of the SRC, and twelve or so TAB members. In time participation broadened to include members of the Board of Directors, the Government Advisory Committee, and the University Advisory Committee. The summer study became an annual SRC activity that took on a strategic agenda for the organization. Ralph Cavin reflects back on the initial reaction to the first goal set:

> It's really amazing, they were aggressive goals, they were talking about quarter micron technology by 1994 and DRAMs of 256Meg. And you know when I would go around and give a talk on those goals, people laughed. They were almost not taken seriously. It was really interesting. I remember getting up at some major national computer conference

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[70] Larry W. Sumney, "Research Goals for the SRC," *SRC Newsletter*, Vol. 3, No. 4, April 1985, 1. Note the "two years earlier" objective that mirrored the just-canceled Leapfrog proposal; emphasis added.
[71] Burger, *Cooperative Research*, op. cit., 57.
[72] Daughton interview.
[73] Ibid.

> and giving those goals, and looking out at the audience and there was a lot of disbelief on their faces.
>
> We were trying to do research on behalf of this industry. "How do we want to help it change over the next decade?" was the question we were asking ourselves. And so we eventually came up with the ten-year goals. And those things were remarkably good, considering how they were done. They were pretty accurate.[74]

The second TAB summer study was held in August 1985 where the discussion of the goal set addressed expansion of the SRC scope to meet increasing industry expectations. Burger reveals one of the byproduct benefits that roadmaps had greatly provided, namely *communication*:

> With respect to the performance of the SRC, the summer study agreed that the organization's goals were being met but that member company expectations sometimes exceed these realistic goals. It was recommended that the SRC provide more definitive roadmaps for its research in order that improved understanding of the nature of the SRC can be communicated to its members.[75]

Additionally, a key to acceptance of this emerging research roadmapping practice is the critical participation of industry. In 1985 Sumney stated:

> [T]he semiconductor industry has no systematic and complete process that supports technological forecasting. In fact, the desirability for some collective actions in this regard is under discussion, and the limits of such collaboration are not defined. Inherent in any such process is the involvement of enough industry participants so that credible forecasts are obtained, desirable responses are identified, and appropriate follow-through actions will occur.[76]

The third summer study in 1986 in fact focused on research roadmaps. Responding to a request from a member company, the SRC began an effort toward developing a "view" of the semiconductor industry in 1995. Roadmapping was becoming more integral to the operation of the SRC:

> The technical roadmaps that have been the subject of much effort during the past year were presented and discussed... The microstructure science roadmap is built on technology thrusts ... Quarter-micron CMOS is the largest research program, consisting principally of unit process development thrusts. The roadmap plans for process integration in 1989-91. Lithography has been identified as the pacing technology... The roadmap in manufacturing sciences is centered on the 1986 update of the Long Range

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[74] Cavin interview.
[75] Robert M. Burger, "TAB Summer Study," *SRC Newsletter*, Vol. 3, No. 10, October 1985, 2.
[76] Larry W. Sumney, "The SRC and Its Role in the Transition of the Semiconductor Industry," *SRC Newsletter*, Vol. 3, No. 11, November 1985, 2.

> Plan [including] ... the identification of a facility to demonstrate manufacturing technology.[77]

Sumney articulated the use of goals and roadmaps in helping to guide the consortium's research efforts:

> The SRC bases the structure of its industry/ university cooperative research upon goals and roadmaps that define where we want to be in ten years and is allocating its resources to accomplish these objectives.[78]

Perhaps more telling was that the early experience in roadmapping revealed shortcomings in the process, and a call for an "integrated roadmap":

> The roadmaps have demonstrated significant advances in planning, and strong linkages are being established among the three technical areas. These should be strengthened by integrating the roadmaps. [However] [t]here is partial coverage of too many research areas. For efficiency and effectiveness, the SRC must use leverage to the fullest, avoid niches, and find ways to focus its efforts on only the most important technical areas. These would be identified in the integrated roadmap.[79]

The fourth summer study in 1987 addressed goals and roadmaps again, but the primary focus was devoted to Sematech, the new manufacturing research consortium that the SRC had long advocated. In fact, from May to September 1987, Sumney was designated acting head of the Sematech start-up operation. The 1994 goal set was reconsidered according to Edward Hall of Motorola:

> Technical roadmaps have been developed by the SRC. In particular, integration of the research roadmaps has been a key item in 1987... New roadmap requirements are to be defined and should include a risk assessment, including alternate routes for high risk areas... Four years have passed since the SRC goals for 1994 were defined. Now is an appropriate time to assess industry requirements for 2001.[80]

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[77] Robert M. Burger, "Summer Study Report," *SRC Newsletter*, Vol. 4, No. 10, October 1986, 1. Note that the last phrase, "identification of a facility to demonstrate manufacturing technology" refers to the discussions on the Sematech proposal that were circulating at the time. A month earlier appeared a request to "Create a Major Industry/Government Semiconductor Manufacturing Technology Effort."
[78] Larry W. Sumney, "Goals in Microelectronics," *SRC Newsletter*, Vol. 4, No. 9, September 1986, 3.
[79] Ibid.
[80] Summarized in James F. Freedman, "TAB Summer Study," *SRC Newsletter*, Vol. 5, No. 10, October 1987, 1-2.

As Carruthers recalls, "Suddenly around 1987 we looked at this [1984] roadmap and said "Whoa!" this roadmap is really off the mark after three years. We either should not do roadmaps or we should do them better. It was silly. It was put together too quickly."

In preparation for the 1988 TAB Summer Study, Sumney elaborates on the need to revisit the goals:

> The SRC TAB formulated goals for the research program. The research goals now being used were developed in 1983 and 1984 and are directed toward semiconductor device technology capabilities for 1994. These goals were stated in relative terms, e.g., a 250-times increase in functionality of an integrated circuit chip and a 104 increase in functional throughput rate over the capabilities existing in 1984... Research goals serve as the basis for technology roadmaps that identify projected temporal and task parameters. Roadmaps tend to be specific to a technical thrust area, such as the one-quarter micron CMOS, reliability, and bipolar efforts.
>
> The SRC is in the process of defining a new set of goals for its research. These will be directed to the turn of the century, the year 2000. Since research, by its nature, addresses needs that are keyed to applications five or more years into the future, the 1994 goals are approaching the end of their usefulness in planning future research. The 1988 TAB Summer Study agenda includes consideration of the new goals.[81]

The process of replacing the original 1994 research goals was started in the 1988 (fifth) Summer Study. According to J. Richard Burke:

> "Technical Goals for 2001" was introduced at the 1988 Summer Study to initiate consideration of the nature and categories of the technologies, devices, chips, and systems that will be needed beyond the 1994 goal set. This extension of the goals is essential to assure that the SRC Research Program will be contributing effectively to the competitiveness lead of the U.S. semiconductor industry by the turn of the next century... The group recommended that the global goals and roadmaps to achieve these goals be developed during the next year and presented at the 1989 Summer Study.[82]

The 1989 (sixth) Summer Study further examined and refined the now-2001 goals set. Syed Rizvi, on assignment to the SRC as an Industrial Resident from TI projects a wide range of technology targets necessary to achieve broader goals. These are a simplified precursor to Micro Tech 2000 targets and subsequent SIA Roadmap ORTC tables to follow:

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[81] Larry W. Sumney, "Generic Semiconductor Research by the SRC," *SRC Newsletter*, Vol. 6, No. 6, June 1988, 2.
[82] J. Richard Burke, "1988 TAB Summer Study: Initiating Goals for 2001," *SRC Newsletter*, Vol. 6, No. 10, October 1988, 1-2.

> When assessing technology trends, the committee revalidated the SRC Research Goals for 1994 (which had been defined in 1984) in light of developments and made projections for 2001 in the area of DRAMs, Microprocessors, ASIC, Manufacturing, Lithography, and Packaging. The technology push for 1 gigabit DRAM toward the turn of the century predicts the minimum-feature size of 0.15um and will require sophisticated lithography such as X-rays. For microprocessors, the gate delays are projected to be 15 ps with a 200MHz clock frequency. Wafer size will exceed 250 mm. Single-wafer and fab cost is expected to exceed $1 thousand and $1 billion, respectively. Packaging/interconnect complexity will increase in importance and will require 1000 I/O terminals.
>
> In most cases, SRC goals were defined simply by the scaling "up" or "down" of certain parameters. The minimum-feature size, for example, is to be "scaled down" to 0.15um... On the other hand, an increase or "scaling up" of the functional density was projected for the 2001 goal set. The number quoted for 1000 Mbit memory and for logic application are 10^9 and 10^7 devices/cm sq.[83]

According to Burger: "In 1989, when the new SRC research goals took shape, they were largely an update of the 1984 goals... Goals for 2001 were set but before long they would be replaced by the broader goals then emerging."[84] Burger was alluding to two things. First, the NACS Micro Tech 2000 activity that would soon follow was based on stretch goals including Goals 2001. More importantly, the first SIA-sponsored Roadmap (discussed in Chapter 10) which quickly followed Micro Tech 2000 cited:

> The research vision of the SRC, *SRC 2001*, was an important foundation of the SIA [Roadmap] Workshop's efforts.[85]

The SRC held its seventh TAB Summer Study in 1990, "which was the third of these annual meetings that focused on development or realignment of 2001 Goals for the Research Program." Hall articulates the need for a "ten-year, industry-wide, strategic plan" working with the National Advisory Committee on Semiconductors which accurately anticipates Micro Tech 2000:

> A recommendation voiced by several working groups was the need for a ten-year, industry-wide, strategic plan for semiconductors. An action item is for the SRC's working with the National Advisory Committee on Semiconductors (NACS) to include the 2001 goal set and Sematech's competitive analysis information as part of this overall ten-year

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[83] Syed A. Rizvi, "TAB Summer Study: Defining Research Goals for 2001," *SRC Newsletter*, Vol. 7, No. 11, November 1989, 1,4.
[84] Burger, *Cooperative Research*, op. cit., 61.
[85] SIA, *Semiconductor Technology Workshop Conclusions*, 1992, op. cit., iii.

U.S. strategic semiconductor technology plan. Envisioned is a broad, high-level type of document, created by the end of 1991.[86]

It may seem a bit redundant for the SRC to reconsider their long-term goals in the TAB Summer Studies from 1987 through 1990. What is interesting about this exercise is that it became a routine activity to annually review and revise their strategic goals. A decade later, immediately following the publication of the third edition of the SIA Roadmap, the 1997 National Technology Roadmap for Semiconductors, the creators realized that copper metalization, a critical process technology that had just been introduced, had essentially been overlooked in the near-term targets of the 1997 NTRS. So they set out to "update" the Roadmap in a 1998 publication. The Roadmap renewal process, as it is now called, calls for new editions every two years and updates in the between years. Essentially this means the Roadmap is published annually and that the process is effectively on-going. What the SRC TAB realized early on is that things change (e.g., technologies, other key planning assumptions, etc) and technology roadmaps, if useful tools must also change, especially with respect to the cadence of Moore's Law.

Sematech and Strategic Planning [Technology Roadmap] Workshops

Throughout the 1980s several U.S. industries continued to experience international competitiveness challenges, particularly from Japanese industries. Japan's ability to capture significant market shares in stalwart U.S. industries such as automobiles, steel, consumer electronics, and semiconductors as well as semiconductor manufacturing equipment was nothing less than amazing. Several factors contributed to this situation (referred to as crisis by many)[87] including reduced quality and productivity, but also inadequate human resources, skills, and education. Inflation, recession, trade balances, exchange rates, and other economic factors also

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[86] Summarized in Richard LaScala, "TAB Summer Study," *SRC Newsletter*, Vol. 8, No. 10, October 1990, 1-2.

[87] See for example W. Edwards Deming, *Out of the Crisis*, Cambridge, MA: Massachusetts Institute of Technology Center for Advanced Engineering Study, 1982.

played a role. Finally, government policy regarding trade, antitrust, and advanced research and development—particularly in defense—were all in need of reexamination.

Several initiatives were undertaken by or in support of the U.S. semiconductor industry in response to the competitiveness challenge. The SIA, the industry's trade organization, had been formed in 1977 and began to address international trade issues with policymakers in Washington. As just discussed the SIA created the SRC in 1982 to address the problem of inadequate manpower and long-term research in U.S. colleges and universities in silicon-related areas.

In 1984, the National Cooperative Research Act (P.L. 98-462) was passed by Congress to relax antitrust regulations and encourage organizations to undertake joint research too risky to be undertaken by a single firm. One of the major research projects that followed was the creation of Sematech in 1987. Sematech[88] was established as another separate organization under the SIA to address the problem of manufacturing processes, then perceived as the industry's major competitive weakness. Sematech differed from previous developments because it came out of Congressional statute that provided 50% government funding, initially $100 million per year, to support the research consortium which consisted of fourteen of the largest producers of semiconductors at the time. The goal of Sematech was to work on *pre-competitive* research areas that would help the U.S. industry regain its leadership position in the worldwide semiconductor market.

The creation of Sematech was unique in several ways. One that directly pertains to this study is its early adoption of technology roadmapping practices. The activity that served as an early form of roadmaps was a series of strategic planning workshops conducted by the Sematech start-up team starting in June 1987 and continuing until the new organization's move to Austin, Texas in March/ April 1988. The early history of Sematech is thoroughly covered in Browning's and Shelter's *Sematech: Saving the U.S. Semiconductor Industry*, where there is a good amount of

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[88] The Sematech name was derived from *Se*miconductor *Ma*nufacturing *Tech*nology.

discussion regarding these workshops.[89] With this background the author was able to access Sematech archives and contact workshop planners and participants to better understand the significance of these early roadmapping activities. What is of particular interest (and logical in hindsight) is the critical coordinating role that Sematech played in industry roadmapping essentially from its inception. This is later evident in Micro Tech 2000 and most certainly in the evolution of the national and now international industry roadmaps that have since followed. This next section examines the technical planning approach crafted by the Sematech start-up team members when the organization barely existed on paper in a temporary location at National Semiconductor in Santa Clara, California.

For the first ten months of Sematech's existence—most of which occurred *before* the actual legislation authorizing a federal role—a series of strategic planning workshops was conducted around the U.S.[90] These workshops were effectively technology roadmaps (in fact, many were even called that) for the broad array of technical activities Sematech would become involved in. Collectively they represented a more comprehensive approach to an industry-wide technology roadmap than the SRC Summer Studies had thus far achieved. The numbers of participants increased from a few dozen in the SRC sessions to hundreds in the Sematech workshops. This section describes these workshops in more detail along with their significance to industry roadmapping practices. Browning and Shetler provide the following background information:

> On March 10 [1987], a planning task force of thirteen volunteers from ten SIA firms ... was formed to write the [Sematech] operating plan. Called the "Black Book," it outlined Sematech's goals and the organizational, business, and technological strategies for achieving them... It [Black Book] presented a road map for three projected phases of technological achievement, each phase increasing the miniaturization of features on silicon chips... It allotted a five-year federal budget horizon for these phased goals. The three phases corresponded with Sematech's three-stage overall strategic objectives. These objectives, to be achieved by 1992, included recovering global competitiveness, maintaining a globally competitive position, and regaining global leadership in semiconductor manufacturing.[91]

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[89] Larry D. Browning and Judy C. Shelter, *Sematech: Saving the U.S. Semiconductor Industry*, College Station, TX: Texas A&M University Press, 2000.
[90] Sematech authorization became official in late December 1987.
[91] Browning and Shetler, *Sematech* (draft manuscript), 27, 31-2.

Colin Knight, former research director at AMD, was Sematech's first co-COO (IBM's Jack Woods was the other co-COO). Part of the Sematech start-up team, Knight's initial task was to help prepare the first operational plan, the so-called "Black Book" for membership approval. The result was a 5yr plan involving three phases of progressive technology generations (Phase I: 0.8 micron, Phase II: 0.5 micron, and Phase III: 0.35 micron processes) with the overall goal of *catching up with and ultimately surpassing projected Japanese technology advancements* within this timeframe. Knight states that the small start-up group was "thin" technically, consisting mostly of high-level managers, by then some distance from the technology. He says bluntly, "sitting down to tell industry what to do seemed crazy."[92] So he proposed to do a series of *technical* workshops involving engineers and scientists from industry, government, the SRC, and universities. The list of participating organizations went well beyond Sematech's membership. Browning and Shetler emphasize the importance of "rank-and-file" participation in these workshops:

> These workshops were among the earliest activities organized by Sematech's founders. The SIA provided start-up funds for the workshops, which were held not so much to explain the consortium as to pinpoint and gather specific data on the key technical problems in all areas of semiconductor manufacturing. The workshops were designed to accumulate this information from the industry rank-and-file so that Sematech could concentrate on what was actually needed rather than dictate unwanted prescriptions.[93]

According to Hasty, former Research Executive at TI and Sematech's second COO,[94] the original purpose of the Black Book operating plan was to somehow get U.S. industry to learn to manufacture by building things, thus the plan for three separate fabs or "product vehicles" (e.g., DRAM .8, .5, .35 processes). Says Hasty, "The problem was you really couldn't do this unless you started from scratch, but there wasn't enough time or money [for this]." So the alternative was to foster technical workshops and ask industry *how* to achieve the Black Book targets (.5 by 1990, .35 by 1993), trying to determine equipment needs vs. building fabs. While working in a TI plant in Japan, Hasty learned that one of the Japanese secrets to successful chip-making was

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[92] Colin Knight, telephone interview, June 6, 2000.
[93] Browning and Shetler, *Sematech*, op. cit., 39.
[94] Hasty also served as acting CEO between Noyce and Spencer.

very close relationships with their suppliers. He cited a prime example at the time: a new Intel fab that had cost $¾ billion to construct sat idle for 18 months because no equipment was available. This was the bigger challenge that Hasty saw and workshops involving both chip makers *and* suppliers, among others, could start a meaningful dialogue on how to better coordinate technology development.[95]

Knight says that when he planned the workshops he put himself in technologists' shoes "to get hold of something." In other words, he wanted to organize the participants into subsections (of 10-15 people) by specific technologies (e.g., lithography, etch, etc) and really focus on what it would take to meet the process technology targets laid out in the 5yr operational plan. He planned the workshop structure to ensure that participants were not only provided needed background and context, but also that everyone was afforded the opportunity to speak. He also planned in some overlap of related workshops. Most importantly, he needed a way to get feedback and establish a permanent record. The kick-off workshop, held at the Naval Postgraduate School in Monterey, CA, was organized in three weeks and received "enormous" response by many of the industry's best people. A total of fifty people attended. Although 180 were invited, Knight points out that the compilation of 180 names from industry, government, and universities was the first real database of key technologists that "fanned and penetrated the armor" of the semiconductor community. This list only grew with time as word spread and the community became more accessible. Moreover, the Monterey workshop spawned the next 10-15 workshops. From the very start Knight felt the need for a *series* of workshops, but this was not finally agreed upon until the Monterey workshop.[96] Knight's directions to participants briefly explain the purpose of the workshops:

> The objective of these workshops is to develop detailed roadmaps for the development and implementation of technologies required for Sematech to achieve its objective of providing competitive manufacturing technology to the Sematech consortium member companies. The generation of comprehensive roadmaps will require coupling the

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[95] Turner Hasty, telephone interview, May 10, 2000.
[96] Knight interview.

> expertise of the Semiconductor Device Manufacturers with that of the Semiconductor Equipment and Materials Suppliers and the Research and Defense communities.
>
> This workshop is one of a series of Sematech planning workshops, the output of which are development roadmaps for strategic technology required to meet the Sematech goals of transferring competitive manufacturing technology to member companies for 0.5 micron devices by 1990 and 0.35 micron devices by 1993. The roadmaps will be used to develop the Sematech operational plan and these workshops present the best opportunity for your corporation to influence the direction of specific technology developments by Sematech to meet your future needs. The workshops are attended by key technologists from all major semiconductor companies, equipment and materials suppliers, Universities, National and Federal Labs and the SRC.[97]

In an unpublished paper Bill Spencer, then Sematech CEO and Tom Seidel, then Sematech Chief Strategy Officer, state that Sematech itself was developed in large part with the help of this roadmapping process involving a wide range of participants:

> The early planning of Sematech was greatly influenced by a set of industry-wide roadmap workshops... These early workshops were driven by a group of about 20 planners from the future member companies of Sematech; leaders included Turner Hasty who was later to serve as Chief Operating Officer. The first "organizing" workshop was held in Monterey, CA; it provided a global competitive overview and developed guidelines for additional technology roadmapping to reach a competitive technology position for U.S. semiconductor manufacturers by 1990-93. The workshop also identified topics for about 30 detailed workshops.[98]

This is corroborated by Gordon Moore:

> Early in Sematech's formation, its founders organized a series of industry-wide workshops to identify the technological advances required for the U.S. semiconductor and supplier industries to catch up with Japanese industries. The outcome, in March 1988, was a timeline and the specifications for a sequence of technological generations that would lead to parity by 1994 - a "road map for semiconductor technology." The timeline specifications required the demonstration of a 0.8 micron technology in Sematech's new wafer facility in 1989, with further advances to 0.5 micron technology in 1990, 0.35 micron technology in 1992, and 0.25 micron technology in 1994.[99]

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[97] Memo and workshop handout from Colin Knight to Sandy Kane and others, May 22, 1987, Sematech Archives.

[98] W.J. Spencer and T.E. Seidel, "National Technology Roadmaps: The U.S. Semiconductor Experience," paper given at a Chinese conference following publication of 1994 NTRS.

[99] Gordon E. Moore, "Some Personal Perspectives on Research in the Semiconductor Industry," in Richard S. Rosenbloom and William J. Spencer (eds.), *Engines of Innovation: U.S. Industrial Research at the End of an Era*, Boston: Harvard Business School Press, 1996, 173.

Following the Monterey workshop, another thirty or so workshops were conducted.[100] Table 9-2 is a partial list of the early Sematech strategic planning workshops (in alphabetical order).[101]

Table 9-2. Sematech Strategic Planning Workshops (1987/88)

Advanced Lithography	Chemical Vapor Deposition
Chemicals and Gases	D.I. Ultrapure Water
Defect Detection and Reduction	Diagnostic Systems
Electrical Test	Environmental Health and Safety
Epitaxial Silicon Wafer	Facilities
Facilities Overview	In-Situ Process Control
Ion Implantation	Manufacturing Science
Manufacturing Systems	Materials & Equipment for Assembly and Packaging
Metrology and Process Control	Optical Lithography
Passivation, Packaging, and Reliability	Phase 2 Process Architecture Integration
Phase 3 Process Architecture Integration	Physical Vapor Deposition
Plasma Etch	Procurement
Robotics and Automation	Test Vehicles and Testing
Thermal Processes	Transfer of Technology/ Culture
Wafer Cleaning Technology	Wafer Size Determination

Source: Sematech Archives, used with permission

Most of the workshops were completed by the spring of 1988, coincident with Sematech's move to its permanent location. Members of the start-up team as well as experts in at least thirty different technical areas from companies committed to Sematech had conducted the sessions. They assembled and interpreted the data they generated for the consortium to use, sometimes in

[100] The exact number of workshops is uncertain: Browning and Shetler state that 34 were conducted, Turner Hasty recalls 37 separate workshops, and others use an estimate of "about thirty."
[101] "Sematech Strategic Planning Workshop Summary" (partial list), Sematech Archives.

the form of a "technology road map."[102] A small sample of the workshop objectives follows in Table 9-3. Note that some explicitly use the term *roadmap*. Even if the term is not used it is evident that this is what they had in mind.

Table 9-3. Sample Sematech Workshop Objectives

Workshop	**Objectives**
Optical Lithography	- Evaluate current capabilities in exposure tools, photomasks, resists, and metrology. - Estimate future capabilities, addressing specific areas where improvement is needed in order to meet Sematech goals.
Passivation, Packaging and Reliability	- Develop *roadmaps* for passivation, assembly processes, packaging systems and reliability for a mixed device and variable quantity manufacturing environment.
Physical Vapor Deposition	- *"Roadmap"* the requirements for, directions of, and issues associated with the technology, manufacturability, equipment and metrology for the physical vapor deposition of metals in a "4 layer metal" system - Identify the issues to be resolved in cooperation with other working groups.
Wafer Size	- Define current characteristics of the state of the art of 200mm wafers and the requirements for phase II (1990). - Identify known and potential problem areas in the manufacturing of wafers for phase II requirements.

Source: Sematech Archives, used with permission, emphasis added.

Perhaps most evident is not in the use of text, but in the use of *charts and other graphics* to portray a roadmap. Figure 9-2 is taken from the workshop report on advanced lithography and resembles the familiar format of roadmaps that would follow.

[102] Browning and Shetler, *Sematech*, op. cit., 40.

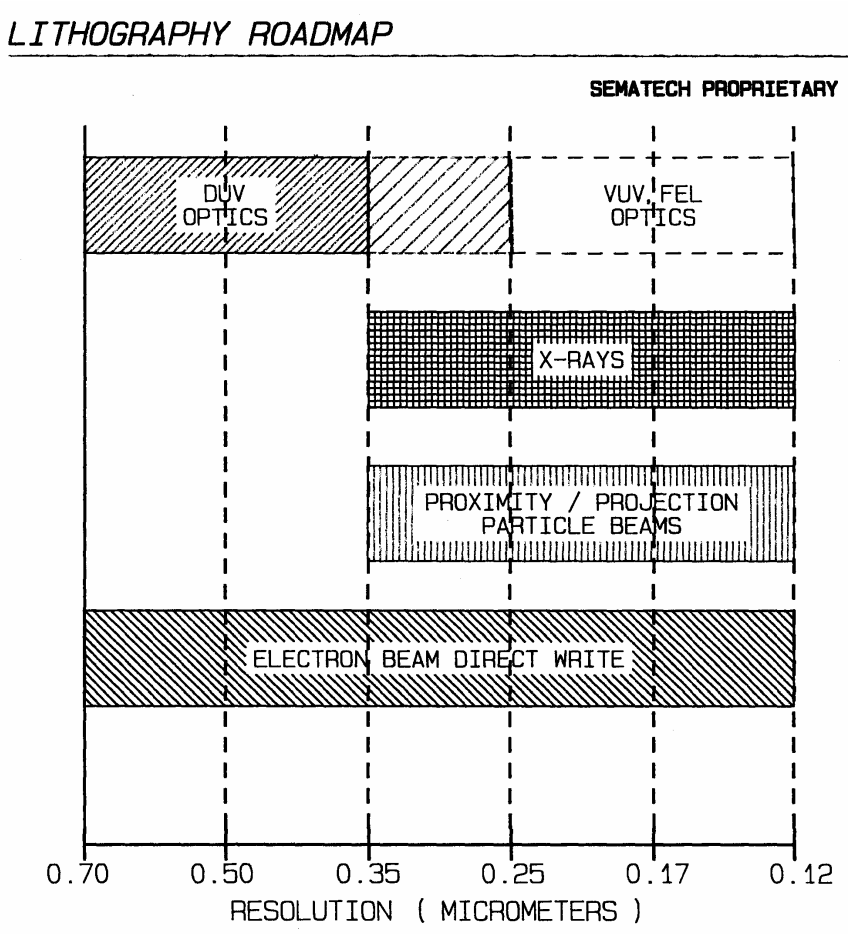

Figure 9-2. Sematech Workshop Advanced Lithography Roadmap

Source: "Final Report: Sematech Planning Workshop on Advanced Lithography," Burlingame, CA, January 25-27, 1988, Figure 2, 11, Sematech Archives, used with permission.

A most telling result of these early activities is revealed by a participant who completed a questionnaire (anonymously) at the end of the *Wafer Size Determination* workshop. The participant offered these additional comments:

> "Before the meeting, I had doubts whether SEMATECH was [a] viable idea. The openness and discussions have convinced me that the number of companies are willing and SEMATECH will work."[103]

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[103] "Summary of Feedback Questionnaire," in Sematech, "Final Report: Sematech Planning Workshop on Wafer Size Determination," Dallas, Texas, August 10-12, 1987, Sematech Archives, used with permission.

By "openness" the participant echoes what others in this particular workshop also acknowledged—specifically how much IBM contributed in knowledge and experience with three years of processing 200mm (8-inch) diameter wafers. IBM had led the industry in 200mm wafer development in the early to mid 1980s and most others had not yet converted to 200mm tools. In fact, the purpose of this particular workshop was to plan availability of 200mm wafers for Sematech Phase 2 (1990). So sharing leading-edge knowledge among competitors (i.e., AMD, ATT, Intel, National, Harris, HP, Motorola, and TI also attended) and suppliers (i.e., General Signal, Applied Materials, Varian, Perkin-Elmer, and KLA were in attendance) helps explain the participant's comments. Broader benefits of the workshops are summarized by Browning and Shetler:

> Besides developing Sematech's technical agenda, the workshops provided a valuable forum for sharing ideas - something that had never been available, or even possible, before the new level of antitrust protection. The workshops publicly signaled a new era of cooperation. They brought together people who ordinarily had no chance to meet and provided a noncompetitive arena for discussing common problems and working out potential solutions.
>
> The workshops also helped attendees understand what technical problems they shared before they attempted to develop solutions. In fact, the workshops inspired Sematech's first comprehensive roadmaps correlating the collective technological needs of various sectors of the entire industry with programs that addressed them, and their projected timetables. For many rank-and-file industry members, the workshops and their resultant road maps were the best thing to come out of the start-up period. As [Sam] Harrell recalls: "Those were working sessions which drove to some conclusions about the needs and requirements of the industry and what was most likely alternatives to meet those needs and requirements. Those were very powerful interactions that had never been able to happen before."
>
> The workshops began providing an immediate and important leveraging effect to the young consortium even before the organization was officially in place. Says Harrell: "They empowered enormous amounts of investment to get focused on those problems. Sematech's [proposed] $100 million from the government and $100 million from industry was peanuts compared to what the industry spends on its own balance sheets. Suppliers alone spend $1.4 billion a year on RD&T [research, development, and testing]. The member companies spend $6 to $7 billion a year on RDT&E in a comparable basis. What the strategic workshop road maps did was to set in motion a bunch of focusing activities of $8 or $9 billion worth of effort, not just $200 million worth of effort."[104]

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[104] Ibid., 41-2.

> The workshops produced other benefits. Two unifying effects on Sematech assignee morale during the Santa Clara[105] period came from the ongoing technology workshops, as recalled by one observer: "They [the workshops] were the ideal team-building exercise. First, they provided a well-defined work schedule, outlining tasks on which assignees could work together without being concerned about their need to push company agendas or protect company secrets. Second, in providing a public forum on the issues, they also provided the catalyst for nationwide support for the idea. This support, garnered from industry, government, and the universities proved to be very important in establishing the worth of Sematech."[106]

In a section entitled "Road Mapping Shows Gaps," Browning and Shetler state: "Creating road maps that integrate information about all the pieces necessary for future manufacturing was becoming an increasingly important strategic tool for many businesses at this time." One of the chief findings of the workshops was that the chipmakers' biggest headaches stemmed not only from technological problems but more from difficulties with suppliers. The unanimity of their response was striking to the surveyors.[107] In relation to this, what was emerging was the need to synchronize "cadence" of technology development. In its own planning, Sematech realized that its member companies would not be able to use its Phase I-III submicron technology if U.S. equipment development failed to closely coordinate suppliers' tools and manufacturing processes with advances in chip design. For Sematech to be successful, they needed to both lead and be in step with the industry, rather than become isolated from real-time commercial urgencies. A footnote refers to the importance of the supplier industry to be in synch with device makers:

> The 1990 Advisory Council Report stated flatly: "The task of restoring independence is not only a matter of developing world-class manufacturing technology. It also involves restoring or sustaining the commercial strength of financially pressed U.S. equipment and materials suppliers. To meet the latter requirements, new or improved equipment and materials must be developed *in phase with chipmaker's purchasing cycles* for the next two generations of semiconductor device technology ... reflected in the time lines for Phases 2 and 3."[108]

Following the technology workshops in Sematech's early days, Roadmaps began to become common practice at the consortium:

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[105] Sematech started in Santa Clara, CA in a facility provided by National Semiconductor and remained there until the Austin, TX facility was completed in 1988.
[106] Browning and Shetler, *Sematech*, op. cit., 67.
[107] Ibid., 100.
[108] Quote by Mayer et al., Advisory Council Report [emphasis in original] in Browning and Shetler, op. cit., 108.

> Research done by the early PFTQ [Partnering for Total Quality] task force had shown the importance of technology road maps that could demonstrate the simultaneous coordination of multiple interactions among chip makers and suppliers. Sematech began to use such road maps more extensively. They were similar in nature to those created in the 1987-88 planning workshops.
>
> Tom Seidel ... became the consortium's chief technologist and was charged with overseeing much of the road-mapping activity. Technology road maps, he says, relate many elements - such as R&D, training, and equipment, resources - that act on each other. The maps include time as a critical dimension by shoeing anticipated windows of technological and equipment opportunity, as well as the schedules and required deadlines to make it all work together. These maps not only coordinate efforts, they demonstrate how the output from one area becomes the essential input of another in order to leverage their strengths. Eventually, Sematech's technology maps would show cost and market factors as well... With road maps from different levels, Sematech's competitive analysis could evaluate the consortium's projections against both the industry's future and the global picture.
>
> In the previous atmosphere of proprietary secrecy, when chip makers and their U.S. suppliers experienced problems, it was easy for them to blame each other, each firm thinking its problems were unique, and not wanting to expose its difficulties to rivals. However, cooperative road mapping laid out the problems and interdependent strategies for the consortium, and everyone had to face up to their responsibilities and determine what they could do to improve the situation. Road maps also continually reminded them that not everything could be done at once with the resources available.[109]

Finally, in a section entitled "The Importance of Road Maps," Browning and Shetler draw the following conclusions regarding roadmaps at Sematech:

> In retrospect, we can see how the consortium had used road maps from the very beginning as an ongoing aid to its own internal cooperation - from Obi Oberai's first consensus-building agenda road map, to the ones used to coordinate joint equipment improvement and development projects. Road maps had been used to help coordinate the consortium's ongoing PFTQ efforts with suppliers and were the basis for the 1991 planning for Sematech II. Later still, the consortium had begun participating externally in developing road maps for the larger industry picture, such as the ... Microtech 2000 road map of April, 1991.[110]

From someone who played an active role in the management of the workshops, Hasty views the early Sematech workshops as very important for several reasons. First, they were the basis for the immediate plans for the various processes in manufacturing that was Sematech's initial priority (i.e., technical roadmaps). Secondly, the workshops were an early opportunity to *work together* in a non-threatening manner. "They turned a chaotic situation into working as a team" says Hasty. Third, they helped develop national support for the Sematech cause. By including

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[109] Ibid., 135.
[110] Ibid., p155.

universities, DoD, and DoE, everybody "got their say" and he emphasizes, "The workshops were amazingly successful in getting a national voice." Finally, Hasty sums up in an almost philosophical sense: "Roadmaps are good practice, they keep people thinking."[111]

National Advisory Committee on Semiconductors (NACS) and Micro Tech 2000

As stated at the beginning of this chapter, most refer to Micro Tech 2000 as the origin of semiconductor industry roadmapping. Technically this is correct, but there had been almost a decade of industry-type roadmapping activities preceding the Micro Tech 2000 Workshop in 1991, a product of the National Advisory Committee on Semiconductors (NACS), established by Congress in 1988 to "devise and promulgate a national semiconductor strategy." The committee, which included leaders from both industry and government, published a series of recommendations for strengthening the nation's semiconductor industry. The first annual report issued by NACS, *A Strategic Industry at Risk*, was published in late 1989 and discussed the competitive challenges then facing the U.S. semiconductor industry. In addition to the three required annual reports, NACS also undertook studies of segments of the industry that were of particular concern. These included examinations of the critical semiconductor equipment and materials industry as well as the high-volume electronics industries that had both increasingly become less American-owned. The final special study/report published by NACS was *Micro Tech 2000 Workshop Report: Semiconductor Technology Roadmaps.*[112] Micro Tech 2000 was an attempt to chart a technology strategy over the decade of the 1990s with an end goal of achieving a significant technical target by the year 2000. The objective was not only to match the Japanese technical superiority at the time, but surpass it. It was commonly believed that the U.S. industry technologically lagged the Japanese by one or two years as a result of a slower pace of technology advance. Thus the goal of the Micro Tech 2000 initiative was to increase the U.S. pace to where it was one-third faster than that of the Japanese, and operate at this accelerated

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[111] Turner Hasty, telephone interview, May 10, 2000.
[112] National Advisory Committee on Semiconductors, *Micro Tech 2000 Workshop Report: Semiconductor Technology Roadmaps*, August 1991.

pace for the next decade. Achieving this goal would be an ambitious undertaking and one requiring massive resources that did not presently exist. The drill was basically to determine what it would take to achieve such a target. In other words, develop a roadmap to achieving a specific technical target by the year 2000. To accomplish this it was clear that broad participation was required.

John Armstrong, NACS industry member and then-Vice President for Science and Technology at IBM, originated the idea for Micro Tech 2000. He said in a press release announcing the initiative: "The general idea is to see what is an appropriate technology goal which can accelerate the development of advanced technology ... by the year 2000." The hope is that research institutions will soon lay out a "road map for cooperation."[113]

In April 1991, NACS and the White House Office of Science and Technology Policy (OSTP) cosponsored a workshop that brought together ninety representatives of U.S. semiconductor manufacturers, equipment makers, materials suppliers, private research institutions, universities, and Federal Government agencies and laboratories to help create an aggressive set of technical roadmaps for U.S. semiconductor technology development over the next decade:

> The primary task assigned to the Micro Tech 2000 Workshop participants was to create technical roadmaps that, if followed would contribute to the U.S. semiconductor industry's efforts to develop advanced technology throughout the next decade, and that would help propel the industry to world leadership position by the year 2000. *The objectives of the workshop were to determine if the Micro Tech 2000 technical goal of developing a competitive 0.12 um semiconductor manufacturing process ahead of current forecasts is feasible, to identify the most critical efforts that should be undertaken to develop the manufacturing process and to produce engineering samples of a product using the process, and to determine when resources would have to be made available to reach the goal by year 2000.*[114]

The Micro Tech 2000 Roadmap process borrowed heavily from previous roadmap exercises developed both at the SRC and Sematech in the early development of their technology goals and strategies as previously discussed. Recall that the SRC and Sematech roadmapping processes

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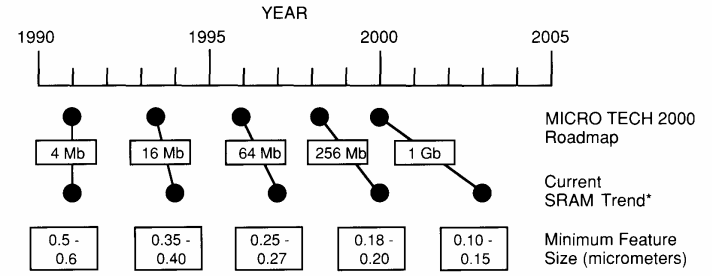
[113] Evelyn Richards, "Industry Effort Aims to Keep Lead in Semiconductors," *The Washington Post*, Feb 21, 1991.

[114] Ibid., iii, emphasis in original.

were brought by consortia member companies such as Motorola, IBM, Texas Instruments, Honeywell, and others. The outcome of the workshop was published in August 1991 and included the roadmaps shown in Figures 9-3a and -3b and Table 9-4. Note the similarities in lithography roadmaps shown in Figure 9-3b as compared with Figure 9-2 previously shown. Given that 1Mb SRAM chips were in volume production at the time and the next generation 4Mb designs using 0.5 micron minimum feature sizes had just been introduced, traditional scaling would have put the 1Gb and 0.12 targets out at least twelve years (four 3yr device generations) to 2003. Thus, Micro Tech 2000 called for significant acceleration well beyond the current capability of the industry. The targets were achievable, but experts estimated it could require as much as $1 billion in additional funding to achieve. Ian Ross, NACS Chairman and then-President of AT&T Bell Laboratories, said the program would be "bigger than Sematech," whose budget was about $200 million a year. He said developing an advanced chip like the one envisioned would cost billions of dollars over the next decade. Indeed, he likened the initiative to the Apollo space program of the 1960s.[115]

Figure I-1. MICRO TECH 2000 Engineering Samples Roadmap

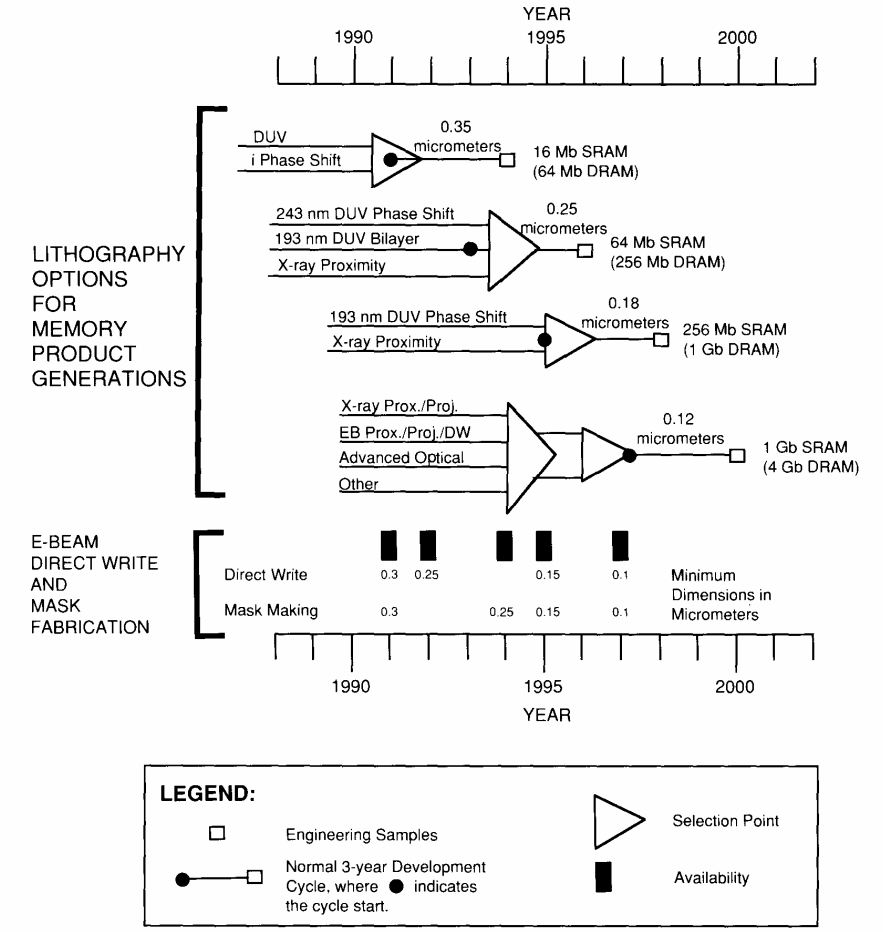


* The SRAM trend is based on the historical pace of memory development, where a new product generation has been developed every 3 years.

(a)

[115] See Andrew Pollack, "Apollo-Type Program Is Envisioned for Chips," *New York Times*, Feb 21, 1991, Business Section, 2, and George F. Watson, Alfred Rosenblat, "Advisory Committee Report: 'Apollo'-type program for chip industry proposed," *The Institute: Inside IEEE*, Vol. 15, No. 4, April 1991, 1, 8.

Figure II-1. Lithography Roadmap



(b)

Figure 9-3. Micro Tech 2000 Engineering Samples and Lithography Roadmaps

Source: NACS, *Micro Tech 2000 Workshop Report*, August 1991. Figure I-1, 6; Figure II-1, 11.

Table 9-4. Micro Tech 2000 SRAM Architecture Roadmap

Year Required	*1993*	*1996*	*1998*	*2000*
Maximum density	16Mb	64Mb	256Mb	1Gb
Minimum design rules (um)	0.35	0.25	0.18	0.12

Source: Ibid., Table II-5, 31.

On balance, the workshop report received mixed reactions. Researchers were generally pleased with the outcome, however the industry generally felt the timetable was not feasible, especially lacking the additional resources necessary to achieve the accelerated schedule. Probably the most important response was a general consensus that the roadmap exercise was useful. Here are a few of the documented assessments of Micro Tech 2000 by key members of the semiconductor community:

> The workshop report was widely circulated and created a great deal of discussion by the U.S. semiconductor industry. There was a general sense that the technology could be accelerated. There was a question by the industry as to whether the economics of the acceleration were worthwhile.[116]
>
> Although this Roadmap found limited acceptance because of its focus on a single product capability, it demonstrated the roadmap process and provided a pattern for the next step which followed in less than a year.[117]

The "next step" referred to above was the inaugural SIA Roadmap that followed almost immediately. One obvious reason why the industry generally rejected the timing of Micro Tech 2000 was lack of funds—the industry was recovering from one of its cyclical downturns and the federal government was not going to assist in the initiative (e.g., the NACS charter would soon expire). The other argument has been discussed already regarding attempts to jump or "leapfrog" a device generation in order to accelerate the pace of chip technology. This interferes with the learning tradition in chip development—namely that one learns to develop the next generation based on the experience from the previous generation. Although theoretically possible, the engineering and manufacturing communities making the products argued that disrupting this tradition was unrealistic. Some from industry recall the unrealistic nature of the proposed leapfrog development approach, referring to it as an "absurd" idea possibly costing the industry a billion dollars it did not have. Interestingly, Armstrong reminds us of another important consideration:

> A leapfrog approach was the only way at the time to get competitive people in a room together to work on something because it wasn't perceived as collusive, had a longer-

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[116] Spencer and Seidel, "National Technology Roadmaps: The U.S. Semiconductor Experience," op. cit..
[117] Jim Glaze, Owen Williams, Tom Seidel, and Bob Burger, "The National Technology Roadmap for Semiconductors," unpublished paper, approximately early 1995.

> term horizon, and also was a bold and challenging goal looking 8-10yrs into the future. It was good fit for researchers.[118]

Tak Ning, IBM scientist, who worked for Armstrong at the time and participated in the Micro Tech 2000 workshop, echoes this view: "Research roadmaps are somewhat different than product roadmaps. Research roadmaps usually don't try to take such small steps. You take big steps and Micro Tech 2000 was one of the big steps."[119] The Micro Tech 2000 Roadmap and those that had preceded it were primarily planning exercises by researchers. Although engineers, developers, and indeed some manufacturing people participated in these early roadmaps, there was a basic research objective: can it be done? The demographics[120] of the 90 Micro Tech 2000 Workshop participants was as follows:

industry	38	42%
government	17	19%
universities	11	12%
consortia	11	12%
consultants/NFPs	8	9%
national labs	5	6%

A closer examination of the industry participants reveals that many were probably from research labs or departments of their companies. Furthermore, about 60% of all participants held PhDs. This further underscores the research emphasis of the workshop.

However, the fact that the exercise stimulated much technological curiosity, even confidence, helped build the consensus that Micro Tech 2000 was a very worthwhile technology planning exercise. Again, probably its biggest achievement was demonstrating that a collaborative activity that involved the broad network of the semiconductor community—including fierce competitors—could work.

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[118] John Armstrong, telephone interview, January 23, 2002.
[119] Tak Ning, personal interview, July 18, 2000.
[120] Classification by Bob Burger in post-workshop briefing.

Meanwhile, NACS was a three-year committee activity that would end in early 1992. So in late 1991, in preparation for its third and final annual report, NACS asked the SIA to take over some of its activities, including the implementation of the Micro Tech 2000 workshop report. The SIA accepted responsibility for the Micro Tech 2000 vision at its October 1991 meeting. The SIA had recently formed a Technology Committee under the leadership of Gordon Moore, then Chairman of Intel, who recommended the formation of a team to fully assess implementation of Micro Tech 2000. Moore was also an invited member of NACS and very familiar with Micro Tech 2000 as a key participant. As SIA Technology Committee Chair, Moore chartered a task force as follows:

> A group is chartered to determine how aspects of Microtech 2000 plan can be used to integrate the efforts of Sematech and SRC and other semiconductor research and development activities to assure U.S. manufacturing leadership in semiconductors.[121]

Interestingly, the focus of this evaluation would be *manufacturing*, not technology:

> The Technology Committee is convinced that the problem is not technology "per se," but the ability of U.S. producers to bring products and processes to the necessary levels of world manufacturing competition. The real question at this juncture is to determine if the SIA-sponsored activities in Sematech and SRC are sufficient.[122]

According to Moore, Intel had used internal roadmaps for some time (like many other companies) so he transferred the planning process to the SIA Technology Committee and Micro Tech 2000 follow-on efforts. The SIA Technology Committee saw the opportunity to use Micro Tech 2000 as a starting point for a comprehensive industry roadmap as *the* guiding plan to cover both Sematech and SRC research needs. A longer horizon was needed; one based on 3yr device generations made sense for industry to look out about 5 generations. Company roadmaps usually had much shorter focus (2-3 generations). Micro Tech 2000 had covered 5 generations but had accelerated the timeframe. Furthermore, with an industry-wide roadmap in place, the SIA could effectively respond to the federal government's request of the industry to "speak with one voice"

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[121] Enclosure #1 of SIA memo from Gordon E. Moore, Chairman of the SIA Technology Committee to SIA Board of Directors, November 21, 1991.
[122] Ibid.

regarding technical needs. The SIA had built its reputation in Washington as an organization that effectively represented one industry in trade issues, thus it only made sense to do the same regarding technology.[123]

Considerable planning and preparation went into the follow-on effort of Micro Tech 2000. Another workshop would be convened in 1992. The purpose, format, and structure of the upcoming workshop were formulated. It is clear that one major goal of this new effort[124] would be to consolidate the work of previous roadmapping efforts (i.e., SRC, Sematech, and Micro Tech 2000) to enable SIA to more clearly articulate a single technology strategy. It is also evident that this would be a continuous process:

> The purpose for this document is to describe the process whereby a single consistent position for all SIA activities on the evolution of the semiconductor technology will be developed. To that end this document will combine the efforts of the Science TABs of the Semiconductor Research Corporation, the Focused TABs of Sematech, and the Microtech 2000 workshop. The result will be a single strategy, identified needs, set of roadmaps which cover the entire spectrum of technology used in the design and manufacture of semiconductors. These roadmaps are to be updated annually.[125]

From this point forward semiconductor industry technology roadmaps would enter a new era where they served national and ultimately international needs. This line of analysis will be continued in Chapter 10.

Discussion: The First 15 Years of Roadmaps

This chapter's focus is the period of the mid 1970s to about 1991 during which time technology roadmaps clearly emerged within the semiconductor industry. This analysis reveals several major themes from this first 15yr period that are instructive as the technology roadmap process became more widely accepted. These themes are discussed in the following paragraphs.

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[123] Gordon Moore, telephone interview, February 11, 2002.
[124] An interesting note is that the new initiative was referred to briefly as "Microtech 2001" as an obvious follow-on to its predecessor but also consistent with SRC 2001, that organization's strategic plan. The Microtech 2001 name only appears once in historical documents.
[125] "SIA Consolidated Roadmaps: The Planning Methodology," (fax dated 7/14/92 from Motorola External R&D), author unknown.

Origin/ Source of Roadmaps

Although the exact origin - the "first roadmap" if you will - remains a mystery, what has been shown is that there are early identifiable sources of use, particularly within the U.S. Government. This may be the case simply because there exists a better documentation trail, at least for defense-related programs that were public knowledge. Examining Motorola's roadmapping practices as a representative case study suggests that profit-seeking firms also realized the technical and economic benefits of this new technology planning technique. Informants from several other companies (e.g., IBM, TI, Intel, and Honeywell to name a few) had also indicated that roadmaps were used within their firms during this time, but these were rarely documented for public interest since they were used for competitive advantage. The growing concerns with international competitiveness and, to a lesser extent, national security provided the common ground for roadmaps to be shared. The VHSIC program is one example of a very possible connection where government and industry were mutually interested in roadmapping within the defense semiconductor community. Government/ Industry cooperation is also evident in energy and automobile sectors, and later in the commercial semiconductor sector. This is consistent with earlier findings that crisis serves as a catalyst to roadmapping.

Another related observation is that the practice started in the domain of research & development. This is evident in the Motorola case and especially in the SRC and Sematech consortia early planning activities and later in Micro Tech 2000. It is also an area where non-competitive - later called pre-competitive - activities can be conducted. Relaxed anti-trust rules would eventually allow roadmaps to be used in operational areas, but initially they seemed to emerge from research.

Although research-driven, the historical literature suggests and informants emphasize that roadmaps were adopted by industry because they proved to be a simple yet useful tool. Other than gathering the necessary participants, they were not difficult to do. Creating a roadmap was almost intuitive as seen in the SRC 10yr goal exercise or the Sematech workshops. This "no

instructions needed" approach suggests the increasing acceptance over this period. Of course the process would become more formal with time, but the initial roadmaps just seemed to "happen."[126]

Roadmapping as "Organized Innovation"

One theme that repeatedly appears is that a roadmap focuses effort, resources, or activities in some particular direction (destination). Similar terms like organize, synchronize, align, and coordinate were all mentioned in the literature or by informants as a descriptor for roadmaps. In the semiconductor case roadmaps are very much goal-oriented. Examples are date-certain technology targets based on process feature size or product density/ capability (e.g., VLSI, VHSIC, Ceres and Project Leapfrog, SRC's 1994 Goal set, Sematech Phases I-III, and Micro Tech 2000). In some cases, the first goal is to actually set the goals as in VHSIC and the SRC Summer Studies. In other cases (and in follow-up to the initial goal-setting exercise) the task is to take established goals - as in Sematech's initial 5yr plan phases - and develop roadmaps to achieve them. Certainly in corporate applications like Motorola, product development goals are paramount. In all cases, the major point is that there is a common understanding of roadmap goals. Further, roadmap goals or targets need to be measurable to be of any use. Again, this was the situation in all non-DoD cases described in this paper, particularly with regard to the SRC, Sematech, and Micro Tech 2000. Finally, the roadmapping process helps validate, refine, and give credibility to goals.

In every case, time (temporal dimension) became the main variable to measure performance against. Roadmaps drawn on a two-dimensional axis quickly became gauges for benchmarking. Once the future path of the technology's trajectory - or "scaling" - was understood, then a roadmap was developed to accelerate the pace (sometimes without much thought). As firms and industries alike began to realize this, this led to a propensity toward technology acceleration and

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[126] Moore interview, February 11, 2002.

terms like "skip" or "leapfrog" became commonplace, especially in the earlier days. Interestingly, this behavior continues today as firms continuously attempt to "beat the roadmap" to remain competitive.

Strategic and Systematic Approach

Roadmaps, coming mainly out of the research community, had a longer-term planning focus than most were familiar with at the time. In the 1970s the integrated circuit segment of the semiconductor industry was still in its formative stages leaving little time or desire for long-term planning. Roadmap time horizons were typically 5 or 10yrs, or longer. Thus this was a strategic planning approach that stretched the sights of operational types. This "beyond the next generation" focus also helped garner higher levels of collaboration as common problems and needs became obvious to all.

In the Motorola case in particular, upper management support was a key ingredient to the success of roadmapping. The commitment on the part of Bob Galvin and his executive team resulted in a process that permeated the company to the point that it eventually became part of its culture. A related aspect of this that departed from traditional technology planning efforts was the thorough and systematic approach taken to planning. Again, this was very evident in the Motorola case - a more formalized review process was needed, and one that was reviewed systematically (e.g., the RMTR). This was a much more complete approach, involving supporting technologies and other factors critical to the success of the technology in question. The comprehensiveness of the thirty or so Sematech workshops that followed the Monterey workshop is further evidence of this point.

Finally, developers and users of roadmaps realized that a roadmap was much more than a date-stamped chart that was prepared and periodically looked at but not revised. As the SRC TAB learned only a few years into their summer studies planning exercises, the 10yr goals and their roadmaps were not simply one-time extrapolations, but living instruments needing on-going

examination and revision. Motorola's RMTRs and later ITRS updates essentially meant that roadmapping, if done well, is an on-going process.

Broadened Scope and Process Commonality?

Continuing with this last point (on-going process) and expanding a bit further, this early history suggests an evolutionary nature to roadmaps and roadmapping practices. One can almost imagine the first Motorola roadmaps as not much more than a simple one-page chart of a particular technology's capability vs. time (also recall the first SRC 10yr goal set). A decade later roadmapping had become a company-wide process at Motorola with significantly more sophistication, detail, and support resources. The scope had broadened, thus the roadmapping process had to become more standardized to be of corporate value. As roadmapping evolved from company to industry levels in particular, there is little doubt that sharing of company roadmapping practices brought even more standardization or commonality in processes and methods. It is quite possible that a hierarchical design emerged, even unintentionally. Member companies supporting the SRC or Sematech would naturally want to coordinate their technology plans (roadmaps) with whatever industry roadmaps were under development at the time. There is some anecdotal evidence from informants that roadmaps became more common over time, but this is an area that deserves further research. This, however, is consistent with the suggestion that roadmapping was a logical step as the industry matured. It also appears that the semiconductor industry is the first major industry sector to employ an *industry* roadmap.

Communication Tool

One of the byproducts that upper management and roadmap participants alike refer to repeatedly is the great benefit of roadmaps as a communication tool. First, the process affords an opportunity for many different players, especially the "rank-and-file," to work together, share knowledge, and contribute to the roadmapping effort. Motorola's RMTRs and the Sematech workshops illustrate this. This can also have motivational benefits that an otherwise top-down

form of technology planning may not offer. In addition to the sociology of the process, a technology roadmap makes public the important tacit knowledge of the technologists involved in the process that otherwise wouldn't be explicated. A published roadmap becomes an intra-organizational record enabling all readers to commonly understand its direction and how each might fit into the bigger picture. And as Turner Hasty points out, a roadmap can also give an organization an important "voice" to the public at large. As just one example of this, communication (or sharing) of roadmaps externally to suppliers, customers, or other semiconductor community members has become an integral part of strategic and tactical planning within this industry. Finally, if there were one word that summarized the overall usage, benefit, or purpose of roadmapping, it would be that the roadmap process provides a *dialogue* or *discussion* of key technology challenges that will be faced "down the road."

PART THREE: ITRS CASE STUDY

CHAPTER 10: The International Technology Roadmap for Semiconductors—A Decade of Industry Roadmapping[1]

"If we can stay on the SIA Roadmap, we can essentially stay on the [Moore's Law] curve. It really becomes a question of putting the track ahead of the train to stay on plan."

- Gordon Moore[2]

"That's where I see roadmaps really being applied and used effectively, and with benefit. And it's tremendously important here because you need the whole infrastructure to come with you. This is the *value* of roadmapping."

- Randy Isaac[3]

"You cannot have a document live in this industry for two years."

- Paolo Gargini[4]

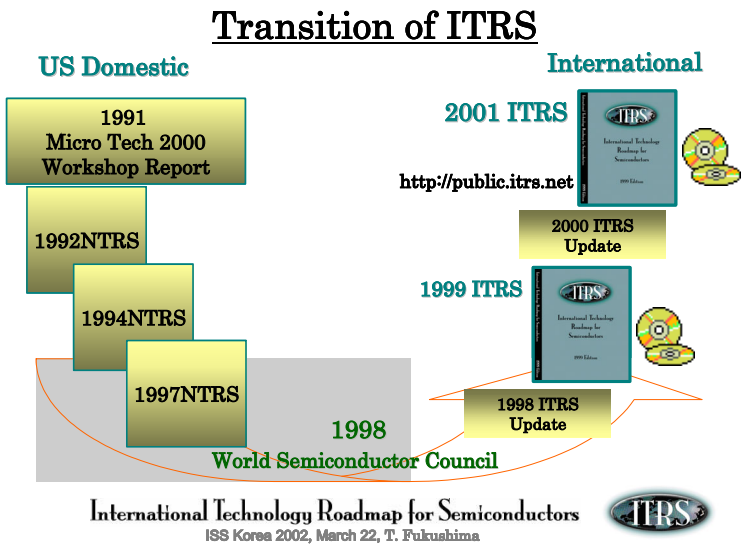

Figure 10-1. NTRS to ITRS Transition

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[1] The author is indebted to Ms. Linda Wilson of International Sematech who contributed substantially to this chapter.
[2] Ed Korcynski, "Moore's Law Extended: The Return of Cleverness," (interview with Gordon Moore) *Solid State Technology*, Vol. 40, No. 7, July 1997, 364.
[3] Randy Isaac, personal interview, July 18, 2000.
[4] Paolo Gargini, quoted in Robert Lineback, "Roadmap can't keep up, may need annual update," *Semiconductor Business News*, December, 1998.

Source: Toshitaka Fukushima, "An Overview of the ITRS 2001," manuscript. Note that Fukushima is General Manager, Fujitsu Ltd. and IRC member 1999, 2001 ITRS. He also participated in the ITRS survey conducted by the author.

Introduction

The year 2003 heralds a full decade of technology roadmapping for semiconductors by the Semiconductor Industry Association (SIA). Often used as a model for industrial roadmapping, the recently published *2003 International Technology Roadmap for Semiconductors (ITRS)*[5] marks the sixth edition of the SIA Roadmap process that began with the publication of the first industry roadmap, *Semiconductor Technology Workshop: Conclusions and Working Group Reports*, developed in 1992. The significance of the 2003 ITRS is acknowledged by many involved in its creation:

> Thus, the 2003 edition covers the years 2003 to 2018. The 2003 ITRS might well be considered the 10th anniversary edition, since completely new full-text versions have been issued in 1992, 1994, 1997, 1999, 2001, and now, 2003.[6]

The ITRS and the series of industry roadmaps that preceded it have traversed several generations of device families despite advancements or delays in processing innovations or product announcements, market downturns, and pervasive technical challenges of the global semiconductor community. The ITRS enables the identification of pre-competitive solution sets serving the entire infrastructure of chip manufacture. The research community, chip designers, R&D consortia and institute teams, suppliers of fab equipment and processing materials, factory scientists, chip processing manufacturers, and government agencies and laboratories now rely on the assessments and forecasts of the ITRS. At one level of analysis, this chapter continues the historiography of the previous chapter. However, at another level the transition to full-fledged *industry* roadmap represents a significant perturbation in the evolution of semiconductor industry

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[5] Semiconductor Industry Association, *International Technology Roadmap for Semiconductors, 2003 Edition*, San Jose, CA, 2003, available online at http://public.itrs.net/

[6] Wolfgang Arden, Infineon; Joop Bruines, Philips; Bob Doering. Texas Instruments; Paolo Gargini, Intel; Gerhard Göltz, ST Microelectronics; Toshiaki Masuhara, ASET; Toshihiko Osada, Fujitsu; Young-Jin Park, Hynix; Jack Sun, TSMC; Makoto Yoshimi, Toshiba; "Introduction to Highlights of the 2003 ITRS," *Future Fab International*, January 2004.

roadmaps and is treated as such later in the chapter. This is a key premise of this chapter: that the Roadmap became an industry-level instrument to serve a *common* national interest. It has since evolved into an international instrument serving an even larger common interest: perpetuating the technology for the global industry's collective benefit. Consistent with the findings in Chapter 9 the series of SIA Roadmaps highlights how roadmapping has adapted over time to the changing needs of the semiconductor community.

936 technologists from around the world participated in the development of the 2003 ITRS. In the decade since, the SIA Roadmap process has expanded its scope in depth and breadth so that it is now truly an international process involving all major chip-making regions (i.e., U.S., Europe, Japan, Korea, and Taiwan) and industrial sectors now representing annual revenues of about $200 billion. One of the unique aspects of the semiconductor industry is the historical pattern of exponential technological advance that has contributed to such rapid growth as semiconductor devices increasingly find application in more and more areas. Indeed it's very hard anymore *not* to find semiconductor content in anything electronic. The simple explanation of the decades-old pattern of technological advance in semiconductors is known as "Moore's Law" as earlier described (see especially Chapter 8). This means that devices that are "faster, cheaper, better" have become commonplace in modern society.[7] The evolution of personal computer technology is but one recognized example of this phenomenon, while technological advance based on broader application of chips has been argued by economists as the single greatest factor contributing to the sustained productivity improvements since the mid 1990s. Central to keeping this rate of advance going is overcoming the increasingly difficult challenges of making device feature sizes smaller. The sheer complexity of this challenge is pushing the very limits of physics as individual chips packing billions of circuits today require design rules[8] that have

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[7] See for example Nikhil Hutheesing, "Faster, cheaper, better—forever," *Forbes*, July 7, 1997, 172-178.
[8] Design rules state the allowable dimensions of features used in the design and layout of integrated circuits. Each set of rules is unique to a specific process technology node. The rule set is usually designated by the patterned gate length. For example, a .1um (100nm) rule set means that the patterned gate length is .1um (100nm).

surpassed the near-atomic or *nano*-scale level of one-tenth of one-millionth meter (0.1 micrometers/microns or 100 nanometers) dimensions.[9] Each time device feature sizes get smaller—and they must on a regular basis according to Moore's Law—manufacturing equipment, materials, and processes must be modified or totally replaced. Today's modern fabrication facility costs upwards of $3 billion to construct and outfit, and may only produce output for one or possibly two device generations before major retrofitting is needed. This is an extremely expensive proposition, even for industry giants. Since timing is so critical, vital coordination of resources among the infrastructure supporting the enterprise is paramount. Add to this the truly global nature of the industry and it is very clear that a collective method of technology planning is necessary to help keep the industry in synch in areas where there is a common need: pre-competitive manufacturing processes. This is the purpose of the ITRS.

The ITRS forecasts a 15-year set of characteristics of future memory, logic, and other semiconductor device structures and performance, the technology set of process requirements for these characteristics, the challenges to have such requirements realized, and possible solutions to those challenges. It is acknowledged that the Roadmap is successful as a tool to help the overall industry maintain focus and leverage investments toward solutions the entire industry benefits from.

The current theme of the ITRS keys on prime objectives and an important recognition for encouraging innovation. One key objective of the Roadmap has traditionally been to limit its content to silicon-based substrates and CMOS devices, however the 2003 ITRS considers III-V compound semiconductors for the first time in recognition of divergent market needs. Another goal of the Roadmap is to be an inclusive process in the search for solutions to meet the technical requirements of the future device characteristics. These two thematic and seemingly dichotomous objectives have helped strengthen the credibility of the Roadmap, while also

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[9] 100 nanometers is also the wavelength of visible light used to perform the optical lithography process in fabrication, thus the impending need for next-generation lithography (NGL) based on non-optical methods.

drawing criticism of exclusivity and a perceived danger that if a technological solution is not discussed in the Roadmap, then the potential for an innovative solution to become viable as a product is jeopardized. Further, these goals are tempered with the recognition that solutions for the technical challenges of decreasing feature sizes and high performance must begin to comprehend an approaching finality to familiar processes and architectures as chips move beyond 45-nanometer dimensions—certain long-standing technologies simply cannot build devices that small. There is an increasing need to understand possibilities for future innovations for products and applications that may not yet be well defined. As the ITRS has matured, these objectives and recognition factors now appear to be complementary. The Roadmap is becoming a forum for truly identifying near-term needs and solutions (i.e., one-six year timeframe), and long-term challenges (i.e., 7-15 years), and exploring realms of innovations that require continued examination and are possible candidates for future incubation (i.e., beyond the timeframe of the Roadmap).

As described in Chapter 9, an identifiable semiconductor industry roadmapping process began to emerge in the late 1980s as a national effort within the United States. Following the third official SIA Roadmap, international review and participation was invited in 1998 and the process continues to evolve. It has morphed from a national roadmap designed to pull together the domestic leading-edge chip manufacturers to ensure continued growth and profitability to an instrument that serves the global community in addressing future technical issues all manufacturers face. The anticipated result of such a Roadmap is to ensure that the historical manufacturing of chips—characterized as competitively priced, better performing, and more reliable—maintains the high average of productivity and profitability. Indeed, the indirect effect is an abundance of cheaper chips in electronics and other product goods that ultimately have the same attributes, such as more affordable personal computers that perform better and are more reliable. Another attribute is the potential for creating major growth in related industries, as well as within the semiconductor business enterprises. For near and long term assessments, solutions

should comprehend normal production environments, either currently in existence or perceived as economically feasible future factories. The nature of Roadmap solutions demands balancing the extension of current process and fab infrastructures with newly developed systems and thoughtful consideration of the timing of such solutions. Also, since the introduction of such technologies typically involves an introduction phase marked by unpredictability and possibly an initial slow return, such endeavors involve risk. This risk, however, is leveraged through the Roadmap process.

Thematic Review

This chapter is part descriptive and part analytical. The descriptive element of the chapter follows the historiography of the previous chapter and specifically addresses the critical juncture when formative research roadmaps coalesced to become a single *industry* roadmap in the *1992 SIA Workshop Reports*. Comparisons are made between the 1992 Workshop Reports (commonly referred to as the 1992 Roadmap) and its predecessor, *Micro Tech 2000* which was addressed in detail in Chapter 9. Insight is provided on the transition from a government-sponsored program to an industry-led initiative. The analysis reveals that the transition was not a simple process as has been previously reported. However, the handover did succeed and the resultant product, the 1992 SIA Roadmap, set the foundation for all successive industry roadmaps.

Following this historical discussion a more analytical approach reviews the set of six SIA Roadmap editions as a whole, first in summary fashion to briefly demonstrate how each succeeding SIA Roadmap has grown increasingly complex in content and interpretation. For the overall purposes of this study—to assess the Roadmap's influence on innovation, strategy and policy—the summary approach proved appropriate.[10] Following this summary review the *2003 International Technology Roadmap for Semiconductors (ITRS)* is briefly presented in a manner that the reader may grasp the significant changes (and similarities) between the first SIA

[10] A comprehensive content analysis of each Roadmap edition was attempted but proved too exhaustive.

Roadmap (1992) and the most recent (2003). The chapter concludes with a discussion of three noteworthy developments that characterize major challenges that have cropped up over the decade of industry roadmapping. In total, this analysis provides the context for the research findings on the Roadmap process presented in the next chapter (11) as well as strategy and policy implications presented in Chapter 12.

Data sources for this chapter included all six Roadmap editions, of course, along with the precursor *Micro Tech 2000 Workshop Report*. But the Roadmaps, by themselves, cannot tell the whole story. Therefore, the Roadmaps are supplemented with an external evaluation that comprises a review of pertinent literature and personal or telephone interviews conducted by the author. Altogether more than 140 Roadmap citations from the trade press or academic literature have been considered along with fifty interviews with Roadmap participants (see Appendix D10). Finally, the author was allowed to observe three Roadmap workshop sessions during the development of the 1999 ITRS. Considering all these data sources made it possible to cross-check major themes, concerns, and other issues addressed in the actual Roadmap publications, improving the study's validation. Additionally, historical demographic data of Roadmap participants is presented to help explain some of the thematic changes in the Roadmap over time.

Considering all the sources, the analysis strongly suggests that the semiconductor industry Roadmap process has reflected the changing needs of the community for which it serves, remaining a source of consensus among a broad and diverse audience that expands with each edition. This is one of the hallmarks of its continued success. At the same time there is a pattern of emerging topics addressed in each Roadmap that represent non-consensus items. After all, the Roadmap is a research planning exercise that starts with widely accepted principles such as traditional device scaling performance. However, the Roadmap's planning horizon of 15 years forces participants to look well beyond what they can see "down the road." The 2003 Roadmap comes at a crucial point in the industry's history. Economic and technological challenges loom

larger than ever as discussed throughout this study. This analysis may help in both answering questions about the Roadmap process, and in asking new questions not yet considered.

Transition to an *Industry* Roadmap

The chapter now closely examines the transition to an industry roadmap in 1992, noting fundamental changes in motivation, participation, interpretation and use. Following SIA's full acceptance of the process a more summarized investigation of subsequent SIA Roadmaps will distinguish an overriding theme: *increased involvement and granularity* (i.e., the level of detail of Roadmap technology characteristics).

The latest edition of the SIA Roadmap, ITRS 2003, is the culmination of a decade of formal industry collaboration that began with the 1992 Roadmap, but can be traced back to Micro Tech 2000 which was developed under the auspices of the National Advisory Committee on Semiconductors (NACS). Recall from Chapter 9 that the NACS charter was due to expire in 1992 and that, in preparation, the SIA was requested to take over the Micro Tech 2000 technology initiative. This would not be a simple handover as the SIA was technically ill-equipped as an organization at the time. Don Wolleson, who participated in Micro Tech 2000 and each subsequent SIA Roadmap, recalls that the SIA in 1991 was primarily concerned with trade issues, thus it employed about fifteen or so social scientists (i.e., economists, policy types, etc.) but no technologists.[11] Sematech and the SRC were the technical arms of SIA and Wolleson states that SIA initially attempted to delegate the responsibility to one of these consortia. It would take a few meetings with government officials to convince SIA to take over as governing agent. SIA had recently established a Technology Committee, chaired by Gordon Moore, which also included the CEOs of both industry consortia. Bill Spencer of Sematech accepted the responsibility to review Micro Tech 2000 and prepare a response to the SIA BoD by March 1992. Spencer turned to an outside consultant, Bill Howard, Professor from University of California

[11] Don Wolleson, telephone interview, August 10, 1999.

Berkley and former senior semiconductor executive at Motorola, to head up a task force to study the matter. As previously stated the task force's charter included both integration of Sematech and SRC R&D activities along with a manufacturing—more specifically *process technology*—emphasis. Spencer emphasized three issues of pressing concern to the SIA:

1. The SRC/Sematech interaction must be improved to ensure efficiency, and the relationship should be viewed as a single entity under the direction of the SIA,
2. SIA should be viewed as the keeper of "manufacturing" issues and the consortia approach as a model for other industries, and
3. SIA must find ways to influence government R&D spending through DoD, DoE, DoC, NSF, National Labs, etc. since the SIA felt that no new semiconductor consortia were necessary.[12]

Thus it is clear that efficiency in manufacturing-related R&D would be a major consideration in any new SIA technology initiative. In other words, if the goals of Micro Tech 2000 were to be achieved this would be accomplished through existing resources, both publicly (i.e., government support) and privately (i.e., consortia membership fees). This sentiment was a practical response to the "Apollo-like" request from NACS and reflected Spencer's more incremental approach to improving manufacturing technology.[13]

Micro Tech 2000 Implementation: the "Howard Report"

Howard's task force report was presented to the SIA Board in February 1992 with this conclusion:

> *The task force accepted the Micro Tech 2000 roadmap directions but concluded that the rate of progress is faster than available resources are likely to permit.* It therefore concentrated on industry actions to best realize the Micro Tech 2000 vision within realistic constraints.[14]

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[12] Bob Burger, minutes of meeting held December 13, 1991 at Sematech.
[13] George Leopold, "Sematech beginning to broaden its scope," *Electronic Engineering Times*, December 13, 1993.
[14] "Micro Tech 2000 Implementation Task Force Report," February 28, 1992, emphasis in original. Since Bill Howard chaired the implementation task force, this report was commonly referred to as the "Howard Report," emphasis in original.

The task force probed further into the new emphasis for the technology planning effort: *manufacturing technology development*, and the agents chiefly responsible for implementation: *Sematech and SRC* through broadened responsibilities:

> *The underlying objective of this recommendation is to develop, articulate and act on a common industry technology agenda.* This agenda must outline how more effective manufacturing technology development can be planned and acted upon ... The Micro Tech 2000 Workshop Report serves as an initial vision... *we propose that appropriate established Sematech and SRC panels be charged to address broader issues. Similarly, we do not recommend a separate new Micro Tech 2000 initiative.*[15]

The report goes on to define the overall strategy and structure for carrying out the proposed industry technology agenda centered around manufacturing technology development. A new *Executive Technical Coordinating Group* (ETCG) consisting of the SIA Technology Committee Chairman and the Sematech and SRC CEOs would oversee newly established *Focus Technology Groups* (FTGs) in areas such as Lithography, Packaging and Interconnect, Metrology, and other critical gap technologies. The FTGs would come from existing combinations of Sematech FTABs (focus technical advisory boards) and SRC Science TABs and be primarily responsible "to develop and maintain industry roadmaps and to develop industry action plans. The FTGs should be the "keepers" of these roadmaps and should solicit input from throughout the technical community to ensure continued vitality of the Micro Tech 2000 vision."[16]

Finally, the report concluded that Sematech and the SRC should be "conveners in critical technology areas" and suggested an ongoing roadmap process that went beyond existing methods of exchange within the national technology development community:

> The semiconductor industry has outgrown the ability of general industry conferences to address the level of detail required by many of today's critical technology areas... In order to facilitate progress in such fields, *Sematech and the SRC, as extensions of their roles and with the coordination of the ETCG, must convene experts from throughout the industry to review and consider future developments as the technology unfolds.* Results of these meetings should help guide the manufacturing development process.[17]

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[15] Ibid., emphasis in original.
[16] Ibid., emphasis in original.
[17] Ibid., emphasis in original.

In May 1992 Bill Howard formally presented the task force findings and recommendations to the SIA Board. It was accepted and the "SIA Roadmap" process was officially started.[18] Shortly thereafter the task force report was published intact by the SIA in draft form with a new title: *Towards a National Technology Strategy*.[19] Planning for a "SIA Semiconductor Technology Workshop" to be held in Irving, Texas in November was well underway. Howard, who had drafted the implementation report, and Bob Burger, SRC research executive, would head the effort. Burger had co-led the Micro Tech 2000 Workshop. Gordon Moore would deliver the keynote address as he had done at Micro Tech 2000.

Because of Burger's previous experience, a considerable amount of pre-workshop planning was already underway to ensure the success of this follow-on initiative. Numerous committees were established: a steering committee and technology committee that mirrored Micro Tech 2000, along with ten working groups that would address individual technology areas (e.g., lithography, chip design and test, etc). Total participation in this new effort would be close to 200 people, much broader than Micro Tech 2000.

Gordon Moore emphasized the purpose of the upcoming roadmap exercise as a means to develop a unified vision for the industry: "We must create a common national plan from these separate approaches so the industry is all singing from the same sheet of music, as well as enlisting outside support."[20] Owen Williams,[21] former research executive at Motorola, was a member of the implementation task force. He recalls the importance of the industry to "speak with one voice" through a comprehensive roadmap:

> In the 1980s the U.S. semiconductor industry was faced with the fact that they were losing share of market to Japanese companies and made a significant joint effort to re-

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[18] Bill Howard, correspondence with the author, September 5, 1999.
[19] Semiconductor Industry Association, "Towards a National Semiconductor Technology Strategy," Draft, June 1992. Interestingly, NACS second annual report published February 1991 was titled "Toward a National Semiconductor Strategy," while the third and final annual report published February 1992 was titled "A National Strategy for Semiconductors: An Agenda for the President, the Congress, and the Industry."
[20] Jack Robinson, "Moore: Unity Tech Strategy," *Electronic News*, July 27, 1992.
[21] Owen Williams would become the first Chair of the Roadmap Coordinating Group and oversee development of the 1994 and 1997 SIA Roadmaps.

> establish technology leadership. To do this they established the SRC, SEMATECH, and facilitated the National Advisory Council to the President on Semiconductors. Unfortunately all three of these entities acted independently, approached the U.S. Government for funding to solve this research dilemma. Each was asking for substantial government funding, claiming they had the solution, but each had a different approach. The Government came to the SIA and told them they needed to present a unified front to the Government. An industry taskforce was established and chaired by Bill Howard to propose ways to "speak with one voice." I was on that taskforce. The output of the taskforce was a report (the "Howard Report") that recommended, among other things, a continuous roadmap. The SIA implemented this recommendation.[22]

Elements of the consolidated SIA Roadmap were defined. One particular characteristic would be that the SIA Roadmap would be a requirements document: "…each technology area is driven by a set of requirements... Therefore, before a roadmap is finalized the needs must be articulated."[23] The definition of a roadmap was stated as "a description of technology over several years (or generations)." To accomplish this, requirements must also be described over several years (or generations). These requirements would start with "Product Requirements" taken from SRC 2001 Goals.

Regarding methodology, the consolidated SIA Roadmap would have a consistent format, but more importantly the planning assumption for timing would be "ready for commercial use":

> Roadmaps exist today in three different formats and yet, none are complete in total coverage of the entire spectrum of technology needs. The first step in the consolidation process is to establish the format in which the roadmaps will be displayed... In any case *it is necessary to be very clear when the technology is ready for commercial use.*[24]

Equally important was the decision *not* to select a single-product focus such as the 1Gb SRAM used in Micro Tech 2000. Recall from Chapter 9 that a similar choice was made almost a decade earlier by a young SRC organization, driven in part by anti-trust concerns. Regarding the 1Gb SRAM, an interesting side-note is that John Armstrong had initially chosen the more popular DRAM product as the Micro Tech 2000 target but had difficulty attracting interest because all but three U.S. chipmakers (i.e., TI, Micron, and IBM)[25] had exited that market following intense

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[22] Owen Williams, e-mail communication with the author, August 21, 1999.
[23] "SIA Consolidated Roadmaps," op. cit..
[24] Ibid., emphasis by the author.
[25] Note that Armstrong was former VP for Science and Technology at IBM.

competitive pressures from the Japanese in the 1980s. In response to a "don't care" attitude Armstrong received from industry on the 4Gb DRAM target,[26] Tak Ning suggested an SRAM target because it was a more applicable design to U.S. manufacturers making logic chips, then emerging as new technology driver. Further, Ning was concerned that DRAM scaling trends would not hold as well as those for SRAM devices.[27] Regarding a product-specific target for the SIA effort Moore simply stated that "choosing a specific semiconductor vehicle doesn't make a lot of sense. It's hard to select one product that everybody will want."[28] In connection with this, Spencer and Seidel note a fundamental difference in the starting point. The authors state:

> Unlike the MicroTech 2000, which set the challenges for a particular technology generation (1GB SRAM) circa the year 2000, the 1992 roadmap assessed the current status and then set down the needs for each of five succeeding generations, looking out 15 years from 1992 to 2007.[29]

Note that, as described in Chapter 2, the proposed SIA roadmap would be a *technology-push prospective* approach (i.e., starting from the present and going forward), in contrast with the *requirements-pull prospective* approach used in Micro Tech 2000 (i.e., starting from a future target and working backwards). A table in the workshop planning documentation shows *six* generations for the first time: 0.8u, 0.5u, 0.35u, 0.25u, 0.18u, 0.12u and although years are not shown,[30] this translates into a 15yr time horizon (i.e., current plus 5 future generations, also see Box 10-1) that would become the baseline for future SIA Roadmaps as just described by Spencer and Seidel. This document continues with the utility of this longer planning horizon:

> Now with this additional table of requirements, strategies can be put into place to address extendibility of equipment over several generations of processes. Equipment suppliers

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[26] A 1GB SRAM is equivalent in device complexity to a 4Gb DRAM. In other words, they would belong to the same product generation.
[27] Tak Ning, "1-Gb SRAM vs. 4-Gb DRAM," presentation slides, September 1990. Personal interview with the author, July 18, 2000. Also note that the demise of U.S. Memories Inc. in January 1990 affected disinterest in DRAMs among American chipmakers (Source: John Armstrong, telephone interview, January 23, 2002).
[28] Moore, quote in Robinson, op. cit.
[29] W.J. Spencer and T.E. Seidel, “National Technology Roadmaps: The U.S. Semiconductor Experience,” invited paper (Conference in China), approximately 1995, 215.
[30] Author and date unknown, "SIA Consolidated Roadmaps: The Planning Methodology," copy of FAX dated July 14, 1992 from MOT (Motorola) External R&D, 5pp., 4.

and material developers can now have longer lead times to meet the requirements and finally researchers can have an insight into the real future needs.[31]

Finally, the document called for the development of "Strawman Roadmaps" prior to the workshop so that workshop participants could focus on validation and finalization of the Roadmap. It is important to point out the significance of the selection of minimum feature size as the primary metric for technology generations. While this was also included in Micro Tech 2000, it was a secondary measure to device density (complexity). By specifying minimum feature size the emphasis would firmly be placed on *process technology* that would enable a particular product vis-à-vis the other way around. This would also mark the beginning of a redefinition of technological progress, hence Moore's Law as described by Mack in Appendix C.

In February 1992 NACS published its third and final annual report entitled, *A National Strategy for Semiconductors: An Agenda for the President, the Congress, and the Industry*. The first recommendation under the objective, "Enable U.S. Industry to Achieve a Competitive Technology Positions," was:

1. Implement a Semiconductor Technology Roadmap for the Industry (1992)
    - Plans to implement technology roadmaps such as those developed at Micro Tech 2000 should be considered by senior semiconductor industry leaders.
    - The roadmaps for semiconductor technology development should be updated regularly by the industry.
    - Universities should make contributions toward achieving the industry's technology roadmaps through funding from the Semiconductor Research Corporation, the National Science Foundation, and others.
    - Joint manufacturing facilities should be considered for early production of deep submicron technologies.[32]

With this final report NACS obligations were fulfilled and the committee disbanded. Of all that is attributed to NACS, Micro Tech 2000 is perhaps its most enduring legacy as described in Box 10-1.

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[31] Spencer and Seidel, op. cit.
[32] National Advisory Committee on Semiconductors, *A National Strategy for Semiconductors: An Agenda for the President, the Congress, and the Industry*, February 1992, 18.

Box 10-1. Micro Tech 2000: A Reassessment in a Research Context[33]

"I've always thought Micro Tech 2000 was more important than it was given credit for at the time."

- John Armstrong[34]

Micro Tech 2000 (MT 2000) was a research roadmap with ambitious goals. Armstrong points out that MT 2000 was *not* part of NACS' original agenda; it came about in the second year after meeting with White House staff who were very skeptical of a controversial non-profit proposal (i.e., ECC) and anything of that sort that smacked of industrial policy. With this fresh reminder NACS evolved MT 2000 as a politically-neutral activity. Armstrong himself suggested this technical initiative. He was very pleased with the North Carolina MT 2000 workshop lamenting that this was one of the highlights of his NACS involvement. The workshop was attended by technologists, not policy types nor industry executives. All these people knew each other but prior to this did not have the charter/forum to do this legally because of anti-trust limitations. He distinctly remembers all NACS meetings began with an admonition about anti-trust from a lawyer and thinks MT 2000 workshop also began this way.[35] He makes an important point about the oft-criticized "leapfrog" approach: although viewed as impractical by most, this was the only way at the time to get competitive people in a room together to work on something because the longer-term horizon wasn't perceived as collusive. Additionally the bold and challenging goal (i.e., 8-10yrs into the future) was a good fit for researchers as mentioned in Chapter 9.

According to Armstrong, one of the most important things about MT 2000 was that it shared the idea-generation process. Formerly IBM and ATT did a disproportionate share in research; few others could afford to. Gordon Moore would later state, "In fairness to Micro Tech 2000, its charter was only to come up with the best technical roadmap possible, regardless of financing."[36]

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[33] This account draws from a telephone interview with John Armstrong and e-mail, January 23, 2002.
[34] Ibid.
[35] See Appendix D10-A as a possible set of anti-trust ground rules used in meeting from a decade later.
[36] Moore, quoted in Robertson, op. cit.

Armstrong states that the period following MT 2000 (i.e., implementation) was not "transitioned over" to SIA as is popularly reported. Like Wolleson, he was surprised that SIA was caught off guard with MT 2000; they were not really prepared technically to take it over. After publishing the workshop report, NACS had absolutely no involvement. The sentiment from SIA was one of apprehension about somebody else doing this other than them, the group representing industry. He recalls Gordon Moore, SIA Technology Committee Chair, stating that SIA would "take care of Micro Tech 2000 implementation" and subsequent actions in picking up the roadmap. He views this as consistent with traditional manufacturing (i.e., SIA) distrust with research (i.e., NACS).

One reason MT 2000 was a success to Armstrong is that it focused on silicon, the industry's mainstream substrate material. He felt that government IC research had been misdirected away from silicon. Neither DARPA nor NSF supported research in silicon "yet that's where the industry was going." Most efforts were in germanium or gallium arsenide, the latter concluded to be a fast successor in silicon. He could not get anyone in the government to listen about the need for silicon research with the exception of VHSIC where IBM was a participant (see Chapter 6). However when IBM's VHSIC work was completed and delivered to DARPA, they said thanks but they "wouldn't know what to do with it." Perhaps VHSIC sped up the roadmap a little, but industry was going to continue with silicon anyway. In Armstrong's view, DoD was naïve thinking that they were fostering "research" with non-silicon efforts.

Despite the criticism levied against NACS and Micro Tech 2000, Armstrong suggests that in fact MT 2000 was one of the good, unintended consequences of NACS. He likens this to Sematech, where it is widely recognized that their longer-term benefits came from strengthened the tool industry and figuring out areas where industry could truly work together, both of which weren't in the original charter. The Sematech experiment proved you really could work together on how future equipment could be designed, checked out, etc., in a rational way, but wouldn't give anyone a competitive advantage. Research resources could be used more efficiently and

effectively as a result despite so many unrealistic expectations about Sematech (e.g., actually generating technology).

1992 Roadmap: SIA Semiconductor Technology Workshop

After considerable planning, a workshop was held in November 1992 in Texas that brought together "179 of the country's key semiconductor technologists … to create a common vision of the course of semiconductor technology over the next 15 years."[37] The SIA Roadmap built off of previous roadmap exercises and suggested that this was just the start of a more permanent process:

> The visions that had previously been put forth by the Semiconductor Research Corporation (SRC), Sematech, and the Microtech 2000 workshop (sponsored by the National Advisory Committee on Semiconductors) were used as a foundation from which to build a single set of roadmaps that use the talents of the expert participants to anticipate the needed technological developments... To be of ongoing utility, the roadmaps will need regular updating as the future becomes more clearly visible. The plan is to reconvene a workshop every couple of years to keep them current and vital.[38]

It is clear that the SIA, representing the U.S. semiconductor industry, had fully accepted the technical charge articulated by Micro Tech 2000:

> With the expiration of NACS, the SIA accepted responsibility for continuing [Microtech 2000]. The SIA Semiconductor Technology Workshop and its associated implementation plan are the next steps.[39]

But the workshop took a different approach than the preceding NACS effort. The most noticeable difference is in the timing. Device generations no longer reflected the one-generation acceleration central to Micro Tech 2000; instead they reflected historical scaling of 3yrs per generation. Related to this, the planning assumption for timing was development of "engineering samples" in Micro Tech 2000 whereas the 1992 Roadmap schedule was organized by "date of

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[37] Semiconductor Industry Association, *Semiconductor Technology Workshop Conclusions*, San Jose, CA, 1993, Foreword.
[38] Ibid.
[39] Ibid.

production startup." The net result was that the 1Gb SRAM and 0.12 feature size targets from Micro Tech 2000 would now be shown occurring a full four years later in 2004.

Sam Harrell, former Chief Strategy Officer at Sematech and SEMI/Sematech executive, had directed Bill Howard to ensure the SIA Roadmap be a *practical* roadmap, in contrast with the leapfrog goal of Micro Tech 2000 that he felt was fundamentally flawed given limited resources available. Using more of an incremental innovation approach, future capabilities of supporting technologies were extended based on what was doable. Sematech's experience in cost modeling helped bring a more logical approach to planned technology advance by considering economic factors. The idea was by incorporating a practical methodology to an industry roadmap, Sematech could play a vital role in helping to set a realistic "cadence" that could win over time.[40] Cost, a primary consideration throughout the Workshop, was budgeted among the technology areas as shown in Table 10-1.

Table 10-1. 1992 Technology Workshop Cost Targets

Lithography	35%
Multilevel Metals and Etch	25%
Furnaces/Implants	15%
Cleans/Strips	20%
Metrology	5%

Source: SIA, *Semiconductor Technology Workshop Conclusions*, 1993, Table 3, 6.

Also, the need to coordinate the long-range activities of the SRC and Sematech caused the SIA to consider a different set of planning challenges. Unlike Micro Tech 2000, which set the challenges for a particular product by a particular date (i.e., 1Gb SRAM by the year 2000), the 1992 roadmap update assessed the current status and then set down the technology needs for

[40] Sam Harrell, telephone interview, May 11, 2000.

each of the five succeeding generations, looking out fifteen years to 2007.[41] Note the similarities in Table 10-2: both workshops used the same feature size and corresponding memory chip capacity targets, however the timing for achieving these targets had been delayed at least a generation.[42]

Table 10-2. Comparison of Overall Roadmap Technology Characteristics

Feature size (um)	**0.50**	**0.35**	**0.25**	**0.18**	**0.12**	***0.10***
1991 Micro Tech 2000	1991	1993	1996	1998	*2000*	
Current SRAM Trend	4M	16M	64M	256M	*1G*	
1992 SIA Workshop	1992	1995	1998	2001	2004	*2007*
Bits/chip: SRAM	4M	16M	64M	256M	1G	4G
Bits/chip: DRAM	16M	64M	256M	1G	4G	16G

Source: NACS, *Micro Tech 2000 Workshop Report*, Figure I-1, 6, and SIA, *Semiconductor Technology: Workshop Conclusions*, 1993, Table 2, 6.

Box 10-2. SIA Roadmaps: Why 15 Years?

One of the unique aspects of the series of SIA Roadmaps is the planning horizon of 15 years. This convention began with the 1992 Roadmap and continues through the 2003 ITRS. Thus, with each new edition the end of the Roadmap reaches farther into the future like a moving yardstick. This researcher asked the question, "why 15 years?" of many informants because fifteen did not seem like a conventional research planning horizon (i.e., 15 is an *odd* number). Five, ten, or even twenty years are more typical time-spans for strategic planning purposes. The reason for 15yrs involves the unique pattern of technology advance every 3yrs as described throughout this study and in particular in Chapter 8. Simply, five future generations three years apart equal 15 years.

[41] Spencer and Seidel, op. cit..
[42] Note that Micro Tech 2000 assumed demonstration of "engineering samples" while the SIA Workshop used "date of production start up" which might be as much as a product generation (i.e., avg. 3yrs) difference in availability.

This answered the 'how' question, but still did not answer the question, why? In fact, none of the roadmaps or strategic plans that preceded the SIA Roadmap used 15 years as a baseline. Sematech had used five years primarily because the organization was half funded by government for 5yrs. The SRC, involved in longer-term academic research, had developed strategic plans based on 10yr horizons. Micro Tech 2000, developed in 1991, used a 9yr horizon to the year 2000. Its premise was to "leap" a generation and essentially pull in a projected 4th generation through an all-out development effort.

There is some documented evidence for a 5 (6 counting the starting) generation roadmap timeframe. As previously mentioned, a planning document provided in preparation for the 1992 Workshop shows the current plus the next 5 generations (thru 0.12 um) but without any dates. The document also provides a definition of a roadmap as "a description of technology over several years (or generations)."[43] Interestingly, a very close set of targets is shown in an earlier document from the early Sematech strategic workshops (see Chapter 9). For instance, in the final report on the Advanced Lithography Workshop held in January 1988, several roadmap tables show six generations along the bottom axis as follows: 0.70, 0.50, 0.35, 0.25, 0.17, and 0.12 micrometers (um) (see Figure 9-2).[44] Note the similarities with Micro Tech 2000 and 1992 SIA Workshop projections, developed a generation or so later. Again though, no time period is given. A review of other strategic workshop reports (e.g., optical lithography, wafer size, metrology, and EH&S) does not show this long view. It is understandable why *advanced* lithography would because its express purpose was to replace optical lithography which at the time was projected to continue through 0.25 um, or another three generations into the future.[45]

Asked this question, Moore himself stated that it was based on 3yr device generations and it "made sense for industry to look out about 5 generations" because company roadmaps usually

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[43] "SIA Consolidated Roadmaps," op. cit., 2.
[44] "Final Report: Sematech Planning Workshop on Advanced Lithography," Burlingame, CA, January 25-27, 1988, courtesy of Sematech Records & Archives.
[45] Ibid., 12.
[46] Gordon Moore, telephone interview, February 11, 2002.

had much shorter focus (about 2-3 generations) and the SIA Technology Committee, which he chaired, had a definite idea of the SIA Roadmap as "the" guiding plan to cover both Sematech and SRC needs which covered farther out generations.[46] Indeed, the 1992 SIA Workshop, as an industry assessment and response to Micro Tech 2000, extended the "leap-frog" 1G SRAM (0.12 um) projection out based on normal scaling of 4 generations to twelve (not nine) years. Twelve years would have easily accommodated the planning horizons of both Sematech and SRC strategic plans. But why 15 years, not 12 (10 is not divisible by 3) or 18? Other informants could not pin down the exact reason either. One speculation is that 15, although an odd number, seems to fit better than 12 and conveniently occurs if you add one more generation on the end. Add to this the perceived formidable barrier of 0.10 as that next generation and it is plausible that this was considered "the end of the road." Expanding on this last point note in Table 10-2 the 0.10 um milestone scheduled for 2007. This value had appeared in Micro Tech 2000, but as a range (i.e., 0.10 - 0.15) associated with 1Gb SRAM capability. The 0.10 um (also referred to as the elusive "point one") barrier was considered at the time as the ultimate scaling limit in much the same way that 1 micron was viewed not quite a decade earlier (see Chapters 3 and 4 discussion on limits).

Or it might simply have been that extrapolation of historical trends carried the industry there (i.e., Moore's Law) and it didn't really matter whether it was some seeming barrier or not. In any case the 15-year Roadmap horizon is the accepted convention. Regardless of why, it is so, somewhat like why Moore's Law came to be defined as discussed in Appendix C; it just is.

In perspective, fifteen years is a very long time, especially in this industry. Recall Gargini's opening quote about two years being too long for a document's currency. Change simply occurs too fast. For instance, in the first 15 years this young industry had commercialized the IC. In the next 15 years came the manifestation of Moore's Law that would bring the DRAM, microprocessor and, other high-volume chip applications. In the next 15 years the PC revolution would change computing forever. The current 15 years have brought the internet, cell phones, and untold wireless and embedded applications. Interestingly, this 15yr period will end in 2007,

coincident with the end of the first Roadmap. It is difficult to imagine what might occur over the next three years, much less the next fifteen.

"Why 15 years?" is not a trivial question. In all likelihood it was probably arrived at without great deliberation based on traditional scaling trends that created distinct 3yr generations, and the confidence that this pattern would continue into the future with the insurance of a Roadmap sustaining it. But as discussed in Box 10-3, this 3yr generation—now referred to as technology node—pattern no longer applies as many factors have converged to redefine—or rather refine—the metric. In fact, this refinement started with the 1997 NTRS, the first Roadmap to reflect technology acceleration and as a result, projects *seven* generations (current plus 6) in a 15yr window.

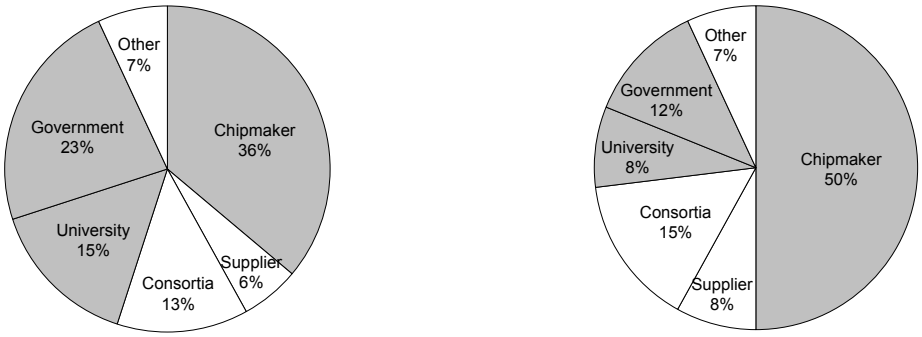
For the last few Roadmaps, the end of traditional CMOS scaling as the basis behind Roadmap timing has been acknowledged. Thus by the end of the current 15yr Roadmap timeframe (2018) it is expected that bulk planar CMOS, the basic device that has been the key industry driver since the 1970s, will no longer play the leading role. In fact, this has already begun to occur with DRAMs, where device scaling (i.e., in bits/chip) has actually been reduced by at least half (see Figure 10-11). Hence the "several generations" premise for a 15yr Roadmap timeframe has changed. Yet 15yrs, based on CMOS technology scaling circa 1990, remains as the time horizon. This might help explain the increased attention devoted to Technology Node definition and refinement in recent Roadmaps. In this respect, "why 15 years?" is not a trial question.

Other differences between the reports of the 1992 SIA Workshop and 1991 Micro Tech 2000 Workshop included the adoption of complementary metal-oxide silicon (CMOS) as the underlying assumption for "semiconductor" devices. Also, for the first time an industry *technical* roadmapping process prioritized the "cost-to-produce" as a key metric. The cost per square centimeter (cost/cm^2) was taken as a benchmark metric against which budget targets were developed for the

various fab production technologies (e.g., lithography, multilevel metals and etch, etc.). The objective was to keep the semiconductor industry on the historic productivity curve of 30 percent reduction in cost per function per year.

Two documents were published in the spring of 1993 to represent the 1992 Roadmap: *Semiconductor Technology Workshop Conclusions* and *Semiconductor Technology Workshop Working Group Reports*. Although strictly a U.S. effort, these documents were made available worldwide at no cost. Combined with a third report, *Semiconductor Technology: An Agenda for American Cooperation*, these were the first technology strategy publications issued by the SIA in its 15yr history. One of the key conclusions of the 1992 Roadmap was "the recognition that the infrastructure was unbalanced in its investments among fab technologies and design, test, packaging and TCAD."[47] The SIA had organized the preparation of the 1992 technology roadmap to serve as a guide for the R&D programs of industry, SRC, Sematech, government agencies and national laboratories, and universities.

One final point is the discernable change in demographics in participation as shown in Figures 10-2a and -2b.



(a) 1991 Micro Tech 2000 **(b) 1992 SIA Roadmap**

Figure 10-2. Comparison of Participation by Category: Micro Tech 2000 vs. 1992 Roadmap

[47] Ibid., TCAD stands for Technology Computer Aided Design.

Source: NACS, *Micro Tech 2000 Workshop Report*, Appendix A, 41-43, and SIA, *Semiconductor Technology Workshop Working Group Reports*, Appendix: Semiconductor Technology Workshop Participation, 148-153.

The most pronounced change in these two graphs is the considerable reduction (almost by half) in the mix of government and university participants. On the other hand, there was a noticeable increase in the mix of chipmaker—and to a lesser extent, suppliers and consortia—participation. While many from Micro Tech 2000 also participated in the 1992 SIA Workshop, attendance doubled in number and most of that increase came from chipmakers, suppliers, and consortia. As had been intended, the 1992 SIA Roadmap was an *industry* roadmap, a feature that would become even more the case in successive Roadmaps as will be discussed shortly.

The trade press took notice of the 1992 Roadmap (see Appendix D10-D). One selected account reflected a few important themes that have been discussed:

> Unlike many previous lofty proposals, the new roadmap isn't dependent on federal funding. "This is primarily an industry initiative to get all segments working with each other… Micro Tech 2000 was an unrealistic attempt to create a Manhattan-type Project for semiconductors without regard to costs. We have to be far more pragmatic. If any technology roadmap is going to work, it has to be affordable," said Dr. [Gordon] Moore… William Howard co-chaired the session here, and said the roadmap "will be down to earth" compared with earlier industry studies. He believes the effort will be more effective by not focusing on any single target vehicle, such as the 1G SRAM proposed by NACS.[48]

The transition from an ambitious research initiative—some might liken to a major 'science project'—to a "down to earth" industry roadmap marks a significant amendment to the evolutionary process of roadmapping processes described in Chapter 9. The rest of the chapter addresses this new *Industry Roadmap* era. Analysis will not be historiographic but follow a more summarized approach, examining the series of SIA Roadmap editions as a whole while noting important differences among individual Roadmaps. The chapter will end with a discussion of major issues drawn from this analysis.

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[48] Jack Robertson, "New Roadmap Pinpoints IC Goals: Semiconductor Industry Association Seminar Sets 15-Year Plan for Integrated Circuits," *Electronic News*, November 23, 1992.

To begin, Table 10-3 summarizes key characteristics of the six SIA Roadmap editions beginning with the 1992 Semiconductor Technology Workshop and concluding with the 2003 ITRS.

Table 10-3. A Summary of SIA Roadmap Editions

Title, Edition	Page Count, # Fig. & Tab.	Timeframe, Geometries	Major Themes	Significant Changes
SIA Semiconductor Technology Workshop, 1992	154pp +60 *Conclusions* (separate, non-technical volume), 44 figures 28 tables	1992-2007, 0.5-0.10um	- Consolidate research visions (roadmaps) of SRC, Sematech, and Micro Tech 2000 - Foster era of shared vision—commonly understood view of technology needs as the basis for effective U.S. development efforts - Develop a kind of "virtual vertical integration" to link independent companies, government, R&D programs, and universities into effective working partnerships	Compared with *Micro Tech 2000*: - broader participation, greater detail - prospective (start with known and work forward) vs. retrospective (start with future target and work backward) - 3yr generations timing: more practical, affordable, "down to earth" approach - 15yr timeframe (current plus 5 future generations, 6 total) - not one-time exercise: to be maintained on regular basis
National Technology Roadmap for Semiconductors, 1994	168pp +38 appendix, 42 figures 54 tables	1995-2010, 0.35-0.07um	- First renewal called *National* Roadmap, stresses importance to continue common vision and increased cooperation to ensure historical rate of progress (Moore's Law) is maintained for U.S. industry - “Urgency without crisis” call with implication that to not pursue such an effort will result in crisis - Recognizes that in the long term, technology alternatives are more numerous and significant paradigm shifts increase	- no change in 3yr node timing - separated out crosscut technologies: manufacturing, materials, metrology, modeling, standards, quality/reliability - added *Grand Challenges* - introduction of *ORTC*, with technology drivers, minimum feature size, product drivers, chip and package, fabrication, electrical design and test metrics - table and graphic structures enhanced and more consistent (e.g., performance envelopes)
National Technology Roadmap for Semiconductors: Technology Needs, 1997	196pp +30 appendix, 49 figures 65 tables	1997-2012, 250-50nm	- Emphasis on technical barriers at 100nm and the *no known solutions* dimension in the technology requirements tables - Describes continued need for sustained government support of semiconductor research as a direct influence on strong economic growth for the U.S. - Raises context of research gaps as	- 3yr renewal (all others 2yrs) - switch from microns (millionth of meter) to nanometers (billionth) as node measure - timeline acceleration, 2yr cycle next 4 nodes (1997-2003), then goes back to 3yr cycle, thus adds additional (7th) node, also emphasizes need for more frequent updates - 7 Focus TWGs and 4 Crosscut TWGs

			identified by SRC and Sematech - Makes concerted effort to fully describe challenges, quantify requirements and add timing to potential solutions	- consistent format in coding technology requirements: solutions exist (white), solutions being pursued (yellow), and no known solution (red) - Concept of near-term and long-term requirements more evident: difficult challenges before/after 2006 (100nm) - emphasis that the Roadmap encourages further innovation and makes a point that it does *not* identify all solutions, thus subtitle: *Technology Needs*
International Technology Roadmap for Semiconductors, 1999	330pp +22 appendix, 62 figures 87 tables	1999-2014, 180-35nm	- First *International* Roadmap, sponsored by SIA *in cooperation with* EECA (Europe), EIAJ (Japan), KSIA (Korea), and TSIA (Taiwan) - *No known solutions* in most cases shown within 5-year reach, thus includes new concepts of *Equivalent Scaling* [extension of device scaling approach by improving electrical performance with new/improved materials], consideration of System on Chip (SoC) needs, consideration of planar CMOS alternatives including new devices beyond limitations of CMOS - Suggests that Roadmap may also apply to new devices, compound semiconductors, MEMS, and nano technology. States that future editions of the ITRS may point to more radical approaches in order to stay on productivity trends, including new *manufacturing paradigms* - Discusses "on/off the Roadmap" and mentions that future ITRS editions may distinguish different "shades of red"	- follows 1998 *Update* 1yr earlier that included international participation, now annual process - much more comprehensive (granular): text page count increases by 68%, figures and tables total 149, up from 114 in 1997 NTRS - *not* mentioned is need for government involvement, instead focus is clearly on semiconductor industry and research communities to spur activity. Likewise, involvement of SRC and Sematech barely mentioned - system-on-a-chip (SoC) chapter addresses needs of fast-growing ICs in consumer and other markets driven more by cost (vs. technical) limits - return to 3yr node cycle, 6 nodes/ generations, but nodes pulled in 1yr - split of near-term (1999-2005 annual) and long-term (last 3 nodes 3yrs apart) years, high granularity applied to the annualized near-term metrics - Moore's Law defined as "the number of components per chip doubles every 18 months" - public website http://public.ntrs.net established
International Technology Roadmap for	434pp 64 figures 103+ tables	2001-2016, 130-22nm	- Repeats *manufacturable solutions are not known* in most cases shown within 5-year reach, refers to "Red Brick Wall"	- complete international ownership: *Jointly sponsored* by all 5 regions - includes demographic data on ITWG composition

Semiconductors, 2001			- States "*The International Technology Roadmap for Semiconductors (ITRS)* has been an especially successful worldwide cooperation" and "ITRS has improved the quality of R&D investment decisions made at all levels and has helped channel research efforts to areas that truly need research breakthroughs." - Includes a chapter called "System Drivers" that expands 1999 SoC chapter but more fully addresses changing *market* drivers - Significantly address post-CMOS devices - Describes rationale for pull-in of the ORTC to reflect true manufacturing reality for leading edge companies and products	- more detailed: 23% increase in page count, figures/tables count climbs to more than 167 - redefines status codes: *Manufacturable solutions exist, and are being optimized; Manufacturable solutions are known, Manufacturable solutions are NOT known* - Moore's Law for DRAMs to slow to 2x every 3yrs (4x/6yrs) due to return to 3yr node cycle - microprocessor equal to DRAM as technology driver - rounded vs. actual ITRS nodes - chapters on *System Drivers* and *Emerging Research Devices*
International Technology Roadmap for Semiconductors, 2003	614pp +32 appendix, 85 figures 122+ tables	2003-2018, 100-18nm	- For first time in 7 years (past 3 Roadmaps), "the *2003 ITRS <u>does not predict</u>* a further acceleration in the timing of introduction of new technologies as the industry struggled through the worst recession of its history." - However, notes an increase in 2003 ITRS global participation from 2001 ITRS (936 vs. 839), also provides insight on demographics differences across five regions (variations by industry sectors, technology focus, etc.) - PIDS section addresses technology needs of fast-growing RF and analog/mixed-signal *wireless* applications including group III-V compound semiconductor devices - *Emerging Research Devices* chapter expanded to include scaling non-classical CMOS devices to end of the Roadmap	- includes disclaimer on cover, "The ITRS is devised and intended for technology assessment only and is without regard to any commercial considerations pertaining to individual products or equipment." - significant level of detail/granularity: almost 50% increase in page count, figures/tables count exceeds 200 - new status color/code acknowledging temporary work-arounds added between yellow and red: *Interim Solutions are Known*  - more definition of metal half pitch metric, thus metal hpXX node indicator (e.g., *hp90* = half-pitch 90nm) official ITRS node definition - Moore's Law projected to slow further in DRAM to 4x/7yrs while MPU/ASIC set at 2x/3yrs, to be slightly faster than DRAM

When viewed chronologically, Table 10-3 is very revealing. One very noticeable point is *growing complexity*. The most obvious measure is the increasing counts in pages and figures & tables. The 2003 ITRS is three to four times the size of the 1992 Roadmap by these measures. Figure 10-4 shows the total number of Roadmap participants over time that also reflects growing complexity.

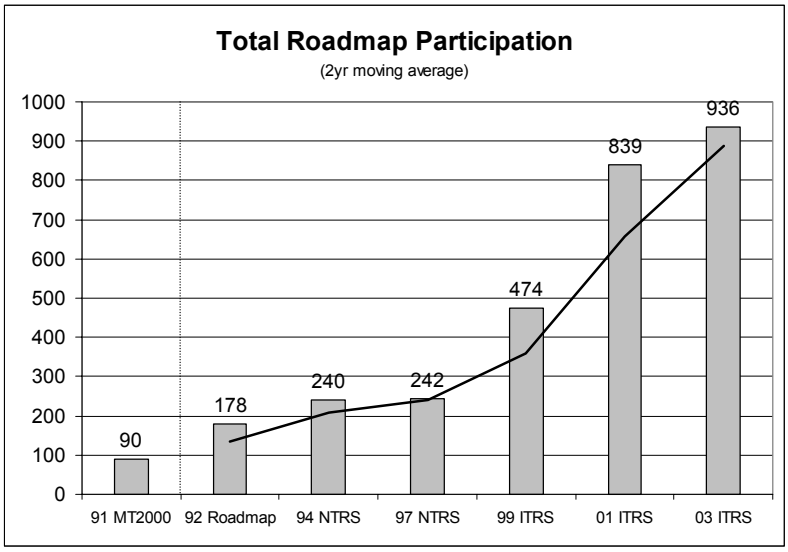

Figure 10-4. Total Roadmap Participation

Source: Micro Tech 2000 and SIA Roadmaps, various editions.

Moreover, the increased role of industry participation first noted in the 1992 Roadmap would continue to become more pronounced as shown in Figure 10-5.

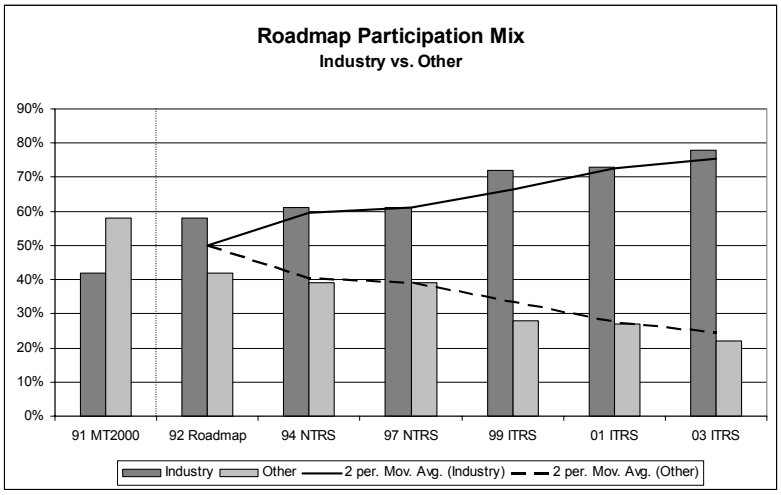

Figure 10-5. Total Roadmap Participation

Source: International Sematech. Note that *Industry* includes Chipmaker and Supplier while *Other* includes Consortia, University, Government, and Other (see Figure 10-11).

Less obvious is the impact from changes in major themes and characteristics of successive Roadmaps. One surrogate measure is the amount of trade press coverage as shown in Figure 10-6.

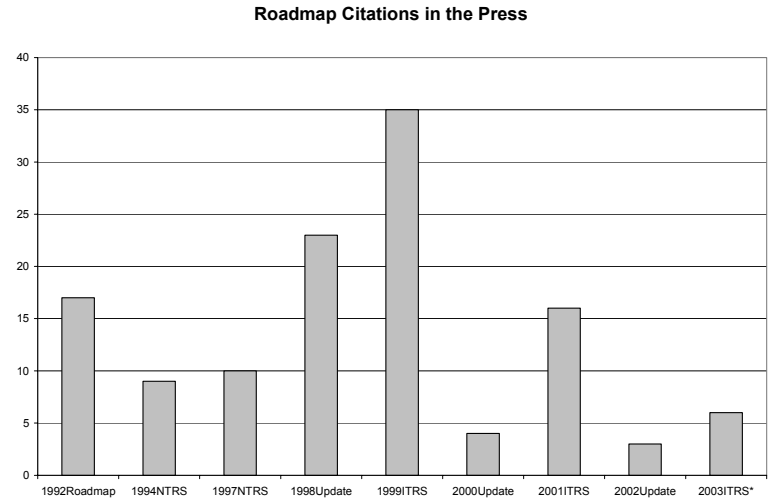

Figure 10-6. Roadmap Citations in the Press by Publication

Source: Author's Research, see Appendix D10-D, *2003 is partial (through February 2004).

While the citations graphed here are not a complete list, the trend suggests that press coverage has fallen considerably compared with earlier Roadmaps. The very noticeable spike in 1998 Update and 1999 ITRS coverage occurred because of the controversy and general interest regarding the transition to an *International* Roadmap, discussed later in the chapter. Discounting the great interest in the 1998 Update as this was the first such 'off-year' (even-year) update, the subsequent 2000 and 2002 Updates have attracted less attention than the publication (odd) years as expected. What is not captured here is the amount of international interest in non-U.S., certainly non-English publications.

More lengthy coverage such as academic articles and descriptive manuscripts, often contributed to by practitioners, have also fallen off considerably. For the 1992 and 1994 Roadmaps the author found thirteen publications, whereas for the 1997 and 1999 Roadmaps only six were found (see Appendix D10-C). The reasons behind the reduced outside interest are not clear except for a few specific reasons such as the transition to an International Roadmap as previously mentioned. One speculation is that the need to explain has reduced with time as the process has become more known. One contributing factor is the creation of a public website http://public.itrs.net in 1999 that has achieved a tremendous amount of success in terms of overall hits, visits, and download traffic as shown in the following figures and tables.

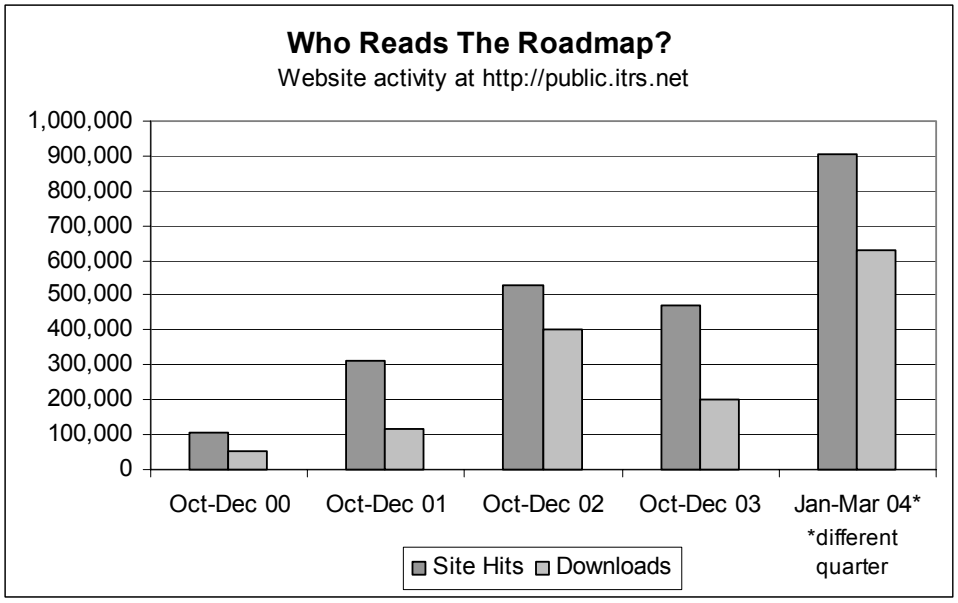

Figure 10-7. ITRS Public Website Activity

Source: http://public.itrs.net historical archives

Figure 10-7 shows significant increases in successful site hits and downloads (visitors can download individual ITRS chapter files in PDF format). Note that since the Roadmap is published in December of the odd years (e.g. December 2003), the bulk of download traffic occurs in the following quarter. This is why download activity in Jan-Mar 2004 total is more than triple the download activity for Oct-Dec 2003. Even more telling is the average Roadmap visits per day over the same period as shown in Figure 10-8 and Table 10-4.

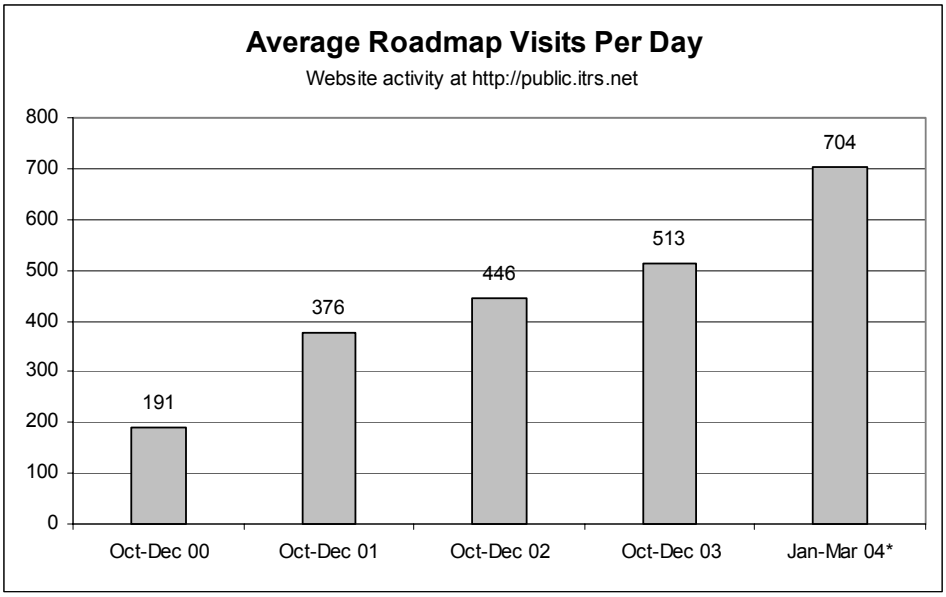

Figure 10-8. Average Roadmap Visits Per Day

Source: http://public.itrs.net historical archives

Table 10-4. ITRS Public Website Activity

	Oct-Dec00	Oct-Dec01	Oct-Dec02	Oct-Dec03	Jan-Mar04
Site Visits	17,805	35,031	41,487	47,257	64,068
Average per Day	191	376	446	513	704
International Visits	55%	54%	57%	56%	~55%
Visits from U.S.	45%	46%	41%	42%	~43%

Source: http://public.itrs.net historical archives. Note that a *visit* constitutes a longer view of a particular page whereas a *hit* is a simple raw count of entire site traffic. Thus *visits* may be a more valid measure of site interest. Also, international and U.S. visits averages may not add to 100% due to visits of unknown origin.

Finally, Tables 10-4, 10-5 and 10-6 demonstrate the global interest level in the Roadmap. Interestingly, in the top ten ranking of most active countries shown in Table 10-5, China (#7) and Australia (#8) are not sponsoring regions of the ITRS. Singapore (#12), also not a sponsoring region, is not far behind in interest. In sum, public internet access greatly assists in the diffusion of the Roadmap to both existing and potentially new regional participants.

Table 10-5. Most Active Countries, Oct-Dec 2003 Site Visits

Rank	Country	Visits	Rank	Country	Visits
1	United States	19,673	2	Japan	9,177
3	Taiwan	1,803	4	Germany	1,782
5	Korea (South)	1,495	6	France	1,188
7	China	1,122	8	Australia	1,053
9	Europe	1,000	10	United Kingdom	970
11	Canada	857	12	Singapore	745
13	India	552	14	Netherlands	474
15	Italy	355	16	Sweden	351
17	Belgium	330	18	Israel	292
19	Switzerland	220	20	Finland	216
				Total for these Countries	*43,655*

Table 10-6. Most Active Cities, Oct-Dec 2003 Site Visits

Rank	City	Visits	Rank	City	Visits
1	San Jose, California, U.S.	2,323	2	Tokyo, Japan	1,886
3	Herndon, Virginia, U.S.	1,873	4	Kanagawa, Japan	1,312
5	T'ai-pei, Taiwan	954	6	Santa Clara, California, U.S.	679
7	Middletown, New Jersey, U.S.	627	8	Singapore, Singapore	533
9	Austin, Texas, U.S.	504	10	Hsin-chu, Taiwan	452
11	Beijing, China	451	12	Atlanta, Georgia, U.S.	338
13	San Francisco, Calif., U.S.	319	14	New York, New York, U.S.	300
15	Milton, Australia	293	16	Isenburg, Germany	276
17	Taiwan, Taiwan	264	18	Cambridge, Mass., U.S.	258
19	Grenoble, France	233	20	Seoul, Korea (South)	230
				Total for these Cities	*14,105*

A brief look at the 2003 International Technology Roadmap for Semiconductors

The focus now turns to the 2003 ITRS, the latest Roadmap. Again, a quick scan of Table 10-3 and the preceding demographics tables reveals increased levels of complexity. At the same time, the two 'bookend' Roadmaps (i.e., 1992 and 2003) do share much in common. The 2003 ITRS reads in the *Introduction*:

> *The ITRS* … presents an industry-wide consensus on the "best current estimate" of the industry's research and development needs out to a 15-year horizon. As such, it provides a guide to the efforts of companies, research organizations, and governments.[1]

This statement—following "*The ITRS*"—could have easily been used in the 1992 Roadmap.

Box 10-3. Overall Roadmap Technology Characteristics (ORTC): 1992 vs. 2003[2]

1992 Roadmap Table 2.*

	1992	*1995*	*1998*	*2001*	*2004*	*2007*
Feature size (um)	0.5	0.35	0.25	0.18	0.12	0.10

* Entries in this chart are organized by date of production start up.

2003 ITRS Tables 1a and 1b.

Table 1a Product Generations and Chip Size Model Technology Nodes—Near-term Years

Year of Production	***2003***	***2004***	***2005***	***2006***	***2007***	***2008***	***2009***
Technology Node		***hp90***			***hp65***		
DRAM ½ Pitch (nm)	***100***	***90***	***80***	***70***	***65***	***57***	***50***
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm) ††	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
ASIC/Low Operating Power Printed Gate Length (nm) ††	90	75	65	53	45	40	35
ASIC/Low Operating Power Physical Gate Length (nm)	65	53	45	37	32	28	25

Table 1b Product Generations and Chip Size Model Technology Nodes—Long-term Years

Year of Production	***2010***	***2012***	***2013***	***2015***	***2016***	***2018***
Technology Node	***hp45***		***hp32***		***hp22***	
DRAM ½ Pitch (nm)	***45***	***35***	***32***	***25***	***22***	***18***
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	42	38	30	27	21

[1] *2003 ITRS*, 1.

MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	35	32	25	22	18
MPU Printed Gate Length (nm) ††	25	20	18	14	13	10
MPU Physical Gate Length (nm)	18	14	13	10	9	7
ASIC/Low Operating Power Printed Gate Length (nm) ††	32	25	22	18	16	13
ASIC/Low Operating Power Physical Gate Length (nm)	22	18	16	13	11	9

Notes for Tables 1a and 1b:

†† MPU and ASIC gate-length (in resist) node targets refer to the most aggressive requirements, as printed in photoresist (which was by definition also "as etched in polysilicon," in the 1999 ITRS).

However, during the 2000/2001 ITRS development, trends were identified, in which the MPU and ASIC "physical" gate lengths may be reduced from the "as-printed" dimension. These "physical" gate-length targets are driven by the need for maximum speed performance in logic Microprocessor (MPU) products, and are included in the Front End Processes (FEP), Process Integration, Devices, and Structures (PIDs), and Design ITWG Tables as needs that drive device design and process technology requirements.

In addition, during the 2003 ITRS development, an attempt has been made to reconcile the many published press releases by Logic manufacturers referencing "90 nm" technology node manufacturing in 2003. Since the metal 1 (M1) half-pitch of actual devices was cited at 110–120 nm, confusion arose regarding the relationship to the ITRS DRAM half-pitch-based header targets. After conversation with leading-edge manufacturers, it was determined that the public citations were in reference to an "indexed" technology node roadmap that represented the average of the half-pitch (for density) and the printed gate length (for speed performance).

The IRC has decided that the best way to minimize confusion between the ITRS and individual company public announcements is to identify the ITRS table header node with the industry's most aggressive half-pitch targets, and to label these targets as hpXX (i.e., hp90, hp65, hp45, etc.). Currently the industry's most aggressive half pitch is the DRAM cell metal half-pitch.

Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

Another common feature is the 15-year Roadmap horizon (see Box 10-2). Related to this, the master table referred to as Overall Roadmap Technology Characteristics (ORTC) provides top-down guidance for the roadmapping process today in much the same way as in 1992. Box 10-3 compares ORTCs of the two Roadmaps with respect to device minimum feature size.[3] A line has been superimposed that connects corresponding generations or nodes: 0.10 um which the 1992 Roadmap projected in 2007 is equivalent in value to 100nm actually achieved in 2003. In other words, the industry has reached the "end of the road," a target of one-fifth the geometric size of when it started in 1992. Likewise the latest Roadmap charts a future path that takes geometries down a similar order of reduction in the next 15 years.

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[2] *2003 ITRS*, Tables 1a and 1b, 41.

[3] Device minimum feature sizes are only one ORTC measure. Space does not allow a complete comparison. For instance, the 2003 ITRS ORTC consists of a set of ten tables of which only two are shown here. The complete 1992 ORTC table also includes other important parameters including gates and bits/chip, chip size, wafer diameter, no. of I/Os, etc. These factors are also included in the 2003 ITRS individual technology roadmaps. See Appendix D10-E as an example for Lithography.

While minimum feature size remains the key ORTC metric, one cannot help but notice the increased granularity in 2003 compared with 1992. Close examination of the *notes for tables* that follow the 2003 table sheds some light on, among other things, the difficulties in continuing application of the traditional 3yr generation timing as discussed in Boxes 10-2 and -4. Many of the more than 120 tables that appear in the 2003 ITRS are accompanied by similar notes. For example in Appendix D10-E see *Tables 77a and 77b Lithography Technology Requirements*, which are linked to the ORTC. The solid red boxes that appear in 2010 node hp45 have been colloquially referred to as the lithographic "red brick wall" when next-generation lithography (NGL) must be available to replace optical exposure tools which by then will have reached their limits.

Box 10-4. Technology Nodes: What's in a Name?

The definition of a technology node is far from precise. The ITRS continues to devote significant space—in text and graphics—to define and refine the concept. As the primary Roadmap metric, interpreting technology nodes is essential. However, it is no longer a simple matter. The past few Roadmaps have begun the explanation with the statement:

> The concept of "technology node" used to be quite straightforward to understand as it has historically been linked to the introduction of new Dynamic Random Access Memory (DRAM) generations with a 4× increase in bits/chip between generations. For as long as this cycle strictly followed Moore's Law (three-year cycle for 4×), the technology nodes and DRAM generations were essentially synonymous. However, in recent years, a greater diversity of products serving as technology drivers, faster introduction/optimization of product-specific technology, and the general increase in business and technology complexity are all tending to de-couple the many technology parameters that have traditionally characterized "advance to the next technology node."

In rendering graphics like Figures 10-10 and 11-1 especially, one of the challenges this author faced was the reliability and consistency of the minimum feature size metric. All attempts were made to compare like measures, but it was not totally possible due to differences in definitions, sampling times, etc. The author requested review by a few key Roadmap participants to help validate the findings. The following caption from Bob Doering, co-Chair of the U.S. IRC and long-time SIA Roadmap executive and participant, sheds important insight on the difficulties

of using technology nodes as an universal metric:

> [Figure 11-1 and accompanying text provide] a continuing detailed comparison between technology scaling trends from various sources. This is difficult in part due to the various definitions, not only of timing (e.g., "engineering samples" vs. "production"), but also of "minimum feature size." We continue to debate/modify these definitions in the ITRS process, but it is difficult to converge. There are different products, features, business models, and other complications which keep this from being very precise or even well-understood by the participants in the process. As one quick example, note that transistor gates are typically the smallest feature on some products, but this parameter is not very well related to the overall density which can be achieved in scaling CMOS. It is much more complicated now than twenty years ago, and trend charts which span that range of time often have a hidden "change of definition" on minimum feature size. We try to use the "minimum half-pitch on any level of any product" (typically DRAM metal-1) as the "node measure," but people keep trying to interpret the node definition in a favorable way to market their products. Thus, there is a lot of confusion. A few years ago, I recommended that we stopped using "node" as a Roadmap terminology. But, it seems to be too ingrained. People want to use it even if they don't really know what it means. So, you see the various company and other Roadmaps describing their "product technology nodes" very loosely. So, you need to look at these sources, including the ITRS, very carefully, or, at least, with a grain of salt.[4]

Interestingly, as imperfect as the technology node measure might be, Doering cites that "it seems to be too ingrained" to be changed. Similar statements have been made about the terms "roadmap" and even "Moore's Law." This says a lot about deep-rooted culture and tradition within this industry. Nonetheless, these terms continue to be used, even as they require more and more explanation regarding their proper interpretation and use.

Another point that Doering raises is the practice used by various company and other roadmaps describing their 'product technology nodes' "very loosely." This assertion was echoed from other sources. One Roadmap informant from an equipment supplier serving leading-edge chipmakers noted the misuse and stated flatly, "The Roadmap is now almost a joke because it is owned by marketing people, not technologists." This informant noted a certain "spin" in node names because they increasingly do not reflect reality. Specifically referred to was the then-current 90nm which was "not really where the industry is at, it's more like 120nm." Thus, technology nodes have lost some of their meaning as Doering suggests.

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[4] Bob Doering, e-mail to the author, October 8, 2002. Doering is a Senior Fellow at Texas Instruments.

Finally, a recent article dealing next-generation lithography (NGL) in a trade publication contained a useful discussion from the lithography community on the Roadmap node definition controversy. A section sub-titled "What is a node?" expands on Doering's earlier comments and is excerpted below.

What is a node?[5]

Part of the reason Intel figures on being able to extend dry ArF lithography through the 45 nm node is because of its interpretation of the ITRS. Traditionally, a technology node on the roadmap is dictated by the half-pitch of a circuit design. Although those are admittedly loose guides, Intel's roadmap shows a significant difference in numbers (Table 2). At the 45 nm node, Intel's logic chips are expected to have a half-pitch of ~75 nm.

Table 2. Intel's Logic Roadmap

Technology node	**90 nm**	**65 nm**	**45 nm**	**32 nm**
Year	2003	2005	2007	2009
Half-pitch (nm)	110	105	~75	~52
Gate length (nm)	<50	<35	<25	~15
Wafer size (mm)	300	300	300	300

(Source: Intel)

Source: Aaron Hand, "NGL Fights Through Economic Adversity," *Semiconductor International*, September 2003, Table 2, 66.

"It's almost a marketing kind of thing to decide which node you're going to call it. The customers expect that you're going to go from 130 to 90 [nm] and so on." said Nikon's [Gene] Fuller, who was involved in lithography at Texas Instruments. "My observation looking at quite a few roadmaps of different companies now for the last few years that I have access to is that everybody does it a little differently. When you look at the real internal product roadmaps, and what feature size they're going to have, they're all a little bit different, and they all reference the same ITRS."

"What is at this moment a node? There are no nodes anymore," [Paul] van Attekum argued, noting that ASML has customers and applications with half-pitches every 5 nm, or even every 2 nm. Ultimately, lithographers are more interested in a realistic, optimized solution than they are in a particular node. If you talk about the 45 nm node, then you have quite a different set of requirements if this is for a memory manufacturer than that same label for a microprocessor manufacturer."

The whole node concept may just diffuse away after 65 nm, mentioned Chris Progler, chief scientist at maskmaker Photronics (Allen, Texas), at the [July 2003] Lithography Breakfast Forum. Chipmakers will likely be more interested in fine-tuning cost vs. performance rather than trying to keep pace with the node system.

Although Fuller supports the concept of a roadmap, it's used more as a guide than a

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[5] Aaron Hand, "NGL Fights Through Economic Adversity," *Semiconductor International*, September 2003, 66.

> driver. "It's not the actual process plan of any given company," he said. "The only suggestion is the one that everybody says—that we're just stretching the truth a little bit when we talk about these nodes. I don't think it has to change, necessarily, but, if you ask anybody…they'll all acknowledge that the roadmap is a little bit out of whack right now."

Finally, continual advances in lithography technology have been and continue to be a key driver in realizing Roadmap goals. Figure 10-9 compares lithography roadmaps included in 1992 and 2003 Roadmaps. They are strikingly similar in format and approach, especially from a distance. However upon closer examination they tell different stories as much has changed in lithography in the past decade. For example, *none* of the longest-term (0.12um generation on lowest band) options projected in 1992 have come about as optical exposure methods have been stretched well beyond its perceived limits. More will be said about this shortly.

In this brief review, it has been shown that the 2003 ITRS embodies much from the 1992 Roadmap. A similar conclusion may be drawn if all intermediate Roadmaps are included in the analysis. Each is built upon the other and with each renewal cycle this becomes more evident. Linda Wilson, International Sematech Information Manager and ITRS managing Editor, has been involved in every Roadmap since the 1992 Roadmap and reflects on major themes:

> The overall theme of the various Roadmaps does not change much from the 1992 effort, which is that of shared vision. Also pervasive is a very strong message of need for affordable and cost-effective methods (processes/fabs) as well as the obvious interdependencies of the industry sectors and technology sectors. The sub-themes of what this entails in each Roadmap edition drives the maturation of the Roadmapping process from national to international and from a technology-specific, almost project planning [tactical] approach to a more integrated technologies systems approach.[6]

[6] Linda Wilson, e-mail to the author, April 23, 2002.

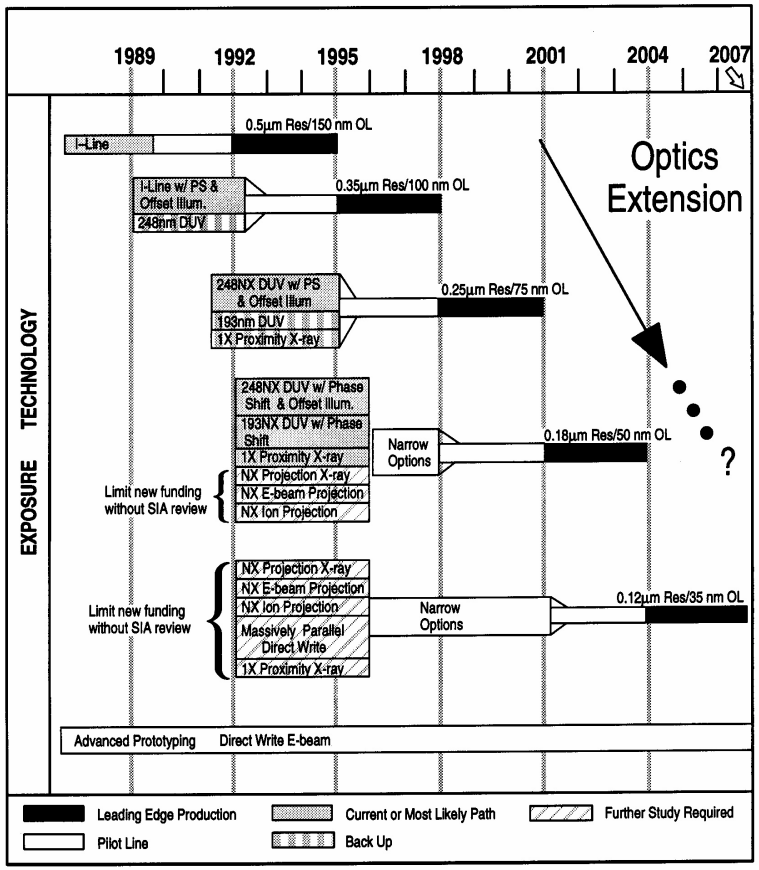
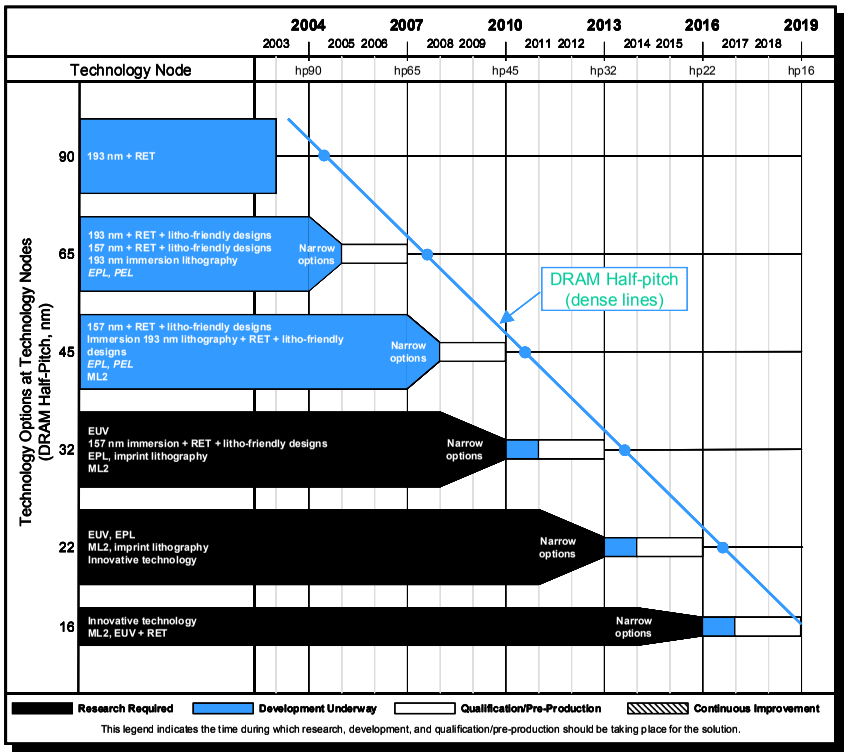


Figure 7 Exposure Technology Roadmap



Technologies shown in italics have only single region support.
RET—resolution enhancement technology EUV—extreme ultraviolet
EPL—electron projection lithography
ML2—maskless lithography PEL—proximity electron lithography

Figure 53 Lithography Exposure Tool Potential Solutions

(a) 1992 ROADMAP **(b) 2003 ITRS**

Figure 10-9. Comparison of Lithography Roadmaps: 1992 vs. 2003

Source: *1992 Semiconductor Technology Workshop Working Group Reports*, Figure 7, 38; *2003 ITRS*, Figure 53, 386.

1992-2003 Roadmaps: Noteworthy Developments

Studying the changing contents of the series of Roadmaps reveals much as described above. In addition, examining changes in the Roadmap process (e.g., participation demographics) provides further meaning. The opportunity to observe the Roadmap process in action along with dozens of informative interviews with participants gave the author considerable insight. However, this line of empirical analysis does not sufficiently explain the dynamic nature of the Roadmap—specifically how it affects change and is affected by change. The challenge is just how to do this. In choosing the case study method, the overriding goal is to investigate the Roadmap within its real-life context. To accomplish this, the final section examines three *noteworthy developments* involving the Roadmap. The three major developments analyzed in detail are: 1) technology acceleration, 2) international Roadmap, and 3) 300mm wafer transition. Out of all the possible major topics involving the Roadmap that could be examined these three were chosen based on the collective level of interest paid them from all the data sources including the Roadmap publications, interviewees, press coverage, or other archival materials. Further, each occurred at roughly the same time (or at least overlapped each other) and in fact, are in some ways interrelated. Finally, the author's field research was conducted within the timeframe when these topics were current, thus they helped inform the overall study. Again, this last section is intended to better characterize the Roadmap in action, for what it *does* (vs. what the Roadmap *is*), however in some cases the role of the Roadmap as influencer is debatable.

Technology Acceleration

Technology (or node) acceleration is perhaps the most discussed issue associated with the Roadmap. This was first observed following the 1994 NTRS as companies, by then familiar with the document, began referring to it when making product and process technology announcements. Leading edge producers such as Intel, Texas Instruments, Fujitsu, Samsung and others announced as early as 1995 that process technologies were advancing faster than

Roadmap targets. Further, interviewees suggested that the 1992 and 1994 Roadmaps took a more conservative approach in future projections and thus already lagged industry performance levels when they were published. Paolo Gargini, involved in the Roadmap since 1993 and the lead or co-lead on each Roadmap starting in 1997, has stated that the 1992 Roadmap "came at government's request from DARPA. The Roadmap was developed quickly in response." The value of the 1992 Roadmap was that it was a "neutral document" (i.e., no specific firms cited but everyone's reference was "based on the roadmap"). Also, everyone was showing afterward that they were "beating the roadmap." Gargini felt that these targets were "relaxed" based on government (vs. industry) as the primary user. He states for example that the technology cycle of the 1970s/80s was based on observation only (i.e., Moore's Law) and produced the historical 3yr cycle. According to Gargini, "Everyone was comfortable with that pace although it was obvious to some that this pace was based on conservative beliefs. One effect of this was the Roadmap wasn't really used by anyone other than DARPA." In sum, the first Roadmaps did represent consensus agreement on needs, but were mostly "useless academic exercises" as the primary purpose was for government funds, and the process was strongly driven by universities/national labs, *not* industry.[1] Demographics of Roadmap participants presented earlier support Gargini's view. As previously discussed, similar comments were also expressed regarding *Micro Tech 2000*.

Table 10-10 illustrates Roadmap node cycle acceleration. As a starting point, Table 10-10a shows all the technology nodes from each Roadmap beginning with Micro Tech 2000 (in shaded boxes since this is not technically part of the Roadmap series). Table 10-10b then links these nodes across successive Roadmap publications. By doing so node cycle acceleration becomes very evident in the 1997-2001 time period. This line of analysis is used again in a broader fashion in Chapter 11 (see Figure 11-1).

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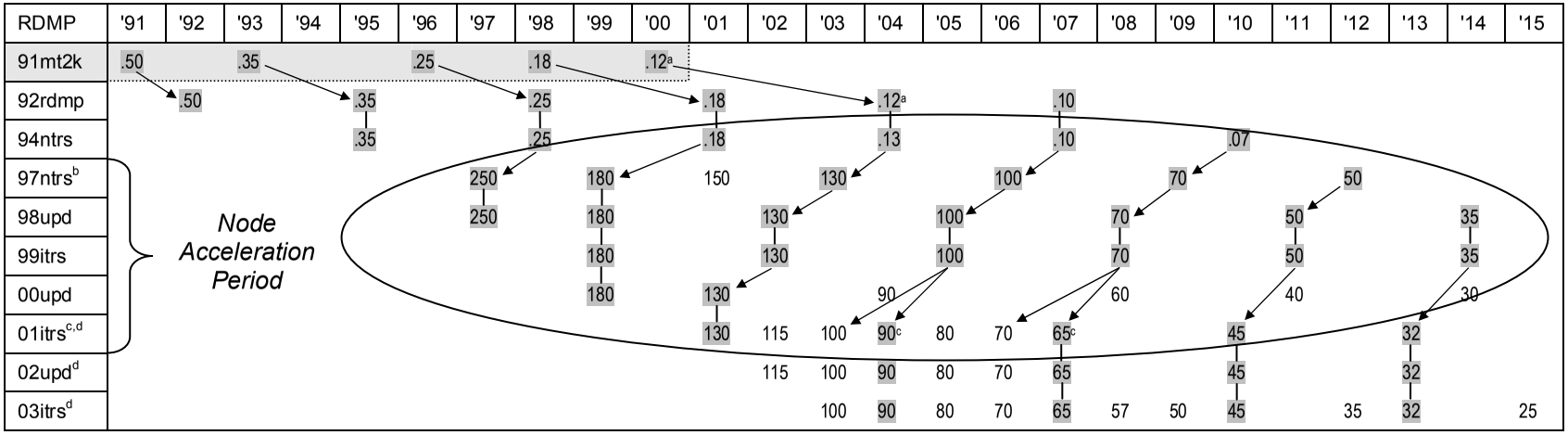
[1] Paolo Gargini, telephone interview, August 16, 1999.

Gargini's insights on conservative estimation offer an important but partial answer to the reasons behind node acceleration. The most cited technical reason was the extension of optical lithography which far predates the Roadmap era. As has been discussed in several places throughout this thesis, the limits to optical exposure methods, forecasted as early as 1977, have yet to be realized almost three decades later. Rebecca Henderson's (1995) research into the photolithography industry is referenced in Chapter 4's discussion of evolutionary theory. Henderson's catchy title, "Of life cycles real and imaginary: The unexpectedly long old age of optical lithography," captures the key point.

RDMP	'91	'92	'93	'94	'95	'96	'97	'98	'99	'00	'01	'02	'03	'04	'05	'06	'07	'08	'09	'10	'11	'12	'13	'14	'15
91mt2k	.50		.35			.25		.18		.12[a]															
92rdmp		.50			.35			.25			.18			.12[a]			.10								
94ntrs					.35			.25			.18			.13			.10			.07					
97ntrs[b]							250		180		150		130			100			70			50			
98upd							250		180			130			100			70			50			35	
99itrs									180			130			100			70			50			35	
00upd									180		130			90				60			40			30	
01itrs[c,d]											130	115	100	90[c]	80	70	65[c]			45			32		
02upd[d]												115	100	90	80	70	65			45			32		
03itrs[d]													100	90	80	70	65	57	50	45		35	32		25

(a)



(b)

Figure 10-10. Comparison of Roadmap Minimum Feature Sizes

Source: NACS Micro Tech 2000 and SIA Roadmaps, 1992-2003

Notes:

1. ORTC node metric changed from micron (millionth of meter) to nanometer (billionth of meter).
2. Early .12 targets were actually .125 (one-eighth micron), later target was rounded to .13 so both are considered the same.
3. Projected node dimensions were recalculated in the 2001 ITRS to conform more precisely to the traditional CMOS scaling factor 0.7x each node or 0.5x per 2 nodes. Nodes (in nanometers) are restated as follows:

1999 ITRS	130	100	70	50	35	25
2001 ITRS	130	90	65	45	32	22

   Thus, there are two arrows linking the .1 micron and .07 nodes from the 1999 ITRS with their respective nodes in the 2001 ITRS. The first arrow links with the same value 2001 ITRS node and is shaded for continuity. However, .1 (100nm) and .07 (70nm) are no longer official ITRS nodes. The second arrow links with the restated (and official) node values of .9 (90nm) and .65 (65nm) respectively.
4. Technology nodes for 2016-2018 are not shown due to page space constraints.

Considering the considerable R&D challenge in funding and expertise associated with NGL (e.g., IBM had spent "billions" on x-ray lithography before abandoning it; note also that DARPA was a key sponsor as Gargini points out), it is understandable why early Roadmaps, including Micro Tech 2000, placed emphasis on NGL. Extension of optical lithography tools has become such standard practice that "optics forever" camps have emerged as follows:

> Canon still maintains the pursuit of "Optics Forever," which, in general, affirms that after 248nm will come 193nm, and then 157nm—then EUV (a natural extension to optical projection lithography). In the next two years we will continue to apply our heavy investment in R&D for the 157nm and EUV generation, even knowing the big roadblocks to be overcome.[1]

Through creative engineering work, workaround methods or "tricks" such as Optical Proximity Correction (OPC, described in Chapter 6 Box 6.2) and Phase Shift Masking (PSM) are just two examples of how optical lithography continues to print ever-smaller feature sizes. The newest technique to emerge is the use of liquid immersion that might possibly extend DUV (Deep Ultraviolet) Lithography to the hp45 node scheduled in 2010 (see Table 10-4). Yet another important factor is better alignment of the complete *tool set* associated with lithography as suggested by Doering following the release of the 1999 ITRS:

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[1] Naoki Ayata, "The next two years," (Commentary) *Chilton's Electronic News*, Vol. 48, No. 9, February 25, 2002. (Naoki Ayata is a senior VP and general manager, Semiconductor Equipment Division of Canon U.S.A., Inc.) Also see Phillip Ware, "So many options, so little time: Why optics is forever in lithography," *Solid State Technology*, Vol. 43, No. 5, May 2000.

> The biggest surprise we've seen in the last two roadmaps, especially between 1994 and 1997, was how fast lithography was able to continue to push to smaller feature sizes. It wasn't just the steppers themselves but the other technologies associated with it—the photoresists that we use—and other aspects of lithography that enable us to move faster than anybody had imagined back in 1994.[2]

It is important to note that the optical lithography limit has always been about six years (i.e., 2 or 3 generations) into the future. A review of Roadmap lithography sections where limits are routinely stated is summarized in Table 10-4.

Table 10-4. The Roadmap and Optical Lithography Limits

Roadmap	*Optical Lithography Limit*	*Node Year*	*# Years to Limit*
1992	0.25um, maybe 0.18um	1998-2001	6-9
1994	0.18um (180nm)	2001	7
1997	130nm	2003	6
1999	100nm	2005	6
2001	65nm	2007	6
2003	45nm	2010	7

Source: SIA Roadmaps

The consequences of the "pull-in" effect have been substantial. One quick illustration that links the two "bookend" Roadmaps of the past decade together is the fact both shared the 0.10 um (100nm) generation/node, but as *different* markers: the 1992 Roadmap called for 0.10um feature size as the *last* node to occur (in 2007) whereas the 2003 Roadmap uses 100nm as its *starting* node. So the connection was made four years ahead of schedule as shown in Table 10-3. Figure 10-10 actually shows the full effect of node acceleration throughout the Roadmap era. Correlated with this, Box 10-5 contains the detailed survey findings from Appendix B for the free-form statement pertaining to the pace of innovation eliciting a detailed response from participants. It is presented here in total because this is one of the questions/statements modified as the field

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[2] Bob Doering, quoted in Tom Murphy, "The Brick Wall Will Crumble," *Electronic News*, November 29, 1999.

research began. Specifically, the phrase "and even accelerated" was included after preliminary research indicated this might be a major trend. According to these participants the Roadmap and technology acceleration were closely related.

Box 10-5. ITRS Survey: Regular, Predictable, *Even Accelerated* Pace of Innovation[3]

17. Hypothesis 1: The SIA Roadmap has contributed to a more regular, more predictable, *and even accelerated* pace of innovation through deliberate coordination of pre-competitive R&D and related industry resources.

There were 34 total responses to this question. They are categorized as follows:

Response Category	#	% of total
Agree	29*	85%
Disagree	2	6%
Other	3	9%
Total Responses	34	100%

* includes 2 strongly agree and 1 partly agree

These numbers overwhelmingly favor *Agree*. Perhaps more than any other single research question, respondents found strong association between the Roadmap and this variable under inquiry. Specifically, technology acceleration was cited most often as the definitive contribution of the Roadmap process. Even some of those classified as *Other* could be interpreted as somewhat in agreement. Those who explicitly disagreed cited specific situations that may or may not reflect an accurate perception of the overall purpose of the Roadmap. Some lengthy responses were broken up for ease of reading.

Agree that Roadmap has contributed to a more regular and accelerated pace of innovation

'Beat the Roadmap' behavior is often cited as central to explanation:

- Most have said that, if anything, it has accelerated the pace because it gives a benchmark, and right away people, with their competitive nature, want to beat it, so by constantly throwing it out there. We have an interesting situation though, because each year we make the Roadmap tougher: when we redo it, it gets pulled in, right? And then we have to beat an even harder goal. So it's a difficult environment that industry people live in - they all lament, "Oh God, I never worked so hard in my life!" That's an interesting phenomenon.
- Yes, and to the extreme, once milestones are defined, competitors attempt to design strategies to accelerate or 'beat the roadmap'.
- Yes, sure. by saying Moore's Law is going to happen, manufacturers will make it happen, thus always accelerating - writing it down, guarantees to be beaten.
- Yes, definitely pulled in pace of innovation ('beat the roadmap' behavior).
- Yes, has accelerated. Each company looks and tries to "beat the roadmap."
- Pull-in or "beat the roadmap" behavior the result of public knowledge of roadmap targets. Competitive firms trying to beat everyone else to the goal. Earlier targets, SRC goals, MT

[3] This also appears in Appendix B, Q17.

2000, etc. not really public or adopted broadly by industry so largely ignored.

- Technology acceleration: result of roadmap. Take a lesson from roadmap: write it down, then someone says "I can beat that," accelerating the pace.
- Roadmap is considered a standard and provided "line in the sand" - leaders would "step over it" or beat the roadmap.
- Has accelerated pace of innovation: benchmark for IC manufacturers to beat.
- Roadmap is goal/need "scorecard." Chicken or egg: observing or driving. Contributed to our understanding of the pace and what drives it - identification of pace: best snapshot in time.

Other reasons were also cited:

- Unqualified yes, look at semiconductor industry before and after, can measure.
- Strongly agree - business issues, sharing knowledge (anti-trust laws relaxed), way industry works
- Agree. There is a sense that innovation is accelerating and one can argue a roadmap allows for coordination that assists in the innovation process. Key barriers, technology nodes, etc. all ensure the chip makers and their suppliers are on the “same page.”
- Agree. The very fact that the Roadmap tends to be over run at each edition is *prima facie* proof of its success.
- I agree, because the certainty of the requirements provided by the Roadmap eliminates wasted time in trying to determine the technology requirements before solutions are developed. Additionally the Roadmap allows for elimination of programs which obviously result in technology which will not meet the requirements thereby reallocating scarce research funds to projects of higher potential. Finally, the Roadmap, through its consensus building process, not only generates the requirements but also automatically communicates those requirements to the entire semiconductor community.
- Agree, provides a guideline for collectively concentrating resources to focus (e.g., SIA focus center program in response to roadmap challenges) or (earlier) international competitiveness (when all needs laid out collectively).
- With roadmap, tendency is probably to accelerate change. Without a roadmap, most people would still know, but a roadmap makes it more apparent/visible to everyone. Don't use the prior (older) technology. Lowering production cost: economic bias, equations lean to new equipment/technology. Shrinks will continue (need concept/ideas to continue).
- Agree. The ITRS covering the wide range of technology thrusts gives trustworthy impacts to semiconductor community.
- Agree - yes it is Moore's Law 'insurance' - more than Moore's Law.
- Agree: common vision, visibility of common metric yields guideline.
- Yes, to some extent, but we do not have the nonexistent case to compare to.

<u>Disagree that Roadmap has contributed to a more regular and accelerated pace of innovation</u>

- Disagree - the forecast of the introduction of 300mm wafers on a time schedule that the full supply chain could not support was a very destructive result of consensus based planning (as opposed to reality based). Technology acceleration has really been the result of individual leading edge companies serving their own needs.

- Disagree - roadmap is political, dominated by a few, very strong companies like Intel. Everyone knows this and acts accordingly.

Other factors

- ITRS doesn't so much do it. But sitting down and sharing does it. AMD doesn't like acceleration, whereas Intel and DRAM companies like Samsung do like acceleration. DRAM design features size: all people sit down and talk, even Intel couldn't do it by itself.
- I think the overall acceleration is driven by factors beyond the roadmap and the semiconductor industry. Society's thirst for information - lots of it and lots of it now & for free - and efficient communication are the real drivers behind innovation… behind the road map itself. Innovation is market driven not necessarily technology driven.
- Also other issues critical - compare rate of change between pre-Roadmap and now. Roadmap has accelerated process: undirected activity had direction with imperative (no one telling), sets up problems. Not intended as an instruction manual, to set expectations, sort of guidebook, establishes a framework.
- Design engineers in semiconductor industry more isolated from process and other functions than in other industries (chemicals, autos) - reason is time (compressed internet time) narrows focus, no time to share, thus have to stay on target.

As in the extension of optical lithography, technology acceleration was not new to the industry.[4] Sematech is but one example where sustained 2yr node scaling was demonstrated. The primary reason was through close coordination with suppliers (e.g., sole-source contracts with U.S.-made GCA and SVG stepper systems early in its history, and similar arrangements later as International Sematech). Boxes numbered 1-5 in Table 10-5 show Sematech's combined operational plan phases (see Chapter 9) that projected (and later achieved) a 2yr node cycle. The last box was outside the planning horizon of the initial Sematech plans but shows that the 2yr node cycle continued as the organization transformed into International Sematech.

Table 10-5. Sematech Process Technology Progress

Plan Phase	*1*	*2*	*3*	*4*	*5*	*N/A*
Year	1988	1990	1992/93	1994	1996	1998
Goal (um)	0.8	0.5	0.35	0.25	0.18	0.13

Source: Phases 1-3 of Sematech I and 4-5 of Sematech II Plans from various reports on Sematech, 1998 data from *Sematech/International Sematech 1998 Annual Report*, 18.

[4] In fact, both functions are interrelated.

Note that Sematech was already a generation ahead of industry when the 1992 Roadmap was published (i.e., 0.35um vs. 0.5). This is understandable because this was part of their charter to assist the U.S. chip makers regain industrial leadership—as a research organization, they could (and should) pace ahead of industry. But the important point regarding the Roadmap is that Sematech's demonstration of accelerating the traditional pace to 2 years through focused effort showed what was possible in a way that validates Gargini's earlier suggestion of what many knew. In the meantime, leading-edge producers (including Gargini's Intel) were reporting that they were "beating" the Roadmap. In reality, many already had when the "conservative" 1992 Roadmap was published. Again, the major contribution—demonstrated by Sematech in a controlled (lab) environment—came from close coordination between chip makers and the equipment and materials suppliers in the development and implementation of new process technologies. With a consensus Roadmap that articulated a common set of needs, suppliers increasingly gained confidence to develop equipment and materials to a schedule with far less guessing and risk. This point was underscored repeatedly by Roadmap participants (see Chapter 11).

Given these considerations, technology acceleration or "pull-in" may not have been the correct descriptive label for what was really going on. A more appropriate label might be technology *calibration* or more precisely, *Roadmap calibration* with industry. This reality was increasingly reflected in successive renewals of the Roadmap and in fact in the latest Roadmaps—the 2003 ITRS in particular—technology nodes may indeed show a *faster* pace than reported in industry. This is due in part to changing device drivers described in Box 10-4 that bring into question the ongoing utility of technology node as a singular Roadmap metric. Linda Wilson has followed the "node timing" debate which has been central to RCG and later, IRC planning discussions since about 1998. She reflects on the difficulties that arise in finding consensus on such a basic, yet controversial issue:

> Changing timing every year is almost like beating a dead horse, but eventually it will be resolved. Timing has had too much attention. Once a pace is set then okay, there's a

> need to move on. Maintaining some sort of steady state vs. continuing to jerk timing around is a question the IRC is growing tired of asking.[5]

In fact, the 2002 Update, underway when Wilson's statement was made, did not accelerate node timing. This was the first time since the 1994 NTRS that generation/node cycle timing was not accelerated in the Roadmap. Furthermore, the 2003 ITRS continued this policy, declaring "The *2003 ITRS* *does not predict* a further acceleration in the timing of introduction of new technologies…" citing continuing industry recessionary pressures.[6] At the core of the node timing issue is increasing complexity as the scope of the Roadmap continues to broaden to accommodate a wider variety of international interests, which also means differences in device drivers and effectively, different Roadmaps. Katherine Derbyshire, Managing Editor of *Semiconductor Online*, who has covered the Roadmap in the trade press, has observed this trend:

> As the Roadmap gets broader in scope, then it's harder to serve everyone's needs such as different segments, families of devices, etc. The Roadmap is getting pretty unwieldy now, and is really three different roadmaps: memory, logic, and microprocessor. They are all going the same place, but at different speeds. The Roadmap is becoming more of a map vs. a "TripTik" which shows one route.[7]

Technology acceleration in the Roadmap, therefore, has many influencers. Changing device drivers is one of these and will be addressed shortly. It is closely related to the globalization of the Roadmap which is now discussed.

International Roadmap

The interest in international involvement in the Roadmap is commonly reported as occurring in early 1998 when a Japanese consortium declared it was developing a "competing" roadmap. One press account from March 1988 states:

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[5] Linda Wilson, telephone interview, February 20, 2002.
[6] 2003 ITRS, i, emphasis in original.
[7] Katherine Derbyshire, telephone interview, January 12, 2001. *TripTik*, a registered trademark of the American Automobile Association (AAA), is a customized "strip map" prepared for a road traveler's planned route.

> [T]he Japanese semiconductor industry is trying to form a "global" roadmap effort, which could upstage the SIA's National Technology Roadmap for Semiconductor… A global workshop will be held on March 8-9 in Kyoto by ASET (Association of Super-Advanced Electronics Technology), the Japanese R&D consortium, to discuss drafting a global roadmap for semiconductor generations with feature sizes of 0.10 micron and below.[8]

As a result, in April 1998 the SIA extended an invitation at the World Semiconductor Council (WSC), a trade body established as part of the 1996 U.S.-Japan semiconductor trade agreement renewal, to include international participation—on a trial basis—in the upcoming Roadmap renewal cycle. The offer was accepted by four trade associations:

- European Electronic Component Association (EECA), later European Semiconductor Industry Association (ESIA)
- Electronic Industries Association of Japan (EIAJ), later Japan Electronics and Information Technology Industries Association (JEITA)
- Korea Semiconductor Industry Association (KSIA)
- Taiwan Semiconductor Industry Association (TSIA)

The four groups participated in what the SIA ultimately deemed a successful "trial" and the *International* Technology Roadmap for Semiconductors was developed, first in 1998 as an ITRS Update,[9] and officially in a more complete 1999 Edition.[10]

No other Roadmap issue garnered more press attention than international participation (see Figure 10-6 spikes in 1998 and 1999 and Appendix D10-D). This is easily explained by the controversy involved, particularly toward Japanese participation as many SIA members expressed concern that it was only a decade earlier when deliberate actions were taken to block any such involvement. Some of these actions were still in place well into the 1990s. But the situation had changed considerably by the late 1990s. Wilfred Corrigan was Chairman and CEO of LSI Logic, had also served as SIA Board Chairman, and was chairman of the U.S. delegation

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[8] Jack Robertson, "Japanese push global roadmap that could replace SIA version," *Semiconductor Business News*, March 1998.
[9] The 1998 ITRS Update was actually released April 1999 along with the launch of a public website http://www.itrs.net/ntrs/PubIntrs.nsf later changed to http://public.itrs.net
[10] Technically, the 1999 ITRS was sponsored by the SIA "in cooperation with" the four other international participating organizations while the 2001 ITRS was "jointly sponsored by" all five participating organizations/regions.

to the World Semiconductor Council where he made the formal proposal for international participation. He offered the following perspective:

> We have come a long way from the mid-1980s when the word 'confrontation' was used to accurately describe the international relationship on semiconductors. Today, the word 'cooperation' accurately describes our relationships.[11]

Other SIA officials also acknowledged that taking this route might head off a move by other countries to develop their own competing roadmaps which could create confusion and possibly even throw the market into chaos.[12] For instance, one chief value of the Roadmap to semiconductor suppliers is that it is a single-source consensus of needs from chip makers, their customers. If a competing roadmap were developed with differing needs, timing, etc., suppliers might react with uncertainty and possibly disrupt the coordination benefits afforded by a single source. Given considerations such as these, the SIA agreed to expand participation internationally.

Other forces were also at play. The idea of international participation actually dates back to the start of Sematech a decade earlier where several of the strategic workshops pointed to international involvement, especially since much of the supplier infrastructure had by then become global. Turner Hasty recalls the discussions about international involvement at the time. He and others saw it as "natural" way to go, but it was not the time or place for serious consideration:

> Most larger companies had similar roadmaps [to the early Sematech technical workshops]. Sematech needed to see a broader view than these so it was natural to go international. We saw the international perspective early, but it was not only politically incorrect, but also strategically incorrect at the time [to pursue].[13]

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[11] Wilfred J. Corrigan, quoted in Jim DeTar, "SIA Seeks International Roadmap," *Electronic News*, Vol. 44, No. 2215, April 20, 1998, 1, 65, emphasis in original.
[12] Jim DeTar, "Globalizing the semiconductor business," (commentary) *Electronic News*, Vol. 44, No. 2216, April 27, 1998.
[13] Hasty interview, op. cit.

Obi Oberai echoes Hasty's view, "We needed Canon, Nikon, and others to progress, but could not do anything about it."[14] By the early to mid 1990s this view became more accepted. Perhaps the deciding factor was Sematech itself, when in October 1994 the consortium decided to no longer accept federal funding starting in 1996. With much fanfare William Spencer, Sematech CEO, affirmed:

> The industry can afford to support the consortium and we should. We are setting an example for other U.S. industries and for the world. We never intended direct federal funding to become an entitlement program.[15]

While this unprecedented move was generally covered as a successful completion of a model private-public partnership, the motivation behind the change is that government funding by then had become as much a liability as an asset to the organization. So long as Sematech was under the guise of federal funding and oversight, international membership was practically prohibitive. By the early 1990s the entire semiconductor industry was unquestionably international and growing more so every year. All of Sematech's members had either international operations or had formed strategic alliances with international partners. This was the real catalyst for *International* Sematech and a closely-related *International* Roadmap. According to Roadmap participants the international issue generated noticeable attention during the 1994 *National* Roadmap workshop, however no mention is made in the document itself. In an SIA press conference for the release of the 1994 NTRS, Craig Barrett, then Intel COO and SIA Technology Strategy Committee Chairman, stated:

> The industry is becoming increasingly international as we move forward. My guess is you will see this (SIA Technology Roadmap) to have an increasingly international content moving forward. There is no formal framework at this time but the SIA had had communication with its international counterpart. Sematech has had communication with its international counterpart. You will see increasing international cooperation in the future.[16]

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[14] Avtar "Obi" Oberai, telephone interview, May 1, 2000.
[15] William Spencer, quoted in "Topic of the Times," *New York Times*, October 12, 1994, reprinted in Browning and Shetler, op. cit., vii.
[16] Jim DeTar, "SIA accents funding issue in tech. roadmap update," *Electronic News*, Vol. 40, No. 2043, December 5, 1994, 2(2).

Barrett was not alone in arguing for international participation. Shortly after this William Spencer, Sematech CEO and Tom Seidel, Sematech Chief Strategy Officer, stated in an invited paper presented to a conference in China:

> [T]here seem to be many areas where setting international priorities might make sense… The development of these science and technology roadmaps should not be a one-time effort, but a continuing effort by the best science and technology talent in the world. The roadmaps for particular technologies should be led by industry with international participation.[17]

Finally, Sam Harrell, Tom Seidel, and Bernard Fay, all from Sematech, stated in a paper under a paragraph titled "Roadmapping the Semiconductor Future":

> There is likely to be international cooperation on a broader basis, since the cost of each core competencies is rapidly rising. The semiconductor business is international. Therefore, the SIA and Sematech have made the NTRS openly available worldwide. All of us must do our best to move our industry ahead.[18]

These last two references (and most likely the first one) were public indications that Sematech was becoming an international organization, thus an international Roadmap was a logical next step. When the international Roadmap issue surfaced in the press a few years later it was probably not much of a surprise to the SIA, Sematech, and their members. The bigger question raised by the SIA was not why but how. Specifically, how could participants located around the globe in different time zones who speak different languages adhere to the tight Roadmap development schedule already underway? As it turned out international participation, while difficult at first, continued to improve and contribute to a more complete Roadmap, the ultimate goal. Evidence of this is clear in Tables 10-4 and 10-5. Figure 10-11 is the first graphic that appears among 85 in the 2003 ITRS and shows the composition of Technology Working Group members by region and affiliation (i.e., industrial sector or function). Note that 58% of all members are non-U.S.A. This is further evidence that the "SIA" Roadmap has become truly international.

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[17] W.J. Spencer and T.E. Seidel, “National Technology Roadmaps: The U.S. Semiconductor Experience,” invited paper (Conference in China), approximately 1995, 219.
[18] Sam Harrell, Tom Seidel, and Bernard Fay, “The National Technology Roadmap for Semiconductors and Sematech Future Directions,” *Microelectronic Engineering*, Vol. 30, 1996, 12.

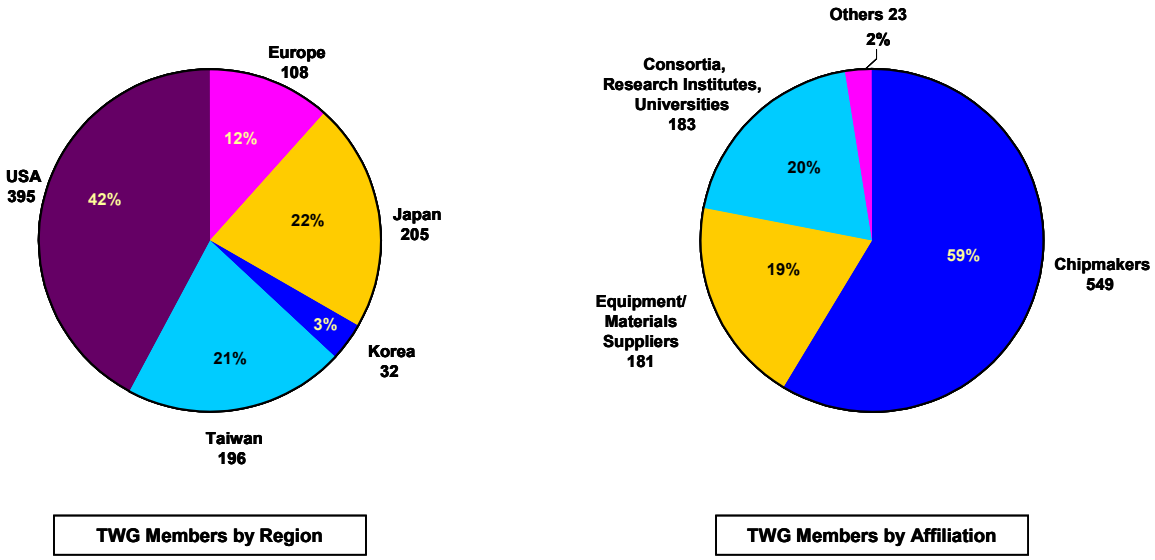

Figure 10-11. Composition of the 2003 ITRS TWGs—936 Global Participants

Source: 2003 ITRS, Figure 1, 6. Also appears as Figure 3-4.

Box 10-6 includes direct insight gained from Roadmap participants regarding the transition from a *national* to *international* Roadmap. The survey was done primarily in the 1999-2000 timeframe when international participation was relatively new. Despite this early assessment, the findings do reveal a generally positive opinion regarding the transition while offering some specific explanatory comments.[19]

Box 10-6. ITRS Survey: Advantages and Disadvantages of *International* Roadmap

As part of the ITRS Survey administered by the author, a question was asked specifically about the advantages and disadvantages of an *International Roadmap*. Evaluation of international involvement was not one of the research hypotheses, however Hypothesis 3 evaluates "global strategy in the late-1990s to stay on the industry's productivity curve." The researcher became involved as the 1998 Update was nearing completion and the 1999 ITRS was starting up. As this was the critical "trial" period of whether international participation could work, it

[19] See Appendix B, Q29 for detailed findings.

only made sense to probe the international aspect. The question below was asked of respondents. Summarized responses from the detailed findings in Appendix B follow.

29. What are the major advantages and disadvantages of an *International* Technology Roadmap process as compared with a *National* Technology Roadmap process?

There were 34 responses to this question. Several responses gave both advantages and disadvantages. Further, some gave multiple reasons. For this analysis combined replies were separated and classified as follows. Note that even after this breakdown, advantages perceived by the respondents almost doubled the amount of disadvantages stated.

Advantages	33	65%
Disadvantages	18	35%

The detailed findings of both categories follow, preceded by summaries.

Advantages of an *International* compared with a *National* Technology Roadmap process:

Reason	#	%
Global technology and industry	10	31%
Broadened involvement, scope, and cooperation	7	21%
Worldwide consensus	6	18%
Diverse technologies	5	15%
Added knowledge	5	15%

Global technology and industry: International roadmap is a good thing: technical issues are common (electrons don't know cultural boundaries), Roadmap in the future: more inclusive, more participation, more consensus (international device makers and tool makers) - Infineon, TSMC, etc. felt intimidated at first, now more comfortable.

Broadened involvement, scope, and cooperation: As cost of R&D gets higher, roadmap will gain in importance, solidifying need for international involvement. Greater pooling of resources and coordination to contain exponential cost increases.

Worldwide consensus: Worldwide perspective, global participation.

Diverse technologies: It becomes less likely that one semiconductor manufacturer will dominate the roadmap process. Also different global regions broadly represent different industry segments i.e. DRAM manufacture is concentrated in Korea, foundry manufacture is predominantly in Taiwan and Singapore.

Added knowledge: International is a better "standard." More sharing is better, more productive in setting right targets - not stuck on past paradigms.

Disadvantages of an *International* compared with a *National* Technology Roadmap process:

Reason	#	%
Logistics more difficult	7	39%

Cultural differences complicate process	6	33%
Loss of competitiveness	4	22%
National security risk	1	6%

Logistics more difficult: Greater difficulty in maintaining consensus building: non-linear confusion factor. Always have the danger of committees designing camels instead of horses - the bigger the committee and the more language problems, the uglier the result.

Cultural differences complicate process: Cultural styles make it a challenge (e.g. U.S. vs. Japan). Japanese example of international barriers: Japanese decision-making process very different than U.S. "let's cut to the chase" method. A certain level of frustration is built in. More difficult to get consensus. Note: in reality not consensus, but compromise, e.g., technology "nodes" terminology vs. Japanese "generation." What year .13 micron? 2001 or 2002, compromise - not necessarily consensus.

Loss of competitiveness: Concerned about international involvement: competition ("trying to do it better" incentive) is essential to innovation - competition in technology is key driver; if everyone participates, then no competition - can't have a big "love-in." Are we better off with "competing" roadmaps from different countries?

National security risk: There may be a long-term strategic risk militarily in going with an International Technology Roadmap process.

Finally, a major reason for the Roadmap's increased complexity and granularity described earlier in the chapter is the inclusion of global participants. One advantage given in Box 10-6 is labeled *diverse technologies*. The early Roadmaps were DRAM-centric because this device was traditionally the acknowledged technology driver because of its relatively simple design that also represented a significant percentage of world chip sales. Recall that the regularity in DRAM scaling forms the basis for Moore's Law (i.e., 4x increase every 3yrs). With time, changes in market demand shifted to other products such as logic-based microprocessors and ASIC devices. Traditionally, these products would lag DRAMs in process technology because they are more complex designs and represented smaller production volumes. This shift had already begun before the Roadmap became international, however the transition only magnified the trend. While the U.S. was the dominant producing region in microprocessors, they were weak in DRAMs and other devices. Bringing on board Japan and Korea particularly helped strengthen DRAMs while Taiwan's inclusion strengthened ASIC devices, many of which were made by foundries.

A recurring theme throughout the evolution of Roadmaps is the change in device drivers as logic products have gradually closed the gap on DRAMs. This has been another key contributor to the node cycle acceleration discussed earlier. Effectively the gap has been closed and, if anything, DRAMs are beginning to trail logic product families. The 2003 ITRS states, "With this 2003 Roadmap it is recognized that DRAM and microprocessor products share the technology leadership role."[20] Figure 10-12 compares the scaling trends of the three major Roadmap product classes (i.e., DRAM, MPU/microprocessor, and ASIC).[21] It is very clear that DRAM scaling has slowed while logic-based device scaling has accelerated. Coupled with the fact that logic-based devices represent an increasing share of world production and sales, the changing product mix has also contributed to node timing acceleration discussed earlier.

One contributor to the change in product mix is the maturity of the PC industry, long the largest user segment for ICs, predominantly for DRAMs and microprocessors. As average unit prices for PCs fell below the $1000 threshold by the end of the 1990s (and continue to fall, now close to half of that figure), cost became a larger driver than performance. As a result, chips for handheld and wireless applications such as ASICs and DSPs increasingly became more important. The 2001 and 2003 Roadmaps acknowledge this trend in a new chapter called "System Drivers." Another interesting point shown in Figure 10-12 (and partly a consequence of changing system drivers) is the gradual slowdown of Moore's Law, as traditionally measured by historical DRAM scaling. Note that the bit density doubling rate had started to stretch out the 18-month doubling rate (see Chapter 8) with the 256Mb chip in 1999, but it is the 1Gb chip, just recently qualified, that has stretched the doubling rate out to 2 to 2½ years (see Appendix C-3). Later this decade the doubling rate is projected to exceed 3 years.

The last few paragraphs illustrate the interrelatedness of the transition to an international Roadmap and the technology acceleration trend discussed earlier. Likewise, the third

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[20] 2003 ITRS, 40.
[21] Note that these three traditional Roadmap product classes have since been further defined and expanded in a chapter called "System Drivers" in the 2001 and 2003 Roadmaps.

development, 300mmm wafer transition, is also related but in a different way. While these first two major Roadmap developments focused primarily on the interests of chip makers, the third addresses the needs of another important Roadmap constituent group, namely the supplier community.

(a) NTRS/ITRS DRAM Bits/Chip Projections

TRS[a]	'95	'96	'97	'98	'99	'00	'01	'02	'03	'04	'05	'06	'07	'08	'09	'10	'11	'12	'13	'14	'15
1992	64M			256M			1G			4G			16G								
1994	64M			256M			1G			4G			16G			64G					
1997			64M		256M		1G		1G			4G			16G			64G			
1999					256M		512M		1G		2G						16G				
2001							512M	512M	1G	1G	2G	2G	4G			8G			32G		
2003									1G	1G	1G	2G	2G	4G	4G	4G		8G	8G		16G

4x/3yrs 4x/4yrs 4x/5yrs 4x/7yrs

(b) Logic/MPU (High-volume: Microprocessor) in millions of transistors/cm^2

TRS[b]	'95	'96	'97	'98	'99	'00	'01	'02	'03	'04	'05	'06	'07	'08	'09	'10	'11	'12	'13	'14	'15
1994	4			7			13			25			50			90					
1997			3.7		6.3		10		18			39			84			180			
1999					6.6	9.4	13	18	24	33	44			109			269			664	
2001							38.6	48.6	61.2	77.2	97.2	122.5	154.3			309			617		
2003									61	77	97	122	154	194	245	309		490	617		980

4x/6yrs

(c) Logic (Low-volume: ASIC) in millions of transistors/cm^2

TRS[b]	'95	'96	'97	'98	'99	'00	'01	'02	'03	'04	'05	'06	'07	'08	'09	'10	'11	'12	'13	'14	'15
1994	2			4			7			12			25			40					
1997			8			14		16		24		40			64			100			
1999					20	28	40	54	73	99	133			328			811			2000	
2001							89	112	142	178	225	283	357			714			1427		
2003									142	178	225	283	357	449	566	714		1133	1427		2265

4x/6yrs

Figure 10-12. Comparison of Roadmap Timing Changes in Transistor/Bit Density Projections by Major Device Type

Notes:

a. 1992 and 1994 Roadmaps used *date of production start up* and *year of first DRAM shipment* respectively, whereas 1997 and subsequent Roadmaps use *generation at production (ramp)* as planning assumption. Thus, comparing 1997 with 1994 data will be skewed farther out by one (4x) generation, however from 1997 on this is not the case.

b. 1992 Roadmap did not measure these values.

c. Technology nodes for 2016-2018 are not shown due to page space constraints.

300mm Wafer Transition

Perhaps the one Roadmap development most recalled by the supplier community in particular was the delayed transition to 300mm (12-inch) diameter wafers. This topic has been previously discussed, especially in Chapter 3's discussion on increasing complexity. One consequence of technology acceleration, especially occurring during an industry downturn, was an interruption in the traditional industrial cadence described in earlier chapters. This led Paul Peercy, then-President of SEMI/Sematech, to reflect on in an article cleverly titled, "Of rough seas, forecasts, and courses to plot," in late 1998.[1] Peercy, speaking for the supplier community, described the potential disruption in tool development plans that were based primarily on Roadmap projections. Others would raise similar concerns.[2] Within a year SEMI/Sematech initiated an "Infrastructure Roadmap" effort intended as a formal response to the ITRS that would provide "a balanced technical and business analysis of the requirements for critical technologies in the Roadmap."[3]

Meanwhile, SEMI, the SM&E industry's trade organization, had joined in the effort (along with counterparts from Europe and Japan) and assigned SEMI Board member, Jim Greed, to direct the assessment. Greed possessed extensive background in the SM&E industry while also an active Roadmap participant that dated back to the early Sematech workshops described in

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[1] Paul Peercy, "Of rough seas, forecasts, and courses to plot," *Semi/Sematech News*, Fourth Quarter 1998, 1.
[2] Author unknown, "Suppliers ponder whether chip technology map is road to ruin," *MICRO Magazine*, January 2000.
[3] "Global suppliers initiate response to SIA Roadmap," *Semi/Sematech News*, Fourth Quarter 1999, 1.

Chapter 9.[4] Greed observed a trade-off between supplier and international participation in the 1999 ITRS:

> Capital equipment and material suppliers' participation in the roadmap development process increased … through the development of the last national roadmap in 1997. A set of rules describing the composition of the Technical Working Groups (TWGs) developing the plan was specific as to the inclusion of suppliers. As the effort moved to the international scene, the rules shifted somewhat. The ITRS control groups opted not to impose rules for TWG composition on the new regions joining the process. To some elements of the supplier community, it seems as if supplier input was reduced during development of the first international roadmap.[5]

Greed would later expand, "The [National] Roadmap was the crowning success of Sematech in 1995-96. Device makers and suppliers were by then together enough."[6] But as the interest and attention in an international Roadmap intensified, especially following the publication of the 1997 NTRS, U.S. supplier interests seemed to diminish. The supplier community was by then even more global than its customer, the chip making industry. Several interviewees pointed to this (i.e., involvement of foreign suppliers) as rationale behind an international Roadmap. But trying to accommodate all interests while maintaining (actually hastening) an already-tight Roadmap production schedule proved challenging at the very least, while to some in the supplier community it proved very disappointing. Then came the 300mm debacle when "fighters went back to their corners" per Greed.[7]

Box 10-7. Device Maker - Supplier (customer-vendor) Relationships: A Look Back

Animosity between device maker and supplier sectors in the U.S. semiconductor industry is certainly not new. Distrust comes from many sources, one of these being intellectual property (IP) concerns. This is why traditional sector relationships have been at arm's length. As background

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[4] James Greed was former president of VLSI Standards. Greed also participated in the 1992, 1994, 1997, 1998 Update, and 1999 Roadmaps. He was formerly with General Signal Corporation (parent company of GCA that innovated the optical wafer stepper) and member of the Equipment/Process Working Group in the 1987/88 Sematech workshops. He is the author of "Sematech 200mm Implementation Workshop: Report of the Working Group on Process and Equipment Requirements," Dallas, Texas, August 10-11, 1987.
[5] Jim Greed, "A Supplier's Perspective on the International Technology Roadmap," *Semiconductor Magazine*, Vol. 1, No. 5, May 2000, 15.
[6] Jim Greed, telephone interview, August 2, 2000.
[7] Ibid.

consider these two perspectives from the 1980s:

> "One of the advantages that the Japanese companies have always had is their strategic alliances with their vendors. There is a very close working relationship. In fact, we have always had closer working relationships with our Japanese [device maker] customers than we have [with] our U.S. customers. U.S. customers would traditionally get the equipment in their plants and then pull down the curtain and make believe that their capability and process gave them some kind of an advantage, so they wouldn't tell anybody about it." (supplier)[8]

> "Finally, after a lot of acrimony, one of the [device] company guys, who happened to be the head of intellectual property for one of the big companies, gets up and says, 'Look, I don't want to take any more of this… We all know you equipment guys are thieves, you've been stealing our technology for years, and we're the ones who are keeping you guys in business. I'll be damned if we're going to finance this, and turn it all over to you.' When he said, 'we all know you're a bunch of thieves,' everybody said, 'yeah.' It really captured the essence of the relationship between the supplier and producer in American industry." (device maker)[9]

On balance, these are set-up views that follow with counter arguments as follows:

> "We have seen strong interest from our U.S. customers in forming strategic alliances with equipment vendors and we are working with a number of them. They have recognized the process interdependence and the degree to which they are dependent on their equipment suppliers for not only the equipment, but also process knowledge and support… They want tight working relationships with their vendors, including process involvement and support in meeting their strategic objectives. These actions by the device industry will certainly force a restructuring of the semiconductor equipment industry." (supplier)

> "That [view] has changed dramatically. It is one of those soft changes, but it is one of the most significant changes in how the U.S. [semiconductor] industry performs... An infrastructure that supports everybody." (device maker)

While relations between the two sectors have improved considerably compared with the first set of accounts in Box 10-7, it did not take much to regress—and the falseness in the Roadmap's 300mm projection caused a rift in this relationship. Because of this, the SIA commissioned Arthur Anderson as a third party to conduct qualitative interviews and quantitative surveys of both sides in preparation for a 300mm Lessons Learned Report. According to Greed, the supplier

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[8] Larry Hansen, quoted in E.F. Hutton & Company Inc., "E.F. Hutton Semiconductor Production Equipment Forum," September 1986, 91. Hansen was Executive Vice President, Varian Associates at the time.
[9] Clark McFadden, personal interview with Larry Browning, May 28, 1993, Sematech Archives. McFadden provided legal counsel to the SIA and was recalling a chipmaker representative's comments in a meeting attended by lawyers from both device making and supplier companies. Quote was later used in Browning and Shetler, op. cit., 37 (draft).

community was not as upset about technology acceleration as much as that it was explained after the fact, after the Roadmap was published. It was more a communications issue.[10] In the Roadmap's defense, Mark Melliar-Smith, Sematech's CEO stated, "The road map cannot be a whipping boy. It has been a very, very useful instrument."[11] Sematech had, in fact, initiated a series of high-level meetings between device manufacturers and global suppliers referred to as Industry Executive Forums (IEFs) that began in June 1999. Several of these forums were held and even scheduled around important Roadmap planning dates so that information could be shared and considered.

In terms of Greed's assignment, there was difficulty coordinating a very diverse global supplier community response because of the fragmented industry structure. Thus the "Infrastructure Roadmap" idea was dropped and instead, an alternative approach was taken to identify critical Roadmap needs in the areas of etch, PVD, lithography, and metrology. Greed presented the study's findings at an IEF in December 2000 that coincided with the release of the 2000 ITRS Update. As an appeal for more Roadmap participation, his concluding slide simply states:

> Development of a RESPONSE is much less efficient than direct PARTICIPATION in Roadmap development.[12]

Greed noted differences in the "volume" of response between the two segments, but assessed an overall positive outcome.[13] By this time both sectors had made considerable headway in rebuilding relationships. The Roadmap process had been amended, and was mutually acknowledged as the basis for dialogue.

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[10] Greed interview, op. cit.
[11] Mark Melliar-Smith, quoted in David Lammers, "Chip-Gear Leaders Draft Road Map…" *Electronic Engineering Times*, Issue 1068, July 5, 1999.
[12] Jim Greed, "Infrastructure Response to the 1999 ITRS," (PowerPoint presentation) Japan, December 8, 2000, 44, emphasis in original.
[13] Greed interview, op. cit.

Finally, from a Roadmap participant's viewpoint, Box 10-8 contains analysis from Appendix B detailed findings that offers a good summary explanation of the 300mm transition issue and context.[14]

Box 10-8. ITRS Survey: #2 Weakness of the Roadmap Process—Supplier Participation

When the bulk of the field work for this study was conducted in 1999 and 2000 much attention was devoted to the international transition of the Roadmap. At the same time another major development, however more concentrated, involved the industry's transition from 200mm (8-inch) to 300mm (12-inch) wafers. Compared with the International Roadmap, the transition to 300mm did *not* go as smoothly. In fact, the Roadmap was cited as a (some said *the*) key reason for the problem. Many from the supplier community in particular came to "blame the Roadmap" for projecting a need for larger wafers before they were needed. The analysis below captures the sentiment at the time. Note that if the question was asked and answered again, chances are the perspective would be much different.

31. Similarly, name two (2) weaknesses of the SIA Semiconductor Technology Roadmap process.

There were 42 responses to this question which is considerably more than the previous "name two strengths" question. Furthermore, several respondents provided more than two answers, bringing the total weaknesses listed to 91, almost double the total of the strengths list (50). There was even a wider variation in the wording of individual replies compared with the previous question. However some patterns still emerged allowing classification into major categories as shown below. In several cases a stated weakness could be considered in more than one category, but the most likely one was selected. Once again, the actual percentage breakdown by category might be different if reconsidered. Even so, the two most-cited weaknesses were:

1. Stifles innovation or emphasizes only incremental innovation
2. ***Participation inadequate or imbalanced (especially supplier community)***

One point worth noting is the unmistakable influence the 300mm wafer diameter transition had on the overall credibility of the Roadmap and reflected in these responses in particular. The 1994 NTRS had projected the need for 300mm wafers by 2001 while the 1997 NTRS accelerated this requirement to 1999. The key driver for this was the trend in increasing chip size. Implementing a new wafer diameter necessitates an entirely new tool set and in fact, a new fab. This is a very costly venture (some have estimated the total cost of 300mm transition upwards of $10 billion industry-wide) and the burden lies heavily on the tool (equipment) maker. Two factors

[14] See Appendix B, Q31 for detailed findings.

had changed that had profound effects on the 300mm transition schedule and neither was captured in the Roadmap process. The first was more technical: the slowing down – and eventual stopping – of chip size increases. Developers realized that the decreased reliability and other practical trade-offs that came with larger chip sizes led to severe scaling limitations so more emphasis was placed on "shrinking" device feature sizes to keep pace with Moore's Law. The second and more important factor was economic: an industry downturn that had started in 1996 had hit its trough in 1998, causing chip makers to scale back or entirely scrap plans for retooling or building new fabs. Many suppliers went ahead with development of 300mm tools (according to the Roadmap schedule), but chip makers instead "stretched" the use of existing tool sets vs. replacing these tools with new ones. The result was a significant production overcapacity by both device makers and suppliers, and increased tension between the two industries in search of an explanation. This problem was front-and-center when much of this research was conducted so this flavor (i.e., #2 weakness: participation by supplier community inadequate) is very evident. Since then the issue has been resolved and the Roadmap process is better for it.[15]

As stated in Chapter 3, Roadmap projections for 300mm wafer development produced a great deal of discussion between device makers and supplier communities. Some of these exchanges were heated, but the end result was a much closer working relationship between the two sectors along with a revision in the Roadmap process to better accommodate the needs of suppliers.

Summary and Conclusions

Linda Wilson is Managing Editor of the Roadmap and has overseen the last four editions of the Roadmap while contributing to the edition preceding these. While officially she has the role of Roadmap keeper or guardian, Wilson holds the unique position of Roadmap expert or *guru*. She has been involved in practically every decision, both big and small, involving the Roadmap contributing far more than her official title suggests. Her insight has proven invaluable to this research and appears more than formally acknowledged in the text of this and other chapters. Asked about her perspectives on the Roadmap, its evolution and its future, Wilson offered a thoughtful reply included below in Box 10-9. She cites some of the themes captured in the preceding paragraphs of this chapter, while others are addressed in succeeding chapters.

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[15] The consensus is that the Roadmap *per se* was not the "cause" of the 300mm early transition problem, but a contributing factor.

Specifically, the changing role of government and research into alternative approaches are discussed in Chapter 12: Implications for Industry Strategies and Public Policies.

Box 10-9. Linda Wilson's Perspectives on the Roadmap[16]

Particular fluxes in the Roadmap timing of minimum features are more driven as a response to reality rather than a pull of the industry by the ITRS predictions for leading edge manufacturers to hit market sooner, but the "who is driving whom?" argument (roadmap drives industry versus industry drives roadmap) definitely exists. However, the result of acceleration [rather than whether it is from the ITRS or by the industry] is a critical need to address the also accelerating technology limitations sooner as we continue to shrink features.

Hence the increase in acknowledging the various solutions that could eventually be commercialized as an ultimate reality of satisfying the technology requirements.

I see a move FROM including a government funding argument for further research TO a request to the semiconductor community to decide which areas of focus to address and then collectively seek solutions.

Behind the scenes meetings are now formatted to include meetings among several working groups—almost hybrid teams—for reaching solutions for best impact.

Also, this movement for globally leveraged research resources also encourages very early knowledge sharing of innovations and new concepts. While the statements regarding new technologies are full of caveats, such discussions placed in the 1999 and 2001 Roadmaps increase as the [government] funding discussions become increasingly quiet. I think this is to show that industry solutions are driven by the industry and will occur—maybe a subtle way of showing that we are reaching a critical point in our technology sets.

I believe that the focus for the semiconductor roadmap shows that current solutions and research activities for items already destined for commercialization are still primary and do not deviate from what the Roadmap has always been. Also, I think that it is a natural course for the process to continue to encourage activities and alternative approaches whose merits have not been proven as acknowledgment that many solutions exist and instead of focusing on those concepts, it is to support the theme of leveraged research and cooperation.

Wilson also raises additional topics of interest for future possible research. The last item, "the theme of leveraged research and cooperation," not only describes a core value of the Roadmap to date, but also serves as guidance for future Roadmaps that will incorporate yet more interests as technological challenges become more formidable. In sum, this chapter has attempted to demonstrate that throughout its evolution the Roadmap has adapted to the ever changing needs of those who use it. For it to continue to be of value it must continue this tradition.

[16] Linda Wilson, e-mail to the author, April 23, 2002.

CHAPTER 11: Summary Findings[1]

"[G]ood innovators are optimists, virtually by definition."

- Stephen Kline and Nathan Rosenberg[2]

"Every time we've done projections in the past, the future always looked red five years out."

- ITRS survey respondent, 1999

"These limits have a habit of receding as you get close to them."

- Gordon Moore[3]

"The value of the roadmap is in doing it, not just reading about it."

- Court Skinner[4]

Hypotheses versus Propositions as Research Statements/Questions

Research questions were initially formulated in this dissertation to guide the study (see Chapter 1). These questions were stated in the form of hypotheses to be tested through a qualitative research design. The process of data collection revealed much insight into each of the hypothesized statements, however it was not possible to definitively "prove" nor "disprove" any of them as would typically be the case in a quantitative study. Despite this shortcoming, the research statements do help organize the summary findings while enabling continuity in the

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[1] The bulk of the research for this chapter was completed by 2002 following publication of the 2001 ITRS. Since then the 2002 Update and 2003 ITRS have been published. While a few references may be made to these later versions much of the detailed analysis ends with the 2001 ITRS.
[2] Stephen J. Kline and Nathan Rosenberg, "An Overview of Innovation," in Ralph Landau and Nathan Rosenberg, eds., *The Positive Sum Strategy* (Washington, DC: National Academy Press, 1986, 297.
[3] Gordon Moore, Extreme Ultraviolet Lithography press conference call, September 11, 1997, http://www.intel.com/pressroom/archive/speeches/euv91197.htm
[4] Court Skinner, quoted in Ted Agres, "IC Density growth is key issue for industry," *Research & Development*, Vol. 38, No. 7, June 1996, 29.

research design. Most importantly, this approach structures the findings in a way that helps either support or refute hypotheses without declaring them as simply true or not.

Overall Hypothesis:

Technology Roadmaps and related roadmapping processes comprise a new and emerging field as has been discussed in this dissertation. The overarching research question is:

How have technology roadmaps affected innovation, strategy, and policy in the semiconductor industry?

This question was explored in detail through an examination of the technology roadmap "landscape" more generally and a comprehensive case study of the SIA Roadmap as the unit of analysis. Several hypotheses were formulated to help seek greater and deeper understanding of this new field. These hypotheses were considered starting points to guide the research.

Summary Finding:

The overall purpose of the Roadmap is to sustain—and even perpetuate—the semiconductor industry's historical productivity curve. This has traditionally been defined by Moore's Law, the exponential rate of technical progress that has characterized this industry since the 1960s. In so doing the Roadmap helps the global semiconductor community defy conventional S-shaped curve behavior in technological innovation. The Roadmap is thus a type of insurance or guarantee on the industrial future of semiconductor technology. The emergence of an industry roadmap reveals much about the pattern of technological innovation within the semiconductor community.

The evolution of *industry* roadmapping reveals that this process emerged from individual firms within the industry (influenced by the development and use of their own roadmaps), thus the resultant industry roadmap initially was the outcome of, or was affected by, the behavior of the industry. In fact, the Roadmap traces its origin to both industry strategy (i.e., SRC 10yr research goals, SIA technology committee and formation of technology strategy) and deliberate public

policy (i.e., Sematech, NACS, Micro Tech 2000). As the Roadmap gained support and credibility, it became a powerful coordinating vehicle that affected innovation, strategy, and policy in direct and indirect ways. A distinctive 'beat the roadmap' pattern ensued within the context of increased globalization and sustained technical progress and the on-going nature of the Roadmap is now a give-and-take process: it both affects and is affected by industrial innovation, strategy, and policy.

Hypothesis 1:

Roadmapping differs from other methods of technology planning and forecasting due in large part to its inherent practical nature. A roadmap is not a prediction of future breakthroughs in science or technology, but rather an articulation of requirements to support future technical needs. A roadmap assumes a given future and provides a framework toward realizing it.

Summary Finding:

A roadmap provides many advantages over other methods of technology planning: one being that is simple and straightforward—"no instructions needed" as one informant put it. Because the practice of roadmapping came from a more practical, problem-solving engineering community (vs. a more theoretical academic community), it has been more widely accepted and adopted. The Roadmap is expressly concerned with requirements, NOT solutions. This has been an area of misinterpretation of the Roadmap (i.e., mistaking it as a definitive plan containing "all the answers."). An informant underscores the advantages and potential disadvantages of engineers as authors of the Roadmap:

> "One of the benefits that the SIA Roadmap has over other industry roadmaps is that it's authored by engineers. It's authored by folks who are doing the work, as opposed to marketing types, or people that are apart from - even product planners or product managers who aren't part of - the technology. The down side to that or trade-off is that there's a tendency to want to get too detailed."

Other distinguishing factors include: 1) express domain of pre-competitive technologies, 2) breadth and structure of participation—broad forum includes universities, suppliers, as well as

device makers (no single agent dominates), 3) the collaborative and consensus process of identifying common needs (Roadmap is a consensus document), 4) voluntary (vs. internal company planning), 5) the process (i.e., people, consensus-building, etc.) driven by industry, not universities or government, thus more commitment level.

Hypothesis 2:

Technology roadmapping, as a practice, emerged from industry as a practical method of planning for new technology and product requirements. Therefore its adoption rate is much greater than its more academic cousins such as technological forecasting and technology foresight.

Summary Finding:

See Hypothesis 1 above regarding practicality and the role of the engineering community. In terms of wider adoption, the universality of the term *roadmap* as a metaphor for planning has been significant. Although the diffusion of roadmapping practices was not examined *per se*, practically every organization that the researcher investigated in the semiconductor community—whether private company, government lab or agency, research organization, or equipment and material supplier—had a roadmap.

In a recent assessment (de Laat and McKibbin, 2002) of 78 industry roadmaps (including the ITRS), the authors conclude that technology roadmapping (TRM) is exceptional in large part because it is *not* characteristic of an academic exercise, or at least one carried out by a small number of experts from a research team or central planning office. They emphasize the roadmapping's collective process involving all relevant stakeholders:

> TRM is not an intellectual "desk exercise," but is presented without exception as series of collective procedures and steps in which all relevant stakeholders should be involved. Whether it is performed on national, sector [industry] or company level, TRM involves by definition a huge amount of actors that are to deliver input to roadmaps during the process but also take benefit from it once it is finished. It is through and through a collective process… In sum, TRM would be characterised by the following features:

- It is a means of co-ordinating actors
- It starts from the hypothesis that the future can be constructed and is not simply 'happening'
- It gives great importance to the involvement of all relevant actors/stakeholders
- It gives great importance to iteration[5]

The historical review of roadmapping practices revealed the following findings. Although the exact origin—the "first roadmap" if you will—remains a mystery, there is evidence that the early identifiable sources of use were within the U.S. Government. This may be the case simply because there exists a better documentation trail, at least for defense-related programs that were public knowledge. Examining Motorola's roadmapping practices as a representative case study suggests that profit-seeking firms also realized the technical and economic benefits of this new technology planning technique. Informants from several other companies (e.g., IBM, TI, Intel, and Honeywell to name a few) had also indicated that roadmaps were used within their firms during this time, but these were rarely documented for public interest as they were used for competitive advantage. The growing concerns with international competitiveness and, to a lesser extent, national security provided the common ground for roadmaps to be shared. The VHSIC program is one example of a very possible connection where government and industry were mutually interested in roadmapping within the defense semiconductor community. Government/ Industry cooperation is also evident in energy and automobile sectors, and later in the commercial semiconductor sector. This is consistent with earlier findings that crisis serves as a catalyst to roadmapping.

Another related observation is that the practice started in the domain of research & development. This is evident in the Motorola case and especially in the SRC and Sematech consortia early planning activities and later in Micro Tech 2000. It is also an area where non-competitive—later called *pre-competitive*—activities could be conducted. Relaxed anti-trust rules

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[5] Bastian de Laat and Shonie McKibbin (Technopolis), "The Effectiveness of Technology Road Mapping: Building a strategic vision," a study for the Dutch Ministry of Economic Affairs, est. 2002, 4-5, emphasis in original.

would eventually allow roadmaps to be used in operational areas, but initially they seemed to emerge from research.

Although research-driven, the historical literature suggests and informants emphasize that roadmaps were adopted by industry because they proved to be a simple yet useful tool. Other than gathering the necessary participants, they were not difficult to do. Creating a roadmap was almost intuitive as seen in the SRC 10yr goal exercise or the Sematech workshops. This "no instructions needed" approach suggests the increasing acceptance over this period. Of course the process would become more formal with time, but the initial roadmaps just "seemed to happen."[6]

Hypothesis 3:

Existence of a consensus paradigm increases the success rate of S&T roadmaps. Thus, the unique pattern of technological change in semiconductors following "Moore's Law" is a key factor in the success of the SIA Roadmap.

Summary Finding:

This assertion was put forth by a variety of informants both within and outside of the semiconductor industry. Those within the industry especially express that having a future vision is very important, and that Moore's Law provides the necessary faith of vision. Some even refer to Moore's Law as myth or culture; that its real power isn't in the reduction to a simple description of density doubling every so often, but its symbolic, even religious value. Informants remind us that institutions like Sematech and the Roadmap were advocated by industry leaders such Noyce, Moore, Galvin, Sporck, and others who held and preached this vision, which engineers need for guidance. As one respondent stated, "We engineers can't innovate in a box." Furthermore, this high level vision is fulfilled by the semiconductor engineering community's acceptance and

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[6] Gordon Moore, telephone interview, February 11, 2002.

translation of Moore's Law into practice where the nature is order and problem solving. Envisioning and doing are thus connected through a consensus paradigm.

Similarly, one dissertation committee member noted the difficulty in reaching agreement on research goals. Roadmaps, on the other hand, are a form of goal-oriented research planning. Having an agreed-upon goal like advancing Moore's Law or its corollary, reduced device minimum feature size, helps ensure success. He drew the parallel with NASA's widely-shared Apollo goal of the 1960s.[7]

The strong engineering element in the Roadmap that operates within this conceptual framework is viewed as a key success factor. It was pointed out and confirmed that roadmaps from other industries where the developers were mostly management or even marketing types were not as consistently successful as the ITRS. The combination of Moore's Law and an engineering community that helps realize it underpins the Roadmap process. The expectation is that engineers know where the technology is going to be; another informant said, "that's our job." An outsider may then say 'gosh, we are going to run out of lithography in two years!' In fact, that is what the Roadmap does in a very real sense: makes requirements explicit. The informant continues, "But say the word challenge to an engineer, how can you beat that, how do you get around that, how do you 'engineer' your way around that? And enough of that churning goes on that guess what, we just pushed this time frame out."

Finally, the question was asked of survey respondents: "Do you think that Moore's Law drives the Roadmap or is it the other way around?" The responses can be summarized simply as Moore's Law and the Roadmap are two sides of the same coin as the results fell almost evenly to both sides. This helps confirm the unmistakable interrelatedness of the two factors. What can be concluded is that the Roadmap would *not* be what it is without Moore's Law, however the reverse

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[7] Christopher T. Hill, Vice Provost for Research and Professor of Public Policy and Technology, George Mason University, April 15, 2004.

is probably also true. One respondent's reply is most telling: "It's [Moore's Law] the carrot before the horse, but the horse often wins."

Hypothesis 4:

Roadmapping works better for technologies experiencing incremental versus discontinuous or disruptive innovations. Thus, development of technology roadmaps is consistent with strategies for a normal innovation pattern (i.e., the coevolution of an established network and technology along an established trajectory).[8]

Summary Finding:

Although this question was not directly asked of survey respondents, indirect inquiries and other research supports this hypothesis. The Roadmap is a manifestation of the four decade-long incremental or normal innovation pattern of the semiconductor industry that began with the bulk planar IC. The alternative case of roadmapping disruptive innovations was not found during the study. In fact, the Roadmap Coordinating Group (RCG), the management committee that oversaw development of the early national technology roadmaps, deliberately limited the scope to a very narrow, silicon (Si)-based focus. Thus, alternative materials (like Gallium Arsenide: GaAs) were not considered in the Roadmap process. More recently, the industry, along with 25% government support, has instead chosen other methods to seek out radical innovations in materials and device structures though five Focus Research Centers associated with the SRC. It should be pointed out that this program was established as the result of the Roadmap's projection of a "Red Brick Wall" and the industry's realization that this was "end of" or "beyond" the Roadmap research. Thus the Roadmap was used to identify the need to develop novel technologies in much the same fashion as Constant's (1980, 1973) *presumptive anomaly* guided those who led the turbojet revolution. The difference of course is that the "red brick wall" is explicit to the global semiconductor community by way of the Roadmap, while the presumptive anomaly

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[8] Robert W. Rycroft and Don E. Kash, *The Complexity Challenge: Technological Innovation for the 21st Century*, London: Pinter, 1999.

(anticipated performance failure) of propeller-powered aircraft was only implicitly understood by a few people, unaware of each other.

The historical review of roadmapping practices revealed the following additional findings about an approach that is more strategic and systematic, typical characteristics associated with the normal innovation pattern. Roadmaps, coming mainly out of the research community, had a longer-term planning horizon than most were used to in the 1970s when the IC segment of the semiconductor industry was still in its formative stages, with little time or desire for long-term planning. Roadmap time horizons were typically 5 or 10yrs, or longer. Thus this was a strategic planning approach that stretched the sights of operational types. This "beyond the next generation" focus also helped garner higher levels of collaboration as common problems and needs became obvious to all. The evolution to enterprise-wide, then industry, and ultimately international scope for roadmapping is evidence of this tendency.

Finally, a most recent special issue of *Technological Forecasting & Social Change* (2004), entitled, "Roadmapping: from sustaining to disruptive technologies," addresses roadmapping and disruptive innovation. This compilation of articles begins to examine the role of roadmaps and roadmapping practices in this new arena.

Hypothesis 5:

The widespread presence of technology roadmaps at all levels within the semiconductor industry has contributed to a qualitatively different landscape for innovation, strategy, and policy in the (roadmap era) 1990s as compared with the (pre-roadmap era) 1980s.

Summary Finding:

This statement was modified after studying the history of roadmapping practices in semiconductors. Two distinct eras of technology roadmaps can be acknowledged: *1980s research roadmap era* vs. *1990s (and continuing) industry roadmap era*. Early U.S. industry-level exercises in strategic technology planning based on projected device scaling include DoD's Very

High Speed Integrated Circuit (VHSIC) Program, Semiconductor Research Corporation's (SRC's) development of 10yr goals, and Sematech's start-up strategic workshops are referred to here as roadmap exercises.[9] Micro Tech 2000, sponsored by the National Advisory Committee on Semiconductors (NACS), was the culmination of these events and bore the subtitle, "Semiconductor Technology Roadmaps." The nature of these activities (i.e., overall goals, type and number of participants, etc.) is primarily one of research, thus this period is referred to as the *research roadmap era*.

Figure 11-1 shows semiconductor device minimum feature size targets for thirteen Roadmap activities spanning a planning horizon of 25 years (i.e., 1986-2010). Figure 11-1 links common values together as they were planned during different Roadmap exercises, and also shows a horizontal line separating Micro Tech 2000 developed in 1991 and the first SIA Technology Roadmap developed in 1992. All Roadmap-related activities that occurred above the line are considered in the *research roadmap era*, while Roadmaps developed afterward are considered in the *industry roadmap era* (see diagram). Note the distinctive pattern in the shifting of technology targets during these two eras. The research era is characterized by a 'pushing-out' effect. That is, the initial targets proved too aggressive so they were delayed in subsequent Roadmap exercises. In contrast, technology targets stated in the SIA Roadmaps (industry roadmap era) have consistently portrayed a 'pulling-in' effect. In other words, initial targets proved too conservative and were accelerated in subsequent Roadmaps. Chapter 10 provides more explanation on the factors underpinning this effect.

Firm-level product-technology roadmaps were not directly studied but through the course of research it was discovered that they have become more widespread but continue as proprietary tools for competitive purposes. Qualitative differences between 1980s and 1990s (and continuing) eras are the 'pushing-out' vs. 'pulling-in' effect of technology nodes. This is due to many factors,

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[9] 1987/88 Sematech Strategic Technology Workshops used the term "Roadmap" extensively, while earlier SRC and VHSIC exercises did not.

but development by industry (and supplier) members vs. earlier research community members (including industry representatives but more so consortia and government agencies and labs) is a significant factor.

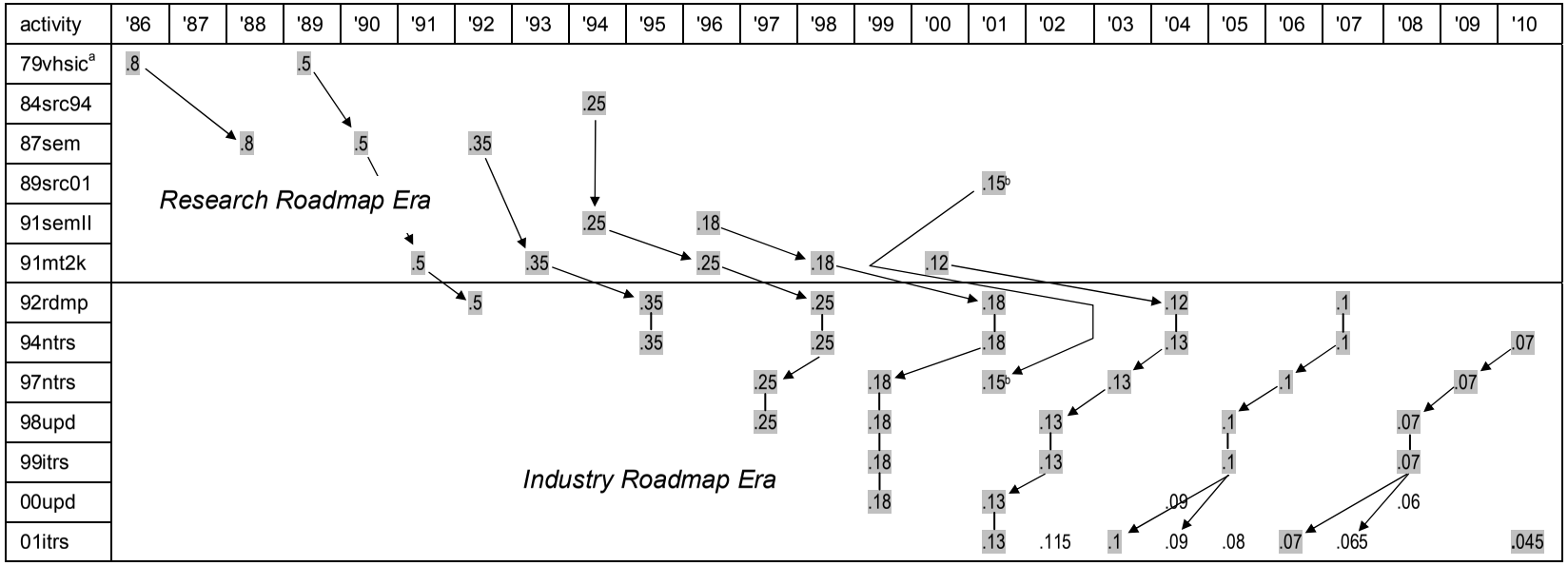


Figure 11-1. Linked Device Minimum Feature Size Targets by Roadmap Activity, 1979 VHSIC through 2001 ITRS

Notes:

a. VHSIC 1983 target of 1.25 (the real starting point) is not included here due to page space constraints. Likewise, technology nodes for 2011-2018 are also not included.

b. .15 was later dropped as a DRAM technology node.

c. See Figure 10-10 for other notes that also apply here.

Legend:

Activity	Description
79vhsic	U.S. DoD Very High Speed Integrated Circuit program
84src94	1984 SRC 10yr Goal Set
87sem	Sematech Black Book (initial strategic goals)
89src01	SRC 2001 Goal Set
91semII	Sematech II Strategic Plan
91mt2k	Micro Tech 2000 Technology Workshop
92rdmp	SIA Technology Workshop
94ntrs	1994 National Technology Roadmap for Semiconductors
97ntrs	1997 National Technology Roadmap for Semiconductors: Technology Needs
98upd	1998 ITRS Update (pilot of international participation)
99itrs	1999 International Technology Roadmap for Semiconductors
00upd	2000 ITRS Update
01itrs	2001 International Technology Roadmap for Semiconductors

Hypothesis 6:

The SIA Roadmap has contributed to a more regular, more predictable, ***and even accelerated*** *pace of innovation through deliberate coordination of pre-competitive R&D and related industry resources.*[1]

Summary Finding:

Yes, in fact a major finding is that the Roadmap has *accelerated* the pace of innovation through collective "beat the roadmap" behavior. More than any other finding this was emphasized by survey respondents and corroborated with empirical data shown in Figures 10-10 and 11-1.

The unique nature of the semiconductor industry has created a need for the Roadmap. The disintegration of vertically-integrated firms into a fragmented structure of multiple firms comprising the semiconductor materials and equipment industry requires much coordination. The rapid pace

[1] This statement was modified during the survey instrument iteration process with Sematech. A few words were removed, but most importantly the phrase, "and even accelerated" (emphasis added) was inserted to specifically test this premise.

of change accentuates the need for a coordinating mechanism. Thus, the semiconductor industry can't make any changes without integration of disparate companies. For example, i-line 248nm to 193nm photolithography technology required an exposure tool (6 companies), resist technology (3 companies), mask technologies (2-3 firms) and other industries to fully implement.

This hypothesis poses several additional questions:

1. *Why has the semiconductor industry in particular embraced roadmapping so enthusiastically?*

   Summary Finding: Economic risks are great. Required investments in research and manufacturing are considerable (i.e., currently $2-3 billion for new fabs) and materials approaching ultra purity levels, the Roadmap helps bring about a degree of standardization with materials and processes. Further, the lead time between research and manufacturable product presents additional risk. Thus it is in the industry's best interest to select a “winning” solution that further foster standardization. Industry roadmaps have evolved to help continue coordination between device maker and supplier industries as the two industries, once vertically integrated, have grown farther apart; now SM&E is a strong industry in itself, but still highly fragmented. The Roadmap helps coordinate and communicate across dispersed players. Finally, rapid pace of change necessitates coordination of tool development.

2. *What benefits does technology roadmapping offer semiconductor firms (and industry) that other methods of technology / product planning do not?*

   Summary Finding: See answer to hypothesis 1 regarding collaborative, consensus driven process. As previously mentioned, the "no instructions needed" simplicity of the roadmapping process is of great benefit. In the historical Motorola case in particular, upper management's influence resulted in a process that permeated the company to the point that it eventually became part of its culture. A related aspect of this that departed from traditional technology planning efforts was the thorough and systematic approach taken to planning. In the Motorola case a more formalized review process was needed and one that was reviewed

systematically (e.g., the RMTR). This was a much more complete approach, involving supporting technologies and other factors critical to the success of the technology in question. Indeed, the roadmap process is a much more holistic planning approach as the "whole process" is examined to a degree of granularity that is unprecedented. The comprehensiveness of the thirty or so Sematech workshops that followed the Monterey workshop is further evidence of this point. Finally, developers and users of roadmaps realized that a roadmap was much more than a date-stamped chart that was prepared and periodically looked at but not revised. As the SRC TAB learned only a few years into their summer studies planning exercises, the 10yr goals and their roadmaps were not simply one-time extrapolations, but living instruments needing on-going examination and revision. Motorola's RMTRs and later the Roadmap renewal process essentially meant that roadmapping, if done well, is an on-going process.

3. *To what extent do organizations such as organizational networks or technological communities (e.g., SIA) affect the process?*

Summary Finding: In the spirit of Tocqueville's earlier comments, when one properly examines the Roadmap, there is far more than meets the eye. The Roadmap is *one* outcome of a sociological process that by definition involves people: Roadmap members or participants. This represents a network of technical experts (i.e., TWGs or technology working groups) drawn from broader technological communities in industry, universities, research consortia, and government. This network is now truly global and numbering close to one thousand members. Hence, a deeper interpretation of the Roadmap is that it is a network. Beyond the ITRS development network, the Roadmap affects and is affected by a much bigger semiconductor community. This is illustrated in the following paragraph describing roadmaps and roadmapping practices in general.

One of the byproducts that upper management and roadmap participants alike repeatedly refer to is the great benefit of roadmaps as a communication tool. First, the process affords

an opportunity for many different players, especially the "rank-and-file," to work together, share knowledge, and contribute to the roadmapping effort. Motorola's RMTRs and the Sematech workshops illustrate this. This can also have motivational benefits that an otherwise top-down form of technology planning may not offer. In addition to the sociology of the process, a technology roadmap makes public the important tacit knowledge of the technologists involved in the process that otherwise wouldn't be explicated. A published roadmap becomes an inter-organizational almanac or record enabling all readers to commonly understand its direction and how each might fit into the bigger picture. And as Turner Hasty points out, a roadmap can also give an organization an important "voice" to the public at large.[2] As just one example of this, communication (or sharing) of roadmaps externally to suppliers, customers, or other semiconductor community members has become an integral part of strategic and tactical planning within this industry. Finally, if there were one word that summarized the overall usage, benefit, or purpose of roadmapping, it would be that the roadmap process provides a *dialogue* or *discussion* of key technology challenges that will be faced "down the road."

4. *Does the SIA roadmap foster roadmapping activities in firms, or vice versa?*

Summary Finding: Yes, also see the next question as it is interrelated. Suppliers' technology roadmaps in particular are designed to anticipate future needs by targeting specific solutions to the yellow and red zones. Many equipment supplier roadmaps are directly linked to the ITRS. It is used to signal how and when to enter new market segments. For example, the "red brick wall" will be a time of opportunity for new venture or new market segments, thus the Roadmap helps level the playing field.

At the research consortia level, both Sematech and the SRC have developed strategic plans based on the Roadmap. The SRC undertook a major reorganization following the publication of the 1994 NTRS in order to align its research programs (and roadmaps) more

[2] Turner Hasty, telephone interview, May 10, 2000

closely with the needs stated in the Roadmap. Following the 1999 ITRS, Sematech undertook a strategic directive to "Realize the Roadmap." Although Sematech had used the Roadmap as a key element in its strategic plan for many years, "Realize the Roadmap" provided a common theme and rallying point for the organization's plans and roadmaps.

At an even broader level, the success of earlier SIA *national* industry roadmaps, particularly the 1997 NTRS, allegedly influenced the Japanese semiconductor industry to develop a 'competing' national roadmap. To prevent the possibility of alternative technology needs and targets that might confuse the global supplier industry in particular, the SIA proposed a single, *International* Roadmap at the World Semiconductor Council in April 1998. The proposal was accepted on a trial review basis for the 1998 ITRS Update and fully adopted with the 1999 ITRS.

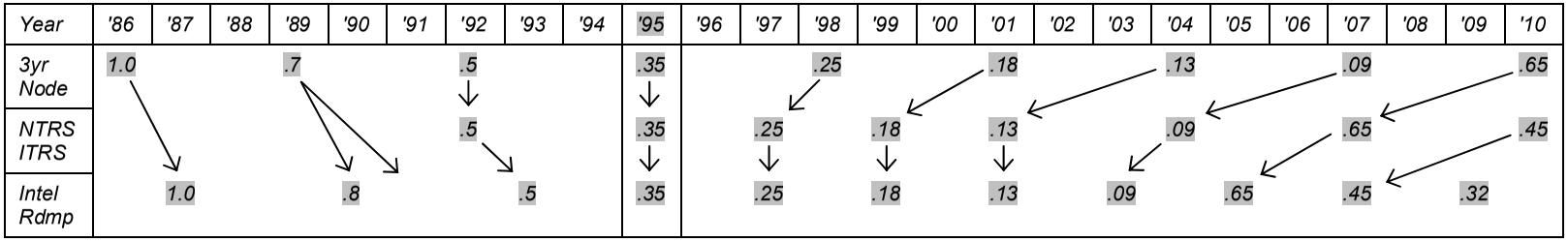
5. *To what extent do industry and firm roadmaps line up? Is there an underlying structural hierarchy among various roadmaps? If so, is it intentional?*

Summary Finding: There is strong evidence that individual firms' and industry roadmaps do line up and limited evidence that there is an underlying hierarchy within the semiconductor industry. In terms of the downstream electronics industry the situation is apparently different.

The ITRS is a high-level starting point, not end point. The Overall Roadmap Technology Characteristics (ORTC) have, from the start, provided top-down guidance to individual TWGs in the development of their roadmap sections. In terms of connections to other roadmaps, some indicate that company roadmaps contribute to the ITRS (bottom-up) in a real-time, interactive process. Many say that companies generally try to set their roadmaps at least as aggressive as the ITRS in their targeted areas of competence. The "beat the roadmap" behavior starts here. Also, the more recent editions of the Roadmap (beginning in 1997) reflect the timing assumptions of leading-edge companies' roadmaps. The very leading edge companies fully intend to stay ahead of the Roadmap, and there are more conservative companies who will minimize risk and R&D expense by intentionally staying one half or even

a full technology node behind the Roadmap. In sum, understanding and reacting to Roadmap node timing is an essential action practiced by individual industry members. Figure 11-2 compares the Roadmap with one particular firm roadmap (Intel Lithography Roadmap) and suggests a relationship between the two (see also Box 10-3). More research is needed, but the evidence so far seems to support the idea of some degree of integration among roadmaps within the semiconductor industry.

Figure 11-2. Node Scaling Comparisons (in microns): CMOS Traditional 3yrs vs. NTRS/ITRS vs. Intel Lithography Roadmap



3yr Node Source: 2001 ITRS, p33, Figure 5 MOS Transistor Scaling (1974 to present): S=0.7 each node [0.5x per 2 nodes].

Intel Roadmap Source: Peter J. Silverman, "The Intel Lithography Roadmap," *Intel Technology Journal*, Volume 6, Issue 2, May 16, 2002, pp56-7 (Figure 1, Table 2).

Notes:

- Before 1995: Intel Roadmap at 3yr scaling but actually behind historical 3yr CMOS scaling trend.
- 1995: Intel Roadmap accelerated node scaling to 2yrs, pulling in NTRS and ITRS through 2001 (reflecting actual performance). Compromise is ITRS out-year nodes still at 3yr scaling vs. Intel 2yr scaling.
- 2003 ITRS: Most likely pull-in .09 node to reflect Intel's and other leading-edge device makers' capabilities.[1]

[1] See for example Jack Robertson, "Samsung taking hefty gamble on NAND chips," *EBN Online*, September 20, 2002, where Samsung announced they will begin mass producing a 2Gbit NAND chip built on a 90nm process at a 300mm-wafer fab in the third quarter of 2003. NAND technology is a flash memory chip used in non-PC applications.

Another area that could be considered horizontal alignment with the Roadmap is the fast-growing chip foundry industry. Large foundries such as Taiwan's TSMC and UMC increasingly expand their global market shares producing a wide range of products for design-only or "fabless" companies. A decade ago, the emerging foundry industry typically lagged the integrated device maker (IDM) industry (e.g., Intel) by at least one process generation. However, this technology gap has narrowed considerably with experience so that foundries now equal (if not lead in some product sectors) the IDMs as shown in Figure 11-3. The increasing role of foundries, along with their ability to close the technology gap, has further contributed to the technology acceleration trend.

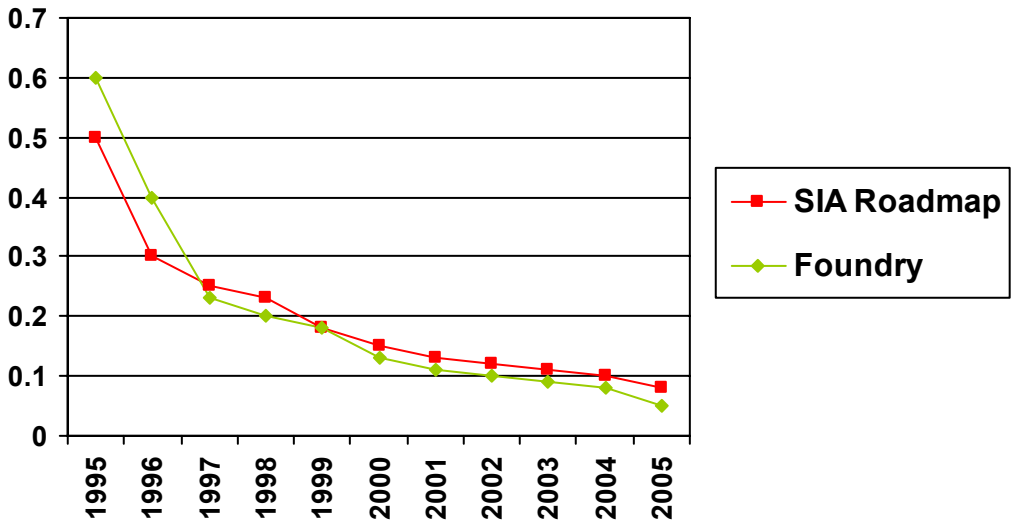


Figure 11-3. Relationship between SIA and Foundry Roadmaps (um)
Source: Fabless Semiconductor Association (FSA) http://www.fsa.org

In the broader landscape of industry roadmaps, integration in the U.S. electronics industry, represented by the National Electronics Manufacturing Initiative (NEMI) Technology Roadmaps, is very evident. The NEMI Roadmaps are prepared every two years by over 400

engineers/scientists from over 190 different organizations.[1] The SIA is a key contributor with responsibility for the Digital Silicon Technology Chapter. This is done through members of the ITRS U.S. Roadmap TWGs. The NEMI Roadmap also started a collaboration between NEMI and the other major roadmapping bodies in North America, to reduce effort and overlap in the various roadmaps. The National Electronics Roadmap Coordinating Committee was formed to minimize overlap and synchronize publication schedules, years of coverage and, where possible, common product emulators. As a result, the 2000 roadmap continues strong linkages between all major national Roadmaps: SIA, IPC, IMAPS, USDC, NSIC, OIDA:

> The NEMI roadmaps are designed to identify gaps in industry/government-sponsored research and infrastructure efforts. These system-driven roadmaps connect, as appropriate, to existing roadmaps, such as those from the Semiconductor Industry Association (SIA), Optoelectronics Industry Development Association (OIDA), the Institute for Interconnecting and Packaging Electronic Circuits (IPC), United States Display Consortia (USDC), and the National Storage Industry Consortia (NSIC). There is no intent to duplicate efforts already underway... As a result, the NEMI roadmaps span the entire electronics industry [and] emphasize the integration of the entire electronics manufacturing enterprise.[2]

As just one example of this coordination between industry roadmaps, NEMI publishes every two years on even years (i.e., the present 2002 Roadmap is in process), while ITRS editions are prepared on odd years (e.g., 2001 ITRS).

Finally, at the international level there is coordination. For example, in Japan the Semiconductor Technology Roadmap Japan (STRJ) and the *Jisso* Technology Roadmap for packaging technologies both closely coordinate activities and share data with the ITRS.[3]

6. *How does the industry know if technology roadmaps work and how is success measured?*

Summary Finding: Respondents offered a variety of answers to this question. Probably the simplest answer is that the Roadmap has been achieved, and in the process has earned

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[1] In fact, the NEMI Roadmaps in their present form adopted the general format and roadmapping process from the 1994 NTRS SIA Roadmap process.
[2] NEMI Roadmap, 1998.
[3] Yoshiko Hara, "Japan develops packaging technology road map," *EE Times*, March 29, 2001. Selection of the Japanese term *jisso*, for which there is no English equivalent, is intended to convey the concept of total solutions, encompassing interconnect, mounting, assembly, packaging, and system design integration.

industry-wide acceptance through repeated validation. The ITRS is widely considered a credible resource. Outside the industry it is deemed by many as a "model" (see previous discussion on adoption for NEMI Roadmap process). One way to measure success is to look at progress against key technology challenges identified in the Roadmap, and the extent to which collaborative research and development has been spurred by the roadmap document. If projects are started to address the “red” areas or effort is increased on these, this is a good indicator. If tools and process/device solutions are delivered when needed, this is another good measure. Some assert that maintaining the technology pace without stumbling is a measure of success. To others there is no simple numerical measure of success. Rather, the Roadmap gathers people together to understand different area of technology, breaking down silos and fostering collaboration and consensus.

One vivid example of success is the continued extension of optical lithography reflected in the Roadmap over time. Lithography has traditionally been the key technology driver for the semiconductor industry, thus it has commanded particular attention. Table 11-1 compares expected use and extension limits stated in the Lithography section from each Roadmap edition. Note the distinct pattern of stretching the capability to smaller geometries over longer timeframes. The means to achieving this is through continuous improvements in mask making and related technologies. The Roadmap has brought industry-wide visibility to the difficult challenges of optical lithography technologies and helped leverage research efforts toward needed solutions.

Table 11-1. Roadmap Optical Lithography Extension Limits

Roadmap	Expected Use	Year	Extension limit	Year
1992/4 NTRS	0.25 micron	1998	0.18 micron	2001
1997 NTRS	180 nanometers	1999	130 nm	2003
1999 ITRS	130 nm	2002	100 nm	2005
2001 ITRS	90 nm	2004	65 nm	2007

Sources: SIA Roadmap Editions, 1992 (Working Group Reports), 45; 1994, 81; 1997, 83; 1999, 143; 2001, 241, 245.

7. *Is there a relationship between product / technology or industry life cycles and technology roadmap success?*

Summary Finding: This question was not asked of Roadmap participants, but the topic did come up in several exploratory interviews and discussions. Several informants were familiar with—and some had even participated in—other industry roadmaps (e.g., NEMI, IPC, OIDA). They naturally compared these with the SIA Roadmap. Pertaining to this question, flat panel display technology in the Optoelectronics Industry Development Association (OIDA) Roadmap was singled out as a case that was not yet successful in part because of the early stage of the technology's life cycle. According to informants the U.S. flat panel display community was attempting to get back into general display business, thus the need for an industry roadmap. Using a Japanese roadmap as a baseline, the U.S. OIDA Roadmap was intended to match and ultimately surpass them. However, there were alternative display technologies in which DARPA had been investing, hence there was no single base technology from which to project. In other words, they were creating an inflection point in the display market. One informant remarked that roadmaps "work pretty well as long as you are not dealing with inflection points." Another was more poignant regarding the OIDA effort:

> "One of the problems with the OIDA Roadmap was that there were two many different technologies that were involved and they hadn't reached a dominant design phase yet so they didn't know what their next step would be."

The co-evolution of industrial development and roadmapping practices is evident in the Roadmap's broadened scope and increased process commonality. The early history of roadmapping at Motorola suggests an evolutionary nature to roadmaps and roadmapping practices. One can almost imagine the first Motorola roadmaps as not much more than a simple one-page chart of a particular technology's capability plotted over time (similar to the first SRC 10yr goal set). A decade later roadmapping had become a company-wide process at Motorola with significantly more sophistication, detail, and support resources. The scope had broadened, thus the roadmapping process had to become more standardized to be of

corporate value. As roadmapping evolved from company to industry levels in particular, there is little doubt that sharing of company roadmapping practices brought even more standardization or commonality in processes and methods. It is quite possible that a hierarchical design emerged, even unintentionally. Member companies supporting the SRC or Sematech would naturally want to coordinate their technology plans (roadmaps) with whatever industry roadmaps were under development at the time. There is some anecdotal evidence from informants that roadmaps became more common over time, but this is an area that deserves further research. This, however, is consistent with the suggestion that roadmapping was a logical step as the industry matured. It also appears that the semiconductor industry is the first major industry sector to employ an *industry* roadmap.

8. *What relationships exist between technology roadmaps and innovation, strategy, and policy?*

   Summary Finding: This question was further divided into two separate questions in the survey; one dealing with technological innovation, and the other addressing corporate strategies and public policies. Regarding innovation, two major themes emerge. The first is that the Roadmap has helped accelerate or "pull in" the technology in time compared with Moore's Law scaling: specifically a 2yr cycle vs. historical 3yrs. This is a common theme raised throughout the interviews and verified in Figures 10-10 and 11-1. Many relate this to continued improvements in industrial productivity. The second theme is basically the rationale behind the accelerated pace; namely the Roadmap focuses collective attention on technology needs, thus it has enabled investments and R&D to be earmarked more cost-effectively while stopping or mitigating work on not-needed technologies. It has also enabled new equipment to be available when needed while pointing out the timing of the exhaustion of a particular approach. One respondent simply said it has lead to more “rifle shot” rather than “shotgun” planning activities for R&D. This would also apply to the supplier community. Some others said the ITRS has helped provide tools, students, and new knowledge which have been

critical to the continued evolution of the industry. Despite these benefits, there are concerns that the Roadmap has stifled innovation by being too prescriptive and path dependent.

Regarding corporate strategies, there is general agreement that corporate strategies are affected positively as the Roadmap not only clarifies but helps prioritize future technological needs for the industry. However, some respondents point out that the Roadmap mistakenly drove 300mm equipment R&D too early. Regardless, the Roadmap influenced corporate strategies in a more coordinated and focused manner.

When asked about public policies, though, it is unclear to most respondents what effect the Roadmap has had—at least recently—on public policies. By examining public policy effects more closely through other sources such as background interviews and archival records, there seems to have been three phases of public policy over the Roadmap era of the last decade. The first phase was an explicit role of the U.S. federal government as *advocate*, or even *sponsor*. Public policy (NACS) brought forward the Roadmap with the development of Micro Tech 2000 in 1991. The first SIA Roadmap (1992) was the industry's implementation assessment of Micro Tech 2000. One of the express purposes of the 1992 and 1994 Roadmaps was to provide the government a single voice of industry needs for R&D funding. For example, the metrology program at NIST was established as a result of the 1994 NTRS.

In the second phase (1994-97, and especially reflected in the 1997 NTRS) the government could be described as *indifferent participant* as the government deliberately distanced itself from industry support. Three factors were at play. First, the U.S. industry had recovered from the international competitive crisis of the late 1980s and had regained its global leadership position. For this reason and the fact that international membership was being sought, Sematech requested elimination of government funding. The second reason has to do with political change. At about the same time as the Sematech request, the leadership changes resulting from the 1994 Congressional elections produced a political climate that was far less sympathetic to industry support. The new Republican leadership

labeled activities similar to Sematech as "corporate welfare" and called for major reform. Thirdly, the perceived 'success' of the Roadmap implied that industry had a plan and did not need any help since all related knowledge of S&T was 'in the Roadmap'.

The third phase (1997-2002 and continuing) has seen the Government become a more active but in a more targeted way. For example, the Government provides 25% support of MARCO Focus Center Program, which stemmed directly from the Roadmap as the official "beyond the Roadmap" research initiative. In this capacity the Government could be called a *partner*.

Implications for industry strategies and public policies are discussed in Chapter 12 in more detail.

Hypothesis 7:

The SIA Roadmapping process involves a broad organizational network. Thus, collaboration in the roadmapping process is not new. Yet the structure and methods employed (e.g., pre-competitive basis, broad participant network, process—not product—emphasis) are clearly unique.

Summary Finding:

The SIA Roadmap was the first industry roadmap (1992), and later the ITRS was the first international roadmap (1999). In this respect the process is totally unique. The most often cited reason for its uniqueness is a high degree of consortia involvement. Many acknowledge the role of SRC and Sematech research consortia in particular, however this has now extended to include other regional consortia such as IMEC, Selete, and ERSO. One respondent noted the trend in the last decade toward the consortium, cooperative, and other forms of collaborative processes as "a unique sociological design. It's helped make this creativity public in a sense." The Sematech culture of consensus in particular is cited as a contributing factor especially since most TWGs were initially co-chaired by someone from Sematech. Further, the Roadmap process has brought

a long-term focus: before the Roadmap, U.S. manufacturers would look typically ahead only a few years, but there was little interest in "down the road" planning.

Also, an increasing number of manufacturing processes are considered pre-competitive. While it is very true that proprietary information is closely held by participants, the proportion of total knowledge that is considered pre-competitive has grown over time, thus successive Roadmaps have become more complete (i.e., increased specificity and granularity of technology requirements). This is the result of two factors. The first is that the semiconductor community has become much more comfortable sharing common knowledge. This process began in earnest with the creation of research consortia, especially with Sematech, and continues today as the limits of technological progress fast approach. The second reason is related and accentuates this effect. As the Roadmap has become more widely accepted and used, participation has broadened significantly. The 2001 ITRS is the product of 839 participants located around the globe. Considering that participants in the Micro Tech 2000 Workshop from a decade earlier involved roughly 10% of this number, and those were mostly from the research community, the innovation enterprise has greatly expanded. The result is that pre-competitive Roadmap knowledge is now a greater share of a growing pool of technological knowledge. This is one key reason that the Roadmap has attained a considerable level of legitimacy within the global semiconductor community. Again, a driving force here is the collective attempt to mitigate R&D risk by focusing on shared solution sets such as shared equipment or shared ESH technologies.

Hypothesis 8:

The key driver for the SIA Roadmap has evolved from a competitively defensive, national industry strategy to a more universal and global strategy to stay on the industry's productivity curve as defined by Moore's Law.

Summary Finding:

The answer to this question was most evident to participants familiar with the historical background of the Roadmap, many of whom had participated in early pre-Roadmap exercises. Catch-up or "leap-frog" had been the traditional purpose of roadmap activities starting with Japan's VLSI Program of the late 1970s. While there is not consensus, many informants acknowledge the VLSI program as the *first* industry roadmap exercise.[4] The purpose of the U.S. DoD's VHSIC Program of the 1980s was to regain technological parity with commercial industry. A by-product was a hope to positively influence the U.S. semiconductor industrial sector and thus, international competitiveness. The formation of the SRC in 1982 and specifically the development of the SRC 10yr goals in 1984 were express attempts to strategize what it would take to catch up with projected Japanese technological advances. In 1987 following more than a year of U.S. industry "soul searching," Sematech was formed in a 50/50 arrangement between the industry and U.S. Government expressly to regain global leadership in semiconductors. The ensuing strategic workshops to formulate a technology strategy for the new organization were technology roadmaps in form and name. In 1988 Congressional legislation established the National Advisory Committee on Semiconductors (NACS) to "devise and promulgate a national semiconductor strategy." The capstone of this committee's effort was the Micro Tech 2000 Workshop and Report (subtitled "Semiconductor Technology Roadmaps") in 1991. Micro Tech 2000 was "an effort to address the technological competitiveness of the U.S. semiconductor industry" and was a bold attempt to lay out a plan (roadmap) to skip a technology generation by the year 2000. With the expiration of NACS, the SIA formed a Technology Committee and accepted follow-on responsibility for Micro Tech 2000.

The charter of the 1992 SIA Roadmap included: "to ensure that the U.S.-based semiconductor industry would have the necessary basic technology and technological options for

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[4] The author attempted to include the VLSI Program in Figure 1 but was unable to gather line width data. Projected DRAM chip density targets were collected, which helped support the argument by some that this was an industry roadmap exercise, if not by name.

success in the competitive world market." *National* appeared in the title of the subsequent 1994 SIA Roadmap: "The National Technology Roadmap for Semiconductors" (NTRS). By late 1994, U.S. industry had convincingly regained global leadership in market share, thus one of the major themes of the 1994 NTRS was that it was "designed to build a culture of 'urgency without crisis'." Reference to international competitiveness appears in the 1997 NTRS, but is no longer a major theme. Instead, the 1997 NTRS is subtitled "Technology Needs," and an impending technological barrier is featured as a major theme:

> "[I]t now appears that the industry is rapidly approaching a formidable "100 nm barrier,"[5] consisting of an unprecedented number of distinct technical challenges which threaten continuation of its historical success formula. Hopefully, this Roadmap can be used as a focal point for reaching agreement on what needs to be addressed and as a guide to marshall [*sic*] adequate resources required to support the research and development needed to overcome this "barrier.""[6]

Two pressing issues surfaced in 1998 that needed to be addressed by the Roadmap. The first was IBM's unexpected announcement of copper as a conducting material. This had been projected in the 1997 NTRS but not until the next technology node in 1999 at the earliest. Copper's beneficial characteristics over aluminum influenced the Roadmap projections so much that revision could not wait for the next edition in two years. Hence, the first Roadmap *update* was planned for 1998. At the same time international competitiveness would return as a major Roadmap concern, but this time the tables were turned. It was reported that Japan was developing a competing industry roadmap (see Hypothesis 6.4. findings). Following an appeal to the World Semiconductor Council, the Roadmap update would be called the *International* Technology Roadmap for Semiconductors (ITRS) 1998 Update and include membership from Japan, Taiwan, Korea, and Europe regions on a trial review basis. If this pilot was successful (as it turned out to be), the 1999 ITRS would be the first official International Roadmap as each member region would contribute equally to the process. The migration from NTRS to ITRS demonstrates the global commonality of purpose. Mark Melliar-Smith (1998), then Sematech

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[5] The 100nm node was later corrected to 90nm in the 2001 ITRS.
[6] SIA, *1997 NTRS*, ix.

CEO, reflects this sentiment: "For the next 10 years, there's a different crisis. It's no longer 'beat Japan,' but to stay on the productivity curve."

The 1999 ITRS editions further emphasized technology requirements and challenges within an international context, and began to discuss "off the Roadmap" requirements. The 2001 ITRS used the phrase "Red Brick Wall" and explicitly acknowledges the need for "novel devices" in the approaching "non-CMOS" era:

> It is recognized that research and development on emerging non-CMOS devices is proceeding rapidly toward the end of the Roadmap. Owing to the difficulty of successfully scaling conventional bulk planar CMOS technology to meet to meet the increased performance, density, and reduced power dissipation required for future technology generations, such novel devices will likely be needed eventually. Implementation of non-CMOS device structures and architectures, including interconnect and memory, will drive major changes in process, materials, physics, and design. The emerging non-CMOS devices may coexist with conventional-CMOS integration.[7]

Indeed, a new section appears in the 2001 ITRS that addresses "Emerging Research Devices." Recognizing the potential end of conventional-CMOS scaling within the planning window of this Roadmap, the purpose of this section is to "cast a broad net" to stimulate invention and research leading to feasibility demonstration for one or more Roadmap-extending concepts. Novel device types such as quantum cellular automata, nanotube or molecular devices, and many others are featured as possible candidates to extend scaling capabilities and thus, sustain the industry's productivity curve.

Hypothesis 9:

The SIA Roadmap has qualitatively affected R&D expenditure patterns of the U.S. semiconductor industry in significant ways. The emphasis seems to be more on "D" than "R."

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[7] SIA, *2001 ITRS*, 14.

Summary Finding:

In the survey instrument the sentence, "In other words, the Roadmap has shortened the research agenda horizon." was added to the end of this statement for more clarity. The overall response was split about evenly with a slight edge given to *Disagree* (45%) versus *Agree* (41%). What is more revealing is the context of the comments. Those that agreed viewed the Roadmap's primary emphasis as on mainstream development, pointing out in particular that this was the case at Sematech where the Roadmap is the first-order guidance and influence is on suppliers.

Some saw the purpose of the Roadmap as having fundamentally changed from its original research focus to one that provides directives to suppliers in the interest of the semiconductor industry to maintain historical productivity. In a related manner, device makers currently use it as a benchmark to surpass or "beat the roadmap." Some mentioned the possible stifling effect in university research, asking "why work on something that says 'solutions available'?" A few respondents argued that the Roadmap creates path dependency citing the continued research emphasis in the bulk planar CMOS domain. However, a few argue the counterpoint: that the Roadmap focused industry research on CMOS that would not have occurred otherwise, thus it helped galvanize people to look at the industry's most important technical issues.

On the other hand, several disagreed with the statement for different reasons. The first is that the Roadmap clearly delineates future research challenges with red cells to the point that a "red brick wall" has emerged and requires fundamental solutions. Another points out that "there is very little 'R' in this industry anyway." More importantly, the precipitous decline in basic research over the past decade or so, especially with the dramatic reduction and in some cases outright elimination of industrial labs, coincides with the Roadmap era. Thus, as several respondents indicate, this cannot be attributed to the Roadmap *per se*. "Remember, we don’t have Bell Labs anymore, and IBM is not the altruistic think tank that it once was." states one respondent.

Several respondents who disagree cite the MARCO Focus Center Program as a principal example of the Roadmap's longer-term focus. Some see the Roadmap as having a very far out

horizon in an attempt to define research needs particularly in universities. Three highlight that misinterpretation of the Roadmap as a book of solutions still plagues the Roadmap developers. Finally, one respondent summarizes, "It has improved vision on BOTH. Yellow is 'D' and Red is 'R'."

However, demographics have changed in Roadmap membership from the *research era* (through Micro Tech 2000) including Government involvement to *industry era* (SIA Roadmaps, 1992-2003 and continuing), with particular emphasis on increasing supplier industry participation. Bob Burger, former Senior Scientist at the SRC and co-chair of the Micro Tech 2000 Workshop, expresses concern:

> There is a periodic tendency, derived from the technology roadmap exercise, to define the results expected from the research. Such efforts are misdirected because, if results are definable, then the effort is not research but development, and university efforts directed toward development are a poor use of the university capability.[8]

Finally, it should be noted that the Roadmap is primarily authored by the chip making industry who attempts to communicate requirements to two distinct audiences: near-term (suppliers with a 6yr horizon), and long-term (research with a 6 to 15 year horizon). As discussed in Chapter 10, the format for the ITRS table structure that portrays future projection timing was changed from a single table that projected six technology nodes into the future (each either 2 or 3 years apart) in the 1997 NTRS and preceding Roadmaps. For the 1999 ITRS, the technology requirements tables are divided into near-term and long-term years, with high granularity applied to the near-term metrics (annualized for 6yrs) versus the long term requirements shown at 3-year node intervals only (see Box 10-2). This makes very clear the focus of the two audiences.

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[8] Robert M. Burger, *Cooperative Research: The New Paradigm*, SRC manuscript, 2001, 137.

Other Key Findings

Accelerated Technology Nodes

One of the salient features of the Roadmap (and previous roadmap exercises) is the projected process technology targets—referred to as technology nodes—arrived at based on timing assumptions. Moore's Law (historically 2x density every 18 months) and close derivatives have demonstrated advances in technology node timing every three years. This is called device scaling and the industry has settled into a pattern of halving the minimum feature size or line width every two nodes. Note that whenever the feature size is halved, the circuit density increases by four-fold. Thus, density doubling as described by Moore's Law is realized every technology node. For example, the 1997 NTRS reflected 250 nm technology being introduced in volume production while the 1999 ITRS showed 180 nm and the 2001 ITRS 130 nm. Process technology was halved between 1997 and 2001. Likewise, 180 nm technology will be halved in the next node (i.e., 90 nm projected to occur in 2004 per 2001 ITRS). This scaling pattern has been a key planning assumption in the Roadmap formally since its inception, but in fact can be traced back to the first SRC 10year goal set in 1984. What is notable here is that scaling timing has been accelerated in the three Roadmaps (1997, 1999, and 2001) and intermediate *Updates* from the traditional 3yr cycle (nodes halving every six years) to a 2yr cycle (halving every four years). Table 11-2 compares the traditional 3yr scaling timing extrapolated backward to 1974 with the actual line widths achieved over the same time period. A line between 1989 and 1992 columns represents the start of the SIA Roadmap era.

Table 11-2. Previous Scaling Trends Extrapolated From 1974[9]

Year	*'74*	*'77*	*'80*	*'83*	*'86*	*'89*	*'92*	*'95*	*'96*	*'97*	*'98*	*'99*	*'00*	*'01*
3yr Scaling	*4.0*	*2.8*	*2.0*	*1.4*	*1.0*	*.7*	*.5*	*.35*			*.25*			*.18*
Actual Nodes[10]	*5.0-6.0*	*3.0-4.0*	*2.5-3.0*	*1.5-2.0*	*1.0-1.5*	*0.8-1.0*	*.5*	*.35*		*.25*		*.18*		*.13*

A couple of points are noteworthy in Table 11-2. First, node timing has accelerated beginning in 1997 and continuing through 2001, as noted in the 2001 ITRS and discussed in Chapter 10. The economic benefit to the industry has been significant according to analyst Dan Hutcheson:

> I figure that the ROI [return on investment] for the SIA Roadmap is an astounding 640% per year (yes, I double-checked it, there is NO decimal point there). The net gain per cycle has been $16B for the chip industry and $5B for the equipment industry, while the cost was under $50M. Here is how I came to these numbers: The logic starts with the fact that shortly after the Roadmap came into being, the time to execute a technology node was cut from three years to two. This cut is an equivalent net saving of one year's R&D per technology node. This is where the total gain of $21B comes from. Now for the cost: About 500 people participate in making of the roadmap each year. Take the time spent in meetings times a liberal pay and benefit schedule; then add travel expenses; multiply by 3 for the three year effort; and I come up with a number that is just under $50M. Then all you have to do is calculate the ROI. For shareholders this adds about 4% to net margins—or at a P/E ratio of 20; it has added $143B to the combined value of the chip and equipment industry's stock—not bad for three year's work of 500 some-odd part-timers.[11]

Technology (node cycle) acceleration and the underlying factors that contribute are discussed in more detail in Chapter 10.

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[9] 3yr scaling trend source: *2001 ITRS*, Figure 5, 33, MOS Transistor Scaling (1974 to present): S=0.7 each node [0.5x per 2 nodes].

[10] The sources of 1974-1989 actual line widths are William E. Steinmueller, *Microeconomics and Microelectronics: Economic Studies of Integrated Circuit Technology*, Ph.D. Dissertation, Stanford University, March 1987, p221, and Intel Microprocessor Quick Reference Guide http://www.intel.com/pressroom/kits/quickreffam.htm Line widths are stated as ranges to accommodate differences in historical archives. SIA Roadmaps (1992-2001) are the source of actual line widths starting in 1992.

[11] Excerpted from an e-mail dated February 15, 1999, subject "The Chip Insider: 990216" (Dan Hutcheson is CEO of VLSI Research Inc.). Note that this estimate does not include Sematech's recurring costs in dedicated staff, production and reproduction, and related Roadmap expenses.

Micro Tech 2000 goals achieved

Another historical achievement worth noting is that the original Micro Tech 2000 goals that basically established the baseline for the subsequent Roadmap era were attained. Recall from Chapters 9 and 10 the almost-unanimous rejection by industry of the Micro Tech 2000 targets as simply too aggressive for implementation at the time. In fact, the SIA was quick to publish its first Roadmap in late 1992, less than 18 months after Micro Tech 2000, reflecting future scaling targets relaxed to their normal 3yr cycle. This was industry's official reply to the research community; in essence saying "we can do it, but in this more reasonable timeframe." Table 11-3 compares the Micro Tech 2000 goals established in 1991 with conventional 3yr scaling reflected in the 2001 ITRS and actual line widths reflected in this and preceding SIA Roadmaps.

Table 11-3. Comparison of 2001 ITRS and 1991 Micro Tech 2000 Technology Nodes

Year	*'91*	*'92*	*'93*	*'94*	*'95*	*'96*	*'97*	*'98*	*'99*	*'00*	*'01*	*'02*	*'03*	*'04*
3yr Scaling (2001)		*.5*			*.35*			*.25*			*.18*			*.13*
Actual Nodes		*.5*			*.35*		*.25*		*.18*		*.13*			*.09*[+]
SRAM 3yr Scaling (1991)	*.5-.6*			*.35-.4*			*.25-.27*			*.18-.20*			*.10-.15*	
MicroTech 2000 Goals (1991)	*.5-.6*		*.35-.4*			*.25-.27*		*.18-.20*		*.10-.15*				

Remember that Micro Tech 2000 was a *research* roadmap and based its technology generation (now called *node*) projections on the availability of "engineering samples" or a "manufacturable semiconductor process," whereas the SIA *Industry* Roadmaps that followed projected technology nodes based on "year of introduction to volume manufacturing." Since the gap between demonstration and volume production has been 1-2 years historically, these scaling targets—done 10yrs apart—amazingly line up.

Allowing for a 1-2yr difference between demonstration and volume production, the out-year Micro Tech 2000 goals are compared with actual technology nodes and also line up as originally projected. Specifically, the Micro Tech 2000 target of .12 micron technology (actually .125 or .13 since rounded up vs. down) engineering samples by the year 2000 did come to pass, and in fact the accelerated timing called for was achieved as early as 1997. However, the methods used to accomplish this did not transpire as originally planned. As discussed in Chapter 9 the U.S. industry rejected the "multi-billion dollar initiative" that NACS had called for to achieve such aggressive goals. Recall that the strategy behind Micro Tech 2000 was for the U.S. industry to skip (leapfrog) one technology generation in order to catch up with and surpass the then-advanced Japanese industry. Planners believed that significant investment in process technologies such as advanced lithography would produce these results. For practical reasons this more radical approach was not followed. Instead, the U.S. and in fact the global industry applied the traditional incremental innovation strategy with the help of the SIA Roadmap process as a coordinating mechanism. The results were the same.

Fast, slower, faster again

Another observation from Table 11-3 is that actual node timing in the 1970s and into the 1980s was actually faster than the CMOS 30%/yr extrapolated trend. According to historical records, feature size scaling was even faster in the 1960s, falling ten-fold from 100 microns in 1959 to 10 microns by 1969. (Steinmueller, 1987; Noyce, 1977) This supports Moore's original plot (Moore, 1965) of 2x density increases annually or 4x every two years. Starting during the 1980s and continuing through the mid 1990s the slower but more regular 3yr scaling pattern was established showing decreases of 11%/yr (Meindl, 1987) or 30%/3yrs(2001 ITRS). But by the mid 1990s node timing began to accelerate again as reflected in the 1997 NTRS and continuing through the 2001 ITRS. Hence, the 2yr scaling pattern now in place reflects the original Moore's plot (at least through 2001). Appendix C provides more detail on changing scaling patterns.

To put this in a broader perspective, Figure 11-1 shows the projected semiconductor device minimum feature sizes (line widths) expressed in microns (micrometer or millionth of a meter) that distinguish each future generation or node of process technologies. For example, state-of-the-art fabrication processes in 2002 are using 0.13 micron (130 nanometers) technology while some leading-edge manufacturers have implemented 0.10 micron (100 nanometers) technology as indicated on the chart. The charts are populated with target dimensions included in various published technology roadmaps or roadmap-related exercises dating back to the VHSIC program in 1979. The projected timeframe for all these activities span ten to fifteen years. For analysis purposes the period 1986 to 2010 is included in Figure 11-1.

Research versus Industry Roadmaps

A distinctive pattern emerges in Figure 11-1. The projections from earlier exercises were consistently *extended* in time in subsequent exercises, while projections from later exercises were consistently *shortened* in time in subsequent exercises. A line was added to indicate the beginning of the SIA Roadmap process. This line clearly separates the two patterns which we will refer to as two different eras of roadmaps: research roadmaps and industry roadmaps.

The era of industry roadmaps is by definition the SIA Roadmap era that began in 1992. The previous section described the technology node acceleration that characterizes this era. This is made more evident in Figure 11-1 with all node projections revealed. The research roadmap era, on the other hand, is not as clearly defined. The pre-SIA Roadmap activities shown in Figure 11-1 combine data from four different organizations (i.e., VHSIC Program, SRC, Sematech, NACS) and on the surface grouping these together may seem a bit of a stretch.[12] However, informants who had participated in these activities underscored the similarities of these events. They further stated that in most cases many of the same organizations (including sometimes the same people)

[12] See especially Box 10-3.

were participants. In the tradition of Constant (1980, 1973) and Vincenti (1990, 1984) technological or practitioner communities were then well established.

Another characteristic of these early roadmaps was the small number of participants. The VHSIC program involved a handful of contractors while the SRC 10year goals were developed in a "summer study" of about twenty people. The composition was mostly researchers as SRC and later Sematech were both research consortia. This factor is strongly reflected in the participant list of the Micro Tech 2000 Workshop. The result was aggressive and seemingly impractical technology targets based on what was possible, but not necessarily deemed feasible by industry. Steve Kline from Stanford reminds us that science (research) and technology really ask two different questions: "It's not because it is impossible, see that's what science asks, it's not feasible… [in technology] in the end it's the feasibility that's decisive."[13]

IBM researcher Tak Ning, who was a Micro Tech 2000 participant and advocate, draws a distinction between research and product roadmaps:

> Research roadmaps are somewhat different than product roadmaps. Research roadmaps usually don't try to take such small steps. You take big steps and Micro Tech 2000 was one of the big steps.[14]

The evolution of these research-oriented roadmapping activities into an official industry roadmap was covered in detail in Chapters 9 and 10. In sum, by the early 1990s the U.S. semiconductor industry was ready for such an approach and had deemed it a priority. By accepting the responsibility for the NACS recommendation to "Implement a Semiconductor Technology Roadmap for the Industry" (NACS, 1992:18),[15] the SIA initiated a process that has

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[13] Steve Kline, personal interview, June 13, 1996.
[14] Tak Ning, personal interview, July 18, 2000.
[15] This was one of only two new recommendations issued by NACS in their final report, *A National Strategy for Semiconductors: An Agenda for the President, the Congress, and the Industry*, February 1992. The other recommendation was "Encourage Increased Collaboration and the Formation of Consortia." Ironically, NACS has been most remembered for the nineteen other recommendations made in its first two years, most of which were deemed too interventionist for the Government at the time. Thus, none of these previous recommendations was seriously ever acted upon. Micro Tech 2000, as controversial as it was at the time, was acted on by industry with the development of the SIA Roadmap and perhaps is NACS' most successful endeavor.

now evolved to an on-going effort of international scope involving all major sectors of the global semiconductor community.

2002 and Beyond

What's next? A peek into the 2002 ITRS Update, presently underway, reveals that the 2yr accelerated scaling pattern will *not* be assumed beyond the 2001 ITRS: "No changes to the [2001] ORTC scaling targets and chip size models—first time since 1994 NTRS!"[16] This means that the accelerated timing pattern indicative of the industry roadmap era may not be repeated in the 2002 Update. If this is the case, the "pull-in" process begun in the 1997 NTRS will stop and straight lines will be drawn down to link nodes in a similar fashion as between the 1992 and 1994 Roadmaps. Other factors may be at play. Most notably is the continued economic downturn in semiconductor demand. Some analysts are forecasting that it may be 2004 before the industry recovers to its 2000 record level where worldwide revenues exceeded $200 billion. Cyclical demand is typical in this industry, however the severity of the present downturn is unprecedented (see Figures 4-18 and C-8).

Persistent softness in the present U.S. macroeconomic conditions may affect these forecasts further. While demand factors are not the focus of this study—in theory Moore's Law and the *Technology* Roadmap process are supply-oriented—the reality is that investment patterns are tied to demand. Thus, downstream as well as upstream economics are always a consideration. The preceding downturn from 1996 to 1998 was one factor that contributed to the delay in the transition to 300mm wafer tools and process technologies.

Of course one consequence of the advanced pace of technology is the earlier arrival of the real physical limits of semiconductor technology. Red cells in the Roadmap blocks in the technology requirements tables identify *manufacturable solutions that are NOT known*. The ITRS is now full of red cells to the extent that these red cells collectively form a proverbial “red brick

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[16] Alan Allan, "Overall Roadmap Technology Characteristics (ORTC) Overview," PowerPoint presentation, July 24, 2002.

wall" in the not too distant future. The 2001 ITRS fully acknowledges that future solutions will need to be qualitatively different to avoid hitting the "wall":

> The *ITRS* time horizon (15 years) provides a limit to what may be considered "on/off the Roadmap." To date, each edition of the *ITRS* has been built around a view toward continued scaling of CMOS (Complementary Metal-Oxide-Silicon) technology. However, with the 2001 edition, we are reaching the point where the horizon of the Roadmap challenges the most optimistic projections for continued scaling of CMOS. It is also difficult for most people in the semiconductor industry to imagine how we could continue to afford the historic trends of increase in process equipment and factory costs for another 15 years! Thus, the *2001 ITRS* begins to address post-CMOS devices.[17]

In fact, the first of several *Grand Challenges* cited in the 2001 ITRS long term timeframe (i.e., 2008 through 2016) is a call for "Non-CMOS Device and Architecture Including Interconnect and Memory." Developed by the Process Integration, Devices, and Structures (PIDS) TWG, this section of the ITRS explicitly recognizes that research and development on emerging non-CMOS devices is proceeding rapidly toward the end of the Roadmap.[18] As previously discussed, a new section appears in the 2001 ITRS that addresses "Emerging Research Devices" (see Hypothesis 8).

In the short-term, the next technology node (90 nm in 2004) may be the most difficult to achieve given economic and other factors. At the same time, leading-edge device makers seem to be prepared to continue technology acceleration. Figure 11-2 compares node scaling trends of traditional CMOS devices (3yr node scaling) with combined NTRS/ITRS scaling (3yrs, 2yrs, then 3yrs) and Intel's latest Lithography Roadmap (2yrs). This comparison suggests a relationship between Intel and industry Roadmaps and might partly explain a major element that helps accelerate technology nodes. How much does Intel affect ITRS (industry) technology acceleration? According to Chi Shih Chang, who has actively participated in the Roadmap process as a device maker (IBM), Consortium member (Sematech), and supplier (Kulicke and Soffa), no single firm, including industry-leader Intel, drives the industry Roadmap. The key to acceleration is coordinated availability of tools. Tool makers will not make investment decision off

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[17] 2001 ITRS, 2.
[18] Ibid., 14.

of one company's roadmap, but will check against the ITRS since this is a consensus document reflecting all needs. Applied Materials, the leading SM&E firm, and other tool makers might begin advanced development based on Intel's Litho Roadmap, but typically will not alter shorter-term production decisions. Chang summarizes, "ITRS and Intel Roadmaps influence each other, but the ITRS definitely influences supplier roadmaps."[19]

The survey instrument, list of respondents, related statistics, and detailed analysis of each survey research question are included in the appendix.

[19] Chi Shih Chang, telephone interview, September 11, 2002.

CHAPTER 12: Implications for Industry Strategies and Public Policies

"Companies in the semiconductor industry have pioneered in creating a comprehensive approach to collaboration with government and universities, one that includes … a detailed industry technology roadmap."

- Donald Rea, Harvey Brooks, Robert Burger, Richard LaScala[1]

"Before, when IBM was trying to convince the supplier infrastructure to work with us on a new technology, we had to spend a lot of time convincing them that this was real, that it was not just IBM going off on its own in a certain situation, We lost time doing that, but now the discussions with the suppliers go very rapidly. The roadmap is very helpful in that regard."

- John Kelly III[2]

"I figure that the ROI for the SIA Roadmap is an astounding 640% per year."

- G. Dan Hutcheson[3]

"Policy problems are harder to solve, and probably more important than the technology ones. Policy doesn't have a simple answer. Sometimes it has to do with attitude, sometimes it has to do with culture, sometimes it has to do with the legal framework."

- Vint Cerf[4]

"It's absolutely critical for the federal government to fund basic research. Moore's Law will take care of itself. But what happens after that is what I'm worried about."

- Gordon Moore[5]

This chapter examines macro level effects of the Roadmap in both private and public arenas.

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[1] Caption below title in Donald G. Rea, Harvey Brooks, Robert M. Burger, and Richard LaScala, "The Semiconductor Industry—Model for Industry/University/Government Cooperation," *Research-Technology Management*, July-August 1997, Vol. 40, No. 4, 46.

[2] John Kelly III, quoted in David Lammers and Robert Ristelhueber, "SIA Road Map Charts Wild Ride," *Electronic Engineering Times*, November 22, 1999. Kelly was vice chairman of the SIA and general manager of IBM's microelectronics division at the time.

[3] Excerpted from an e-mail, February 15, 1999, subject "The Chip Insider: 990216." Hutcheson is CEO of VLSI Research Inc.

[4] Vint Cerf, quoted in *KRT/San Jose Mercury-News*, 3 Jun 2002, http://www.siliconvalley.com/mld/siliconvalley/3392998.htm

[5] Gordon Moore, quoted in Dean Takahashi, "Sounding the Alarm," *Electronic Business*, Vol. 27, No. 11, November 2001.

The Roadmap as Strategy

As described in Chapter 2, technology roadmaps and roadmapping practices are a contemporary form of collective strategic planning. Regarding industry strategies, the Roadmap is the technology strategy of the SIA and its global counterpart organizations. As such, it serves a central role in helping to prioritize industrial resource investments in research, semiconductor manufacturing equipment and materials, fab construction and upgrade, even specialized labor. From a public policy standpoint, similar benefits are derived from mission agencies and national labs engaged in semiconductor R&D. In both cases, however, a more general question concerns the traditional industry-government connection that has diminished over the years in this once "critical technology" area. The Roadmap, in many ways, helps fill this void by providing the best available knowledge of present and future semiconductor technology needs that institutions, both public and private, can easily reference. It remains credible because representatives from these very institutions participate in maintaining the Roadmap for everyone's common benefit.

The Roadmap is, in fact, a by-product of public policies crafted in the 1980s in response to rapidly declining global market shares of the U.S. semiconductor industry. This development, by itself, is an interesting study of public policy and parallels that of the creation of Sematech as an early public-private arrangement. Much of the background on the emergence of the Roadmap through policy actions that included VHSIC, Sematech, and NACS, has been revealed in Chapters 9 and 10. From this analysis it is quite clear that the government played a significant role in assisting industry to develop a comprehensive strategy to regain and retain a world leadership position in semiconductor technology. Central to this was the creation of technology roadmaps, first within the industry's research consortia (especially Sematech), then by NACS with Micro Tech 2000, the forerunner to the SIA Roadmap.

The overarching research question of this study is: *How have technology roadmaps affected innovation, strategy, and policy in the semiconductor industry?* While there is not a simple answer to this question, this study has demonstrated that technology roadmaps in general, and the ITRS

in particular, have had profound influence on all three topics of interest. At a closer level of examination, one of the hypotheses of this study was:

> *The key driver for the SIA Roadmap has evolved from a competitively defensive, national industry strategy to a more universal and global strategy to stay on the industry's productivity curve as defined by Moore's Law.*

Indeed, this was found to be the case. At the same time the achievement of a *de facto* industrial policy goal of regaining leadership in international competitiveness in the early 1990s has meant that the public policy needs have changed considerably. Today's policy regime is much different—and much more diminished—than it was a decade ago. This chapter examines why this has occurred and what this might imply for future policies.

Four additional questions were asked of respondents that attempted to probe deeper into the Roadmap's influence on innovation, strategy, and policy:

1. *In what ways has the Roadmap influenced technological innovation in the semiconductor industry?*
2. *In what ways has the Roadmap influenced corporate strategies and public policies for the industry?*
3. *Does the SIA roadmap foster roadmapping activities in firms, or vice versa?*
4. *To what extent do industry and firm roadmaps line up? Is there an underlying structural hierarchy among various roadmaps? If so, is it intentional?*

The answers to these questions are summarized in Chapter 11 and need not be repeated, but the findings show strong evidence that the Roadmap affects particularly the pace of innovation, while having noticeable influence on corporate strategies and internal company roadmaps. On the other hand, the public policy effects are not as clear. The chapter will now proceed to consider industry level strategies and national level public policies.

The Roadmap and the Industrial Research Agenda

In the area of strategy, the Roadmap has had far-reaching effects. In the area of research—its first purpose—the Roadmap has become the very basis for strategic planning at the industry's two flagship U.S.-based research consortia: SRC and International Sematech. It was realized

early on that as the Roadmap represented more accurately industry's needs, then it made it much easier for member companies of these consortia—who make up most of the industry—to agree on the agendas that best suited the most critical requirements in the context of limited resources. One needs to only look at Sematech's and SRC's strategic plans, especially Sematech's present operating theme: *Realize the Roadmap*.[6] This is a marked change in mission from the "beat the Japanese" implicit objective that was so visible in an earlier era when global marketshare charts adorned the walls of the consortium. Now without the 'attached strings' of federal government support and essentially a 'won' battle, International Sematech has reformulated its mission as a truly global participant. The Roadmap is at the heart of this new mission with a call to affect the outcomes of the Roadmap. In other words, to make it happen (i.e., *Realize the Roadmap*). The ITRS provides the performance envelope as shown in Figure 12-1.

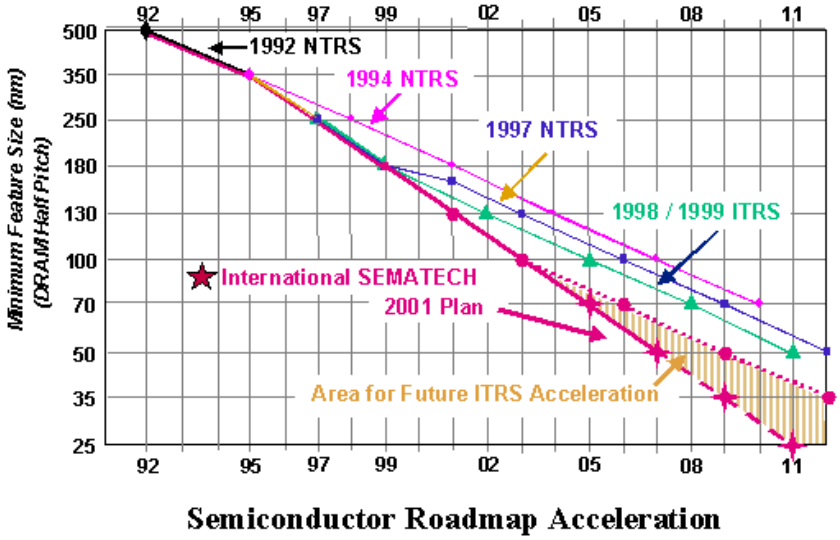

Figure 12-1. Sematech 2001 Plan, "Realizing the Roadmap"

Source: SEMI, "What's Up From SEMI - Industry Report: *International SEMATECH: "Realizing the Roadmap,"* July 2001, http://dom.semi.org/web/wsemi.nsf/webdocs/8251D7045A3F586E88256A7E007AB911

Recall the difficulties in the early days of Sematech finding consensus on the research consortia's mission as the fourteen initial member companies brought disparate individual needs

[6] International Sematech's operating goals include, "Build the necessary infrastructure to realize the Roadmap." Source: ISMT 2002 Corporate Summary, 2.

to the table. Leading edge companies were interested in developing a specific product (i.e., a competitive DRAM or similar chip), thus the construction of a state-of-the-art fab while smaller firms were more interested in obtaining process knowledge (from larger firms). Finally, chip makers in the defense sector were interested in addressing their unique needs. With agreement that the ITRS is the common source that aggregates these needs—members actively participate in its development—it has become much easier for International Sematech (and other consortia) to address the needs of member companies.

In terms of the SRC, they had reorganized in 1995 to align with the Roadmap technology thrust areas, however they reorganized again in 1998/9 to go back to be more science-based, as they were initially structured. The Roadmap plays a major role in defining their research agenda, and ultimately in issuing work to universities, but the downside sometimes is a kind-of path dependency focus on short-term needs, almost "engineering studies" as they refer to them (i.e., already know the answer) vs. basic research into novel materials, methods, device structures, etc. Research managers at the SRC are very mindful of the necessary balance that needs to be maintained in their research agenda.[7]

Perhaps one of the most significant contributions of the Roadmap—for the U.S. industry at least—is the alignment of disparate research activities according to the 15yr timeframe as shown in Figure 12-2. This timed division of responsibilities will be used to examine three areas of research at progressively longer-term stages along the continuum. Each addresses very different aspects of semiconductor technology, but all share the Roadmap's timing framework. The first involves the all-important SM&E industry's *integration* of new materials, tools, and processes (recipes) and would be considered in the *white* space in Figure 12-2. The second involves Extreme Ultraviolet Lithography (EUVL), a next-generation lithography (NGL) that is approximately mid-way through a 10yr active development process and would be classified in the *yellow* space, probably at the farther end. The last addresses the "end of the Roadmap" range,

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[7] Bob Burger, Ralph Cavin, Dan Herr, Jim Hutchby, Bill Joyner, personal interviews, August 1, 2000.

the *red* space, which is the purview of the MARCO Focus Center program, whose mission is to deliberately explore novel materials, device structures, etc.

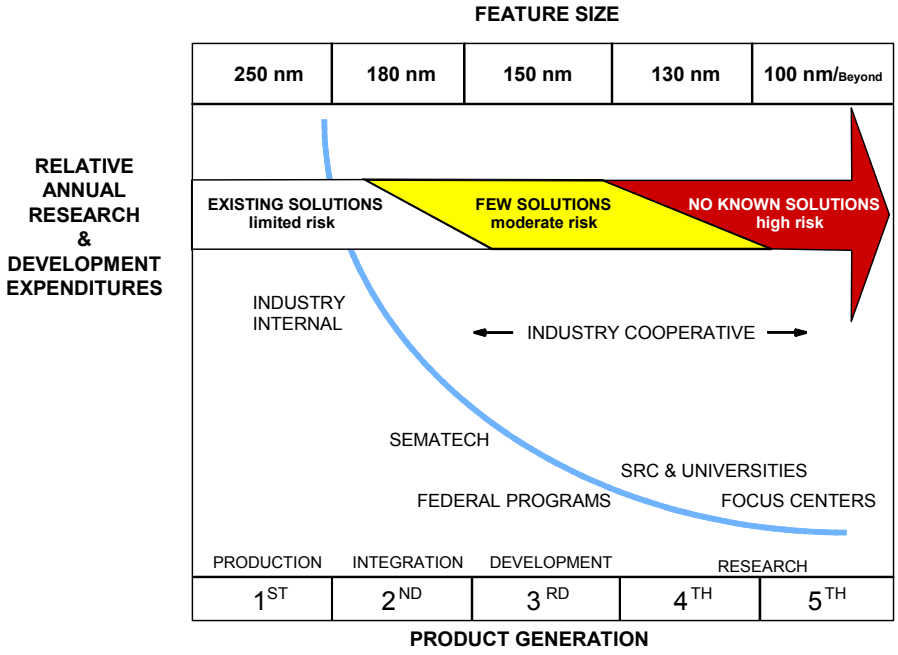

Figure 12-2. Roadmap Timing and Research Responsibility

Source: 1997 NTRS, Figure 2 Present Day Commitment of Research and Development Expenditures, 7.[8]

A more recent application of this research alignment to the Roadmap that considers international consortia involvement is from Intel:

- N+1 (current technology node +1, equivalent to 2nd product generation in Figure 10-2): Intel plus support from International Sematech
- N+2: International Sematech, IMEC, and Intel (smaller role)
- N+3 EUVL, SRC, ASET, and Intel (even smaller role)

[8] Note that the definitions of the colored areas changed in subsequent Roadmaps as follows: White—Manufacturable solutions exist, and are being optimized; Yellow—Manufacturable solutions are known; Red—Manufacturable solutions are NOT known. Further, a new status color was introduced in the 2002 Update as striped beige with a red diamond; it is defined as "Interim solutions are known" and appears between yellow and red. This category represents an engineering "workaround" but one that is not sustainable.

- N+4 MARCO Focus Center Research Program and Intel (smallest role)[9]

IMEC is a European consortium and ASET is a Japanese consortium. EUVL, like Sematech, began as a U.S.-only consortium but has since gone international. Noticeably absent is "N" or the current generation which is technically not pre-competitive so firms will not share (nor divulge) their research plans for devices in production.

White (Manufacturable Solutions Exist, and Are Being Optimized)

In ranges N and N+1 (and to some degree N+2) is the role of the semiconductor materials and equipment (SM&E) industry where the impact of the Roadmap has been profound. These suppliers or tool makers as they are often referred to, hinge their technology strategies to the Roadmap. Here is where industry cadence really matters. Moore's Law is only realized when chip makers have the increased capability—as in more advanced equipment and materials—to fabricate more complex devices. Tool makers, more than anyone, need to understand this cadence so they can bring on line the next generation lithography, etch, or deposition tool when their customers—the chip makers—really need them. As Tak Ning, repeats often, "Timing is everything."[10] There is a competitive advantage of early market entry, but if the market is not ready for your product, that's almost as bad as being late to market. A few stark examples of this follow:

1. *Too early:* transition to 300mm (12 inch) diameter silicon wafers—based on Roadmap timing—occurred in the midst of an unanticipated industry cycle downturn (e.g., Asian crisis '97-'99, see Chapter 7 for more detail), increasing inventories and reducing industry investment, which in turn allowed chip makers to extend usability of existing 200mm (8 inch) tools. The net result was a delay of about two years, and a lot of ill-feeling between suppliers and chip makers. Blame was placed on the Roadmap for inaccurate forecasting. Although not

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[9] Paolo Gargini, "Intel Process Technology Trends," PowerPoint presentation, IDF, February 26, 2001, slide 12.
[10] Tak Ning, personal interview, July 18, 2000.

totally justified (there are several other factors to consider), this issue did make limitation of the Roadmap much more visible: it is a *technology* roadmap, not an economic roadmap. It is in fact developed by technologists, often criticized for not being sensitive to the economics of their decisions. Increased dialogue between the two communities has since resulted in the form of a widely-attended *Industry Executive Forum* series organized by International Sematech along with other mechanisms.

2. *Too late:* there are numerous historical examples since this is a much more common case than being too early. The most notable example is Intel's state-of-the-art fab built in the late 1980s at a cost of three-quarter billion dollars that sat idle for 18 months because equipment was not yet available.[11] This was a big reason for Sematech's early shift from a horizontal to a more vertical focus by fostering better relationships with the supplier sector. This is in fact what the Japanese had achieved beginning with the VLSI program a decade earlier. It would become such an important issue that a sister organization called SEMI/Sematech was established (and housed) alongside Sematech early on to concentrate on U.S. supplier relations.

3. *On time (through coordination):* Browning and Shetler emphasize "the need to synchronize the "cadence" of development of tools and manufacturing processes with advances in chip design, as well as to make timely purchases of the new equipment required."[12] Chi Shih Chang, a very active Roadmap participant, stresses that because manufacturing facilities are so expensive, firms can't afford to have a factory without a full tool set. It could be only one or two tools missing, the result would be the same. Chang states that the Roadmap really makes sure that manufacturing is ready—specifically that alpha, beta, and final manufacturing tool sets are ready in sequence. Karen Brown underscores the importance of close coordination with suppliers of lithography technology: "a systems approach is really

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[11] Turner Hasty, telephone interview, June 1, 2000.
[12] Roadmap references in: Larry D. Browning and Judy C. Shetler, *Sematech: Saving the U.S. Semiconductor Industry*, College Station, TX: Texas A&M University Press, 2000, 108, quotes in original.

> required. Exposure tool, resist, mask and metrology are all needed for success."[13] She states that changes in industry can't really be made without integration of disparate companies offering a wide variety of materials and equipment. The Roadmap helps pull everyone together and most importantly integrates the timing of supplier availability.[14]

As discussed in Chapters 10 and 11, the technology acceleration or node "pull-in" that has occurred since the early Roadmaps is attributable in large part to closer coordination with suppliers. The 2yr node timing that seemed to run counter to the traditional 3yr cycles had been demonstrated at Sematech almost from the start. Because Sematech did not develop these processes from scratch the 2yr timing demonstrations really reflected some of Sematech's member companies' capabilities in a controlled environment, with a neutral party (i.e., Sematech) serving as intermediary between supplier and chip maker. U.S. chip makers were not alone in this ability. Recall the organized effort of the Japanese VLSI consortium in the late 1970s that enabled Japanese firms to speed up introduction of successive DRAM generations, primarily through improvements in manufacturing tools. Furthermore, according to Sematech, Samsung Electronics in Korea had completed five successive 2yr technology node cycles, culminating in the demonstration of a 256Mb DRAM in 1994.[15] NEC was also able to advance technology ahead of the Roadmap:

> NEC is accelerating ahead of the 1997 SIA Roadmap. The introduction in 1997 and 1999 of 0.25m and 0.18m design rules is in accordance with the SIA roadmap. However, in the following years NEC is pulling ahead of the SIA roadmap with the introduction of 0.15m in 2000, 0.13m in 2001, and 0.1m in 2003 design rules in volume production.[16]

Finally, Intel has been successful in maintaining a 2yr cycle for almost a decade as shown in Table 12-1.

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[13] Karen H. Brown, "SEMATECH and the national technology roadmap: needs and challenges," *SPIE, Optical/Laser Microlithography VIII*, Vol. 2440, 1995, 34.
[14] Karen Brown, telephone interview, August 18, 1999.
[15] Tom Seidel in Chapter 8, footnote 47, of Larry D. Browning and Judy C. Shetler, *Sematech: Saving the U.S. Semiconductor Industry*, College Station, TX: Texas A&M University Press, 2000, 252.
[16] Source: Nikkei Microdevices, September 1998. Presented by Paolo Gargini in November 23, 1998 PowerPoint presentation.

Table 12-1. Intel Manufacturing Process Evolution

			Actual			*Forecast*	
Process name	P852	P854	P856	P858	P860	*P1262*	*P1264*
Production	1993	1995	1997	1999	2001	*2003*	*2005*
Generation	0.50	0.35	0.25	0.18	0.13	*0.10*	*0.07 mm*
Gate Length	0.50	0.35	0.20	0.13	0.07	*0.05*	*0.03mm*

Source: Paolo Gargini, "Intel Process Technology Trends," PowerPoint presentation, IDF, February 26, 2001, slide 12.

Once this acceleration pattern became more public through the Roadmap and as suppliers increasingly became more confident in the timing of technology needs laid out by the Roadmap, the 2yr cadence became more the rule than the exception. Coupled with this is the "beat the Roadmap" behavior that was reported so often by Roadmap participants. The competitive nature of humans (and organizations, even nations in a market system) helps explain why the Roadmap technology nodes—especially in the early editions—did not hold from one edition to the next as the industry would consistently achieve the targets faster than projected. In fact, this caused the addition of an off-year "update" because as Paolo Gargini's opening quote from Chapter 10 states, "You cannot have a document live in this industry for two years." Steve Brueck, Director of Center for High Technology Materials at the University of New Mexico, characterizes the Roadmap as "average," thus not the real benchmark:

> "The Roadmap is 'average,' but no one wants to be average so they 'beat the roadmap,' thus they collectively accelerate the roadmap."[17]

As previously stated this theme was repeated often by informants. It is probably one of the most consistent themes observed.

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[17] Steve Brueck, telephone interview, July 7, 2000.

Yellow Space (Manufacturable Solutions Are Known)

Moving further out into the N+3 range the technical challenges become far greater. A prime example of this is next-generation lithography (NGL), the method of patterning chips beyond the limits of optical lithography. Figure 12-3 was used earlier in Chapter 8 to illustrate how roadmapping helps identify possible solutions which can then be narrowed so that scarce resources may be focused on the most likely solution(s). It is used again here because NGL has historically been one of the most challenging technologies for the industry. In fact, the 1997 NTRS listed "Affordable Lithography At or Below 100 nm" as one of the Roadmap's *Grand Challenges*, calling for a "completely different approach … required for patterning as feature sizes approach 100 nm."[18] The optional fingers extending into the N+4 range in Figure 12.3 clearly indicate this.

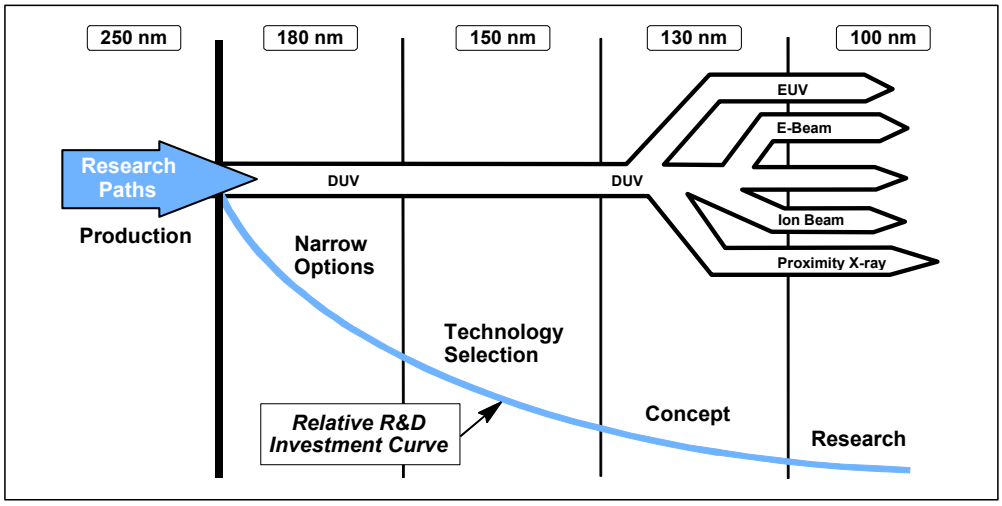

Figure 12-3. Future Lithography Technology Alternatives

Source: 1997 NTRS: Conceptual Illustration of Today's Research and Development Investments for Future Production Technologies, Figure 1, 2. (also used as Figure 8-1)

[18] 1997 NTRS, 9.

Recall from Chapter 10 the legacy of optical lithography—that it has consistently been projected to end an average of six years (about two generations) into the future in every Roadmap. This tendency goes back at least another decade before formal industry roadmaps (e.g., it is evident in the early Sematech strategic workshop held in January 1988 on advanced lithography).[19] As has been discussed, significant investment totaling in the billions of dollars have been spent by industry to develop x-ray (IBM, Nikon), electron beam (AT&T), and other post-optical lithographic technologies. The DoD's DARPA has also funded x-ray lithography development at roughly $50 million annually for several years. Despite this intense focus, no clear winner has emerged. Gordon Moore aptly sums up the long-standing challenge, "Because the semiconductor industry has a major problem to solve here … eventually we'll figure out what the right choice is."[20]

The 1994 NTRS again made this choice very clear and for the first time extreme ultraviolet (EUV) lithography appeared on the list of possible solutions. While EUV had been discussed as an option in earlier roadmaps (it follows visible light and DUV on the frequency spectrum), researchers mostly felt it its use was limited to one or maybe two generations so higher-frequencies like x-ray were often chosen to pursue. But as optical, then its extension DUV, lithography continued to be stretched to successive generations, EUV emerged as a logical successor candidate that might also be extended far longer than initially expected. In the language of Chapter 4, EUV was an evolutionary innovation whereas x-ray and other novel approaches were revolutionary. Consistent with the innovation tradition of the industry, EUV soon became an apparent successor candidate.

Intel began substantial investment in EUV in 1996, and led the establishment of a major EUV lithography initiative, a major private-public partnership between semiconductor manufacturers between three U.S. chip makers and three U.S. DoE National Laboratories (i.e., Lawrence

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[19] Sematech, "Final Report: Sematech Planning Workshop on Advanced Lithography," Burlingame, CA, January 25-27, 1988. Sematech archives.
[20] Gordon Moore, "Extreme Ultraviolet Lithography," (press conference call) September 11, 1997, http://www.intel.com/pressroom/archive/speeches/euv91197.htm

Livermore, Lawrence Berkeley, and Sandia). The program was announced in September 1997 as a three year $250 million cooperative research and development agreement (CRADA) called EUV Limited Liability Company (LLC). Intel, Motorola, and AMD were the initial industry partners. IBM, Micron, and Infineon Technologies later joined the consortium and even Dutch lithography tool maker ASML was allowed to participate.[21]

The three Department of Energy labs had developed EUV technology as part of their efforts to ensure the safety, reliability and security of the nation's nuclear weapons stockpile. Moore explains:

> The national labs has done sufficient R&D to establish the proof of concept, to demonstrate the source, to show that the optics can be made at least at some level to use this kind of radiation. But much remains to be done to move this on to a stage where it can really be designed into equipment we could use in our production lines… The EUV Limited Liability Corporation is going to pick up this program which would otherwise have fallen off the laboratory's plate.[22]

The EUV LLC was a novel approach to longer-term applied research. Instead of individual companies paying their own way (as had been the case with x-ray and electronic beam approaches), or asking government agencies to fund their research, industry was paying the government labs to perform research they were already familiar with. This represented a different twist to private-public partnerships; it was the biggest investment the private sector had ever made in a Department of Energy CRADA.

It will take an estimated 10 years from start of research to volume production, which should coincide with Roadmap timing requirements. Involvement by leading lithography suppliers such as ASML, Nikon, and Canon provides early access to beta and production tools. The proof of concept phase is almost completed and continued support from industry and other institutions including research consortia and foreign governments demonstrate the strong backing behind EUV. International Sematech has even established a new site (i.e., Sematech North in Albany, NY) dedicated to NGL technologies including EUV.

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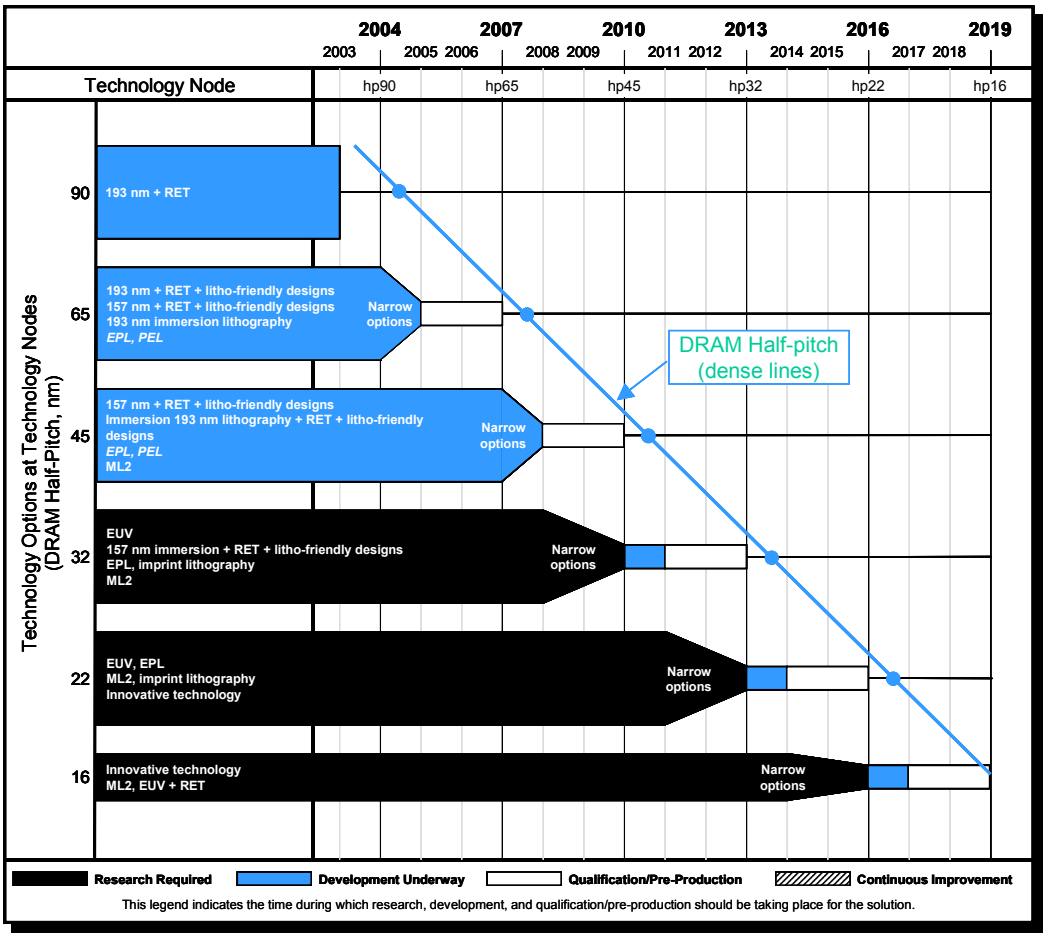
[21] ASML acquired U.S. stepper manufacturer SVG Lithography.
[22] Moore, op. cit.

Meanwhile the 2003 ITRS now shows fewer options for post-optical or NGL alternatives listing in order, EUV, EPL (electron projection lithography), maskless (ML2), and imprint lithography as potential successors (see Figure 12-4). Interestingly, proximity x-ray lithography and ion projection lithography, once leading NGL candidates, are no longer considered as potential candidates. E-beam was last considered in the 1999 ITRS. Thus, comparing Figure 12-4 options with those listed in Figure 12-3 where only EUV remains as a viable option shows how much has changed in six years.



Technologies shown in italics have only single region support.
RET—resolution enhancement technology EUV—extreme ultraviolet EPL—electron projection lithography
ML2—maskless lithography PEL—proximity electron lithography

Figure 12-4. Lithography Exposure Tool Potential Solutions

Source: 2003 ITRS, Figure 53, 386. (also used as Figure 10-9b)

The most recent Roadmap continues its primary role of focusing on common technology needs and potential solutions, which continually undergo change:

> Although many technology approaches exist, the industry is limited in its ability to fund the simultaneous development of the full infrastructure (exposure tool, resist, mask, and metrology) for multiple technologies. The elimination of proximity x-ray and ion projection lithography has not reduced the number of technologies that require simultaneous development, because of the recent emergence of immersion lithography and imprint lithography. Closely coordinated global interactions within industry and the universities are absolutely necessary to narrow the options for these future generations.[23]

Thus there is a good chance that the current candidate list will shorten while adding new options six years from now. This is a major contribution of the Roadmap.

Red Space (Manufacturable Solutions are NOT Known)

The last example is the Microelectronics Advanced Research Corporation (MARCO) Focus Center Research Program, initiated in 1997, that aims to address end-of-the-Roadmap challenges in the N+4 range and beyond the Roadmap's 15yr research horizon. The MARCO Focus Center Program is perhaps the strongest case of combined industry strategy and public policy that has resulted from the Roadmap. Some important background is offered. Recall from Chapter 10 that one primary purpose of the 1992 Roadmap and 1994 NTRS was to consolidate the research needs of the industry in order to "speak with one voice" to government funding agencies. The very first *Key Technology Challenge* discussed in the 1992 Roadmap is management of chip design complexity. This is further defined in these Roadmap captions:

> Currently, design activities are based on loosely coupled ad hoc collections of tools and techniques. Over the next 15 years, the complexity of chips and systems will grow so dramatically that new techniques will be needed to handle the design and test processes. Failure to create these new techniques will result in the failure to convert expensive technology into useful products… The key to the problems of design and test is the management of complexity at all levels. The exponential growth of component count has not been matched by progress in software productivity or fundamental algorithm.[24]

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[23] 2003 ITRS, 385.
[24] 1992 Roadmap, Workshop Conclusions, 24-25.

This message would be repeated in the 1994 NTRS with greater emphasis and expanded definition and clarity. As discussed in Chapter 10, four *Grand Challenges* were aimed in large part at government funding agencies:

(1) Productivity Improvement
(2) Complexity Management
(3) Advanced Technology Development
(4) Technology Development Funding[25]

The last challenge made very clear that the extensive resources expended each year on research by the semiconductor industry required *even greater* financial resources to meet the challenges presented by the Roadmap.[26] The 1997 NTRS, despite significant changes since 1994, echoed a similar call in *The Research and Development Challenge*, one of six *Grand Challenges*.[27] Structural changes in industry underpin the rationale for research needs in the following caption:

> Throughout the history of the integrated circuit industry, much of the equipment and processing research for future manufacturing technology was performed in large, vertically integrated companies in the semiconductor industry. These companies relied on the revenues from systems sales to fund the basic materials and processing technology research, as well as the device research, required to continue to advance the technology according to Moore's Law. The extensive effort and infrastructure required to reduce research concepts to practice was also frequently provided by these vertically integrated companies. To a large extent, the industry is still living off the benefits of its past research and development… With the change of the industry in the U.S., approaches must be found to provide adequate, long-term research to replace the loss of the extensive in-house equipment and processing research in those central research labs of large, vertically integrated companies. Also, a new paradigm must be found to provide adequate research and development for new concepts that will be needed as well as the infrastructure to reduce the research concepts to practice.[28]

Following the 1992 Roadmap, the SIA had lobbied the federal government extensively to assist in the implementation of the Roadmap. This message had already been heeded by government funding agencies and was welcomed by the incoming Clinton Administration, whose

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[25] 1994 NTRS, 5-7.
[26] Ibid., emphasis in original.
[27] 1997 NTRS, 12.
[28] Ibid.

Technology Policy helped create a joint industry/government Semiconductor Technology Council.[29] Established by Congress under the National Defense Authorization Act of FY1994 (P.L. 103-160), the Council replaced the Advisory Council on Federal Participation in Sematech. The Council's charter included a responsibility to the Roadmap:

> Assess technology progress relative to industry requirements and Federal Government requirements, responding as appropriate to the challenges in the national semiconductor roadmap developed by representatives of industry, the Federal Government, and institutions of higher education.[30]

One rendering of the research challenge was a widely-circulated graph commonly referred to as the "design productivity gap" that compared the exponential growth rate in chip complexity (i.e., Moore's Law) with the corresponding growth rate in chip design manpower (see Figure 12-5).

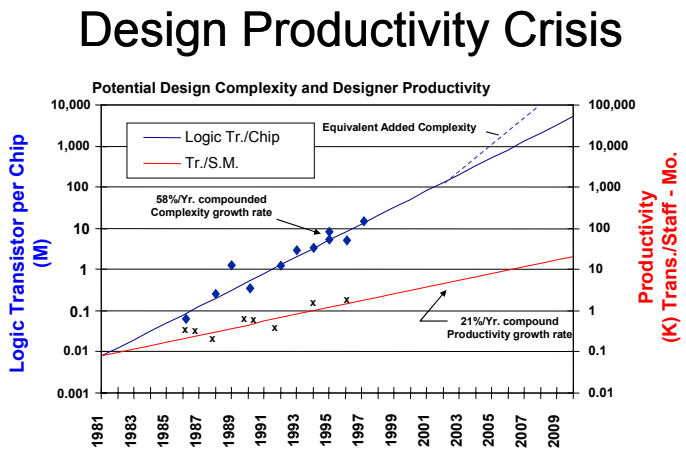

Figure 12-5. IC Design Productivity Gap

Source: Steve Schulz, "ITRS Design TWG," PowerPoint presentation at ITRS Roadmap Conference, Santa Clara, CA, July 8, 1999, slide 9. Also appears in 1999 ITRS, Figure 5, 36.

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[29] William J. Clinton and Albert Gore, Jr., Technology for America's Economic Growth, A New Direction to Build Economic Strength," February 22, 1993.
[30] U.S. Code Collection: Title 15, Chapter 72, Subchapter 1, Section 4603. Semiconductor Technology Council, paragraph b, 2, F, charter filed 1 April 1998, http://www.apeccp.org.tw/doc/USA/Policy/ch72/4603.htm

Discovering the *End of the Roadmap*: Focus Center Research Program (FCRP)

Figure 12-5 makes very evident the IC design community's challenge of keeping pace with the very technology they are to design. The Semiconductor Technology Council assessed the 1994 NTRS and determined in their first report, "Implementation of the Semiconductor Technology Roadmap will be much more costly than it is today or planned… In its best interest, industry should increase R&D investments toward more strategic areas."[31] The Council recommended that the industry focus R&D on advanced lithography and 300-mm wafers, however did not view the U.S. Government as a provider of funds for these applied research programs. The SIA, instead, proposed a longer-view research program to address issues critical to the attainment of end-of-Roadmap goals *not* currently on any research agenda. The proposal considered the broader research infrastructure but was geared primarily toward the academic research community with support from industry and guidance by means of the Roadmap:

> The Problem: We do not appear to have the research infrastructure in place to support rapid growth beyond the year 2000:
>
> - Competitive forces and high capital costs pull industry's time horizon for R & D inward
> - Federal support for civilian technology likely to decline substantially
> - Federal support of university research is flat (at best)
> - University laboratories are under-funded and under-equipped
> - Large funding gaps exist
> - Technology transfer difficult
>
> The Concept: Create a network of Industry-University Focused Research Centers to support implementation of the Roadmap (NTRS)
>
> - NTRS would be used as a guide in structuring focus areas
> - Each center would be managed by a director supported by industry
> - Each Center would operate with a staff that includes university faculty, full-time employees, visiting industry scientists and engineers, post-docs and students
> - Each Center could involve multiple universities with common R & D interests

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[31] Jack Robertson, "Semi Industry Not Keeping Up With Roadmap Timetable—Council Calls For Increased Spending in Strategic Areas," *Electronic Engineering Times*, December 2, 1966.

- Each Center would own, of have access to latest state-of-the-art equipment and facilities[32]

Larry Sumney of the SRC strongly supported the idea, particularly with regard to filling the design productivity gap, noting that by 2007 engineers would have to turn around microprocessor designs with up to 260 million transistors in as little as six months.[33] Recall the trend in complexity of microprocessor designs discussed in Chapter 3. After a year of review the SIA approved the Focus Center Research Program (FCRP) in another unique management and funding arrangement (see Figure 12-5). SIA member companies would fund 50% while 25% would come from a consortium of semiconductor equipment and materials companies. The remaining 25% would be funded by DARPA. MARCO was established in 1998 as a non-profit, wholly owned but separately managed subsidiary of the SRC.

The focus of the FCRP is to develop multi-university research efforts intended to address the technical challenges at the end of the Roadmap and beyond. Up to six centers will be established, each managed by a full-time university center director, to address one of the major technology focus areas of the Roadmap. Two Focus Centers were established upon announcing the program: Design and Test through the University of California at Berkeley (leading nine affiliated universities), and Interconnect through Georgia Institute of Technology (leading six affiliated universities). In 2001, two additional centers were set up: one in Materials, Structures & Devices at the Massachusetts Institute of Technology and another in Circuits, Systems & Software at Carnegie Mellon University. Finally, in 2003, a focus center for Functional Engineered Nano Architectonics was established at the University of California at Los Angeles. This fifth center is charged with the longest view to expressly research "off-Roadmap" post-CMOS

[32] James Glaze, "Semiconductor R&D for the 21st Century: Rethinking the Role of Our Universities," Presentation to Sematech Board of Directors, February 8, 1996, slides 4 and 7.
[33] George Leopold, "SIA Focuses on the Design Gap," *Electronic Engineering Times*, Issue 902, May 20, 1996.

technologies that have been discussed in the ITRS since 2001 (see Chapter 10). Figure 12-6 portrays the FCRP program structure while Appendix 12-A lists all the participating FCRP universities.

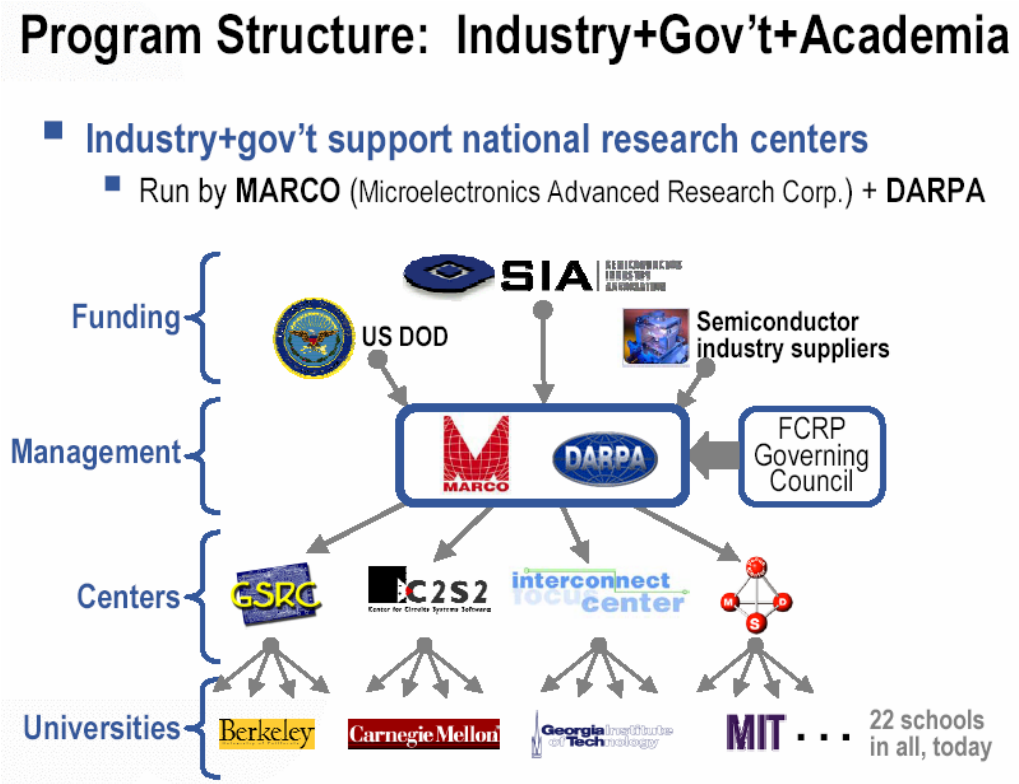

Figure 12-6. FCRP Program Structure

Rob A. Rutenbar, "The MARCO Focus Center Program for Semiconductor Research," FSA Presentation (PowerPoint), January 29, 2003, slide 8. Note that one more focus center (Nano Architectonics) and additional universities have since been added.

Annual funding for the program has gradually increased from $10 million in 1999 to $29 million in fiscal year 2004, of which government contributed $10 million.[34] Funding is expected to continue to ramp up to the projected $60 million level by fiscal year 2007. Since the focus of the FCRP is longer-term (i.e., N+3, N+4, and extending beyond the Roadmap as shown in Figure 12-7), the full effect of the program will not be realized for some time. Valuable research results have

[34] Author unknown, "U.S. to boost funding for semiconductor research," *Bank Systems & Technology*, March 16, 2004, http://www.banktech.com

already materialized and are being utilized in other DARPA programs.[35] As these results continue to materialize they will be reflected in—and in turn revise and improve—the Roadmap. Like other important research outcomes, they will "make it into the Roadmap," thus perpetuating its use and need.

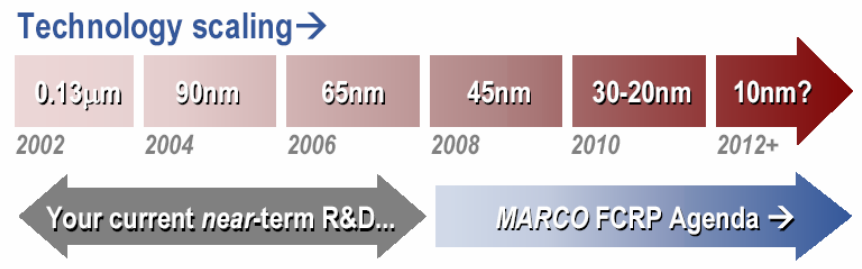

Figure 12-7. FCRP Research Time Scale

Source: Ibid., slide 7.

The Roadmap will continue to serve as the program's primary research guide. In terms of long-term research, the development of the FCRP is an enduring example of the strategy and policy implications of the Roadmap.

The last section addresses public policy pertaining to the semiconductor industry generally, and the Roadmap more specifically.

Public Policy

To help understand the changing roles of public policies over time, Table 12-2 summarizes salient features of semiconductor industrial innovation since the industry's inception. Note the steady increase in complexity as measured by device scaling that has been discussed throughout this thesis. Accompanying this trend are definitive changes in industrial leadership, innovation network, and public policy regimes.

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[35] Semiconductor Industry Association, "SIA Backgrounders: Semiconductor Focus Center Research Program—Laying the Groundwork for the Future of Microelectronics," January 9, 2004, 1.

Table 12-2. Semiconductor Industry Innovation Summary

Time-frame	Complexity (IC scaling)	Key technology driver	Sample capability	Industry leader	Industrial innovation network	U.S. public policy
1950s	N/A, single device	transistor, discrete components	hearing aid, transistor radio	Bell Labs	Bell Labs shared knowledge, electronic system houses dominate, infant merchant semiconductor industry emerges	U.S. government primary R&D sponsor and user
1960s	SSI/MSI	IC: gate array, shift register	mainframe computer, military/space systems	Fairchild	New semi industry displaces system houses, proliferation of spin-offs (i.e., 'Silicon Valley effect')	U.S. government initially sponsors IC industry
1970s	LSI	Kb DRAM, microprocessor 'chip set', microcontroller	calculator, minicomputer, industrial applications	TI, Motorola, Intel	SM&E industry develops, captive IC makers flourish (e.g., DEC), state-sponsored consortia appear (e.g., Japan VLSI)	U.S. government role minimal but starts DoD VHSIC program at end of decade
1980s	VLSI	Mb DRAM, microprocessor	PC, workstation, LAN/WAN, 'smart' devices	IBM, Japanese firms	Creation of U.S. industry consortia (i.e., SRC, Sematech), arms-length relationship between IC and SM&E industries	International competitiveness threat renews major U.S. government role, relaxed antitrust laws, major trade agreement, NACS created
1990s	ULSI	powerful microprocessor, DSP, ASIC	internet, enterprise systems, cell phone, PDA, other consumer electronics	Intel, Korean and Taiwanese firms	SIA Roadmap created, global partnerships and consolidation, proliferation and internationalization of research consortia (e.g., I300I, ISMT),	U.S. government role reduced to niche areas (e.g., metrology, NGL (e.g., EUV LLC), MARCO Focus Centers, nanotechnology
2000s	UULSI or NSI (*nano* scale integration)	GHz/Gb ICs, compound ICs, MEMS	wireless, telecom convergence, integrated information appliance, 24x7 connectivity	Intel, foundry industry	ITRS, continued industrial disintegration (e.g., fabless/foundry model more dominant), international consortia collaboration (e.g., ISMT and IMEC and Selete)	Renewed call for support of basic research in physical sciences, international collaboration (like space station) on post-CMOS R&D

Commenting specifically on the last column of Table 12-2, five phases or eras of national policy involvement during evolution of U.S. industry are discussed below:

1. *Late 1950s to early 1960s (military-centric)*: in the industry's nascent stages the DoD practically funded all the research, development, and commercialization of the integrated circuit. This has been covered extensively by others. Jack Kilby's 1958 discovery at TI was not under a defense contract but the significant amount of DoD contracts that were in place at the time no doubt had influence on IC development there for at least a decade. Fairchild was also a participant in DoD and NASA programs. Government purchases represented 100% of IC industry output in the early 1960s. Manufacturing was experimental (black art processes), thus yields were very low (10-20%) and unit costs were extremely high (as much as hundreds of dollars per device). Thus the government was really the only buyer in a position to support ICs since a feasible market didn't yet exist. Turner Hasty, who was head of TI's R&D in the 1960s, remembers the difficulties penetrating the commercial sector with ICs in those days. It was hard convincing buyers like computer makers that the IC was a viable alternative to discreet components. It took almost a decade for this to occur as described in Chapter 5. Recall the spawning of "Fairchildren" including National Semiconductor in 1966, Intel in 1968, AMD in 1969, among others. By the late 1960s venture capitalists were confident enough to fund these efforts. Note that most were spin-offs from existing firms all supported in some way by government programs.

2. *Late 1960s to late 1970s ("golden age" of U.S. industrial development, reduced government involvement)*: U.S. government efforts had fallen sharply by 1970 (representing roughly 20% of market and falling) as new commercial applications appeared in computers (e.g., DRAMs), consumer electronics (e.g., 'single chip' calculators and digital watches), and industrial applications (e.g., microcontrollers in factory control systems). The entrepreneurial spirit in an emerging "Silicon Valley" brought forth innovations at a break-neck pace. Companies' profits enabled them to fund research, development, and most importantly, capital expansion as a

definite "learning curve" pattern was established and recognizable in volume production runs. By the mid 1970s the U.S. IC industry was well established, user markets were convinced that integrated devices were far superior to discreet devices, and applications just seemed to drop in from the sky (e.g., digital watches). Chip makers produced and produced and young marketing staffs went off and found buyers. The U.S. industry was the undisputed global leader in semiconductors. Government involvement was nil—post-Apollo program and the end of the Viet Nam conflict meant significant draw-downs in government budgets that had previously spawned this industry a decade earlier.

3. *1980s (Japanese threat, second "golden age" of U.S. public policy)*: Rekindled age-old debate over industrial policy. Tensions between sympathetic Democratic Congress vs. indifferent Republican White House forced industry through newly formed SIA (created in late 1970s) to be very forthright in raising public awareness. NCRA, Semiconductor Trade Agreement, Sematech, NACS, National Competitiveness Act, "critical technologies" initiatives were all products of these efforts. Roadmap was direct descendant of these efforts. Another aspect that played to the industry's favor was defense: national security interests as Cold War concerns peaked during the 1980s. The VHSIC program was launched to address this and had significant spillover benefits.

4. *1990s (national to international transition, reduced public role)*: By the early 1990s Cold War was over and U.S. had regained lead of global market share. Japan in decade-long recession. Korea, Taiwan, later Singapore emerge as formidable global players with "foundry" model. Strong U.S. economy and changing political structure (sympathetic Democratic White House but antagonistic Republican Congress) meant continued tension and little policy involvement. Actually, less-so than the 1980s since national security no longer a driving concern. In fact, "commercial-off-the-shelf" (COTS) became the procurement strategy since commercial technology had since replaced advanced defense technologies as state-of-the-art. "Dual-use" was the term given to DoD development contracts that would find application

in both commercial and military environments. In 1994 Sematech gave notice to drop Federal funding in order to accept international members, later the *national* Roadmap transitioned to become *international* (ITRS). Other consortia followed suit (e.g., SEMI/Sematech became SISA).

5. Late 1990s to present (stateless era): As International Sematech, SISA (formerly SEMI/Sematech), the SRC, the ITRS, and other semiconductor institutions have become international entities, the major regional governments have redefined their involvement in the Roadmap process. The transformation of these once domestic-only, protectionist structures to international collaborative bodies has been swift and complete. This has all occurred in less than five years. The rationale is simple: it reflects the globalization of the semiconductor industry. A similar internationalization pattern has occurred in Europe, Japan, and other countries that had established state-sponsored consortia to assist/protect domestic semiconductor industries. As an illustration, the 2001 and 2003 ITRS editions read:

> Jointly Sponsored
> by
> European Semiconductor Industry Association
> Japan Electronics and Information Technology Industries Association
> Korea Semiconductor Industry Association
> Taiwan Semiconductor Industry Association
> Semiconductor Industry Association [U.S.]

U.S. Government involvement in this new international era continues as active *participant*. An example of this is the 25% contribution in the creation of MARCO Focus Centers to address end-of-Roadmap technology needs. Interestingly, the EUV LLC partnership with the DoE national labs initiated by U.S. chip makers (primarily Intel) to develop next-generation lithography now includes the leading European lithography tool maker (i.e., ASML) and has requested inclusion of leading Japanese manufacturers, Nikon and Canon. The reason: the technical challenges are simply too great for one nation to tackle. Global collaboration among international research consortia (e.g., International

Sematech, IMEC, and Selete) is becoming more commonplace. Governments are often strong sponsors of these consortia. The model that seems to be emerging is one likened to the international space station where the collective knowledge and investment of several nations is the only practical means of addressing such daunting technical challenges.

The Roadmap has evolved from a vehicle that primarily targeted U.S. Government funding agencies to one that better serves the international semiconductor industry's needs. It is still used in policy discussions in the U.S. and presumably in other countries. For example, in a recent policy paper the SIA stated that increasing federal funding for fundamental research in the physical sciences and engineering was SIA's top public policy priority. Part of the rationale included the daunting challenges spelled out in the Roadmap (see Box 12-1).

Box 12-1. Public Policy Rationale Citing the Roadmap[1]

3. SCIENCE INVESTMENTS ARE REQUIRED TO CONTINUE MOORE'S LAW

Since 1992, the SIA has coordinated periodic meetings of U.S. semiconductor technology experts from industry, academia, and government to document technology requirements and possible solutions to maintain the industry's pace of quadrupling the number of transistors on a chip every three years. In 1999, this effort was expanded into a cooperative effort with semiconductor trade associations around the world. The resulting International Technology Roadmap for Semiconductors (ITRS) identifies research challenges in the areas of chip design, testing, lithography, interconnect, device structures, defect reduction, metrology, the environment, safety, and health.

In the short term, the ITRS notes that "the number and difficulty of the technical challenges continue to increase as technology moves forward," and that today there are no known solutions to many of the challenges we will face a mere five years from now. Moreover, even with the introduction of new materials to replace or augment existing ones, the planar CMOS process that has been the basis of the semiconductor industry for the last 30 years can only be expected to last for the next 5 to 10 years. With some refinements, this might be stretched out an additional 5 years. Consequently, the international technology experts concluded:

> "…as the ITRS looks at 10-15 years in the future, it becomes evident that most of the known technological capabilities will be approaching or have reached their limits. In order to provide the Computer, Communication, Consumer, and other electronics industries with continuously more efficient building blocks, it becomes necessary to investigate new devices that may provide a more cost-effective alternative to planar CMOS in this timeframe. Adequate preparation for this potential transition must include starting to identify the possible candidates as early as possible and, then, systematically testing their feasibility."

[1] Semiconductor Industry Association, "SIA Position on Federal Science: Increase Support of University Research," Rev 2.2, January 8, 2002, 6.

Looking forward from 2004 the Roadmap will continue to influence public policies as it has in the past. The exact nature and methods will adapt to fit the evolving needs of an industry involving governments of many nations. Given its success to date within the industry as suggested by John Kelly's opening quote, it is likely that the Roadmap will be used as a credible, common reference for *international* discussion of policy issues concerning technological innovation of semiconductors.

CHAPTER 13: Conclusions

"As the human mind becomes more developed, more enlightened, as new discoveries are made, new truths discovered and manners and opinions change, with the change of circumstances, institutions must advance also to keep pace with the times."

- Thomas Jefferson[1]

"All generalisations are dangerous, but without them the intellect is starved."

- Ernest Braun & Stuart Macdonald[2]

"It's a better bet to be optimistic about technology rather than pessimistic. History is on the side of the optimists."

- Dirk Bruere[3]

"For the next 10 years, there's a different crisis. It's no longer 'beat Japan', but to stay on the productivity curve."

- C. Mark Melliar-Smith[4]

Probably the most striking finding of this research was one not initially sought: the legacy of semiconductor roadmaps dates back at least into the 1970s and perhaps implicitly to the early days of the IC industry in the 1960s. This historical point is significant because the continued success of the Roadmap is attributable in large part to the formative roadmapping efforts that helped shape it (see Figure 13-1). Moreover, an increasing number of interrelated industry-level and firm-level roadmaps reach both horizontally across and vertically deeper into the semiconductor supply chain, thus broaden the web of roadmapping behavior and further

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[1] Thomas Jefferson, 1816; also inscribed in the wall of the Jefferson Memorial, Washington, DC.
[2] Ernest Braun & Stuart Macdonald, *Revolution in Miniature*, Cambridge: Cambridge University Press, 1982, 181.
[3] Dirk Bruere, newsgroup posting: From dirk@neopax.com, Subject: Re: Noise threatens Moore's Law, Newsgroups: sci.physics, Date: 2002-12-19 13:39:33 PST.
[4] C. Mark Melliar-Smith, quoted in Jeff Dorsch, "*Sematech*: and then there were nine," *Electronic News*, Vol. 44, Iss. 2227, July 13, 1998, 38.

reinforcing the importance of the "mother" Roadmap. In this sense the linear presentation of Figure 13-1 is insufficient.

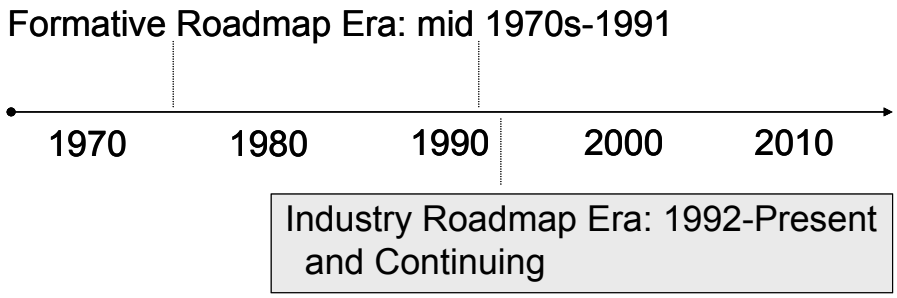

Figure 13-1. Evolution of Semiconductor Roadmaps

Retrospective

This dissertation began as an attempt to study Moore's Law. While unique, interesting and important, this topic soon proved difficult to research in a practical way. After repeated but unsuccessful attempts at making the topic researchable, my advisor finally suggested an examination of the Roadmap, in many ways Moore's Law *operationalized* or as Sonny Maynard referred to earlier as "heavily decorated." Indeed, when I first opened up *The National Technology Roadmap for Semiconductors*, I noted how thoroughly semiconductor technology was examined in a *forward-looking* fashion. This approach stood in contrast to many treatments of Moore's Law which were mostly historical curve-fitting exercises with some simple future extrapolations. On the other hand, the Roadmap's purpose of anticipating, and deliberately sustaining or even perpetuating Moore's Law carried with it profound strategy and policy implications and thus seemed a much more appropriate topic to study. One early informant musingly referred to the Roadmap as Moore's Law "insurance." That interpretation stuck.

My idea was to study this technology "road map" to better understand its role in a broader innovation context. Like any research the path to discovery is rarely straight, however the

Roadmap seemed to run counter to this view. What became apparent upon examining preceding Roadmaps is that there did not appear to be a great deal of difference among the documents. However, upon closer examination small changes were noticed, which begged questions that could not be answered by simply looking at Roadmaps. It became evident that studying the Roadmap meant much more than reviewing publications—these were outcomes of a methodical *roadmapping process* that typically involved a wide range of knowledge, skills, and interests. Roadmapping is a social process applied, in this particular case, to a technological challenge: how to advance semiconductor technology, and do so continuously. The economic benefits from such an effort, whether accrued to a single firm or entire industry, were clear and compelling.

With the Roadmap (not just the document but the process behind it) as the unit of analysis this dissertation covered a broad theoretical base in economics, sociology, and public policy. Numerous studies, reports, books, articles, and other publications covering the semiconductor industry informed the research on all these fronts. A more focused review of the innovation studies literature within the framework of complexity science and especially evolutionary theory provided the conceptual basis. Specialized topics in the areas of technical and engineering knowledge, network and organizational learning, collaboration, industrial organization, and strategic behavior along with contemporary practices in research consortia, technology assessment and forecasting, and management of technology were also surveyed. An academic interest in the phenomenon of Moore's Law along with a former technical background in the computer industry helped translate curiosity into meaningful inquiry. An historical bent ensured that loose ends were carefully tied while context was purposely considered. The richness of the primary data on everything from simple facts to deep insights obtained in interviews of several dozen semiconductor industry representatives afforded the benefit of a more complete understanding and articulation of findings. Finally, a penchant for detail, completeness, and rigor guided a thorough treatment of all data sources.

The net result of all these research considerations is the capacity to now look at a particular figure, table, or statement in the ITRS and perhaps not understand its technical merits, but appreciate and articulate how it was arrived at, how it will be used, and its overall significance to semiconductor innovation, strategy, and policy.

As with any research more questions are produced than answers. These questions are for future study. For now, the answers to the initial research questions are addressed.

The Research Question

How have technology roadmaps affected innovation, strategy, and policy in the semiconductor industry?

Roadmaps and Innovation

I have argued that technological innovation in semiconductors follows a normal innovation pattern. By itself, this is not a new finding. However what has been demonstrated is that evolutionary change best describes the vast majority of semiconductor innovations including the microprocessor, considered by most conventional accounts as a revolutionary change. At a different level, advances in lithography, historically the most critical chip fabrication tool, have followed a very distinct normal pattern. As attempts have been made to introduce revolutionary methods (e.g., x-ray), incremental advancements in optical methods have stretched its utilization far beyond forecasted limits. Even EUV lithography, the industry's apparent current choice of next-generation lithography, is an extension of the present DUV (optical exposure) technology.

Underneath this pattern is a roadmap, whether explicit or implicit, that has predetermined the path of innovation. What makes these roadmaps credible is the collective, accumulated knowledge captured within them. This is most evident in the case of the ITRS due to its public nature. But in earlier pre-Roadmap times the innovation network shared this understanding in large part through the unique scaling properties of IC technology. Moore's Law has become

legacy because the industry has made it so through day-in, day-out engineering practice that continues to expand technical knowledge and thus capability at an exponential rate.

Without initially intending, industrial innovation has increasingly become *organized*—actually *self-organized*—because designing and building semiconductors is very complex and requires considerable coordination and alignment of a wide variety of elements. Thus, organized innovation has benefited greatly from a roadmap. As collective knowledge is made more explicit and codified in ever finer detail in an *International* Roadmap, this awareness allows the innovation network to, in turn, affect the nature and pace of innovation as has become so evident in the SIA Roadmap era. This give-and-take process ensures the primary purpose of the Roadmap: to perpetuate Moore's Law.

Therefore, roadmaps and innovation in semiconductors have become almost inseparable.

Roadmaps and Strategy

The semiconductor industry is unique in many ways, not the least of which is in the sheer diversity of organizations that make it up, whether large or small, private or public, chip maker, tool maker, OEM, materials provider, research consortium, etc. In contrast with the common properties of the technology, very disparate organizations participate in such a way that benefits each while assisting the broader interest. At a top level, "beating the Roadmap" is akin to Adam Smith's *invisible hand* of competition theory of market forces. This helps explain the evolutionary nature of roadmapping from firm to industry to national to international levels.

At a lower level it has been demonstrated how roadmaps can be used to gain competitive advantage. In some organizations the roadmap is the strategy, or at least a large part of it.

In the area of research, one unique factor of this industry is the noticeable 15yr outlook (i.e., research and development time line) that distinguishes research responsibilities among members of the innovation network, from semiconductor equipment supplier to university researcher. Throughout the semiconductor infrastructure exists a roadmapping mentality,

(i.e., "it's on somebody's roadmap"). This is the broader impact of the Roadmap; it really does foster a broad-based, coordinated strategy.

Roadmaps and Policy

Policy, especially public policy, is about crafting and instituting some action that corrects, remedies, or otherwise improves a situation that needs attention. The relationship between roadmaps and policy has varied considerably over time as the situation has changed. Initially a byproduct of policy the Roadmap became an instrument for policy, and has since become an activity almost in *lieu* of policy. Of the three attributes, policy is probably the one least influenced by the Roadmap at the present. This is evident in the reduced levels of Roadmap participation by Government representatives as shown in Figure 13-2.

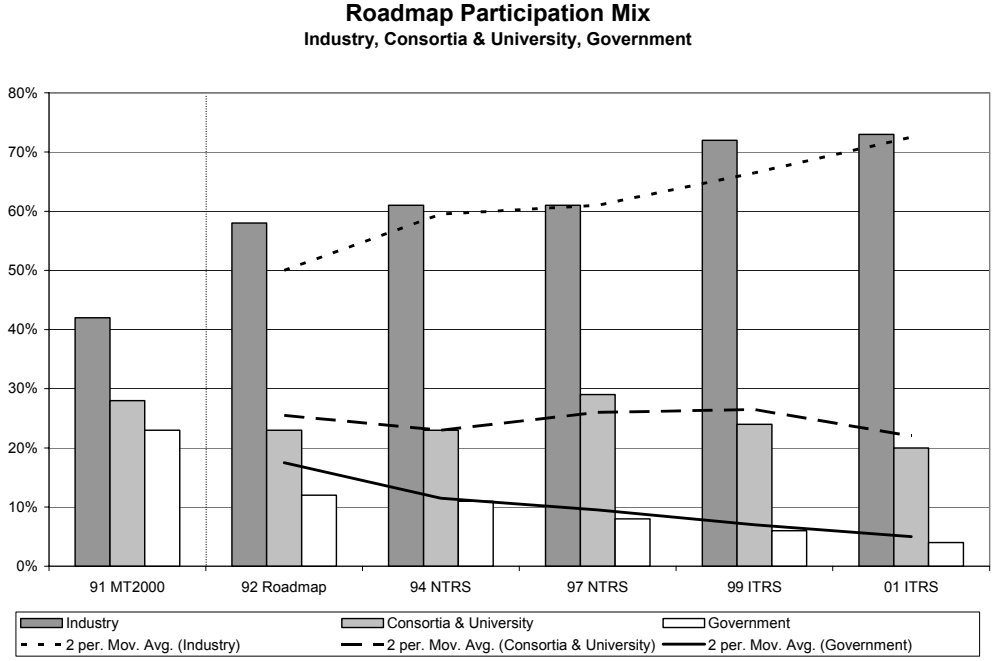

Figure 13-2. Roadmap Participation Mix by Industry, Consortia & University, and Government[5]

Source: SIA Roadmaps, Sematech Archives

[5] Note that data for the 2003 ITRS did not distinguish Government as a single category but was combined into a single category of Consortia, Research Institutes, and Universities which totals 20%. Total industry participation for 2003 increased to 78%.

One particular policy lesson is in the area of research. The U.S. Government has traditionally supported advanced applied research in technologies deemed as replacement technologies. Major examples include non-silicon substrate materials and non-optical lithography. In the vast majority of cases these programs were not successful because they were incompatible with the needs of industry. It has only been recently when industry has essentially chosen the research topic (increasingly from the Roadmap) that Government support has been more useful. Examples include EUV lithography and the MARCO Focus Center Research Program.

Thus both strategic and policy-oriented decisions are best made on the Roadmap or on technologies that do not veer too far from it.

Other Conclusions and Observations

Studying the Roadmap in the context of a broader industry analysis leaves one with many impressions. A couple of points are noteworthy. The first is the very noticeable technology acceleration or "beat the Roadmap" behavior. This suggests strongly that non-technical factors are at play and offer a fertile area for future research. The second is the relatively easy, almost natural flow of roadmapping to increasingly higher levels of participation and use. Another is the ready acceptance and credibility of the Roadmap. Yet another is the all-volunteer nature of Roadmap participation. Since these particular points have already been addressed elsewhere in the thesis, the following paragraphs offer comments on other aspects of the Roadmap that may not have been addressed previously.

Assessing the first SIA Roadmap

Having had the opportunity to examine the 1992 Roadmap over the span of its initial projection (through 0.10 um) allows a researcher to assess it in many ways. Technically, the 1992 Roadmap out-year technology node was achieved in 2003, four years ahead of forecast, as discussed in Chapter 10. So was it successful or not? Secondly, the future has not unfolded as it

was supposed to. For example, we do not have 16G DRAMs and die sizes are not monster 1000 mm^2 as the 1992 Roadmap projected. At the same time, device feature sizes are actually smaller than anticipated and on-chip performance far exceeds 1GHz. Again, what does this say about the Roadmap? As discussed in Chapter 2 forecast accuracy is *not* the only—and perhaps only a minor—success measure for a roadmap. One major factor that contributed to these deviations is that other technology drivers have emerged that required different capabilities than the narrow DRAM and logic/microprocessor assumptions used in the first Roadmap. What seems more important is that successive Roadmaps adjusted for the variances to reflect the best collective judgment at the time. But each required adjustment upon renewal, sometimes major change. Thus is the iterative nature of the roadmapping process: a continual reassessment that becomes obsolete as soon as it is published. Perhaps the best example of this (that also predates industry roadmaps) is the projected end of optical lithography. Yes, the industry still uses optical lithography, and plans to continue for the foreseeable future.

Why is the Roadmap successful?

If forecast accuracy is not the proper success metric, then what is? And what explains this success? This research uncovered a wide variety of success measures. While these have been discussed at various points in this dissertation, the following general proposition is offered.

The Roadmap is "successful" because it is still going, six editions later.

Tens of thousands of hardcopy Roadmaps have been purchased while the public website records more than 5,000 visits per day. Total participation is approaching 1,000 and now consists of more non-U.S. participants than U.S. participants. Users include chip makers, tool makers, materials suppliers, OEMs and other customers, researchers, faculty, government agencies, investors, etc. Iteration (or renewal) is now an annual event. But how long can this continue? Gordon Moore himself suspects that the Roadmap and even Sematech might "peter out" after a

while. His experience is that things like this usually last no more than a decade.[6] For now, though, the Roadmap shows no immediate sign of petering out.

If anything it continues to grow in size, scope, and complexity. The 2003 ITRS is almost 650 pages, single-space, 10pt font, and loaded with more than 200 intricate figures and tables. In comparison the 1992 Roadmap (Workshop Working Group Reports) was 154 pages.[7] Yet, as pointed out in Chapter 10, the first and most recent "bookend" Roadmaps share much in common in large part because the underpinning need has not changed. One informant provides an historical perspective to make this point evident while adding a bit of levity:

> "Today's industry is fragmented, vertically disintegrated, etc., but the "whole thing" hasn't changed much. It's just divided differently on the inside. The same level of R&D needs to go on with equipment suppliers, formerly device makers, in process development. Remember that the Roadmap was always to provide a tool to guide *research*, to identify gaps… thus a "roadmap" to identify needs. The Roadmap has expanded in character over time, but it's still the same issue. The first Roadmap looks very much like the current Roadmap. We're now down to nuances—in ITWG workshops we're arguing over the definition of dimensions (i.e., gate length, half-pitch, etc) or semantics. The discussion is almost, 'How many angels can dance on the head of a pin?' "

The last comment, though facetious, does capture the delicate balance the Roadmap attempts to strike between the forest and trees of research in semiconductor technology. Returning to the original question, exactly *why* the Roadmap is successful has many possible answers. One certainly is the unique scaling nature of the technology and the normal innovation pattern that seems to coincide with it. The existence of "Moore's Law" is a short-hand way of describing this. Another factor is that the Roadmap has been rationalized by industry, not government, academia, or other institution that lacks a market incentive. At the same time, the role of research consortia such as the SRC and especially Sematech in providing the model for industry collaboration has been of critical importance. Additionally, the evolutionary nature of the Roadmap correlates with the industry's evolution. For example, the disintegration, specialization, and globalization of industry necessitate a common reference, which the Roadmap seems to

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[6] Gordon Moore, telephone interview, February 11, 2002.
[7] A second 60pg volume (Workshop Conclusions) summarized the Workshop Reports for a non-technical audience.

provide. This is especially true between device makers and tool and materials suppliers as hinted in the caption above.

Related to this and perhaps the most important reason that the Roadmap continues to be useful and credible is because it is a continual process that must evolve along with the industry. It has become an almanac, an atlas (i.e., collection of maps), a compendium that is reviewed, assessed, and updated (i.e., made current) on a regular basis. At the same time, it changes as needs change. “Renewal” is a very appropriate term. The ITRS has become an ongoing process. Like cartography (i.e., the art of map-making), successive Roadmaps have become more granular. Similarly, the author has noted that a *Rand-McNally Road Atlas* states as its purpose, "keeping the *Road Atlas* up-to-date is job #1." Below is a brief passage from the document that aptly parallels the work embodied in the renewal process of the semiconductor industry Roadmap:

> Every year there are thousands of changes, updates, and additions to the Rand McNally *Road Atlas*. And they have real impact. For example, roads are built, interchanges are constructed, and highways and byways are newly named and numbered. The importance of these changes lies in knowing that you'll reach your destination as planned.[8]

Along with increased granularity, the Roadmap has simultaneously become broader in scope (e.g., international, addressing different devices/drivers, even new status categories like “interim solutions exist”).

The pull-in or technology acceleration is a broader bias reflected in the Roadmap over time. The Roadmap served initially as a research instrument to see what was possible down the road. Thus it was not that concerned with the current state-of-the-art. If anything, the purpose of an early research roadmap like Micro Tech 2000 was to deliberately *change* or disrupt the current state. As such, this was (per Chapter 2) a *requirements-pull prospective* roadmapping approach (i.e., start with a future goal like a 1G SRAM and work backwards). The newer emphasis—starting actually at Sematech—is to fully understand the current state and how to project it

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[8] Preface, *Rand McNally Road Atlas: 2000 Millennium Atlas*, A1, 2000.

forward (i.e., a *technology-push prospective* roadmapping approach). As Government research interest in the Roadmap began to wane in the 1994 and particularly 1997 Roadmaps, the supplier community became a much more significant user which started a shortened view of research. The 1997 Roadmap reflected 2yr technology nodes through N+3 and by 1999 the Roadmap went to two timings: near-term (annual for next 6 yrs) and long-term (last 3 generations over 9 yrs). Most recently (2003), the inclusion of *interim solutions known* status color formally acknowledges a form of "temporary research."

The combined effect of these adjustments is a collapsing research horizon. In other words the Roadmap is now noticeably biased to the front-end. Similarly, the goal-driven roadmapping process runs the risk of path dependency, potentially missing important technological opportunities. While the Roadmap fosters organized innovation, the opportunity cost of roadmapping is some degree of curiosity-driven inventiveness. The very framework that brings about consensus and collaboration is also delimiting of nonconforming views. The extent of this consequence deserves greater attention.

Finally, the Roadmap is but a piece of a larger puzzle that is the uniqueness of the semiconductor industry. All the other pieces or elements (e.g., Moore's Law, industry consortia, standards, etc.) are required to complete the industrial pattern. While the Roadmap works well for the semiconductor industry, it would not necessarily fit within other sectors with distinct needs. Thus the Roadmap, by itself, is not replicable. This finding is consistent with other assessments of industry roadmaps:

> …*there is no one best way* to define the optimal level at which to carry out [technology roadmapping]… Hence a general definition of the best application level cannot—and *should not*—be given. Technology Road Mapping is typically needs-oriented and the definition of the level to which it should apply depends on the specific needs defined by those who participate in the exercise.[9]

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[9] Bastiaan de Laat and Shonie McKibbin (Technopolis), "The Effectiveness of Technology Road Mapping: Building a strategic vision," a study for the Dutch Ministry of Economic Affairs, est. 2002, 7, emphasis in original.

In sum, the Roadmap is "successful" as evident by the hundreds of people who volunteer their time and energy routinely. As one respondent stated:

> "We have learned very simply that if you provide your customer with more capability for the same dollar, year after year, then you'll be able to grow your markets. That's a real simple idea - that's what we've done. Each year we give you more for the same amount of money - more functionality, etc. We do this exponentially - we've been able to do this for two decades now. That's what Moore's Law says: well, surprise, surprise, it really works. And so this industry is *determined* to keep doing that - it sees that as a way of success, growth. My opinion is that we will find a way to push the Roadmap - I'm guessing - at least the CMOS era - maybe ten or fifteen more years."

Prospective

While many questions were addressed in this dissertation, several important questions remain. What is the future role of the Roadmap, especially as the industry approaches the limits of CMOS technology and possibly industrial maturity? What changes must be made to prepare the Roadmap for the second decade of practice? For example, how much longer will a single Roadmap be able to sustain the weight of so many constituents? Should it be broken up into more manageable “volumes” (i.e., more like an atlas) by device type, thrust area, etc.? One respondent offered the idea of two Roadmaps to serve distinct audiences: 1) for suppliers yrs 1-6, 2) for research yrs 6-15. As inter-consortia (and inter-industry) collaboration increases, will the Roadmap become even more important as the common denominator for discussion and debate?

Finally, asked about the future role of Roadmap, respondents consistently viewed it as an important institution within the global semiconductor innovation community. The industry plans to continue Roadmap activity, essentially now a continuous process. When Juri Matisoo, SIA VP of Technology Programs was asked the question, "do you see a time when a roadmap is no longer needed?" he replied by rephrasing the question: "will there be a time when collective research in semiconductor technology will not be required?" His answer: "I don't think so."[10]

In a recent special issue of *Business Week* that examines the changing U.S. position in world science and technology leadership, the authors conclude, "History's powerful lesson: When it

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[10] Juri Matisoo, telephone interview, August 10, 2000.

comes to a nation as a whole, the best system to foster innovation is disorganized and chaotic."[11] The rationale for this statement is that "no central authority in government or industry should decide what the future ought to hold," as entrepreneurial spirit within a market system has proven a better driver of innovation.

In the same issue is an interview with Craig Mundie, chief technologist at Microsoft. Mundie describes innovation more fully as a "symbiotic cycle" that needed balanced attention:

> You have to think of this [innovation] as a symbiotic cycle in which the government funds research and trains people, and businesses create the opportunity for these people to turn their ideas into products. Our great concern is that if you don't pay careful attention to each element of the cycle, you end up with a broken machine.[12]

The concern Mundie is referring to is the diminished investment in fundamental, long-term research that has occurred since the end of the Cold War. This claim has been raised often.

For its part, the semiconductor industry has chosen a much more *organized system of innovation*—greatly assisted by the Roadmap—that seems more aligned with Mundie's symbiotic view than the preceding disorganized and chaotic view. To date it has proven successful for the key reason suggested by Jefferson in the opening quote of this chapter: the Roadmap as an institution has evolved alongside the industry it reflects and supports.

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[11] John Carey, Otis Port, and Adam Aston, "America's Enduring Tech Edge," *Business Week Online* (Special Report: America's Tech Might: Slipping?), March 16, 2004, http://www.businessweek.com/technology/content/mar2004/tc20040316_2875_tc166.htm

[12] Craig Mundie, quoted in Alex Salkever, "Innovation Is a "'Symbiotic Cycle'," *Business Week Online* (Special Report: America's Tech Might: Slipping?), March 16, 2004, http://www.businessweek.com/technology/content/mar2004/tc20040316_9616_tc166.htm

APPENDICES

A. Research Agreement, Interview List, Survey, etc.

B. Detailed Findings

C. Moore's Law Retrospective

D. Chapter Appendices

Appendix A: Sematech Research Arrangement

This appendix includes two documents prepared for Sematech at the outset of this research in September 1998. Since these were not proposals *per se*, there was no official approval sought or obtained. Instead, these served to frame the research in a manner that was acceptable to Sematech and its membership. The research has generally proceeded within the guidelines established herein.

Draft Scope Statement

The National Technology Roadmap for Semiconductors:

A Comprehensive Study of its Past, Present, and Future

for

Linda Wilson, Research Project Coordinator, SEMATECH

by

Robert R. Schaller, Ph.D. Student, The Institute of Public Policy, George Mason University

with oversight by

Don E. Kash, Hazel Chair, The Institute of Public Policy, George Mason University

September 1, 1998

Overview: The National Technology Roadmap for Semiconductors, now in its third edition (December 1997), has been referred to as a "model" for industry-wide strategic planning. It has succeeded in establishing a set of technological innovation targets through a consensus process that is unique among other industries and sectors. This consensus process is presently being expanded to include international participation in the next and future rounds of the roadmap process. Given the roadmap's success and expanded scope, there is good reason to more closely examine the roadmap process and offer insight into its future prospects and challenges. Specific goals of this study will include:

1. Articulate the "story" of the roadmap process from its genesis, through its three publications, to its current status. Essentially, document its history and in the process, explain to roadmap participants, member companies, policy makers, industry strategists, and other users the context within which the roadmap was created, developed, and is currently evolving.
2. Assess the roadmap's success, influence, and impact to date. Critically examine the strengths and weaknesses of the roadmap process through participation in the next process round and a detailed "lessons learned" review. Determine what measurements are most appropriate in determining roadmap "success."
3. Recommend improvements and other changes to the process for future update rounds. Consistent with the practice of continuous process improvement, this goal will help roadmap participants contribute in a more efficacious manner.
4. Speculate on the roadmap's long-term role in semiconductor technological innovation, especially as the process is expanded to a global scope. This includes examining semiconductor research and development efforts at various levels: industry, government, and

universities, and at the national and (soon) international levels.

5. Woven throughout the study is an interest in public policy implications. SEMATECH, and thus the roadmap, have experienced changes over time in public support (e.g., reduction and eventual elimination of government funding). Does this continue to make sense in light of international participation? What is the proper role of public policy in the roadmap process, SEMATECH, and other technologies' research consortia more broadly? Finally, how does the roadmap itself affect policy (e.g., the roadmap's boundary setting process)?

Areas of Inquiry: The idea/phenomenon of industry- or sector-wide roadmaps appears to be relatively new. There is a growing body of literature that suggests that this may be in response to the increasing complexity of technologies, and in particular to the accelerating speed to innovate (e.g., Moore's Law). Seemingly, roadmaps help tie together industry R&D resources to keep up the rapid pace of innovation. At the same time, the consensus-building process brings a disparate group of organizations together, with distinctly different corporate cultures, and now will expand to include international participation in the next round.

There are significant public policy questions and issues to be examined. For example, in another time, roadmap activities may have been perceived as collusive -- what has changed to increase the amount and type of collaboration among producers, suppliers, customers, universities, government agencies, international participants, etc.?

The nature of knowledge creation and dissemination is also of great interest. Do participating organizations -- some competitors -- share knowledge freely, and at what stages (e.g., precompetitive)? Is the knowledge tacit or explicit? Does the roadmap itself serve to convert tacit to explicit knowledge? In the process, does this inform public policy, which operates best with explicit knowledge? Have industry-wide routines/heuristics been created in the process? Is the roadmap a "logical step" in the complex evolution of technologies and innovating organizations? What are the implications for self-organization, path dependence, lock-in, etc.

Additional interest stems from the researcher's curiosity with "Moore's Law," the regular, density-doubling phenomenon that has occurred in semiconductors over the past four decades. Moore's Law is one of the chief planning assumptions in the semiconductor technology roadmap. Collectively, Moore's Law and the roadmap serve to guide, coordinate, and influence industry and firm innovation strategies, resource allocations, as well as related public policies.

The study will also evaluate the roadmap's influence in coordinating and directing industry innovation strategy and resource allocation.

Research Methodology: This will be an historical case study of the semiconductor roadmap development process inquiring into the following list of starting questions:

- what was its genesis?
- how did it evolve?
- what factors/variables influenced it?
- what was the process and structure used, how was it arrived at?
- what were the various organizations' roles in the process?
- what was/is/will be SEMATECH's role? (steward?)
- what were the links to public policy?, etc.
- how/why is semiconductor technology qualitatively different in regards to a roadmap?
- why is this particular roadmap repeatedly cited as the model?

- what role does Moore's Law play in the process?

Research will begin with a detailed literature review of all related information that has been published about the roadmap process by SEMATECH, SIA, SRC, member companies, universities, government agencies, scholars, and journalists. This can be accomplished remotely by the researcher for the most part -- access to archival data will be required.

Once the literature review is completed, a series of personal interviews of key roadmap personnel will be conducted by the researcher for validation purposes and to gain additional insight into the roadmap's historical evolution. The list of interviewees will include past and present members of the Roadmap Coordinating Group, Technology Working Groups, and others as determined by the project coordinator. Interviews will require travel by the researcher, however phone interviews and electronic correspondence will be used as much as possible to minimize travel costs.

Another research method can include administration of a survey instrument to a much broader audience (e.g., member companies, universities, other users) to assess success, effectiveness, and "lessons learned" from the roadmap process. This is an opportunity to cast a wide assessment net to help in future rounds of the process. If feasible, survey links to SEMATECH's, SIA's, and SRC's web sites can be set up for casual user inquiry (e.g., are you aware of the roadmap?, do you use it?, in what ways?, etc.).

Coincidental with these efforts, the researcher will attempt to attend and be part of the next roadmap update process as a guest of the project coordinator. This will provide timely and valuable insight into the process -- for the first to include international participants which is expected to yield significant changes.

Finally, a report (or series of reports) will be published documenting research findings and recommendations. Parts of this report will be used in the researcher's PhD dissertation on technology policy. Additionally, this research can serve as the basis for other possible needs by the project coordinator, including the publication of a piece (book) for wider consumption by an audience interested in this unique consensus-building process.

Project Timeframes & Milestones: [Initial estimates were revised significantly.]

DRAFT

The National Technology Roadmap for Semiconductors:

A Closer Look at the Process

Topical Outline

Bob Schaller

September 18, 1998

Background: The National Technology Roadmap for Semiconductors, now in its third edition (December 1997), has been referred to as a contemporary model of consensus forging on industry-wide R&D and other strategic planning needs. The Roadmap is the culmination of a collaborative 18-month process involving more than 300 scientists from industry, government, and universities. Collectively, these participants have succeeded in establishing a set of technological innovation targets that will extend the historical pace of technological change according to Moore's Law through the year 2012. In sum, the Roadmap is an articulated vision of the near future of technological innovation in semiconductors. Equipped with such a tool, the industry has a clearer picture of where it is headed and can work in concert in bringing about this vision.

The very notion of a Technology Roadmap seems novel at first examination. Competitors in a fiercely competitive and dynamic industry actually working together to advance the technology for their mutual benefit? In another time this kind of activity was not just novel, but illegal. But within a pre-competitive environment the Roadmap process seemingly works well. Some of the key research questions to be asked are "What is unique or different about the Roadmap process; is it really that much different than other forms of collaborative processes involved in bringing about technological change?" Very simply, "Is this a model?"

The literature on technological change is filled with historical examples of technologies exhibiting lawlike patterns of change similar to Moore's Law in semiconductors. Much attention has been paid to both internal factors (i.e., unique characteristics of the technology itself), and external factors (e.g., economic forces such as market demand) that have contributed to these patterns. More recently, it has been argued that the role of collaborative technological networks and communities are also important contributing factors in perpetuating almost predictable patterns of technological change. This is evidenced in numerous cases varying from farm implements to consumer electronics to aerospace.

The Semiconductor Technology Roadmap process involves a broad technological network. Thus, collaboration in the Roadmap process is not new. Yet the structure and methods employed (e.g., pre-competitive basis, broad participant network, process -- not product -- emphasis) are clearly unique. The very metaphor "Roadmap" (one word) has yet to appear in the dictionary.

A closer examination of the Roadmap process as it affects technological change has not been conducted to date -- this is the purpose of this study. This investigation will study the creation and evolution of the Semiconductor Technology Roadmap process from its genesis, through its three publications, to its current status. It will also look at spin-off or parallel Technology Roadmap efforts (e.g., NEMI Roadmap) along with "pre-Roadmap" collaborative activities used in the development of aerospace technology in an attempt to find patterns of similarity or difference. From this examination we may better understand the factors that help make the Semiconductor Technology Roadmap successful (or not) in advancing technological change.

Brief Outline of Study:

1. Historical account of Semiconductor Technology Roadmap
    a. What was the genesis?
    b. Role of SIA, SRC, SEMATECH, other key players
    c. Chronological timeline of events
2. Review of spin-off or parallel Technology Roadmaps
    a. National Electronics Manufacturing Initiative (NEMI) Roadmap
    b. Steel, Aluminum, other industries employing Technology Roadmaps
3. Parallels in aerospace and other communities
    a. Fuselage, engine, and materials advance in aerospace
    b. Possibly other technologies (to be determined)
4. Roadmap process defined
    a. Key ingredients (structure, rules, etc.)
    b. Membership (industry, universities, government)
5. What's new and what's not

   a. Role of collaboration
   b. Importance of pre-competitive basis
6. Conclusions and future research
   a. Is this Roadmap a model?
   b. What does this inform us of future uses of Roadmaps?

Appendix: Personal Interview List

Moore's Law (1996-7):

Erich Bloch

Gordon Moore

Carver Mead

Gordon Bell

Steve Kline

Dan Lynch

Other:

Melissa Appleyard, U of Virginia Darden Business School

Roadmapping Process:

Dudley Caswell

Rich Albright

Tom Kappel

Bob Zurcher

Ron Kostoff

Pieter Groenveld

Rob Phaal

Jim Richey

SIA Roadmap, also other industry and company roadmaps:

Allen (twice)	Alan	Staff Marketing Engineer	Intel; ITRS Overall Characteristics Table
Armstrong	John	IBM S&T VP (retired), former NACS member	
Asher	Irwin	NEMI	
Bennett	Herb	NIST (Compound Semiconductors)	
Bird	Mark	Director	Technical Marketing, Amkor Technology
Bloch	Erich	IBM (retired), former head of NSF	
Bloom	Floyd	Scripps Research Institute	

Bohr	Mark	Intel	
Bracken	Ron	SRC Director	Packaging Sciences
Brown	Karen	Deputy Director	NIST; former IBM and Sematech assignee; former domestic TWG Chair, Lithography
Browning	Larry	U Texas	
Broydo	Sam	Managing Director Special Projects	Applied Material
Brueck	Steve	U of New Mexico	
Burger	Bob	former VP/Chief Scientist	SRC (retired)
Carruthers	John	Director	Intel Components Research
Cavin	Ralph	SRC VP	Research Operations
Chang (twice)	Chi Shih	Sematech Senior Fellow	
Class	Walter	Strategic Marketing Director	Eaton SEO
Colwell	Bob	Independent consultant	former Intel IA-32 Architecture Director
Daughton	Jim	Honeywell (retired)	
Davis	Ken	Motorola	
Derbyshire	Katherine	Industry Analyst	
Diebold	Alain	Sematech Senior Fellow	Domestic TWG Chair, Metrology
Doering	Bob	TI Senior Fellow; RCG Co-chair	
Feinstein	Leo	NEMI	
Fisher	Jack	ITRI	
Fukushima	Toshitaka	Fujitsu	
Galvin	Bob	Chairman	Motorola
Gargini	Paolo	Intel Fellow; RCG Co-chair	
Glaze	Jim	Executive Director	Virtual National Lab, former SIA VP Technology
Greed	Jim	Foothill Technology (for SEMI)	
Hagglund	Neil	Motorola	
Harrell	Sam	Sematech	KLA-Tencor, former SEMI/Sematech
Hasty (twice)	Turner	TI	Sematech (retired)
Herr	Dan	SRC Director	Materials and Process Sciences

Howard	Bill	consultant	former Motorola Sr. Engineering Manager (retired)
Hu	Genda	TSIA	
Hutchby	Jim	SRC Director	Nanostructures and Integration Sciences
Hutcheson	Dan	President	VLSI Research
Isaac	Randy	IBM	VP
Jackson	John	SEMI	
Joyner	Bill	SRC Director	Computer Aided Design and Test
Kahng	Andrew	UC San Diego	ITWG Design Chair
Kleiman	Herb	President Kleiman Assoc.	
Klingenstein	Werner	Infineon	
Knight	Colin	AMD (retired)	
Leckie	Ron	CEO, Infrastructure	completed survey only
Lind	Ted	Motorola (retired)	
Mack	Chris	KLA-Tencor	VP, FINLE Division
Matisoo	Juri	SIA	VP Technology
Maynard	Sonny	SRC Executive VP	Government Affairs
Meindl	Jim	Professor and Director	Microelectronics Research Center, Georgia Institute of Technology
Moore (twice)	Gordon	Intel co-founder and Chairman Emeritus	
Ning	Tak	IBM Fellow	
Novak	Larry	VP Electronics/Semiconductors	Radian; former TI; Domestic TWG Chair, Environment, Safety & Health (ESH)
Oberai	Obi	IBM	Sematech assignee (retired)
Orchansky	Michael	esilicon.com	
Peercy	Paul	former President	SEMI/Sematech
Reader	Alec	Philips	
Rubin	Leonard	Sr. Scientist	Eaton SEO (completed survey only)
Scace	Bob	President	Klaros; former NIST Metrology (retired)
Seidel	Tom	Executive VP and Chief Technology Officer	Genus; former RCG member

Schulz	Steve	Sr. Member Technical Staff	Texas Instruments; Domestic TWG Chair, Design
Skinner (twice)	Court	SRC; former National Semiconductor	
Spencer	Bill	Chairman and former CEO	Sematech
Tasch	Al	Professor and Sr. Research Scientist	University of Texas, JJ Pickle Research Center
Tracy	Dan	Research Associate	Rose Associates
Vojak	Bruce	former Motorola	
Wadsworth	Duane	SEMI Board member	
Weber	Werner	Infineon	
Weisberg	Len	former OSD	
Werner	Bob	Director of Advanced Technology	Sematech; Domestic TWG Chair, Assembly & Packaging
Williams	Owen	former Motorola Sr. Engineering Manager; former RCG Chairman (retired)	
Wilson (several)	Linda	ITRS Information Manager	
Wolleson	Don	Director	AMD Technology & Reliability Engineering
Yu	Hwa-Nien	IBM Research (retired)	

Appendix: Roadmap Participant Surveys

Personal Interview Instrument

International Technology Roadmap for Semiconductors (ITRS)

Personal Interview Questions for International Representatives

Introduction:

A joint project between George Mason University and SEMATECH is underway to examine the Semiconductor Technology Roadmap process. The objective is to understand success factors and perceived historical value to the semiconductor industry. It is acknowledged world-wide that the Semiconductor Industry Association (SIA) Semiconductor Technology Roadmap process is successful. Generalities can be made based on the process to better understand roadmaps with respect to technological innovation strategies and policies.

The results of this project will be incorporated into a Roadmap Primer for use across industries as a compilation of best practices. Additionally, key findings will be included in a Ph.D. dissertation examining this process as a case study of the broader field of technology roadmapping (see http://mason.gmu.edu/~rschalle/rdmprop.html for more information).

Your input as a participant in the SIA Semiconductor Technology Roadmap process or as a Semiconductor Technology Roadmap customer is valuable in this study. The following questions are intended to obtain data on the effectiveness, success factors, and value-added of the Semiconductor Technology Roadmap process. Your own perspectives and general comments will be sought as well. Results of this research will be available upon request.

Please note that the following list of questions is extensive, but not all questions will necessarily be asked. The list serves as a guide for the interviewer and questioning will be tailored when and where possible.

Research Team:

Bob Schaller	Linda S. Wilson
Ph.D. Candidate	ITRS Information Manager
George Mason University	SEMATECH
301/475-2068	512/356-3605
schaller@uzoom.net	linda.wilson@sematech.org

Person Interviewed:

Name: _____ Title:_____

Organization: _____ Date, Time: _____

Interview (circle one): in-person, phone, or e-mail

Involvement in SIA Semiconductor Technology Roadmap:

1. Have you been involved in the Semiconductor Technology Roadmap? _____
2. If yes, how many years? _____ (if no, skip participation questions 3-8, 19-21)
3. Please indicate the extent of your past roadmap involvement (check all that apply)
   - ☐ 2001 SIA International Technology Roadmap for Semiconductors (ITRS)
   - ☐ 2000 Update
   - ☐ 1999 SIA ITRS
   - ☐ 1998 Update
   - ☐ 1997 SIA National Technology Roadmap for Semiconductors (NTRS)
   - ☐ previous SIA Roadmaps (1994, 1992)
   - ☐ earlier (e.g., National Advisory Council MicroTech 2000)
   - ☐ other technology roadmaps
4. How would you rate your involvement?
   - ☐ Very active
   - ☐ Active
   - ☐ Interested
   - ☐ Somewhat interested
5. What is (was) your role in the Semiconductor Technology Roadmap process?
   - ☐ Conference Participant
   - ☐ Technology Working Group (TWG) member
   - ☐ USA Roadmap Coordinating Group (RCG) member
   - ☐ International Roadmap Committee (IRC) member
   - ☐ Other: specify _____
6. If you are (were) a TWG, RCG, or IRC member, estimate the percentage of your time spent on the SIA Semiconductor Technology Roadmap activities outside of the formal workshops and conferences? _____%
7. How and why did you become involved in the Semiconductor Technology Roadmap?
   - ☐ Requested directly from SIA to serve on a TWG, RCG, or IRC
   - ☐ Appointed by your management
   - ☐ Volunteered based on personal or professional interest

8. Why do you attend the formal Semiconductor Technology Roadmap workshops and conferences?
   - ☐ Company/industry analysis Early insight of industry trends
   - ☐ Technical interest
   - ☐ Collaborate with colleagues
   - ☐ Other: specify _____

Assessment of process and benefits:

Please indicate the degree to which you agree with each statement by circling the appropriate number as follows.

N	1	2	3	4	5	6	7
Not Applicable	Strongly Disagree	Disagree	Somewhat Disagree	No Opinion	Somewhat Agree	Agree	Strongly Agree

9. The Roadmap process **meets my expectations**. N 1 2 3 4 5 6 7

10. The Roadmap process **allows me to influence industry direction**. N 1 2 3 4 5 6 7

11. The Semiconductor Technology Roadmap **workshops, conferences, and TWG meetings are a good way to communicate** technology needs and work key issues. N 1 2 3 4 5 6 7

12. The Roadmap's **key value is**: (rate each on scale and rank order in boxes 1 most important, 6 least important)
    - ☐ identifying key technology requirements for the industry N 1 2 3 4 5 6 7
    - ☐ building consensus on priorities for research and development N 1 2 3 4 5 6 7
    - ☐ planning efficient use of industry pre-competitive and R&D resources N 1 2 3 4 5 6 7
    - ☐ coordinating development activities and fostering industry standards across a diverse set of industrial sectors and organizations N 1 2 3 4 5 6 7
    - ☐ collaboration and opportunity to build professional contacts worldwide N 1 2 3 4 5 6 7
    - ☐ obtaining strategic industry information in a timely fashion N 1 2 3 4 5 6 7

13. What other values and benefits do you derive from the Semiconductor Technology Roadmap process?
    _____
    _____
    _____

14. Please rate your preferences for Roadmap participant communication. (1 is most desirable, 5 is least desirable)
    - ☐ Face-to-face
    - ☐ E-mail
    - ☐ Teleconference
    - ☐ Video conference
    - ☐ Personal phone call

15. How will you use the information obtained from the Roadmap process? (check all that apply)
    - ☐ Business planning
    - ☐ Research planning
    - ☐ New product development
    - ☐ Other: specify _____
16. Do you plan to continue your involvement in future roadmaps?
    - ☐ Yes
    - ☐ No, why not? _____

Response to hypotheses (agree/disagree, why?):

17. The SIA Roadmap has contributed to a more regular, more predictable, and even accelerated pace of innovation through deliberate coordination of pre-competitive R&D and related industry resources.
    _____
    _____
    _____
18. Although collaboration found in the Roadmap process is not new, the structure and methods employed (e.g., pre-competitive basis, broad participant network, process—not product—emphasis) are clearly unique.
    _____
    _____
    _____
19. The key driver for the SIA Roadmap has evolved from international competitiveness in the late-1980s to a global strategy in the late-1990s to stay on the industry's productivity curve as defined by Moore's Law.
    _____
    _____
    _____
20. The SIA Roadmap has qualitatively affected R&D expenditure patterns of the U.S. semiconductor industry (emphasizing more "D" than "R"). In other words, the Roadmap has shortened the research agenda horizon.
    _____
    _____
    _____

Open-ended questions:

21. Why has the semiconductor industry in particular embraced roadmapping so enthusiastically?
    _____
    _____
    _____
22. In what ways is the Semiconductor Technology Roadmap process unique as compared with other forms of technology planning for an industry, including other industry roadmaps?
    _____

_____
_____

23. In what ways has the Roadmap influenced technological innovation in the semiconductor industry?
_____
_____
_____

24. Do you think that Moore's Law drives the Roadmap or is it the other way around?
_____
_____
_____

25. In what ways has the Roadmap influenced corporate strategies and public policies for the industry?
_____
_____
_____

26. Can you think of alternative ways that would be effective in obtaining the information contained in the Roadmap?
_____
_____
_____

27. How does the industry know if the Roadmap "works" and how is success measured?
_____
_____
_____

28. Is there a relationship between the SIA Semiconductor Technology Roadmap and corporate roadmaps? If so, is there an underlying structural hierarchy among these roadmaps?
_____
_____
_____

29. What are the major advantages and disadvantages of an *International* Technology Roadmap process as compared with a *National* Technology Roadmap process?
_____
_____
_____

30. Name two (2) strengths of the SIA Semiconductor Technology Roadmap process.
_____
_____
_____

31. Similarly, name two (2) weaknesses of the SIA Semiconductor Technology Roadmap process.
_____
_____
_____

32. Please provide any additional thoughts and comments on the Semiconductor Technology Roadmap process including any suggestions for improving the process.
    _____
    _____
    _____

33. Speculate on the semiconductor industry without a Semiconductor Technology Roadmap: Would technological progress in semiconductors be any different without a roadmap? Would the pace be faster, slower, more irregular? In what other ways?
    _____
    _____
    _____

34. Speculate on the Future: What will the 2005 Semiconductor Technology Roadmap look like? In what ways will it be different than the 1999 Semiconductor Technology Roadmap? In what ways will it be similar?
    _____
    _____
    _____

35. What about the Semiconductor Technology Roadmap process? Will it include other regions of the world? Will/can it become more inclusive of the supplier and/or user community?
    _____
    _____
    _____

International questions:

36. How has (does) the SIA Roadmap serve the needs of the international semiconductor community (i.e., chip customers, chip makers, equipment and material suppliers, universities, and related government agencies)?
    _____
    _____
    _____

37. Has the evolution of the Roadmap taken into account the changing structure of the semiconductor industry?
    _____
    _____
    _____

38. At the device level there is increasing growth of fabless firms and foundries. How are their requirements included in the Roadmap?
    _____
    _____
    _____

39. Do some firms diverge from the Roadmap and if so, why? For that matter, do some firms totally ignore the Roadmap and if so, why?
    _____
    _____
    _____

40. Some have argued that the Roadmap has helped in the recovery of the U.S. semiconductor and SM&E (materials and equipment) industries by better aligning technical requirements along the vast semiconductor supply chain. Do you agree with this and why?

    _____
    _____
    _____

41. Any suggestions for improving the Roadmap process, with particular emphasis on international considerations?

    _____
    _____
    _____

Appendix: Roadmap Participant Survey List

Name	Date[1]	Category[2]	Type[3]	Status[4]	Inter-national
Allan, Alan	8/20/99	Chipmaker, Intel	phone	complete	
Bird, Mark	6/2/99	Supplier, Amkor Technology	face-to-face	partial	Korea
Bloch, Erich	8/16/00	Analyst (Washington Advisory Group)	face-to-face	context	
Bohr, Mark	1/4/00	Chipmaker, Intel	phone	context	
Bracken, Ron	8/3/00	Consortium, SRC	face-to-face	complete	
Brown, Karen	8/27/99	Government, NIST	phone	complete	
Broydo, Sam	3/6/00	Supplier, Applied Materials	phone	partial	
Brueck, Steve	7/7/00	University, U of New Mexico	phone	context	
Burger, Bob	7/15/99	Consortium, SRC	face-to-face	complete	
Carruthers, John	11/30/99	Chipmaker, Intel	e-mail	complete	
Cavin, Ralph	8/1/00	Consortium, SRC	face-to-face	partial	
Chang, Chi Shih	9/11/02	Supplier, Kulicke & Soffa	phone	complete	
Class, Walter	3/6/00	Supplier, Eaton	phone	complete	
Derbyshire, Katherine	1/12/01	Analyst (Journalist, Penwell Publishing)	phone	context	
Diebold, Alain	8/16/99	Consortium, Sematech	phone	complete	
Doering, Bob	7/26/99	Chipmaker, Texas Instruments	phone	complete	
Fukushima, Toshitaka	5/25/00	Chipmaker, Fujitsu	phone	complete	Japan
Gargini, Paolo	8/16/99	Chipmaker, Intel	phone	partial	
Glaze, Jim	7/14/99	Government, Virtual National Lab	phone	partial	
Greed, Jim	6/19/00	Supplier, Foothill Technology (SEMI)	e-mail	complete	
Harrell, Sam	5/11/00	Supplier, KLA-Tencor	phone	context	
Herr, Dan	8/1/00	Consortium, SRC	face-to-face	context	
Howard, Bill	8/99	Analyst, Consultant (former Motorola)	phone	partial	
Hu, Genda	5/7/00	Chipmaker, TSMC	phone	complete	Taiwan

Hutchby, Jim	8/1/00	Consortium, SRC	face-to-face	context	
Hutcheson, Dan	3/10/00	Analyst, VLSI Research	phone	partial	
Joyner, Bill	8/1/00	Consortium, SRC	face-to-face	complete	
Kahng, Andrew	3/1/02	University, UC San Diego	phone	complete	
Klingenstein, Werner	5/11/00	Chipmaker, Infineon Technologies	e-mail	complete	Germany
Leckie, Ron	6/8/00	Analyst, Infrastructure	e-mail	complete	
Matisoo, Juri	8/10/00	Chipmaker (Trade Association, SIA)	phone	context	
Meindl, Jim	8/16/99	University, Georgia Tech	phone	context	
Ning, Tak	7/18/00	Chipmaker, IBM	face-to-face	context	
Novak, Larry	8/26/99	Supplier, USR/Radian International	phone	complete	
Oberai, Obi	5/1/00	Analyst, Consultant (former IBM)	phone	partial	
Peercy, Paul	8/30/99	Consortium, SISA	face-to-face	partial	
Reader, Alec	5/24/00	Chipmaker, Philips	phone	complete	Nether-lands
Rubin, Leonard	3/3/00	Supplier, Eaton	phone	partial	
Scace, Bob	8/16/99	Government, NIST (contractor)	phone	partial	
Schulz, Steve	9/1/99	Chipmaker, Texas Instruments	phone	context	
Seidel, Tom	8/12/99	Supplier, Genus	e-mail	complete	
Skinner, Court	8/17/99	Consortium, SRC	phone	partial	
Spencer, Bill	8/31/99	Consortium, Sematech	face-to-face	context	
Tasch, Al	9/27/99	University, U of Texas at Austin	phone	complete	
Tracy, Dan	3/21/00	Analyst, Rose Associates	e-mail	complete	
Weber, Werner	5/16/00	Chipmaker, Infineon Technologies	e-mail	complete	Germany
Werner, Bob	5/5/99	Consortium, Sematech	phone	complete	
Williams, Owen	8/21/99	Chipmaker, Motorola	e-mail	complete	
Wilson, Linda[5]	5/98-9/02	Consortium, Sematech	phone[5]	context	
Wollesen, Don	8/3/99	Chipmaker, AMD	phone	complete	

Notes:

1. Date reflects the last date of communication between the researcher and the respondent. In several cases there were two or more contacts.

2. Category reflects the last position held relative to Roadmap involvement. Note that many of the respondents had long and extensive careers within the semiconductor community. A number had worked in several capacities, thus much insight from previous and/or succeeding positions was offered. Also, a few respondents labeled *Analyst* were intimate users and not participants in the Roadmap process, but due to their familiarity with the Roadmap were included to help ensure balance of perspectives.
3. Type is the primary data collection method. In many cases there were multiple methods used. A common example is that each e-mail response was either followed or proceeded by a phone call with the researcher.
4. Status refers to the general level of completion of each survey. *Completed* means the major components of the survey (i.e., Roadmap process evaluation questions and four research hypotheses) were completed. However, in some cases not every remaining question was answered due to time constraints and other factors. The cut-off for *complete* is that all but no greater than four (4) questions (out of up to 40) were answered. *Partial* status accounts for any survey with more than four questions not answered. Finally, some interviews of industry executives or former participants where the exact survey flow and line of questioning was inappropriate were labeled *context* surveys. However, the survey instrument was used to guide these interviews in the same fashion as with any other Roadmap participant.
5. Linda Wilson is the ITRS Information Manager at Sematech and Managing Editor of all Roadmap editions and updates beginning with the 1997 NTRS. Communication with her has been on-going throughout this research and has occurred mostly via telephone, but also via e-mail and face-to-face.

Appendix B: Detailed Findings of Survey Data

This appendix includes detailed answers to questions asked of participants in response to the ITRS Survey conducted by the author between July 1999 and September 2002. Responses appear in the same order as the questions were numbered in the survey instrument. An index is included below. Answers to survey questions will be included as they are completed in the proposed format (roughly 2pgs per question). Presently only a few of the more than two dozen answers appear here.

The process involved in presenting these findings started with data entry of all 49 surveys. Twelve surveys were completed electronically within the actual Microsoft Word document and e-mailed to the author. About six surveys were completed in face-to-face interviews either by the author or participant. The remaining thirty surveys were completed by the author during telephone interviews with participants. As discussed in Chapter 5: Research Design, twenty-five or 51% of the surveys were considered complete while another twelve (24.5%) were partially completed. The remaining twelve (24.5%) were considered context interviews but included some answers to survey questions.

A separate Word file was created for each participant survey. Answers were transcribed (or cut and pasted if electronic) *verbatim* from participant surveys. The author then created individual files by survey question and populated each with respective answers from participant survey files. In the process all attribution references were removed and some minor editing changes (composition and spelling corrections only) were made. Otherwise, participants' responses were transferred completely as received.

Once the transfer process was finished the author printed out all answer files in question order. The result was more than sixty single-spaced pages of free-form answers. The author then began the process of developing detailed findings from raw responses in each answer file. This process will vary by type of question, but using Q24 (Do you think that Moore's Law drives the Roadmap or is it the other way around?) as an example the first step was to classify and reorder individual answers (see attached). Once reordered, answers were further arranged if appropriate by consistent patterns or themes in replies. In some cases, longer responses with more than one theme were separated and reordered accordingly. Any redundancies were then removed. In all cases original answers were not changed. If appropriate, statistics were generated for classification of responses. Finally, pertinent analysis was provided.

The goal of this appendix is a detailed yet organized representation of participant responses that sufficiently enables analysis to inform this study.

A note on numbering of questions and answers: there were four slightly different interview instruments used during this research. A basic one, approved by Sematech at the outset of interviews, was modified slightly to correct for redundancy: one question was eliminated through consolidation (out of 36). No other questions were changed. In the process it was also realized that the specific needs of certain participating communities were different (i.e., research vs. supplier). Thus, six additional questions tailored to three different semiconductor communities (R&D, SM&E, and International) were added as optional questions at the end of the instrument (see International example in previous appendix).

Finally, three additional questions were asked as follow-up to some of the early responses to the survey. They were not included in the survey *per se* but were often discussed informally with respondents. The answers are included here at the end to help round out the inquiry.

Index of free response questions and answers:

7. How and why did you become involved in the Semiconductor Technology Roadmap?
8. Why do you attend the formal Semiconductor Technology Roadmap workshops and conferences? (Other)

Comments on Roadmap values and benefits:

9. The Roadmap process meets my expectations.
10. The Roadmap process allows me to influence industry direction.
11. The Semiconductor Technology Roadmap workshops, conferences, and TWG meetings are a good way to communicate technology needs and work key issues.
12. The Roadmap's key value is:
    a. identifying key technology requirements for the industry
    b. building consensus on priorities for research and development
    c. planning efficient use of industry pre-competitive and R&D resources
    d. coordinating development activities and fostering industry standards across a diverse set of industrial sectors and organizations
    e. collaboration and the opportunity to build professional contacts worldwide
    f. obtaining strategic industry information in a timely fashion
13. What other values and benefits do you derive from the Semiconductor Technology Roadmap process?
14. Please rate your preferences for Roadmap participant communication.
15. How will you use the information obtained from the Roadmap process? (Other)
16. Do you plan to continue your involvement in future roadmaps?
17. Hypothesis 1: The SIA Roadmap has contributed to a more regular, more predictable, and even accelerated pace of innovation through deliberate coordination of pre-competitive R&D and related industry resources.
18. Hypothesis 2: Although collaboration found in the Roadmap process is not new, the structure and methods employed (e.g., pre-competitive basis, broad participant network, process - not product - emphasis) are clearly unique.
19. Hypothesis 3: The key driver for the SIA Roadmap has evolved from international competitiveness in the late-1980s to a global strategy in the late-1990s to stay on the industry's productivity curve as defined by Moore's Law.
20. Hypothesis 4: The SIA Roadmap has qualitatively affected R&D expenditure patterns of the U.S. semiconductor industry (emphasizing more "D" than "R"). In other words, the Roadmap has shortened the research agenda horizon.
21. Why has the semiconductor industry in particular embraced roadmapping so enthusiastically?
22. In what ways is the Semiconductor Technology Roadmap process unique as compared with other forms of technology planning for an industry, including other industry roadmaps?
23. In what ways has the Roadmap influenced technological innovation in the semiconductor industry?

24. Do you think that Moore's Law drives the Roadmap or is it the other way around?
25. In what ways has the Roadmap influenced corporate strategies and public policies for the industry?
26. Can you think of alternative ways that would be effective in obtaining the information contained in the Roadmap?
27. How does the industry know if the Roadmap "works" and how is success measured?
28. Is there a relationship between the SIA Semiconductor Technology Roadmap and corporate roadmaps? If so, is there an underlying structural hierarchy among these roadmaps?
29. What are the major advantages and disadvantages of an *International* Technology Roadmap process as compared with a *National* Technology Roadmap process?
30. Name two (2) strengths of the SIA Semiconductor Technology Roadmap process.
31. Similarly, name two (2) weaknesses of the SIA Semiconductor Technology Roadmap process.
32. (and #41) Please provide any additional thoughts and comments on the Semiconductor Technology Roadmap process including any suggestions for improving the process.
    a. with particular emphasis on the SM&E industry?
    b. with particular emphasis on research community considerations?
    c. with particular emphasis on international considerations?
33. Speculate on the semiconductor industry <u>without a Semiconductor Technology Roadmap</u>: Would technological progress in semiconductors be any different without a roadmap? Would the pace be faster, slower, more irregular? In what other ways?
34. Speculate on the Future: What will the 2005 Semiconductor Technology Roadmap look like? In what ways will it be different than the 1999 Semiconductor Technology Roadmap? In what ways will it be similar?
35. What about the Semiconductor Technology Roadmap process? Will it include other regions of the world? Will/can it become more inclusive of the supplier and/or user community?

SUPPLEMENTAL SURVEY QUESTIONS (asked of SM&E, Research, and International respondents):

36. How well does the Roadmap serve the needs of:
    a. SIA members?
    b. the semiconductor material and equipment supplier industry?
    c. the research community, both in industry (e.g., IBM's T.J. Watson's Research Center), universities, and the national labs?
    d. the international semiconductor community (i.e., chip customers, chip makers, equipment and material suppliers, universities, and related government agencies)?
37. Has the evolution of the Roadmap taken into account the changing structure of the industry?
    a. For example, the SM&E industry is now more specialized, stronger, and more knowledgeable/ responsible for industry R&D advances. Is this structural change reflected in the roadmapping process?

b. Has the evolution of the Roadmap taken into account the changing nature of semiconductor research?

38. At the device level there is increasing growth of fabless firms and foundries. How are their requirements included in the Roadmap?
39. Do some firms diverge from the Roadmap and if so, why? For that matter, do some firms totally ignore the Roadmap and if so, why?
40. Some have argued that the Roadmap has helped in the recovery of the U.S. semiconductor and SM&E (materials and equipment) industries by better aligning technical requirements along the vast semiconductor supply chain. Do you agree with this and why?
41. Any suggestions for improving the Roadmap process (see #32)?

ADDITIONAL QUESTIONS (not specifically asked in survey instrument but asked of many informants):

42. In your own words, what is the purpose of the Roadmap?
43. Why is the Roadmap successful?
44. Is there any possibility that the Roadmap process will end? Why or why not?

Roadmap Participants Survey Results: Part A

Note that Table B-1 on the next page is an Excel spreadsheet for questions #1-16 of the survey.

Table B-1. Roadmap Participants Survey Results: Part A

Name	Date	Class (1 IC, 2 sme, 3 res, 4 gov, 5 con, 6 lab, 7 anl)	User only	How long involved in Roadmap? (years)	First Roadmap	Last Roadmap	Rate involvement (1 va, 2 a, 3 i, 4 si)	Role in the Roadmap process	Percent time spent on Roadmap	How/why involved? (1 req, 2 appt, 3 vol)	Why attend workshops? (1 ei, 2 ti, 3 c, r o)	Roadmap process meets my expectations	Allows me to influence industry direction	TWG mtgs good way to communicate needs/work issues	... identifying key technology requirements for the industry	... building consensus on priorities for R&D	... planning efficient use of pre-competitive R&D resources	... coord'ing develop. activities, fostering industry standards	... collaboration and oppty to build prof. contacts worldwide	... obtaining strategic industry information in a timely fashion	Rank order Q12 (a, b, c, d, e, f)	Other (y)	face-to-face	e-mail	teleconference	video conference	personal phone call	How will use info? (1 bp, 2 rp, 3 npd, 4 o)	Plan to continue?
Jim Glaze	14-Jul-99	5(1),6		6	1993	1998	1	RCG	20%	1		7	5	5	5				5	5		y							y
Bob Burger	15-Jul-99	5 (3)		10	1984	1997	1	RCG	75%	1		7										y	1					2	n
Bob Doering	26-Jul-99	1		9	1992	2000	1	RCG,IRC	10%	2	3,1,2	5	4	6	6				7	5		y	1	3	2	3	5	2	y
Don Wolleson	3-Aug-99	1		9	1991	1999	1	RCG	50%	1,2,3	1	6	7	7	6				6	6		y	1	2	3	5	4	1,2,4	
Tom Seidel	12-Aug-99	5 (1)		8	1992	1999	1.5	TWG,RCG	50%	1,2,3	1	6	5	6	7				4	6			1	2	4	4	2	1,2,3	y
Alain Diebold	16-Aug-99	5 (1)		7	1994	2000	1	TWG	15%	3	1,2	6	6.5	6	6.5				5	6		y							y
Bob Scace	16-Aug-99	4		8	1992	2000	2	RCG,TWG																					
Karen Brown	18-Aug-99	5(1),4		6	1994	2000	1	TWG	25%	1	1,2,3	5	3	6	5				6	4		y	1	3	2	5	3	2	y
Alan Allan	20-Aug-99	1		6	1991	2000	1	RCG,IRC	50%	2,3	1,3	5.5	7	6.5	6.5				6.5	6.5		y	1	3	4	2	5	1,2	y
Owen Williams	25-Aug-99	1		9	1992	1997	1	TWG,RCG	10%	1,2,3	1,2,3,4	7	4	7	7				2	7		y	1	4	2	3	5	1,2,4	y
Larry Novak	26-Aug-99	2,5(1)		8	1992	2000	1	TWG	15%	1	1,2,3	6	6	6	7				6	6		y	1	3	2	5	4	1	y
Paul Peercy	30-Aug-99	5 (2)		8	1992	1999	1	RCG	10%	1	4	6	5	6	7				5	6		y	1	3	2	2		4	y
Al Tasch	27-Sep-99	3		6	1992	1997	1	TWG,RCG	10%	3,1	2,1,3	6.5	5	6	6				2			y	1	3	4	2	5	2,4	
John Carruthers	30-Nov-99	1		14	1984	1999	2	P	5%	3	4	6	7	6	7				2	4		y	1	3	2	5	4	2	y
Leonard Rubin	3-Mar-00	2		1	1999	2000	2	TWG	5%	3	1	3	2	2						b/c,a,d,e,f			2	1	3	5	4	1	y
Sam Broydo	6-Mar-00	6		2	1994	1999	2	TWG	5%			5	3	4	7	7	7	5	2	5		y							
Walter Class	6-Mar-00	2		7	1994	2000	1	TWG,IRC,P	25%	3	1	6	5	4						a,c,b,f,e,d		y	2	1	2	5	4	1,2	y
Dan Tracy (Rose Ass)	21-Mar-00	7	y											7	1	2	2	2	3	2		y							n
Obi Oberi	1-May-00	5 (1)		10	1994	2000	1	TWG	20%	2	2	6	6	7						a-f in order		y	1	3	4	5	2	1,3	y
Genda Hu	7-May-00	5 (1)		2	1998	2000	2	IRC	5%	3	1	6	6	6	6	3	5	6	5	5	a-f in order			3	1	5	4	2	2	y
Werner Klingenstein	11-May-00	1	y									6	5	7	6	4	6	5	6	7	f,a,b,c,e,d	y	1	2	5	4	3	1,2	y
Werner Weber	16-May-00	1		2	1998	2000	2	TWG,IRC,P	5%	2	1,2	7	3	6	7	5	6	3	2	4	a,c,b,e,f,d		2	1	3	5	4	2	y
Alec Reader	24-May-00	1		2	1999	2000	1.5	TWG	5%	2	1,2,3,4	5.5	5.5		7	5.5	3.5	3	5.5	3.5									y
Toshitaka Fukushima	25-May-00	1		2	1998	2000	2	IRC	10%	1	1,2	6	7	7	7	7	7	7	7	7	a,f,d,b,e,c			1	2	4	5	3	1,2	y
Ron Leckie	8-Jun-00	7		2	1994	?	2	TWG	5%	2	1	5	6	5	6	5	5	5	7	7		y	1	3	4	2	5	1,3	n
Jim Greed	16-Jun-00	2		9	1992	1999	2	TWG	5%	1	4	5	4	5	1	4	2	3	3	3		y	1	2	3	5	4	4	y
Bill Joyner	1-Aug-00	5 (3)		3	1998	2000	1	TWG	10%	2	2,3	5	5	5	6	5	6	6	5	5	a,c,b,d,f,e			1				1	y
Ron Bracken	3-Aug-00	5 (3)		3	1997	1999	1	TWG	20%	2,3	1,2,4	6	6	6	7	7	6	6	6	6		y	1	3	3	4	2	2	
Andrew Kahng	1-Mar-02	3		6	1997	2001	1	TWG	12%	3	1,3	5	7	3	6	6	1	2	5	5		y							y
Chi Shih Chang	11-Sep-02	2 (5)		8	1997	2002	1	TWG	5%	2	1	7	7	7	7	7	7	6	6	7	a,b,d,c,e,f	y	1	3	2	5	3	1,3,2	y
Sample (n)	30		2	28	28	27	28	28	27	26	24	28	27	27	25	13	13	13	25	24	9	22	22	22	21	21	20	23	25
Totals				173								162.5	142	154.5	150	67.5	63.5	59	119	128			27	52	65	85	73		
Averages				6.9								5.8	5.3	5.7	6.0	5.2	4.9	4.5	4.8	5.3			1.2	2.4	3.1	4.0	3.7		

Roadmap Participants Survey Results: Part B

The following pages are a compilation of detailed responses to survey questions #2-41, followed by responses to three related questions that did not appear in the survey.

2. How many years [involved in Semiconductor Technology Roadmap]?

There were 28 responses representing 173 total years' involvement in semiconductor industry roadmaps. The average involvement for all respondents was 6.9yrs. One respondent had only been involved for 1yr while another had been involved for 14yrs (this respondent had participated in the SRC 10yr Goals exercise in 1984). The range was as follows:

Range (yrs)	#
1 to 3	9
4 to 6	5
7 to 9	11
10 or more	3

3. Please indicate the extent of your past roadmap involvement.

There were 40 total responses. Most of the surveys were conducted between the summer of 1999 and early 2000 coincident with the 1999 ITRS cycle (published December 1999 and distributed early 2000). The 2001 ITRS and 2002 Update choices did not appear in the first survey instruments but were added in subsequent surveys. Note that only two surveys were conducted after 2000 and they were both in 2002. The breakdown of responses follows.

Roadmap Edition	#	%
2002 Update	2	5%
2001 ITRS	2	5%
2000 Update	10	25%
1999 ITRS	33	83%
1998 Update	30	75%
1997 NTRS	27	68%
1994 NTRS	25	63%
1992 Roadmap	18	45%
earlier (e.g., MicroTech 2000)	14	35%
Total Responses	40	100%

Note the large majority of 1999 ITRS participants (83% checked this box). The 1999 ITRS process is the primary unit of analysis for this study. Further analysis helps explain the almost 7year average involvement from Q2 above. That is, more that 90% of the respondents had participated in multiple Roadmaps, and most of these (62.5% of total) claimed involvement on four or more Roadmaps as follows:

No. Roadmaps	#	%
one	3	7.5%

two	3	7.5%
three	9	22.5%
four or more	25	62.5%

These results support what many respondents stated: involvement in the Roadmap process is a longer-term commitment. Given that participation is fully voluntary, this level of dedication helps explain the development and continuance of a true Roadmap community.

4. How would you rate your involvement?

There were 28 responses. All claimed *very active* or *active* involvement as follows:

Rating	#	%
1. very active	17	61%
1.5 'in between'	2	7%
2. active	9	32%
3. and 4. interested and somewhat interested	0	0%

Again, this is consistent with results from Q2 and Q3 above.

5. What is (was) your role in the Semiconductor Technology Roadmap process?

There were 28 responses. Most of the survey participants held leadership or other positions requiring significant involvement. Fourteen or 50% claimed Roadmap Coordinating Group (RCG) or International Roadmap Committee (IRC) involvement while 19 or 68% claimed Technology Working Group (TWG) involvement. Eight claimed both roles. Only one claimed the sole role as *participant*.

6. If you are (were) a TWG, RCG, or IRC member, estimate the percentage of your time spent on the SIA Semiconductor Technology Roadmap activities outside of the formal workshops and conferences? _____%

There were 27 responses ranging from 5% to 75% with the overall average of 18%. The distribution of most cited ranges is as follows:

Range (%)	#	%
5%	9	33%
10 to 15%	9	33%
20 to 25%	5	19%
over 25%	4	15%

There was wide variation in the responses. The wording of this question was too general to accommodate differences among particular Roadmap roles as well as changing roles between editions (e.g., one respondent claimed 50% involvement in '92 and '94 Roadmaps but only 10% '99 ITRS). However, many respondents indicated the significance of this involvement with comments such as:

- averages couple days/month, some peaks 100%

- 50% big task supporting ITRS
- significant (25%)
- 20% (key responsibility)
- roadmap intense right before meetings, suppliers workshop follow-up, etc.

7. How and why did you become involved in the Semiconductor Technology Roadmap?

There were 26 total responses to this question. Respondents chose among three categories as follows. Several respondents selected multiple categories (shown in the # total column) while "# first" shows the count for first category selected. No discernable preference can be drawn from these findings other than volunteering based on personal or professional interest appears to be the least chosen first reason. This may be so because involvement in the Roadmap process requires a good deal of commitment in time and travel.

Reason	# total	# first
Requested directly from SIA to serve on a TWG, RCG, or IRC	11	10
Appointed by your management	12	9
Volunteered based on personal or professional interest	12	7

Additional Comments:

- Sematech good framework to work from.
- Professional interest - very important piece of work - others appointed or dragged.
- No one addressing measurement technology. Personal belief, not just with knowledge but emotions, so Sematech involved - President and COO well-versed. Sematech environment unique: people who understand it are ambassadorial, only a few people really have a job description.

8. Why do you attend the formal Semiconductor Technology Roadmap workshops and conferences?

There were 24 total responses to this question. Respondents chose among four categories as follows. Like the previous question (Q7), several respondents selected multiple categories (shown in the # total column) while "# first" shows the count for first category selected. In this case, *Company/industry analysis* was selected the most, especially as the #1 choice, distantly followed by *Early insight of industry trends*. *Technical interest* ranked last as first choice.

Reason	# total	% total	# first	% first
Company/industry analysis	19	42%	17	71%
Early insight of industry trends	12	27%	3	12.5%
Technical interest	8	18%	1	4%
Collaborate with colleagues	6	13%	3	12.5%
Total Responses	45	100%	24	100%

The following comments were offered in response to the 5th category, *Other*, as follows:

- Consensus-building process (all categories blend together).

- Process lends itself to collaborate.
- Collaborate with colleagues across the world.
- Set research agenda.
- Involvement in roadmap means you'll know early (earlier than others).
- Critically important to the coordination of a global supplier response to the 1999 ITRS.
- Ask you to attend, good for input from suppliers, supplier's reputation okay, keep sanity.
- Combine with something else (e.g., Semicon West show) to justify travel from Europe.

Questions or statements 9 through 12 involved a ranking using a Likert scale from 1 (strongly disagree) to 7 (strongly agree). The middle value of 4 indicated *no opinion* while an outside choice N stood for *not applicable*.

9. The Roadmap process meets my expectations.

There were 28 replies, ranging from 3 to 7 with an overall average of 5.8.

- satisfied, well organized, look ahead of what customers want, "wrong word" if think from supplier's view
- benchmark, keep seeing possibilities
- exceeded
- 7 if better attendance

10. The Roadmap process allows me to influence industry direction.

There were 27 replies, ranging from 2 to 7 with an overall average of 5.3.

- participation does allow influence, doesn't allow to drive (collaboration)
- not influence (not good word) - no axe to grind, but participate in defining direction
- not as influential
- Personally the most rewarding part. Environment to give back (beyond company selfish interests). Engineering employs "optimists," about solving problems and finding answers, frustrating to reinvent the wheel, joy in knowing (optimism). Roadmap is chance to put away selfish interests for "common good."

11. The Semiconductor Technology Roadmap workshops, conferences, and TWG meetings are a good way to communicate technology needs and work key issues.

There were 27 replies, ranging from 2 to 7 with an overall average of 5.7.

- semi (device maker) industry definitely communicates needs
- more global standpoint - implementation done after the roadmap (supplier community)
- brings up points on the table, then can agree on what issues to be worked on, then action
- TWG meetings: not on their own, sessions usually a way of initiating things, follow-up to work issues (e-mail, etc), social impact important!

- TWG meetings are excellent for technology communication. Workshops and conferences are far from ideal.

12. The Roadmap's key value is:

This question was changed when the survey instrument was revised to accommodate research, supplier, and international questions. Three previous *value* questions were consolidated into this question as sub-questions. Three new *value* sub-questions were also added – these three had 13 respondents versus almost twice that number for the other three *value* sub-questions.

The Roadmap's key value is…	#	range	avg*
a. identifying key technology requirements for the industry.	25	1-7	6.0
b. building consensus on priorities for research and development.	13	2-7	5.2
c. planning efficient use of industry pre-competitive and R&D resources.	13	1-7	4.9
d. coordinating development activities and fostering industry standards across a diverse set of industrial sectors and organizations.	13	2-7	4.5
e. collaboration and the opportunity to build professional contacts worldwide.	25	2-7	4.8
f. obtaining strategic industry information in a timely fashion.	24	2-7	5.3

* scale is 1 (strongly disagree) to 7 (strongly agree)

Ranking these values by averages:

1. a. identifying key technology requirements (6.0)
2. f. obtaining strategic industry information in timely fashion (5.3)
3. b. building consensus on priorities for R&D (5.2)
4. c. planning efficient use of industry R&D resources (4.9)
5. e. collaboration and building professional contacts (4.8)
6. d. coordinating development activities and fostering industry standards (4.5)

Additionally, in the revised survey respondents were asked to rank order these values directly. Nine participants responded as follows:

rank	values ranked by respondents (n=9)									top 2 (n)
1.	b/c*	a	a	a	f	c	f	c	b	a (3), c (3)
2.		c	b	b	a	a	a	a	a	a (5), b (2)
3.	a	b	c	c	b	b	d	b	d	b (4), c/d* (2)
4.	d	f	d	d	c	e	b	d	c	d (4), c (2)
5.	e	e	e	e	e	f	e	f	e	e (7), f (2)
6.	f	d	f	f	d	d	c	e	f	f (4), d (3)

* tie

The attempt to rank order values in this manner proved confusing to some respondents, thus the small number of responses. Nonetheless, those that did rank order Roadmap values seemed to

validate the previous ranking method (by averages) because each sub-question appears in the *top 2* list in the same order as by average except for "f."

Comments: although not requested, some respondents added additional comments along with their ratings. They appear below by sub-question.

a. identifying key technology requirements for the industry

- strong, absolutely
- yes, entire industry more efficient in investment of resources
- fair amount of misinterpretation
- sometimes

b. building consensus on priorities for research and development

- strong, absolutely
- more compromise than consensus
- international

c. planning efficient use of industry pre-competitive and R&D resources

- strong, absolutely
- not good word, stimulates and focuses research - universities go off on their own, certain universities take it too literally, too dangerous if too narrow (need to have more freedom) - "more than one way to skin a cat" - important: make clear there is a "challenge" of science (something completely different) - not just more scaling - in European research, roadmap cited in support vs driving role (more freedom in European research, lump sum funding not grant dependent) - fundamental problems to be surmounted: completely new way around it

d. coordinating development activities and fostering industry standards across a diverse set of industrial sectors and organizations

- not establish standards, only common understanding of requirements - not even an attempt to establish standards, but agreement on set of predictions of requirements
- I300I useful - Semi has standards committee

e. collaboration and the opportunity to build professional contacts worldwide

- networking valuable to individuals
- gain efficiency by sharing ideas
- true, troubled by past motivation for competitiveness
- Stability of results, struggle with issues (small hesitancy). Process creates stabilizing effect from device manufacturers and suppliers standpoint, technical requirements not exact, but greatest value in whole worldwide industry working on building relationships.
- not a big deal

f. obtaining strategic industry information in a timely fashion

- yes, sure - info on requirements (non-proprietary)
- already know ahead of time
- Critical factor (timely), time value very high, getting right on cooperative basis. Sematech web service important: go on-line, immediacy crucial, don't have to wait.

13. What other values and benefits do you derive from the Semiconductor Technology Roadmap process?

There were 36 total responses to this question. Many could actually be classified under Q8 or Q12 (previous questions) categories, but this question (Q13) provided space for comments. Responses varied significantly so they have been arranged by types of major benefits. Some responses that included more than one benefit were separated, however there is still some overlap.

Provides focus on key issues

Device maker industry

- Industry unification of key issues such as EHS.
- The Roadmap provides a *consensus* of the semiconductor technology needs to the Research community and to the Supplier Industry. This eliminates endless hours of debate in these two communities over what the technology are needed and allows immediate focused execution on meeting those technology needs.
- Focuses entire industry's attention on critical needs (it is a needs document) if productivity to continue.
- Effect of Roadmap: profound influence on equipment and material suppliers as well as R&D community.

Supplier

- could be deviations: roadmap provides sanity check, better idea where to invest in how used: look at no known solutions (red space), talk to customers (chipmakers), "test" solutions of red zones in an iterative way (understand their "red areas") in lieu of guessing, "gives us an entry" from public domain
- Saves wasted resources working on not-needed technologies. Purchasing agents (engineers/managers working through purchasing agents mistreat suppliers - misuse - get different needs) - toolmakers got a diverse set of needs (working on unnecessary R&D)
- Supplier's chief value: single source consensus of needs - this is the main (single) reason roadmap went international - avoid threat from competing (e.g., Japan) roadmaps.
- From supplier's position: getting unique requirements of customers (chipmakers) - talk to customers, then requirements change according to roadmap. Absolutely necessary to change on Moore's curve (extrapolate from past) - predictions, sanity check - every year roadmap adjusted.
- I think the roadmap is useful because it provides an industry-wide coordination for suppliers and it helps set standards for equipment that makes suppliers jobs much easier.
- Guideline for Equipment supplier.

Development

- I believe that the ITRS tends to DRIVE the development of the processes and equipment that enables the needs to be met. Usually this is before the Roadmap itself projects them.
- obtaining greater efficiency in technology development (reduced R&D budgets lead to consortia - industry-oriented) - gain efficiency by sharing ideas - comment: in early days companies surprised that "their secrets weren't really secret" - roadmap helped break down barriers

- Roadmap has been "pro-optical" - prior to roadmap there was no industry consensus on direction of lithography (some pushing x-ray, some e-beam), after roadmap began then most followed i-line/248/193 optical path - much more efficient use of R&D

Research

- mainly discussion with peers about potential roadblocks
- See later comments - mostly in setting the research agenda and providing long-term direction to suppliers.
- Tremendous way to get university and national labs on research front to work together, also needs of supplier community but much tougher. Research seeing industry needs very important - compelling needs (able to see what industry needs) - what's beyond CMOS transistors? Completely open to work on it.
- Personally helped acquire a better perspective (from a university viewpoint) - gaps in knowledge, really helped bring closer to reality - university faculty need "time to think" - substantial university involvement [in innovation] this order: 1) industry, 2) university, 3) government. Example: device/ion implant modeling, contribution research - help in understanding trends through generations of devices.

Government

- Roadmap is most significantly documented source of industry technology needs: 1) it-is kept up, and 2) is a consensus document representing industry's view - this is chief value for a government agency. Gathers experts
- Roadmap gets the experts together - best people's opinions at the time
- Everybody's expertise in one area, allows broader and deeper understanding

Consensus

- Consensus building
- Key value: consensus of needs - 1. supplier, 2. research community also helped
- Omission: consensus-building process is most valuable benefit (examine pros/cons tradeoffs)
- "Exceeded my expectations": bringing that many people together and then focusing on key issues.

Collective intelligence

- Process allows people to talk to each other. Realistic goals without going to TI, etc. Example is article in Electronic News: TI shipping .8 micron technology, everybody understood what was really going on - niche product - roadmap process gave participants behind the scenes view, allowed them to "talk around," sense of "rhythm" - benefits everyone. For example, 300mm not in rhythm (hardware and software). Provides sense of reality and community.
- Roadmap doesn't cause anything to happen directly. Collectively it's a compromise. What good is it? A process of collective intelligence. A "bar to beat" (like a pole vault bar). Set it, criticize/critique for a year, then sure enough collectively or individually companies respond to "beat the roadmap." Pull-in means not a failure, but we're smarter. But... it is likely that we might do it again.
- The Roadmap is not an exact science. Long lead times (1-3 years) plus lots of zeros in investment (long time to implementation): trying to guide with roadmap. Industry guided: universities, labs, consortia (shorter and shorter focus). Took not only divisions to break down individual companies, took our own government to break down government interpretation of

pre-competitive anti-trust legislation/legacy: had to undo. Now taking to another level at international level. We might naturally move into it without a lot of government involvement: engineering community just seemed to do it without a lot of resistance (real people in real companies sharing on real projects: can't abstract or generalize).

- The most useful part of roadmaps is getting people to talk to each other and share ideas about where the technology is going.

Forecasting

- Roadmap process is a lot like "making sausage" - decisions made whether right or wrong, really don't know at the time, but process is so public allowing freedom to agree/disagree and get to consensus - public consensus opens up the whole process (customers never generated consensus before the roadmap). Roadmap is also political - at least 2 roadmaps: one published, one not (embodies all discussions of dissent, other agendas, interests, etc.)
- Roadmap as a forecast: roadmap is a product of what the industry would like to do, but changes keep it "inaccurate" however a very useful forecasting tool. The purpose of a forecast is to have some idea of the future (e.g. turning on a light is a forecast, or a lion chasing a zebra). Some things are easy to forecast (turning on a light), others are harder (and usually wrong) - these are the ones that get criticized as "inaccurate." The purpose is not accuracy, otherwise companies themselves would have failed - look at new products introduced (were they accurately forecasted? mostly no) - seek right end-result. Application to roadmap: purpose is to narrow the possibilities of which directions to take - to be more efficient - the roadmap serves this purpose. As a forecasting tool, the roadmap has been "relatively accurate" - accurately focused on critical requirements like copper low-k dialectric.
- We benefit from the roadmap in two ways. One is simply that now we have a much better view - not necessarily a super accurate one, but overall much better view of which way the industry is likely to go - by reading the roadmap. The other one is really by participating in the roadmap - in the discussions - you benefit from other people's way of thinking about things. I mean, we are all presented with something - because people have a different view, a different way of looking at it. And it's just like when we go out to a technical conference, you're exposed to people’s thinking, and that benefits the company as well.
- Opportunity to stay current with technology developments (pretty good idea of where the industry is going).
- Early insights into future industry technology needs.

Builds trust

- 5-10yrs ago if you asked for a customer's needs, they wouldn't talk to you (too secretive). Build relationship of trust between user and supplier - roadmap helps provide context for these relationships (facilitates). Customers reference roadmap (e.g., "we're a year ahead of the roadmap"). Roadmap helps bring objectivity to discussions. Greatest benefit is getting together (continuous practice of improving) - starting to be viewed as credible.

Roadmap Process

- Insights which develop as a result of participation in the roadmap process are of greater value than the final document.
- Roadmap role today: benefit is in the process rather than the document.
    - gets experts in industry to sit down and think about where things are going - direct/immediate benefits to participants
    - benefit to non-participants: makes experts' knowledge available (public)

Other

- Additional benefit is broad usefulness of information. Example is university professor request for class use (online NTRS). Also media: Economist editor, writing "The Road to Damascus" inquired about copper interconnect, was directed to website, used as basis for article.
- In my consulting work I use it as a reference tool.
- Roadmap as a market of ideas: roadmap creates a market for technology development - is its own market economy, currency is ideas, motivation is self-interest.
- Roadmap process is one of the best ways to advance your career.
- Continual responsibility (continuity)
- Access to multiple technology roadmaps

14. Please rate your preferences for Roadmap participant communication.

Respondents were asked to rank order (1 to 5: 1 most desirable, 5 least desirable) the communication preferences listed below.

Preference	#	avg	# first	# last	rank
face-to-face	22	1.2	18		1
e-mail	22	2.4	4		2
teleconference	21	3.1		2	3
video conference	21	4.0		11	5
personal phone call	20	3.7		5	4

The mean (average) for each preference was calculated for the sample. Also a modal class for the first (1) and last (5) preference was tallied. The ranking clearly shows that face-to-face is the most preferred method, while video conference is the least preferred method. In discussions with respondents face-to-face, the traditional meeting method, was seen as successful but questions of practicality arose, especially as the Roadmap has become international. Regarding video conferencing, the perceived shortcoming seems to be a combination of limited access and technical constraints. Some indicated these conditions are improving, but presently are not sufficient as a viable substitute for face-to-face meetings. Similar to other rating or ranking questions, some respondents volunteered additional comments as follows.

Face-to-face

- #1, but not practical

E-mail

- more people involved
- best for 1-way communication
- absolutely - hold little virtual meetings, use mail lists
- tie w/ phone call, advantage is many

Teleconference

- advantage: put presentation on web (uploaded foils referenced), 6-8 people on the phone (10 people in conference room)

- yes - hear voices

Video conference

- video conferencing only works well when you know somebody really well
- disadvantage: have tried off and on, room has to be set up properly (very elaborate), technology not there yet, like "outside looking in"
- too hard
- usually disappointed - not much better than teleconference
- not really there yet: can't share graphics, poor quality of audio
- if know people's voices then don't have to see them - regularity precludes having to see people (if already known)
- #2, next but troublesome: incompatible, limited capability
- problem is limited access and high price

Personal phone call

- tie w/ e-mail, more effective but disadvantage is one at a time

Additional comments

- Teleconferencing because of time commitment, face-to-face only when necessary. Now that is going international, very tough to get these people together (logistically and culturally).
- For group communications: Face-to-face: 1, Video conference: 2, E-mail: 3, Teleconference: 4, Personal phone call: 5

15. How will you use the information obtained from the Roadmap process?

There were 23 total responses. Participants were asked to select among three categories (i.e., business planning, research planning, and new product development). A fourth category – *other* – was included to capture any additional uses. Almost half of these selected more than one use as follows:

Use	#	%	# first	% first
Business planning	13	34%	13	57%
Research planning	16	42%	8	35%
New product development	4	11%	0	---
Other	5	13%	2	8%
Total selections	38	100%	23	100%

Multiple selections indicate the diversity of uses of the Roadmap. Research planning was chosen the most often (42%) followed closely by business planning (34%). The origin of the Roadmap as a research planning tool probably explains the frequent selection of this category. However, if only the first choice (or sole choice) of the 23 respondents is examined, business planning was chosen first by a wider margin over research planning (57% to 35%). In fact, when business planning was chosen in combination with other categories it was always chosen *first*. This reflects the growing use of the Roadmap by a broader audience interested in business considerations such as strategic industry direction or competitive implications of individual firms.

Analysis of the comments offered reveals further evidence of the variety of business uses of the Roadmap.

Comments: There were 24 total responses. Participants were asked to specify *Other* category selections, but several offered additional comments in connection with the other categories. Further, some of these comments were taken from context interviews in response to the open-ended question. "How is the Roadmap used?" Overall, there was a wide variation in replies but some are very insightful.

'Beat the Roadmap':

- Original use of roadmap by research community to "solve" problems/challenges identified by roadmap, but actual use is short-term, business community uses as a benchmark to "beat the roadmap"
- As soon as you set a roadmap like that our first objective is to beat it. So that is like waving a red flag in front of Intel. They are going to try to be there before AMD and Motorola or else. So it is a challenge more than anything but I think the roadmap is useful because it provides an industry-wide coordination for suppliers and it helps set standards for equipment that makes suppliers' jobs much easier.

Business planning (other):

- The most useful part of roadmaps is getting people to talk to each other and share ideas about where the technology is going.
- Make use of roadmapping: common reference point, helped enormously in understanding direction of industry.
- [SM&E firm] is a services company (engineering consulting) - traditionally broad environmental mission, semiconductor new business niches.
- Coordinating supplier response especially to business issues.
- Equipment purchase specifications - from suppliers (particularly from research labs) will look to roadmap.
- Roadmap benefit is in strategic marketing. With decreased profit margins (reduced cost per I/O), increased risk of making a mistake forces standardization in the form of roadmapping. [Small firm] actively uses the roadmap to know what's coming so they don't have to guess (wrong). Smaller competitors aren't usually involved in process so can be 6mos ahead of them in strategic knowledge. Even customers that aren't members/participants are enticed to buy the updates - customer choice on the roadmap is a more informed choice than not.
- Semiconductor firms' customers ask to see firms' roadmaps so they get a comfortable feeling that the firm knows where it is going and that they have a migration plan beyond today's sale.
- The use of roadmaps has turned out to be important for suppliers who have to plan their own investments in technology.

Research planning:

- SRC: both on- and off-roadmap research (MARCO)
- SRC Strategic Planning Process influences long-term roadmap, couple SRC into longer-term aspects (10yrs)
- inform SISA members for their R&D planning

- don't do with roadmap per se, forecast near future but Government R&D budget not necessarily a forecast of exactly what's going to happen
- add "guiding"
- add technology planning
- some hesitancy from universities to stay on roadmap
- done way beforehand
- Classroom instruction and graduate student supervision: 100-125 Masters/PhD students, 8 students half-time, able to help the industry with a clearer picture. Research area includes Berkeley, Stanford, NC State. Students also use roadmap. Also included in Engineering course schedule as part of curriculum.

Other comments on uses/limitations:

- strengths: evolutionary, can't accommodate revolution (very few Einsteins)
- in university: roadmapping helps focus - analogous to teaching (focus/explain, learn by doing), also writing proposals (educational process) - have to explain it "reduce fuzz"
- Roadmap not "accurate" - changes over time, but used to communicate what's important.
- very important for future planning, less day-to-day (1-3yrs timeframe), gain insights (e.g., hi-k materials)
- in Sematech SCOE reviews, someone would always "get it wrong" from misunderstanding - roadmap reduces chances of failure or "getting it wrong"
- Roadmap is a "touchstone" - serves an important function in building consensus
- problem with roadmaps: consensus documents - good, but might miss something
- Final comment in response to science roadmaps: "Scientists generally are averse to following a 'well-worn path'."

How is industry roadmap used? (This question was asked in several context interviews)

Process technology development (within the firm):

- [Chipmaker] is an advanced, leading edge device maker (ahead of competition), thus they "lead" the roadmap requirements, don't use it as a guide (as other smaller "follower" device makers may, e.g., early foundries)
- but use it as a tool for development of tools, etc. to solve future problems too big for one company itself to address. Example is photolithography - chipmakers used the roadmap as an industry consensus that identified a future need for 50-70nm feature sizes that led to a consortium for EUV lithography development within the national labs.
- thus, the roadmap helps identify likely solutions, narrow-down options, and pool resources - even for leading chipmakers
- technology development groups (advanced manufacturing process) predominantly participate

Direction to suppliers:

- participants/users are both semiconductor makers and suppliers - equipment and information, academic/research communities
- first and foremost use: helps set suppliers' agenda - since development extremely expensive, share cost of development
- sets standards for equipment so don't differentiate between companies - very expensive - not sustainable (e.g., IBM special-purpose materials superior, but not cost-effective) - note that high-volume manufacturers compete on execution
- Interactive guide, real-time equipment improvement, guides equipment manufacturers to implement projects. Thrusts: interconnect, litho, factory integration - gives us and supplier community confidence. They know maximum stability, robustness.

Direction to research community:

- align/synchronize research agenda - both externally (universities) and internally
- industry roadmap enables "meaningful" (applicable) university research as researcher can "point to the roadmap" for guidance
- use research program to set agenda for roadmap itself (sort of feedback system)
- stage, influence initiation of research programs

16. Do you plan to continue your involvement in future roadmaps?

There were 25 responses with the vast majority (22) answering *yes*. The three who answered *no* did so either because their involvement was a one-time request or they had retired. The general sense is that once participants start in the process they usually continue. This is underscored by the longevity of the participants in the survey sample (i.e., average Roadmap involvement almost 7 years).

17. Hypothesis 1: The SIA Roadmap has contributed to a more regular, more predictable, and even accelerated pace of innovation through deliberate coordination of pre-competitive R&D and related industry resources.

There were 34 total responses to this question. They are categorized as follows:

Response Category	#	% of total
Agree	29*	85%
Disagree	2	6%
Other	3	9%
Total Responses	34	100%

* includes 2 strongly agree and 1 partly agree

These numbers overwhelmingly favor *Agree*. Perhaps more than any other single research question, respondents found strong association between the Roadmap and this variable under inquiry. Specifically, technology acceleration was cited most often as the definitive contribution of the Roadmap process. Even some of those classified as *Other* could be interpreted as somewhat in agreement. Those who explicitly disagreed cited specific situations that may or may not reflect an accurate perception of the overall purpose of the Roadmap. Some lengthy responses were broken up for ease of reading.

Agree that Roadmap has contributed to a more regular and accelerated pace of innovation

'Beat the Roadmap' behavior is often cited as central to explanation:

- Most have said that, if anything, it has accelerated the pace because it gives a benchmark, and right away people, with their competitive nature, want to beat it, so by constantly throwing it out there. We have an interesting situation though, because each year we make the Roadmap tougher: when we redo it, it gets pulled in, right? And then we have to beat an even harder goal. So it's a difficult environment that industry people live in - they all lament, "Oh God, I never worked so hard in my life!" That's an interesting phenomenon.
- Yes, and to the extreme, once milestones are defined, competitors attempt to design strategies to accelerate or 'beat the roadmap'.
- Yes, sure. by saying Moore's Law is going to happen, manufacturers will make it happen, thus always accelerating - writing it down, guarantees to be beaten.
- Yes, definitely pulled in pace of innovation ('beat the roadmap' behavior).
- Yes, has accelerated. Each company looks and tries to "beat the roadmap."
- Pull-in or "beat the roadmap" behavior the result of public knowledge of roadmap targets. Competitive firms trying to beat everyone else to the goal. Earlier targets, SRC goals, MT 2000, etc. not really public or adopted broadly by industry so largely ignored.
- Technology acceleration: result of roadmap. Take a lesson from roadmap: write it down, then someone says "I can beat that," accelerating the pace.
- Roadmap is considered a standard and provided "line in the sand" - leaders would "step over it" or beat the roadmap.
- Has accelerated pace of innovation: benchmark for IC manufacturers to beat.
- Roadmap is goal/need "scorecard." Chicken or egg: observing or driving. Contributed to our understanding of the pace and what drives it - identification of pace: best snapshot in time.

Other reasons were also cited:

- Unqualified yes, look at semiconductor industry before and after, can measure.
- Strongly agree - business issues, sharing knowledge (anti-trust laws relaxed), way industry works
- Agree. There is a sense that innovation is accelerating and one can argue a roadmap allows for coordination that assists in the innovation process. Key barriers, technology nodes, etc. all ensure the chip makers and their suppliers are on the “same page.”
- Agree. The very fact that the Roadmap tends to be over run at each edition is *prima facie* proof of its success.
- I agree, because the certainty of the requirements provided by the Roadmap eliminates wasted time in trying to determine the technology requirements before solutions are developed. Additionally the Roadmap allows for elimination of programs which obviously result in technology which will not meet the requirements thereby reallocating scarce research funds to projects of higher potential. Finally, the Roadmap, through its consensus building process, not only generates the requirements but also automatically communicates those requirements to the entire semiconductor community.
- Agree, provides a guideline for collectively concentrating resources to focus (e.g., SIA focus center program in response to roadmap challenges) or (earlier) international competitiveness (when all needs laid out collectively).

- With roadmap, tendency is probably to accelerate change. Without a roadmap, most people would still know, but a roadmap makes it more apparent/visible to everyone. Don't use the prior (older) technology. Lowering production cost: economic bias, equations lean to new equipment/technology. Shrinks will continue (need concept/ideas to continue).
- Agree. The ITRS covering the wide range of technology thrusts gives trustworthy impacts to semiconductor community.
- Agree - yes it is Moore's Law 'insurance' - more than Moore's Law.
- Agree: common vision, visibility of common metric yields guideline.
- Yes, to some extent, but we do not have the nonexistent case to compare to.

Disagree that Roadmap has contributed to a more regular and accelerated pace of innovation

- Disagree - the forecast of the introduction of 300mm wafers on a time schedule that the full supply chain could not support was a very destructive result of consensus based planning (as opposed to reality based). Technology acceleration has really been the result of individual leading edge companies serving their own needs.
- Disagree - roadmap is political, dominated by a few, very strong companies like Intel. Everyone knows this and acts accordingly.

Other factors

- ITRS doesn't so much do it. But sitting down and sharing does it. AMD doesn't like acceleration, whereas Intel and DRAM companies like Samsung do like acceleration. DRAM design features size: all people sit down and talk, even Intel couldn't do it by itself.
- I think the overall acceleration is driven by factors beyond the roadmap and the semiconductor industry. Society's thirst for information - lots of it and lots of it now & for free - and efficient communication are the real drivers behind innovation… behind the road map itself. Innovation is market driven not necessarily technology driven.
- Also other issues critical - compare rate of change between pre-Roadmap and now. Roadmap has accelerated process: undirected activity had direction with imperative (no one telling), sets up problems. Not intended as an instruction manual, to set expectations, sort of guidebook, establishes a framework.
- Design engineers in semiconductor industry more isolated from process and other functions than in other industries (chemicals, autos) - reason is time (compressed internet time) narrows focus, no time to share, thus have to stay on target.

18. Hypothesis 2: Although collaboration found in the Roadmap process is not new, the structure and methods employed (e.g., pre-competitive basis, broad participant network, process - not product - emphasis) are clearly unique.

There were 24 total responses to this question. They are categorized as follows:

Response Category	#	% of total
Agree	18*	75%
Disagree	4	17%

Not Sure	2	8%
Total Responses	24	100%

* includes 2 partly agree

Three-fourths of respondents chose *Agree*. Some common reasons cited included industry-level focus, breadth of participation, influential/prerequisite role of U.S. research consortia such as the SRC and Sematech, among other factors. Those who selected *Disagree* did not see significant differences, but a few of these were also not familiar with practices in other industries.

Agree that Roadmap process is unique, because of…

Industry-level focus including consensus on common goals:

- Yes, it is unique, because the industry is doing as a group what individual companies have had to do in their preparation for strategic planning, for their next year and "5 year" plans.
- True, unique problem: all disparate companies, equipment, and stuff. Normally don't talk to each other (like Ford and its supplier network). Need some way to get everyone together, so "orchestrate rhythm" to minimize risk.
- Yes, unique but for the greater good. Yes, we are sacrificing by sharing intellectual property, but makes everyone else (including themselves) better. Huge personal risk in sharing: Galvin/Noyce took first step to develop synergy.
- Correct, every company has its own roadmap. These are based mostly on in-company discussions. For example, Motorola won't normally bring in outside suppliers. Whereas ITRS, toolmakers involved, very open process, people are equally challenged. Example is 1997 NTRS: tool companies believed U.S. industry alone couldn't decide which tool to make. Thus expanded scope to international (ITRS). Very important: every company wants to understand what tool is needed.
- Agree, driving toward one goal.

Breadth of participation:

- Distinguished mainly by breadth of participation (suppliers, universities, etc) as peers, # companies involved, openness, now international
- Agree, the previous collaboration for Roadmap is rather limited within a sole technology thrust, e.g. Assembly & Packaging or CAD (Computer Aided Design).

Influential/prerequisite role of SRC and Sematech research consortia:

- Unique event among industries - unique because of Sematech (most successful consortium of government and industry participation). Pre-competitive communications changed balance of power - sat in conference room at Sematech (had to bring in lunch) with competitors - just getting to know each other. Turner Hasty (TI) ended up as COO - he and Bob Noyce set the "tone" environment. Very unique: AMD, Motorola, Intel all working for a TI rep plus consensus process. Sematech allowed you distance from continuous job/pay issue - more of a creative environment (more free to say what you feel) - plus consensus culture. This is all necessary background to roadmap, particularly international and international ITWGs.
- Agree, SRC/Sematech collaboration unique in the U.S. (Japan had already). Roadmap is a continuation of what Sematech already started.
- Initiated in SRC & then SEMATECH & then SIA Roadmap process.
- Agree, I think that SEMATECH had received DOJ permission to do this collaboration.

Other factors:

- Agree, these activities are done with much more conscious decision making.
- Agree, consolidated anonymous statements.
- Completely different (broad trend) than others (e.g., SIA pin count very specific: takes 2 years).
- Culture really matters. Can't really replicate in another industry.

Disagree that Roadmap process is unique

- They are less unique now.
- Not unique, but very good leadership tool.
- No, processes are similar to other institutions in the world of research.
- Disagree - do not see anything unique.

A few respondents were simply not familiar with other industries' methods:

- I have no knowledge of how other industries collaborate on technology forecasting.
- Haven't seen anything else - first one with experience.

Not Sure

- Not as confident about answering vs other industries, don't know of another industry that has organized itself this way. Roadmap, also research consortia more thoroughly developed than others: Sematech focus 1-3yrs, SRC 3-8yrs, MARCO focus centers 8+ yrs. Three coordinated research consortia organized in a thorough and unprecedented manner. Roadmap is natural outgrowth, but also reverse influence: roadmap helped expose MARCO long-term needs.

One respondent cited shortcomings in the process:

- Hard to answer, not aware of other methods. This process still has a way to go to become more efficient, quite a hierarchy in access regime (e.g., executives vs individual contributors), also tendency of roadmap process to giving squeaky wheel the grease (someone yells out about new data), consensus achieved but outliers (loudest voices) do affect outcome.

19. Hypothesis 3: The key driver for the SIA Roadmap has evolved from international competitiveness in the late-1980s to a global strategy in the late-1990s to stay on the industry's productivity curve as defined by Moore's Law.

There were 26 total responses to this question. They are categorized as follows:

Response Category	#	% of total
Agree	22*	84%
Disagree	2	8%
Other	2	8%
Total Responses	26	100%

* includes 4 partly agree

Respondents overwhelmingly stated *Agree*, but more for the latter part of the statement (i.e., *to stay on the industry's productivity curve*) than the former part (i.e., *evolved from international competitiveness*). Many were not familiar with the early history of the Roadmap, thus could not really provide a complete answer. Nonetheless, a wide majority see the Roadmap's purpose today as sustaining the industry's productivity curve. There is also increased acceptance of this mission as a global initiative.

Agree

- I agree there was a sense of urgency for the U.S. chip makers in the late 1980's. I remember being in graduate school studying semiconductor and electronic materials, then being informed the U.S. industry was in dire straits. I began to second guess my choice of career, but here we are in the year 2000 and the U.S. and, generally speaking, the worldwide chip industry is strong.
- Agree. In early versions this emphasis was fairly prominently featured.
- Fair characterization, underneath interest in global strategy, survival of enterprise is driver.
- Yes, again people have accelerated, as the period for generations was 3 yrs (DRAM) in 1992, and is now closer to 2 yrs. The business implications of this are particularly onerous.
- Right, yes. staying on productivity curve is the goal or destination, but see car metaphor: semiconductor industry being 12 sub technologies, view technology as a car, analogs of 8 or 12 TWG component industries - each roadmapping itself as if alone in ensuring Moore's Law (like each category is a one-stop shop, wrong approach), ITRS system drivers; DRAM, logic, SoC.
- Japanese market share objective: survival. Underlying goal to continue Moore's Law. Roadmap's purpose to get more coordination worldwide, among manufacturers and equipment vendors: to reduce costs, increase efficiency, set standards.

Supplier emphasis:

- Agree, guideline for equipment and materials manufacturer.
- True, took on a life of its own. Europeans and Japanese might have been envious - we have strong competitive advantage (Novellus, Applied Materials made inroads in Japan, now 40-50% of market), Europe lacks supplier infrastructure to do a roadmap, competitiveness of US suppliers helped by roadmap, Japanese domestic roadmap (subset of international) published in the fall (98).
- Yes, but wrong question - it's a false dilemma. It was INITIATED in order to make the USA more competitive on a global basis. But when about 50% of the supplier infrastructure is outside the USA, then it is an incomplete Roadmap if you leave their inputs out.

Partly agree:

- True, but only one of several drivers.
- Sematech did evolve from competitiveness, but roadmap reason was a bit different. NACS. In 1992 government approached SIA to quickly (6mos effort) help determine government support of research requirements, but wasn't getting consistent messages - asked SIA to get together and give consensus of research needs. Moore's Law reflects product's rapid pace of development. Hierarchy of what's important: 1) reducing cost/transistor gate, 2) scaling: feature size reduction, and 3) Moore's Law: # transistors.
- Yes, other driver: as technologies mature, investments required to advance further thus increasing complexity and expenditures. For example, litho used to be easy (used physical

masks). Now use invisible light, individual companies can no longer deal with these. Roadmap brings in collaboration.

- Combination of economic and technical factors. Also, realization that we're approaching fundamental limits of CMOS. Analogy of collective interest: we're all on the same planet/spaceship - purely selfish interest "we're all gonna die." Magnanimous desperation leads to extremely cooperative behavior. Roadmap not a substitute for companies talking to companies (can't be used as a crutch). Also not a substitute for going out and talking to customers. Some investors and individual companies have misused Roadmap as to what he (individual) needs.

Disagree

- Disagree, we needed a stronger unifying theme to guide the research and equipment development both of which were becoming more complex and expensive. The Japanese threat was one of efficient execution, not planning.
- Disagree, Moore's Law is an observation and an extrapolation, not a "Law" or even a forecast. The driver is the recognition of the need for continued increases in pervasiveness of semiconductor products to fuel global industry growth.

Other

- True, but for every activity there's an optimum thing. Feeling that we're beyond optimum today: too much detail, 75 tables vs 2 tables. Q: how many hours, time, $ does it take? 10x as much?
- Don't know about the beginning of the roadmap, but the biggest benefit of Sematech consortium has been to suppliers, especially Applied Materials. In a sense, U.S. Government subsidized Applied through Sematech.

20. Hypothesis 4: The SIA Roadmap has qualitatively affected R&D expenditure patterns of the U.S. semiconductor industry (emphasizing more "D" than "R"). In other words, the Roadmap has shortened the research agenda horizon.

There were 29 total responses to this question. They are categorized as follows:

Response Category	#	% of total
Agree	12	41%
Disagree	13	45%
Both or Not Sure	4	14%
Total Responses	29	100%

These numbers slightly favor *Disagree*, but they are basically split fairly evenly. There were actually more that indicated *Agree, Yes,* or *True* in the first word answer, but upon further analysis they either cited a reason other than the Roadmap for this trend or ended up arguing against the statement. For future research, response to this statement might be better asked on a Likert scale (i.e., strongly agree, etc.) than on a simple binary basis since there were varying degrees of emphasis in the responses. Some responses were lengthy and have been broken up for ease of reading.

Agree that Roadmap has shortened research agenda horizon

- Agree, most emphasis is on mainstream development.
- Agree, especially true at consortia (Sematech, SRC). Roadmap is first-order guidance. Influence is on suppliers.
- No longer a roadmap for research, but directives to suppliers - in the interest of semiconductor industry to keep up with historical productivity.
- Original use of Roadmap by research community to solve problems/challenges identified by Roadmap. Actual use is short-term - business community uses as a benchmark to "beat the roadmap."
- True, research in universities focusing on near-term things. There was more research emphasis and flexibility in the past. Research tendency is always on roadmap. If no roadmap then fight for funding, with roadmap then on-roadmap research, if new then must look at roadmap first.
- Roadmap stifles creativity: why work on something that says "solutions available." Problem is that it says or implies "we know." Lots of red space that we're already doing, but is not economical. No "clear space" since already feature size related. Implied solution by extrapolation: 1) cost, and 2) function (physics), will go in different direction if not met: "implied" as evolutionary. Example is DRAM: some shipping 1Gb 6yrs from now - much later than Roadmap. Materials/tools all don't work - "slipping" so Roadmap irrelevant.
- Before Roadmap (haphazard research) > Roadmap (synergy) > 2001-2003 > possible technology demand w/o capability because no current research. Roadmap never reflected reality: before erred on fast side (Concorde: every year faster and faster, but doesn't buy you anything). Like 300mm 1997 prediction, didn't happen and Roadmap lost credibility. Until now Roadmap very aggressive, but closer and closer we get to end we won't have equipment. Examples: IBM 248nm litho 15yr development, so used 193 - this is not possible again, copper at IBM since 1984. No one addressing post-MOS research. Litho one atom at a time not possible with the Roadmap cycle: don't want to say "no" or slow down. 50nm stated as far as we can go, but may not be.
- Agree. It is my impression the burden of research has been placed at the university level and much of the semiconductor specific funding seems to be directed towards more applied type research, less so for some fundamental research. Few U.S. chipmakers have internal research capacity, IBM and Lucent probably remain the exceptions. Sematech member companies rely on it to foster R&D. Also, the manufacturers are also placing more of the development burden on the equipment and material suppliers.
- Could agree in that roadmap very heavily planar, CMOS-centric - doesn't really mess around with non-standard CMOS technologies. This has enormous influence on research allocation. More D than R in the sense that roadmap remains in planar, CMOS domain.
- Concerned about "path dependency" of roadmap, same ingredients, etc - research "too far astray" doesn't get attention, there's comfort level with what one has experience in.
- About 1995, Jack Kilby criticism of Roadmap [from respondent who was at meeting with Kilby]: Roadmap is a focusing tool but with blinders on, may miss other opportunities/discoveries.
- Has to do with timing - gestation process: near term myopia (most activities within first 5 years). International process may balance short- with long-term needs - probably increase research focus (red space) - e.g., copper, low-k dialectric, new materials. Study of near- vs long-term focus (human nature and group behavior) - early meetings not very productive (when you first meet someone you talk about the weather, etc. - you don't talk about the future), thus a long gestation.

- Agree to some extent, since all business units that compete in the industry have their own view of what constitutes an appropriate mix of D and R.

Disagree that Roadmap has shortened research agenda horizon

- I disagree because I have seen no evidence of more research dollars (percentage wise) being allocated by industry. What has changed is the allocation of the research funds, which are available for research. Today the allocation is made with a greater intelligence and results in higher R&D productivity.
- Disagree fundamentally: unintended consequence. On the other hand, roadmap has prompted basic research (red space: don't know how to get there). Serious question now about what is beyond CMOS. MIT researcher believes that the best basic research comes from working on practical problems. Roadmap has helped focus industry research on CMOS, otherwise they wouldn't, galvanized people to look at issues.
- Look at nanotubes, NOT on roadmap, traditionally takes a generation for complete life cycle (idea to full-scale commercialization), industry has now discovered (IBM has announced device in the lab), thus innovation still happens.

Underlying reason is not the Roadmap, but general trend of reduced R&D:

- Disagree, there is very little R in this industry anyway.
- Yes, but that direction was set before the Roadmap process was started - it just reinforced that earlier decision.
- Roadmap just a book, more D and less R due to financial constraints.
- Agree / Disagree. Actually, the roadmap has a very far out horizon in an attempt to define research needs particularly in universities. In fact, more “D” than “R” happens, because that is directly funded by IC producers, and the sources of true “R” funds are scarce. Remember, we don’t have Bell Labs anymore, and IBM is not the altruistic think tank that it once was.
- That's true, but I don't blame the Roadmap for that. I think it's more the environment this industry lives in. Today market life cycles for products are very short, and they've got to hit those windows or they don't make any money. And so that drives the behavior which is afar from papers on fundamental understanding. So what's happened in industry at large is that horizons are shortened for research. They've got to deal with that. That's actually made places like the SRC more important. Usually if a TAB member or an advisory board member is down deep in the technology side, they are focused on that and are less likely to take the bigger picture - like "I'm trying to invent new lives for copper metalization." That's a very specific need that individual is very good at it. So that person is going to want to invent copper liners, he's not going to want to do anything else - that's his interest.
- This is true, and related to a strange thing. R&D is being reduced. Pure research is being very sharply reduced by those organizations that traditionally did lots of it. Bell Labs, Motorola, Xerox, TI, GE, IBM, etc. At the same time, the much lower overall R&D budget is being focused on ‘D’. The research horizon for ‘D’ however is conceptually being pushed out 14 years - which is probably longer than the traditional ‘R’ projects ever ran.

MARCO Focus Centers cited:

- There's more good out of the roadmap than damage - avoid more risk by paying attention to this than other, non-roadmap things. There's a net gain from on-roadmap research, SIA acknowledges risk as cost to bear, but outweighed by benefits. Example of research that

directly resulted from roadmap is MARCO Focus Research Centers (FRCs) to address long-term, non-roadmap targets with more freedom than before.

- On the contrary, the Roadmap has spawned new 'R' investments such as the MARCO program, which was designed because the Roadmap horizon was defining Research needs beyond that. This will swing the momentum to relatively more investments in Research as more and more red zones (areas of no known solutions) appear on the Roadmap.
- Not sure if agree: roadmap is a good way to understand justifications (e.g., MARCO, focus centers play important role), same for front-end processes (FEP) research center.
- Last program is MARCO - Roadmap outlines needs and weakly alludes to solutions.

Misinterpretation of Roadmap:

- Continuous concern with misinterpretation of roadmap: congressional staffers won't read details, uneducated person gets a false sense of security (that roadmap implies implementation/solutions). '97 Roadmap includes red/yellow colors, a significant improvement to identify obstacles. Problem of communication: just how much research needs to be done? Possibly change title name to "research projections" - roadmap not explicit enough - implies where technology is headed (misinterpretation).
- Misinterpretation: not trying to specify solutions, but needs - roadmap of needs - every solutions chart attempts to have alternatives - not trying to eliminate any particular solution. Overall message: don't want to stymie creativity. DARPA wanted to do something, but not on the roadmap (misinterpretation). Paradigm changes are difficult to capture (e.g., transition from multi-level layer interconnect to optical interconnect). Evolutionary trends and bias, not revolutionary - vague transition point with different type of solution, (e.g., optical to x-ray lithography) - this was predicted as early as 1985, now not going to happen because of lack of knowledge, but also extendability of existing lithography (well beyond earlier expectations).
- Have heard this argument. People in research community miss the color. Misinterpretation of "book": don't see red. Not worried about financial community which is companies' emphasis.

Both or Not Sure

- It has improved vision on BOTH. Yellow is “D” and Red is “R.”
- Not clear this is true now.
- Would say another way: if you are university doing research, you go to NSF, DARPA, etc. who will use the Roadmap. This is why university professors participate in the Roadmap. SIA Roadmap is a 15yr window versus Japan 5yrs, the longer years don't get that much attention. Nobody's really comfortable beyond 5yrs. Difficult challenges are laid out in two sectors: short vs. long term. Short term focus accelerates schedule.

21. Why has the semiconductor industry in particular embraced roadmapping so enthusiastically?

There were 31 responses to this question. Answers ranged markedly in reasons given including some lengthy responses that combined multiple reasons. Reasons were separated and organized by general category according to common themes. A total of 38 reasons by major category follows; first in summary, then in detail.

Category of Responses	#	%

Uniqueness of Moore's Law, rapid and regular pace of technological change	11	29%
History of planning (or lack of), common framework	7	18%
Need for coordinated approach	6	16%
Economic scale	6	16%
Stage of industry life cycle	4	10%
Unified response, common needs	2	5%
Opportunity to focus research effort	1	3%
Confidence in overcoming technical challenges	1	3%
Total responses by category	38	100%

Uniqueness of Moore's Law, rapid and regular pace of technological change

- Pace of change very fast.
- No other industry evolves so quickly, yet so predictably (Moore's Law).
- Rapid pace of change, if you don't have a willingness to adapt roadmap frequently, you will die. Semi industry unique, without precedence - some similarities, but nothing with same productivity curve, no other industry.
- I can tell you, everyone knows what the clock frequencies are going to be next year, they are driven by Moore’s Law scaling curve. The industry has been driven by technology evolution more than by product evolution alone.
- Because industry has a unique technology that has advanced as rapidly for so long, produces at any one time alternatives to solve problems.
- A formal recognition of history 1960-1990; uses this (Moore’s law) as guide to planning. Other industries do not have such a clear model, nor are they as viciously competitive.
- Because it has Moore's Law as an economic statement of intent and it used the Roadmap to try to influence U.S. Government support. Now the Roadmap is to guide suppliers and the university research community.
- Driven by the cost and complexity of the technology as well as the rapid rate of change in introducing new technology nodes.
- History of technology progression (Moore's Law) so clearly documented, rate of advance/pervasiveness astounding: DRAM unknown 10 years ago (high-tech term only). Hi-tech vocabulary now known by stock market (great visibility). Technology has progressed so rapidly, trends exponential in line width, density, fab cost, etc.
- Moore’s Law productivity gains are becoming increasingly difficult and costly to implement, yet these productivity gains are essential to industry growth.
- Roadmaps are a new phenomenon and they are very particular to the semiconductor industry as I am sure you learned. The process is probably not as easily extendable to others and they are even problematic in semiconductors given the speed of change and our ability to keep up with that speed of change. And also not have everyone spend 200 percent of their time doing roadmapping. The flat panel display industry tried to mimic and didn't do quite as well.

- History of planning (or lack of), common framework
- Roadmap actually countercultural (not a natural industry activity) - began in U.S. sitting down and looking around (e.g., MITI) doing plans, thus we had to.
- No, did always look forward, maybe not to detail.
- Because the industry is notoriously bad at planning and this gives a common framework.
- It gives a standard framework against which to benchmark the whole business enterprise. Then, strategic competitive plans are catalyzed by asking how "our company" can contribute, or do better?
- It is a strong benchmark for all segments of the chip industry's supply chain to work from. It allows companies to better prepare strategic business plans based on up coming device generations. For example, suppliers can target R&D expenditures to meet a future requirement and, therefore, have a window of opportunity to introduce a new material or piece of equipment.
- It reduced mis-information.
- It has proven to be the best tool we can find; it brings a reasonable degree of order to what could be a chaotic set of options in many technology areas.
- Because people like standards against which they can measure.

Need for coordinated approach

- Semiconductor industry has unique aspects - created a need for roadmap, also made it what it is: can't make any changes in industry without integration of disparate companies. For example, I-line 248nm to 193 requires exposure tool (6 companies), resist technology (3 companies), mask technologies (2-3 other industries) to pull off this change.
- Industry and university synergy - Sematech first got started, ETAB and supplier involvement - first 2-3yrs Sematech synergize with supplier industry (Applied talked with Intel, TI, etc). Before Sematech, talked through supplier, afterwards directly via Sematech pre-competitive communications.
- Probably from desire to avoid wrong investments in tools and manufacturing, though this is less the case now with more diverse participation.
- This industry has pre-competitive consortia (e.g., I300I). International Sematech truly historic - inside Sematech 3 people - I300I Munich - unique international consortia, fairly young industry, really big since 1980s (last 20yrs) - communication itself: almost bootstrap/enabling technology.
- Also, semiconductors depend less on manufacturing skills to achieve competitive differentiation. Therefore the climate for collaboration has become much more favorable.
- A semiconductor manufacturer can no more control the supplier industry.

Economic scale

- Industry at top, costs escalated so rapidly that survival is emphasis (economically driven) - leads to pre-competitive pooled resources, International Sematech (SRC also). The problem

has gotten too big for one company to pool resources to stay on curve - need to coordinate/control costs.

- See Dan Hutcheson article in Sci-Am re: immensity of investment, complexity much greater, very unique industry, successful.
- Because manufacturing facilities very expensive, can't afford to have factory without full tool set. Could be even only one or two tools missing. Who put up first 6" or 8"fabs? Wafer size changes are big changes. IBM introduced 6" 150mm, Intel 8" 200mm, both really in trouble with this, so expensive.
- With the investments being considerable (currently $1-3 billion for new fabs) and materials approaching ultra purity levels, the roadmap in a sense forces a degree of standardization with materials and processes. Not that each chip maker's process is a carbon copy of its competitors, but the industry tends to select a "winning" solution that results in a degree of standardization.
- Greater efficiency needed – competitiveness
- Needs to restrict R&D expenditures, budget constraints.

Stage of industry life cycle

- Automobiles are marketing driven while integrated circuits are not. Therefore, if you are driving something from a marketing perspective you have what is traditionally called a marketing roadmap. They do not have any real technical context. This looks good, fine, but what is behind it? So to the extent that roadmaps are still driven by technical and engineering considerations, then they will probably continue to exist. But if the industry turns into a commodity type industry and becomes more marketing driven then I think technology roadmaps will probably outlive their usefulness. Thus, part of my answer to your question would be as long as we continue our current technology driving force, we will continue the roadmap process.
- Mature industries (e.g., chemicals) have leisure of history, whereas semi industry dynamic and global (practiced around the world), qualitative differences.
- Semi industry economic model very different than other mature industries: chips or computing (use) technical problems revolutionary (e.g., new materials).
- International meetings - more tech conferences/academic flavor compared with auto, steel, other mature industries.

Unified response, common needs

- In the 1980's the U.S. semiconductor industry was faced with the fact that they were losing share of market to Japanese companies and made a significant joint effort to re-establish technology leadership. To do this they established SRC, SEMATECH, and facilitated the National Advisory Council to the President on Semiconductors. Unfortunately all three of these entities, acted independently, approached the U.S. Government for funding to solve this research dilemma. Each was asking for substantial government funding, each claimed they had the solution, but each had a different approach. The Government came to the SIA and told them they need to present a unified front to the Government. An industry taskforce was established chaired Bill Howard to propose ways to "speak with one voice". I was on that taskforce. The output of the taskforce was a report (the "Howard Report") which

recommended, among other things, a continuous roadmap. The SIA implemented this recommendation.

- Reason: heavy/expensive manufacturing technology, many elements common to all, suppliers are glue, solutions need to be common (15 companies all doing CMOS process - all multi-billion companies), suppliers feeding industry. Common needs.

Opportunity to focus research effort

- It may be that the existence of the Roadmap gave industry the confidence that a tightly focused effort that brought in results early would be more beneficial than one that broadly and blindly sought research into the unknown. The Roadmap gave them the promise that they wouldn't be 'blindsided' by something that was completely unanticipated.

Confidence in overcoming technical challenges

- Agrees with "confidence" in psychology of industry members to overcome sometimes insurmountable challenges - strong sense of "we will beat this" attitude, historic characteristic. Past measures of success include transition from NMOS to CMOS and Intel's DRAM to microprocessor decision. Industry thrives on (solving) crises.

22. In what ways is the Semiconductor Technology Roadmap process unique as compared with other forms of technology planning for an industry, including other industry roadmaps?

There were 23 responses to this question. One respondent simply said, "It was the FIRST industry-wide Roadmap in the world. Question: Why didn't we do it sooner?" Similar to other questions, answers varied widely. Responses were organized into major categories as follows; first in summary, then in detail.

Category	#	%
Role of research consortia	6	27%
Pre-competitive (common) technology requirements	5	23%
Comprehensive scope of involvement	5	23%
Multiple reasons	2	9%
Other reasons	2	9%
Not sure if unique	2	9%

Role of research consortia

- The SIA Roadmap was the first industry roadmap and therefore was totally unique. Since it became successful, it has been emulated by many other industries. However, its process for consensus building is still unique. This is due to the industry having the SRC and SEMATECH entities, which other industries have not emulated.
- What's happened to this industry in the last decade: the consortia, the cooperative, collaborative kind of process is really unique - it's a unique sociological design. It's helped make this creativity public in a sense. In fact the industry has learned that by sharing their challenges, their technical challenges that they all commonly face, there's not much loss to

any one of them in doing that. And that by collectively thinking about them, they can be overcome. The SRC has had a big role in that - the first one of these formations.

- Sematech preceded MicroTech 2000, allowed common knowledge as mutual benefit. Sematech culture contributing factor: often TWG co-chair from Sematech.
- Hunch that the SIA Roadmap is unique because of high degree of other consortia involvement (NEMI, ITEC, etc.)
- Any other industry dealing with technological progress in a similar way? Data storage industry is moving much more rapidly than semiconductors. They have developed a roadmap, but haven't taken the next step (no SRC, etc.).
- Centralized corporate research and government funded research (the Vannevar Bush model) are giving way to collaborative research models that require collaborative planning mechanisms. Other industry segments have a slower rate of technical change and are slower to adapt their planning to this new model.

Pre-competitive (common) technology requirements

- It may have been blessed by the DOJ ruling that they could collaborate and not be in restraint of trade. It may also benefit from the early and strong perception that R&D actually created this industry and so was a perceived essential value to it. That would mean that organizing this research effort would be very beneficial.
- General idea of identifying common needs, pre-competitive technology roadmap (not many like this in other industries).
- Large number of things pre-competitive (e.g., chip production) - unique design now competitive.
- Whether or not this is different from other industries, the process has helped participating device producing companies understand that their competitive differentiation occurs in the design and application fields far more than in manufacturing.
- I just attended a telecommunications workshop on what are called IP carrier networks. The telecommunications industry is trying to bring a new technology into the basic old switched backbone. And they don't have any sense of that common technology push that we do in this industry. Maybe the problems are harder, I'm not quite sure why but I was struck by the fact that I don't think those guys could do a roadmap. It's something different - it's just interesting.
- "Moore's Law"

Comprehensive scope of involvement

- Worldwide consensus base, covers almost all semiconductor technology thrusts, updated annually.
- All major semiconductor companies are involved.
- Guideline covers equipment supplier down to product planning.
- Others don't go through complete tool set. Roadmap really makes sure that process is manufacturing ready: alpha/beta/manufacturing tool sets ready in sequence.
- Before roadmap: each US company (TI, Motorola, etc) would look ahead couple of years, but little interest down the road (long term focus).

Multiple reasons

- Three reasons: 1) breadth of participation - broad "forum" to get folks together, 2) voluntary (vs internal company planning), 3) international collaboration unique
- Uniqueness of the process (people, consensus-building, etc.); driven by industry, not universities or government: all are committed; roadmap is "unique experiment that's never been done before."

Other reasons

- [Balanced structure] Structure, diverse involvement (universities and suppliers), no one company dominates, roadmap is a consensus document, Intel not driving roadmap, made special care not to have more than one TWG member per company - added different suppliers to force balance - thus very balanced TWG.
- [Planning necessity] Like Cheshire Cat in Alice in Wonderland: if don't know where you're going, which way should you go? Have to have a juncture, path, map, time-scaled branches (e.g., 29% annual cost/function reduction).

Not sure if unique

- I'm not sure - it would be good to talk with auto or airplane, but since the consolidation is so mature there, it may be more difficult to find analogues.
- No idea - don't know if it is.

23. In what ways has the Roadmap influenced technological innovation in the semiconductor industry?

There were 25 responses to this question. Similar to other questions, answers varied widely. Responses were organized into major categories as follows; first in summary, then in detail.

Category	#	%
Enabled industry consensus of major technology needs	7	28%
Accelerated pace of innovation	4	16%
Made possible efficient use of R&D and other innovation resources	4	16%
Improved innovation planning	4	16%
Increased coordination and timing of innovation across material and equipment supplier sector	3	12%
No or possibly negative effects	2	8%
Other	1	4%

Enabled industry consensus of major technology needs:

- It has established industry consensus on technology barriers and communicated these to university and industrial researchers.

- Focus of key technology driver (litho etc.).
- Standardization and concentration on mainstream solutions.
- Focused industry on potential roadblocks.
- Points out what requires people's attention - attention triggered along "red bricks" - affected direction.
- One significantly contributing factor to highlight needs and problem areas, and finding solutions sooner than expected.
- By giving consensual information.

Accelerated pace of innovation:

- Accelerated
- It has accelerated the technology compared to Moore's Law" (2yr cycle vs 3yrs)
- Pulled in technology in time - advanced linear pace of technology (e.g., copper around a long time, now just getting around to it)
- The roadmap and innovation: The roadmap emerged (grew out of) CMOS and Moore's Law scaling. The roadmap probably has quickened the pace of innovation by focusing collective attention on technology needs in order to continue historical productivity gains.

Made possible efficient use of R&D and other innovation resources:

- Drastic productivity improvement. Not that this wouldn't have happened anyway, but with focus more cost-effective.
- In many cases, it has lead to more “rifleshot” rather than “shotgun” planning activities for R&D.
- Stopped/mitigated work on not-needed technologies.
- Provided tools, students, and new knowledge which has been key to the continued evolution of the industry.

Improved innovation planning:

- Influence of people of having agreed-to target to beat (puts a stake out there). R&D managers get roadmap and assess targets: a) get reps together and ask questions: is it feasible? how did consensus come about? how did decision get made? who decided this? One input might share "we're ready to introduce this next year" (vs 2yrs) or unanimity around the table. Sanity check (reading between the lines). This is the value of participating, then b) compare to internal company roadmap.
- Two types of innovation: 1) incremental innovations along timelines/characteristics of roadmap (Moore's Law), 2) areas of no solution (red), so-called black space: 15yrs out - industry starting to move off-roadmap investment (focus centers) new ideas, alternatives to CMOS processing. SRC funds on- and off-roadmap research (e.g., quantum mechanics) - little room for innovation on roadmap, really bend over backwards not to pick winners.

- Roadmap looks out beyond 5yrs, we need that. So far CMOS only, now talking about post-CMOS. What after copper? Superconductor? Some kind of divergence beyond 5yrs. 15yr timeframe helps this.
- Not innovation so much as its exploitation. Can plan better.

Increased coordination and timing of innovation across material and equipment supplier sector:

- It has enabled new equipment to be available when needed. 2. It has pointed out the timing of the exhaustion of a particular approach, e.g., the replacement of Cu/ low k for Al/ SiO2.
- Roadmap pulling everyone together (resist, mask, exposure tools, calcium fluoride, other materials): integrate timing of supplier availability, IBM: 200mm with 5" tools, needed 75 different tool families. Catch 22: no one wants to invest until the market there.
- It provides goals and objectives for when the industry needs to satisfy the requirements of a given device generation. Investments and R&D can be earmarked accordingly. It is difficult for a supplier to introduce a new material or process tool (equipment) for an existing device generation. By planning according the roadmap, however, a “new” supplier can use a technology change to establish a position in a market segment it never competed in before. (By “new" I do not necessarily mean a company “new” to the semiconductor industry, but a supplier that targets a new process or material market segment to expand its market presence). Again, material and equipment suppliers are expected to deliver process solutions that the chip makers can “plug in” at a given device generation; therefore, companies at this tier of the supply chain now have a greater investment burden. There seems to be a greater degree of consolidation, particularly within the equipment industry, as the chip industry has matured and has advanced to finer device geometries. A given equipment market is typically dominated by one supplier with a couple other suppliers having a smaller presence.

No or possibly negative effects:

- No idea - don't know if it has.
- You hear both sides of this, including assertions that the roadmap has stifled innovation by predicting too much.

Other:

- Need time to think about this from a post mortem point of view, without giving our or other's future strategies away.

24. Do you think that Moore's Law drives the Roadmap or is it the other way around?

There were 30 total responses to this question. They are categorized as follows:

Response Category	#	% of total	% head-to-head (M vs. R)
(M) Moore's Law drives Roadmap	12	40%	55%
(R) Roadmap drives Moore's Law	10	33%	45%
(N) Neither (Moore's Law is observation)	5	17%	---
(B) Both (too interrelated to distinguish)	3	10%	---

Total Responses	30	100%	100%

These summary numbers give a slight edge to Moore's Law as the primary driver, but there is no consensus of view. What can be surmised is that the two factors are very closely intertwined. This was also a question where there was not much indifference in the replies: many responses contained explanations, some extensive. Extracts and analysis of responses follow.

Moore's Law drives Roadmap

The most direct argument refers to Moore's Law as a basis for Roadmap creation, which contributes to its attainment. Interestingly, a credible alternative assumption has not been developed:

- The Roadmap process always assumed the linear extrapolation of Moore's Law, and as such creates a self-fulfilling result. Early critics of the roadmap process said the process was flawed because no maturing or saturation of the metrics was comprehended. Alternately, the RCG could not take any responsibility for modifying the 'Law' or they could not invest in the analysis of predicting a maturing.

Many respondents simply agreed with the statement without much explanation. A few respondents used terms like 'overarching' and 'fundamental' to emphasize their point. The term "self-fulfilling prophecy" was echoed here and elsewhere.

- It is an overarching metric - Moore's Law makes the roadmap possible.
- Moore’s Law is fundamental to continued growth of the industry, it therefore drives the roadmap.
- Definitely the Law drives the Roadmap.
- Moore's Law drives - industry decided on the foundation for it - other way around based on cost.
- Yes, Moore's Law drives the roadmap. Self-fulfilling prophecy, and business demand now.
- The observational trend of 2x productivity every 18mos keeps industry going. Semi industry averages 14-16% compound annual growth rate, thus to maintain must continue Moore's Law.

Some referred to the symbolic, even religious importance that Moore's Law holds within the industry:

- Yes, Moore's Law is the input. Moore's Law is an important symbol to the industry - we'd be embarrassed if it was not met!
- Moore's Law is almost a religion - this religious fervor drives the industry - what to do if it stops?
- How to stop measuring per Moore's Law (density)? We can't really. Moore's Law is a very powerful force.

While agreeing, some respondents called for a revision to Moore's Law or an altogether different measure as a better metric in the future:

- So far answer is yes. In the near future, it will be difficult to keep up with Moore's Law.
- New version of Moore's Law (different) needed, pace of shrinking transistors will slow (traditional scaling principle). 'Functional' density basis of productivity/learning curve: may be different measure. What are we progressing for? Molecular switches 10^{-23} single-electron transistors?

- Roadmap itself envisions the end of "classic" Moore's Law within present scope (15yr horizon). Running off the end of Moore's Law may *force* the industry to mature, because it can't count on exponential improvement to sell its products anymore.
- Moore's Law impact on industry: similarities with Henry Ford's business model: lowering cost/car will expand market was true roughly into the 1930s, then learning curve bottomed out and car costs started going up. Ford refused to see this while Sloan's value model at GM became the norm. Will this happen in the semiconductor industry?
- Economics playing a bigger role (moving off Moore's Law). How many factories can industry support? Compare impact of industrial structure (e.g., GM, Ford, Chrysler) ala Intel, Motorola, TI.
- Recent change in Moore's Law, now 4-5yrs: Gordon Moore stated during July 2002 White House Presidential Medal of Freedom Award.

Other interpretations and considerations:

- It is an algorithm for growth, but putting as a target, there's a better chance of meeting it.
- Keeping industry together is like herding cats, it's almost impossible, so you use Moore's Law.
- Competition (Moore's Law) drives the roadmap.
- Note that U.S. doesn't have a monopoly on Moore's Law - Japan is just as committed to it and in fact even more regimented.

Roadmap drives Moore's Law

These responses were more straightforward. The majority of respondents who saw the Roadmap driving Moore's Law cited a more consistent rationale—the purpose of the Roadmap is to sustain Moore's Law:

- Gordon Moore said at the very first SIA Roadmap workshop (1992) that the purpose of the roadmap is to continue Moore's Law.
- Earlier (1992), Moore's Law drove the Roadmap, now the Roadmap is driving—more appropriately sustaining Moore's Law.
- A Roadmap goal is to sustain Moore's Law.
- It seems to me the roadmap was established so Moore's law would stay on track.
- Roadmap attempts to perpetuate technology trends in cost/function, scaling, chip size.

A few other respondents viewed Moore's Law as an observation of an historical trend that was descriptive but not prescriptive or predictive:

- Moore's Law derived from history (trends), then companies said we need to keep pace with it, now a 'law'. Roadmap says this is what's needed to maintain it.'
- Moore's Law not a law of physics, so other way around. Moore's Law is descriptive (observation of industry): just happened that it moves that way.
- It is the other way round. Moore's law is not a law but a result.

One respondent saw the Roadmap as accelerating Moore's Law, which brings with it both challenge and opportunity. This is also addressed in the first hypotheses question (Hypothesis 1):

- The overall criticism is in accelerated pace of innovation: roadmap has taken all the gains

from productivity and moved down Moore's Law faster (every 2 years) than earlier (every 3 years) - thus we'll bring in or 'hit' the wall sooner than expected and haven't really invested in long-term research. But... the industry's mentality has traditionally been one of quick response: if technology nodes are pulled in, then the sooner we hit the wall, the sooner we'll deal with it.

Neither (Moore's Law is an observation)

Most of these responses are similar to the classification and the previous one (Roadmap drives Moore's Law) as they underscore that Moore's Law is but an observation. However, these remarks do not acknowledge that the Roadmap *per se* is the driver. The last response stands alone, making reference to the "Beat the Roadmap" behavior discussed by many respondents when answering other questions.

- Neither. Moore's Law is an observation of behavior.
- Again, Moore's Law is an observation; the driver is the desire to continue the spectacular growth of the industry, and this is done by dramatic reductions in cost per function resulting in pervasiveness of IC products.
- It is not a driver but a best historical fit/observation, but serves as a goal line.
- Only as a good historical metric. Not really feature size, but how much you can squeeze.
- 'Beat the roadmap' is main reason it changes: self-perpetuating acceleration. Intel wants to 'push' suppliers as fast as possible.

Too interrelated to distinguish or both

Finally, this could easily be called the "not sure" category, but both factors seem very important.

- It's the carrot before the horse, but the horse often wins.
- Interactive cycle: observation > mantra > justification for investment > hope/expectation. Belief: if I do this it will happen. Chicken vs. egg - doesn't really matter. Analogy: like A to D converter with feedback in steps.
- Both perspectives are important and feed off each other.

25. In what ways has the Roadmap influenced corporate strategies and public policies for the industry?

There were 26 responses to this question. Since it combined private and public institutional changes (corporate strategies and public policies) many respondents only replied to one element. When respondents did respond to both, the general perception was that corporate strategies were affected by the Roadmap, but it was less clear whether the Roadmap had influence on public policies. Further, this question elicited different replies dependent on when respondents were involved in the Roadmap. For example, the U.S. Government was the catalyst behind Micro Tech 2000, and continued as the primary audience of early SIA Roadmaps (e.g., 1992 and 1994 NTRS) for the express purpose of determining R&D funding. Over time government-funded R&D was curtailed (e.g., elimination of DARPA funding of Sematech) as the industry itself replaced the government as the primary Roadmap audience and user. The 1997 NTRS and subsequent editions of the ITRS clearly demonstrate this. The maturation of the industry has also played a role in this as reflected in the following analytical response:

"It may be that the fact that the Roadmap has accelerated development and this development has created very wealthy companies, which has encouraged the industry to look away from government funding and more to its own internal funding of development (e.g., the dropping of DARPA funding for SEMATECH)."

Despite the difficulties just discussed, an attempt was made at separating the responses into the two major categories (i.e., corporate strategies and public policies) along with two other entities mentioned that were influenced by the Roadmap (i.e., universities and industrial research consortia). Responses were organized into these categories as follows; first in summary, then in detail.

Category	#	%
Corporate strategies	21	62%
Public policies	9	26%
University research/teaching	2	6%
SIA, SRC, and Sematech research strategies	2	6%
Total responses by category	34	100%

Corporate strategies:

- Corporate strategies yes, public policies not sure.
- Most semiconductor corporations use the roadmap as a basis for their strategic planning.
- By identifying technology barriers it identifies market entry opportunities for semiconductor manufacturers and also semiconductor process and test equipment suppliers.
- The companies that have seen the greatest value from the process have discovered the value in, and the need for assigning top notch people to represent them in the roadmapping process.
- It allows corporations to prepare strategic business plans accordingly to meet specific future technology and process requirements.
- Awareness of technical issues needing advanced development support.
- Focus on process technology progress.
- Streamlining of research and development activities.
- Used national roadmap to drive [material supplier] strategic development plan. It is also used by key customers (chipmakers) in a similar way.
- If you want to invest in a new fab, the Roadmap is in the public domain. Not everyone agrees with it, but can reference it - both device makers and tool makers together. Sematech stays 1 or 2 years ahead of Roadmap because alpha and beta tool phases.
- Moving R&D out of companies into universities. Also increased communications.
- "The purpose of the roadmap is to beat it." It sets the bar/benchmark. Fundamental driver: Moore's Law insurance, substantial increases in productivity (30% reduction in cost/function). Has continually created new demands for communications (e.g., digital cell phones), continual progression of new applications spawned by silicon.
- Corporate strategies: stay even with industry.

- Sharpens focus on next 5 years, especially helpful for suppliers who otherwise get differing views from every customer.
- Mechanism by which people ask for capital and labor for investment, research resources, enables discussions at various levels. "Can't blame it." Provides a discussion for agenda, can't substitute for actual dialogue with customers.
- Leaders try to beat the roadmap.
- Corporate new product strategies.
- VARIES A LOT on corporate strategy.
- More or less, yes. Hasn't yet produced noticeable effects. First reaction: lot more detail than they thought about - a lot of information.
- Corporate strategies: don't have steadfastness of industry (does this mean roadmap's involvement of others - national labs, universities, etc. - brings more perspective???).
- Mistakenly drove 300mm equipment R&D too early.

Public policies:

- Long term view of requirements also allows the industry to recommend directions for government funding of research at various universities.
- Government R&D can do a lot. Also SIA Board very proactive in S&T Policy aimed at academic community (vs industry direct funding). Roadmap is very useful tool to describe what research needs to be done. Nanoelectronics research needs document (beyond roadmap proposal) and this and Roadmap combine to identify problems, thus very good understanding of what the problems are. Use these documents to try to get funding. Industry internally funding about $200M (e.g., SRC, Sematech), lobbying hard for additional funding for physical sciences. SIA focusing on NSF and DoD basic research budgets.
- BIG influence on Government viewpoint on industry technology. East vs west coast: Semi industry (west coast) doesn't tend to look to government for support. Their response is different (i.e., industry roadmap) than other mature industries (autos, steel, etc) - proof is how other industries have copied the Roadmap: semi industry is trail blazer of roadmapping.
- Public policies not sure: NIST, ARPA budgets - hasn't influenced policies, but organizations.
- In the process applying governmental funds. [Japan]
- Public policies: government cooperator and at times enthusiastic participant - more on government involvement: NSF committee, DoD committee, Norm Augustine Defense Science Board, Sematech, OSTP, Commerce, NIST - okay, Energy (Deputy Undersecretary) - diverted a number of times, National Labs. Government has become sideline player - DoD's role much diminished over time - technology policy occurs when a crisis.
- Policy: 1992 great importance (government requested). Now nothing positive, may have been negative: presence of roadmap means maybe don't need help. Also, problem in misinterpretation of "red."
- Concerns about government: never held accountable (in an industry sense) - self-perpetuating motivation without regard to accountability.
- The government decreased support for the industry because 'Roadmap' implies no new knowledge/science is needed

University research/teaching:

- Public policies: don't know, but for universities - what's needed, where industry/technology going positive influence to target research. Also included in teaching - part of engineering course curriculum.
- It influences university research and to a certain extent, the research supported by Government agencies.

SIA, SRC, and Sematech research strategies:

- Don't know of anyone based solely on Roadmap or Sematech - only if they have a bona fide customer (e.g., lots of companies interested in 300mm, but then a recession). Sematech and SRC (research community in general) decision whether new technique/tool to be used can only be made by someone using it (e.g., plasma deposition proof/demonstration of concept: cost 10x as much to prototype) SRC wanted to decide which ones to test, but they weren't the right organization, must be individual companies in industry. Must be compatible with other technologies, also must be economical - only industry can do this implementation: Intel and IBM have funded litho external but nothing has come of this. '94 Roadmap: chart on R&D, production monies spent - dilemma: only so much money to spend - by and large most monies spent by industry on next 2 generations, thus industry can't invest in all far-out technologies (e.g., industry consortia sponsored different NGL options: Intel, Lucent, IBM/Motorola).
- The SIA board and the Sematech board take recommendations from their members, based upon a summary analysis and launch new directions and new programs that are policy driven. In Feb 1993, a Sematech board launched a silicon-systems thrust initiative from a recommendation that was conceived from the 1992 roadmap which recognized that Sematech was not covering vital areas such as Design, Test, Packaging, Materials, 300mm, TCAD. In the next operating plan 1993-94 new programs were launched. In 1995, the crisis of interconnect and lithography areas spawned MARCO driven initiatives to address the roadmap needs near the roadmap horizon. In 1999, the Roadmap will call for several critical needs, these are all materials research related, and may launch new research initiatives that are materials focused.

26. Can you think of alternative ways that would be effective in obtaining the information contained in the Roadmap?

There were 17 responses to this question. Several respondents gave no answer to this question. Further, the answers given were generally brief. The vast majority of respondents felt there was NOT a feasible alternative, thus those who did not respond may have reasoned that no answer meant "no" by default. Responses classified by answer were as follows:

Answer	#	%
No	11	65%
Yes, but limited alternative	4	23%
Yes	1	6%
Other industry roadmaps	1	6%

No:

- No [without comment: 4].
- No - especially to collect a wide range of information through 12 working groups.
- No - this is the only way to get a single industry map.
- I don't see any alternative that provides an overview to the same kind of accuracy.
- Off-hand, no (e.g., textbooks expire when published). Roadmap is a living document. Semi industry holds conferences, but not the same. Roadmap activity more organized, complete form, culmination/compilation in conference or workshop focused solely on roadmap.
- Not as effectively as the Roadmap.
- None that would be as effective, nor as reasonably free from anti-trust and restraint of trade issues.
- I think that we saw a floundering around of research and development before the Roadmap was created. The alternatives would probably be much less efficient.

Yes, but limited alternative:

- There are other ways - but they would have taken much longer to produce the same results.
- Would be very different, have to go to each company individually. For example, Applied roadmaps only for device makers, Intel product roadmap for its customers (PC makers), not really technology.
- Literature search could collect part of it, but would lack "intelligent compromise/consensus-building."
- Benefit is collective intelligence, no other alternative effective in collectively arriving at same point (very inefficient method if rely on natural forces: market inefficiencies, incomplete information). Economic market system criticism, supplier criticism: "Ole Boy System" selfish motives, value market inefficiency "can't fool all the people all the time."

Yes:

- For an equipment supplier, direct communication and collaboration with the semiconductor manufacturer remains the most important means of obtaining roadmap information.

Other industry roadmaps:

- Different technical organizations, societies (MRS, IEEE…SPIE, ECS) may have their own roadmap committees that provide solutions for the roadmap needs or could be some kind of branch (science or engineering). Why would any other process than the one being used be wanted? I suppose that if there are imperfections in the roadmap process, those who recognize the issues may drive the process for getting the information in other ways.

27. How does the industry know if the Roadmap "works" and how is success measured?

There were 26 responses to this question and answers varied considerably. One respondent simply stated, "There might be a lot of different ways you could answer that." Indeed, the purpose for the loose wording of the question was intentional in an attempt to explore the key success factors of the Roadmap as deemed by respondents, most of whom are active participants.

Although a large number (more than one-third) of replies could not be categorized – thus were classified as *Other* – some patterns did emerge as follows:

Reason	#	%
Sustained and accelerating pace of innovation	6	23%
Forecast accuracy	3	11%
Timing	3	11%
By achieving it	2	8%
Extent of research initiated	2	8%
Other	9	35%
Not clear	1	4%

Sustained and accelerating pace of innovation:

- The industry defines success in the achievement or over achievement of the pace of technology advances defined by the "technology nodes." In general, the market conditions have allowed technical success to be accompanied by financial success in these achievements. If the need for technology applications were to fall behind the rate of technology acceleration, this trend could be reversed.
- The success of the roadmap may be measured by things like economic indicators, such as industry revenues, price per function of logic and memory, cost to produce, etc. over time. I have not seen an effort here, there needs to be one. One concern is that our industrial semiconductor army outruns its supply lines (because of the roadmap) and we are left with a chronic over-capacity (driven by litho shrink capability now and 300mm in the future) and that supply is always ahead of applications. So the industry has done such a good job that it has worked itself into a commodity-only economic environment.
- We don't … or do we? How do we know? How WOULD we know? Why did we "Beat the Roadmap" on 250nm node? Why did we have to "pull-in" the Roadmap nodes from 1994-1997 Roadmap? On 1998 update? On 1999 IRTS?
- The roadmap appears to be on track and, in fact, it has been pulled in some as the pace of innovation has increased. Obviously, all parts of the supply chain seem to be meeting the roadmap objectives. This is not to say there have not been hurdles and perhaps some wrong turns along the way. Also, there will always be obstacles with the various supplier-customer relationships.
- Staying on Moore's Law successfully. Meets identified needs.
- If we maintain the technology pace with no stumbles.

Forecast accuracy:

- Measure reality against forecast and expect reality to beat forecast.
- Come back a year later and see if we beat it. Used in trade conferences, for funding allocations on red spaces, identify critical projects, stay on Moore's Law to give customers 2x functionality on a regular basis. Giving customers more for less: this has been fundamental. Leading edge drives technical capability, everyone else drafts behind. We measure success by growing at regular rate. Job is to keep it going, knowing paranoiacally that it only works if

everyone works together. Industry growth math: 1.59 (cum annual unit qty growth) x .71 (cum annual unit price reduction) = 13% annual industry revenue growth.

- By 1997 we had to be at X, then compare actuals. Earlier roadmaps more conservative, 94-97 actuals showed industry made faster progress.

Timing:

- The fact that equipment and processes are available to bring in the fulfillment of needs BEFORE they are projected is the measure of this success.
- Tools and process/device solutions delivered when needed.
- In time availability of equipment, and continuing progress in productivity.

By achieving it:

- "We've achieved it!" - industry-wide acceptance - identifying boundaries along the way, set of needs.
- There might be a lot of different ways you could answer that but I suppose the simplest answer to that is that we've achieved it. It's something that industry-wide is accepted and achieved. That would be one way of arguing that it works. And along the way we've identified barriers, things we've had to overcome and we do! That's what the Roadmap is - a set of needs and assessment of what we know about them - how we're going to do them. And historically we've been able to achieve those.

Extent of research initiated:

- No official measure, but if projects are started to address the “red” areas (or effort is increased on these), this is a good indicator.
- One way is to measure the progress against key technology challenges identified in the roadmap, and the extent to which collaborative research and development has been spurred by the roadmap document.

Other:

- By reaction given by relative industries.
- Not a numerical measure. Gets people together to understand different area of technology, breaks down silos.
- I had a professor in college who was asked to define “Hi Fi.” His answer was, “Hi Fi” is whatever makes you pat your foot. The definition of a “working Roadmap” is a roadmap to which everyone is dancing. When they stop dancing, the roadmap is not working.
- Testament of success: no Japanese crisis.
- Reasons for success of roadmap: focus on central core of technology (CMOS), rational question, constrained, Moore's Law, very focused. Got lucky, but not perfect. Packaging/interconnect/IPC tougher issues (lots of diverging views, different players).
- SIA Roadmap ROI of $640 million: before/after roadmap look at industry - roadmap process is key factor in accelerating rate from traditional 3-yr cycle (before) to 2-yr cycle (after) - the 1

yr savings of industry R&D is overall benefit. Compare with "cost" of roadmap: # people participating and involved (amount of commitment on their part), value their time (conservatively), travel, meeting costs, etc. then compare cost/benefit (economic analysis). Key assumption: roadmap only new variable in the mix. Conclusion: roadmap is a useful process.

- Difficult, success by going to follow through, more successful coordination/communication with vendors, more focused on critical areas. Each company to be on the trend to beat it. If no roadmap, each company's cost would be "hell of a lot more" - much more difficult to stay on Moore's Law.
- Success: suppliers pay attention.
- Growth rates

Not clear:

- Unclear

28. Is there a relationship between the SIA Semiconductor Technology Roadmap and corporate roadmaps? If so, is there an underlying structural hierarchy among these roadmaps?

There were 21 responses to this question. Better than 80% see a relationship between the ITRS and corporate roadmaps, however there was little response to the underlying structural hierarchy inquiry. One respondent replied that there did not appear to be a hierarchical relationship, however many indicated the use of the ITRS as a benchmark to surpass. Regarding *No* answers, none were really outright no responses but a clarification of differences in processes. Specific comments follow:

Answer	#	%
Yes	17	81%
No, or different process	4	19%

Yes:

- There is a relationship in that corporate roadmaps are no doubt compared to the ITRS, but there does not appear to be a hierarchical relationship.
- Yes, semiconductor manufacturers should answer for themselves, as for suppliers, our technology roadmaps are designed to anticipate future needs, we are targeting specific solutions to the yellow and red zones.
- Yes. ITRS is consistent with other roadmaps like Assembly & Packaging and CAD (Computer Aided Design).
- Yes, there are the very leading edge companies that fully intend to stay ahead of the roadmap, and there are more conservative companies who will minimize risk and R&D expense by staying (intentionally) one half or even a full technology node behind the roadmap.
- Yes, high-level starting point, not end point. In fact, one contributes to the other (bottom-up), real-time/interactive. Logic gate length driving ahead of photolithography - not just DRAM: feedback successive.

- Yes, the SIA Roadmap is timed to reflect leading-edge companies' Roadmaps.
- Yes - leaders (TI, Intel, NEC) marshal forces to beat it.
- Sure there is, managers would want to know why.
- My experience is that corporations use the SIA Roadmap to prepare their internal roadmaps.
- Most companies adopt the SIA roadmap as their own. But keep in mind that this is a roadmap of needs, not solutions. The Company Roadmap also has to include a heavy emphasis on the Technology Solutions. Here the company has to pick winners and losers. But the real solutions have to be picked by the purchasers, not by committee. Where the SIA roadmap addresses technology requirements on standalone basses, the company has to implement an integrated manufacturing process in which the individual technologies are compatible and which is economical.
- If not, that corporation has a problem with developing products too soon or too late. There is no structure - just common sense and good management skills
- Many equipment supplier roadmaps are directly linked to the ITRS. How do we enter new market segments? Red wall: a time when industry threat (by incumbent supplier) is also an opportunity (new venture or new market segment) - helps level playing field.
- Companies generally try to set their Roadmaps at least as aggressive as the ITRS in their targeted areas of competence.
- Firms' inclination: benchmarking opportunity and networking with peers. Most companies have own internal roadmaps.
- Every company has a roadmap and decides to be ahead or behind. For example, Intel Litho Roadmap.
- Usually they try to anticipate the Roadmap.
- Loose coupling - internally we focus only on key issues important to our particular set of future products and technology areas where we are weaker.

No, or different process:

- We did an “AMD Roadmap” in 1995. Not since.
- SIA is a consensus. Corporate roadmaps can be more specific.
- ITRS roadmap is a generalization and consolidation of company specific roadmaps.
- Company/single organizational roadmaps (e.g., labs) - narrow participant, whereas ITRS participants are entire industry.

29. What are the major advantages and disadvantages of an *International* Technology Roadmap process as compared with a *National* Technology Roadmap process?

There were 34 responses to this question. Several responses gave both advantages and disadvantages. Further, some gave multiple reasons. For this analysis combined replies were separated and classified as follows. Note that even after this breakdown, advantages perceived by the respondents almost doubled the amount of disadvantages stated.

Advantages	33	65%
Disadvantages	18	35%

The detailed findings of both categories follow, preceded by summaries.

Advantages of an *International* compared with a *National* Technology Roadmap process:

Reason	#	%
Global technology and industry	10	31%
Broadened involvement, scope, and cooperation	7	21%
Worldwide consensus	6	18%
Diverse technologies	5	15%
Added knowledge	5	15%

Global technology and industry

- It is a recognition that our industry is global. I see no disadvantage.
- An ITRS is a much more realistic way to address a GLOBAL industry.
- Semiconductor industry is a global player and thus requires international support. Challenging goals need to be affordable: this can be achieved more easily by international cooperation. Markets and thus market requirements need to be considered on an international basis.
- Globalization/international trends ties with roadmap. Japanese have done roadmaps for years (done in Japanese language). Semi/Japan "cost-reduction" forums mid-90s with Japanese firms, but narrowly focused on factory costs. ITRS didn't seem that contentious - now a very global industry (look at global makeup, suppliers global, (TI market 1/3 in Europe and Japan). Could have been a Japanese or Korean or Taiwanese roadmap, but wouldn't have coalesced.
- International roadmap is a good thing: technical issues are common (electrons don't know cultural boundaries), Internet is like the railroads of a century ago: compress time and space. Roadmap in the future: more inclusive, more participation, more consensus (international device makers and tool makers) - Infineon, TSMC, etc. felt intimidated at first, now more comfortable. Sematech initially US-only charter - purpose was to beat the world, won the battle, then implemented "Marshall Plan" by creating International Sematech. Roadmap can't be domestically controlled: since roadmap is market for ideas, questions whether SIA should be roadmap sponsor - TSIA, other international groups - maybe International Sematech should be coordinator
- Important that roadmap move with technology trend around the world.
- To make ITRS (international roadmap) work, need international community involved. Gone well so far - including Taiwan and Korea.
- Roughly half of semiconductor equipment is foreign made. Major benefit is to supplier food chain … we need all of it.
- The fact is we are in a global economy, and more and more chip makers are outsourcing production to foundries and assembly houses overseas. Equipment and material suppliers are expected to provide global support. Japanese companies remain the leaders in various segments of the electronic materials markets.

- Sematech freed from government funding in order to pave way for International Sematech, industry has gone global in many ways making it very hard to work within national constraints, e.g., major battles over European litho company (ASML) trying to work with Intel and U.S. National Lab, divergence between national interest and corporate interest (e.g., Intel) led to Sematech non-government charter, then International Sematech, then ITRS, reflected in most recent ITRS with separate goals for memories, logic, and microprocessors.

Broadened involvement, scope, and cooperation

- As cost of R&D gets higher, roadmap will gain in importance, solidifying need for international involvement.
- Drives industry to more aggressive targets, levels the playing field
- Greater influence, carries more weight.
- Greater pooling of resources and coordination to contain exponential cost increases.
- ITRS: "natural extensions" all these things happen (cooperation) at the "right time" - interdependencies huge, worldwide change occurred politically, economic progress well underway, structurally ready (e.g., IBM, Intel, others already multinational), not just individual companies but strategic alliances and partnerships - relationships already there. Appropriate awareness that you've got to be a cooperative team player in the country where you operated (sometimes legislated).
- International Sematech and Roadmap: good to do it internationally, tools are so expensive, suppliers can't afford to develop new tools without a global market, good companies are also good globally.
- Technology Roadmap driven activities help global collaboration in R&D across country borders (i.e., NTRS -> ITRS).

Worldwide consensus

- Worldwide consensus.
- A world wide consensus on requirements.
- Worldwide perspective, global participation.
- Now a global consensus rather than just US.
- Still broader consensus.
- Feels pretty good job building consensus: common bond/interest, breaks down inhibitions, built trust and confidence.

Diverse technologies

- The balance of adding a memory component, which was not present in the NTRS.
- It becomes less likely that one semiconductor manufacturer will dominate the roadmap process. Also different global regions broadly represent different industry segments i.e. DRAM manufacture is concentrated in Korea, foundry manufacture is predominantly in Taiwan and Singapore.
- Japanese are very good at packaging (e.g., 2lb Sony laptop)
- In interconnect, Japanese still ahead, but U.S strong in metalization (microprocessor needs vs. DRAM), copper (IBM), and chemical mechanical polishing (CMP), also IBM.
- Worldwide participation brings new perspectives, example: DRAM - first ITRS (1998) weak in DRAM, Micron only U.S. producer, DRAM content strengthened through Japanese and

Korean participation. Reverse example: SoC - brought more attention/emphasis to SoC (U.S. already there but other regions able to benefit from knowledge)

Added knowledge

- More intelligence
- Some argue different ideas on broader needs from different countries.
- International is a better "standard."
- More sharing is better, more productive in setting right targets - not stuck on past paradigms.
- Bring up good arguments, broader base of discussion.

Disadvantages of an *International* compared with a *National* Technology Roadmap process:

Reason	#	%
Logistics more difficult	7	39%
Cultural differences complicate process	6	33%
Loss of competitiveness	4	22%
National security risk	1	6%

Logistics more difficult

- More bureaucracy.
- More people to convince, more difficult process.
- Greater difficulty in maintaining consensus building: non-linear confusion factor.
- Always have the danger of committees designing camels instead of horses - the bigger the committee and the more language problems, the uglier the result.
- Logistics hard, different time zones, payback enormous, risk: being derailed by UN-type of problem (influence of veto).
- The learning process is slow, not yet well-absorbed by the new players.
- As roadmap gets broader in scope, then harder to serve everyone's needs (different segments, families of devices), getting "pretty unwieldy now" - really three different roadmaps: memory, logic, microprocessor, "going same place, but at different speeds" - roadmap becomes more of a map vs. a "trip-tick" (one route).

Cultural differences complicate process

- Complicates process (e.g., language).
- Cultural styles make it a challenge too - e.g. US vs. Japan.
- Difficulty in communicating/working together, lack of a common national purpose.
- More difficult to get consensus. Note: in reality not consensus, but compromise, e.g., technology "nodes" terminology vs. Japanese "generation." What year .13 micron? 2001 or 2002, compromise - not necessarily, Intel "technology leader," others try to slow down roadmap.

- It is hard for the Japanese to sign up to participate in a roadmapping process driven by Americans (or anybody non-Japanese). This is culturally almost impossible for them to do, but they are doing it. So even the Japanese are changing and have been bought into this process. They are doing it because they can't survive without doing it. They are willing to give information and are full-fledged participants. You should see their information. I mean one of the concerns over going international was political and all that. But beyond that it was just the logistics, you know, because you don't have enough time to meet, and now you are going to have more people involved in the process. The Japanese in general are more methodical so that much more deliberation is required and the process becomes even more timely and complex. I think the next version of the roadmap will assimilate those kinds of inputs much more easily because they will use different processes to get there. I think that we are going to learn from each other about how to do it better. The challenge is that everyone feels it is important to do but we are going to have to continue to improve the process.
- Japanese example of international barriers: Japanese decision-making process very different than U.S. "let's cut to the chase" method. A certain level of frustration is built in.

Loss of competitiveness

- Suppose one could argue that the U.S. may forfeit some competitive advantage.
- Concerned about international involvement: competition ("trying to do it better" incentive) is essential to innovation - competition in technology is key driver; if everyone participates, then no competition - can't have a big "love-in."
- Lots of debate on national vs. international - Japan 25-30% of market, hard to ignore a big player, but international focus may dilute effectiveness/substance of roadmap and tendency for a "split" with other country roadmaps - need driver like SIA. Similarly, are we better off with "competing" roadmaps from different countries?
- Competition tougher internationally for U.S. companies.

National security risk

- There may be a long-term strategic risk militarily in going with an International Technology Roadmap process.

30. Name two (2) strengths of the SIA Semiconductor Technology Roadmap process.

There were 27 responses to this question. All but a few listed two responses while a couple listed more than two. There was wide variation in the wording of individual replies but patterns clearly emerged to allow classification into major categories as shown below. In several cases a stated strength could be considered in more than one category, but the most likely one was selected. Thus the actual percentage breakdown by category might be different if reconsidered. Even so, the two most-cited strengths were:

1. Collaborative, democratic, and consensus process
2. Broad participation

Strengths Category	#	%
Collaborative, democratic, and consensus process	17	34%
Broad participation	12	24%
Organized structure	6	12%

Focuses effort on technology needs	4	8%
Coordination/pooling of resources	3	6%
Widespread communications	3	6%
Other	5	10%
Total all categories	50	100%

Collaborative, democratic, and consensus process:

- Process is structurally democratic
- Collaborative learning
- It provides a non-competitive environment for collaborative discussions of technology issues.
- Consensus building
- Social agreement
- All parties are on the same page.
- Expert consensus
- General consensus found
- International consensus involved
- IRC and TWG consensus usually achieved without requiring a vote
- Roadmap enabled agreement of huge brick wall in interconnect - need new ideas (MARCO start-up team) - participation as members.
- Process develops clearly defined targets. Those targets that survive the consensus process are likely to be real.
- Reaching consensus
- Fundamental fairness by including everyone in a balanced way, opportunity for equal representation (avoids railroading).
- Part of "3 legged stool" like government structure, each coming in with a selfish desire, but with checks & balances: not just manufacturers on TWGs, but suppliers.
- Open discussion – everybody has equal voice, Intel not only voice, not like U.N. Security Council (minority voices), inside companies you are inhibited.
- Set yellow and red parameters based on "best judgment" (no known criteria available) using a consensus process via strawman proposal (sometimes offered by chair).

Broad participation:

- Broad participation
- Broad participation: international, IC makers, suppliers, universities, etc.
- Widespread participation by device producers
- People (many and right balance)
- Communication is forced between competitors

- It gets suppliers and customers on the same wavelength
- Coverage from materials to design
- Near-term and long-term aspects
- Suppliers, IC manufacturers, universities, national labs all come together
- Experts from different areas/companies
- It is a collaborative process involving university researchers, semiconductor manufacturers and semiconductor equipment suppliers.
- Diagonalized matrix: the idea of the diagonalized matrix is that we can all work independently in our boxes or “silos” with a minimum of interaction and the whole will turn out right. As the technical complexity increases, there are more “cross terms” that reflect the interactions between the boxes that must be addressed if the whole is to turn out right. This means that we either have to re-diagonalize or determine how to get better interactivity - metaphorically speaking, that is. Design has a large impact on process and the constraints of both have an effect on production and product performance, etc.

Organized structure:

- Structure
- Structure (framework)
- Organized
- Annual updating
- A very well organized infrastructure for group work – conferences, workshops, use of web based technology, modern production (of documentation) methods.
- TWG Chair really plays facilitator role to keep process going when there is a lull, ensures that decisions are made on each parameter/characteristic of tables.

Focuses effort on technology needs: (4)

- Focuses researchers and developers on industry needs.
- Investments can be better focused to meet technology needs.
- Identifying roadblocks (e.g., the present concern with short gate length).
- Has to be driven by manufacturing need (cross-productivity focused) vs. suppliers' supply.

Coordination/pooling of resources:

- Equipment/process standardization
- Overall, reducing cost: helping to gain better efficiency in coordination/expenditures.
- Better relations/communications, pre-competitive pooling of resources.

Widespread communications:

- Maximizes industry communications

- Communication among suppliers, manufacturers, researchers
- Well known among industries

Other:

- Biggest benefit is synchronized individual roadmaps through individuals networking.
- Assurance of need to equipment suppliers
- Roadmap is a "good thing going" like UN, but not a panacea
- The roadmap becomes obsolete the moment it is published. But that's the good news.
- Paolo Gargini very effective in personal diplomacy role

31. Similarly, name two (2) weaknesses of the SIA Semiconductor Technology Roadmap process.

There were 42 responses to this question which is considerably more than the previous "name two strengths" question. Furthermore, several respondents provided more than two answers, bringing the total weaknesses listed to 91, almost double the total of the strengths list (50). There was even a wider variation in the wording of individual replies compared with the previous question. However some patterns still emerged allowing classification into major categories as shown below. In several cases a stated weakness could be considered in more than one category, but the most likely one was selected. Once again, the actual percentage breakdown by category might be different if reconsidered. Even so, the two most-cited weaknesses were:

1. Stifles innovation or emphasizes only incremental innovation
2. Participation inadequate or imbalanced (especially supplier community)

One point worth noting is the unmistakable influence the 300mm wafer diameter transition had on the overall credibility of the Roadmap and reflected in these responses in particular. The 1994 NTRS had projected the need for 300mm wafers by 2001 while the 1997 NTRS accelerated this requirement to 1999. The key driver for this was the trend in increasing chip size. Implementing a new wafer diameter necessitates an entirely new tool set and in fact, a new fab. This is a very costly venture (some have estimated the total cost of 300mm transition upwards of $10 billion industry-wide) and the burden lies heavily on the tool (equipment) maker. Two factors had changed that had profound effects on the 300mm transition schedule and neither was captured in the Roadmap process. The first was more technical: the slowing down – and eventual stopping – of chip size increases. Developers realized that the decreased reliability and other practical trade-offs that came with larger chip sizes led to severe scaling limitations so more emphasis was placed on "shrinking" device feature sizes to keep pace with Moore's Law. The second and more important factor was economic: an industry downturn that had started in 1996 had hit its trough in 1998, causing chip makers to scale back or entirely scrap plans for retooling or building new fabs. Many suppliers went ahead with development of 300mm tools (according to the Roadmap schedule), but chip makers instead "stretched" the use of existing tool sets vs. replacing these tools with new ones. The result was a significant production overcapacity by both device makers and suppliers, and increased tension between the two industries in search of an explanation. This problem was front-and-center when much of this research was conducted so

this flavor (i.e., #2 weakness: participation by supplier community inadequate) is very evident. Since then the issue has been resolved and the Roadmap process is better for it.[1]

Weaknesses category	#	%
Stifles innovation or emphasizes only incremental innovation	18	20%
Participation inadequate or imbalanced (especially supplier community)	15	16%
Roadmap term misleading or misunderstood	12	13%
Narrow (vested) interests sometimes prevail	9	10%
Process becoming too rigid, bureaucratic, detailed, cumbersome, costly, etc.	8	9%
Economics (costs) not considered	6	7%
Process not consistent	6	7%
Forecast inaccuracy (too aggressive or not aggressive enough)	5	5%
Consensus hard and may produce mediocrity	3	3%
Limitation of volunteer participants	3	3%
Other	6	7%
Total all categories	91	100%

Stifles innovation or emphasizes only incremental innovation:

- Absence of suitable marketing that prompted universities to be concerned that the Roadmap would curtail innovation, but it can be used to do the opposite.
- I sense anything more than 2-3 years out on the roadmap is in a way speculative. Competing technologies can emerge that provide different solutions creating new market opportunities.
- It tends to focus our research on a straight line extrapolation and discourage so called disruptive branches as being diversionary.
- Reduced discovery and learning about alternate approaches
- Stifles desire to do fundamental research - grants earmarked for on-roadmap research.
- Too predictive
- Roadmaps must know problems, can't roadmap unknowns (paradigm shift), but "normal" science things like human genome.
- General criticism (from US TWG meeting): roadmap emphasis on incremental changes - no radical changes (job security?)
- Leads to short- vs. long-term focus (as opposed to on- vs. off-roadmap choices) e.g., litho as a silo: people devoting all this effort to what litho option (out of 4 or 5 alternatives), conventional approach frames the question (e.g., litho): "how to *print* 10 micron features?" begs a litho answer (or Moore's Law answer), but if question is addressed in terms of price/performance parameters, then opens up other possible answers, e.g., quantum computing.

[1] The consensus is that the Roadmap *per se* was not the "cause" of the 300mm early transition problem, but a contributing factor.

- "Mindless extrapolation" view
- Criticism of roadmap: people not looking at broader context: other solutions exist (than just smaller transistors).
- There are other solutions that could get more functions with the same cost. Some place we arrive at the "great wall" 2001-2005, hopefully don't crash into it. Making smaller transistors not the only measure of success! DRAM > microprocessor feature size, while real issue is function (functional scaling).
- Most serious criticism heard is possibility of squelching innovation, but roadmap process tries very hard to avoid this (curtailing innovation) by leaving open goals as long as possible, but at some point you have to decide on options.
- Another major weakness cited by critics is that the roadmap doesn't consider alternatives to silicon CMOS - has no direct evidence but suspects it's very hard to obtain non-CMOS research funding.
- Reference Christensen's "Innovator's Dilemma" - roadmap very good at evolutionary, not "disruptive" innovations.
- Might miss something through risk avoidance: if $100 million to spend, where to spend it? On what you know best.
- The roadmap, I'll take lithography as an example. We try to reach consensus on those tool sets that will be best for each technology generation. We are technology experts if you will, we don't have business people in those meetings. Therefore, we all try to reach consensus on a priority of technologies for each generation that are the best, rather than stepping back at say three or four generations, and asking is there a technology that will be optimal over four generations? It may not be best for each one, so which is better I don't know. But our approach I think it's a potential weakness. I see us at looking at one generation at a time.
- 300 millimeter wafer issue: That is one of them. See, in many ways in my mind 300 millimeter should not even be in the roadmap. Because in a sense that making things slightly bigger, you are not talking about scaling things up by huge amounts: scaling from 8 inch to 12 inch - it is a more challenging way to do it - the cost may be dear, but it is not really a technical issue. It is more an engineering and economic issue rather than technical issue. It is a challenge but it is not really a fundamental type of thing that you want a professor to work on. What you want the professor to work on is that simply how do you design the process, make plasma etching more uniform, period. Then it's up to the specific tooling company to simply say, "how uniform is uniform now? 1 inch, 5 inch, 8 inch, 12 inch, or 24 inches?" But I want the professor to simply work out and tell me how sensitive it is to the area. I really don't want the professor to design for me exactly something for 12 inch, right? When you think of it in that way, we accomplish the job. The purpose of the roadmap: funding the professor to work on things of interest to the industry, but not holding the professor responsible: "hey, how come I don't have 12 inch by such a date."

Participation inadequate or imbalanced (especially supplier community):

- Many global regions have not participated very effectively.
- Strong dominance of a few American companies even if they are not leading companies (DRAM).
- SEMATECH domination
- Poor participation by Korea (where more IC production occurring in Asian-Pacific region)

- Still very American vs Asian-Pacific countries flavor (foundries)
- Global focus stretches bandwidth of domestic needs (better job planning)
- RCG too heavily weighted to chip companies, no outside advisors, thus problems like 300mm can arise.
- Focus on litho
- Don't actually have balanced representation (but process allows it)
- Not enough participation from suppliers. "Nuts and bolts" not getting enough research (proportionate to impact), SRC is looking into this now.
- Increased message of needs to suppliers
- Does not have adequate supplier input.
- Suggest 2 Roadmaps: Part A first 6yrs for supplier community, Part B for universities/basic research community (7-15yrs out) - suppliers don't care.
- Limited supplier involvement (old problem, but still exists). Since limited number of suppliers represented on TWGs, only large companies will send reps (smaller suppliers can't afford to participate). Recognize that supplier industry is less mature (more competitive) than device makers. No consensus on pre-competitive areas, fewer standards, "20 years behind" culture.
- DRAM not served well until recently so didn't enter into picture (1999 Roadmap started this discussion). Chip size: DRAM aggressive requirements.

Roadmap term misleading or misunderstood:

- Name (Roadmap): misleading (as if we know exactly where we're going) - proposed a few years ago a different name "Challenge."
- Roadmap title misleading, although states research needs more and more (focused more on problems with no known solutions).
- The term Roadmap does a disservice to the research community.
- The term "roadmap" is a little bit misleading.
- Misunderstood as a “forecast.”
- Misunderstood by Government as a *fait accompli*.
- It tends to give the impression to academics that all of our real research has been done and just filling in the blanks is needed from R&D.
- Implies known, predictable, "going to Santa Fe" prescribed route.
- "Roadmap" misunderstood: think it's filling out forms. Dates back to TI's OST (Objectives, Strategies, Tactics) also MBO - obsession with forms, mechanical process without thinking.
- Make sure roadmap used properly: to define needs and potential solutions (not the only "route" to take).
- It can also be binding for researchers. The word "roadmap" carries with it implicit belief that you know where you're going and how to get there. In fact, for many of the technologies we have to invent, we don't know. And so I have always felt that it somewhat overstates the state of our knowledge. And faculty sometimes chafe at it because you know 'it's hard to get students interested because, see there's a roadmap, that means you don't have to do anything'.

- From people along the front line, when we first did the MicroTech 2000, and then the first official SIA Roadmap - and when the roadmap started to be called the *national roadmap* many of the professors were very upset. The reason being, "wait a minute - if my idea of solving the problem is not contained in the roadmap, NSF may say you're not proposing something that industry recognizes to be an acceptable solution. Therefore, your idea is not supported." It's not so much they don't want to fund - any funding agency: the manager - if they fund something not contained in the roadmap, he has a lot of explaining to do. On the other hand, if he simply checks out the roadmap book he can say "the industry says so, I cannot be wrong." Right? And even today there are a lot of people saying that - in a sense that indeed, if you take it so literally it can be very confining. So the way out of that, and unfortunately it's not captured all the time and it's not explained well - we keep saying that, "look, the roadmap should be used to highlight problems, but *not* really solutions."

Narrow (vested) interests sometimes prevail:

- In some times, rather political intentions are involved.
- Potential to load the map with issues from those with vested interests or an agenda, but with broad participation this is hard.
- I think suppliers further down the supply chain are not always (seldom) included in the process at the early stages.
- Lack of meaningful (that is, listened to) supplier input.
- The belief that consensus on the part of device makers is equivalent to pointing to the direction in which technology will go - for example, the 1992 forecast that we would be seeing widespread use of X-Ray lithography long before now.
- High emphasis on high performance microprocessors
- Consensus sometimes loudest voice vs rational voice
- Misuse of roadmap as tactical step/tool for funding. Related to above, roadmap can be used politically, placing undue weight on certain issues. Again, be careful not to have a small jury vote a certain way. Overcome through wider representation (all points considered).
- Historical pitfall or danger is "railroad" effect or narrowing bias - make sure there is balance in participation (through Delphi).

Process becoming too rigid, bureaucratic, detailed, cumbersome, costly, etc.:

- Roadmap growing too large and unwieldy
- Too many meetings - suggest one meeting for off-years
- Every year process tiring industry
- "We have gone overboard on strategy, formality…"
- Flexibility is low
- Structure (overly)
- Considerable time spent updating figures and tables
- I am still not in favor of including too much detail in the roadmap - trying to including all the details in the roadmap causes problems. Over-specification, and that's where things got into trouble - putting too much information, unnecessary information in the roadmap. It continues

to get deeper and deeper - continuously the case - example is 300mm - you don't need to put it on certain date - you can make it so "fuzzy" that somewhere after 200mm will be 300mm and you can make a ten year transition period - or five years - rather than two year, date certain! Unfortunately, for engineers it has to be exact. Because at the end you have one single design point. Very often it drives engineers crazy because they find that, "wait a minute, are you saying that if I agree to this roadmap number, then tomorrow or by that day I have to design a transistor with these set of characteristics? It's impossible." There's too much detail in it.

Economics (costs) not considered:

- ROI (return of Investment) is not considered.
- Business level/ROI-removed, normally only at technical/science level.
- Does not include the economics of the industry.
- Lots of technical concerns, sometimes cost not known (no clear criteria).
- Approaching "red brick wall" and getting to it is getting harder and harder (increasing marginal cost), especially with finite R&D funds.
- Here is the industrial research that's really driven by the economic model of the business. This 300 millimeter timing is really an economic model, it is really not technical. What they are saying, what people are complaining about: "wait a minute, you somehow tricked me into spending money on the 300 millimeter tool development way too early." This is the criticism from the suppliers, but that is not written in the roadmap exactly when what volume would be produced using what tool. They're simply saying that, "yes if we draw the line this way, chances are it's likely that we might need 300 millimeter." It doesn't really say that if you don't have it, the market will collapse - it did not really say anything like that too, either. Then if subsequently people are too eager to say and maybe some people have taken things out of context, in my opinion, they got into trouble.

Process not consistent:

- Deterioration in TWG and RCG member representative assignments which was originally established to provide for a broad semiconductor community collective input of knowledge. Had particular trouble with litho, wanting to bring their own agenda - very concerned with representation of entire semiconductor community - need for policy (e.g., make-up of TWGs - representatives, also guidelines for RCG) - industry already had advisory groups from SRC and Sematech (focused TAB) - hierarchy of advice for RCG.
- Different interpretations of yellow and red areas: "We can do .04 micron today (EUV), we just can't afford it," thus red space doesn't always mean "no known solution": in litho it means "no affordable solution," not the case in metrology, packaging and other areas (we really don't know)
- Not all sub-groups use the same framework - e.g. strange how test and packaging are the only two areas that have roadmap elements of cost/price (I do not believe that this directly belongs in a technology roadmap - it should be the result of the roadmap).
- Makeup of US TWG (logic/MPU centric) - complaint when international started (DRAM, SoC) flavor changing as roadmap goes international.
- Needs to be automatically internally consistent (e.g., automate linked spreadsheet) to help in TWG coordination (overall ORTC formally linked in).

- Every TWG concerned with reliability, but no reliability TWG (assumptions made about what other TWGs incorporate into their roadmap assumptions).

Forecast inaccuracy (too aggressive or not aggressive enough):

- Roadmap forecast blunder: 300mm - bad set of economics, also failed as interests of chip makers' (represented in Roadmap requirements) were in a sense dictated to suppliers (who had little say) - end result was $5B cost wasted by equipment industry.
- Credibility example is lithography in earlier roadmap: forecasted larger chip sizes - based on ORTC (extrapolation), one of the places where technology and economics strongly interact - required by big reticles (12") - people questioned, suppliers wondered, is this credible?
- Aggressiveness such as 300mm - before its time
- Timing is the average of many companies - not for the fastest - and this confuses suppliers
- Relaxed inputs to achieve better marketing arguments afterwards

Consensus hard and may produce mediocrity:

- Consensus is hard in groups
- Different companies have different assumptions
- Can develop a lemming-like mentality. One sees this often in SEMATECH. Example: the great cost advantages touted by SEMATECH for 300-mm wafers have been ten years late in arriving (still not here), and a serious financial burden on the suppliers.

Limitation of volunteer participants:

- The volunteers with time often are the drivers, but they may not be the best for the job.
- Remember all volunteer emphasis (get out what you put in) - lot of formal work required, never real consensus since much follow up after meetings - industry driven activity.
- Limited resources force trade-offs

Other:

- Enthusiasm is waning somewhat (99 is a lot easier than 94)
- Danger of complacency - market downturn has hurt (freeze on travel)
- Lack of implementation focus: no response from suppliers on needs ($) to implement - definite need in industry for response (e.g., 300mm debacle: cost a lot of money - Semi/Sematech example).
- The means for communicating the roadmap to the technology community requires substantial improvement.
- Need stronger leadership
- Whole notion of pre-competitive is a "broken" concept in that it's a wrong assumption that companies will freely contribute to the roadmap - anything that's strategically important won't get from the source, but from a third party. Pre-competitive usually pertains to standards issues such as wafer size, pin counts, etc. vs. Roadmap really deals with leading edge issues

(immediate semi capability) thus everything competitive.

32. (and #41) Please provide any additional thoughts and comments on the Semiconductor Technology Roadmap process including any suggestions for improving the process.

There were 54 total responses to questions #32 (31 responses) and #41 (23 responses). Both questions were identical, except that #32 was included in all surveys while #41 was part of the revised set of surveys geared to specific participant communities (i.e., SM&E, R&D, and international). Thus there was some redundancy in replies. Responses from both questions are combined here for better organization.

Answers to question #32:

There were actually 20 complete responses to this question, which expanded to 31 when separated by major category as follows. Note that the largest category is really an aggregate of individual suggestions that could not be placed in any single category. Following this first group, the "top 2" suggestions that represent half of all suggestions were:

1. Improve participation
2. Consider economics

Suggestion category	#	%
Process suggestions (specific)	9	29%
Improve participation	8	26%
Consider economics	7	23%
Meeting frequency and logistics	3	10%
Integrate with other efforts	2	6%
Don't change	2	6%
Total all categories	31	100%

Process suggestions (specific):

- Generational timing not ironed out: IRC decisions change at the last minute.
- Review comments “no known solution” carefully and consider possible workarounds.
- Needs improvement - bottom-up (universities predominant) or top-down (this needs to be done) or something in-between.
- Final comment/observation: seems newer roadmaps losing some steam - great number of people get together but come up with minor additions.
- "Roadmap" not a good metaphor - "trail blazing" is more appropriate.
- As process becomes less US-centric and more global-centric, challenge is how to continue process and keep it useful - CD-ROM will be very useful and informative.
- I often find that there is no effort to reconcile divergent sections of the Roadmap.
- Figure out optimal level of detail to focus on important things.
- Standardize and simplify formats.

Improve participation:

- Contributors contribute "for free," probably a stipend for certain committee members, sanctioned by their companies would help.
- Roadmap takes about 20% of time (Sematech Director) - most directors involved in Roadmap, recommends should be part of a person's job (included in performance appraisal)
- Identify and enlist the right people for the job. Identify responsible vs. review roles.
- Improve international participation and contribution.
- Reduce management overhead.
- Alan Allen, craftsman/artist of ORTC – is there a more productive use of his time?
- Balanced participation.
- Intel and SIA very effective in pulling off ITRS and getting international buy-in. Expanding the leadership base to include other companies and organizations will help maintain Roadmap credibility.

Consider economics (costs):

- ROI should be considered. And that kind of information should be given to related industries.
- Needs much more business perspective (and this is being addressed). Need fuller involvement of the supply chain, in particular the suppliers of critical materials.
- Would like to see the roadmap consider economic well-being of companies involved. Supposed to be a needs roadmap in cost per function (Moore's Law). Driven by lithography, now everyone can see it's changing. Has become a silicon-lithography roadmap. 97 Roadmap shows litho running out of steam (economics) - if you do everything by 2003, then won't be on Moore's Law. There are other non-litho solutions if you get clever. Roadmap needs to get back to needs. Intel wants to pull in, international involvement will counterbalance. Japan beyond silicon after 0.1.
- Roadmap is technology roadmap (ITRS), runs risk of being a technology "wish list" - not considering economics: timing, costs, "ecosystem" of interconnected parts; decoupled from business issues (e.g., 300mm); aggravated by continual technology acceleration, plus Asian flu that led business downturn in semiconductors. Already excess capacity, then 300mm in volume doubled capacity - prices fell; 97-98 DRAM unit volumes increased, but revenues fell due to lower prices. 1994 Roadmap projection/assumption: 1995 $150B semi industry, by 1998 $300B expectation - needed 2x devices, thus kicked off 300mm process - result: didn't happen! Need economic model of industry, not fab.
- Cost is major factor in determining colors (white, yellow, red).
- Cost factors: "whole cost" is system solution and related tradeoffs.
- What criteria to use to classify white, yellow, red: engineering/technical discussion draws out consensus from 'experts' thrashing back and forth, but major issue is cost: can it be done at a reasonable cost?

Meeting frequency and logistics:

- Making this a continuing year-long process is NOT helpful in maintaining and obtaining participation.
- Process relatively stable - now "painless" but still engage in dialogue. However, now needs to be revised so frequently that eventually that's all you do - look at any process improvements to use people's time more effectively.
- Workshop days tend to be long days (8am-8pm) - too packed, very tiring, thus suggest structure not so much formal sessions: make "enjoyable" vs. pressured. There's a perception that everything will be done on those days, but reality is that all doesn't get done. Major point is that goals of team-building and consensus have to be accomplished in less-formal settings (e.g., planned evening activities).

Integrate with other efforts:

- Roadmap has to have a better link/relationship with research: roadmap vs. "mapping" (no roads) in research - some long-term research not well thought out (e.g., lithography - placeholder?). '99 Roadmap does a better job, but "lost something" (trade-off); for instance, when does traditional scaling end? What replaces it? "Functional" scaling (not just smaller transistors) - '99 Roadmap discussed "equivalent scaling": not everything needs to scale at same rate - some things can scale slower or even "de-scale" (go backwards).
- Integrate more closely with SRC, MARCO, Sematech strategic plans.

Don't change:

- Keep process going: if the process works (like 92, 94, 97) it's a powerful tool: everyone falling in line - it does two things: 1. consensus of needs, 2. communicates to everyone. Critique both ways: you to someone and them to you, group critique process brings about consensus.
- Just keep at it.

Answers to question 41: …with particular emphasis on the SM&E industry?

There were 8 responses to this question. The top suggestion category (5 of 8 or 63%) was: *Increase involvement of supplier community*. This is very consistent with answers to #32 and other questions. The remaining 3 suggestions were too specific and lumped together in *Other*.

Increase involvement of supplier community:

- More involvement.
- Roadmap needs to serve supplier community better.
- More inclusion of the supplier - especially material suppliers when such drastic changes in materials are being forecast.
- Wafer manufacturers are not well represented on the roadmap. Process for communicating the roadmap to the SM&E industry continues to need work. Continued credibility of the Roadmap is crucial.
- What suppliers contribute to semi device manufacturing - having more clear understanding of what's possible (coloring boxes). Roadmap is simply requirements (what are capabilities?),

not cost, but now more aware of cost (e.g., 300mm, very cost-sensitive issue) - this is new question asked of suppliers.

Other:

- This is not really a suggestion for improving the roadmap process, but companies along the supply chain are implementing business-to-business e-commerce technologies. This will eventually have a significant effect on supplier-user relationships.
- No budget, won't change. Every year Semicon West, Europe, Asia; will continue to try meetings but may change.
- Management overhead???

41. …with particular emphasis on research community considerations?

There were 6 responses and each suggestion is specific enough that no categorization could be easily made. You will note the similarity of replies with answers to other questions.

- The term "roadmap" is not a good term for NTRS: identifies barriers, not solutions (paths).
- Implement besides DRAM and Microprocessor a specific chapter on mobile communication/low power.
- Current research problem in industry: not close enough to details. TSMC building transistors - issue is IP circuit design vs. device design. More and more chip industry becoming increasingly ignorant of equipment, thus IC circuit design (nuts and bolts). First IC makers built equipment: understood in detail. Then spun off: told requirements to suppliers. Now don't know what goes on in equipment. Result: "process architecture" now done in isolation, far from actual circuit design (IP). Industry has got to fund research - need to guide this - Roadmap doesn't say much about their job in "nuts and bolts" research. Interesting fact: Applied Materials now second largest company in semiconductor industry - bigger than TI's semiconductor division.
- Design vs. manufacturing: design tool makers (e.g., Cadence, Metrographics, Avanti) have close relationship with university research, SRC, comfortable with roadmap, etc. Equipment suppliers, on the other hand, never perceived as important as design (traditional ME doesn't have the panache of EE). Roadmap problem is red brick wall more related to ME than EE. Need to extend research spectrum. "Industry" is fragmented, vertically disintegrated, etc, but "whole thing" hasn't changed much - just divided differently on the inside. Same level of R&D needs to go on with equipment suppliers, formerly device maker "process development." Ditto with OEMs (users) systems/software, research "less natural" than at more fundamental level. Remember, Roadmap was always to provide a tool to guide research (identify gaps). After Sematech formed, not enough $ to do everything, so get government involved, after convincing that Japan coming, needed to put more money, thus "roadmap" to identify needs. Expanded character over time, but still same issue. First Roadmap looks very much like current Roadmap, now down to nuances: ITWG workshop - arguing about what is dimension (gate length, half-pitch, etc) - semantics - "how many angels can dance on the head of a pin" discussion. Alan Allan most tuned into this. Current controversy: white, yellow, red - true meaning?
- One of the things we were pushing on last year and this year is Andrew Kahng's work - he's a professor at UCLA, design department, and a member of the design TWG. He's involved with the GSRC, the design and test focus center at Berkeley. And one of the things he's working on is an interactive roadmap. In other words can we hook up the models the GSRC has with

the models that Alan Allan and everybody has in here in the next go-round and make them available for example on the ITRS website? So if you're coming along and saying, well I don't think I agree with that. Suppose the dimensions were like this? Do "what if" experiments to change the tables - not to change the periodical tables, but say I'm changing this and I want to see how that affects all the other tables. I want to see what the model is, what the algorithm is that was used on that table and maybe the algorithm is different. I want to change that, and then report back those findings so that we all could take advantage of that. And when I mentioned this to Alan Allan he says that might be a nightmare if we really do it. I said Alan, it's hard to get the people who are supposed to be working on the Roadmap to do this already. It's not clear that just people off the street are going to, that it's going to be overwhelming. But I think it could be an opportunity to let people challenge the assumptions in here. Because we think small changes - some of these things included in Alan's numbers - small changes to that could make big differences out in 2014 on the end of the Roadmap.

- Lucent leaning to red for unknown gate dielectric and means for getting ultrashallow junctions at gates, i.e. whole gate structure is a challenge both to design and to have enough process control to produce. Keep in mind that the current mind set is to build circuits with a minimum of redundancy by striving for defect free production. Another paradigm might be considered where the yield was very low, but the quantity of gates (e.g. molecules) very high so low yields would still create products. HP is working on such an approach, but it doesn't fit on the current ITRS format. In 3yrs we'll figure it out - from desktop bias. Question: where is market going and shouldn't Roadmap reflect this?

41. …with particular emphasis on international considerations?

There were 9 responses to this question. The top suggestion category (5 of 9 or 56%) was: *Improve participation*. Once again, this is very consistent with answers to #32 and other questions. The remaining 4 suggestions were too specific and lumped together in *Other*.

Improve participation:

- Need to get more industry people actively involved.
- Get all parties involved more, Sematech still plays major role - others have to.
- They might consider getting a small professional cadre to mind the shop between the periodic updates. These would seek to resolve inconsistencies and seek new paradigms.
- Meetings sometimes ad hoc, TWGs different, time to get every TWG in line. Also, no budget, participation is based solely on good will. For example, TWG participation from Sematech membership.
- The challenges are: 1) getting participation, and 2) finding ITWG chairs.

Other:

- Outcome to be more readily accessible (web, CD-ROM, etc) - this is already being acted upon. Analytical tools for getting deeper behind the data (spreadsheets) - no longer just a hardbound roadmap: superficial. Need more formal integration, more specific cross-TWG working group formats vs. ad hoc (e.g., chip size, SoC groups). Possible topical study group to include pin type, pin count, packaging to study how many signals and ground pins?
- Ever since we had that meeting in San Francisco [December 1998], I think when you go to these roadmap meetings each group will stand up and say "we've decided that we need to

add..." just like here we have System on a Chip, well we need to add a new table addressing this, we need new lines addressing this, etc. I think there's a real concern here. I talked to Linda Wilson and Paolo Gargini about it. It's not clear that the bigger this gets - the more tables, the more chapters - the more effective it is. I think the converse is true, I think it gets less effective. Because it's much more difficult to find what you're looking for in the Roadmap because it's so big and there's so many more tables, I think the roadmap then tends to lose some of its effectiveness. It's getting harder to even understand anymore. For example, one of our criteria for being chair of a TWG is you had to understand Alan Allan's charts and all of this which is a mystery to me.

- Environmental TWG (ESH): compliance standards are the focus today, but we really need to be much more proactive (tired word, but reactive is what we do today and we need to do the opposite).
- To keep the process so far is important.

33. Speculate on the semiconductor industry <u>without a Semiconductor Technology Roadmap</u>: Would technological progress in semiconductors be any different without a roadmap? Would the pace be faster, slower, more irregular? In what other ways?

There were 27 responses to this question. The wording of the question provided some guidance to respondents (i.e., pace of progress), but almost half responded that the biggest impact would be less efficient and organized use of R&D resources as follows:

<u>Category</u>	<u>#</u>	<u>%</u>
Less efficient/organized use of R&D resources	13	48%
Slower pace	9	33%
Irregular pace	2	7%
Other	3	11%

<u>Less efficient/organized use of R&D resources</u>:

- Pre-roadmap activity: wasted resources from not knowing needs, same in research - getting grants, far-out concepts
- Pre-roadmap era: case-by-case - one tool - couldn't look at whole picture.
- In the years before the Roadmap (CA ‘61-‘86), big budgets were spent on R&D. The result was spotty and the process very inefficient. I believe that if it had kept on much longer that management would have almost given up on that. That is precisely what happened to GE. They were early and heavy investors in semiconductor research. It never paid off. Jack Welch simply decided that ‘The emperor had no clothes’.
- To direct the R & D in relative industries, the more influencing consortia / joint programs among semiconductor manufactures have to be organized.
- Supplier R&D would be more difficult to focus; more options would exist without user agreement on new approaches.
- Equipment development would be at higher risk; higher count of “flop” vs. top development, less overall productivity gain.

- More expensive: development cost, redundancy. Philosophy of roadmap (real plus): good thing to just continue these trends, now consensus about limits by 15yrs out (1999 Roadmap first to recognize this) - wouldn't have happened 2yrs ago. No MARCO.
- Overall integration would not exist (e.g., 1Ghz chip w/o boards could happen - illustrative of integration). Semi community issues like new material for gate dialectric or gate electrode: needs to be brought up by the entire semi community (via roadmap).
- Today every company doing roadmaps, without centralized (plan) 10yrs ago disjointed: lost competitive advantage, Japan crisis, then pre-competitive - common tools/technologies. Testament of success: no Japanese crisis.
- Major contribution: no way to keep cost down, move progress forward. US economy/internet success is one result. Supplier community productivity, device yields, uptime of tools, drive to lower cost: all the result of the roadmap. Also "without Sematech": hard to separate the two [ITRS and Sematech].
- Couldn't have a 12" fab without coordination (like Intel story of fab idle for 18mos because no tools to outfit it). Roadmap has helped cut down on wafer size transition. Look at 6" to 8" service life compared with 12" - will be in use for 9-12yrs. 16" 450mm may not be necessary. No longer bigger chips.
- Would have been a "sort of" default roadmap - most companies have them, not in-synch as much.
- There wouldn't be a commonly accepted target.

<u>Slower pace</u>:

- Slower pace, lower support for new initiatives.
- Pace would be slower & more expensive to industry.
- Pace would likely be slower. Awareness to certain challenges would be smaller.
- Slower average pace for industry. Possibly may have had larger separation between leaders and laggards.
- Structure of industry maybe not any different, US maintained technology leadership (also other economic factors), but progress wouldn't be as fast - Moore's Law symbiotic with Roadmap
- At device level: wouldn't be much difference, but confusion, dissatisfaction, things not available, some element of slower pace from one element missing (conceptually not as good). Semi equipment level: same answer.
- Retrospective without Roadmap: technology generations would probably have been slower, but not sure if that's good or bad. Foundries/fabless have had no impact. Ditto small firms. Regarding MicroTech 2000, initial reaction was that the market would determine timing of generations, in retrospect it was the technology.
- Another chicken/egg question. Might have been a bit slower or faster. Might have measured something else. Market pressures independent of technology (necessity is mother of invention). Industry did realize results of roadmap: it caused things to happen - probably faster than would have been possible. There's been a call to "slow down" roadmap (pull-in).
- That is a hard question to answer. Without the roadmap and SRC and Sematech, we would not be where we are today. And the paradigm here that we are talking about is consortium managed collaborative research. Even universities use this model and so research consortia

are pre-competitive arrangements. These are the ones that are really the most creative in terms of generating new knowledge and accelerating learning. And if people are willing to buy into that model then that will be very successful. And it takes a lot of socialization. And the Roadmap is a major socialization. I think the answer to your question is that we would be way behind where we are at today without these collaborative roadmap and research activities.

Irregular pace:

- I believe the pace would be irregular and the industry would probably have experienced less consolidation at the supplier level. I would argue that a Technology Roadmap was an inevitable outcome of the demanding process requirements and infrastructure investments required for manufacturing increasingly complex devices.
- More irregular as stumbling blocks arise.

Other:

- Without roadmap vehicles, hard to start conversations
- Without roadmap? "worse off" - believes that progress is most important.
- Technology progress in the competitive arenas would not be affected. The major progress is in the pre-competitive arena, and in providing clearer requirement statements to industry suppliers.

33. Speculate on the Future: What will the 2005 Semiconductor Technology Roadmap look like? In what ways will it be different than the 1999 Semiconductor Technology Roadmap? In what ways will it be similar?

There were 38 total responses to this question representing one of the largest response rates to an individual survey question. Additionally, some of the answers were very detailed and informative. In short, few respondents shied away from predicting the future of the Roadmap (this may have something to do with the nature of the Roadmap process). In terms of the breakdown of answers, a vast majority (31 of 38 or 82%) cited potential differences which are further categorized below. The 7 (18%) similarities that were stated could not be easily categorized.

Different:

Category of what will be different	#	%
Alternative device structures/materials (post-CMOS)	11	36%
Changing industry structure (outsourcing trend, increased role of foundries, etc)	8	26%
More (basic) research emphasis	5	16%
Slowing of traditional scaling (smaller geometries)	2	6%
Other	5	16%
Total all categories	31	100%

Alternative device structures/materials (post-CMOS)

- CMOS may not be the only technology, other technologies may be featured or more noticeable.
- In 2005, the industry may well be in a broad deep crisis because it has not been able to find solutions to the limitations (gate, high K dialectrics, doping to exceed the solubility limits) now defined in 1999.
- The industry by then will know whether there is a true "End of the Roadmap" in sight. Probably silicon will go on to much smaller dimensions, but things like packaging and chip interconnect will require paradigm changes. There will not be the infrastructure to support this compression. Reorientation will be needed to solve these problems. During this hiatus Moore's Law will show a 5-10 year pause.
- The 2005 ITRS will have to address the shift from silicon technology to another base material.
- It will become more comprehensive in representing different, more diverse device requirements and will also concentrate more on innovative solutions which are less linked to CMOS scaling.
- 2005 Roadmap needs to include more alternative technologies besides CMOS. 2005 Roadmap will focus on system concepts.
- Beyond shrinking lines - another direction: packaging solution, new design - need to plan for future.
- 2005 is post-100nm era (red space). Challenges: 1) History of NGL: whole other set of issues than just roadmapping. 2) Theoretically will reach limit on copper (then optics, RF?). Roadmapping the breakthroughs, clear resolution on 450mm next wafer size or alternative (squares?).
- Future Roadmap challenges: SoC and die size. How do goals of one thrust area affect system level implementation? Can we just let it happen? Test area, also packaging: both limiting factors, product-specific - must deal with actual products, can't generalize - ultimate challenge is SoC, what happens then? When to integrate? Ability to carve out pre-competitive, what is SoC? ASIC? Die size affects many other roadmap entities (e.g., litho field size, defect density) - build team out of separate TWGs. Design, packaging, test must form teams like companies (must create virtual system like in a company) without specifying by device (DRAM, SRAM, etc).
- Future projections: 10 years from now about the inflection point for CMOS (won't disappear but will no longer be dominant technology driver). New types of devices will include MEMS, photonics, and new interconnect technologies. For these activities, "roadmapping is a lot tougher." In other words, not just extrapolating past performance, but different companies/alliances going different ways. New roadmap (replacement for CMOS) will await industry to demonstrate successful example (dominant design), then follow suit. The Roadmap won't identify revolutionary technologies, but will identify the goals and criteria that the revolutionary technology would have to achieve (i.e., the current CMOS technology performance benchmarks).
- Much richer discussion of post-CMOS technology (horizon for CMOS) - more consortia activities - areas now competitive will move to pre-competitive (e.g., supplier: resist coating machine) - problems become more difficult, must collaborate. Sees limits, but never sees roadmapping ending: productivity not only Moore's Law (50% from shrinking), other 50% from other factors (e.g., frequency on/off chip).

Changing industry structure (outsourcing trend, increased role of foundries, etc)

- Foundries growing rapidly, will have much stronger role: not just trailing technologies, now leading edge. Samsung and Hyundai will have bigger say, shift to less American and more Asian-Pacific region. How long will it take? 5-10yrs.
- A lot depends on company's health. IDM (Motorola, AMD) will become fabless.
- Industry global and maturing (e.g., Asian TSMC foundries), now manufacturing "jelly beans"; "technology faith" (in Moore's Law) will continue until physical "end of shrink"; 7 alternative paths - transistors minor component now - interconnect major issue; theory/fear of industry life cycle: Asian countries like China are much better at mature industries - ten years from now when end of scaling (Moore's Law), industry will be forced into maturity - which means "end of the U.S. industry"; ten years from now industry will be using a new device - Roadmap will reflect that; "Who would have thought that interconnect would be big issue today?"
- Will deal with more fundamental roadblocks and more speculative potential solutions. Will also become more product-specific (e.g., DRAM, SoC), more complex (quagmire), with more precise definitions to help interpretation (e.g., significance of red).
- Emergence of foundries (TSMC, UMC): processes becoming pretty standard. Cost of tools getting even higher, so processes become even more standard. Future of device maker industry: driven by cost. Intel and TI will be the last to move significant production to foundries - majors will continue to dictate needs. Foundries more involved in chip design in future, thus need to incorporate their needs. 2005: research-dominated focus: fundamental atomic limits - how to resolve these roadblocks with new technologies. Research community: basic research - more of that. Semiconductors: evolving technology - reaching limits. Today: synergize process with supplier community. Tomorrow: synergize process with research community. Need new chip methodology (alternatives to CMOS, like lithography in 97 Roadmap). 2003 roadmap: how to do single atom layers. Major change in structure: makeup of TWGs needs to change - different participants (universities). Yoshi Onichi Semi/Sematech talk at Semicon West: movement of research out of TI. Intel: we don't do "Research" but farm it out to universities/institutes. Move to standardize processes, outsource - majors will benefit from outside knowledge.
- International will strengthen, element of semi manufacturing from different countries reluctant to "show cards" - not inclusive, more competitive, foundries (don't have own products) less likely to disclose info.
- Industry economic model recognizing much more costly to scale - concern that manufacturing can't recover investment in next generation - more people concerned about keeping up with Moore's Law. TSMC (leading foundry) 1999 sales $2.5B vs. Intel $24B, but spending 2/3 of Intel in capital spending ($4B vs $6B) through government-backed subsidies and debt (highly-leveraged).
- Future role of Roadmap: what happens when we reach the "red brick wall"? Intel will then be forced to turn enormous resources elsewhere. Someone will have alternative ("next" Andy Grove) such as optical, quantum computing, etc. Probably not Intel (per Christensen's Innovator's Dilemma), maybe at Yorktown (IBM) or Lucent (Bell Labs) and probably not a start-up (garage-type): immense infrastructure needed. Start-up might contribute to one aspect, e.g., software or innovative circuit design: can you make circuit less linear (neural structure) than conventional von Neumann serial approach? Since parallel processing with software has lots of overhead, need both software and hardware - and hardware doesn't need to be expensive.

More (basic) research emphasis

- More inputs will be solicited and provided by universities and National Labs.

- Panic, reality that current timing of solutions will not happen (will be at 50nm and will have to address limits). Problem is 20yr cycle of research needed, but industry can't wait that long. Need more balance of research vs. supplier needs to further broaden Roadmap purpose.
- Progress will continue, but qualitatively different: need money into research.
- Note that breakthroughs will (and must) occur in next 15-20 years, but breakthroughs aren't "roadmappable" - only what we already know how to do.
- Research needs document: putting red where no solutions identified. Text in beginning: research needs highlighted. SIA view: universities always looking at funding. People worried about losing identity with changing name, maybe title in parenthesis. "Yell wolf too loud" ridiculous request from government research funds (i.e., if I agree to say this in a research document, they will have to give more money). De-emphasis on resistance to changing title.

Slowing of traditional scaling (smaller geometries)

- As we hit technical limits, feature-size scaling will slow or stop.
- How to build bigger chips without finer lines.

Other

- Roadmapping will continue but challenges will be different. There's a lot of work to do: costs $500M+ each year to turn colors (red to yellow to white). If we turn spots white, we'll find other red areas.
- Maybe different: extend to 3yr process (inadequate bandwidth) - books editing every 2yrs vs. original publication - need more continuity in TWG chairs.
- SoC will be more precisely defined. The outputs from cross-cut working groups [may] be more theoretical.
- New industry metric of progress - maybe not cost per function: issue is about function: cost per function may not be metric in the future - may need a different metric; when traditional scaling of feature size slows down - meaning "classic" Moore's Law (components per chip) slows down, cost per function will continue to fall at historic 30% per year, but because of some other factor (design, etc.) - meaning the result is the same: "new" Moore's Law continues on. This may be true, but cost per function may not be as important in the future. Historical example of cost per transistor (when they were a dollar) - the $1 transistor was the accepted industry (first principle) metric for years until IBM's new packaging technique (*flat pack* introduced with the 360 series) made them a penny, then the metric was no longer important. Same kind of thing happened later with memory, cost per bit (who knows or even cares anymore what the cost per bit is?). At one point memory was a limiting factor - no longer the case. Cost per chip more important now. The utility of the rest of the system (software, end product, etc.) really matters more.
- Need better cost awareness, ROI (include benefits along with cost). Maintaining Moore's Law no longer a question of existence, will need optimization. Moore's Law is a kind of meta-law - many factors play into this. Two questions the Roadmap asks: 1) Can we maintain Moore's Law? and 2) What is the most effective way to maintain Moore's Law? Considering global changes, economic cycles, finite R&D, etc - becomes a zero-sum game at some point, especially in tough economic times. Up until now Roadmap emphasis has been on Q1 (can we?) and industry has consistently responded. Note traditional barriers such as 1 micron, optical wavelength, and others - all have been "engineered away." Finally, the pre-competitive barrier: has to be a huge change in roadmapping mindset where people are willing to part with fairly competitive data.

Similar:

- The process and the format will be similar, but improved in clarity.
- Hopefully will be even more complete in scope as we learn what is missing each time.
- Nodes will be pulled in. Overall structure will be similar.
- Each Roadmap changes some from its predecessor … continuous improvement.
- Transistor not near its "end" - still a long way to go. What's different about today? Every time we've done projections in the past, the future always looked red five years out.
- In general it should look similar, though some technology can change or different solutions may emerge that change some aspects of the Roadmap. There are some hurdles, such as with photolithography, that place a burden on the equipment and material suppliers who may not have the “deep pockets” to support several competing R&D technologies. This is particularly true if the industry goes through another downturn; some suppliers will be hard pressed to make the required R&D investments. The 2005 Roadmap will probably involve more collaboration with other segments of the electronics industry, particularly the printed circuit board industry.
- 2005 Roadmap will not depart too much from today - should still be what everyone works from. Historical pitfall or danger is "railroad" effect or narrowing bias - make sure there is balance in participation (through Delphi). Also make sure Roadmap used properly: to define needs and potential solutions (not the only "route" to take). Continue to "map" options - one vs. others - use to select best option, but don't use Roadmap to limit possible solutions. 2005 Roadmap will involve more suppliers (and their suppliers) - focus on broadening participation - not creating new structure. No dramatic change (materials not dying) - still have to meet market requirements.

35. What about the Semiconductor Technology Roadmap process? Will it include other regions of the world? Will/can it become more inclusive of the supplier and/or user community?

There were 17 responses to this question. Almost 90% (15 of 17) answered yes to one or both questions. The *Yes* answers were further categorized by the nature of the answers as follows. The widespread recognition of the globalization of the semiconductor industry (device maker and SM&E sectors) underscores these answers. New regions including Singapore, China, Russia, and South America were suggested for inclusion in a future Roadmap process.

Answer category	#	%
Yes	9	53%
Yes, with new regions specified	3	18%
Yes, as necessary	3	18%
No, or if necessary	2	11%

Yes:

- Yes to both
- Yes and Yes
- Yes, probably, but a process of controlling the complexity has to be fine-tuned.

- The semiconductor industry is a global industry so other regions of the world will be included. Companies at the forefront of technology development and with a greater market share of course will likely have considerably more influence during the process. It must become more inclusive of the supplier level (and the supplier's supplier level) for the industry to meet the demanding requirements for future device geometries. With new materials and processes being developed, new suppliers have entered certain market segments. Some of these suppliers are unfamiliar with chip maker's requirements and processes for qualifying a new technology.
- Other regions will be difficult, but foundries will need to be included. Suppliers should absolutely be a part as more process development is put on their shoulders.
- As CMOS scaling becomes increasingly challenging and "single node" solutions become the norm, greater degrees of collaboration between semiconductor manufacturer and supplier become mandated, therefore it must increasingly become a more inclusive of the entire community. Single node example is lithography: 193nm cutting edge tools for two technology nodes, then 153nm for maybe only one technology node, then no known solutions. If only one node solution, then why pursue it? Scaling challenge includes lagging design productivity, instruments, doping.
- Roadmap process needs to include all regions of the world. Roadmap process will be more inclusive with respect to the supplier community.
- It must become more inclusive of suppliers. They bear the cost burden early, get returns late. Wrong Roadmap predictions make this far more difficult. Supplier input will help assure closer touch with reality.
- Role of SIA in future ITRS: ITRS jointly sponsored - will stay that way for a while; special role for SIA: spelled out in MOU; SIA reserves right to name IRC chair; SIA retains copyright - someone has to own it; various regions of world in different stages on involvement; U.S. farthest along; Japan second (farthest along of international regions); Europe next - still getting organized; then Korea and Taiwan (toss-up) - note that Korea didn't participate at all in first round; For future roadmaps: as trade-offs become more pronounced, look at dependencies on other TWGs in a similar fashion as grand challenges - propose cross-TWG attendance like SOC working group.

Yes, with new regions specified:

- Yes. Possibly should include China and Russia. It will expand the involvement of suppliers.
- Singapore wants to participate (has participated in packaging), but has to expand involvement to include lithography, device, interconnect, and FEP to become full ITRS participant. Two players: Government-sponsored research institute and Charter (private firm). China: not now because still using older technologies. Total participants will decrease in size because not building fabs, thus fewer technologies/tools needed. For example, HP stopped manufacturing and now outsources to Singapore's Charter.
- Yes, probably have to incorporate South America, China. All emerging regions will play a part but not in the same way (i.e., cooperative basis). Interesting if no regional differentiation, industries will have consolidated - all companies exist around intellectual property. Identification of product/technology decision of region might be different (e.g., DRAM). Industry as inclusive as possible, but bigger companies tend to take leadership role - suppliers even more so (as individual suppliers/regions choose to participate). Smaller companies don't have the wherewithal. Post-inclusion: no longer capability-specific.

Yes, as necessary:

- More suppliers are now on the TWGs. SEMI has helped this and is providing feedback through a separate study.
- It already includes other regions. Suppliers will and should be included.
- At the present time, all of the important regions of the world are represented. As additional regions get seriously involved in the industry, it will be in everyone's interest for them to be participants. More supplier input? I certainly hope so!

No, or if necessary:

- The member associations at present cover more than 90% of world semiconductor production. Therefore no more new association will be required.
- If NECESSARY. Will/can it become more inclusive of the supplier and/or user community? More … NO … it already includes suppliers.

SUPPLEMENTAL SURVEY QUESTIONS (asked of SM&E, Research, and International respondents):

36. How well does the Roadmap serve the needs of:

This is the first of six questions added to the revised survey instrument in an attempt to obtain specific feedback from different Roadmap participant communities (i.e., supplier, research, and international). There were 25 total responses to this question as follows: 1 SIA, 13 SM&E, 8 Research, and 3 International. Categorization was only possible with the SM&E answers. Responses appear by participant group below.

a. SIA members?

There was only 1 response as follows:

- Quite well - taken very seriously; Roadmap purpose is to identify problems that stand in the way of the historical growth path; serves as guide to research community; also guides supplier community, particularly in terms of timing.

b. the semiconductor material and equipment supplier industry?

There were 13 responses for this group. The largest single category of use (62%) is *provides consensus of needs and timing for product development* as shown below:

Category	#	%
Provides consensus of needs and timing for product development	8	62%
Limited use (needs improvement)	3	23%
Other	2	15%

Provides consensus of needs and timing for product development:

- New product planning.
- Telling them what their customers need: very important for planning equipment development.
- This (1999) iteration, supplier community takes a lot more seriously now (in business planning) - used as one piece of information that goes (not totally) into product/business planning.
- It produces a consensus of needs. It also produces a consensus of potential solutions (sometimes far from correct).
- Generalized overview on expectations yielding distinction between mainstream and sophisticated approaches.
- It provides a benchmark for suppliers to work from, and for preparing a strategic business plan. Also, a supplier can target a future device generation for introducing a new technology so to widen its overall market presence in the chip industry. New and smaller firms also use future device generations to introduce a new material or equipment to the market.
- If you want to get a fab together, need tools and materials ready. Cost escalation big issue. For example, silicon ingot (or wafer slice?) 8" $50-70 vs. 12" $350 (was $600). Set of masks now $1 million. Lithography tool now $30 million, thus need many customers, uses ITRS (consensus view) to determine industry needs. Roadmap allows look ahead to possibly stretch tool use: 130 to 90 to 65nm, which tool? 193 for 90nm node, if 157 not ready for 65

then stretch 193 litho tool. Toolmaker use of Roadmap: as tool supplier make sure tool ready on time (not early, not late). Tools make technology acceleration!

- Suppliers concern mainly with timing: technology moving so fast, having tough time keeping pace (making investments and seeing returns) - business/economics concerns. Press reports overstate situation. "Don't know what can be done about it" - pace of things is reality: "ITRS reflects reality"; fast change is fundamental to the industry. If you asked all the people in the industry, "who would like to move slower?" nobody would answer - nobody is going to slow down; every company needs to decide individually, based on their own self-interest, when to make investments. "Timing" is the collective result of actions by individual companies making decisions in their own best interest; traditional example is capacity shortages - firms react, some over-react. Can't "regulate" this (anti-trust violation); response to suggestion for "economic roadmap": would be totally different document with a different purpose; ITRS is a technology roadmap: identifies technical problems; stands on its own merits. Bill Spencer of Sematech advocates "smoothing" of cycles but not convinced anything can be done (cyclical industry by nature); what can be done/is being done: more supplier involvement in Roadmap process. For example, Apr '00 SIA letters to Stan Myers (SEMI) and SISA proactively inviting supplier community into the process; IRC: each region to formally invite their supplier community; remember whole thing is volunteer operation - do the best they can.

Limited use (needs improvement):

- Roadmap has lost credibility with suppliers over 300mm - severe skepticism - die size didn't go up with 15%/yr increase trend (rule of thumb <100 die/wafer). Roadmap community under gun to improve credibility SEMICON/West (the equipment exposition that SEMI puts on every July in San Francisco is a "black hole" for activities and absorbs lots of time before/after. This means that we either have to join them and be part of their action or get out of the way. Joining is the better option because the suppliers must be included in the Roadmap activity if it is to continue to be meaningful. Must do a better job getting suppliers involved: Sematech orientation (suppliers vs. manufacturing customers are not equals).
- Only partially, since it tends to be dominated by logic and MPU needs.
- "Red" difficulties don't have ideas.

Other:

- Supplier community research is difficult: short-range focus - can't accommodate longer range needs - time-to-market pressures - thus, very little R&D investment - difficult for SRC to work with them. History: originally TI made own fab equipment - very inefficient, chipmakers competing on fab line (processing). Applied evolved, now cooperating. Then foundry model - now competition in system design: time-to-market "takes all the marbles." Crisis: semi manufacturing off-shore; evolution (included in Roadmap): change in competitive make-up -> SRC, Sematech missions -> "move up the ladder."
- Rationale for ITRS: tool/materials companies wanted broader markets. Look at TWG chairs for growing influence in Roadmap, tool company voice into TWG as chair/co-chair, for example FEP Walt Class co-chair has big influence, interconnect co-chair Chris Case (Edwards BOC).

c. the research community, both in industry (e.g., IBM's T.J. Watson's Research Center), universities, and the national labs?

There were 8 responses for this group. Most were longer, essay-type answers that did not allow for categorization. General themes that were discussed included distinguishing between on- vs. off-Roadmap research, short- vs. long-term focus of research organizations such as the SRC, MARCO, and universities. One omission in this version of the question was the lack of inclusion of Sematech as part of the research community. Individual responses follow:

- Provides a broad perspective on important problems, etc.
- It has allowed Watson to 'off-load' some far out tasks to other organizations for speculative exploration.
- In serving needs of SRC/research community, Roadmap has prime influence in defining research agendas and courses taught. Has unifying effect in university research (traditionally too much redundancy). Roadmap has helped, has had on-roadmap bias since the beginning (wasn't expansive enough) - 15-yr pursuit of fine line. Need alternative pathways - academics haven't sought off-roadmap research - lots of "swirl" in academic community. Reference Jim Meindl 10-15yrs "limits talk" GaTech, formerly RPI, Stanford; ARPA. NSF slow to fund longer range investigations - not doing a good job addressing off-roadmap (engineering departments). SRC/MARCO research program is longer range (engineers typically worried about next week), government R&D budget partly funds. Shouldn't "punish" them with Roadmap.
- Three types/directions for academic research: 1) On-Roadmap needs - most desirable from industry standpoint, 2) researchers not aware of Roadmap - typically not useful/meaningful since the Roadmap represents industry needs, usually moves faster than academic community, 3) Off-Roadmap (intentionally) or "outside-the-box" (better than CMOS) revolutionary (vs. evolutionary). Current Roadmap is "CMOS-centric." Must be careful what performance goals/criteria should be to be meaningful (different than type #2). Example is MARCO Focus Center for Interconnect chaired by Jim Meindl, GaTech. Objective is to develop strong revolutionary concepts (e.g., optical).
- The SRC in particular has required all university professors who may submit proposals to show a relevancy of the proposed research to the Roadmap. This has been done for years. Not so much that the SRC is on a one-track train since the mission is really about doing things that are creative, off the Roadmap. The SRC has somewhat tempered the guidance to university professors by stating that some fraction of the research accepted for funding should be on the Roadmap and some fraction should intentionally be off the Roadmap. Another important thing is the funding of the MARCO Focus Research Centers which operate under the umbrella of the SRC. Craig Barrett's concern was that the SRC was funding more and more short-term research that was increasingly driven by the Roadmap. The MARCO Centers addressed this problem by stressing longer time horizons and more control over the research agenda by the university professors themselves.
- Research community: for years, Roadmap served very well - yellow/red spaces (holes) meant go do work - workshops to solve problems. Technology acceleration is the result of the Roadmap. Recent phenomenon: students see as a *fait accompli* - no new ideas. What's new? CDR (cross-discipline research) - outside Roadmap. Small scale, million dollars total budget: $20K projects - 36 applications, 10 funded so far, lots of institutions. Only 5% of SRC budget: 40% materials, 25% new devices. Challenge: how to keep students interested, make it more exciting. Remember that Roadmap is written by engineers. The challenge is how to write it with enough "levity" yet with competence to be taken seriously. Suggest more visual: multi-media, AV, etc.
- How to balance on- and off-Roadmap research? Stress Roadmap's purpose to identify the set of problems to be solved; thus a lot of research has focused on Roadmap needs; not comfortable with on- and off-Roadmap terminology. Don't know what that really means.

Roadmap identifies problems, but some problems not identified in the Roadmap, so focus on radical alternatives - breakthroughs: Focus Center Program; control is through universities (25% government funded, 75% industry); different focus than SRC which is more hands on, incremental.

- How as a Roadmap user? Too broad to cover to allocate resources. It's a 2-way street as a researcher - this is true of any participant in the Roadmap: each has a certain expertise, thus bias - for example NIST (CMOS RF) or Japan (productivity) - those things will be reflected in the tables. As a user, never do anything that's NOT a priority: strong correlation between funding agencies and Roadmap priorities. Researcher notices when Roadmap addresses something different. Researcher joins Roadmap process to change something or to change what you do - both are very hard. Researchers can't change directions very fast, hard to walk into new community, students stay around for 5 years or so, multi-year funding, and other institutional barriers.

d. the international semiconductor community (i.e., chip customers, chip makers, equipment and material suppliers, universities, and related government agencies)?

There were 3 responses for this group. They are short and fairly straightforward (see below). It is important to note that at the time when the bulk of this field work was completed (mid 1999 to early 2000), Roadmap involvement by the international community was just getting started.

- Everyone uses it - strongest with SM&E because chip makers are customers.
- Conferences. PR through member associations. Delivery of CD-ROMs and books. Web page.
- Involvement should be stronger, which is primarily not the fault of the American community.

37. Has the evolution of the Roadmap taken into account the changing structure of the industry?

There were 24 responses to this question. The first 6 answers are essay-type responses taken from context interviews. These provide informative background regarding the evolution of the industry (see immediately below). These responses are followed by replies to sub-questions relating to the SM&E and Research communities.

Context answers:

- Evolution of industry collaboration (major Roadmap ingredient): Traditionally, semi industry was vertically integrated - IBM, TI, Fairchild, Motorola all did everything in-house in 50s and 60s. By 1970s this was a very "fool hearted" exercise - developing every tool, etc. - just didn't have enough knowledge, worse didn't have enough market most of the time to recoup such a large expenditure.
- It's easier today to share info (predominantly semi makers), production processes now pre-competitive (IBM, Intel, TI don't make their own equipment anymore). Used to compete on process technology and tools (e.g., photo-resist coating, plasma matchers), now compete on design: design TWG toughest (most touchy areas).
- Industry evolution (Jim Meindl's inverted pyramid): 20yrs ago industry was vertically integrated: users > computer equipment makers > semiconductor makers > semi equipment makers > materials (silicon mine). Today: no longer the case (e.g., foundry model). What's next? Next level not technological, but economic: must spread investment across as many assets as possible. It will be about how much money to spend, and in what markets, are they

growing/expanding, etc? Begs for the need for globalization throughout Europe, Asia, and U.S. Getting to this level, fundamental economics in emerging regions (Asia, Africa, Eastern Europe). All about capital, wise investment (IMF, WTO must find ways to), at same time be competitive. Technical capability that anyone can do with the right amount of capital - efficiency gains are becoming more limited.

- Technology drivers: DRAM technology driver of the past (20+ years), cost, productivity - most bits on a chip and on a wafer. Japanese: continuous improvement, driving machine. For most part logic has paced well behind (2-3yrs): first DRAM, then logic. Late 80s-early 90s with advent of PC: pressure to competitively drive performance. By mid 90s data starts on rapid acceleration (from being 2-3yrs behind, logic using technology already there from DRAM), crossover DRAM by late 90s happened (see Roadmap scaling graph, logic on steeper slope than DRAM). Late 90s Roadmap: extreme demand now, used to 2x every 18mos (vs. 1.5x). Two forces met during hard economic times (Asian crisis). Coincidental with litho extending to 248nm (95-98 especially), also pressure placed upon materials community for set-up availability. PCs now a commodity (cost driven). New challenge for equipment companies: recoup investment over 3yrs (performance, extreme cost measures, extend technologies).
- Industry "government": Example is wafer size. Intel funded 6" 150mm, IBM funded 8" 200mm (working closely with equipment makers, bridge tools retrofitted to handle 300mm), 12" 300mm tens of billions of dollars: collective approach (consortium). Also, equipment industry asked to pay more of a share, asked to pay their own way. Consortium guidance like R&D technology tax. How much government do you want and how do you pay for it? R&D not yours today, more like savings (deferred wealth). Must have a long view, how do I collect taxes? Big prices/profits. Industry government (infrastructure) $10B tax for 300mm from profits of companies that paid for development. Traditional "sugar daddies" no longer there (more productive). New funding model is flat tax.
- Economics is now the holy grail: economic limitations (revenues, profits, prices) - "slippery slope." Affordable cost: need to make a reasonable profit. Pre-competitive technology safe (continuously improve cost/function curve) vs. "pre-competitive" economics touchy (implies control of market, any smacking of limitations). IEF (Industry Executive Forum) group meets twice a year to discuss "how do we collectively afford R&D, goals, timing, etc?" but not spend too much. (Same discussion as 6" wafers 12yrs ago, but corporate memory lapse.) Sematech task to do modeling: market segmentation data, data mining, technology node cycles. "Global Economic Symposium" is foundation of economic roadmap (collective intelligence). Moore's Law is collective enemy if productivity stops. Macroeconomic view only models the industry in a gross way (chaos like Wall Street). Since we don't know, must create good ideas that help guide decision-makers. Equipment suppliers attempting their own roadmap (consortium), but so few hard to find agreement on requirements.

a. For example, the SM&E industry is now more specialized, stronger, and more knowledgeable/ responsible for industry R&D advances. Is this structural change reflected in the roadmapping process?

There were 13 responses to this sub-question. Most of these are short replies and are presented in a somewhat ascending order relative to degree of agreement:

- No - suppliers need to be treated as partners - not vendors
- Suppliers are still not well represented at the RCG level.
- Maybe
- Somewhat

- Indirect way, when people sit down reflects diverse needs.
- There has been some improvement in this direction, but this is an area of considerable opportunity for improvement.
- Fabless should get more involved.
- Starting to change - international obvious change, DRAM into consideration, foundries and fabless.
- Yes, restructured working groups reflect horizontalisation trends in industry.
- As investment requirements increase and the burden has shifted down the supply chain, I think the industry will experience more consolidation at the supplier base.
- As industry matures, IC companies don't compete on process, but design. IC firms now buy processes (doing a good job). Because of this can come together (pre-competitive).
- Suppliers are key to Moore's Law. Convenient: Roadmap gives one set of numbers - good for starting point in planning process, thus has improved planning process.
- Semi equipment industry now where semi industry was 20yrs ago (fragmented, everyone different) - one reason no SME Roadmap yet (no commonality). Differentiator today: products, speed to market. Something cooking regarding cost: advisory committees, additional groups, councils, but not a need for semi equipment roadmap.

b. Has the evolution of the roadmap taken into account the changing nature of semiconductor research?

There were 5 responses to this sub-question. Each reply should be considered on its own merit:

- It has defined this nature.
- Decided pre-competitive area was where to cooperate to plan, result was U.S. won the "cold" (chip) war.
- Original impetus of Roadmap goes back to U.S. semiconductor industry problems in the 1980s - U.S. industry was in fear of being left behind, so looked around and saw other nations were successful in part from long range strategic plans (e.g., Japan's MITI strategy).
- Research approach in Europe is structurally different than in U.S.: intermediary role of institutes. EMAC (Belgium conference) now involved in advisory role, Lete in France, Frauhoffer Institutes in Germany. IC companies (Philips, Infineon, ST, etc.) must get institutes involved, but limited number of leading IC oriented institutes. Institutes have better contacts with universities than IC companies: industry > institutes (facilitator) > universities: middle is necessary step to get everyone involved.
- Consider factors like economic cycles, reduced government funding, international threat of other roadmaps. Despite industry evolution Roadmap content has not changed a lot. For example, Design chapter (20-30 pages), design issues very generic - fundamentally at different elements of design but same process: figure out, check it, did you do correctly? Executing design, not really many levels of design: cocktail napkin, Boolean, RTL or physical, logical, behavioral correspond to these basic levels. Say very similar things (obvious in retrospect), scope of design much broader than interconnect or test (both 30 pages) - very specific goal: get product to market. Design chapter devotes 4pgs for test (ATE), imbalance. Design really central issue: what you can't solve in design must solve in process manufacturing.

38. At the device level there is increasing growth of fabless firms and foundries. How are their requirements included in the Roadmap?

There were 14 responses to this question. In more than half of the replies respondents indicated that foundries (some by name) were already involved in the Roadmap process. Those replies are listed below in ascending order of involvement. Most of the other comments seemed to acknowledge that the needs of these important sectors were being addressed by the Roadmap.

Evidence of participation:

- Insufficiently.
- Integrated guys (IDMs): foundries (TSMC, most in Taiwan) very important today - don't play as much into Roadmap.
- Through present member associations.
- Via the foundries.
- They are part of the ITRS process.
- TSMC participates.
- Design and test, fabless firms don't show up, don't care (design houses afraid); TSMC and UMC participate.
- The major foundries are participating, and due to the recognition of their manufacturing prowess, they are being listened to.

Other comments:

- Roadmap provides link between fabless firms and foundries; but both rely on open discussions.
- Presumably through better future Roadmap participation by the foundries. However, design issues are clearly identified in the Roadmap, which are of paramount importance for the fabless firms.
- The ITRS includes most of the technology thrusts necessary for semiconductor manufacturing. This means that the ITRS gives enough information also for the foundries and fabless design houses.
- Internationally a good move: foundries all outside the US, all international, thus makes stronger ITRS case. Does not really change requirements, but customers change.
- Foundries' needs (TSMC) included but feels forecasts (by Dataquest) are grossly overstated (presently 8% of chip sales, 20% of equipment buys).
- Not certain what role fabless firms and foundries have played in the current Roadmap process. Fabless firms, however, are one segment driving innovation so their suppliers, the foundries, will probably have an increasingly more prominent role in the Roadmap process. Material and equipment suppliers are improving their partnerships with foundries.

39. Do some firms diverge from the roadmap and if so, why? For that matter, do some firms totally ignore the roadmap and if so, why?

There were 13 responses to this question. The majority (69%) said *No* (some with qualification), but the remaining 31% agreed based on "Beat the Roadmap" behavior. Answers were categorized as follows:

Yes, "Beat the Roadmap" or lag Roadmap timing	4	31%
No, but some firms have different needs	4	31%
Not used literally	3	23%
No	2	15%

Yes, "Beat the Roadmap" or lag in Roadmap timing:

- Absolutely, "beat the roadmap" approach. Some companies even more technology aggressive - try to prove to other people "business agenda" vs. "common good."
- Some companies, interestingly enough, use the Roadmap as a stalking horse. It's sort of a target that they can surpass, the "beat the roadmap" behavior - an interesting sociological phenomenon.
- The problem with it has been that no one inside a company actually believes in the Roadmap node timing. You know that Intel does not do things on a three-year cycle, but more like a 2 1/4 year cycle and the Roadmap is a 3-year cycle. So the industry sets the Roadmap and then it's immediately ignored. Suppliers get different directions and they complain. As soon as you set a Roadmap like that the first objective is to beat it. It is like waving a red flag in front of us - we are going to be there before our competitors. So it is a challenge more than anything, but I think the Roadmap is useful because it provides an industry-wide coordination for suppliers and it helps set standards for equipment that makes suppliers' jobs much easier.
- Yes, there are the very leading edge companies that fully intend to stay ahead of the Roadmap, and there are more conservative companies who will minimize risk and R&D expense by staying (intentionally) one half or even a full technology node behind the Roadmap.

No, but some firms have different needs:

- I do not think so. Micron ignores the process. Why?
- No, but National is not an active participant. They make a different kind of product (not leading edge). They stay involved because they still need tools.
- A specific example does not come immediately to mind, but I think a smaller company that is developing a truly innovative process or material technology is in a better position and more likely to diverge from the roadmap. If this new technology is proven successful then it can cause a revolutionary change in how chips are processed.
- Some like Delco and Kodak feel that NEMI is more suited to their needs. This is due to the nature of their businesses (high temp and optical scanners). Some feel that the Roadmap is so beyond these capabilities that they are OK with pursuing their niche and letting the rest of the world go by (e.g., Honeywell and InterSil).

Not used literally:

- Current Roadmap is strongly MPU and Logic-centric. It therefore is not sufficiently broad in scope to satisfy the needs of the various semiconductor manufacturers. Some companies may also feel that they have such strong direct ties with their customers that the Roadmap is superfluous to their needs.
- The Roadmap compiles a best guess on expectations. None of the firms will strictly follow the Roadmap. Application driven technologies may not follow mainstream expectations and requirements.
- All the time, doesn't change requirements. Roadmap adjusted every year. No customer doesn't use it for planning - certainly not the only source - doesn't point out "yes sir" tell us what is next. Researchers use it for materials purposes.

No:

- No firm can diverge from the Roadmap because of pressure from customers.
- No - I don't see divergence.

40. Some have argued that the roadmap has helped in the recovery of the U.S. SM&E industry by better aligning technical requirements along the vast semiconductor "food (supply) chain." Do you agree with this?

There were 10 responses to this question. This was one of the last questions asked and was often skipped. Even so, the replies broke down evenly as 50% agreed while 50% disagreed. Additional contributing factors (e.g., Sematech, chip industry cycles) were cited in some of the *Disagree* comments.

Agree:

- Agree
- Agree: visibility of mainstream and thus less wasted efforts.
- Very true, has been useful - more important down the road.
- Yes, has helped worldwide. Look at last 5-10yrs. Tool sales in U.S., Europe, and Japan. Applied sales international.
- I agree. It is certainly a different picture today for the U.S. SM&E industry compared to the late 1980s. But things are constantly changing, and as noted above in the questionnaire, foundries and fabless firms are gaining a greater presence and the industry has become more global.

Disagree:

- Absolutely not! SM&E industry cycles are driven by chip industry over-and under-capacity cycles which not strongly linked to food chain technical requirements. Helps to clarify technology enabling equipment sets. As a supplier, 1998 devastating year, foolish over-expansion - Korea in mid-90s in DRAM expansion, Taiwan now. Samsung and Hyundai 1:1 revenue to new capital ratio "heavy into the bank" or ruthless spending. Highly leveraged, now excess capacity (e.g., in 1995 4Mb DRAM cost $13 so everyone wanted in - even Mobil Oil, then lower prices, yet high fixed cost) everyone lost money from price collapse: 16Mb $50 in '95 fell to $3 by mid-98.

- Disagree - I see the achievement of (then US only) SEMATECH bringing the infrastructure and the IC producers into a useful improved relationship as the key factor in this improvement.
- No - we need a business roadmap that will address the unstable cyclicality of the industry.
- No, but certainly contributed to clarity of needs - some still deviate.
- I do not think this is true. The American industry has thought of its technical and innovate strengths which have brought it back onto the leading edge.

41. Any suggestions for improving the Roadmap process?

See answers to Question #32.

ADDITIONAL QUESTIONS (not specifically asked in survey instrument but asked often of informants):

42. In your own words, what is the purpose of the Roadmap?

Official responses:

- The purpose of the Roadmap is simply to provide a reference document of requirements, potential solutions, and their timing for the semiconductor industry. (*Semiconductor Magazine*, Vol. 1, No. 1, January 2000) - other quotes taken from this article:
  - "This roadmap provides a realistic, globally synchronized approach to what we can expect technically for our industry in the future." (Paolo Gargini)
  - The ITRS represents an up-to-date, global industry consensus on the technical challenges that our industry will address. Each challenge is also an opportunity for the semiconductor community to add to the history of breakthrough achievements upon which the growth of our industry has been based." (Bob Doering)
  - "The key factor in [the Roadmap's] success is the ongoing emphasis on obtaining consensus on industry drivers, requirements, and technology timelines." (George Scalise)

Other responses:

The above excerpts were drawn from one of several trade news articles that covered the release of the 1999 ITRS. The author compiled the following 18 additional responses through the course of interviews for this research that bring added context to the purpose of the Roadmap:

- The purpose of the Roadmap is to beat it.
- The purpose of the Roadmap is to minimize risks, here I think you want to minimize surprises. So the Roadmap is serving its purpose for creating a very predictable path for members and suppliers to follow that will enable them to meet their deadlines.
- The real purpose of the Roadmap is collaboration - everybody can agree on what to work on, has never heard the criticism about the Roadmap limiting research.
- Purpose: suppliers use in their planning - speed up through supplier/equipment community (industry needs equipment). Research community no less important (e.g., MARCO).
- Self-explanatory - roadmap is a metaphor: Micro Tech 2000 evolved into the SIA Roadmap.
- ITRS has provided a framework for making investment decisions not only among semiconductor companies, but also at national labs and at universities.
- The purpose and style of roadmaps vary significantly with the stage of the industry - balance between market and technology.
- The Roadmap is "average," but no one wants to be average so they "beat the roadmap," thus collectively accelerate the roadmap.
- We are careful not - how can I put this? - not to make the Roadmap God. What I'm trying to say here is that the Roadmap is essentially a scaling method - I actually call it a business strategy.
- Roadmaps are good practice - keeps people thinking.
- The Roadmap has catalyzed the continued orderly advancement of the integrated circuit… This process may be the most important product of semiconductor industry cooperation.

- The Roadmap is a process of collective intelligence.
- A copy of the Roadmap won't tell you how to do a roadmap, at best.
- The Roadmap won't identify revolutionary technologies, but will identify the goals and criteria that the revolutionary technology would have to achieve (i.e., the current CMOS technology performance benchmarks).
- Roadmaps are very useful for establishing interchange between University/Laboratory research community and industry. It is especially important to involve the research community in the Roadmap process; industry has increasingly short term focus, research community has to respond to longer term needs.
- What do you want the roadmap to do? At first, the first version of the Roadmap said, "What's the Roadmap for?" It's for two things: one is to tell the tooling industry when to expect to need what - that's one thing. The other thing is that telling those universities - all those applying for funding for research, is to say what to work on - and also help the funding agency with what to fund.
- Roadmap process is "evolutionary" (not revolutionary - new innovations); very good job helping to move current scaling - won't reach the "end" of Moore's Law *per se* but will continue with other functions (3D dimensions, software, etc.); eventually will hit limits - need new materials (low-k dialectric); industry using 2D CMOS last 2 decades (dominant design, still fastest moving) - look at industry to be ultimate conservative: fab practice, manufacturing community, it has to work (research output much more speculative).
- Standards are strongest tie (like European telecom) - roadmaps similar, interactive commonality: semi industry heavily organized (around standards), SEMI, Sematech, SRC (consortia). While standards play a role, a major reason for the Roadmap is to provide a long range and comprehensive outlook on major trends (and metrics) in CMOS manufacturing that are believed to be critical to maintaining progress according to Moore's Law. The trends identified and the corresponding metrics that must be achieved are believed to be a common challenge for all CMOS manufacturers.

43. Why is the Roadmap successful?

There were 24 responses to this question. The largest success factor is attributed to Sematech's active and supportive role of the Roadmap. The fact that Sematech was initially assigned by the SIA as the organizer and publisher of the first 1992 Roadmap and has continued in this capacity ever since is a big part of this. Further, Sematech's consensus process used to collectively work technical challenges has arguably become part of the Roadmap process. The breakdown of other success factors follows:

Category	#	%
Active and supportive role of research consortia, especially Sematech	9	38%
Psychology of engineers (authors of Roadmap)	6	25%
Unique technology (Moore's Law legacy, historical exponential progress)	3	12.5%
Proven process	3	12.5%
Driven by industry's common purpose	2	8%
Other	1	4%

Active and supportive role of research consortia, especially Sematech:

- Sematech preceded Micro Tech 2000, allowed common knowledge as mutual benefit. Sematech culture contributing factor: many TWG co-chairs from Sematech.
- Sematech role in Roadmap is continuity year-to-year, consistency, one message; focal point, collection point, resource; big investment
- Success of Roadmap comes from Sematech's involvement. Linda Wilson's thorough editing ensures consistency cover-to-cover. Also now the Roadmap is web-based. It has served as a benchmark for other roadmaps including Japanese publications.
- SRC, then when Sematech had established culture essential for Roadmap: Collectively discuss in a social process fiercely competitive issues.
- Roadmap compatible with mission of Sematech: 10-15 member company consortium that builds consensus on a portfolio of projects among other things.
- Sematech consensus process ingrained since most TWGs are chaired or co-chaired by Sematech personnel.
- Sematech and Roadmap is a logical connection. Early Sematech: there were no secrets (all the same secrets). Wouldn't have had semi folks sending the best people without Japanese crisis. Japanese crisis was the catalyst that brought the industry together (Sematech), but once together then they shared (Roadmap).
- Participation done on a "volunteer" basis (over and above job), but Sematech taking active role by providing co-chairs on many TWGs. 80% of major university players represented as participants on TWGs, provides credibility, supported by top management in companies. Need to do on a regular basis. Sematech involvement to show leadership, global business very complex, needs structure, model, system driven. Becoming imbedded within organizations' business models, both at strategy and tactical levels.
- Roadmap has become credible because of who sponsors and the level of resource that goes into it.

Psychology of engineers (authors of Roadmap):

- Ironically, group of engineers (miscast, misunderstood) have developed a successful roadmap process.
- Look at red spaces in past Roadmaps and see what happened to them (to turn from red to yellow to white) - "we'll figure it out" attitude prevails.
- Optimism or "field of dreams" attitude needed for Roadmap to be successful - can't look at Roadmap as a one-way street or dead-end, but a means to identify needs that the industry (firms) needs to address through R&D.
- Past successes have something to do with it - we've been able to do it - when I came to work here the one micron barrier loomed big of course. And there were those prophets of doom who said, "you will never get past 1 micron - it's against the laws of nature" In fact, we did - we went through it and didn't even notice it. Today, 100 nanometers sounds like a formidable barrier - but we will get through it. My view is that the bulk planar CMOS device we've been building will probably change in structure in time. It will still be a CMOS technology, still be silicon, but it might not look the same - we'll have to re-engineer it. And I think by doing that we can probably go another order of magnitude in shrink with this technology before we have to invent something else.

- This is an important point that is not really understood: so long as there are engineers - this is an interesting community to watch, in action. Their nature is order, problem solving, and if you look at other roadmaps in other industries where there is some engineering but it is mostly management types or they don't have the same motivation and when you draw this and unique to this technology as well because it is on an exponential. But when you draw this and you stop here today and the future as you know two generations out what it will be and you don't have to draw the line. The expectation is that engineers know that's where it's going to be - "that's our job." You know to just draw it out and the lay person says gosh, we are going to run out of lithography requirements in 2 years! Because that is what the Roadmap does. But say the word challenge to an engineer, how can you beat that, how do you get around that, how do you work, "engineer" your way around that? And enough of that churning goes on that guess what, we just pushed this time frame out.
- One of the benefits that the SIA Roadmap has over other industry roadmaps is that it's authored by engineers. It's authored by folks who are doing the work, as opposed to marketing types, or people that are apart from - even product planners or product managers who aren't part of the technology. The down side to that or trade-off is that there's a tendency to want to get too detailed. And I think a certain fuzziness should be in there rather than too detailed. It's the consistency of the detail, and sometimes they insist on the consistency, and that's what causes the problem. In my opinion if you insist on consistency, there should be a very small set of parameters - that small set needs to be consistent - everything else is simply depending on the application - you can vary all over the place using the same set of capability.

Unique technology (Moore's Law legacy, historical exponential progress):

- Moore's Law myth or culture: can't really describe it. Industry dealing with alchemy: gold out of lead: device > system > architecture > frequency > "cleverness." Moore's Law: boundaries for chip size, scaling (litho makes happen), "cleverness" factor led to extreme competition to do something about it. Enter the Roadmap: Noyce and others at Sematech (Sporck, Galvin, etc): they had vision - we engineers can't innovate in a box. Productivity focus: can't waste resources, collectively saves money, etc. (cooperate vs. individually), also fosters regional competition.
- What this operation indicates is that roadmaps work pretty well as long as you are not dealing with inflection points. And the flat panel display people in this country are tying to get back into general display business. They needed to take the Japanese roadmap or something like that to try and do the next step or try to beat them in the next step. Well the interesting thing there is there are other alternative technologies that are coming on very strongly in displays and that is what the US primarily and DARPA in particular has been investing in. In other words, they are creating an inflection point in the display market. So I think for a different kind of display applications that different other technologies will probably be required.
- Well one of the problems with the Optoelectronics Industry Development Association (OIDA) roadmap, was that there were two many different technologies that were involved and they hadn't reached a dominant design phase yet so they didn't know what their next step would be.

Proven process:

- The process (people, consensus-building, etc.).
- It is NOT a one shot process: the moment it's done it's obsolete.

- Roadmap seen as a successful "process" (not just a book).

Driven by industry's common purpose:

- Driven by industry, not universities or government: all are committed.
- Roadmap not about "getting rich" (egalitarian/common purpose brings people together). Industry really not about getting rich either - happened by accident (high-tech).

Other:

- The Roadmap is "unique experiment that's never been done before"

44. Is there any possibility that the Roadmap process will end? Why or why not?

This question was not asked until well into the field research phase so there were only 9 responses. The reason for asking this question was to test a hypothesis that emerged in earlier interviews: that the Roadmap had developed a life of its own and thus would continue. The results – although limited – seem to bear this out: all but one or 89% replied that the Roadmap process would NOT end. The one who replied that it would eventually end "as we know it" based the answer on historical precedent while suggesting – in effect – alternative roadmaps as the means to continuation.

No, will continue:

- The SIA Roadmap has become an ongoing, "never-ending" process - very formal process.
- Plan to continue activity - now a continuous process through RCG/IRC efforts (used to be every 2 or 3 years).
- Asked question, "Do you see a time when a roadmap is no longer needed?" Response was rephrasing of question: "Will there be a time when collective research in semiconductor technology will not be required?" Answer: "Don't think so."
- Roadmap is a very useful document, many people volunteer their time and energy - it will continue.
- Roadmap won't stop but will become routine (second nature), thus will lose its "pizzazz" (interest by press and others).
- No, I think it is here to stay. It is institutionalized and it serves an important function of basically having people communicate and galvanizing the infrastructure that is needed for the whole industry. Even if the industry changes, roadmapping will continue. If there is something else going on here that is going to change this Roadmap then I think the same roadmapping process will be used to jump on that bandwagon.
- You lose the integrating force behind the consortium if you pull roadmapping away. Because what other reason would people have to be in a consortium but to accelerate their learning and build standards. The way they used to participate was to sit at a table looking at each other and wonder who would make the first move. Those were the meetings I sat in on in the early 80's. Now the interactions are different - "when are we having the next meeting, who got all the action items, and if you can't get the data I got some I can bring." If we have problems we can help solve them. We attack these challenges together so actively that I think we now almost go to the other side and say - don't give away too much information. But the final

analysis in what we are doing inside each of our companies is done so differently that you can share the knowledge but it won't do anybody any good.

- We have learned very simply if you provide your customer with more capability for the same dollar, year after year, then you'll be able to grow your markets. That's a real simple idea - that's what we've done - real simple: each year we give you more for the same amount of money: more functionality, etc. We do this exponentially - we've been able to do this for two decades now. That's what Moore's Law says: well, surprise, surprise, it really works. And so this industry is determined to keep doing that - it sees that as a way of success, growth. My opinion is that we will find a way to push the Roadmap - I'm guessing - at least the CMOS era - maybe ten or fifteen more years.

Yes, will end at some point:

- Suspect that Roadmap and even Sematech might "peter out" after a while: historically things like this only last a little more than a decade or so. Cautious about the evolving nature continuing (MT2000 > NTRS > ITRS > future?). The purity of the roadmap idea is in importance of "laying track" on what's known, need to be very careful not to mix (e.g., alternative device structures) and dilute the Roadmap. Instead, consider parallel paths (other roadmaps).

Appendix C: Moore's Law Retrospective from 2004

Much has been written about Moore's Law since 1996, and much more has been learned by this author regarding innovation within the semiconductor industry. With the original article (Chapter 8) as a basis, this section will address three subjects: 1) important corrections and amendments, including reflections, 2) significant changes in context from 1996 to present (February 2004), and 3) a summary of other interpretations of Moore's Law as they pertain to industrial cadence and the ITRS.

1. Corrections, Amendments, and Reflections

The article, when published in *IEEE Spectrum* in 1997, received a significant amount of interest and generally favorable feedback. More than a dozen e-mails were received from readers within a few weeks of publication and at least that many have been received since. Two readers posted letters to the editor in a subsequent edition. Further, the *IEEE Spectrum* article has been cited by others in a wide range of literature, from academic articles to newspaper stories, however the actual number of citations is not known. More surprisingly is the amount and type of feedback received on the original article which was posted online at the author's Ph.D. student webpage in 1996.[1] Citations of this article have also been found in a variety of publications.

Why 18 months?

The most cited correction was the statement that in 1975 Moore revised upward the annual density-doubling rate to 18 months. Moore has repeatedly stated, "I never said 18 months" and in turn this author has been reminded as often. The reason for the error is at the same time simple and more complicated. It is addressed here in detail because it is revealing of how Moore's Law, based on a simple observation of three data points, has grown to something with such authority that it is referred to commonly as a *Law* (in upper case) while words such as axiom, maxim, dictum, rule, and others suggesting "truth" are used to describe it. It is all part of the mystique of Moore's Law that has caught the attention of so many.

The simple answer to the error is incomplete research on this researcher's part who took at face value a statement (i.e., Moore's Law is defined as an 18-month rate of circuit density doubling per chip) and failed to verify its validity in published literature. The author even interviewed Gordon Moore extensively about Moore's Law and completely overlooked the matter. In short, I got it wrong.

The more complicated answer is that the author accepted the 18-month rate much like everyone else and thought he had verified the 18-month rate with Moore's own charts, thus was surprised when so many were quick to correct him. This will be explained shortly. To begin it is important to understand that when this research was conducted in late 1995 and early 1996 copies of the original articles concerning Moore's Law were scarce. In fact, the author was only able to locate the famous three and one-half page (with 3 illustrations) 1965 *Electronics* article at Intel headquarters and it took them a week to find a copy, which was of poor quality. Today of course all this (and more) is available at their website.[2] But then it was a much different question. The consequence was that the author did not obtain a key document, the 1975 update, another

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[1] See http://mason.gmu.edu/~rschalle/moorelaw.html

[2] The "original" article in pdf form is available for download at the Intel website. This version is actually not an image of the original; it is a retyped reprint with the three graphics (actually four including Moore's photo) scanned and inserted where they appeared in the original. Interestingly, the blemished copy faxed to the author from Intel on April 9, 1996 bears the same two random dots in the graph extrapolating forward from 1965 to 1975 that appear in the pdf file version now available at the Intel website.

short, three-page (with 5 illustrations) article where Moore revises his forecast and clearly states that the annual doubling rate stated in the 1965 article might slow by a factor of two to every two years as follows:

> With this factor disappearing as an important contributor... The new slope might approximate a doubling every two years, rather than every year, by the end of the decade.[3]

This author would not find this out until a reader of his article pointed out the mistake and provided a citation.[4] The author was fortunate to have received from Moore a copy of a 1995 presentation that contained all the charts from the 1975 update (and more) including a chart that showed the revision but did not show values nor contained any statement indicating how much change.[5] Figure C-1b represents Moore's 1975 replot. The second curve labeled "LIMIT" illustrates "a new slope [that] might approximate a doubling every two years, rather than every year, by the end of the decade." Moore had explained this chart to the author but not with any particular values. He simply said that he determined in 1975 that the annual doubling rate would (and actually did) slow down.

Recall that 18 months was, by then (1996), almost-universally accepted as *the* definition of Moore's Law. The author even found and included an equation (i.e., Circuits per chip = $2^{(year-1975)/1.5}$) that pegs the start date at 1975 and the factor at 1.5.[6] Taking this definition at face value, the author presumed that the revised slope in this chart reflected this slower doubling rate. Examining Moore's analysis (from his 1995 documents) of the three factors contributing to the yearly doubling rate revealed that increased die size and dimension reductions (finer device structures) supplied "approximately half" of the progress and the residual was referred to as "device and circuit cleverness." It was this latter category, often shortened to simply *cleverness* that Moore refers to in the quote above as disappearing, thus the basis for halving the slope. However, the actual graph that Moore used shows not half and half, but about an equal contribution of all three factors (see Figure C-1a). This rough estimation was the basis for the statement in the article, "roughly one-third of the exponential remained unexplained." Further, examining both charts together shows that the new "LIMIT" curve (Figure C-1b) is the same slope as the sum of the first two factors curve labeled "PRODUCT OF DIE SIZE AND DIMENSIONS" (Figure C-1a). Hence, an 18-month slope (reduction of about one-third) did not match with what Moore had stated (approximately half) somewhat casually in the 1995 paper but more clearly in the 1975 paper (I would later learn). Moore even noted the ambiguity in his 1995 analysis:

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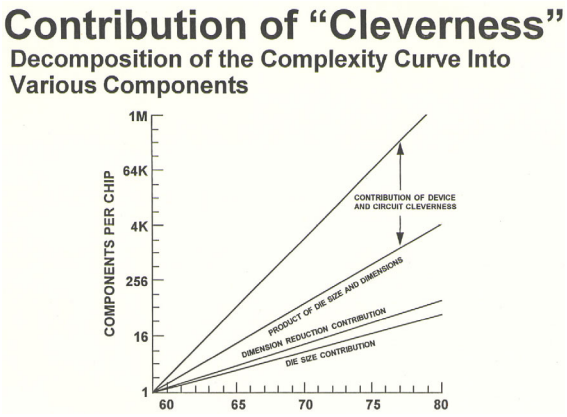
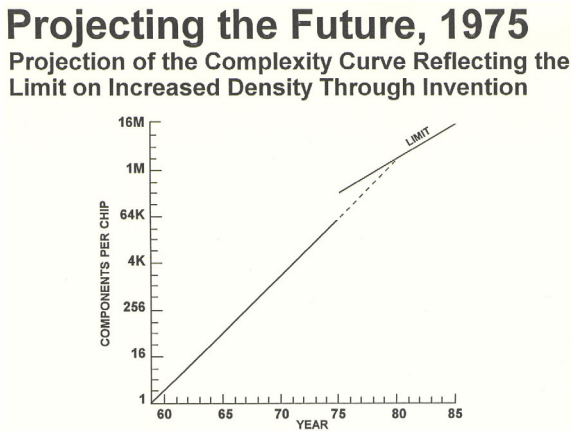
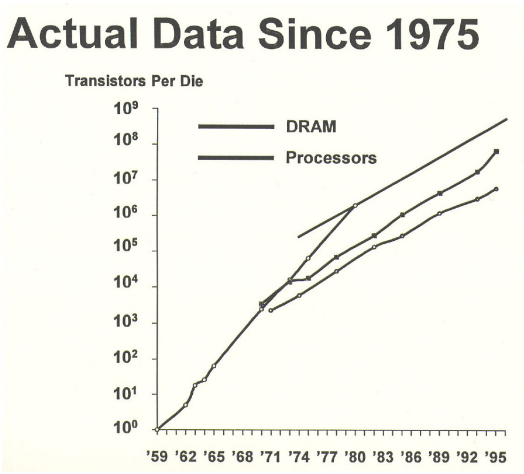
[3] Gordon E. Moore, "Progress in Digital Integrated Electronics," paper given at IEDM, December 1, 1975, 13.
[4] Ibid., 11-13.
[5] Also provided was an accompanying article included a narrative explaining this and other charts but the wording differed from the 1975 article. See Gordon E. Moore, "Lithography and the Future of Moore's Law," paper given at SPIE, February 20, 1995.
[6] Original source unknown.



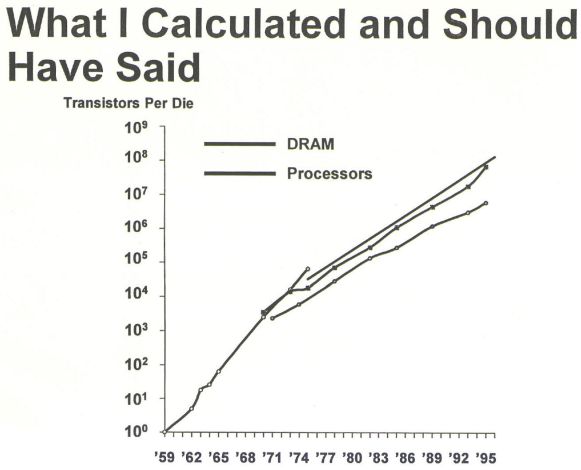
(a) Slide 13



(b) Slide 14



(c) Slide 15



(d) Slide 18

Figure C-1. Moore's SPIE 1995 Charts

Source: Gordon E. Moore, "Microlithography Symposium," Presentation at 1995 SPIE, February 20, 1995.

> Looking at this plot, I said that approximately half the progress had come from die size and finer structures, the remaining half from "cleverness". If one looks closely, however, more than half comes from the first two factors, more like 60 percent. I didn't think that the data was good enough to push this much, however, so I stuck with half.[7]

Note that a slope of 60% produces a doubling rate about every 20 months. This is actually the slope that Moore plotted forward, to begin in 1980. Moore also stated during his interview with this author:

> But if I had pushed the data harder, further than what it really should have been, my projection would have been right on.[8]

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[7] Gordon E. Moore, "Lithography and the Future of Moore's Law," paper given at SPIE, February 20, 1995, 7.

[8] Moore interview, 1996.

Like he did in 1975 with actual data since 1965, Moore compared actual data since 1975 against his replot (Figure C-1c). Although, different than his previous comparison the data did not fit as well. One major factor was the timing of the inflection. He had predicted in 1975 that this would be delayed until about 1980 (note dashed line in Figure C-1b) because of internal new product knowledge he had. But as has been previously reported, these products (namely CCD memories) did not materialize as planned. So the complexity curve changed slope immediately (actually it had already begun as new product families from the early 1970s began to exhibit unique scaling patterns, see Figure C-1c). Finally, Moore adjusted his 1975 replot by starting it earlier (in 1975) and increasing the slope to fit the actual data for DRAM devices (see Figure C-1d). He humbly called this chart, "What I calculated and should have said." The actual change in slope is slight but noticeable (compare Figures C-1c and C-1d), hence in a range closer to 18 months (if not less).[9] This was the chart that Moore was describing to the author when he made the previous statement, "had I pushed the data harder … my projection would have been right on."

This author took this to mean 18 months, again the accepted definition at the time. The actual number was not addressed with Moore, neither of us reached for a protractor to check the slopes, it was approached in the spirit of learning from experience. Basically, if the plot didn't fit the data you changed it to fit; it was no big deal. Therefore, while it may seem to be nit-picking now, a debate over 18- vs. 24-months as the doubling rate was not considered a major issue then (at least until after the article was published). Considering all this the author logically concluded that a rate closer to the conventional 18-month rate really seemed to have some theoretical basis, thus the carefully chosen wording, "eighteen months seemed to be a reasonable rate." [10]

The lesson in all this is that Moore prepared and used these charts as illustrations supporting the general argument that semiconductor technology advanced at an exponential, and fairly predictable, rate. To be credible required engineering-like analysis. The problem was the data—there was not enough or it was not firm. But Moore was not writing a dissertation, he was trying to make a simple but powerful point to a broad community of not only engineers, but managers, investors and others involved in the young semiconductor industry. Hence, Moore used the data along with the simple forecasting technique of extrapolating the few data points forward with a ruler on semi-log paper to generate his famous "plot" in 1965. When validated 10 years later it was revised in much the same way, with some but certainly not complete engineering precision. Another reexamination 20 years after this would call for further tweaking. And on it goes. Despite the shortcomings in the charts they have been generally accepted, perhaps because they are simple and do, in fact, prove Moore's point. While much discussion and debate have ensued over the analytical integrity of Moore's charts (including this author's own interpretation as described above) they still stand. In some sense they are not subject to debate; they just are, just like Moore's Law.

A Simple Plot Becomes a Law

Returning to the 1975 projection, independently and probably before his 1975 presentation at IEDM, Moore's plot was dubbed a *law* by someone other than him, perhaps by someone else at

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[9] Note that microprocessor devices do not follow the same scaling pattern as packing densities are not as great as in DRAMs. Microprocessor transistor per die doubling rates lag DRAMs by a few months, hence the "safe" general definition of Moore's Law of 18 to 24 months.

[10] Interestingly, see Chris A. Mack, "Using Learning Curve Theory To Redefine Moore's Law," *Solid State Technology*, July 2003, 52, for a more recent but similar line of analysis where Moore's "retelling of the story" at SPIE 1995 resulted "in a doubling of transistor counts/chip ~18 months." Note that Mack's article was based on a paper given as keynote speaker at SPIE 2003.

Fairchild or Intel, or perhaps by Carver Mead as has been suggested.[11] There are only a handful of "Moore's Law" references for the period covering the late 1970s through late 1980s (see Box C-1 and Figure C-6) and the rates vary from 12- to 18- to 24-months including combinations like 18-24 months. By the early 1990s though, 18 months seemed to have emerged as the accepted definition. Whether this was simply splitting the difference between 12 and 24 or actually fitting performance backward to 1975 as Moore "calculated and should have said" is not clear. However, like Moore's charts and Moore's Law, 18 months just is.

Box C-1. Early Moore's Law References from Fairchild and Intel

Moore's Law has been cited in the literature countless times. This is a sample of some of the earliest uses and definitions of the term by Fairchild and Intel personnel.

The first published references to "Moore's Law" by Fairchild or Intel personnel the author has found were in 1977 and in both cases *law* is used in lower case.

In the first known reference the term is used often by C. Lester Hogan, "Reflections on the Past and Thoughts About the Future of Semiconductor Technology," *Interface Age*, Vol. 2, No. 4, March 1977, 24-36. Hogan, then Vice Chairman of the Board of Fairchild, refers to Moore's 10yr thousand-times complexity projection in his 1965 paper and states "This has since come to be known in the industry as Moore's law and it has been an extremely accurate projection of the industry's capability for the past ten years." (32) Later in the paper he asserts, "one gets a view of the future by extrapolating the performance of LSI chips to 1985. According to Moore's law, a single integrated circuit chip will have more than 10,000,000 components interconnected by 1985. (36) Hogan has carefully incorporated Gordon Moore's December 1975 IEDM projection of device density doubling on a yearly basis until 1980 when Moore reduces the rate of doubling to every two years. Going forward from Moore's starting point in 1975 at 64K (actually 65,536) components, a 1985 device could contain more than 11 million components.

Robert N. Noyce, then Intel's Chairman, writes in "Microelectronics," Introduction to A *Scientific American* Book, San Francisco: W.H. Freeman and Co., September 1977, that "Today, with circuits containing 2^{18} (262,144) elements available, we have not yet seen ant significant departure from Moore's law." (5) He defines "Moore's law" as a doubling each year.

Moore himself used the term (in upper case) in the April 1979 issue of *IEEE Spectrum* where he refers to the "Moore's Law" limit in a graph in Gordon Moore, "VLSI: some fundamental challenges," *IEEE Spectrum*, April 1979, Fig. 3, 34. In the same issue Roger Allen, "VLSI: scoping its future," 31, defines Moore's Law as "a doubling of IC device densities every year." The *limit* Moore refers to had been labeled as such in his December 1975 IEDM paper (Figure 7-4b). The slope of the curve appears to reflect the milder, every two years doubling rate. He defines this curve or frontier as the "limits of device complexity" and notes that few Intel products in 1977 and 1978 approach this limit.

Patrick P. Gelsinger, Paolo A. Gargini, Gerhard H. Parker, and Albert Y.C. Yu, all from Intel, state

[11] Moore interview, 1996. Also note that Figure 6-7 in Chapter 6 is taken from B. Hoeneisen and C.A. Mead, "Fundamental limitations in microelectronics. I. MOS Technology," *Solid-State Electronics*, Vol. 15, 1972, 819, Fig. 1 which caption reads "History of integrated circuit complexity. Line corresponds to a two-fold increase in the number of components per chip per year. This figure is due to Gordon E. Moore." The data plotted on this graph are basically the same points through 1972 that later appeared in Moore's 1975 IEDM paper. Hoeneisen and Mead continue the annual doubling rate forward to 1980 where they state a possible limit for dynamic MOS transistors might be met. Interestingly, this is the same projection that Moore makes in 1975. Moore does include more recent data from 1973-1975 in his chart, but his continuation also ends in 1980 when it changes to the milder slope. Thus it is possible that Mead not only coined the term Moore's *Law* but helped Moore make the argument by providing this early chart with a MOS scaling theory that would carry at least through 1980.

"Moore's Law: at least a doubling every two years." in "Microprocessors circa 2000," *IEEE Spectrum*, October 1989, 46.

In 1990 Andrew S. Grove, then Intel's CEO and President, states in "The Future of the Computer Industry, *California Management Review*, Fall 1990, 148, "Moore's Law: it posits that the transistor density that is feasible on a chip doubles every 18 months."

The more likely source to the 18-month rate is the historical progress of DRAMs as shown in Table C-1. Note the pattern of 4-times capacity increases almost every 3 years. The pattern was so noticeable that new each device type was referred to as a new *generation* as described in Chapter 4. A million-fold increase in thirty years (i.e., 1K in 1971 to 1G in 2001) represents 20 doublings (2^{20}). Restated in Moore's density doubling terms, this represents a doubling every 18 months.

Table C-1. Device Density in DRAMs 1971-2001

DRAM Device Type	Volume Production Year
1K	1971
4K	1974
16K	1977
64K	1979
256K	1983
1M	1986
4M	1989
16M	1991
64M	1994
256M	1998
1G	2001

Sources: 1K through 1M from Jeffrey T. Macher, David C. Mowery, and David A. Hodges, "Reversal of Fortune? The Recovery of the U.S. Semiconductor Industry," *California Management Review*, Vol. 41, No. 1, Fall 1998, Table 1; 4M through 1G from Randall D. Isaac, "Beyond Gigahertz and Gigabit Chips," PowerPoint presentation, undated, received 2001.

Figure C-2 follows the general pattern of Moore's 1995 "what he should have said" chart and represents a more recent plot (through 2000) of the two distinct trend lines. The data in Table C-1 match fairly well with the top DRAM line of this graph.[12] The respective "Law" lines are fitted by regression according to the authors.

[12] Dates differ on some DRAM device types by one or two years. Raw data is as follows: 1K 1970, 4K 1974, 16K 1975, 64K 1978, 256K 1982, 1M 1985, 4M 1989, 16M 1993, 64M 1995, 256M 1999. Annual coefficient used is 49% CAGR in bit count which approximates a doubling rate of every 20 months.

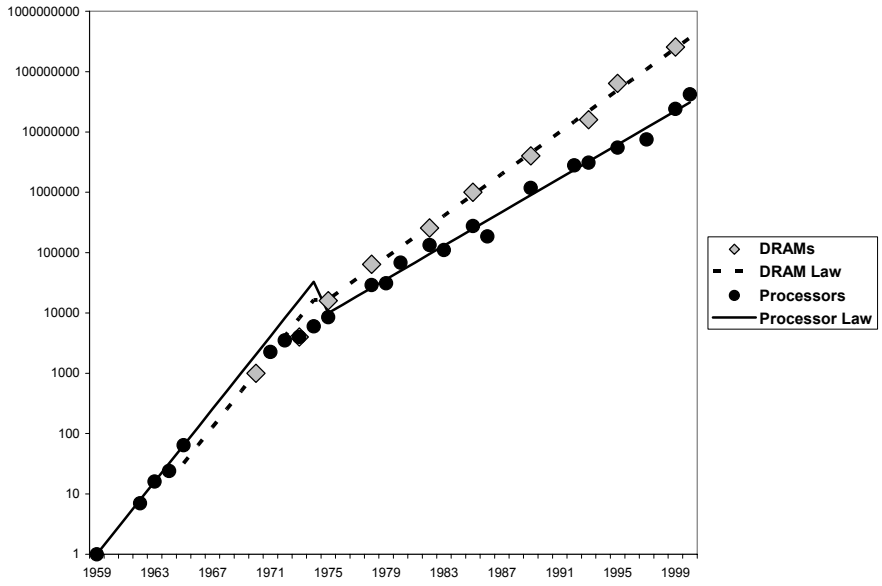

Figure C-2 Moore's Law Versus Actual Chips (number of bits or transistors on one chip)

Michael L. Barnett, William H. Starbuck, and P. Narayan Pant, "Which Dreams Come True? Endogeneity, Industry Structure, and Forecasting Accuracy," *Industrial and Corporate Change*, Vol. 12, No. 4, 2003, Figure 1, 655

DRAMs did not yet exist when Moore made his original plot in 1965. Recall that he and Noyce would in fact later leave Fairchild and found Intel to pursue solid state memories. Moore's Intel would introduce the world to DRAMs and be a dominant player in this market until it withdrew in the mid 1980s (see Chapter 3). However in 1975 when Moore replotted his graph, only a few generations of DRAMs had been produced so there was little scaling experience with the new device.[13] Thus DRAMs, although they appear on Moore's 1975 charts, may not have yet carried great influence on the slope of overall IC progress. But ten years later the DRAM had become the industry's *technology driver*, which meant among other things that it was the global volume and sales leader. As DRAMs went so went the industry. Recall also that during this ten year period (1975 to 1985) the Japanese VLSI program was launched and Japanese chipmakers eventually overtook American chipmakers in global DRAM leadership. As just stated, Intel (and others) withdrew entirely from the business.

Moore did not revisit his charts in 1985 as he had done ten years earlier. He would not do so formally until 1995 when he was in the twilight of his career at Intel, by then the most powerful company in the industry. During this long stretch Moore's Law was elevated to a status that had gone beyond him. Gordon Moore was no longer the sole keeper of Moore's Law. For a long time Moore actually resisted the use of the term stating, "It used to grate on me. I kind of cringed when anybody said Moore's Law. I wasn't very comfortable having something called a law named after me. It wasn't a law in any real respect."[14] In fact he told this author of his refusal to call it "Moore's Law" until the early 1990s when he eventually "just gave up."[15] Moore's distaste for the phrase may partly explain the long absence of coverage—lasting throughout the 1980s and into the early

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[13] The term "generation" denoting a scaling pattern probably did not yet exist.
[14] Gordon Moore, in interview with Dori Jones Yang, "On Moore's Law and fishing: Gordon Moore speaks out," *U.S. News*, July 10, 2000, http://www.usnews.com/usnews/transcripts/moore.htm
[15] Ibid.

1990s—of Moore's Law associated with him in particular. Recall that others at Intel were using (and modifying) the term during this time (see Box C-1). Moore reflects on finally embracing the notion:

> You know it's funny, I used to think it was kind of ridiculous, thinking if the thing I ended up being remembered for was this [Moore's Law]. It was absurd. But it's gotten picked up as just about anything that's a straight line on semi-log paper related to industry, so I take credit for all of it.[16]

This extreme attention devoted to "why 18 months?" seems at first trivial, but it is grounded in the precision found within an engineering culture and more importantly within the culture of Moore's Law as will be discussed shortly. A second and related concern was raised by several readers, including one who submitted a letter to the magazine's *Forum* in a subsequent issue:

> In Fig. 4, Schaller presents data to support Moore's Law. The figure shows transistor count per die plotted against year of introduction for commercially available dynamic RAMs and Intel microprocessors since 1970. According to the caption, the data show that the microprocessors and dynamic RAMs have followed the law that complexity doubles every 18 months. But I calculated the rate of increase and found that for dynamic RAMs the complexity doubles every 22 months, and for Intel microprocessors the doubling period is a little over two years…
>
> Before discussing whether Moore's Law will continue to hold true in the future, we should decide whether—and in what form—it has held true in the past.[17]

Has Moore's Law Really Held True?

The second criticism of the article has to do with whether Moore's Law has actually held up to any stated rate, whether it be 12-, 18-, 20-, or 24-months. Again this may at first seem trivial but there has been much debate over the empirical evidence as captured briefly in the reviewer's caption above. The broader question is twofold. The first concerns the specific rate as expressed above. The second concern is more about the regularity, thus the predictability of the pattern if used prescriptively.

The concern regarding differences between the stated rate and actual performance has been raised before. When this occurs some quip that it is part of an effective Intel PR campaign. While there may be some merit in this the reality is that these rates are rough approximations as is evident from the previous discussion. Further, the actual numbers can be problematic (this is even more the case with historical roadmaps as will be discussed later) as the definition of the data elements has changed over time.[18] In 1965 Moore used minimum component cost as the parameter for ICs selected, but by the late 1970s he referred to highest complexity chips available. Additionally, Moore's initial unit of measure was *components* per chip which encompassed transistors but also other supporting devices such as diodes, capacitors, and resistors. But by the mid to late 1970s *transistor* count had become the key measure (e.g., compare differences in vertical axis labels of Figures C-1a and -1b with Figures C-1c and -1d). This can be significant if combining data from the two timeframes as is often done. For example, Intel's state-of-the-art 16K DRAM or CCD memory chips in 1975, made up of more than 16,000 transistors, also contained about the same number of capacitors. Using the original definition this would represent 32K components while the revised definition (as transistors per die) halves this total. This partly explains the abrupt change in the location (i.e., lower starting point) of the revised curves shown in Figures C-1c and -1d). In other words, the two plots represent apples and oranges to some degree. Furthermore, the dates selected for the data points may vary from

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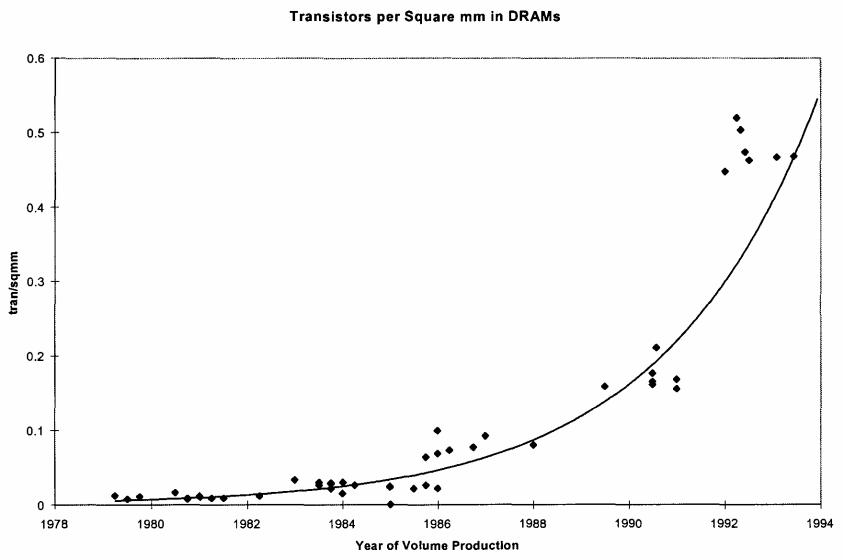
[16] Ibid.
[17] Michael G. Kane, Letter to the Forum, *IEEE Spectrum*, August 1997, 8.
[18] Note that Tuomi points out these important distinctions regarding changes in definition. See Tuomi, op. cit.

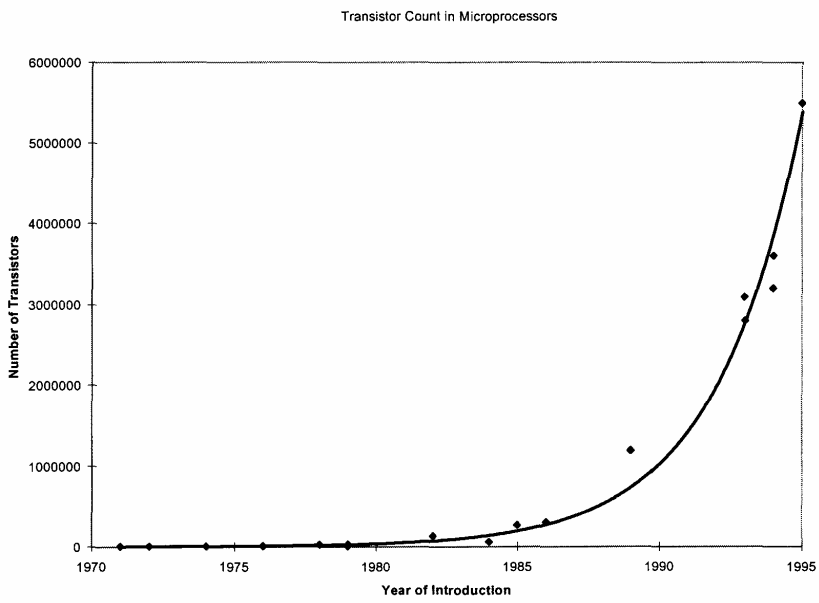
laboratory demonstration to volume production, a period that can span years. There was always "something in the lab" included in the early graphs. The consistency of this parameter has been improved with time, tending to use volume production, but the choice of dates for earlier data points, as few as there were, was not always the best for longitudinal measurement purposes.

A few examples of others' analysis of actual performance are discussed briefly. Ethan Mollick (1997), in his senior thesis at Harvard, pointed out that data for five generations of commercial introduction of DRAMs between the late 1970s and mid 1990s "fell into an exponential curve that approximated a 31 percent improvement per year, or doubling around every twenty-six months."[19] Similar results were found for Intel microprocessors as shown in Figure C-3.



(a) Transistors per square mm in DRAMs[20]

[19] Ethan Mollick, *Foundations of Sand: Moore's Law and the Semiconductor Industry*, Senior Thesis, Harvard University, March 1997, 36.
[20] Ibid., per the author data courtesy of Marcos Iansanti: 43 data points included in data set.



(b) Transistor count in Intel Microprocessors

Figure C-3. Transistor Density Trends of DRAMs and Microprocessors

Source: Ethan Mollick, *Foundations of Sand: Moore's Law and the Semiconductor Industry*, Senior Thesis, Harvard University, March 1997, Figures 5 and 6, 35, 37.

In an incisive piece titled, "Moore's Law … The mother of all engineering laws," Dan Hutcheson, a respected industry analyst who has probably studied Moore's Law more intently than anyone, points out that the doubling rate has changed over time, gradually slowing down, then speeding up:

> The doubling period had stretched out to an average of 17 months in the decade ending 1975, then slowed to 22 months through 1985 and 32 months through 1995. It has revived to a now relatively peppy 22 to 24 months in recent years… "It's averaged every two years since the late 1970s, although Intel's PR department likes to average the earlier number with the later and call it 18 months."[21]

Perhaps the most critical assessment is Iikka Tuomi's "The Lives and Death of Moore's Law" (2002).[22] Tuomi attempts to argue many points in his article but a central theme is the assertion and demonstration that Moore's Law is invalid. He uses several metrics and diagrams such as Figure C-4 that portrays three different eras of progress for Intel microprocessors with each one slowing.

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[21] G. Dan Hutcheson as quoted in Philip E. Ross, "5 Commandments: The rules engineers live by weren't always set in stone," *IEEE Spectrum*, December 2003, 32.

[22] Iikka Tuomi "The Lives and Death of Moore's Law," *First Monday*, Vol. 7, No. 11, November 2002, http://www.firstmonday.org/issues/issue7_11/tuomi/index.html

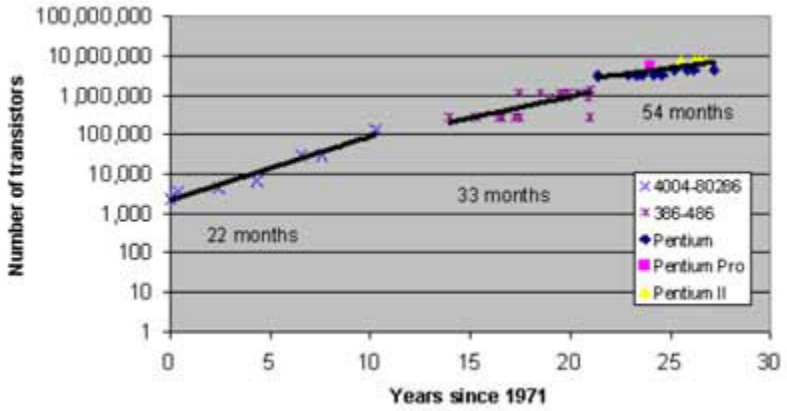

Figure C-4. Tuomi's Rendering of Intel Microprocessor Progress in Transistor Count

Source: Iikka Tuomi "The Lives and Death of Moore's Law," *First Monday*, Vol. 7, No. 11, November 2002, http://www.firstmonday.org/issues/issue7_11/tuomi/index.html, Figure 3: Number of transistors on Intel microprocessors.

Tuomi concludes, among other things, that progress according to Moore's Law is an "illusion":

> Semiconductor technology has not developed according to Moore's Law. The claims that future developments in semiconductors, computer technology, or information processing would be determined by the continuation of Moore's Law are, therefore, obviously invalid… [R]eferences to Moore's Law qualitatively miss the character of development in semiconductor technology and the information society… In other words, the apparent explosive big bang of semiconductor technology is also an illusion.[23]

Assertions such as these have generated much discussion and debate. One particularly engaging retort is from Ray Kurzweil, noted inventor and author, who has written about Moore's Law for more than a decade.[24] Suffice it to say that not everyone agrees that Moore's Law is invalid. At the same time, Moore's Law has not always behaved with the regularity of popular claims, whatever the rate of doubling. From a purely analytical view, the above references may simply represent an academic debate around statistical methods: which points does one choose to measure? From a broader perspective, though, is the question of usefulness of such a phenomenon.

How Much Does Culture Matter?

One factor that is notably absent in analysts' debates and discussions over doubling rates is the role of culture, the set of key values, beliefs, understandings, and norms that members of a society, organization, or in this case *industry* share. While analysts may question the validity of the "rate" (and have good reason) in some sense this is but an academic exercise. Moore's Law has taken on a life of its own; it transcends even its namesake as previously discussed. A noted futurist likens it this way: "Moore's Law may be after the microprocessor, the single most

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[23] Ibid.
[24] Ray Kurzweil, "Exponential Growth an Illusion?: Response to Ilkka Tuomi," http://www.kurzweilai.net/meme/frame.html?main=/articles/art0593.html Also see Raymond Kurzweil, "The Paradigms and Paradoxes of Intelligence: Building a Brain," *Library Journal*, November 15, 1992, Vol. 117, No. 19, where he states "Moore's Law, the driving force behind a technological revolution, says that computing speeds and densities double every 18 months."

important contribution Intel's made in the industry."[25] Moore's Law is a distinct part of the culture within the semiconductor industry and carries with it tremendous, almost religious influence. For instance, Schulz statement at the beginning of Chapter 8 that Moore's Law "has become gospel." Culture is as important a factor as technology and economics behind the idea of Moore's Law as a self-fulfilling prophecy (see Box C-2 for an alternative explanation). Similarly, embodied in Chris Mack's opening quote, "Moore's Law is not a law; it is an act of will" and Carver Mead's "belief systems" interpretation is culture. Similarly, a few informants spoke of Moore's Law as an "act of faith." Simply put, the heritage of the semiconductor industry is to keep Moore's Law going because forty-plus years of experience have revealed the tremendous economic incentives of doing so. It is not done explicitly as one informant described its effect upon workers, "They may not say to themselves explicitly 'my job is to keep Moore's Law going today' but in a sense that's what they're doing. That's what Moore's Law is all about. Nobody's going to stop that. There's a momentum going that is going to continue on." Unfortunately, the implicit nature of this factor does not lend itself to analytical treatment. This is an area that deserves further research to more fully understand Moore's Law.

A few observations are offered as a starting point for future research. An outsider may wonder why Moore's Law is viewed with such importance within this industry, as did this researcher initially. But having been associated with the semiconductor community during this research provided insight that Moore's Law carries with it an industry tradition, legacy, lore, and other such highly-held values. In short, Moore's Law *is* the semiconductor industry; it's what helps make it so unique. Moore's Law is what unknowingly guides engineers and scientists every day in the relentless quest to push the technology past known limits. It's also what drives managers and executives to deliver greater functionality at lower unit cost ahead of their competitors who are working with the same basic formula. The reach of Moore's Law is far and wide. The important community of manufacturing equipment and materials suppliers increasingly follows, and in turn contributes to, Moore's Law as the chip industry continues to disintegrate and specialize. The rapid growth of both fabless and foundry industries illustrates this. At the same time participants located in all parts of the globe, throughout the value chain, share Moore's Law as a form of common innovation language independent of geographic and political borders.

Hutcheson has stated to this author that "Moore's Law is almost a religion. This religious fervor drives the industry. What does the industry do if it stops?"[26] This of course is a rhetorical question, however one that the industry hopes not to have to answer soon. This point was reinforced by several other Roadmap informants where some describe Moore's Law with terms such as: *technology faith*, *myth*, or *culture*. One emphasizes the symbolic value of it: "Moore's Law is an important symbol to the industry. We'd be embarrassed if it was not met!" Summary findings are presented in Chapter 11 while detailed responses are included in an appendix. Summing up, it is well beyond the scope of this research to fully address the role of culture other than to say one cannot simply analyze around such a tremendous force.

Box C-2. Moore's Law as a Self-fulfilling Prophecy through Strategic Behavior[27]

In 1964, Gordon E. Moore, research manager of Fairchild Semiconductor, observed a regular periodic doubling of the number of 'gates' (a measure of complexity), and claimed, by extrapolation, that this would continue. This prediction has come true so beautifully, that nowadays we speak of 'Moore's Law,' as if it were a law of Nature. The validity of this law cannot

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[25] Paul Saffo, Institute of the Future, http://www.intel.com./intel/museum/25anniv/html/int/saffo.htm
[26] Dan Hutcheson, telephone interview, March 10, 2000, Hutcheson is President, VLSI Research.
[27] Excerpted from Harro van Lente and Arie Rip, "Expectations in technological developments: An example of prospective structures to be filled in by agency," manuscript received July 2002 from the second author. An earlier version of this paper was prepared for presentation to the XIIIth World Congress Sociology, ISA, Bielefeld, Germany, July 18-23, 1994.

be understood from the technical procedures by which the chips are made. The fact that the law holds so well is an effect of the way actors (in industry, in science and in government) judge their own and each others' accomplishments with respect to what Moore's Law predicts. They direct their efforts towards achieving the predicted values. Laboratories evaluate and plan their efforts in terms of Moore's Law; when there is danger of specifications falling short at the predicted moment, extra effort is expended. Firms use the law to guide investment decisions in specific technologies; for example whether or not to develop products that need chips with the predicted capacity - such as calculators or compact disc players. Governments are willing to provide subsidies in order to help firms avert the danger of not meeting the predicted value. All actors exert themselves to measure up to the predicted competition and to stay in the race. Moore's Law is the yardstick for the behaviour of chip producers and governments in Japan, the United States and Europe, and it shapes their mutual dependency in the strategic game they play with one another.

Because it holds so well, other firms use a modified version of Moore's Law that claims a reduction in the price per gate of 30% annually. This version allows one to predict the commercial opportunities for products like pocket calculators, compact disc players and videotext systems. Assuming, for instance, that chips more expensive than 10 to 20 dollars are a barrier to widespread use in consumer electronics, one could predict a market for pocket calculators, with their 1K (= 1024 gates) chip, only after 1972, when the price per gate had fallen to about $0.01. By the same token, firms saw opportunities for producing a compact disc player (with its 70 K chip) in 1985, when the price per gate had dropped to $0.00015.

We may speak of a self-fulfilling prophecy, but the fulfilling did not occur because it was a prophecy, but because actors took up the prophecy and acted accordingly. This was a basis for other actors to accept the expectations and act accordingly, etcetera. The promise has now become part of a *prisoner's dilemma*: firms and governments in Europe, Japan (and now also other countries in South-East Asia) and the United States stay in the race for superior chips, even if this requires huge investments, because they do not want to run the risk of falling behind the other parties in the triad. And while not absolutely certain, they strongly suspect the others will continue - simply because chips are a promising technology.

Prisoner's dilemma situations (and similar phenomena analyzed in game theory) are widespread and explain why actors remain involved. However, the model does not explain the nature of decisions and mutual coordination through the content of the technology. The vocabulary of 'generations', and the regularity of generations following each other according to Moore's Law, allow decisions to be made in terms of: which generation are we working on? Can we leap toward the next generation? The antagonistic coordination of the chips race is made possible by 'reading' the opportunities in and requirements for the coming generations of chips. It is only because of this reflexive agency that the division of labour and the strategies allow one to speak of a 'self-fulfilling prophecy'.

The lesson of this example is that actors start to take mutual account of each other because of the opportunities they perceive in the future technology. Initially, the participating actors belong to different organizations and different sectors, but by commonly anticipating a future technology, they become interconnected. These interconnections are not like producer-client relationships or hierarchical relations: actors do not exchange products, but ideas about technology and technical opportunities.

2. Change in Context

The focus now turns to examining the significant changes in context that have occurred between the article's preparation in 1996 and today. Because of rapid product cycles, seven or

eight years in semiconductor technology is a long time. Since the mid 1990s the industry has advanced at least four technology generations (i.e., .from 35u to .25u, .18u, .13u, .1u) and leading-edge producers are already at .09u (90nm).[28] According to the 1994 NTRS (published in 1995) .1u (100nm) was not projected until 2007 while .09u, although not considered a node then, would have fit in at 2008 (i.e., .07u was projected at 2010).[29] The industry achieved the .01u milestone *four years ahead of schedule*. Very simply, semiconductor technology has accelerated. In other words, Moore's Law has sped up. Hutcheson's earlier cycle estimates hinted at this. On the other hand, the industry's economic performance has not been as successful. It is not clear if there is any relationship, however at least one industry member sees one. Bijan Davari, VP at IBM Microelectronics Division, notes a relationship between improved productivity enhancement (i.e., increased density and number of chips per wafer as a result of Moore's Law) and consumption. Discounting for short-term industry cycles, chip consumption has historically grown faster than productivity enhancement, thus prices and revenues have remained healthy. According to Davari, "From the late 1970s up to the mid-1990s, the productivity enhancement was about 100 times for every 10 years. And the consumption rate was about 400 for every 10 years. So revenue increased about four times every 10 years." [30]

But since the mid 1990s, productivity enhancement has risen faster, by as much as 200-300 times per 10 years due to technology acceleration (faster Moore's Law). So in effect the capabilities of chips are increasing faster than customers are buying them. "We are selling more and more chips, but revenues are staying flat or going down."[31] A chief reason behind this is a precipitous decline in average unit prices following a preceding period of increasing unit prices (and profits). This point is discussed as part of the following paragraphs which provide more notable changes in context.

Important Background

Moore's Law started as a simple observation by one who was head of research at the leading semiconductor maker. At the time Fairchild, like others, was vertically integrated and controlled the entire process of chip design, development, and manufacturing. Gordon Moore was directly involved in the products that he reported on. He was more than analyst, he had a hand in contributing to his observation (the single planar transistor starting point was actually his design). Extrapolating from this was certainly risky but Moore was perhaps in the best position to do so.

By 1975 the annual doubling forecast had (almost) been realized. Much had changed in ten years in this industry. Moore was no longer head of research at Fairchild, he had co-founded and was now President and CEO of a start-up firm called Intel which was in many respects a technology leader like his prior firm. But Intel did not control all of its manufacturing processes; by this time a semiconductor materials and equipment industry had emerged. The chip industry was now much larger and no longer the sole domain of American producers. Global semiconductor revenues had grown four-fold to $5 billion as non-U.S. chipmakers increased their global marketshare from about 25% to almost 40%. From 1975 to 1985 the global industry had grown even faster driven by a larger contribution by non-U.S. chip manufacturers who would contribute half of world output by 1985. Due to persistent losses in global marketshare, Intel and other U.S. manufacturers chose to exit the DRAM business, the market that they originally created and that by then was the industry's largest segment.

But between 1985 and 1995 the global industry had grown at an even faster rate, almost six-fold. Intel was now the leading chipmaker designing and producing leading-edge microprocessors

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[28] Intel Press Release, "Intel Introduces Intel Pentium 4 Processors On High-Volume 90-Nanometer Manufacturing Technology," Santa Clara, CA, February 2, 2004, 2p.
[29] Note that .07u was the last node projected in the 1994 NTRS. It represented the end of the 15yr horizon.
[30] Bijan Davari, as quoted in Geppert, op. cit., 77.
[31] Ibid.

they sold by the millions at several hundred dollars apiece. Moore was Intel's Chairman. The U.S. now only represented about one-third of total world output as the global industry continued to expand at record rates. In thirty years Moore had been part of a remarkable transformation. He no longer engineered products but had so influenced the research and engineering process through successful leadership at Intel, strong advocacy of U.S. research consortia, a national technology roadmap process, and increasing admiration of his "law" that it appeared to many that Moore's Law might go on 'forever'.

It was following the banner sales year of 1995 that analysts paid serious attention to "high tech" as the engine driving the new economy (see Figure C-5). It was also in late 1995 that this researcher first took an interest in Moore's Law as *the* possible explanatory variable for this tremendous growth. Industry and financial analysts alike sought answers, consequently Gordon Moore and his *Law* received much attention.

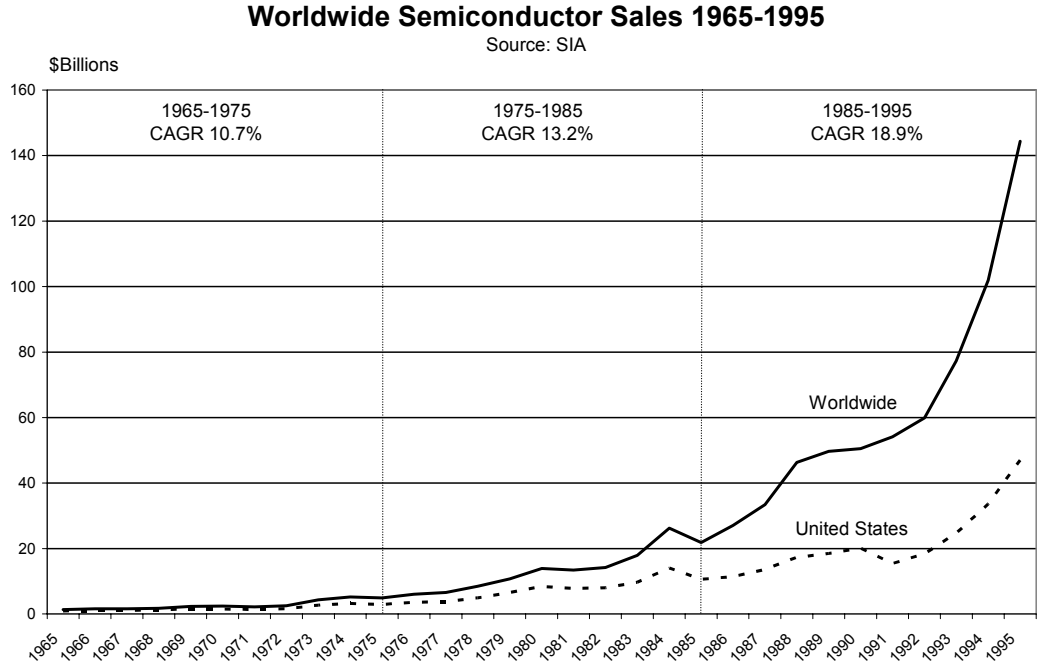

Figure C-5. Worldwide Semiconductor Sales 1965-1995

To demonstrate the increased interest in "Moore's Law," the author attempted to catalog related documents collected since 1996 that now fill more than three 3" binders. These archives include a wide variety of materials. The task proved overwhelming so it was abandoned. In the original paper the author stated, "Out of well over 100 pertinent references, more than two dozen quality references were obtained." This statement was based primarily on several Internet search engine keyword searches of websites and newsgroups at the time (e.g., Yahoo, AltaVista, Infoseek, DejaNews, and others). To determine any change in general interest a few select keyword searches on "Moore's Law" were conducted online on February 22, 2004. The results are shown in Table C-2.

Table C-2. Basic Keyword Search Results of "Moore's Law"

Source	Results
Google http://www.google.com/	about 83,700 hits
Newsgroups http://groups.google.com/	about 19,700 hits
Amazon.com book search http://www.amazon.com/	845 results including a "how-to" guide[32]
FindArticles.com http://www.findarticles.com/	831 articles
ProQuest[33] http://proquest.umi.com	387 articles
EBSCO Publishing[34] http://www.epnet.com/	335 articles

It is very apparent that an increase from 100 to 100,000 (combining both *Google* searches) represents a dramatic, perhaps exponential, increase in general interest. The author had done periodic keyword searches on "Moore's Law" but had not documented the results. Nonetheless, the trend had been recognized earlier. Like the archival materials these results proved too immense to sort through individually as had been done in 1996. So one source was selected (i.e., *ProQuest*, the article database service used by several colleges and universities, including the author's) and the results were categorized by year of publication as shown in Figure C-6.

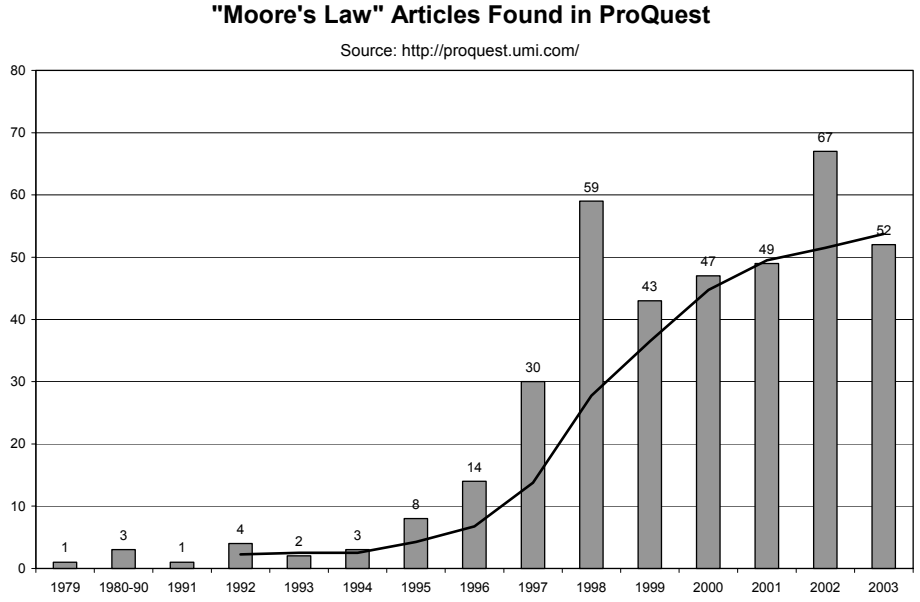

Figure C-6. "Moore's Law" Articles Found in ProQuest by Year of Publication

Keyword Search Conducted February 22, 2004, 387 total articles found (4 to date in 2004)

Trend line is 4yr moving average

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[32] Dana Blankenhorn, *The Blankenhorn Effect: How to Put Moore's Law to Work for You*, Trafford, ISBN: 1553953673, 206 pages, December 2002, $24.95 paperback.

[33] The ProQuest® online information service provides access to thousands of current periodicals and newspapers, many updated daily and containing full-text articles from 1986.

[34] Business Source Premier provides full text for more than 3,650 scholarly business journals, including full text for nearly 1,100 peer-reviewed business publications. Coverage includes virtually all subject areas related to business.

Note the annual doubling of publications over the five-year period of 1993-1998. This pattern almost follows the almost-tripling revenue growth pattern from 1990-1995 in Figure C-5. Historically a cyclical industry, the early 1990s marked a very strong upswing for the U.S. industry in particular following the very tumultuous decade of the 1980s (see Chapter 6). A key driver was increased demand for PCs, which by then accounted for about 60% of semiconductor revenues.[35] Thus strong demand for microprocessors and DRAMs saw their unit prices stabilize and in some cases increase. With the introduction of the Intel Pentium microprocessor, Netscape Navigator internet browser, and Microsoft Windows 95 in rapid succession, strong growth was expected to continue through 2000 with forecasts ranging from $250 to more than $300 billion.[36] Simply extrapolating forward a 20% compound annual growth rate (CAGR) from 1995, a commonly-held number at the time, pegged 2000 revenues at more than $350 billion. Optimism seemed to abound. For example, one wildly optimistic forecast from a professional analytical firm projected an $850 billion industry by 2005.[37] Always the pragmatist, Moore himself joked about blind extrapolation by showing that if the industry continued its incredible growth trend unabated, the semiconductor industry would surpass world GDP in about 50 years as shown in Figure C-7:

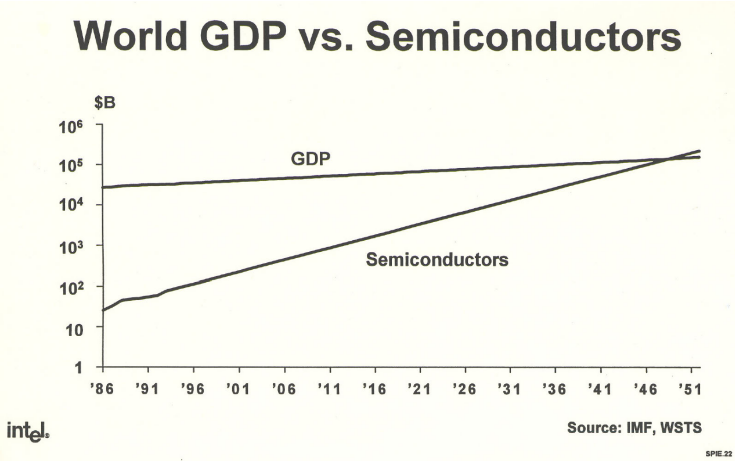

Figure C-7. World GDP vs. Semiconductor Industry

Source: Gordon E. Moore, "Lithography and the Future of Moore's Law," paper given at SPIE, February 20, 1995, Figure 17, 11.

But the rosy 2000 forecasts, much less the ones further into the future, would not materialize as the industry faced almost immediate troubles on many fronts. Many PC users initially balked at purchasing Windows 95 because of the additional memory and processing requirements. Chip inventories rose and unit prices fell markedly in 1996. In 1997 the Asian currency crisis had begun and would plague both supply and demand factors for years to come. Demand in American markets would pick back up by decade's end fueled by two factors: the rapid growth in the Internet and heavy corporate spending in preparation for Y2K. The large spike in 2000 revenues, to a level exceeding $200 billion, reflects this. Not only did the Y2K problem not surface as widely expected, the year 2000 also saw the implosion of the Internet dot-com bubble.

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[35] Dan Hutcheson, as reported in "Semiconductors: When the chips are down," *The Economist*, March 23, 1996, 21.

[36] See for example EIAJ, "The Globalization of the Semiconductor Industry," http://www.eiaj.org/ 1996, which projected $270 billion total sales, and Dataquest, "Dataquest Reports Worldwide Semiconductor Market to Return to Double Digit Growth in 1997," April 17, 1997, which projected revenue totaling $318.2 billion by 2001.

[37] Robertson Stephens & Co. forecast as reported by William Davidow, "The Deconstruction of the Semiconductor Industry," *Forbes ASAP*, February 26, 1996, 70.

Sales of networking equipment, disk drives, and computers for Web hosting farms plunged, driving down demand for chips for these systems.[38] The telecom industry, also a large user of chips, was already mired in its own recession. A U.S. recession, coupled with the tragedy of the September 11 terrorist attacks, saw sales drop by a startling $64B or more than 30% in 2001. To put this value in perspective, the whole industry had not achieved $64B in revenues until 1993, just eight years earlier. As discussed in Chapter 3 the industry in 2004 is recovering from the worst sustained downturn in its history. This cycle is preceded by a similar but milder one that began in 1995 for reasons just discussed. Figure C-8 compares the 1985-1995 period with a CAGR of almost 19% to 1995-2005 with a CAGR of 1.3% through 2003 or 3.6% including the forecast through 2005. Two starkly different views of performance over the past two decades are evident.

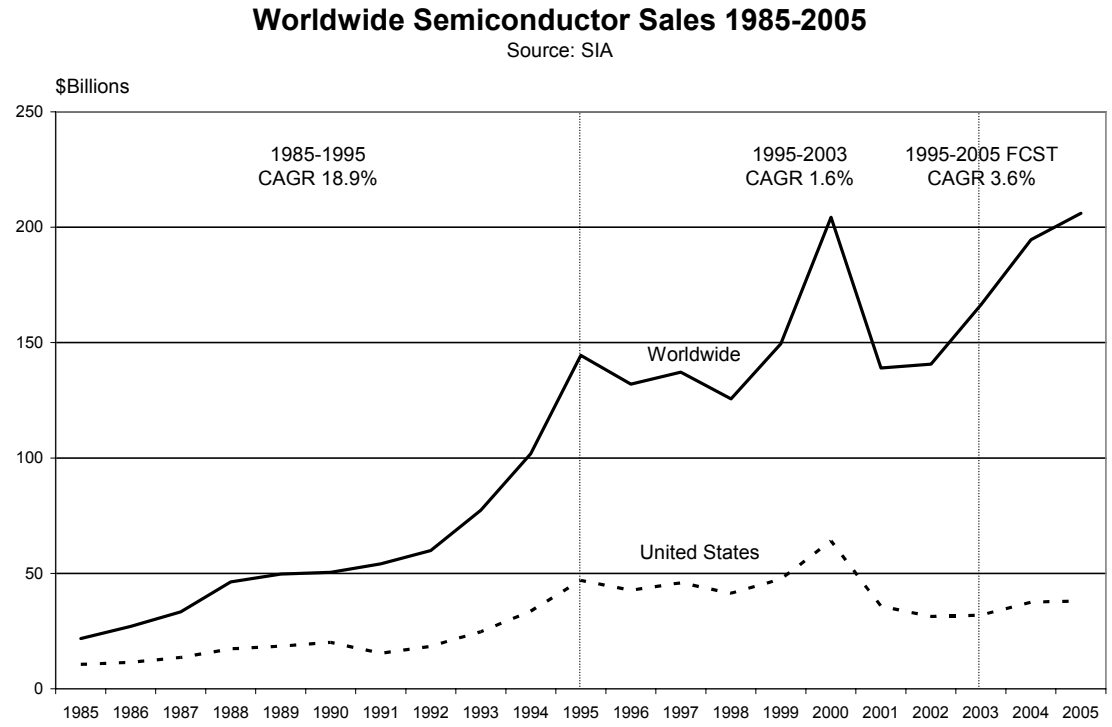

Figure C-8. Comparison of Sales Growth Trends: 1985-1995 vs. 1995-2005

The preceding analysis of global industry revenues only tells part of the story. An important contributing factor was declining unit prices that some have argued were precipitated by an acceleration of Moore's Law. For instance, Hutcheson, a leading industry analyst, argues this very point (see Figures C-9a and -9b).[39] Of course there were numerous other factors affecting the industry's performance. The data is presented here simply to illustrate how much differently the past eight years' performance has been in comparison to where the earlier trends had pointed.

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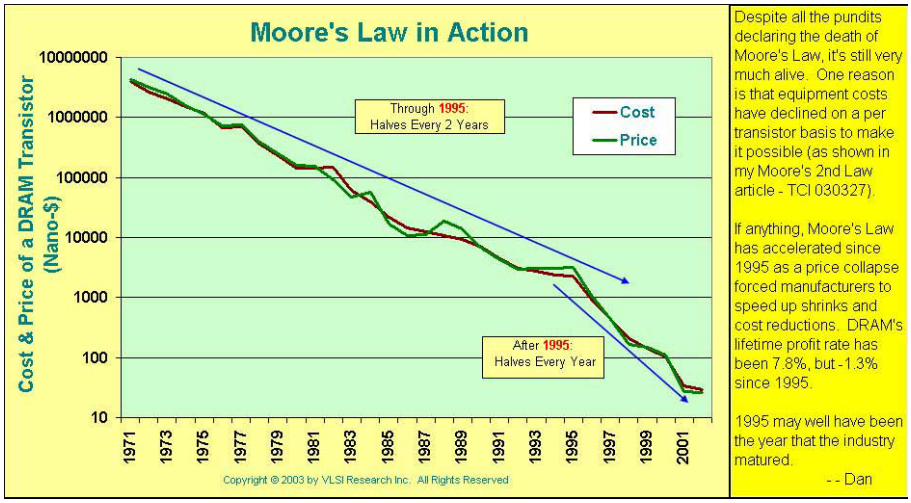
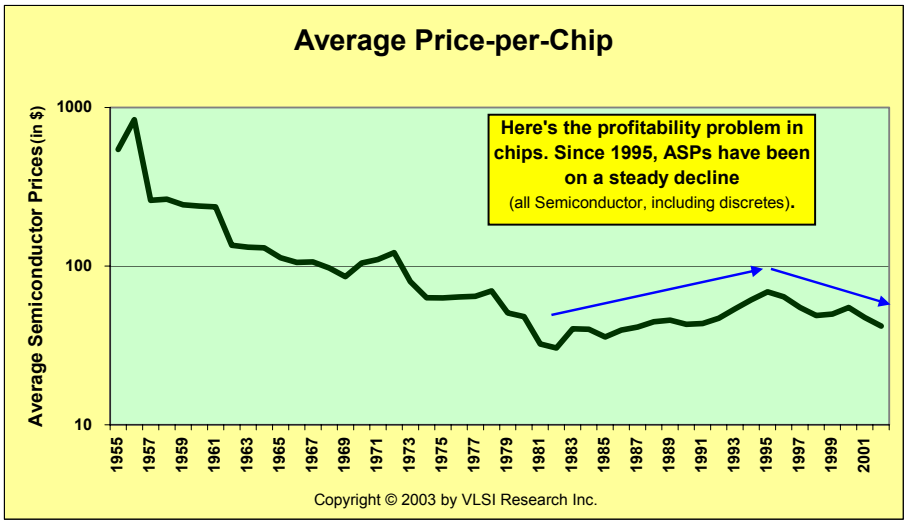
[38] Linda Geppert, "A Sea Change in Semiconductors," *IEEE Spectrum*, January 2003, 76.
[39] G. Dan Hutcheson, VLSI Research Inc., "Moore's Law: Its Death Has Been Greatly Over-Exaggerated," ISSM Keynote Address, October 1, 2003, http://www.vlsiresearch.com/



(a)



(b)

Figure C-9. Moore's Law and Average Price-per-Chip

Source: G. Dan Hutcheson, VLSI Research Inc., "Moore's Law: Its Death Has Been Greatly Over-Exaggerated," ISSM Keynote Address, October 1, 2003, slides 5 and 11, http://www.vlsiresearch.com/

In summary, interest and coverage of Moore's Law followed the industry's success through the mid 1990s. The S-curve logistic function is very noticeable in Figure C-6. This author's article was part of that interest. From 1999 on the coverage of Moore's Law has started to flatten out. The nature of the coverage has also been characteristically different. The dampened mood illustrated in practically flat sales performance the past eight years is also reflected in the coverage of Moore's Law. A content analysis would be useful to help pull out major themes in the literature but it is not possible here. Instead, one recent essay from a noted industry journalist that has received much attention is featured. Michael Malone, who has been a strong Moore's Law

advocate, opined in a recent article simply called, "Forget Moore's Law."[40] Malone asserts that Moore's Law "has become dangerous" in this lengthy caption:

> Forget Moore's law, but not because it's merely a commitment by the semiconductor industry to drive silicon gate technology forward 67 percent a year.
>
> Forget Moore's law, but not because it isn't true. On the contrary, Moore's law may be the truest "truth" about human events over the last half-century. In fact, while our understanding of the cosmos, particle physics, and brain chemistry gets revised almost by the month, Moore's law—so fragile, so on the razor's edge of knowledge, so at the mercy of human weakness—clicks on with the precision of an atomic clock. Indeed, there are days when Moore's law seems the only thing we can still believe in.
>
> Forget Moore's law because it is unhealthy. Because it has become our obsession. Because high tech has become fixated on it at the expense of everything else—especially business strategy. It is precisely this fixation, at the cost of other considerations like profit, product, and market, that led to the dot-com bubble and bust.
>
> Forget Moore's law because there are more important things to worry about—like restoring the lost vitality of the electronics industry. The only people who ought to be obsessing about Moore's law are the folks working in the semiconductor industry, and Gordon Moore himself has suggested that even in the chip business his law hasn't always been a helpful fixation. Lately, some disturbing new trends support his case.
>
> But most of all, forget Moore's law because it has become dangerous. It is a runaway train, roaring down a path to disaster, picking up speed at every turn, and we are now going faster than human beings can endure. If we don't figure out how to get off this train soon, we may destroy an industry.[41]

Malone's dark sentiment stands in stark contrast to views expressed in his popular 1995 book, *The Microprocessor: A Biography*, celebrating the history of the microprocessor and Moore's Law as one of its key drivers. These are a few pertinent excerpts:

> Moore's Law, as it came to be called, has proven to be the most influential and accurate measure of the development of the electronics industry…
>
> As the semiconductor industry quickly recognized, the implications of Moore's Law were awesome…
>
> Moore's Law also told you that the process was not only open-ended but continuous; that you needed to design your devices, especially microprocessors, right now so they would have *upward compatibility* to descendants two decades from now that might have a thousand times their performance…
>
> But perhaps most importantly, Moore's Law suggested that each generation of semiconductor devices was a bundle of variables—notably performance, size, and price—each defining a unique competitive arena… Moore's Law suggested that any of these paths could be viable; that there was no perfect "product point". Rather, the one rule was that whatever path you picked, you had better keep moving . . . fast.[42]

As editor of *Forbes ASAP*, Malone also prepared a comprehensive special issue in early 1996 upon the 25th anniversary of the microprocessor. His feature article then also carried a

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[40] Michael S. Malone, "Forget Moore's Law," *Red Herring*, February 10, 2003.
[41] Ibid.
[42] Michael S. Malone, *The Microprocessor: A Biography*, Santa Clara: Springer-Verlag, 1995, 166-7. Interestingly, note how Malone used the term Law in upper case vis-à-vis his usage more recently in lower case.

simple and upbeat title, "Chips Triumphant." This special issue represented at the time the single, most comprehensive coverage of the semiconductor industry by a major business magazine. Industry giants including Andy Grove (Intel), James Morgan (Applied Materials), Jerry Sanders (AMD), Wilf Corrigan (LSI Logic), Carver Mead (Caltech), and others were featured. Moore's Law was also featured heavily including results of one of the few surveys on the phenomenon ever conducted. The two questions asked of eleven industry officials were:

1. How many more years will Moore's Law play out?
2. What will stop it—design, limits, manufacturing limits or fab costs?

Answers to the first question were summarized in this author's original article. That's where one respondent, Dan Lynch, answered "We'll all be dead when Moore's Law is played out." Lynch's reply to the second question on what will stop Moore's Law: "Moore's Law is about human ingenuity progress, not physics." Interestingly, and to underscore the overall point about the optimism that was so pervasive at the time, was an industry sales forecasting question (actually two): "How large will the global chip industry be by 2000? When will it reach $1 trillion?" The answers were as follows:

1. 2000: $500 billion. 2005: $1 trillion.
2. 2000: $400 billion. 2005: $1 trillion.
3. $1 trillion by 2000 if other countries adopt electronic communication at a rapid rate.
4. 2000: $300 billion. We will certainly see $1 trillion by 2010, perhaps by 2007.
5. 2000: $250 billion maximum.
6. I don't know; depends on the business cycles.
7. 2000: $350 billion or higher. 2006: 2006 or 2007: $1 trillion.
8. It grows as Moore's Law. Chips and stuff built on them will become most of the GNP. Yes, even food. [Dan Lynch]
9. No answer.
10. 2000: $350 billion. 2006: $1 trillion.
11. 2000: $300 billion. 2010: $1 trillion.

Compare this sampling of forecasts with the previous discussion, particularly the 2000 projections. Although a small and biased sample (i.e., some were CEOs of chip companies or directors of chip operations in larger firms while others were analysts and journalists following the industry), these forecasts underscore the pervasive optimism of the time. However, achieving $166 billion in 2003 global sales (and up for the second straight year, see Figure C-8) is the sobering reality that none of these respondents could have imagined. Asking these same questions in 2004 would certainly elicit different answers. The questions themselves would most likely change too. Specifically, the question "when will the industry reach $1 trillion?" might be revised to a simpler "will the industry ever reach $1 trillion in your lifetime?"

Malone reflects on both the pros and cons of Moore's Law. His argument is a valid one: the economics of maintaining Moore's Law are daunting, especially in a downturn. Others agree noting that while it's technologically possible to continue following Moore's Law, "the cost of doing so no longer appears to be justified when there are other places to put R&D dollars."[43] This view is also easily extended to equipment and fabrication expenditures (i.e., Moore's Second Law).

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[43] Ed Sperling, "Wake Up and Smell the Silicon," *Electronic News*, Vol. 49, Iss. 15, April 14, 2003, N.

Malone's closing remarks suggest a new type of acceptance including, if and when necessary, to overlook, even ignore Moore's Law:

> We cannot escape the rule of Moore's law, nor should we want to. It has brought us untold blessings, and it will bring us many more in the years to come. But even as we celebrate Mr. Moore's brilliant law, we must also free ourselves of its tyranny. Before it's too late, we somehow must put Moore's law in its place. We must learn to work beyond it, or at least in spite of it.
>
> Somehow, even as we dance to its beat, we must learn to forget it.[44]

Again, Malone's question—and one increasingly asked by others—is can the industry continue to blindly follow (thus pay for) Moore's Law? That due to the considerable changes in the basic microeconomics of the industry along with the broader macroeconomic environment over the past decade or so, new approaches need to be sought to revitalize industry. This is not a new idea to this very-cyclical industry—each downturn causes a reassessment of fundamental assumptions. The difference this time, according to Malone, is that the industry's most basic economic assumption, Moore's Law, is open to (re)examination.

One final factor not yet considered in this discussion is the role and influence of the Roadmap, which has been in effect through this entire period. In 1995/6 the 1994 NTRS was in force and scheduled for a three-year renewal in 1997. The 1997 NTRS would be the last *national* Roadmap and from that point forward the *international* ITRS would be renewed every two years. The 2003 ITRS was just renewed and involved almost 1,000 contributors from all over the globe. The history and role of the Roadmap will be discussed in detail in subsequent chapters.

3. Other Interpretations of Moore's Law

The original article examined a few interpretations and uses of Moore's Law outside of its original objective of regular doubling of transistor densities per chip. Of course processor performance as measured by MIPS (now BIPS) is a close corollary.[45] Not much farther a field is Metcalfe's Law for the Internet and Wirth's Law for software (i.e., software gets slower faster than hardware gets faster; discussed in the article although not by this label). Other close cousins are the even-faster scaling trends found in optical and hard disk drive (HDD) technologies.[46] Equipped with a wider-angle lens it could be (and has been) argued that Moore's Law behavior is exhibited not only at the system and network level (i.e., Metcalfe's Law), but also in other sectors that do not appear related at first glance.

For example, Nathan Myhrvold, former CTO at Microsoft and cited in this original article, is now a managing director of Intellectual Ventures, and recently argued that Moore's Law can hold for many technologies besides semiconductors including genomics and biotechnology.[47] Indeed, Moore's Law has been picked up by industries as diverse as pulp and paper, banking, and education. It is commonly used within the financial community as a bellwether for high-tech markets. Because of its broad application, it is not possible here to present a complete picture of the various uses of Moore's Law outside of semiconductors. Instead, three views relevant to this

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[44] Malone, 2003, op. cit.
[45] Interestingly, Moore has stated that it was David House, former Intel executive, who said sometime in the 1980s that microprocessor performance doubles every 18 months. This assertion may have played a role in the commonly-held view of Moore's Law as an 18-month rate, even though its basis was not transistor density doubling.
[46] See for example R.J.T. Morris and B.J. Truskowski, "The Evolution of Storage Systems," *IBM Systems Journal*, Vol. 42, No. 2, 2003, 205-217.
[47] Michael F. Wolff, "Chase Moore's Law, Inventors Urged," *Research Technology Management*, Jan/Feb 2004, Vol. 47, No. 1, 6.

research have been selected and will be briefly discussed. The first, by Ray Kurzweil, represents a visionary's view that may not afford direct usage by decision makers, but elicits thoughtful consideration about the generalizability of Moore's Law. Randy Isaac argues that "cost per function" should replace the classic Moore's Law measurement of components per chip. In so doing it would be possible to extend Moore's Law beyond the point when physical barriers ultimately prohibit cramming any more transistors on a chip. Isaac's view is in fact shared by informants of this research. Finally, Chris Mack, who interestingly references Kurzweil's work, "redefines" Moore's Law within a learning curve framework and in doing so offers as the metric transistor shrinks (vs. transistor density) consistent with the industry's Roadmap, the unit of analysis of this study. Mack's reformulation deserves due consideration by industry policy and strategy makers.

Ray Kurzweil unmistakably holds the longest view, contending that "Moore's Law was not the first, but the fifth paradigm to provide exponential growth in computing."[48] In Figure C-10 Kurzweil plots the speed in instructions per second per $1,000 (in constant dollars) of 49 famous calculators and computers spanning the entire twentieth century. He notes that each time one paradigm runs out of steam, another picks up the pace, enabling a smooth flow of increasing capability in information processing. His interpretation clearly extends the conventional definition of Moore's Law to technologies that predate the integrated circuit. Kurzweil further suggests a sixth paradigm to follow (i.e., three-dimensional molecular computing) that will ensure continuity of this exponential trend. He projects improvements in processing capability from this exponential will approach and exceed that of the human brain within the first half of this century.[49]

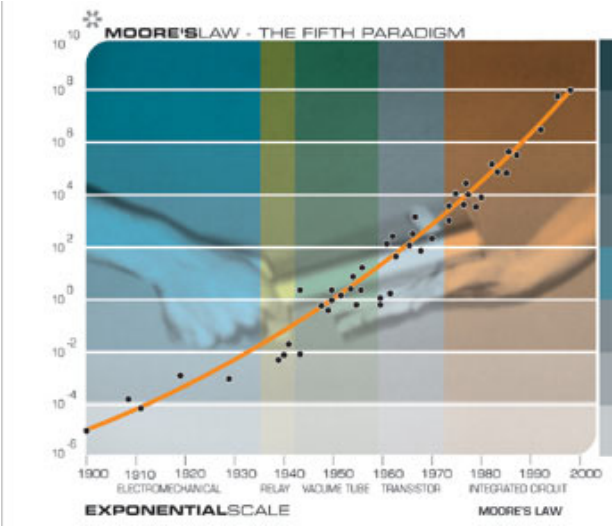

Figure C-10. Kurzweil's Extension of Moore's Law

Source: Raymond Kurzweil, "The Law of Accelerating Returns," March 7, 2001, http://www.kurzweilai.net/articles/art0134.html

[48] Raymond Kurzweil, "The Law of Accelerating Returns," March 7, 2001, http://www.kurzweilai.net/articles/art0134.html

[49] Rob Fixmer, "Moore's Law & Order," *eWeek*, April 15, 2002, 39-40.

Chris Mack, in his own analysis of Moore's Law, also references Kurzweil's interpretation and calls it "a retroactive look at Moore's Law" providing a table that seemingly demonstrates a continuum of reductions in feature sizes over time (Table C-3).[50]

Table C-3. A Retroactive Look at Moore's Law

Year	Feature Size	Technology
1900	1 inch	Telegraph wires
1912	1/4 inch	Electromechanical relays
1924	1/16 inch	de Forest Audion
1936	16 mils	Triode vacuum tubes
1948	4 mils	Miniature vacuum tubes
1960	1 mil (25 μm)	Planar transistor

Source: Chris A. Mack, "The End of the Semiconductor Industry as We Know It," Paper presented at SPIE 2003, February 2003, Table 1, 5. Data taken from Raymond Kurzweil, *The Age of Spiritual Machines*, New York: Penguin Books, 1999.

Though the data seem to fit well, demonstrating some fundamental driver of innovation at work, Mack points out the limitations in attempting to extend the idea too far:

> But let's be honest—the data in Table 1 [Table C-3] is contrived. Backtracking the Moore's Law numbers and finding some convincing technologies that fit each "node" was easy, and almost without meaning. Of course, innovation is fundamental to the human condition, but the pace of innovation is not. One must look a little more carefully to find out how the semiconductor industry in particular has kept such a consistent pace of technology development.[51]

Mack is correct that Moore's Law is fundamentally about the pace of innovation, and more precisely about the pace of semiconductor innovation. At the same time though, Kurzweil's interpretation like others causes us to think in a contexts that are unconventional at first. One of the appeals of Moore's Law—also one of the dangers—is the ease of generalization. As Moore himself has acknowledged often, there is a tendency for any exponential to somehow become associated with Moore's Law. Kurzweil's thesis that growth in computing power has become a continuous, evolutionary process that follows an exponential trend is very plausible. Moore's Law, technically representing only one part (paradigm) of this evolution according to Kurzweil, may have served as the enabler to see it in this fashion.

The next interpretation of Moore's Law to be discussed is that of Randy Isaac, VP, Systems, Technology and Science, IBM Research Division at the T. J. Watson Research Center. Since his career at IBM Research began in the late 1970s Isaac has witnessed, and been part of, a wide array of technological innovations in semiconductors including copper interconnects, silicon-on-insulator (SOI), silicon germanium, carbon nanotubes, and others. During that time he has also become a student of Moore's Law and similar technological trends. Like Kurzweil he holds a broader interpretation, but Isaac's is more germane to the semiconductor industry:

> "I used to think (Moore's Law) was a historical curiosity. As I continued to work on it, I thought it was a self-fulfilling prophecy. Now I view it more as a self-consistent economic

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[50] Chris A. Mack, "The End of the Semiconductor Industry as We Know It," Paper presented at SPIE 2003, February 2003.
[51] Ibid., 4-5.

> cycle." Isaac explains that, basically, there are a lot of factors – expectations, money and many different pieces of technology – that feed and play off one another to perpetuate Moore's Law. "It just hangs together."[52]

Isaac is quick to point out two definitions of Moore's Law: the *classic* definition as originally put forth by Gordon Moore (i.e., based on components per chip), and a newer definition based on *cost per function*. Like Moore, Isaac views economics as a key driver but his interpretation goes well beyond the classic view as briefly described in the caption above. Isaac elaborates on the importance of seeing Moore's Law in this new light:

> As you get more components on a chip, you get more function, more speed, and lower cost per function. And anytime you get more function and speed at lower cost that's productivity. So Moore's Law really talks about components per chip. He never said anything about Megahertz, he never said anything about all this other stuff that people attribute to him. The core is that these are the technical drivers that help reduce cost per function and speed. That is the essence of Moore's Law and it is so powerful. Now the reason that I believe it is an economic driver is that what happens is the actual cost of doing this - of sustaining Moore's Law - the actual cost of adding more components per chip is enormous. So to amortize that increased cost you need to have this extra productivity - you need to get lower *cost per function*. And that lower cost per function needs to stimulate a larger market. And the larger market then amortizes the cost of doing the work and funds the research and development. So it's a complete cycle - you have a cycle here.
>
> Now the concern about Moore's Law is not so much technical about the future, but it's economic. Because when you invest an enormous amount to get another factor of 2 times or even 50% more components in the chip, but if the result of that ended up that the cost didn't decrease - so you did not have a lower cost, then you are not going to expand the market. And then if you don't expand the market, your returns aren't going to come, and you're not going to be able to invest in the next turn of the crank, and it slows down. And so many of us feel that the economic issues are going to be more important than the technical ones in terms of how this ends up. But this is why I feel that it's more than just a self-fulfilling prophecy. This is an economic cycle here that pulls this together. Because you can't afford to invest large amounts in new technologies if that doesn't end up reducing the cost per function.[53]

Given this reformulation, Isaac stresses that by using cost per function as the goal then following traditional scaling or simply adding more components per chip may not be necessary:

> That's where this is an economic necessity. That's why I keep saying here that there are other ways of reducing cost per function. Or, said another way, there are many different ways than adding more components per chip that would be more efficient in terms of design efficiency, what it takes - how many transistors does it take to implement a function. So you can make it more efficient and get more components that way. But ultimately, the real measure is cost per function. That is your real measure - that's what you're getting at in Moore's Law. Nobody's talking about that.

This concern was also raised by Roadmap participants (see Chapter 11). The idea of *functional scaling* (i.e., not just smaller transistors) has been discussed for some time. In fact, the 1999 ITRS introduced the idea of *equivalent scaling* (see Chapter 10) which means not everything needs to scale at same rate. Some things can scale slower or even "de-scale" (i.e., go

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[52] Randall D. Isaac, as quoted in Kevin Maney, "Breakthroughs affirm computer guru's growth theory," *USA Today*, September 25, 1997, http://www.usatoday.com/life/cyber/tech/ctb315.htm

[53] Randy Isaac, personal interview, July 18,2000.

backwards like die sizes shrinking not growing). Isaac expands on the limitations of components per chip:

> Components per chip which is the real Moore's Law - the *classic* Moore's Law - and it's components per chip that has driven all this, right? We may be coming to the point where components per chip is no longer increasing, but that the cost per function, which is the *real* economic driver, continues to reduce because of *other* factors. That is design efficiency in programming, because initially - when Gordon Moore started here you had 60 components per chip, you didn't have a whole lot of things you could do with that. So your only path to improve cost per function was components per chip, and that has been the key driver. But one of my messages is - when I give this talk - is that there's a hierarchy of contributions to this cost per function. So yes, you still have the core drivers and we expect that to continue but let's suppose it didn't - just hypothetically. Now look at all the parameters we still have at our disposal now because if you have a billion transistors on a chip, and more, you now have such incredible amount of potential in terms of how you utilize these that you still have the opportunity to dramatically lower cost per function and still get a lot out of it. So a curious notion that I haven't taken very far yet - but this notion that in a way Moore's Law has set in motion an economic cycle that may indeed continue *without* more components.[54]

The "talk" that Isaac refers to is a presentation entitled "Beyond Gigahertz and Gigabit Chips," that he first gave in Japan and has since delivered to various audiences. Figure C-11 illustrates the many factors that Isaac sees as contributing to system performance. Note the basis of this chart is Moore's 1975 chart that shows the three factors that had contributed to progress since 1965 (see Figure C-1a). The lowest two of Isaac's factors (i.e., process technology and circuit design) capture Moore's three original factors (i.e., reduced circuit dimensions, increased die size, and circuit cleverness). These are fundamental to continuance of the classic Moore's Law. The other nine factors are what Isaac refers to as additional contributors to decreasing cost per function, his new definition of Moore's Law. Thus it is possible with all these variables in play to continue to achieve progress even if the bottom two factors fail to contribute to increases in components per chip.

[54] Ibid., emphasis per the author.

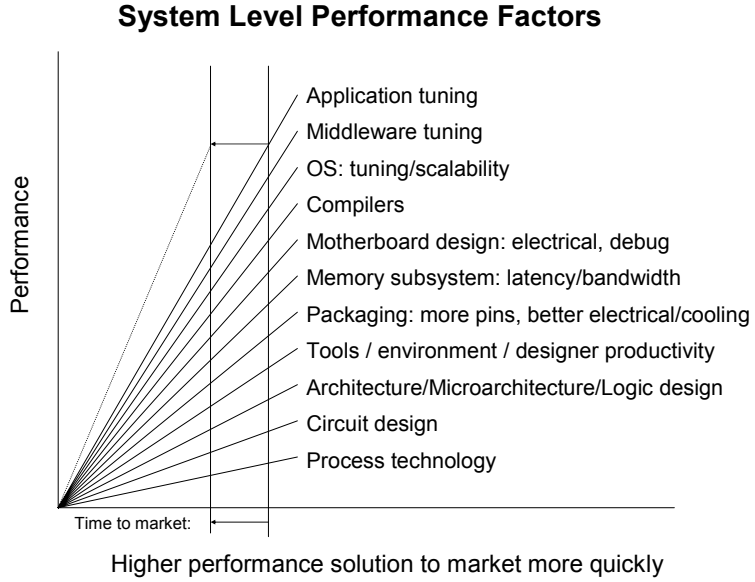

Figure C-11. System Level Performance Factors

Source: Randall D. Isaac, "Beyond Gigahertz and Gigabit Chips," PowerPoint presentation, undated, slide 42 (of 44).

Isaac views lithography as the key driver to increases in components per chip, attributing half of past progress to this one factor. He then speculates the possibility that if an important enabler like lithography were to stall, or even stop altogether, progress in reduced cost per function could continue:

> So suddenly if something were to magically freeze at once, then how would you get your reduction? Well you still have a cost reduction because suddenly all your fabs would be depreciated, right? By the time you write it off you won't have to replace them. Hey, your cost has gone down dramatically, without taking the lithography step - very interesting. So, there's still a lot of room for the whole economic cycle to just keep going. That's just a trivial example - you know you get more yield, you get more design productivity, you get other factors, you focus because right now a given technology doesn't exist long enough to wring the cost out of it - because you keep going to the next. It's more cost effective to go to the next technology.
>
> Now if Moore's Law were to magically stop - which it won't by the way, I do not expect it to. But this hypothetical - what happens if? There's still enormous productivity enhancement available in manufacturing: you'll continue to drive lower cost per function, plus on top of that you have all these parameters still churning. So I see this whole economic cycle of productivity continuing for a long, long time, no matter what happens to transistors or lithography. So it's a really fascinating economic cycle that's kicked off.[55]

As previously stated, Isaac is not alone in his call to reformulate Moore's Law around functions vis-à-vis transistor counts. Of course one major challenge is defining, and finding consensus in, the term "function." That's one reason *classic* Moore's Law has been so enduring—the simple measure of transistor count is straightforward, not open to interpretation. Nonetheless,

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[55] Ibid.

Isaac puts forth a proposal that is deserving of consideration as the semiconductor industry approaches the maturity stage of its life cycle.

A final consideration raised by Isaac and others is the critical role of market forces. Recall that Moore had raised the "product definition" problem of the late 1960s when increased chip complexity exceeded any apparent demand. The emergence of the electronic calculator and other consumer applications would help bring this situation into balance. When this problem occasionally resurfaced during the industry's history, new applications emerged (e.g., the PC in the 1980s and the Internet in the 1990s) to absorb the vast capabilities made possible by Moore's Law. But at the turn of the 21st century there appears no similar "killer application" to absorb the most complex chips in great volumes, the basis for Moore's Law. Some have referred this contemporary 'product definition' problem as "outrunning the supply lines." Instead, markets have become more specialized with products that do not necessarily require the complete complexity. While it remains possible to produce the level of complexity called for by classic Moore's Law, increasingly there are not sufficient economic incentives (i.e., demand and profits) to do so. In other words, if you build it, they might *not* come. Box C-3 explains how changing market forces have affected Moore's Law.

Box C-3. Moore's Law Meets the Market

Moore's Law, Microprocessors and Semiconductor Manufacturing Equipment per Mathew C. Verlinder, Steven M. King, Clayton M. Christensen[56]

For decades, the semiconductor industry has successfully and single-mindedly pursued a set of traditional performance trajectories. The pursuit of Moore's Law … has delivered enormous value to the market and the companies that have enabled this progress.

But is shrinking linewidth likely to be as competitively crucial in the future as it was in the past? Our observations and research suggests not—that there are other performance parameters that will become increasingly more important. To explain why we believe the future will look different from the past, we must look at the semiconductor industry through the lenses of models—disruptive technologies and the drivers of modularity.

[T]he pace of technological progress almost always exceeds the rate at which customers can utilize those improvements. As a result, the performance delivered by products can, over time, come to exceed the performance that customers in any given tier of the market can utilize. When this "performance overshoot" occurs on a historically valued measure used by firms to garner premium prices, customers cease to value further improvements on that measure. These customers will gladly accept increased performance but will be increasingly unwilling to pay a premium for it. Market forces then compel companies to find new ways to attract overserved customers, whose attention shifts to value provided along new trajectories of innovation.

In the microprocessor and semiconductor equipment industries, computing performance and price/performance, fueled by the industry's collective attention to Moore's Law, have been the measures of improvement valued in all tiers of the market. In the future, however, and beginning in the least demanding tiers (such as hand-held devices), speed to market, and the ability to conveniently custom tailor the features and functions of microprocessors to the needs of specific classes of customers, will be the type of innovations that matter. Continued adherence to the Moore's Law trajectory might be necessary to remain competitive, but will unlikely be sufficient to ensure success.

The speed of the [Intel] Itanium, Pentium IV and [AMD] Athlon class of microprocessors, while still good enough for bleeding-edge customers, is far greater than what most mainstream

[56] Excerpted from Mathew C. Verlinder, Steven M. King, Clayton M. Christensen, "Seeing Beyond Moore's Law," *Semiconductor International*, July 2002, 50-57.

users—those that employ computers for word processing, scheduling, e-mail and Internet access—can utilize. In the late 1990s Intel addressed the first wave of disruption coming from the low end with its Celeron brand microprocessor. This "good-enough" product's architecture is far more modular than that of the Pentium products… In simpler market tiers—particularly for embedded devices—companies like Tensilica[57] already are custom assembling highly modular microprocessors from configurable, reusable cores. In the absence of these theories of disruption and disintegration, such efforts might be dismissed as insignificant blips on the radar of industry leaders. In the context of there theories, however, these fledgling developments are harbingers of massive change within the industry.

The relentless pursuit of Moore's Law historically has not allowed the semiconductor manufacturing process to mature and stabilize, particularly semiconductor manufacturing equipment. Equipment manufacturers have been driven by their best customers to continuously push the technological frontier to achieve smaller geometries. In this race to satisfy the demands of their best customers, they have designed and built tools to "wring out" the highest performance possible. In this era, high performance means smaller geometries, not tools that are highly reliable.

As is reasonable given their history, microprocessor design, fabrication and equipment manufacturing firms have been laser-locked on maintaining the compute performance trajectory established by Moore's Law. Attention currently is paid to shrinking linewidths, building smaller transistors and fabricating larger wafers. Sleep is lost over whether or not this is possible, and how much it will cost.

Will devices hit a physical limit? Probably. But this may be the right answer to the wrong question. The important question is, as technological progress surpasses what we can utilize, how do the dynamics of competition begin to change?

Moore's Law and DRAMs per Randall D. Isaac[58]

I've been fascinated by what is actually happening in the DRAM industry. I believe this sheds a lot of light on the essence of Moore's Law… To double the number of transistors every 18 months, the lithography resolution must decrease by 30% every 3 years, the chip size must increase by 40% every 3 years and innovation must lead to a 40% improvement in density every 3 years. As you point out, the DRAM industry has exemplified this trend the best with a 4x/3 year increase in bits/chip.

Now take a look at the data. The DRAM bits/chip trend deviated from this trend in about 1997 when it slowed to a 2x/3year trend. Moore's law would have predicted that 4Gb chips would be qualified by the end of 2003 but in fact the first 1Gb chip was qualified in March 2004. WHY? Look at the technology: cell sizes kept getting smaller at the same trend for another 3-4 years. Then it began to slow also. WHY? What's going on?

My view: building on my comments that you cited, it's all economics. That is, the market did not need more bits/chip and so the industry didn't build them, even though they could have. WHY? At long last, PC's, which are the dominant DRAM market with about 70% share, don't need dramatic increases in memory capacity. WHY? It's really a 'good enough' phenomenon. Not even Microsoft can build operating systems requiring memory that doubles every 18 months. The high-volume average PC doesn't need 1GB of memory and an optimum DRAM chip for 1GB of

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[57] Author's note: Tensilica, founded in 1997, is one of dozens of new semiconductor IP companies that provides configurable microprocessor cores (and a suite of software development tools) used in complex system-on-a-chip (SoC) designs for wireless, consumer, and network infrastructure products.

[58] Excerpted from Randall D. Isaac, e-mail to the author, March 18, 2004.

memory is 512Mb.

So what happened? The focus was on economics and cost reduction rather than on higher bits/chip. In fact, the trend for lithography INCREASED in 1997 to a 30% every TWO year pace. To balance the equation, chip size stopped growing. That is also because of a practical economic consideration: beyond a certain size of chip, a DRAM becomes much more expensive to package. Besides, chip size is the single biggest factor in the cost of a chip. Also, in the last few years, the DRAM cell innovation factor has slowed considerably and has asymptotically approached what is considered the limit. What does this mean? Lithography has become nearly 100% of the factor behind "Moore's Law" rather than 50%. Since lithography accelerated, the bits/chip only deviated from Moore's Law to some extent.

Another way to say it: lithography advances were translated into cheaper chips rather than more bits on a chip. It's all about economics!

In a nutshell, we have clear evidence now that in the DRAM industry, Moore's Law no longer holds. Understanding the elements behind Moore's Law helps us to understand the technical factors involved and how it really is economics that drives the industry, not a mythical law.

The final interpretation of Moore's Law is from Chris Mack, VP at KLA-Tencor's FINLE Division. Mack draws from his more than twenty years of experience in lithography in a detailed analysis entitled "Redefining Moore's Law."[59] Mack expresses concern that Moore's Law has grown beyond its original intentions and is in danger of losing its meaning and possibly its usefulness.[60] He argues for both a redefinition and reformulation of Moore's Law, The redefinition is in the metric itself. He points out that this has actually changed subtly but qualitatively since the first definition. This concern was previously discussed and presents a problem when trying to compare data before and after the mid to late 1970s. The more significant change that Mack suggests is to replace the traditional transistor density unit of measure with minimum lithographic feature size, the key metric used by the industry's Roadmap. He states:

> "Moore's Law is not about scaling up, but scaling down. Moore's Law is no longer about [the number of] transistors on a die. Moore's law is about shrinking transistors."[61]

Indeed, the Roadmap, concerned primarily with process technologies, has defined "technology node" as the minimum feature size printed (measured as "half-pitch") that enables the fabrication of a certain device type. Historically there has been an inverse relationship between minimum feature size and transistor density: the smaller the minimum feature size printed, the greater the density per chip. For instance, a 1G DRAM chip requires a minimum printed feature size of 100nm while a 4G chip will need 65nm nm dimensions. Continuance of Moore's Law has been made possible through printing ever smaller transistors, thus cramming more onto each chip. Chapter 11 Box 11-1 provides important background on why this relationship may no longer apply.

Mack calls attention to the fact that the trends in DRAM and microprocessor chip deliveries in the last five years or so show a remarkable change in that the number of transistors per chip has not kept pace with the historical pace of the past few decades. He asks, "Why aren't 4Gb DRAM chips in mass production today, as the historical Moore's Law trend would suggest?" and answers, "Quite simply, there is no mass market demand for such a chip."[62] Recall Isaac's

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[59] Chris A. Mack, "Redefining Moore's Law," Paper presented at SPIE 2003, February 2003, 11pp.
[60] Chris A. Mack, "Using Learning Curve Theory to Redefine Moore's Law," *Solid State Technology*, July 2003, 51. Note that this article is derived from the article cited in the previous footnote.
[61] Chris A. Mack, as quoted in Mark LaPedus, "Moore's Law recast as defining transistor shrinks, not their scaling," *Electronic Engineering Times*, March 3, 2003, 24.
[62] Mack, "Redefining Moore's Law," op. cit.

description of the traditional industry cycle where increased functions at lower cost expand markets, which generate profits for investment in future products, etc. The present economic downturn is probably exacerbating the problem of weak demand, but Mack raises a very valid question. At the same time, minimum device feature sizes continue to get smaller in accordance with the Roadmap. This is where the claims of technology *acceleration* or speeding up of Moore's Law have occurred. While a slowdown in the transistor density doubling rate has occurred there is no let-up in shrinking transistors.

Economic downturn aside, part of the reason for the slowdown in the transistor density rate could be characterized as the "product definition" problem that has periodically plagued the industry since its first customer, the U.S. Government, cut back on its expensive appetite of early ICs. Recall that in the mid to late 1960s as the integrated circuit was advancing faster than there were obvious uses Moore himself wondered what application would absorb the increased capability in sufficient volumes to be profitable. Solid state memories and the calculator served as initial important drivers. Then a decade later a similar quandary arose until the microprocessor found volume traction in the PC. The internet helped to provide stimulus throughout the 1990s. The industry has been seeking "the next big thing" for several years now. In lieu of a single driver, specialty markets have emerged such as wireless and handheld applications, most of which do not require gigabits and gigahertz-capable chips. Surprisingly, shrinking transistor features have enabled suppliers of these chips to be very competitive at the price points required in their specialty markets (this is described in Box C-3 and 11-1). It's an odd kind of Moore's Law success story more along the lines of Randy Isaac's reduced cost per function, but in this case without more—but maybe different—functions.

Mack's proposal to shift the industry's measure of progress from transistor density to feature size is consistent with the Roadmap and, as such, the industry's direction. Having said this means that this has already begun. One problem is that it's harder for a layperson to understand terminology like minimum device feature size, minimum half pitch or gate length. Transistor count is so much easier and, as discussed earlier about Isaac's cost per function, there is little room for interpretation. Already the term "technology node" is increasingly being misused as a marketing ploy to help in the promotion of new "leading-edge" products. Further, the larger audience will have to reorient their thinking about progress (i.e., downsloping curves don't carry the same appeal of upsloping curves as a measure of progress). Mack has begun to address this with his call to scale down, not up. Nonetheless, Mack proposes to legitimize what the semiconductor innovation community has already adopted as the all-important *technology node*. Chapter 10 will examine the Roadmap (ITRS) in detail and reveal that indeed Moore's Law has been reoriented from a device scaling metric based on transistor density to one based on minimum feature size. Thus within the industry there is already broad acceptance. The bigger challenge will be in getting the wider community to follow along.

Moore's Law as a Learning Curve

The second and more significant change Mack proposes is to reformulate Moore's Law from a time-based measure of progress to a learning curve framework where cumulative volume of output serves as the y-axis. This is not a new idea to the semiconductor industry. It was, in fact, studies of Texas Instruments' early production of silicon transistors by the Boston Consulting Group (BCG) in the late 1960s that served to put forth a general theory of the *experience curve*, a similar but broader concept (see Figure C-12). Note the steady unit price decline with each year's (points on the graph) additional level of output. Also note that lower unit price may not be an accurate indicator of progress, especially if the data from the later years included integrated circuits that contained more components per unit. If so, the real *unit* (i.e., transistor) price would have fallen much more dramatically. This is the effect that Gordon Moore observed early on.

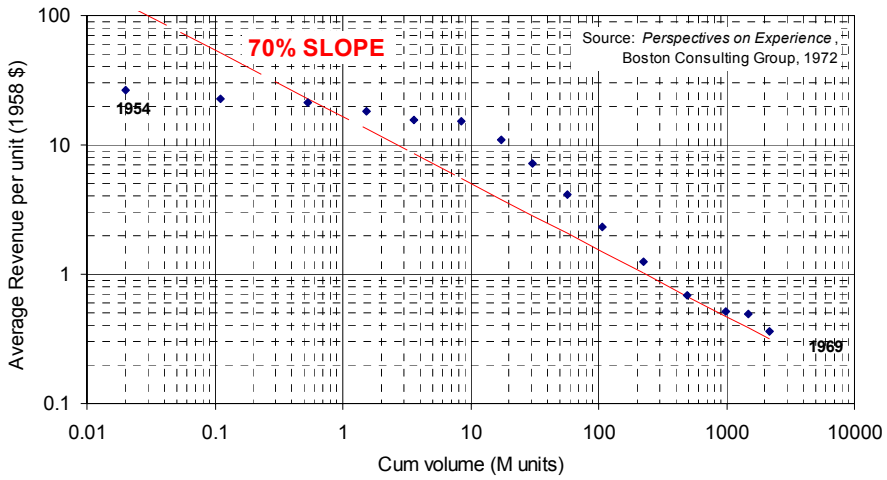
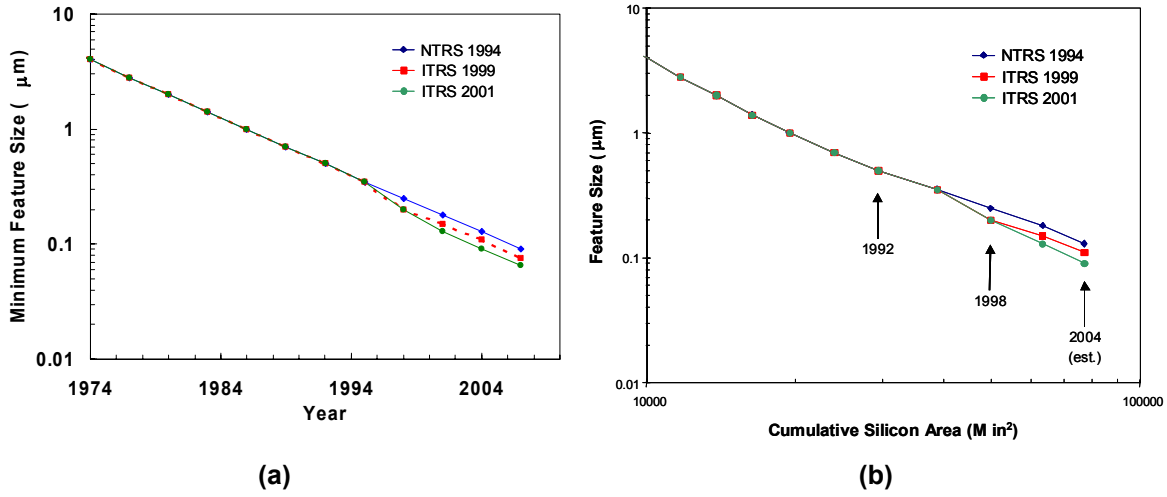


Figure C-12. TI Silicon Transistor Experience Curve: 1954-1968

Source: Boston Consulting Group, *Perspectives on Experience*, Boston: Boston Consulting Group, 1972.

Mack observed that by viewing the progress in reduced feature size in the traditional method (i.e., the Roadmap and his proposed metric for Moore's Law) as shown in Figure C-14a, technology acceleration since the mid 1990s that is widely recognized becomes apparent. However, if the bottom axis is changed from a yearly measure to a learning measure—in this case cumulative silicon area produced—a different picture emerges (Figure C-13b). In this view technology advance was actually decelerated slightly through the early to mid 1990s and has since caught back up to its traditional rate. Mack summarizes:

> Note that changed predictions of Moore's Law found in the 1994 through 2001 roadmaps, while often called an "acceleration" of Moore's Law, can be seen in the learning curve formulation as a correction back to the historical trend line from the slowdown of the early 1990s.[63]



[63] Ibid., 6.

Moore's Law shown (a) as the traditional time-based progression, and (b) as a learning curve, plotting minimum feature size versus cumulative area of silicon produced by the industry on a log-log scale.

Figure C-13. Moore's Law as Minimum Feature Size and as Learning Curve

Source: Chris A. Mack, "Redefining Moore's Law," Paper presented at SPIE 2003, February 2003, Figure 3, 7.

Mack states that cumulative silicon area is a sound independent variable. First, advances in functionality brought forth by Moore's Law have offset rapid and significant increases in production costs if measured on this basis. Also, despite the changes in wafer and die sizes over time, the cost/cm^2 has remained roughly the same over time. Mack goes on to espouse the advantage of a learning curve formulation as more predictive of future trends. More importantly he states that continuous innovation is predicated on increased silicon volume:

In order to continue Moore's Law, an ever increasing output of silicon is required.[64]

But Dan Hutcheson does not agree that Moore's Law is a learning curve.[65] The reasons are not clear but it may be that Moore's Law is fundamentally a time-based innovation pattern. This is what engenders all the debate over the actual *rate* of progress. To embed this idea in a cumulative output measure may miss essential determinants of Moore's Law. The learning curve effect basically is a relationship between learning and efficiency. In short, the more one (or an industry) does, the better they are at it (i.e., practice makes perfect). In contrast, decreasing line widths are not really an efficiency measure. Indeed they are essential milestones, but this year's accumulated learning (production) on the current technology node does not necessarily translate into efficient implementation of the next node. There is certainly some relationship but each of these nodes is a distinct milestone often requiring entirely new fabrication facilities and equipment. Technology nodes would better be described as an effectiveness, rather than efficiency, measure. Finally, the contribution from R&D in new lithographic methods, novel device structures, or new materials—all important to keeping Moore's Law going—is not captured in a learning curve.

There are probably many applications where learning curve theory applies in the semiconductor industry, but probably not in the leading-edge applications where feature size is so critical. For example, it would apply in the area of microcontrollers or the vast quantity of legacy products that have long product life cycles and stable production methods. As an example, the TI study by BCG mentioned earlier measured the silicon transistor as the unit of analysis.

In summary, Mack proposes to change both axes of Moore's Law which is quite ambitious. The first suggestion to replace minimum device feature size for transistor density (i.e., the y-axis) may be easier than reformulating the x-axis from a time-based to cumulative output measure. However, Mack has officially begun an important debate about the future of Moore's Law by offering a thoughtful proposal worthy of thoughtful consideration.

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[64] Ibid., 8.
[65] Chris Mack, telephone interview, October 15, 2003.

Appendix D: Chapter Appendices

Appendix 2-A. Other Deficiencies and Limitations of Roadmaps

The authors' findings of roadmap deficiencies and limitations extend beyond quality and effectiveness factors. The following paragraphs briefly outline a partial list of these issues and concerns gleaned mostly from evaluative literature on roadmapping as well as personal experiences, often under the heading "lessons learned."

Limits on Inclusion One major weakness of most S&T roadmaps is that criteria for inclusion or exclusion of S&T programs (cutoff criteria) are rarely specified. How similar do S&T programs have to be to the central theme of the roadmap to be included? How strong do the linkages between candidate S&T programs and roadmap resident S&T programs / capability targets have to be in order to be included?

Overconstraining the relationships required for candidate S&T programs to be included in the roadmap could limit consideration of complementary S&T areas, and could exclude innovative ideas possibly extrapolatable from disparate technical areas.

Linearity A related issue and perhaps the most cited concern with roadmapping more generally is the tendency toward linear thinking. That is, the structured (and linear) design of some roadmaps limits the field of alternative paths, often based simply upon extrapolating past performance of a single scenario into the future. Kappel's (1998) technology roadmapping research found evidence when "too much exploitation of the current technological paradigm and not enough exploration of alternatives that may come to dominate." Reflecting similar concerns, Owen Williams, former chairman of SEMATECH's Roadmap Coordinating Group, emphasizes,

> "[O]ften times, it's perceived that these [roadmaps] are the only way to do it, so funding agencies won't fund any out-of-the-box thinking. . . The [SIA] Roadmap is not intended to stymie creativity or to pick winners or losers." (Nesdore, 1997)

Studies in the economic history literature illuminate the role of path dependency and lock-in of technology choices including the QWERTY keyboard design, internal combustion engine, VHS videocassette recorder, and others. Whether there is grounded theory behind these assertions or not, decision making among alternative options (paths) naturally implies trade-offs as the chosen option derives benefits sometimes at the direct expense of the one not chosen. In an extreme case, a roadmap could become a myopic 'one-way street' for research and other investment decisions.

Thus, the oft-cited SIA Roadmap is somewhat of a double-edged sword. Gordon Moore himself, champion of early semiconductor roadmaps, has said (Korcynski, 1997), "If we can stay on the SIA Roadmap, we can essentially stay on the [Moore's Law] curve. It really becomes a question of putting the track ahead of the train to stay on plan." Hence it is not that surprising that innovations in semiconductor technology continue at the regular pace of Moore's Law. The basic S&T ingredients (e.g., silicon, photolithography, manufacturing processes, even R&D) seem to become even more self-reinforcing factors. If anything, an innovation path dependent roadmap assures more regularity, possibly at the expense of faster innovation cycles.

One-Time, Static Exercise The authors' experience is that most roadmaps do not have a sufficiently flexible structure to incorporate dynamic changes. Typically, linkage relationships are not functional, and changes inserted at any node in the roadmap network do not automatically impact the other network nodes through the linked functional relationships. This absence of functional relationships and capabilities among the nodes is a key deficiency of present roadmaps, and is a major barrier to wider acceptance and utilization of these tools.

Further, as has been discussed, there is an important distinction between a roadmap and roadmapping. Some incorrectly confuse the two and thus see a roadmap as simply a 'book' and fail to realize the full potential available from a dynamic *process* of roadmapping.

Isolated Decision Aids To be most effective, roadmapping and other management decision aids need to be fully integrated into the strategic planning and business operations of the organization (Peet, 1998). Employment of roadmaps in a band-aid or afterthought mode will result in a fragmented product with limited potential for organizational implementation. The combination of roadmapping with strategic planning, information retrieval, data mining, S&T evaluation, and organizational performance metrics, has to be addressed well in advance of the implementation of a roadmapping process.

Kappel (1998) and Radnor (1998b) observed an interrelated problem they refer to as "de-coupling," occurring when an organization attempts to formalize roadmapping, but in fact its apparent adoption is only a paper exercise, not truly linked (coupled) to any broader strategy.

Questions for Future Research The list of issues and concerns concerning roadmaps and roadmapping includes the following additional questions deserving further research:

1. Despite the rhetoric about the long-term, strategic emphasis of roadmapping, the research to date shows a short-term bias in corporate roadmapping practice. Why does this occur, and is this also true in other roadmapping applications?
2. How can roadmapping practitioners avoid the multiple interpretations and misinterpretation inherent in this new practice?
3. To date, roadmapping has been the province of large organizations and programs. Why is there this emphasis on 'big' S&T; what are the fundamental barriers to small organization implementation? How can medium and small organizations engage in roadmapping?
4. What are the true roadmapping burdens in time, cost, and other resources? How much should roadmapping cost?
5. What are the limits to roadmapping application? Is there 'creep' beyond product / portfolio management applications?
6. To what extent is automation useful for roadmapping? What kinds of tools are required?
7. As roadmaps are tending to become broader in scope (e.g., crosscut industry roadmaps), how much can these roadmaps continue to be useful as working tools?
8. What are the barriers to international roadmapping/ roadmap development in a global environment?
9. Is there a need to structure a more formal research program/ curriculum for roadmaps and roadmapping in order to formalize the practice and create / build a body of knowledge?

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Appendix 3-A. "The 101st Benchmark"[1]

by Bob Colwell

You start a major project such as a new microprocessor design in a small room with about 5 of the brightest people in the company. That group establishes a few initially promising directions for the architecture and microarchitecture of a new chip. The architecture manager deploys a small team to go chase down those ideas and confirm-or-deny them. After about 5 months the best one is picked, and everyone jumps onto it, fleshing it out, testing it, and filling in any conceptual blanks from the early vision.

As time goes on, the RTL designers, circuit designers, layout folks, and others get involved, and the project picks up momentum. After 2 to 2.5 years of this, the RTL has come together and the circuit design team has gotten serious about whether they can actually realize the circuits implied by the RTL and the design goals (e.g., clock rate).

Only at this point can the architecture and performance teams start asking deep questions about how well this new machine will perform against non-trivial benchmarks. All along, of course, there has been a performance model developed and tested by the performance team, but that model always has limitations and areas where it diverges seriously from the RTL. Sometimes you know where those holes are, and sometimes you get surprised. The point is that the project is close to 3 years old when you get to this phase where the real performance cracks begin to appear - and they always do. That's why this is referred to as the "101st" benchmark problem, not the "4th" benchmark problem. You've been testing benchmarks all along, on the RTL and on the performance model, and had any of those been disastrous, you'd have already fixed them.

Then a serious performance problem occurs and you begin to delve deeply into exactly why this particular benchmark is so bad if the other 100 weren't. Three possibilities:

a. Simple bug: fix it, now all 101 benchmarks look good.

b. Not simple: complicated interaction of 17 different microarchitecture mechanisms. Band-aids look feasible; lose a little performance on some of other 100 benchmarks but 101st now ok.

c. Complex: best band-aid itself is very complex and not well understood. Implement that and strenuously test.

The hard issues are generally associated with "c" above. You implement the best band-aid you can find, then retest all benchmarks to see if you've broken anything while trying to fix the 101st. A month of this ensues, in which the army of validators is off retesting their entire validation suite in case the new performance fix has broken anything functionally. This results in the designers implementing the new fix in a slightly buggy way, and the usual sequence of code/test/validate/debug/new-code commences.

Eventually the validators come back and tell you "ok, the machine mostly works, but we're seeing occasional deadlocks now, and we think they're related to your performance fix. About every 90 billion instructions we see this." Running anything like 90 billion instructions of simulation is impossible pre-silicon (chip prototype); RTL simulators are far too slow for that. So the validators are using some statistical methods to have estimated that one-in-90 billion.

And now you're at the crux of the issue. At this point you have reasonable assurance that there is a deadlock problem in your new machine. The architects say they have no better way to fix the performance problem short of ripping up too much of the current design. The validators believe that the newly-implemented fix causes occasional deadlocks. (By the way, a machine that runs at 2GHz may be executing up to 4 billion instructions per second, so one-in-90 billion would

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[1] Bob Colwell, e-mail to the author, June 6, 2002.

manifest as the machine running for 20 seconds and hanging. Not a recipe for a successful product.)

So you commission the architects to take one last look at the deadlock problem because they might see a way to avoid it. They don't. So you then commission them to see if there's a way for the machine to at least recognize that it has gotten into the deadlock state, and get itself out of that. They find several ways to accomplish that. By this time, schedule pressures become paramount and make you override that nagging doubt that this is a reasonable way to design complicated machines. The result: you implement the fixes (of fixes).

What have you done? You've now thrown so much complexity into the performance struggle that the machine is behaving in some unexpected ways; you fix those by tacking on even more complicated stuff, which then causes it to hang occasionally in ways that are too difficult to fix. So you let that happen, but throw in one more level of complexity to detect it and reset the machine state back to a place where you know it will behave more predictably.

Appendix 7-A. Manufacturers of Microprocessors, 1975[2]

(Firms in late 1975 producing or about to produce microprocessors)

Advanced Micro Devices, Inc.
American Microsystems, Inc.
Burroughs Corp.
Electronic Arrays, Inc.
Fairchild Camera and Instrument Corp.
General Instrument Corp.
Intel Corp.
Intersil, Inc.
Monolithic Memories, Inc.
MOS Technology, Inc.
Mostek Corp.
Motorola, Inc.
National Semiconductor Corp.
Panafacom
Raytheon Co.
RCA Corp.
Rockwell International Corp.
Scientific Micro Systems
Signetics Corp.
Teledyne, Inc.
Texas Instruments, Inc.
Toshiba, Ltd.
Transitron Electronic Corp.
Western Digital Corp.

Source: *Electronics*, Oct. 16, 1975, p. 78; *Appliance Manufacturer*, July 1975, p. 32; *Electronic News*, June 9, 1975, p. 43; *Electronic News*, May 27, 1974, pp. 1ff.

[2] Douglas W. Webbink, *Staff Report on the Semiconductor Industry: A Survey of Structure, Conduct, and Performance*, Federal Trade Commission, Bureau of Economics, January 1977, Table V-6, 132.

Appendix 7-B. Selected Early Microprocessor-related Patents

Source: Delphion Research online at http://www.delphion.com and http://www.uspto.gov/

Patent:	US 3,462,742	Title:	Computer System Adapted to be Constructed of Large Scale Integrated Circuit Arrays
Assignee:	RCA Corporation, New York, NY	Inventors:	Miller, Henry S.; Linhardt, Robert J.; Sidnam, Robert T.
Filed:	1966-12-21	Published:	1969-08-19
Excerpt:	A general-purpose computer system is disclosed which is particularly adapted to be constructed of a plurality of integrated circuit arrays. The computer system consists of partitioned parts which are interconnected by means of system buses… Each partitioned unit is preferably fabricated in the form of a single integrated circuit array… Prior computer systems have been constructed of individual component circuits or gates and have been organized to employ a minimum total number of such circuits. Now it is possible to fabricate an array of a large number (such as 100 or 200) of interconnected circuits or gates as a single unit known as an integrated circuit array. A "large" integrated circuit array is one having over 50 gates.		

Patent:	US 3,760,375	Title:	Source Data Entry Terminal
Assignee:	Sycor, Inc., Ann Arbor, MI	Inventors:	Irwin, Samuel N.; Ann Arbor, MI; Levine, Michael R.; Ann Arbor, MI
Filed:	1971-07-26* [originally filed 1969-06-13]	Published:	1973-09-18
Excerpt:	A source data entry terminal device for capturing and storing data for future processing or the like, comprising in combination: a keyboard …; an optical display …; and a programmed microprocessor interfaced to each of said entry means, said display means and said coupling means; said microprocessor including a fixed-program read-only memory and a central logic unit embodying substantially all of the control logic for said entry means and display means; said read-only memory having a built-in program dedicating the terminal to a particular functional configuration and establishing an instruction set which time-shares said central logic unit with said entry means and display means to control the same in conformance with such functional configuration.		

Patent:	US 3,579,201	Title:	Method of Performing Digital Computations Using Multipurpose Integrated Circuits and Apparatus Therefor
Assignee:	Raytheon Company, Lexington, MA	Inventor:	Langley, Frank J.; Carlisle, MA
Filed:	1969-09-27	Published:	1971-05-18
Excerpt:	A digital computer, exemplifying a method of organizing and controlling the elements of a general or special purpose computer, incorporating identical multipurpose		

	integrated circuits in the control and/or arithmetic elements, each one of such circuits being responsive to the combination of commonly applied clock pulses and coded function signals and a unique enable signal. With such an arrangement, a basic design of such control and/or arithmetic elements may be changed to expand word length, memory capacity or instruction repertoire by connecting similar multipurpose integrated circuits to existing ones as required… a primary object of this invention to provide an improved digital computer in which identical multipurpose integrated circuits are used in the control and/or arithmetic elements.

Patent:	US 3,702,988	Title:	Digital Processor
Assignee:	The National Cash Register Company	Inventors:	Haney, Ralph D.; Zacher, James E.; Drozd, Charles J.
Filed:	1970-09-14	Published:	1972-11-14
Excerpt:	A digital processor built entirely of metal-oxide semiconductor devices constructed on integrated circuits by large-scale integration techniques is shown… One good way to reduce the cost and the size of any digital system is through the use of four-phase metal-oxide semiconductor (MOS) large scale integration (LSI) integrated circuits. On a given substrate of silicon, one may construct, by MOS LSI techniques, hundreds or thousands of different MOS transistor elements which operate as switches. Thus one may build a digital processor using the four-phase MOS LSI techniques on, for instance, twenty or thirty integrated circuits. The drawback when MOS integrated circuits are used is that they are relatively slow when compared to, for instance, transistor-transistor logic type integrated circuits. However … certain applications speed is a relatively minor factor, and economy is the major consideration.		

Patent:	US 3,654,617	Title:	Microprogrammable I/O Controller
Assignee:	IBM Corporation, Armonk, NY	Inventor:	Irwin, John W.; Longmont, CO
Filed:	1970-10-01	Published:	1972-04-04
Excerpt:	A microprogrammable plural ALU (arithmetic-logic unit) controller utilizes task assignments for improving processing efficiencies. The ALU's are selected to be low-cost, low-capability devices. Each ALU is within one independent Micro Programmable Unit (MPU). Interconnection registers, preferably symmetrically arranged, provide program synchronization between the plural MPU's.		

Patent:	US 4,942,516	Title:	Single Chip Integrated Circuit Computer Architecture
Assignee:	None	Inventor:	Hyatt, Gilbert P.; La Palma, CA 90623
Filed:	1988-06-17* [originally filed 1970-12-28]	Published:	1990-07-17
Excerpt:	A single chip stored program digital computer implemented on a single integrated circuit chip, said single chip stored program digital computer including an integrated circuit read only memory storing computer instructions, wherein said integrated circuit read only memory is implemented on said single integrated circuit chip.		

Patent:	US 3,859,635	Title:	Programmable Calculator
Assignee:	None, but later Hewlett-Packard, US 3,839,630 filed 1971-12-27	Inventors:	Watson, Robert E.; Walden, Jack M.; Near; Charles W.
Filed:	1971-06-15	Published:	1975-07-07
Excerpt:	A modular read-write and read-only memory unit capable of employing both direct and indirect decimal and symbolic addressing, a central processing unit capable of performing both serial binary and parallel binary-coded-decimal direct and indirect memory register arithmetic, and an input-output control unit capable of bidirectionally transferring information between the central processing unit and a number of input and output units are controlled by a microprocessor included in the central processing unit… The central processing unit includes four recirculating 16-bit serial shift registers, a four-bit serial shift register, the arithmetic logic unit, a programmable clock, and a microprocessor… The microprocessor includes a read-only memory in which a plurality of microinstructions and codes are stored.		

Patent:	US 3,757,306	Title:	Computing Systems CPU
Assignee:	Texas Instruments Inc., Dallas, TX	Inventor:	Boone, Gary W.; Houston, TX
Filed:	1971-08-31	Published:	1973-09-04
Excerpt:	A central processing unit (CPU) is utilized in combination with external random access or serial memory units. The CPU includes a parallel arithmetic logic unit (ALU), accumulator and file register, program and memory address register, and a 7 level program address stack. The parallel processor includes programmable logic arrays, shift registers, and random access memories combined monolithically on a single chip… The present invention is directed to a central processing unit (CPU) integrated on a single chip in combination with external RAM and ROM memory units… The CPU can be divided generally into four sections: a data section, an address section, a control section, and an arithmetic logic unit.		

Patent:	US 4,037,094	Title:	Multi-functional Arithmetic and Logical Unit
Assignee:	Texas Instruments Inc., Dallas, TX	Inventor:	Jerry L. Vandierendonck; Houston, TX
Filed:	1971-08-31	Published:	1977-07-19
Excerpt:	[Note: this patent is almost identical to the previous "Boone" patent; it was filed simultaneously but published four years after the Boone patent. The abstract differs slightly as shown below.] A computing system includes a central processor unit (CPU) in combination with external memory units. The CPU includes an arithmetic logic (ALU), an instruction register, a random access memory, and a control system for interconnecting the functional elements of the CPU via sequential use of a common parallel buss, enabling the CPU to be defined on a single chip.		

Patent:	US 3,757,308	Title:	Data Processor
Assignee:	Texas Instruments Inc., Dallas, TX	Inventor:	Fosdick, Robert E.; Austin, TX
Filed:	1971-09-03	Published:	1973-09-04
Excerpt:	A MOS data processor fabricated on a single MOS semiconductor chip. The logic, arithmetic and storage functions are fabricated on one semiconductor chip.		

Patent:	US 3,748,452	Title:	Electronic Cash Register
Assignee:	Vorhee; Alan M., Montgomery County, MD	Inventor:	Ruben, Murray A.
Filed:	1971-11-17	Published:	1973-07-24
Excerpt:	An electronic cash register whereby a manually operable keyboard produces signals indicating the keys operated which are received by an electronic microprocessor which in turn derives, stores and displays transaction data. The microprocessor includes a random access memory … and a read only memory.		

Patent:	US 3,793,631	Title:	Digital Computer Apparatus Operative with Jump Instructions
Assignee:	Westinghouse Electric Corp., Pittsburg, PA	Inventors:	Silverstein, Steven L.; Daggett, Kenneth E.
Filed:	1972-09-22	Published:	1974-02-19
Excerpt:	Disclosed is a digital computer system including a programmed microprocessor system of the type used in real time systems, in industrial process control and in small scale data processing … a specific embodiment of the subject microprocessor system may be structured modularly… Thus, such system can be used as a small, high speed, read-only memory, programmable microprocessor system intended, for example, to replace relay logic, for industrial process control applications, to control peripherals, or as a communications controller. This small system may comprise only three basic units: a basic microprocessor including an arithmetic and logic unit ALU; a read-only memory ROM; and a small set of addressable registers.		

Patent:	US 3,878,514	Title:	LSI Programmable Processor
Assignee:	Burroughs Corporation, Detroit, MI	Inventor:	Ulbe Faber, Honeybrook, PA
Filed:	1972-11-20	Published:	1975-04-15
Excerpt:	A microrogrammable serial byte processor suitable for complete implementation of memory, logic, control and addressing functions on a single integrated circuit chip through large scale integration technology. An instruction set, at the microprogrammable level, is provided for controlling the processor in executing basic computer functions… Specific circuitry for executing serially by bit the individual instructions of the instruction set is maintained at a simple and minimal level by		

	employing a soft machine architecture with a microprogramming approach.

Patent:	US 3,943,495	Title:	Microprocessor with Immediate and Indirect Addressing
Assignee:	Xerox Corp., Stamford, CT	Inventor:	Garlic, Richard A.; Irvine, CA
Filed:	1972-12-26	Published:	1976-03-09
Excerpt:	A microprocessor with a bus structure for carrying address and data signals wherein an address may be modified by an index value for indirect addressing.		

Patent:	US 3,821,715	Title:	Memory System for a Multi-chip Digital Computer
Assignee:	Intel Corporation, Santa Clara, CA	Inventor:	Marcian Edward Hoff, Jr., Stanley Mazor, Federico Faggin
Filed:	1973-01-22	Published:	1974-06-28
Excerpt:	A general purpose digital computer which comprises a plurality of separate MOS chips is described. The chips are interconnected by a number of lines, including four bi-directional data bus lines. One chip includes a central processing unit that is coupled by the bi-directional lines to a plurality of memory chips which include random-access-memories (RAM) and read-only-memories (ROM). A plurality of separate RAMs and ROMs may be added to the bidirectional lines… In the presently preferred embodiment, each of the chips are mounted on standard 16 pin dual in-line packages… The processor shown in FIGS. 1 and 2 may be fabricated using circuits used in many prior art central processing units utilized by digital computers. In the presently preferred embodiment the processor which is fabricated on a single MOS chip includes a control unit, a four-bit arithmetic unit, an index register, and an address register.		

Patent:	US 3,999,165	Title:	Interrupt Information Interface System
Assignee:	Hitachi, Ltd., Japan	Inventors:	Yuzo Kita and Kazuo Watanabe, Kokubunji, Japan
Filed:	1973-08-27	Published:	1976-12-21
Excerpt:	The primary object of the present invention is to provide an interrupt interface system which may be satisfactorily applied to an LSI one-chip computer. Briefly stated, registers into which interrupt information is set and an LSI one-chip computer are interconnected by a single interface line so that the set interrupt information may be transferred.		

Patent:	US 4,087,852	Title:	Microprocessor for an Automatic Word-Processing System
Assignee:	Xerox Corp., Stamford, CT	Inventors:	Kenneth C. Campbell, Werner Schaer, Harry W. Swanstrom

Filed:	1974-01-02	Published:	1978-05-02
Excerpt:	The keyboard, printer and recording means are peripheral units under the control of a microprocessor including a programmable read-only memory from which appropriate control instructions are derived.		

Patent:	US 3,986,170	Title:	Modular Control System Design With Microprocessors
Assignee:	GTE Automatic Electric Labs, Inc., Northlake, IL	Inventors:	John G. Valassis, Elmwood Park, IL; James R. Holden, Chicago, IL; Madhukumar, Gujrat, India
Filed:	1974-05-30	Published:	1976-10-12
Excerpt:	This invention relates to an expandable modular control system with reduced memory requirements employing a universal microprocessor module comprising a microprocessor device and having novel program interrupt means.		

Patent:	US 4,177,511	Title:	Port Select Unit for a Programmable Serial-bit Microprocessor
Assignee:	Burroughs Corp., Detroit, MI	Inventor:	Taddei, Vincent J.; West Chester, PA
Filed:	1974-09-04	Published:	1979-12-04
Excerpt:	An apparatus and method for selecting the operation of digital data ports for regulating information flow between a programmable serial-bit, microinstruction processor and a multiplicity of peripheral devices connected to the processor.		

Patent:	US 3,984,813	Title:	Microprocessor System
Assignee:	Fairchild Camera and Instrument Corp., Mountain View, CA	Inventor:	Chung, David H.; Palo Alto, CA
Filed:	1974-10-07	Published:	1976-10-05
Excerpt:	A microprocessor system having at least two separate large scale integration devices. A first of the two large scale integration devices is a central processing unit formed on a single semiconductor die, and the second large scale integration device is a memory circuit formed on a separate single semiconductor die. The term "die" as used herein is conventional and refers to a unitary semiconductor body or chip. The central processing unit requires an external program counter which contains memory addresses of instruction codes to be used by the central processing unit. The memory device is electrically coupled to the central processing unit and includes a memory for storing the instruction codes, and a program counter for addressing the memory. Provision is made to incorporate additional memory circuits to expand the size and capability of the microprocessor system. System interrupt circuitry is also provided for interrupting system operation to change to a new sequence of instruction codes.		

Patent:	US 3,970,998	Title:	Microprocessor Architecture
Assignee:	RCA Corporation, New York, NY	Inventor:	Weisbecker, Joseph A.; Cherry Hill, NJ
Filed:	1974-10-15	Published:	1976-07-20
Excerpt:	Background of the Invention: This application is related to U.S. Pat. No. 3,798,615 [published 1974-03-19, filed 1972-10-02] by the same inventor and assigned to the same assignee as this application. The material therein is hereby incorporated as reference. 1. Field of the Invention [Definition]: This invention relates to microprocessors. A microprocessor is a device capable of performing arithmetic, logical, and decision making operations under the control of a set of stored instructions, but of small size, capable of being manufactured on a few (not more than four) integrated circuits… 2. Description of the Prior Art: Large scale integration techniques have made it possible to produce in a small space, logic circuits which formerly required thousands of discrete devices… One of the problems encountered when putting a data processing system on a few integrated circuits is the limitation on the number of external connections that can be made to the integrated circuit. The invention disclosed is a microprocessor organization that is suitable for implementation on a single integrated circuit requiring a minimum of external connections consistent with an acceptable operating speed.		

Patent:	US 3,987,418	Title:	Chip Topography for MOS Integrated Circuitry Microprocessor Chip
Assignee:	Motorola, Inc., Chicago, IL	Inventor:	Buchanan, John K.; Tempe, AZ
Filed:	1974-10-30	Published:	1976-10-19
Excerpt:	The chip architecture of an MOS microprocessor chip includes data bus input-output buffer circuitry located along the lower right hand edge of the chip. High order address buffer output circuitry is located along the bottom of the chip. Directly to the left of the data bus input-output buffer circuitry is the arithmetic logic unit circuitry, and to the right of this and adjacent to the high order address bit buffer circuitry is located a register section including first accumulator register, a second accumulator register, high and low order index registers, a high order incrementer and an associated program counter, a low order incrementer and associated program counter, a high order stack pointer register and a low order stack pointer register, and a temporary register arranged on the surface of the microprocessor chip in a particular sequence. To the left of the register section and along the lower left hand edge of the chip is located a plurality of low order address bit buffer circuits. Above and coupled to the register section and to the arithmetic logic unit is located a plurality of bootstrap driver circuits for driving signals which enable programmed data transfers between the various registers, the arithmetic logic unit and a plurality of internal data bus and address bus conductors coupled to the data bus input-output buffer circuitry and the high order and the low order address bit buffer circuits, respectively. Read/write circuitry, a condition code register, decision logic circuitry, and an instruction register are located in sequence along the upper righthand edge of the chip. To the left of the decision logic circuitry and the condition code register and above the bootstrap driver circuitry and coupled thereto is a logic control circuitry		

	section. Above the logic control circuitry and along the upper edge of the chip to the left of the instruction register is located an instruction decoder circuitry section. Along the upper lefthand edge of the chip is located input-output control circuitry and look-ahead circuitry for the instruction decoder. Between the lefthand portion of the logic control circuitry and the right hand portion of the I/O control circuitry is located timing generator circuitry coupled to the logic control circuitry for enabling the selected logic gates therein, which are selected and driven by the instruction decoder.

Patent:	US 3,980,992	Title:	Multi-microprocessing Unit on a Single Semiconductor Chip
Assignee:	Burroughs Corporation, Detroit, MI	Inventors:	Bernardo Navarro Levy, Ann Arbor, MI; David Chin-Chung Lee, San Diego, CA
Filed:	1974-11-26	Published:	1976-09-14
Excerpt:	This disclosure relates to a microprocessor unit which is adapted for implementation in a single MOS semiconductor chip, which unit includes a plurality of sets of registers where each set represents a different processing capability… This invention relates to a microprogram multiprocessing system which resides in a single semiconductor chip.		

Patent:	US 4,101,449	Title:	MOS Computer Employing a Plurality of Separate Chips
Assignee:	Intel Corporation, Santa Clara, CA	Inventors:	Federico Faggin, Masatoshi Shima, Stanley Mazor
Filed:	1974-12-31	Published:	1977-03-01
Excerpt:	Improvements in an MOS computer have been disclosed which enable the fabrication of a multi-chip MOS digital computer for less cost and with more potential capability than with similar prior art computers. We claim … an MOS computer employing a plurality of separate chips including a separate central processing unit chip (CPU chip) …; at least one memory disposed on a second chip; a plurality of bidirectional data bus lines interconnecting said CPU with said memory.		

Appendix 8-A. Chapter 8 Bibliography

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Appendix 9-A. Early Roadmap Reports in DoD and related Government Agencies

Overview

Most of the following citations (over two dozen in all, many with abstracts) were obtained on-line from the Scientific and Technical Information Network http://stinet.dtic.mil/ from a simple keyword search for "roadmap" or "road map." The Defense Technical Information Center (DTIC) Scientific and Technical Information Network (STINET) Service helps the DoD community access pertinent scientific and technical information to meet mission needs more effectively. Public STINET provides access to all unclassified, unlimited citations to documents added into DTIC from late December 1974 to present. These particular citations date from 1975 to 1986. Although this is most likely not a complete account,[3] this list does represent the kind of roadmap activity going on within US Government agencies prior to the formation of Sematech in 1987. This time period also overlaps the period industry informants state that company roadmapping practices emerged (i.e., starting in the mid 1970s).

This list contains references from all armed services, however the Air Force represents almost one-half of the total, followed by the Army, Navy (including Marines), then DoD/DARPA. The FAA and NASA also have citations.

Year	Dept	Title	Excerpt
1975	Army	An Analysis of the Army Wholesale Supply Management Information and Control Systems **(ROADMAP)**	The report determines if the existing or planned supply management information and control systems are compatible with a general logistics philosophy designed to support Army operations.
1976	Navy/ ARPA	On Cognitive Strategies for Facilitating Acquisition, Retention, and Retrieval in Training and Education	The idea ... is explored in relation to recent advances in the cognitive and neurosciences, with the objective of integrating information from these sources into a unified viewpoint that could serve as a **roadmap** for research and as a context for discussion.
1976	Army	Risk Analysis of the Army Production Plan for Self-Propelled Howitzers	Based on the relationships/interfaces among the milestones, a network model was developed to depict these relationships and serve as a **road map** for accomplishing the goals within the desired time frame.
1978	Navy	A **Road Map** of Methods for Approximating Solutions of Two-Point Boundary-Value Problems	no abstract available
1979	Army	The Armor Development Plan. Volume II	It presents a plan--a **roadmap**--for the future of training in Armor.
1980	Air Force	Mini-Drone/RPV Technology **Road Map**	no abstract available

[3] There may be DoD references prior to 1975, but the DTIC database begins at this time. Further, this database only shows data that is unclassified.

1980	Air Force	Predictive Software Cost Model Study: Volume I	The objectives of this Phase I study of the Predictive Software Cost Model (PSCM) program were to determine the feasibility ... and to generate a **roadmap** for development of such a model.
1980	Navy	**Roadmap** for Navy Family Research	The purpose of this effort was to develop a **roadmap** or plan for systematically targeting Navy research at the most critical family issues and providing long-range guidance for Military family research.
1980	FAA	The FAA Plans and Programs for the Future Airport and Air Traffic Control System	Today's ATC System-Problems and Need for Change; An Overview of the FAA Engineering and Development Program; Scenario for the Future System - The **Roadmap** of the System of the future.
1981	FAA	Preliminary Functional Description of Integrated Flow Management	A **road map** projection of the IFM near term evolution through the late 1980s and remaining open issues related to the IFM development are also presented.
1981	Army	Subpopulation Differences in Performance on Tests of Mental Ability	Selected references (40) are briefly described in an annotated bibliography in order to: . . . (c) provide a general **'road map'** for those who wish to pursue further the subject of the paper.
1982	NASA	Systems Study of Transport Aircraft Incorporating Advanced Aluminum Alloys	The results of the investigation provided a **roadmap** and identified key issues requiring attention in an advanced aluminum alloy and application technology development program.
1982	Air Force	Night Attack Workload Steering Group. Volume III. Simulation and Human Factors Subgroup	In composite the SHFR recommendations provide a comprehensive **roadmap** for workload data development needed to support night attack system acquisition through the 1980s.
1984	Navy	**Roadmap** for Navy Civilian Personnel Research	The **roadmap** includes a model for prioritizing research projects and for managing research efforts through time.
1984	Air Force	On Space Warfare: Military Strategy for Space Operations	The results of this exploration must them be consolidated into an agreed upon long-range strategy for space that will serve as our **road map** to the future.
1984	Air Force	ICAM (Integrated Computer Aided Manufacturing) Conceptual Design for Computer-Integrated Manufacturing.	[R]eport that simplifies the modernization process considerably by providing a logical process to sequence improvement events, prioritize those operations that merit immediate attention, eliminate replications of procedures, and establish a pattern or **road map** that is designed to be a pertinent while ... flexible.
1984	Navy	Prioritization of	Following the development of a **roadmap** or plan (Phase I of this Project) for systematically

		Roadmap Research	targeting research efforts . . . , the research areas designated in that **roadmap** were prioritized.
1985	Air Force	Military Space Systems Technology Plan. Volume 5B. Part 2. **Roadmaps**	no abstract available
1985	Air Force	LAN (Local Area Network) Interoperability Study of Protocols Needed for Distributed Command and Control	The study examined distributed processing requirements for strategic and tactical C3I systems ... Ten recommendations are given, providing a **roadmap** to guide the Air Force in developing C3I systems and LAN-based protocols.
1985	Air Force	Analysis of Applications for an Interactive Maintenance-Aiding System	The objectives of this study were to 1) explore the feasibility and benefits ... and 4) develop a **roadmap** for implementation of an IMAS, including prototype development.
1985	Air Force	The AFSC (Air Force Systems Command) Cost Methods Improvement Program (CMIP) **Road Map**	The Cost Methods Improvement Program (CMIP) was formed with the development of the AFSC Cost Analysis Improvement Group (CAIG) in 1981. The CAIG prioritizes and approves funding for research projects which benefit more than one Product Division.
1986	DoD/ DARPA	MIMIC **Roadmap** Released by DoD	MIMIC was the DoD's Microwave and Millimeter-Wave Integrated Circuit program.
1986	Air Force	Artificial Intelligence/Expert System Cost Research **Roadmap**	This **roadmap** defines the 'what, why, when and the priority and cost of the specific tasks to be undertaken' that will enable quality cost estimates for AI/ES projects in the future.
1986	Army	Medical Materiel Acquisition Management Handbook	It describes the Medical Materiel Life Cycle System Management process and serves as . . . a **roadmap** for product development action officers to follow.
1986	Army	Army Strategic Plan for Civilian Personnel Management Research: A **Roadmap** for the Future	The **Roadmap** provides a framework for capturing and analyzing data needed to formulate and implement effective management policies and programs that address the objectives of the Army's civilian personnel system.

Appendix 10-A. Anti-trust Ground Rules

Source: International Sematech, "Industry Executive Forum," December 8, 2000

Meeting participants must not make any agreement that restricts output, capacity or the pace of technology innovation.

- No discussion on what any company will do on:
  - Prices it will charge, or any pricing formula it will use
  - Products it will offer, unless previously publicly announced
  - Quantities it will produce or min / max capacity it will add

- No agreement on timing of technology changes
  - Individual companies may state their individual timing to ensure availability of tools and infrastructure
  - May not predicate timing on what competitors are willing to do or agree to

Appendix 10-B. NTRS/ITRS Roadmap Editions

Semiconductor Industry Association, *Semiconductor Technology: Workshop Conclusions, and Workshop Working Group Reports* (two volumes), San Jose, CA, 1992.

Semiconductor Industry Association, *The National Technology Roadmap for Semiconductors*, San Jose, CA, 1994.

Semiconductor Industry Association, *The National Technology Roadmap for Semiconductors: Technology Needs*, 1997 Edition, San Jose, CA, 1997.

Semiconductor Industry Association, *International Technology Roadmap for Semiconductors, 1999 Edition*, San Jose, CA, 1999.

Semiconductor Industry Association, *International Technology Roadmap for Semiconductors, 2001 Edition*, San Jose, CA, 2001.

Semiconductor Industry Association, *International Technology Roadmap for Semiconductors, 2003 Edition* (proof copy), San Jose, CA, 2003.

Also available online at http://public.itrs.net/

Appendix 10-C. NTRS/ITRS Process Interviewees

Function	Name	Organization[4]	Date
Chipmaker USA	Alan Allen	Intel	1999/2000
	Mark Bohr	Intel	January 2000
	John Carruthers	Intel	November 1999
	Bob Doering	Texas Instruments	1999-2001
	Paolo Gargini	Intel	August 1999
	Gordon Moore	Intel	February 2002
	Tak Ning	IBM	July/August 2000
	Steve Schulz	Texas Instruments	September 1999
	Don Wollesen	AMD	August 1999
Chipmaker Int'l	Toshitaka Fukushima	Fujitsu	May 2000
	Genda Hu	TSIA, ERSO, ITRI, TSMC	May 2000
	Werner Klingenstein	Infineon Technologies	May 2000
	Alec Reader	Philips	May 2000
	Werner Weber	Infineon Technologies	May 2000
SM&E	Mark Bird	Amkor Technology	August 1999
	Sam Broydo	Applied Materials	March 2000
	Chi Shih Chang	Kulicke & Soffa	September 2002
	Walter Class	Eaton	March 2000
	Jim Greed	Foothill Technology (for SEMI)	June 2000
	Sam Harrell	KLA-Tencor	May 2000
	Larry Novak	URS/Radian International	August 1999
	Paul Peercy	Semi/Sematech (SISA)	September 1999
	Tom Seidel	Genus, Inc.	August 1999
SIA	Juri Matisoo	SIA	August 2000
Sematech	Alain Diebold	International Sematech	August 1999
	Bill Spencer	International Sematech	August 1999
	Bob Werner	International Sematech	April-July 1999
	Linda Wilson	International Sematech	1999 to 2004

[4] This is the organization at the time of the interview. Note that many interviewees had (and have since) worked in different organizations as Roadmap participants.

SRC	Ron Bracken	SRC	August 2000
	Bob Burger	SRC	July 1999
	Ralph Cavin	SRC	August 2000
	Dan Herr	SRC	August 2000
	Jim Hutchby	SRC	August 2000
	Bill Joyner	SRC	August 2000
	Court Skinner	SRC	1999-2000
University	Steve Brueck	University of New Mexico	July 2000
	Andrew Kahng	UC San Diego	February 2002
	Jim Meindl	Georgia Tech	August 1999
	Al Tasch	University of Texas	September 1999
Government	Karen Brown	NIST	August 1999
	Jim Glaze	Virtual National Lab	July 1999
	Bob Scace	NIST (Klaros)	1999-2000
Analyst	Katherine Derbyshire	Semiconductor Online	January 2001
	Dan Hutcheson	VLSI Research	March 2000
	Ron Leckie	Infrastructure	June 2000
	Dan Tracy	Rose Associates	March 2000
Other	Turner Hasty	Retired (formerly Sematech, TI)	May-August 2000
	Bill Howard	Consultant, Retired (formerly Motorola)	1999-2000
	Obi Oberai	Retired (formerly Sematech, IBM)	April-May 2000
	Owen Williams	Retired (formerly Motorola)	August 1999

Appendix 10-D. NTRS/ITRS Selected Bibliography

1992/1994 NTRS

W.J. Spencer and T.E. Seidel, “National Technology Roadmaps: The U.S. Semiconductor Experience,” invited paper (Conference in China), approximately 1995, 211-220.

Jim Glaze, Owen Williams, Tom Seidel, and Bob Burger, "The National Technology Roadmap for Semiconductors," manuscript, approximately 1995, 8pp.

Karen H. Brown, “SEMATECH and the national technology roadmap: needs and challenges,” *SPIE, Optical/Laser Microlithography VIII*, Vol. 2440, 1995, 33-37.

Tak H. Ning, "A CMOS Technology Roadmap for the Next Fifteen Years," *Proceedings of 1995 IEEE Tencon*, 4pp.

William T. Lynch, “The SOI Option – The SRC Research Portfolio and its Relationship to the SIA Roadmap," *Electromechanical Society Proceedings*, Vol. 96-3, 1996, 351-363.

James D. Plummer, “TCAD – The Semiconductor Industry Roadmap and a Path to the Future, *Electromechanical Society Proceedings*, Vol. 96-4, 1996, 3-17.

Sam Harrell, Tom Seidel, and Bernard Fay, “The National Technology Roadmap for Semiconductors and Sematech Future Directions,” *Microelectronic Engineering*, Vol. 30, 1996, 11-15.

Gordon E. Moore, "Some Personal Perspectives on Research in the Semiconductor Industry," 165-174, Chapter 7 in Richard S. Rosenbloom and William J. Spencer (eds.), *Engines of Innovation: U.S. Industrial Research at the End of an Era*, Boston: Harvard Business School Press, 1996.

Heiner Herbst, Doris Schmitt-Landseidel, and Matthias Schobinger (Siemens AG), “From Roadmaps to Reality: The Challenges of Designing Tomorrow’s Chips,” *IETE Technical Review*, Vol. 13, No. 6, November-December 1996, 345-349, (reprinted with permission from Seimens Review, R&D Special, Spring 1996).

Giuseppe Zocchi, "Semiconductor Technology Roadmap and Industry Strategic Planning, *IEEE Proceedings of Melecon '96*, May 1996, 75-79.

Marie L. Garcia, *Introduction to Technology Roadmapping: the Semiconductor Industry Association's Technology Roadmapping Process*. Albuquerque, NM: Sandia National Laboratories Report SAND97-0666, April 1997, 50p.

Donald G. Rea, Harvey Brooks, Robert M. Burger, and Richard LaScala, “The Semiconductor Industry—Model for Industry/University/Government Cooperation," *Research-Technology Management*, July-August 1997, Vol. 40, No. 4, 46-54. Also appeared earlier in manuscript as Donald G. Rea, Harvey Brooks, Robert M. Burger, Richard LaScala, and W. Clark McFadden II, “The Semiconductor Industry: A Paradigm for Industry/University/Government Cooperation,” approximately 1995.

Larry D. Browning and Judy C. Shetler, *Sematech: Saving the U.S. Semiconductor Industry*, College Station, TX: Texas A&M University Press, 2000.

1997 NTRS

Lewis M. Branscomb and James H. Keller (eds.), *Investing in Innovation: Creating a Research and Innovation Policy That Works*, Cambridge, MA: The MIT Press, 1998.

Rose Marie Ham, Greg Linden, and Melissa M. Appleyard, "The Evolving Role of Semiconductor Consortia in the United States and Japan," *California Management Review*, Vol. 41, No.1, Fall 1998, 137-63.

A.P. Mozer, "Silicon Wafer Technology, Status and Overlook at the Millennium and a Decade Beyond," *Solid State Phenomena*, Vols. 69-70, 1999, 1-10.

1999 ITRS

Robert R. Doering, "Limitations of (and Off) the SIA Roadmap Trends," manuscript, 1999.

Robert M. Burger, *Cooperative Research: The New Paradigm, Semiconductor Research Corporation*, manuscript, 2000.

Tak H. Ning, "CMOS in the New Millennium," *IEEE Custom Integrated Circuits Conference*, 2000, 49-56.

Appendix 10-E. NTRS/ITRS Selected Press Coverage

I. 1992 Roadmap

1. Jack Robertson, "Moore: Unify Tech Strategy," (interview with Intel Corp. Chairman Gordon Moore) *Electronic News*, July 27, 1992.
2. Jack Robertson, "Sematech Funding Seen Restored in Bill," *Electronic News*, October 5, 1992.
3. Jack Robertson, "New Roadmap Pinpoints IC Goals: Semiconductor Industry Association Seminar Sets 15-Year Plan for Integrated Circuits," *Electronic News*, November 23, 1992.
4. Jack Robertson, "SIA Technology Roadmap Hits the Streets: Semiconductor Industry Association's Plan for Industry Future," *Electronic News*, March 1, 1993.
5. William J. Spencer, "Creating a roadmap for the U.S. semiconductor industry," *Solid State Technology*, April 1993, 67.
6. Author unknown, "Federal Labs Join Forces to Help Make U.S. Industry More Competitive," *Electronic Materials Technology News Business Comm.*, Vol. 7, No. 5, April 1, 1993.
7. J. Robert Lineback, "Sematech, Jessi Talks Progress Slowly," *Electronic News*, April 12, 1993.
8. Jack Robertson, "U.S. Lithography: A Bad Projection," *Electronic News*, May 17, 1993.
9. George Leopold, "Sematech beginning to broaden its scope," *Electronic Engineering Times*, December 13, 1993.
10. Don McIntosh, "Fab of the future: an operational view," *Solid State Technology*, Vol. 37, No. 1, January 1, 1994.
11. Robert I. Scace, "Metrology—what next?" *Solid State Technology*, Vol. 37, No. 3, March 1, 1994.
12. Peter N. Dunn, "Larger wafers coming, probably in 300-mm size," *Solid State Technology*, Vol. 37, No. 4, April 1, 1994.
13. Jack Robertson, "Japan Still Gives a DRAM," *Electronic Buyers' News*, No. 900, April 18, 1994.
14. Peter N. Dunn, "X-ray's future: a cloudy picture," *Solid State Technology*, Vol. 37, No. 6, June 1, 1994.
15. Richard C. Johnson, "Why international consortia collaboration makes sense," *Solid State Technology*, Vol. 37, No. 7, July 1994, 208.
16. Dan Maydan, "Industry should evaluate a move to 14-inch wafers," *Solid State Technology*, Vol. 37, No. 10, October 1, 1994.
17. David Hack and Jim DeTar, "Sematech Vows Future Fiscal Independence," *Electronic News*, Vol. 40, No. 2035, October 10, 1994.

II. 1994 NTRS

1. Robert Haavind, "Roadmaps versus reality: It's not always easy to follow that purple street," *Solid State Technology*, December 1994, 10.
2. Jim DeTar, "SIA accents funding issue in tech. roadmap update," *Electronic News*, Vol. 40, No. 2043, December 5, 1994, 2(2).
3. Jack Robertson, "Semi Roadmap Shows Obstacles: Report Focuses on Industry Changes," *Electronic Buyers' News*, No. 933, December 5, 1994.
4. Robert M. Burger, James A. Glaze, Tom Seidel, and Owen Williams, "The SIA's Roadmap: Consensus for Cooperation," *Solid State Technology*, February 1995, Vol. 38, No. 2, 38-40.
5. Solid State Technology, "Processes of the future," (cover story) *Solid State Technology*, Vol. 38, No. 2, February 1995, 42-53.
6. Peter N. Dunn, "SIRIJ: Japan's IC think tank will propose US-style cooperation," *Solid State Technology*, Vol. 38, No. 4, April 1995, 40 (2).
7. Solid State Technology, "Questions on the Roadmap," (Editor's note) *Solid State Technology*, Vol. 38, No. 5, May 1995, 16.
8. Ted Agres, "IC Density growth is key issue for industry," *Research & Development*, Vol. 38, No. 7, June 1996, 29-32.
9. Jim DeTar, "Advances Outpace SIA Roadmap," *Electronic News*, Vol. 42, No. 2147, December 16, 1996, 8(3).

III. 1997 NTRS

1. Paul Nesdore, "Semiconductor Industry Association Roadmap: Blueprint for tomorrow," (interview with Owen P. Williams) *Solid State Technology*, December 1997, 42, 45.
2. J. Robert Lineback, "1997 roadmap sets new course for microprocessors and DRAMs," *Semiconductor Business News*, December 1, 1997.
3. Jim DeTar, "SIA sees a new future," *Electronic News*, Vol. 43, No. 2196, December 1, 1997, 1, 85.
4. Andy Santoni, "SIA group sketches the future," *InfoWorld*, Vol. 19, No. 50, December 15, 1997, 29.
5. Linda Geppert, "Solid state," *IEEE Spectrum*, Vol. 35, No. 1, January 1998, 23-28.
6. Paolo Gargini, James Glaze, and Owen Williams, "The SIA's 1997 National Technology Roadmap for Semiconductors," *Solid State Technology*, January 1998, 73, 74, 76.
7. Ted Agres, "Roadmap Points to Crucial Semiconductor Needs," *R&D Magazine*, February 1998, 23.
8. Solid State Technology, "The Blurring generations," *Solid State Magazine*, Vol. 41, No. 2, February 1998.
9. Stanley T. Myers, "Looking for potholes along the SIA Roadmap," *Semiconductor International*, Vol. 21, No. 2, February 1998, 120.

10. Joe E. Brewer, "A New and Improved Roadmap," *Circuits & Devices*, Vol. 14, No. 2, March 1998, 13-18.

IV. 1998 Update

1. Jack Robertson, "Japanese push global roadmap that could replace SIA version," *Semiconductor Business News*, March 1998.
2. Jack Robertson, "Japanese consortium explores global roadmap effort," *Semiconductor Business News*, March 3, 1998.
3. Jack Robertson, "Where will the money come from now?" *Semiconductor Business News*, April 1998.
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Appendix: 10-F. Lithography Technology Requirements

Source: *2003 ITRS*, 374-375.

Table 77a Lithography Technology Requirements—Near-term

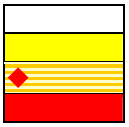
Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM							
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
Contact in resist (nm)	130	110	100	90	80	70	60
Contact after etch (nm)	115	100	90	80	70	65	55
Overlay	35	32	28	25	23	21	19
CD control (3 sigma) (nm)	12.2	11.0	9.8	8.6	8.0	7.0	6.1
MPU							
MPU/ASCI Metal 1 (M1) ½ pitch (nm)	120	107	95	85	76	67	60
MPU ½ Pitch (nm) (uncontacted gate)	107	90	80	70	65	57	50
MPU gate in resist (nm)	◆ 65	53	45	40	35	32	28
MPU gate length after etch (nm)	45	37	32	28	25	22	20
Contact in resist (nm)	130	122	100	90	80	75	60
Contact after etch (nm)	120	107	95	85	76	67	60
Gate CD control (3 sigma) (nm)	◆ 4.0	3.3	2.9	2.5	2.2	2.0	1.8
ASIC/LP							
ASIC ½ Pitch (nm) (uncontacted gate)	107	90	80	70	65	57	50
ASIC/LP gate in resist (nm)	90	75	65	53	45	40	36
ASIC/LP gate length after etch (nm)	65	53	45	37	32	28	25
Contact in resist (nm)	130	122	100	90	80	75	60
Contact after etch (nm)	120	107	95	85	76	67	60
CD control (3 sigma) (nm)	5.8	4.7	4.0	3.3	2.9	2.5	2.2
Chip size (mm^2)							
DRAM, introduction	485	383	568	419	662	449	356
DRAM, production	139	110	82	122	97	131	104
MPU, high volume at introduction	280	280	280	280	280	280	280
MPU, high volume at production	140	140	140	140	140	140	140
MPU, high performance	310	310	310	310	310	310	310
ASIC	704	704	704	704	704	704	704
Minimum field area	704	704	704	704	704	704	704
Wafer size (diameter, mm)	300	300	300	300	300	300	300

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known ◆
Manufacturable solutions are NOT known

Table 77b Lithography Technology Requirements—Long-term

Year of Production	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*
Technology Node	*hp45*		*hp32*		*hp22*	
DRAM						
DRAM ½ Pitch (nm)	45	35	32	25	22	18
Contact in resist (nm)	55	45	40	35	30	25
Contact after etch (m)	50	35	30	25	21	18
Overlay	18	14	12.8	10	8.8	7.2
CD control (3 sigma) (nm)	5.5	4.3	3.9	3.1	2.7	2.2
MPU						
MPU/ASCI Metal 1 (M1) ½ pitch (nm)	54	42	38	30	27	21
MPU ½ Pitch (nm) (uncontacted gate)	45	35	32	25	22	18
MPU gate in resist (nm)	25	20	18	15	13	10
MPU gate length after etch (nm)	18	14	13	10	9	7
Contact in resist (nm)	59	46	42	33	30	23
Contact after etch (nm)	54	42	38	30	27	21
CD control (3 sigma) (nm)	1.6	1.3	1.2	0.9	0.8	0.6
ASIC/LP						
ASIC ½ Pitch (nm) (uncontacted gate)	45	35	32	25	22	16
ASIC/LP gate in resist (nm)	32	27	22	19	16	13
ASIC/LP gate length after etch (nm)	22	19	16	14	11	9
Contact in resist (nm)	59	46	42	33	30	23
Contact after etch (nm)	54	42	38	30	27	21
CD control (3 sigma) (nm)	2.0	1.7	1.4	1.3	1.0	0.8
Chip size (mm^2)						
DRAM, introduction	563	353	*560*	*351*	*464*	*292*
DRAM, production	83	104	83	104	138	87
MPU, high volume at introduction	280	280	280	280	280	280
MPU, high volume at production	140	140	140	140	140	140
MPU, high performance	310	310	310	310	310	310
ASIC	704	704	704	704	704	704
Minimum field area	704	704	704	704	704	704
Wafer size (diameter, mm)	300	450	450	450	450	450

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Tables 77a and 77b:

[1] The dates in this table are the year of first product shipment of integrated circuits from a manufacturing site with volume exceeding 10,000 units. Exposure tools, resists, and masks for manufacturing must be available one year earlier. Development capability must be available two–three years earlier.

[2] Linewidth variations are based on linewidth deviations from target dimensions for all critical features for a given product. For example, for microprocessors these would be the gate features critical to circuit performance. This total linewidth variation includes contributions from errors within each exposure field for features of various orientations and with varying pitch. Variations also include contributions from linewidth changes across individual wafers and from wafer-to-wafer. The variances of the final dimensions after etch are assumed to result 2/3 from variance of the linewidths in resist and 1/3 from the etch process for all processes except MPU gates, where it is assumed that 80% of the variance of the linewidths comes from resist and 20% from the etch process. It is assumed that the allowable variations in linewidth are ±15% of the final, etch feature size for DRAMs and ASICS and ±10% for MPUs.

Appendix 12-A. Participating Universities in the Semiconductor Focus Center Research Program

University Participants	Gigascale Silicon Research Center	Inter-Connects for Hyper-Integrations Center	Nanoscale Technology Center	Center for Circuits Systems & Software	Functional Engineered Nano-Architectonics
Arizona State University					X
California Institute of Technology	X		X		X
Carnegie Mellon University (CMU)	X	X		**X**	
Columbia University				X	
Cornell University		X	X	X	
Georgia Institute of Technology	X	**X**		X	
Massachusetts Institute of Technology	X	X	**X**	X	X
North Carolina State University		X	X		X
Pennsylvania State University	X		X		
Princeton University	X		X		
Purdue University	X		X		
Rennselaer Polytechnic Institute		X			
Stanford University	X	X	X	X	
SUNY – Albany		X	X		
SUNY – Stony Brook					X
Univ. of Calif. Berkeley	**X**	X	X	X	X
Univ. of Calif. Los Angeles	X		X	X	**X**
Univ. of Calif. Riverside					X
Univ. of Calif. San Diego	X			X	

Univ. of Calif. Santa Barbara	X	X	X		X
Univ. of Calif. Santa Cruz	X				
University of Southern California					X
University of Central Florida		X			
University of Florida			X	X	
Univ. of Illinois - Urbana-Champaign	X			X	
University of Maryland			X		
University of Michigan	X				
University of Minnesota					X
University of Texas at Austin	X	X	X		
University of Virginia			X		
University of Washington				X	

Source: Semiconductor Industry Association, "SIA Backgrounders: Semiconductor Focus Center Research Program—Laying the Groundwork for the Future of Microelectronics," January 9, 2004. Universities in **bold** are leads of the five MARCO focus centers.

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