READOUT INTEGRATED CIRCUIT (ROIC)

FOR 8 ´ 8 QWIPs ARRAY

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Design Team

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1.0   FEATURES OF ROIC

ROIC for 8×8 QWIP array has the following features:

- Single output with 10MHz output data rate (at 77K)
- Detector bias adjustment (at array level)
- Signal skimming
- On-chip programmable gain
- Windowing (four predefined windows of 4×4 size)
- Snapshot integration
- Integrate-Then-Read and Integrate-While-Read Mode
- Invert / Revert capability in Full window
- Variable integration capability
- Temperature sensor
- On-chip ESD protection

2.0   Product Description

This X-Y addressable CMOS Readout Integrated circuit (ROIC) SC3981, is for 8×8 array of Quantum Well Infrared Photo diode (QWIPs) operating in long wavelength Infra Red (LWIR) region with detection bandwidth of 8-10 micron. The SC3981 is fabricated in in-house standard 0.8micron double poly double metal 5V process (with option of triple metal) and is specified for operation at 77K. The SC3981 is a prototype 8×8 pixel Readout Integrated Circuit (ROIC) with snapshot mode integration capability and it serves as precursor to future array of 320 x 256 pixels. This ROIC will be integrated with QWIP pixels to produce FPA (Focal Plane Array). Default mode of SC3981 directly supports single output. It supports advanced features including windowing and signal skimming, variable gain and biasing, integrate-while-read and integrate-than-read operations.
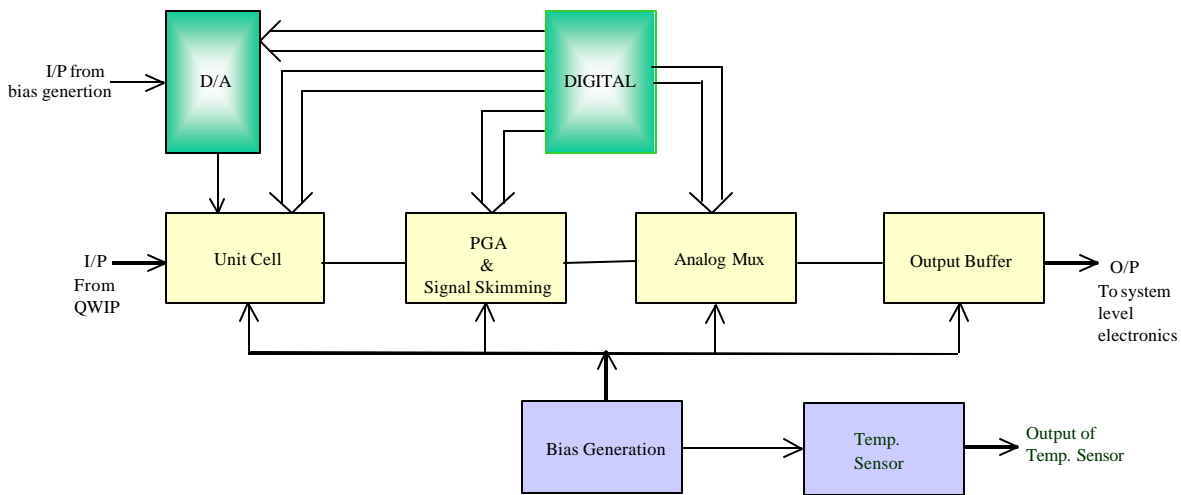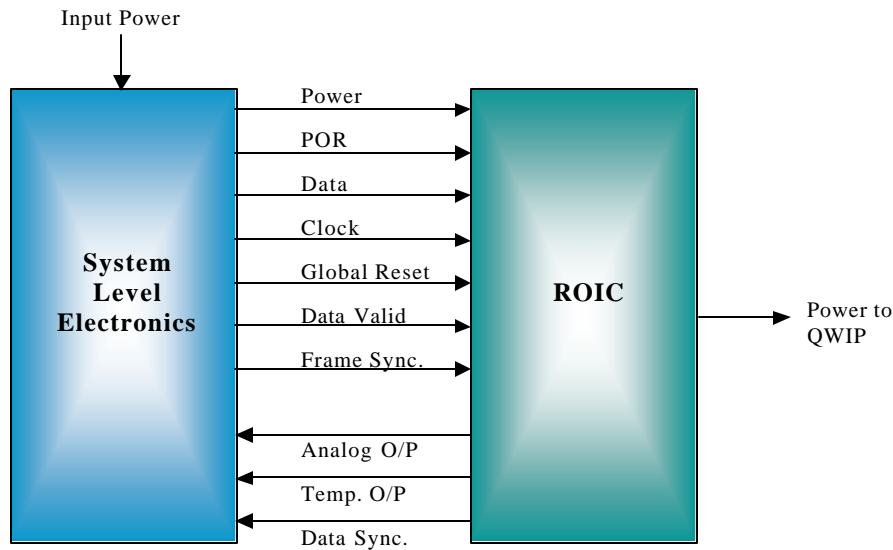
Figure 1

Fig.1 shows the block diagram of SC3981 ROIC. The detector bias is adjustable through Digital-to-Analog converter in SC3981. The unit cell uses three topologies DI, BDI and CMI. The ROIC converts the current from each photodiode to a voltage in each pixel, and multiplexes all the pixel voltages into a serial stream through column level amplifier, multiplexer and output buffer. Each pixel contain circuitry for sample and hold of integrated voltage. The circuitry surrounding the pixel array includes column and row selection and timing control circuitry which directs the output from each unit cell to a column bus and pass through programmable gain amplifier (PGA) to output. A skimming function is also provided here, to globally offset the o/p signal. A differential temperature sensor output is available for monitoring the ROIC substrate temperature

3.0 COMMUNICATION PROTOCOL BETWEEN ROIC AND SYSTEM LEVEL ELECTRONICS

Figure 2: Interfacing Signal Between ROIC and System Level Electronics

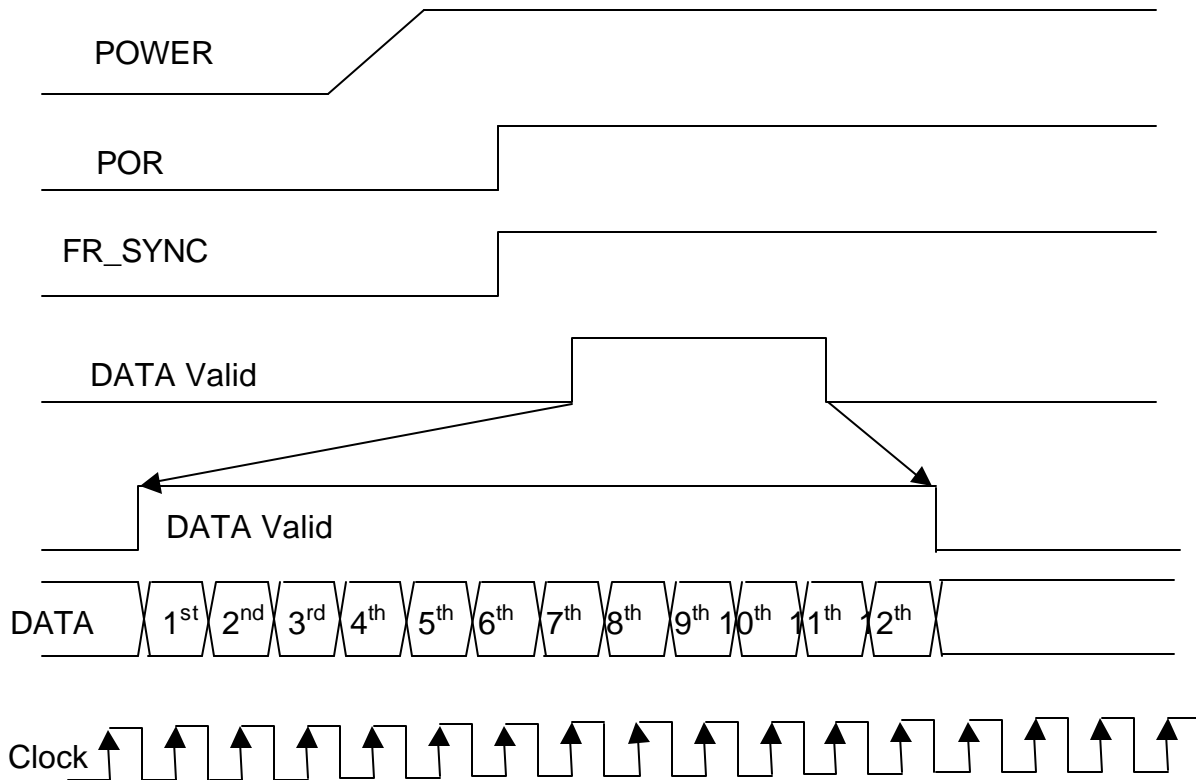Brief description of interfacing signals is given below:

Inputs to ROIC

- Power   :   Power to ROIC is supplied from system level electronics. ROIC in turn supplies power to QWIP.

- POR   :   Power-On-Reset is generated in system level electronics and is sent to ROIC.

- Clock   :   Clock signal of 10MHz with rise/ fall time of < 2ns.

- Global reset :   This signal is given to ROIC to reset the operation of ROIC if needed.

- Data   :   This is 12-bit data given serially to ROIC in 12 clock cycles. Inside the chip this data is loaded in serial control register (SCR).

- Data valid   :   This is the signal which controls the enable time of SCR to take serial input data.

- Frame Sync. :   This is master signal which controls the different integration modes of ROIC as well as frame time.

Outputs from ROIC

- Analog O/P   :   Analog data output from ROIC

- Temp. O/P   :   Temperature sensor output from ROIC (Differential signal)

- Data Sync.   :   Synchronization signal for analog data output, given to system level electronics

POWER

POR

FR_SYNC

DATA Valid

DATA Valid

DATA | 1st | 2nd | 3rd | 4th | 5th | 6th | 7th | 8th | 9th | 10th | 11th | 12th |

Clock

Data Valid, DATA transition occurs at the falling edge of Clock others signals make transition at rising edge of clock.

4.0   Specification and Requirements

ROIC Specification	Specification Requirements	Comments
Array Configuration	8×8	
Pixel Pitch	300μm × 300μm	
Indium Bump Size	200μm × 200μm	Centric to pitch square
Input Polarity	Common terminal of all QWIP detectors in QWIP array going to ground (0V)	
Detector Bias Range	0.4V – 1.0V @ ~50mV resolution	
Detector Resistance (R_{DET})	1.62E09 Ω @ 0.4V 0.75E09 Ω @ 1.0V	

Detector Current
  Dark Current
  Photo Current (This excludes Dark Current)
	170pA @ 0.4V & 1nA @ 1.0V
	170pA – 680nA @ 0.4v
	340pA - 1000nA @ 1.0V	

Input Configuration	DI/ BDI/ CMI	
Multiplexing Configuration	Voltage Mode	
Well Capacity	43 Million e⁻	
Variable Integration Time (Tint)	$>7μs$ – $~T_{frame}$	
Output	Single Output	
Output Load	>500KΩ/ <25pF	Continuous (not- switched) load
Output Voltage Swing	2.1V	(0.6V to 2.7V @ 5V power supply)
Power Supply	5V ±1%	
Skimming Voltage Range	0.9V to 3.5V	Loading of 15pF
Frame Rate	100 Frames/Sec	
Data Rate	10MHz	
Data Settling Time	≤75ns	Settling to 0.1% of final value
Input Clock	10MHz	50% duty cycle
Input Clock Rise and Fall	<2ns	
Control Register Function	Gain select (2-bit) Skimming enable (1-bit) Detector bias adj.(6-bit) Invert/ Revert/ Windowing (3-bit)	
Gain Control	G1 G0 Rel. Gain 0 0 1.0* 0 1 1.33 1 0 2.0 1 1 4.0	* Typical default gain setting
Trans-impedance Non-Linearity	< 0.5%	Max. deviation from straight line fit
Minimum Window Size	4 Columns × 4 Rows	

5.0   Theory of Operation

A general description of the SC 3981 operations is given in this section.

5.1   Unit Cells Circuitry

Within each pixel, photodiode current is integrated for a period of time. At the end of integration time the integrated voltage is sampled and held on the hold capacitor. In prototype SC3981 uses three different topologies DI, BDI, and CMI as unit cell architecture to perform this integration, while sample & hold capacitor is used to store the integrated charge. Each row is sequentially connected to an array of column amplifiers via column buses that are shared by all of the pixels in a column. The outputs of the column amplifies through level shifters are then multiplexed to form the analog output using an analog multiplexer. By varying the sequence of the row and column selections the SC3981 enables such features as windowing, signal skimming, integrate while read and integrate then read operations. In order to begin another integration, the integration capacitor is reset through a switch. When this reset switch opens the new integration begins. The detector bias voltage is varied by Digital to Analog converter & programmed by programmable control resister in ROIC.
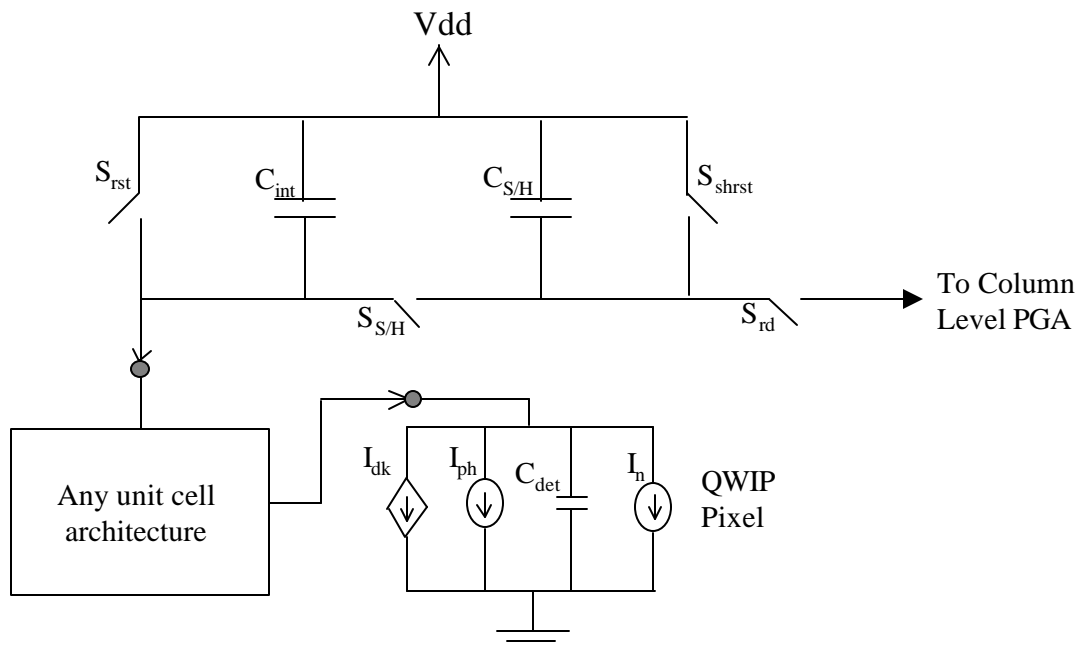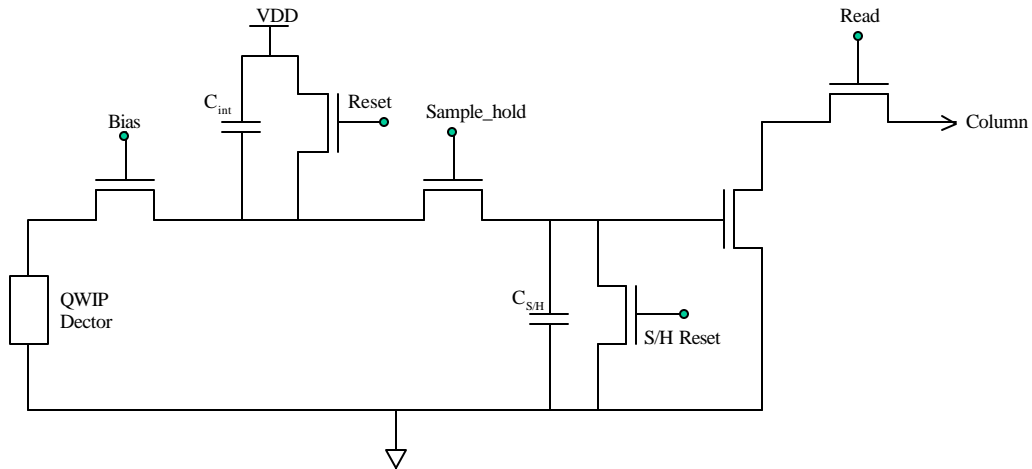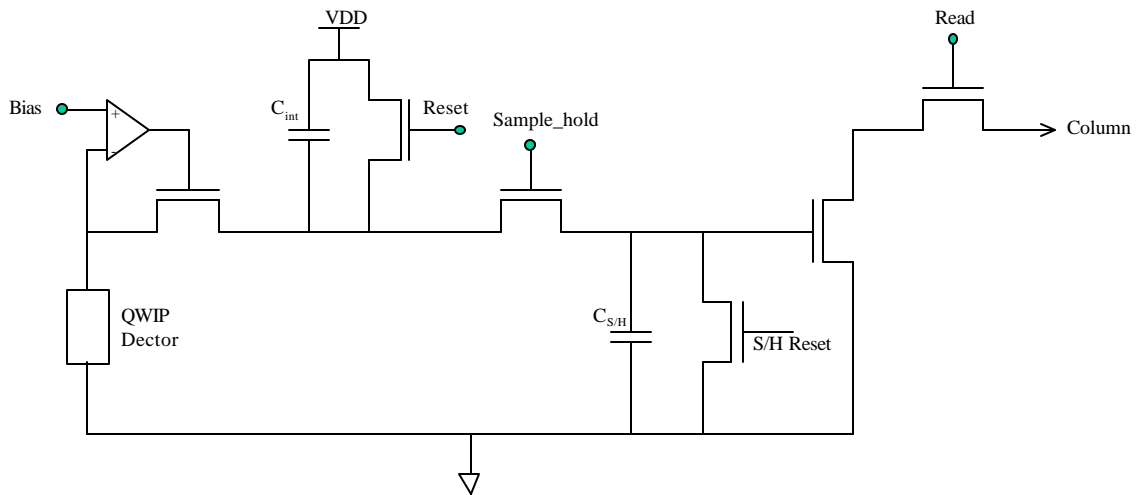

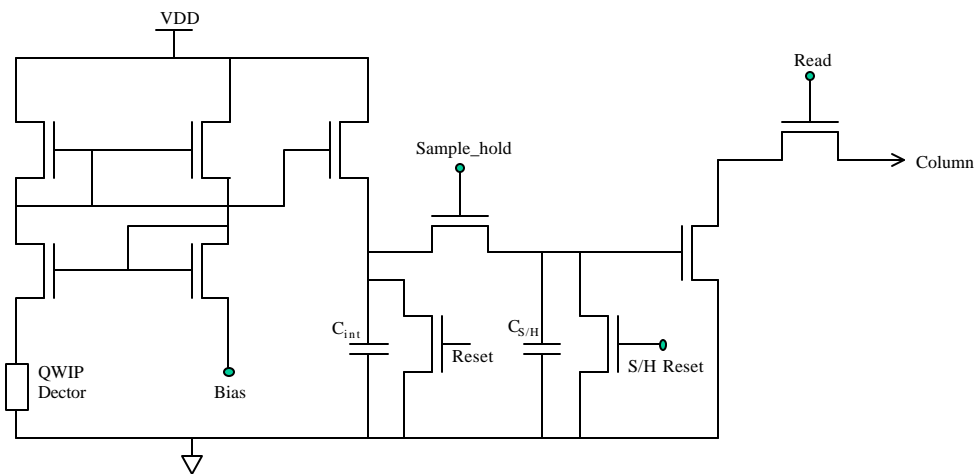**Figure 3 : ROIC Unit Cell ---- General Concept**

Figure 4 : Direct Injection

Figure 5 : Buffered Direct Injection

**Figure 6 : Current Mirroring Integration**

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5.2   Programmable Gain Amplifier

The PGA is used here as column amplifier, it provides amplification and skimming functions. The signal from the unit cell is the input of this block. The four different gains 1, 1.33, 2 & 4 are controlled by the Read 1, Read 2, Read 3, and Read 4 switches. Skimming function is implemented through Dynamic Level Shifter controlled by S1 , S2 & S3 switches . The PGA is also used to drive the output multiplexer.
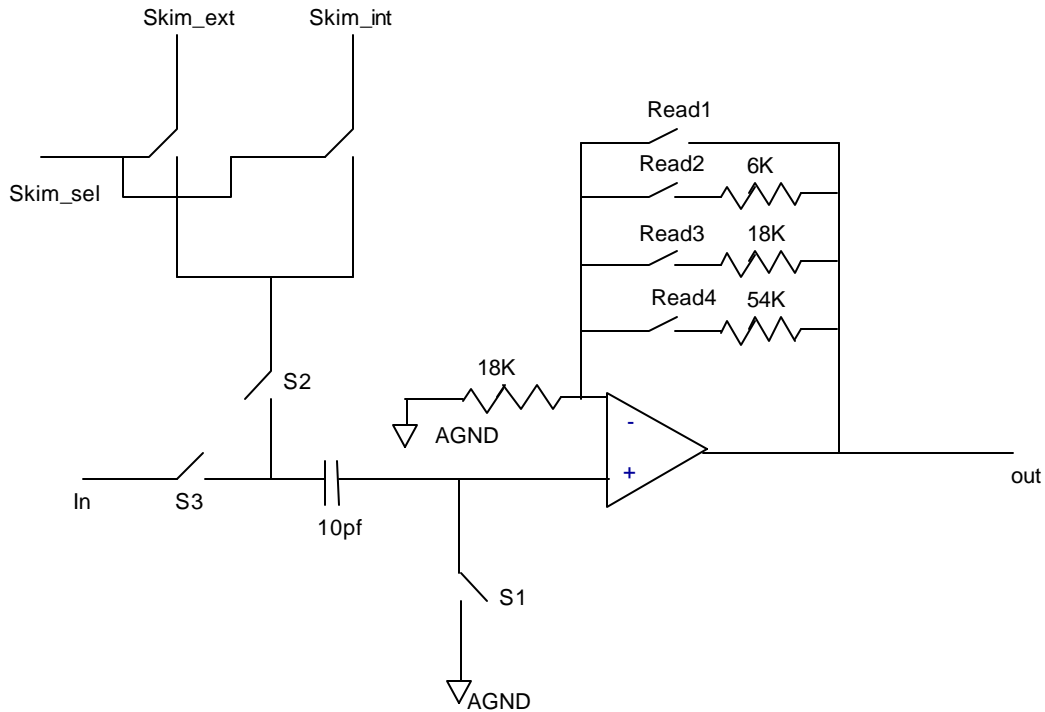
Figure 7 : Programmable Gain Amplifier

5.3 ROIC DIGITAL

This is overall description of digital part of ROIC. Timing and control logic consist of a serial control register storing the user sent control bits, which control the programmability of ROIC.

'W' is the 1st bit sent by the user and 'SKIM' is the last one that is 12th bit.

W	I	R	DB5	DB4	DB3	DB2	DB1	DB0	G1	G0	SKIM

1st bit   **12h bit**

Bits Position in Serial Control Register

Description of bits in serial control registers:

* W $\longrightarrow$ Window

* I $\longrightarrow$ Invert

* R $\longrightarrow$ Revert

* DB5, DB4, DB3, DB2, DB1, DB0 $\longrightarrow$ Detector bias

* G1, G0 $\longrightarrow$ Gain

* SKIM $\longrightarrow$ Signal skimming

Table 1

W	I	R	Different reading options
0	0	0	Full window, non-inverting and non-reverting
0	0	1	Full window, non-inverting and reverting
0	1	0	Full window, inverting and non-reverting
0	1	1	Full window, inverting and reverting
1	0	0	Windowing (1st window)
1	0	1	Windowing (2nd window)
1	1	0	Windowing (3rd window)
1	1	1	Windowing (4th window)

Note: *Invert and revert function is only present in full window case. There is no invert and revert capability in windowing mode.*
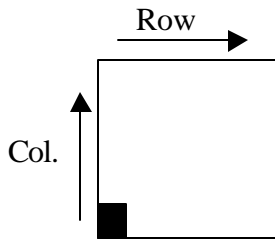
(8, 0)

1st Pixel to be read in full widow invert, non-revert mode

1st Pixel to be read in full widow invert, revert mode

(8, 8)

1st Pixel to be read in full widow non-invert, non-revert mode

1st Pixel to be read in full widow non-invert, revert mode

(0, 0)

(0, 8)
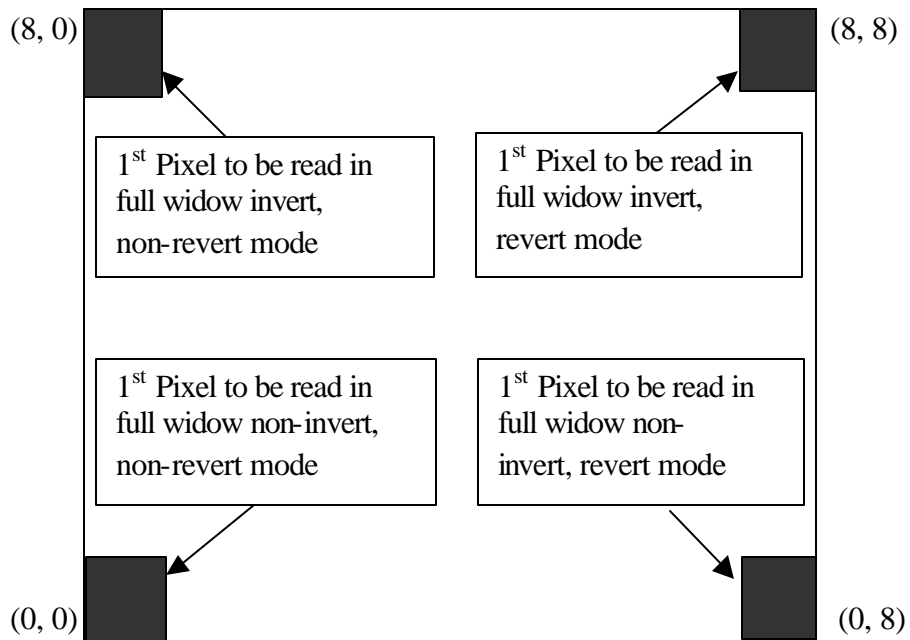
Figure 8

The solid box marks the first pixel to be read in various reading option available in full window case (i.e. reading or 8 ´ 8 = 64 pixel).
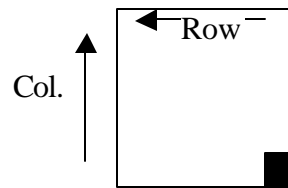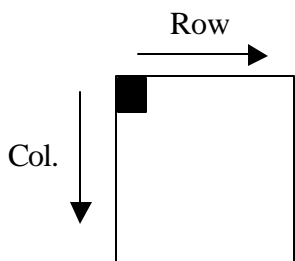
1) For W=0, I=0 and R=0

Row →

Col. ↑

Full window

2) For W=0, I=0 and R=1

← Row

Col. ↑

Full window

3) For W=0, I=1 and R=0

Row →

Col. ↓

4) For W=0, I=1 and R=1

← Row

Col. ↓

5) For W=1, I =1 and R=0

Row →

Col. ↑

3rd

6) For W=1, I =1 and R=1

Row →

Col. ↑

4th

7) For W=1, I=0 and R=0

Row →

Col. ↑

1st

Row →

8) For W=1, I=0 and R=1

Row →

Col. ↑

2nd

Row →
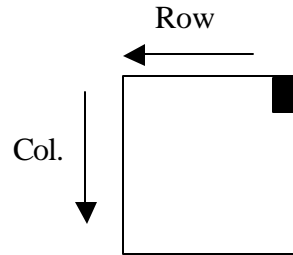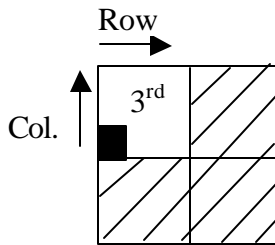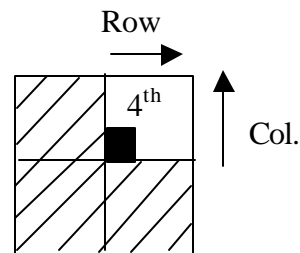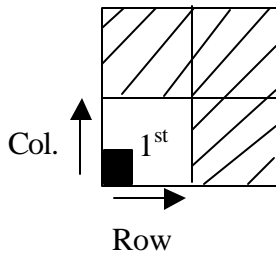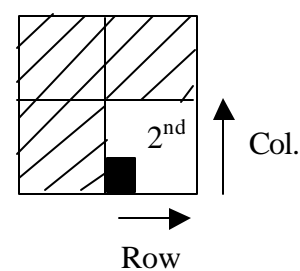
Figure 9 : This figure depicts the eight reading options which are present in Table 1

■ *This solid box marks the first pixel to be read in all the above-depicted eight cases.*
The arrows marked "row" and "column" depicts the direction of reading of array starting from the first pixel.

* G1, G0   ⟶   Analog gain, 2-bit, 4 gain levels

G1	G0
0	0
0	1
1	0
1	1

* SKIM   ⟶   Background subtractions enable
(Signal skimming at column level)

5.4 DIFFERENT INTEGRATION MODES

- INTEGRATE-WHILE-READ
- INTEGRATE-THEN-READ

5.5 READING OF ROIC PIXEL ARRAY

Fig. 10 shows the reading of rows in normal mode (full window, non-inverting & non-reverting). As visible, reading is always happening on row-by-row basis (ripple type).
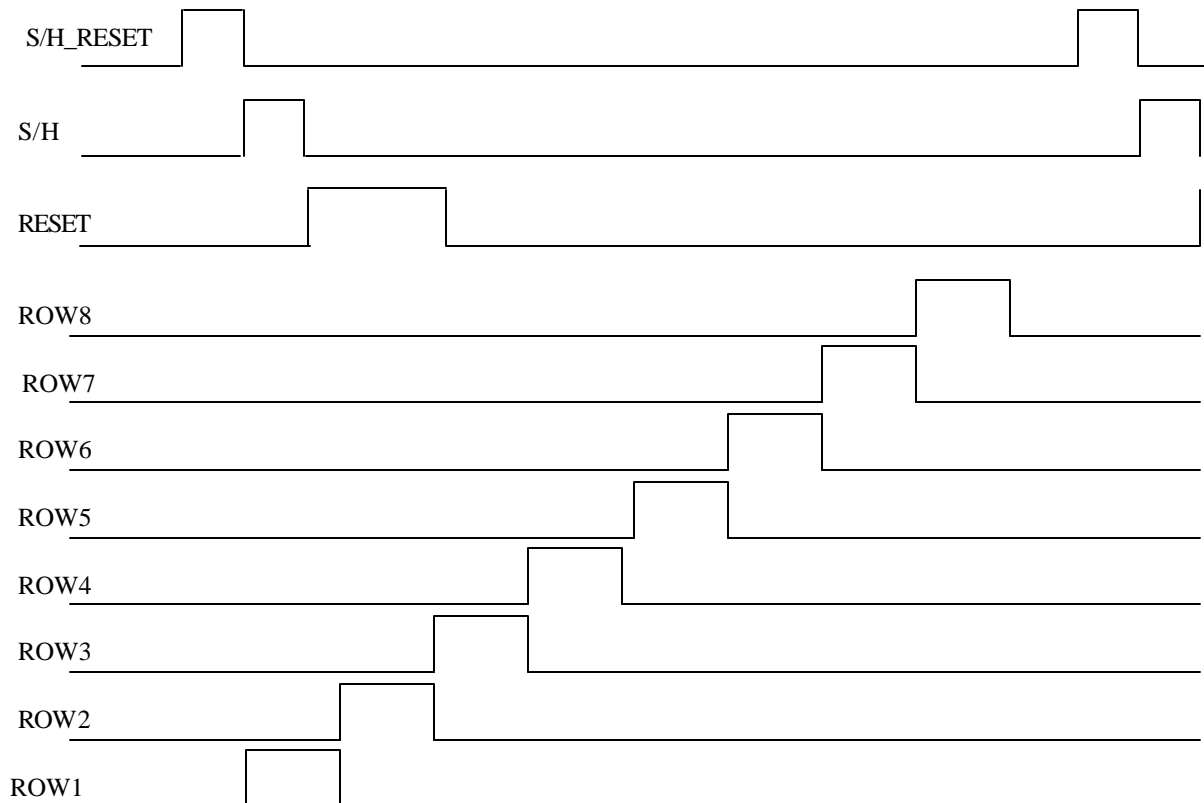

Figure 10

5.6   COLUMN LEVEL ACTIVITY
Fig. 11 shows the reading of columns in a single row in normal mode (Full window, non-inverting & non-reverting)
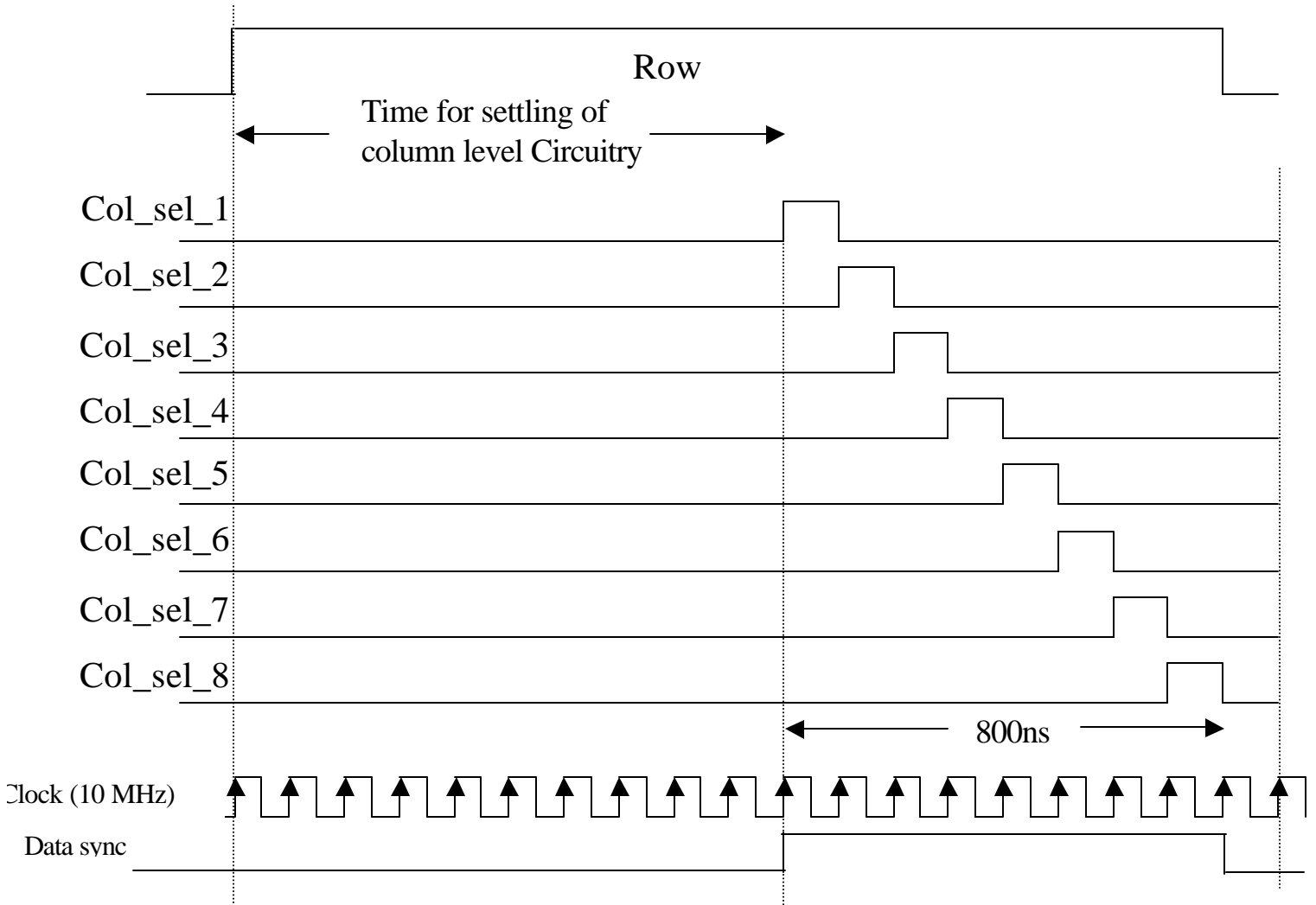

Figure 11

6.0 MODELING APPROACH

Our approach towards modeling the behavior of MOS device at LNT(77K) was based upon the application of temperature scaling rules as we move from 300K to 77K. **This allows us to predict the circuit behavior to first order approximation.** Towards this, In-house measurement at RT (300K) & LNT(77K) was made on fabricated MOS devices with different aspect ratios. The critical parameters of MOS like ---- Threshold voltage, Tran conductance factor, channel length modulations were observed to be used for predictive analysis of circuit.

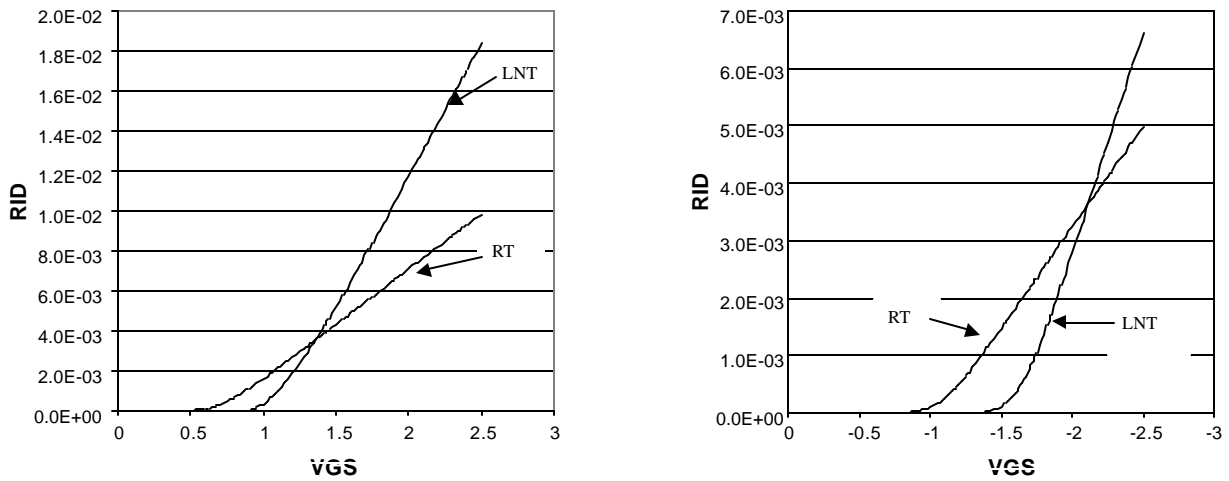### TRANSFER CHARACTERISTIC OF MOS DEVICE AT RT(300K) AND LNT(77K)

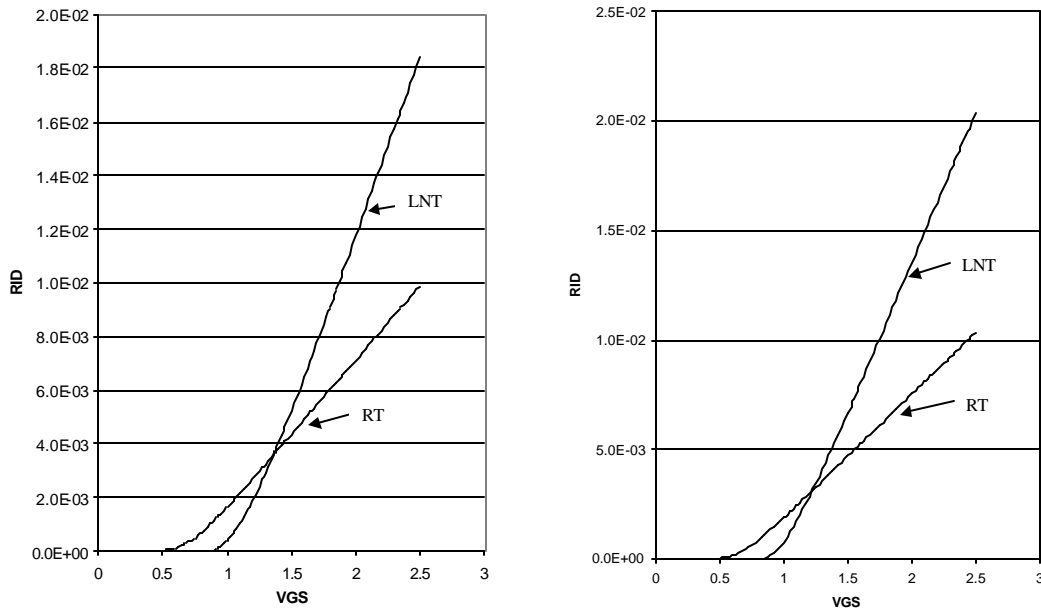**Figure 12 :** $\sqrt{}$ID Vs VGS curve for PMOS

Figure 13 : $\sqrt{}$ID Vs VGS curve for NMOS

7.0 TESTING STRATEGY AND FLOORPLANNING

- Current Splitter circuit to generate current in range of µA to tens-of pA was added in every pixel to inject current into the unit cell architecture (without QWIP).This scheme was adopted in prototype development so as to test the complete ROIC without bonding it with QWIP first, finally after the bonding of QWIP array provision was made to set the current splitter circuit inactive.

- Keeping the future version of ROIC in view a separate die containing smaller pixels of $46\mu m \times 46\mu m$ (without snapshot) was also sent for fabrication.
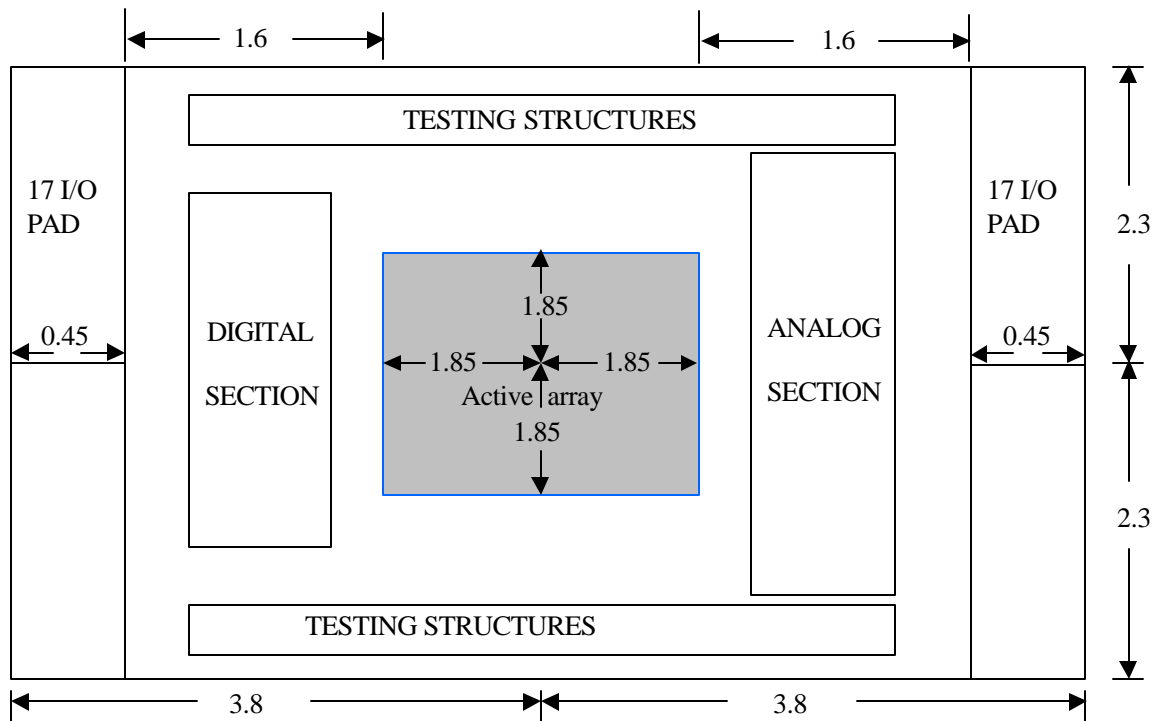
* **All dimension are in mm**

Gray area shows the QWIP die dimensions.
QWIP die attaches with ROIC die by In/Solder bumps.
Spacing between QWIP die to I/O pad in X direction is 1.6mm.

AREA : 7.6 ´ 4.6
(these dimension are without scribe line)

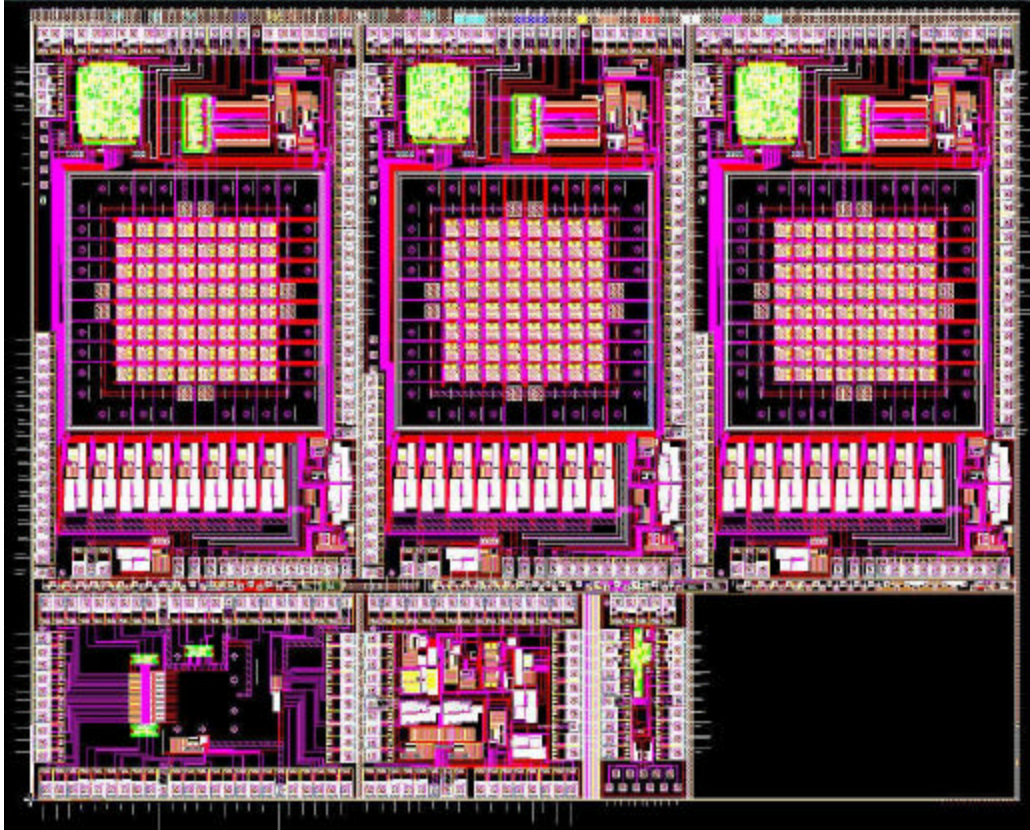**Figure 14: FLOOR PLANNING OF ROIC DIE**

8.0 PG TAPE MATRIX

Figure 15 : ROIC SC3981 PG Tape MATRIX

THE END