The evolution of interconnect technology for silicon integrated circuitry.

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INTRODUCTION

Silicon integrated circuit interconnect technology has evolved rapidly, driven by the continual increase in device functional density. This paper reviews past technology developments and highlights current innovations such as the use of copper metallisation and low k dielectrics to overcome device speed limitations. Areas of convergence between silicon and compound semiconductor interconnect technologies are discussed and future requirements reviewed.

PAST EVOLUTION

Table 1 highlights the major technology milestones in the evolutionary history of silicon interconnect technology.

In the mid 1980's, devices having ~1µm feature sizes were in mass production, these typically having one or two layers of sputtered aluminium alloy metallisation. The relatively deep transistor junctions and wide contacts allowed low leakage, low resistance contacts to be formed using sputtered aluminium. Similarly, vias were generously sized enough for sputtered aluminium to give acceptable step coverage.

TABLE 1
Key interconnect technology innovations and drivers

Technology	Node	Driver
AlSi alloy	1.0µm	Contact reliability (leakage/spiking)
AlSiCu alloy	0.8µm	Line reliability (EM)
TiN /TiW barrier	0.5µm	Contact reliability (Rc; spiking)
W-plug	0.5µm	Scaling – straight sidewalls in contacts & vias (step coverage)
TiN-AlCu-TiN Metal lines	0.5µm	Reliability – hillocks Top ARC provision
Contact silicide	0.35µm	Scaling – junction depth
CMP	0.35µm	MLM lithography Global dielectric planarisation
Cu metallisation	0.18µm	R-C propagation delay
Dual damascene	0.18µm	Lithography – global planarisation Cu RIE process
Zero overlay line-via	0.18µm	scaling
Low k dielectric	0.13µm	R-C propagation delay

Eventually, reliability concerns led to the introduction of 1-2 atomic percent silicon into the aluminium to prevent Al-Si inter-diffusion and resultant junction spiking. Copper was introduced in similar quantities to improve the electro-migration resistance of the aluminium wiring. BPSG was used as pre-metal dielectric with CVD SiO_2 uses as the IMD.

CONTACT METALLISATION

As contact sizes and junction depths decreased, use of AlSi alloys was limited by increased contact resistance caused by silicon precipitation, and by junction leakage. Precipitation occurred during the routine thermal cycling experienced by devices during manufacture. The introduction of sputtered diffusion barriers, typically Ti-W or more commonly TiN, prevented Al-Si inter-diffusion and allowed the formation of stable contacts on to shallow junctions. As junction depths decreased still further, silicide (typically $TiSi_2$) was introduced to maintain low contact resistivity.

VIAS AND INTERCONNECT

Increasing device complexity drove the industry towards multi-level metallisation, which allows increased functionality (transistor connectivity) whilst simultaneously decreasing the average metal line length, the latter having a large influence on interconnect-related RxC (resistance x capacitance) signal propagation delay.

As the number of metal levels increases, the reliability of the via technology used to connect the metal layers together becomes ever more important. Sputtered aluminium vias were used at the 1.0µm technology node but shrinking feature sizes exacerbated the step coverage problems which caused high via resistance. Consequently, CVD tungsten (W) plugs were adopted as the technology of choice for via fill and remain so for advanced, aluminium-based interconnect. Use of CVD W requires the use of a via liner to avoid chemical interaction between the CVD precursor WF_6 and the SiO_2 IMD. Additionally, tungsten in the field regions of the wafer must be removed either by etch-back or, more latterly, by CMP.

As the number of metal levels increases, loss of surface planarisation can cause lithography depth-of-focus problems at the higher metal levels due to cumulative topography effects. Surfaces can be somewhat planarised using etch-back techniques and/or incorporating dielectrics with inherent planarising capability. However, when more than 3 or 4 levels of metallisation are used, the above techniques cannot provide sufficient planarisation and CMP must be adopted. CMP technology enables today's advanced multi-level interconnect architectures, both aluminium and copper based.

The IMD used in aluminium based interconnect schemes must also have good gap filling capabilities, particularly at the lower metal levels where the metallisation has the tightest

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pitches and highest aspect ratios. Gap fill down to 0.1µm can be achieved using CVD processing [1].

TECHNOLOGY DIVERGENCE.

At around the 0.5µm technology node, interconnect technologies become noticeably product specific, with advanced logic devices having significantly greater device functionality and wiring complexity than DRAM products.

By contrast, DRAM metal pitches are tighter to achieve the cost benefits of high memory cell packing density and this demands that the IMD has excellent gap filling capability.

Table 2 summarises key technology parameters for state of the art logic and DRAM interconnect technologies [2] and a clear divergence between logic and DRAM technologies is seen.

TABLE 2
Key 130nm technology node parameters for logic & DRAM.

Parameter	Logic	DRAM
Year of production	2001	2001
No. metal levels	8	3
Local wiring pitch (nm)	350	260
Wiring	Cu	Al
Eff. resistivity (µOhm-cm)	2.2	3.3
Interconnect architecture	damascene	Metal RIE
Eff dielectric constant	3.0 – 3.6	4.1

PROPAGATION DELAY – PERFORMANCE LIMITER

Figure 1 shows the propagation delay plotted against technology node[3]. The major components of the delay are firstly, the resistance and capacitance associated with the transistor junctions (principally CMOS gate delay) and secondly, the resistance and capacitance associated with the interconnect. For technologies down to 0.25µm, the delay component from the transistor gates dominates. Below 0.25µm however,

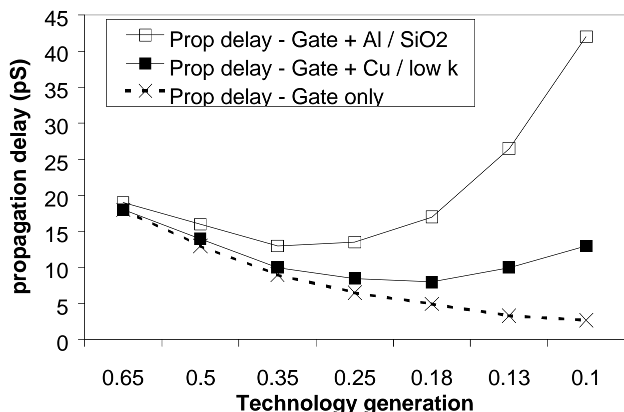

Figure 1: Dependence of propagation delay on technology node

the interconnect-related delay increasingly dominates. This is due to the effects of device scaling which diminish the transistor gate delay whilst amplifying the interconnect related delay. Specifically, tighter metal pitches lead to higher interline capacitance and higher metal sheet resistance.

Unless high frequency device performance is to be adversely affected, the interconnect-related RxC propagation delay must be reduced and consequently chip makers are introducing Cu metallisation instead of aluminium to reduce line resistance, and low dielectric constant (low k) materials to reduce interline capacitance.

The resistivity of copper is nearly 50% less than that of aluminium whilst porous low k materials are available with dielectric constants ~50% lower than that of SiO_2. An additional and important benefit of the use of copper is improved reliability due its higher melting point (1085°C vs 660°C for Al) and so improved electro-migration resistance [4].

INTEGRATION OF Cu .

The introduction of copper metallisation is normally associated with a switch from subtractive metal etch patterning to so called ‘damascene’ patterning. Damascene technology reverses the patterning process such that the via and metal line patterns are first etched in dielectric and then the etched structures are inlaid with copper. When the via and trench are etched and then both filled during the same copper deposition step, this is known as ‘dual damascene’ processing. The principal advantages of damascene patterning for copper based interconnect are

1. Dry etch of copper is replaced with simpler dielectric etch.
2. Copper and dielectric are planarised at the same time, thereby eliminating a CMP step and providing the global planarity needed for multi-level metal processing.

Copper diffuses rapidly in silicon and is also a mid-band gap impurity capable of potentially fatal degradation of device performance. Consequently, tungsten plugs are usually preserved in the contacts to silicon with copper being used in the first level of interconnect and above.

Copper also diffuses rapidly in many dielectric materials and, unlike aluminium, also ionises and drifts in these materials under the influence of electric fields. Such diffusion and drift threaten device reliability through increased dielectric leakage currents and eventually, dielectric breakdown. To prevent this, metallic diffusion barriers, typically refractory metals or their nitrides, are used to line the sidewalls of vias and lines prior to copper deposition. The diffusion barriers have significantly higher resistivities than copper itself and so thin layers must be deposited to avoid an unacceptable increase in the effective resistivity of the metal lines. Typically, barriers are deposited using enhanced PVD or CVD processes to ensure adequate sidewall coverage in dual damascene structures. The vias and lines are then filled with copper by electroplating over a thin PVD copper seed layer. The effective (barrier + copper) resistivity is typically

<2.2µOhm-cm and so is still significantly lower than that of aluminium alloy (~3.3µOhm-cm).

LOW K DIELECTRICS – CANDIDATE MATERIALS AND INTEGRATION

The introduction of low k dielectrics poses a greater integration challenge than the introduction of copper metallisation and this is reflected by the fact that many device manufacturers have chosen to introduce copper before low k.

Candidate low k materials can be categorized by type (silicates, fluorosilicates and organo-silicates, organic polymeric etc.) and by deposition technique (CVD; spin-on).

Dielectric constant reduction is achieved by one or more of the following:

1. Reducing polarizability
2. Reducing density
3. Introducing porosity

To achieve a dielectric constant of below 2.5, significant porosity is needed in the film and this can be achieved by both spin-on [5] and CVD [6] approaches.

Table 3 lists some of the challenges associated with low k integration. The reduction in dielectric constant is usually achieved at the expense of other desirable material properties and this can make integration somewhat more difficult. Low density/porous materials are softer and less thermally conductive than SiO_2 but must still be able to withstand the mechanical stresses applied during CMP and packaging.

TABLE 3
Low k dielectric integration challenges.

Low k property	Impact
Hardness, modulus	CMP, packaging
Thermal conductivity	reliability
Porosity	Etch / strip / barrier deposition
Chemical stability	Etch / strip compatibility
Thermal stability	BEOL process compatibility
Electrical stability	Reliability – leakage & breakdown
Adhesion	reliability

The tightly pitched interconnects used in advanced devices draw high current densities which leads to joule heating. Low k dielectrics have lower thermal conductivity than SiO_2 and so are less able to dissipate the heat generated; a potential reliability problem.

Doped and porous materials can be more difficult to etch and the dual damascene process often necessitates the use of etch-stop and hard-mask layers which can increase the effective dielectric constant of the IMD. Furthermore, it can be difficult to obtain continuous metal barrier coverage over porous sidewalls and any discontinuity in the barrier allows copper to diffuse through.

FUTURE SILICON INTERCONNECT

The introduction of increasingly porous low k dielectrics to reduce interline capacitance will force manufacturers to reduce or eliminate some of the mechanical stresses imposed during CMP and packaging. It is likely that purely chemical planarisation techniques will be introduced and packaging methodologies modified.

As metal lines are scaled to below 100nm, the resistivity begins to rise rapidly due to electron scattering from surfaces. The effect is severe enough to negate the inherent benefits of copper metallisation and so alternatives must be found. Silver exhibits the same scattering effect but the onset occurs at smaller linewidths and so use of silver offers some extendibility. Beyond that, researchers are considering the use of RF wireless and optical interconnect.

CONVERGENCE

There is increasing convergence between silicon and compound semiconductor interconnect technologies. Compound semiconductor manufacturers are using 150mm wafers and beginning to take advantage of the high productivity, single-wafer cluster tooling used in the silicon IC industry. Conversely, silicon RF CMOS and BiCMOS chip manufacturers are now using on-chip passive components (resistors, capacitors and inductors), a practice long familiar to the compound semiconductor industry.

Convergence will inevitably continue and will be accelerated by technological developments such as the ability to deposit defect free compound semiconductor materials on to silicon substrates. Such innovation will allow electronic and opto-electronic circuitry to be integrated on to the same device whilst maintaining the cost benefits associated with large area silicon substrate processing.

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ACRONYMS

BPSG: Boro-Phospho-Silicate-Glass
CVD: Chemical Vapour Deposition
PVD: Physical Vapour Deposition
IMD: Inter-Metal Dielectric
CMP: Chemical Mechanical Planarisation
DRAM: Dynamic Random Access Memory
CMOS: Complimentary Metal Oxide Semiconductor
BiCMOS: Bipolar-CMOS
EM: ElectroMigration
RIE: Reactive Ion Etch

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