Charge Pumps: An Overview

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Abstract- In this paper we review the genesis of charge pump circuits, their evolution and improvement in design and their importance in nonvolatile memory circuits, low-voltage analog building blocks and other applications.

I. INTRODUCTION

Charge pumps are circuits that generate a voltage larger than the supply voltage from which they operate. To see how this is possible, consider the simple circuit consisting of a single capacitor and three switches shown in Fig. 1.

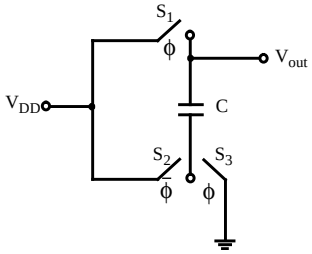

Fig. 1. Simple voltage doubler

During clock phase ϕ, switches S_1 and S_3 are closed and the capacitor is charged to the supply voltage, V_{DD}. Next switch S_2 is closed and the bottom plate of the capacitor assumes a potential V_{DD}, while the capacitor maintains its charge of $V_{DD}C$ from the previous phase. This means that during $\bar{\phi}$

$$(V_{out} - V_{DD}) \cdot C = V_{DD} \cdot C \tag{1}$$

or

$$V_{out} = 2 \cdot V_{DD} \tag{2}$$

Thus, in the absence of a d.c. load, an output voltage has been generated that is twice the supply voltage.

In order to accommodate a load at the output, the circuit would be modified by adding an output capacitance as shown in Fig. 2.

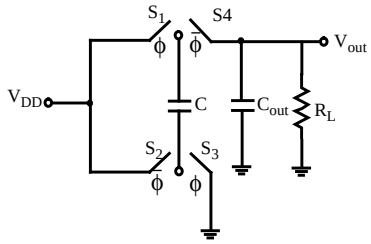

Fig. 2. Practical voltage doubler

In this case, the ideal output voltage is given by

$$V_{out} = \frac{C}{C + C_{out}} \cdot 2 \cdot V_{DD} \tag{3}$$

If a load R_L is present, then a ripple voltage, V_R, is generated at the output. The ripple voltage can be reduced by making C_{out} sufficiently large so that V_R is negligible compared to V_{out}.

Voltage multiplication greater than twice the supply voltage can be achieved by cascading more than one capacitor in series. This voltage multiplier technique seems to have first been proposed by Cockcroft and Walton [1] and was used to generate steady potentials near 800,000 volts in connection with studying the atomic structure of matter. The Cockcroft-Walton multiplying circuit is shown in Fig. 3. Three capacitors, C_A, C_B and C_C, each of capacity C, are connected in series and capacitor C_A is connected to the supply voltage V_{DD}. During phase ϕ capacitor C_1 is connected to C_A and charged to voltage V_{DD}. When the switches change position during

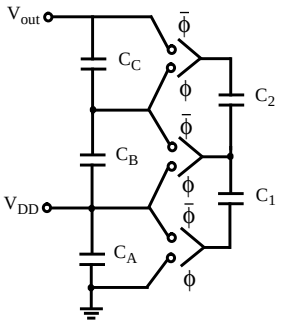

Fig. 3. Cockcroft-Walton voltage multiplier

the next cycle, $\bar{\phi}$, capacitor C_1 will share its charge with capacitor C_B and both will be charged to $V_{DD}/2$ if they have equal capacity. In the next cycle, C_2 and C_B will be connected and share a potential of $V_{DD}/4$ while C_1 is once again charged to V_{DD}. It is thus obvious that if this process continues for a few cycles, charge will be transferred to all the capacitors until a potential of $3V_{DD}$ is developed across the output V_{out}.

The principle is easily capable of extension, and by adding more capacitors, any multiple of the supply voltage, V_{DD}, may be obtained. However, in practice, the Cockcroft-Walton multiplier becomes somewhat inefficient if implemented in monolithic integrated form because of the relatively large on-chip stray capacitance. In addition, the output impedance of the multiplier increases rapidly with the number of multiplying stages.

In order to overcome these limitations, a new voltage multiplier circuit was devised by Dickson [2] that is suitable for integration in monolithic form. It is similar to the Cockcroft-Walton multiplier except this new configuration achieves more efficient multiplication even in the presence of stray capacitance and its drive capability is independent of the number of multiplier stages. Since many CMOS charge pumps are based on the circuit proposed by Dickson, a thorough analysis of this classic multiplier is presented next.

II. DICKSON CHARGE PUMP

The Dickson charge pump [2] is shown in Fig. 4. The circuit consists of two pumping clocks, ϕ and $\bar{\phi}$, which are anti-phase and have a voltage amplitude of V_ϕ. The diodes operate as self-timed switches characterized by a forward bias voltage, V_d. Stray capacitance, C_s, is included at each node for completeness.

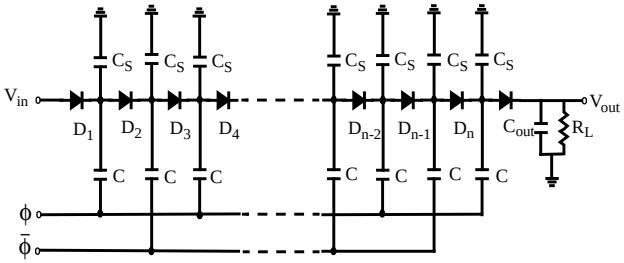

Fig. 4. Dickson charge pump

The multiplier operates by pumping charge along the diode chain as the capacitors are successively charged and discharged during each clock cycle. When clock phase ϕ goes low, diode D_1 conducts until the voltage at node 1 becomes V_{in}-V_d. When ϕ is switched to V_ϕ, the voltage at node 1 now becomes $V_{in} + (V_\phi - V_d)$. This causes diode D_2 to conduct until the voltage at node 2 becomes equal to $V_{in} + (V_\phi - V_d) - V_d$. When ϕ goes low again, the voltage at node 2 becomes $V_{in} + 2 \cdot (V_\phi - V_d)$. After N stages, it is easy to see that the output voltage is

$$V_{out} = V_{in} + N \cdot (V_\phi - V_d) - V_d \tag{4}$$

The stray capacitance, C_s, can be taken into account by noticing that it reduces the transferred clock voltage, V_ϕ, by a factor $\frac{C}{C + C_s}$. Thus, the actual output voltage becomes

$$V_{out} = V_{in} + N \cdot \left(\left(\frac{C}{C + C_s} \right) \cdot V_\phi - V_d \right) - V_d \tag{5}$$

Until now it has been assumed that no load was connected to the output of the charge pump. In the presence of such a load which draws a current, I_{out}, the output voltage is reduced by an amount $\frac{N \cdot I_{out}}{(C + C_s) \cdot f_{osc}}$, where f_{osc} is the operating frequency of the charge pump. The output voltage now becomes

$$V_{out} = V_{in} + N \cdot \left(\frac{C}{C + C_s} \cdot V_\phi - V_d - \frac{I_{out}}{(C + C_s) \cdot f_{osc}} \right) - V_d \tag{6}$$

From this equation it becomes apparent that voltage mul-

tiplication will occur only if

$$\frac{C}{C+C_s}\cdot V_\phi - V_d - \frac{I_{out}}{(C+C_s)\cdot f_{osc}} > 0 \qquad (7)$$

Following Dickson, eq. (6) can be written as

$$V_{out} = V_O - I_{out}\cdot R_S \qquad (8)$$

where

$$V_O = V_{in} - V_d + N\cdot\left(\frac{C}{C+C_s}\cdot V_\phi - V_d\right) \qquad (9)$$

and

$$R_S = \frac{N}{(C+C_s)\cdot f_{osc}} \qquad (10)$$

Equation (6) leads to an equivalent circuit of the charge pump as shown in Fig. 5.

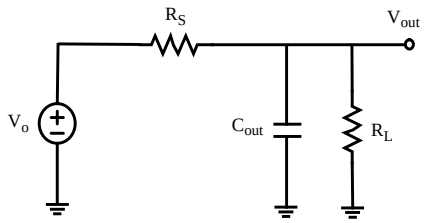

Fig. 5. Equivalent circuit of Dickson charge pump

It should be noted that there will be a small ripple voltage, V_R, at the output due to the load resistance, R_L. This ripple voltage is given by

$$V_R = \frac{I_{out}}{f_{osc}\cdot C_{out}} = \frac{V_{out}}{f_{osc}\cdot R_L\cdot C_{out}} \qquad (11)$$

The ripple voltage can be substantially reduced by increasing the frequency of the clocks or using a large output capacitance. In the latter case, it would take the charge pump significantly longer to reach steady state.

A practical circuit implementation of the Dickson charge pump in CMOS technology is shown in Fig. 6. The multiplier chain is implemented using diode-connected NMOS transistors. Here the diode forward voltage, V_d, is replaced by the MOS threshold voltage, V_{tn},

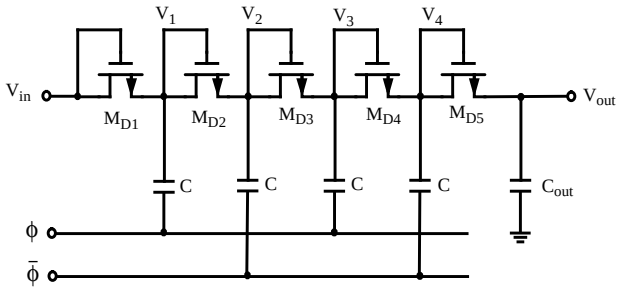

Fig. 6. A four-stage Dickson charge pump

and the output voltage is given by

$$V_{out} = V_{in} + N\cdot\left(\frac{C}{C+C_s}\cdot V_\phi - V_{tn} - \frac{I_{out}}{(C+C_s)\cdot f_{osc}}\right) - V_{tn} \qquad (12)$$

where in this particular case N=4. We now define a useful quantity called the voltage fluctuation at each pumping node, ΔV. This is the voltage change that occurs at each node of a charge pump from one clock cycle to the next. This is illustrated for the four-stage Dickson charge pump in Fig. 7.

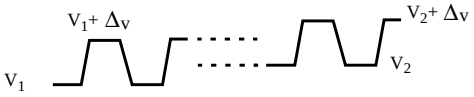

Fig. 7. Voltage fluctuation

For the Dickson charge pump, the voltage fluctuation can be expressed as

$$\Delta V = \frac{C}{C+C_s}\cdot V_\phi - \frac{I_{out}}{(C+C_s)\cdot f_{osc}} \qquad (13)$$

We may also define the voltage pumping gain, G_V, of a charge pump as

$$G_V = V_N - V_{N-1} \qquad (14)$$

For the Dickson charge pump we have

$$G_V = \Delta V - V_{tn} \qquad (15)$$

From eq. (14) and eq. (15) we see that the necessary condition for voltage multiplication is given by

$$(G_V = \Delta V - V_{tn}) > 0 \tag{16}$$

Unfortunately, as the supply voltage decreases, V_ϕ decreases and according to eq. (13) so does ΔV. Consequently, the pumping gain (eq. (15)) is also reduced. It is thus obvious that the Dickson charge pump is not at all suitable for low-voltage operation. If the threshold voltage term, V_{tn}, could somehow be eliminated from eq. (15), the Dickson charge pump would be usable at low-voltages, offer a better voltage pumping gain and a higher output voltage. This can be accomplished by modifying the Dickson charge pump so that it utilizes static charge transfer switches (CTS's). The details are presented next.

III. STATIC CTS CHARGE PUMPS

Static CTS charge pumps are new charge pumps employing dynamic switches to increase the voltage pumping gain. The basic idea behind these multipliers is to use MOS switches with precise on/off characteristics to direct charge flow during pumping rather than using diodes, or diode connected transistors which inevitably introduce a forward voltage drop at each node. One of the first low-voltage CTS based charge pumps with static backward control was presented in Wu [3]. The circuit details of this new charge pump (NCP-1) are shown in Fig. 8.

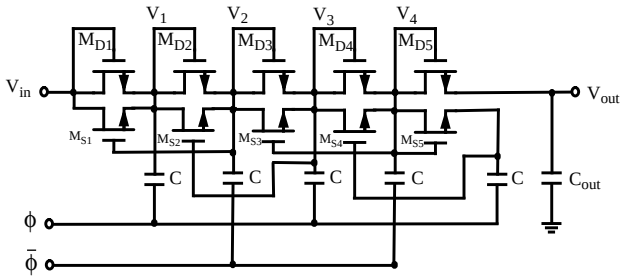

Fig. 8. A four-stage CTS based charge pump

Neglecting for the moment the CTS transistors M_{S1}-M_{S5}, the operation of this new charge pump is identical to the operation of the Dickson charge pump and the same initial voltages will be established at each pumping node. The idea behind the CTS switches is to use the already established high voltages at the various nodes to control the CTS of the previous stage. This will work if the switches can be turned on / off at the designated times such that they allow charge to be transferred in only one direction. When this is the case for each pumping stage, the input upper voltage of each node is equal to the output lower voltage as can be seen in Fig. 9.

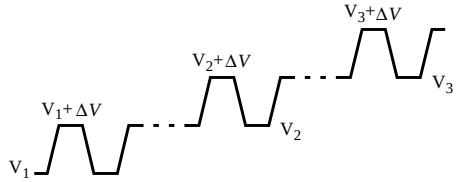

Fig. 9. CTS based charge pump voltage fluctuation

The voltage pumping gain of this charge pump now becomes

$$G_V = V_2 - V_1 = \Delta V \tag{17}$$

Compared with the Dickson charge pump, eq. (15), the NCP-1 proposed by Wu has a much better charge pumping performance since the V_{tn} term has been eliminated from eq. (17).

When clock phase ϕ is high in Fig. 8, the voltages at nodes 1 and 2 are equal, while the voltage at node 3 is $2 \cdot \Delta V$ above those at nodes 1 and 2. This means that the gate-to-source voltage of M_{S2} is $2 \cdot \Delta V$. In order for this transistor to be on, we require

$$2 \cdot \Delta V > V_{tn} \tag{18}$$

Comparing this with eq. (16) we see that the NCP-1 charge pump presented by Wu is much more suitable for low-voltage operation than the Dickson charge pump.

Unfortunately, there is one minor problem with this circuit configuration, namely, charge leakage in the reverse direction. When clock phase ϕ is low, the voltage at nodes 2 and 3 is equal and $2 \cdot \Delta V$ above the voltage at node 1. Thus, the gate-to-source voltage of M_{S2} is $2 \cdot \Delta V$. During this clock phase, we ideally require M_{S2} to be turned off. This will only be the case if

$$2 \cdot \Delta V < V_{tn} \tag{19}$$

Since eq. (18) is always satisfied, it is impossible for the requirement of eq. (19) to be met. Therefore, switch M_{S2} will not be completely turned off and reverse charge shar-

ing will occur between node 2 and node 1.

This reverse charge leakage phenomenon can be eliminated by adding pass transistors (both NMOS and PMOS) to the NCP-1 circuit. The function of these transistors is to apply dynamic control to the CTS's in order to turn them off completely when required and still be able to turn them on easily by the backward control voltage as in the NCP-1 case. The details of this so called NCP-2 charge pump are presented in [3]. It can be shown that the necessary conditions for the NCP-2 charge pump to operate properly are

$$2 \cdot \Delta V > V_{tp} \tag{20}$$

and

$$2 \cdot \Delta V > V_{tn} \tag{21}$$

Unlike the NCP-1, these conditions can be satisfied simultaneously and the resulting charge pump offers excellent performance.

IV. ADVANCED CHARGE PUMP TECHNIQUES

Another class of charge pump designs suitable for high-performance, low-voltage operation are those based on switched-capacitor techniques [4]. A high efficiency CMOS voltage doubler with good accuracy is presented in [5]. This design is simple and power efficient, and with a few modifications represents the current, state of the art in charge pump design.

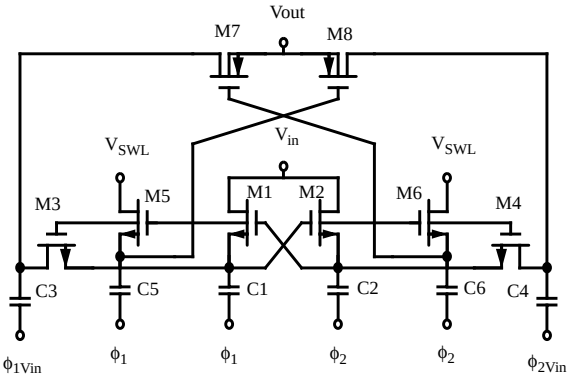

Fig. 10. Modern voltage doubler

A novel, state of the art, high efficiency voltage doubler suitable for low-voltage / low-power applications has been developed by Phang [6] and is presented in Fig. 10. In order to understand the operation of this multiplier, it is helpful to consider the basic charge pump cell [7] shown in Fig. 11.

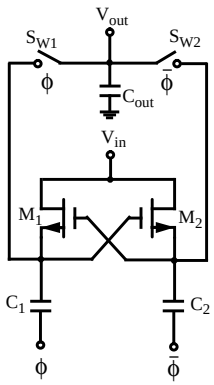

Fig. 11. Basic charge pump cell

The cell uses two non-overlapping, antiphase clocks of amplitude V_{DD}. Transistors M_1 and M_2 are successively switched on and off in order to charge capacitors C_1 and C_2 to the voltage V_{in}. After a few clock cycles, the clock signals on the top plates of the capacitors will assume an amplitude of $V_{in} + V_{DD}$. The switches S_{W1} and S_{W2} are timed so that V_{out} only sees this voltage. If $V_{in} = V_{DD}$ then

$$V_{out} = 2 \cdot V_{DD} \tag{22}$$

and the output is double the supply voltage.

Referring to Fig. 10, we see that the voltage multiplier consists of three closely-coupled charge pump cells. The middle cell comprised of M_1 and M_2 is used to generate a level-shifted clock signal as described in Fig. 11. This level-shifted clock signal is used to turn on the outermost charge pump consisting of devices M_3 and M_4 and pass the input voltage, V_{in}, to the top plates of capacitors C_3 and C_4. The clock signals driving capacitors C_3 and C_4, namely Φ_{1Vin} and Φ_{2Vin} have a reduced voltage swing that is equal to the input voltage, V_{in}. Thus, after a few clock cycles, the voltage at the top plates of C_3 and C_4 fluctuates between V_{in} and $2 \cdot V_{in}$. The last charge pump uses devices M_5 and M_6 to drive the PMOS output

switches M_7 and M_8. It is worth noticing that the design includes a desirable innovation, namely, the low level clock swing has been shifted to V_{SWL} which has been optimized for driving the PMOS output switches. This improves the output resistance of the switches. The full-swing clock signals Φ_1 and Φ_2 were generated from an integrated, non-overlapping, two phase clock generator [8] that is shown in Fig. 12.

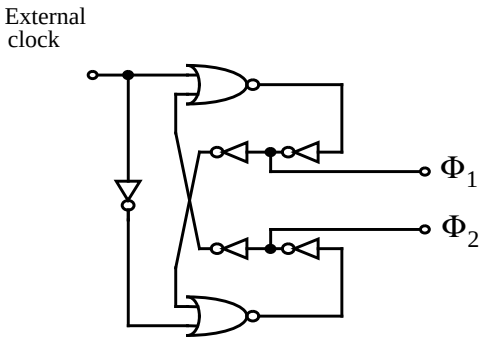

Fig. 12. Non-overlapping clock generator

The performance of Phang's voltage multiplier circuit was simulated and shown in Fig. 13. The simulation used an input voltage of 1.5V and a small output load capacitance of 1.0 pF to speed up the transient response. The circuit exhibited hardly any undershoot and reached steady state quickly due to the reduced switch resistance afforded by the dedicated charge pump driving the output switches.

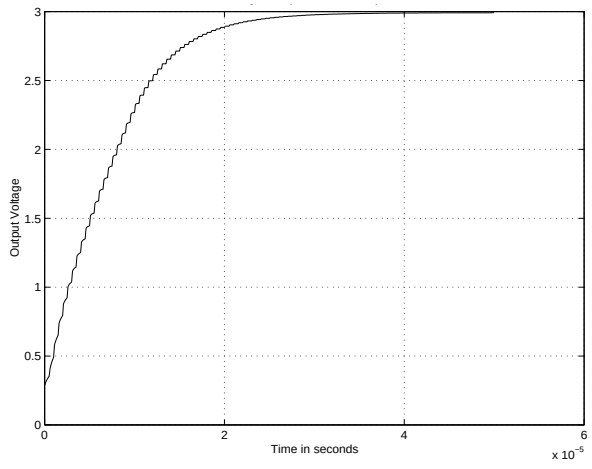

Fig. 13. Simulation of step-up response for voltage doubler

V. APPLICATIONS AND FUTURE CHALLENGES

The most obvious application of charge pump circuits is in the programming of EPROM circuits. Until recently, most EPROMs used hot-electron injection [9] to program these devices and required off-chip supply voltages. This method of programming required large drain currents during device flashing and required a dedicated, non-standard power supply. An alternative method of programming EPROMs is based on tunneling by Fowler-Nordheim field emission. For programming, a large voltage (around 10-15V) is applied to the control gate of the device and charge is transferred to the floating gate. The advantage with using this method lies in the fact that no drain current is required for programming. Hence, on-chip charge pumps can be used to generate the higher than normal voltages required to write or erase information in nonvolatile memory circuits [10].

Recently, charge pumps and voltage multipliers have been applied to low-voltage / low-power analog integrated circuits with some success. A technique known as 'Dynamic Gate Biasing' has been pioneered by Phang[7] and others in a diverse range of applications. In Dynamic Gate Biasing (DGB), controllable charge pump circuits are used for the stable biasing of MOSFET gates. These transistors are biased in the triode region and act as variable resistors. On-chip DGB has shown to be feasible in the design of a low-voltage, CMOS front-end optical preamplifier[6] and in low-voltage, continuous-time, biquadratic filter applications [11][12].

In the future, as analog designers look for new ways to meet the challenge of reduced supply voltages, on-chip charge pumps and voltage multipliers are destined to become an integral part of low-voltage analog and digital circuit designs.

VI. REFERENCES

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