Thermal Management in High-Density Power Converters

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Abstract - This paper gives an overview of basic principles of the thermal management in high density power converters. Methods for heat removal on a device and circuit board level are discussed. New packaging technologies for discrete power semiconductors as well as multifunctional board integration techniques are included. A view is given on future 3D integration techniques that take into account the poor thermal conductivity especially of the passive component materials. With these techniques much higher power densities are possible. Some examples of prototype systems are presented, together with the achieved technical data.

1. Introduction

Miniaturization in power electronics is mainly driven by applications with severe size restrictions like in automotive, robotics and telecommunication, but also by comfort requirements – see e.g. portable equipment (notebook line adapter, charger, etc.). Point-of-load DC/DC converters are used in distributed power supply structures and provide the operating voltage for microprocessors and complex logic devices. Today these converters - completely realized in SMD technology on standard printed circuit boards – can control currents of more than 100A, while fulfilling extreme demands on the transient response. High-power, high-density DC/DC converters will play a central role also in future cars, e.g. for replacing the alternator or coupling ultra-capacitors and fuel-cells to the powernet.

With the increasing power densities, the thermal management becomes more and more a central issue in system engineering. The basic target of thermal management is to ensure safe thermal operating conditions for »all« system components (s. fig.1). This means not only the active and passive components, but e.g. also the circuit board, the interconnections, etc. In consideration of the individual system requirements on lifetime, reliability and safety, this goes far beyond a simple check on compliance with the maximum rating conditions of each component. Special attention has to be paid to lifetime data and useful life deratings, which in general are not only dependent on the absolute temperature but also on the temperature-cycling during operation.

Thermal management starts at the device level, e.g. with the »simple« choice between a package version with or without a heat-slug for a SMT device. Such a small technical decision can basically determine the thermal behavior and reliability of the whole system just as many other decisions do on the board and system level. Each decision must take into account the operating and environmental conditions specified for the final system. Even things which at a first glance have nothing to do with

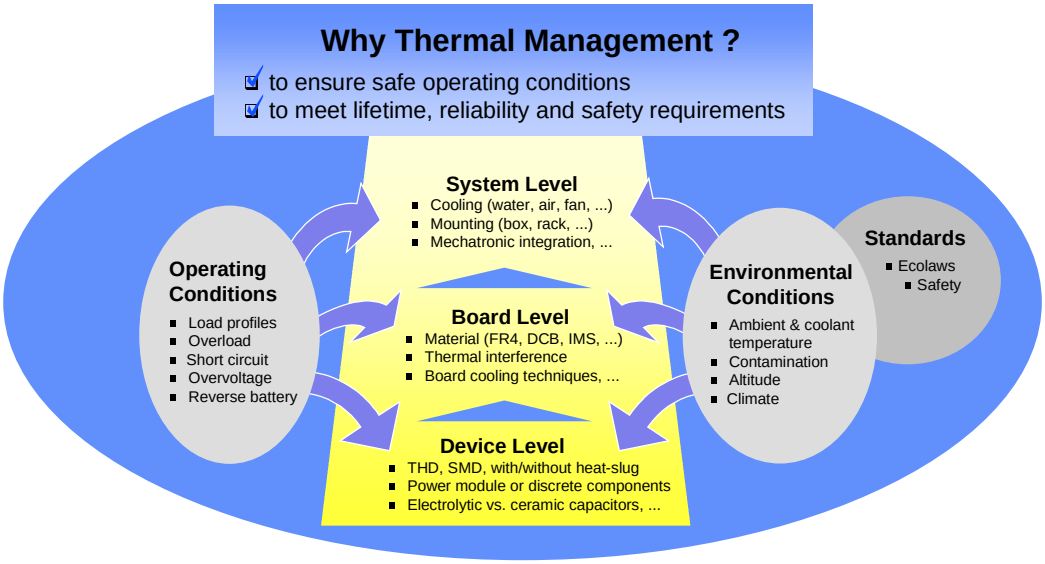


Fig. 1: Thermal management - a continuous process during system engineering.

thermal management can have their impact here, e.g. waste or recycling regulations which aim at a better material separability, reduction of encapsulation materials or ban of certain materials.

Because of the far-reaching consequences of many decisions and the high cost risks of a redesign, it is important that the thermal management is not considered as a separate work-package within a design flow but as a continuous process accompanying the whole system development. This becomes more and more important with the continuously increasing power densities of modern power electronic systems.

2. Thermal Management on a Board Level

Fig. 2 shows the traditional way to realize power electronic systems. This technique is still the most widespread for low-cost applications, e.g. PC power supplies. Discrete semiconductor components are used and individually mounted on heatsinks. SMT and through hole devices (THD) are mixed. Large discrete passive components are used for filter, d.c. link capacitors and transformer. All these components have completely different shapes and nonuniform heights, which results in very large dead volumes and basically limits the achievable power density. The weight and mechanical design of the heatsinks and of the passive components makes them susceptible to shocks and vibrations, a problem if one thinks about a mechatronic integration into automotive systems, robotics or drives. And not least, from a thermal management point of view one must unfortunately state that nearly none of the conventional passive devices has been designed for the purpose of effective cooling. Nevertheless, this traditional technology is mature and allows very low-cost solutions without large investments in highly automated production lines and is therefore still competitive for very low power density applications - at least as long as extreme inexpensive human labour is available anywhere in the world.

A first important step towards less manual work, fully automated production and higher power densities is possible by consistently using modern mounting techniques. Basically there are many different techniques available for the integration of power semiconductors, sensors and control electronics. The most important ones are:

- monolithic integration
- hybrid integration on ceramic substrates
- DCB/DAB technique (Direct Copper/Aluminum Bonded ceramic substrates)
- leadframe technique (e.g. in combination with ceramic substrates and molded packages)
- IMS (insulated metal substrate, metal core boards)
- printed circuit board (PCB)

Fig. 2: Traditional appearance of power electronics

In the low-voltage, low-power range the monolithic integration is well established, e.g. in form of the widespread Smart-Power switches. However, this approach with increasing operating voltage and currents quickly comes to its economic limits, because of the large difference in complexity and costs per chip area of modern semiconductor processes for power and logic devices.

Considering the mounting techniques for discrete components, the hybrid and DCB technologies can realize the best thermal performance with substrate materials like Al_2O_3 or AlN ceramic, but also show the highest costs per substrate area. Common to leadframe, DCB and IMS technology is the generally single-layer copper structure which makes it very difficult to route more complex circuits and greatly limits the package density. The comparatively coarse trace widths in DCB and partially in the leadframe technology also limit the integration of more complex signal electronics. On the other hand the thick copper traces (>0.3mm) which can be realized in DCB technology easily allow to control high currents in the range of several hundred amperes.

The printed circuit board technique is based on the worst heat-conducting substrate material. This approach nevertheless has the charm to open up the great potential of a modern, very innovative, and very high production volume technology, which by far outperforms the competitive techniques with respect to integration density, flexibility and costs per substrate area. The base material is typically an epoxy laminated cotton paper or woven fiberglass. Different material grades like CEM-1 to 4 or FR-2 to 6 are offered which mainly differ in laminate construction, flame retardant content and glass transition temperature [1]. In the following, the potential of printed circuit board (PCB) technology in power electronics will be shown at a few examples:

Look at a discrete power semiconductor device, which is not screwed to a heatsink as shown in fig. 2, but directly soldered on a PCB in SMD manner with about $6cm^2$ ($1in^2$) copper area around the device (e.g. TO-263). With free natural convection and vertical mounting of the board this results in a thermal resistance from chip to ambient of about 40K/W. At a maximum allowable board temperature of 125°C and an ambient temperature of 60°C, a power of about 1.5W can be dissipated – a comparatively low value in view of the quite large board area consumption. However, by glueing the board on a heatsink as shown in fig. 3 the thermal resistance can be greatly improved - despite the bad thermal conductivity of the board material. In this case

the thermal resistance drops below 40 K/W already with the area of the minimum recommended footprint of a TO-263 package (approx. 1 cm^2) so that no board space is lost.

Under the assumption of a one-dimensional heat flow, the thermal resistance (R_{th}) of a piece of material is generally given by

$$R_{th} = \frac{d}{\lambda A} \qquad (1)$$

where d is the length of the heat path (here e.g. the board thickness), A the heat conducting area and λ the thermal conductivity of the material. This very simple equation directly leads to a basic rule of thermal management: »A low thermal resistance can be realized even through materials of bad thermal conductivity by increasing the heat-conducting area and/or reducing the heat path length.«

The diagram in fig. 3 shows the behaviour of the thermal resistance between case and heatsink when we apply this rule to our example and increase the size of the device footprint by the length x all around. The increasing copper area on the top-side acts as a heat-spreader and increases the heat conducting area through the board. The heat flux density in the board material is reduced by this. An enlargement of the footprint of only 6mm around the device reduces the thermal resistance through the board down to 10 K/W. This is a 400% improvement compared to our starting point and allows a power dissipation of typically 6W per device, which is already sufficient for many applications. Due to the lateral thermal resistance, i.e. the resistance in the plane of the copper, there is a maximum

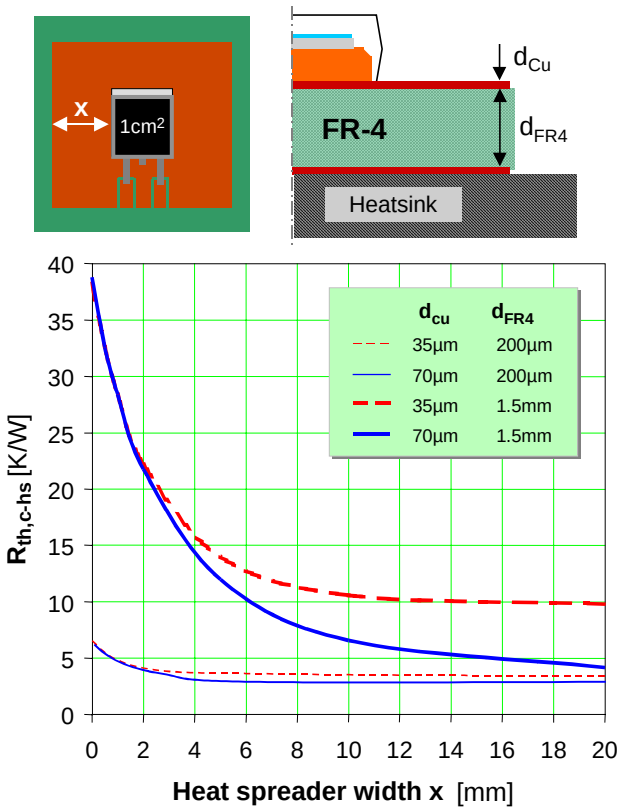
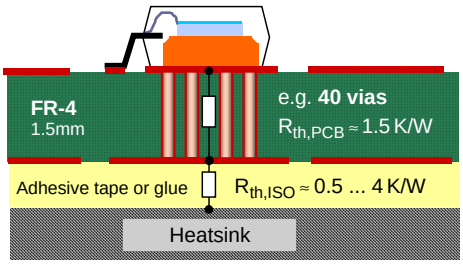


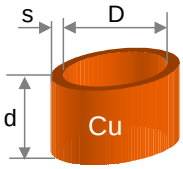
Fig. 3: Thermal resistance through a PCB as a function of heat spreading copper area around a device pad (TO-263)

useful width for any heat-spreader. This width and with that the effectiveness of the heat-spreading considerably increases with the copper thickness as can be seen in the diagram in fig.3.

A further substantial reduction in the thermal resistance of a PCB is possible by the application of electrical vias which today are used in any medium and high density board. In principle each via is a copper sleeve through the board or through a part of the board (blind or buried via). Beside or instead of using its electrical function a via can also be used as a »thermal short«. With the simple thermal model given in fig. 4 and the typical dimensions of a via (e.g. D = 0.7mm, s = 35µm, d = 1.5mm) one gets about 60K/W for the thermal resistance of a single via. Thus a field of 5x8 vias, which e.g. can be easily placed below a TO-263 package, reduces the thermal resistance through the board on 1,5K/W (= 60K/W / 40). Using thicker copper or filling the vias (e.g. with solder) can further improve the thermal conductivity. The main disadvantage of standard



Model of a thermal via:



$$R_{th,via} \approx \frac{d}{\lambda_{cu} D \pi s} \qquad (2)$$

$R_{th,via} \approx 60K/W$ (typ.)

Fig. 4: Thermal vias

thermal vias is the loss of the electrical insulation. Since the backside of most power semiconductors and with that the heat-slug of most discrete power devices is on a high potential, an electrical insulation is generally necessary between the board and the heatsink. Today the insulating glued joint is realized either with special double-sided adhesive tapes (e.g. 9892FR from 3M™) or by using a glue, which contains a small amount of glass balls with a well-defined diameter. The balls ensure a well-defined thickness of the glue layer and with that reproduceable thermal and electrical insulation properties. Thermally enhanced glues, filled e.g. with ceramic powder, are also available.

Depending on the glue material and glue layer thickness, a total thermal resistance between the case of a power device and the heatsink in the range of 3...6K/W (referring to the size of a TO-263) can be achieved by applying thermal vias through the board (s. fig.4).

The next step towards a higher board integration is shown in fig. 5. This approach is based on the fact that today in many power electronic systems the integration density in the signal and control electronics parts has reached a level (µC, FPGA, etc.) that requires multilayer boards. The integration of the power electronics parts on the same board does not only cause the cancellation of interconnection elements but also allows new dimensions of a multifunctional board integration.

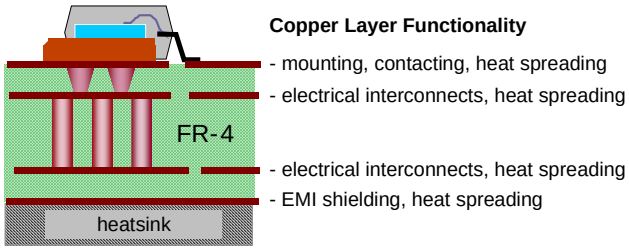


Fig. 5: Multifunctional board integration

By using an intelligent arrangement of blind and buried vias, it is possible e.g. to shift the electrical insulation into the board as shown in fig. 5. A wide spectrum of default prepreg thicknesses allows an individual optimization of the board structure with respect to dielectric strength and thermal conductivity. Even high standards on the insulation quality and safety can be fulfilled with multiple-ply pregregs. The board internal insulation allows the insertion of one or several EMI shielding layers. With that the noise current loops can be closed within the board and no common mode noise is coupled into the heatsink anymore, making EMI filtering considerably easier. Current densities in the copper traces in excess of 60A/mm^2 are possible as a result of the effective cooling. In conjunction with a 75µm, 105µm or thicker copper layer, currents of several hundred amps can be controlled in PCB technology this way. This all results in a lot of benefits of a multilayer PCB integration of power electronics. The most important ones are:

- SMT compatible assembly process (no screws, spring-clips, insulating bushings, etc.)
- integrable heat path with electrical insulation from heatsink
- integrable EMI shields and low-noise ground planes
- high package density due to multilayer routing
- integrable windings for planar magnetics
- cancellation of interconnects between power and signal electronics

Taking all these facts into account, the additional costs for a multilayer board are quite fast balanced by system cost savings.

Fig. 6 shows the power stage of a line-fed 750W drive inverter for an induction motor with the six IGBTs, the line input bridge rectifier, the shunt resistor for current sensing and the HV SMPS-IC for the auxiliary supply. The board is realized in a four-layer structure according to fig. 5, with the insulating prepreg layer made of three 62µm thick plies. The partial discharge quenching voltage of this structure is above 1000V between d.c. link and heatsink.

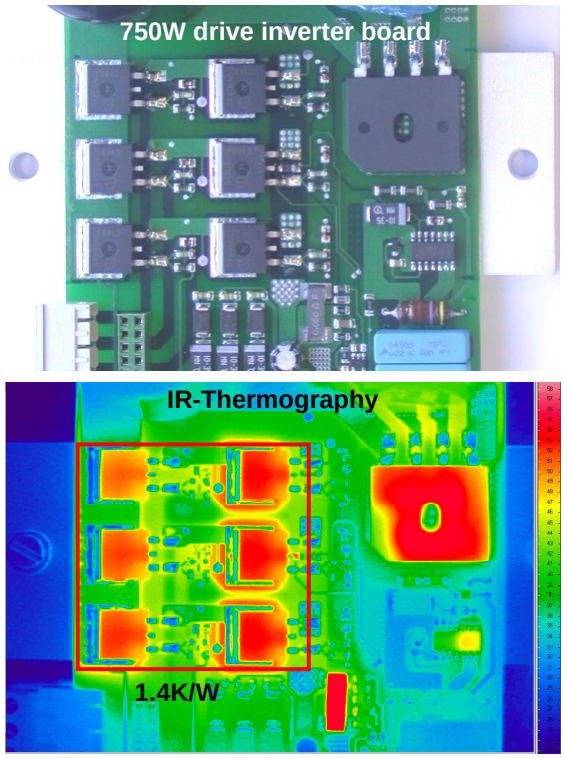


Fig. 6: A 750W drive inverter board with on-board power stage. Bottom: Thermography under nominal load.

The total power dissipation of the inverter is 35W, the power dissipation of the six IGBTs (with package integrated freewheeling diodes) 25W under nominal load (= 910VA at the line input). With the hottest spot on the IGBTs 35K above heatsink temperature, this results in a global thermal resistance of the IGBT bridge of 1.4K/W. This value includes all partial thermal resistances from the IGBT chip through the package, the FR-4 board and the glue layer between the board and the mounting base.

The most important measures for an effective thermal management on a PCB level are shown in fig. 7, which summarizes the results of chapter 2.

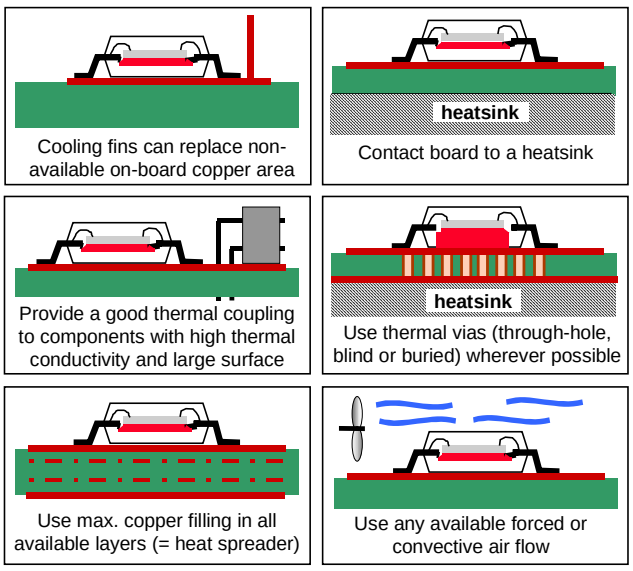


Fig. 7: How to improve thermal properties of SMD boards

3. Package Developments

Over the past years the semiconductor industry has achieved enormous improvements in low-voltage MOSFETs (<100V). Since the packaging technology could not keep up with this development the strange situation intensifies that the key parameters of many modern MOSFET devices, like maximum current, ON-resistance or switching-speed, are greatly influenced if not even defined by the package and not by the silicon.

Current developments in SMD power packages mainly aim at an improvement of the thermal properties of packages with a small form factor (e.g. SO-), and at how to overcome the current, reliability and stray inductance limitations caused by the bond-wire technology. Some of these developments are shown in fig. 8 [2]. The upper two are improvements of the traditional SO package. By applying solder bump technology the bond wires could be eliminated. In the bottomless version the drain back-metal of the chip is directly soldered to PCB. This results in a dramatic reduction of the internal thermal resistance ($R_{th,j\text{-}c}$) from

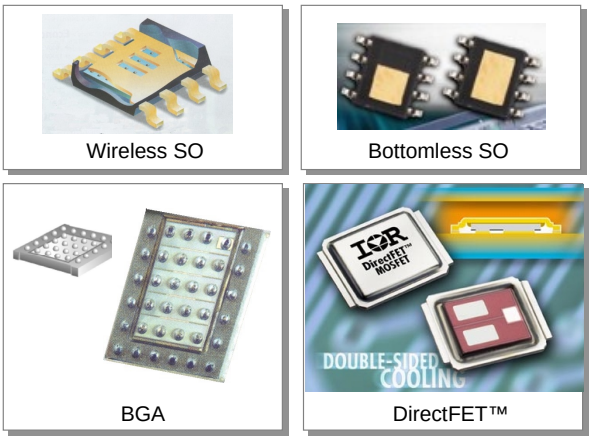


Fig. 8: New developments in SMD packages for discrete power semiconductors

about 25K/W with a standard SO-8 down to 2K/W for the bottomless version. The BGA package offers the most silicon per PCB area, a similar trend-setting approach is the DirectFET™ from IR. Both of these wireless packages combine lowest package resistance and stray inductance with SMT compatibility, a height of only 0.7mm, and the possibility of an effective double-sided cooling. This makes these packages predestined for ultra-high power density converters.

4. Cooling of Passive Components

An absolute prerequisite for achieving high power densities is that also the passive components are included in the thermal management of a converter.

Passive components generally consist of materials with a poor thermal conductivity like polymers (capacitors) or ferrites. An effective cooling requires large heat conducting areas and short heat paths therefore, similar to the situation in a PCB. This inevitably leads to a layer structure, normally a stack of planar layers. A possible realization is schematically shown in fig. 9. Essential criteria for the layer arrangement are the thermal flux density produced by the individual component and the maximum operating temperature of each material. The higher the heat flux density the tighter the thermal coupling to the heatsink must be. Typical heat flux densities are in the range of 1...100W/cm^2 for semiconductor devices, 0.1... 1W/cm^2 for magnetic components and below 0.1W/cm^2 for capacitors.

The diagram in fig. 10 gives the permissible layer thickness (i.e. the heat path length) depending on the heat flux density for a temperature drop of 10K and for different thermal conductivities. In the case of volume heating (e.g. in a ferrite) the permissible layer thickness doubles with single-sided cooling and quadruples with double-sided cooling. Considering the situation in fig. 9 with a single-sided cooled capacitor, fig. 10 gives a permissible height of the capacitor foil stack (λ = 0.35W/mK) of up to 7mm under the assumption of a heat flux density of 0.1W/cm^2 and a maximum temperature gradient across the capacitor of 10K. This stack height is an absolutely practical dimension.

Sometimes more complex laminations of dielectrics and magnetics are necessary, e.g. for resonant converter. In this case interlayers of materials with anisotropic thermal conductivity can be effectively used as »heat extractors«, which simultaneously provide heat conductor and heat-shielding functionality. Plates of natural graphite are excellently suitable for this. This material provides a thermal conductivity of about 370K/W in plane and only 7K/W perpendicular to the plane. With a volume weight of 1.9kg/cm^3 it is even lighter than aluminium [3].

In future, such kind of stacked structures of dielectrics and magnetics will gain more and more importance for high density power converters ([4], [5]). The main advantages of such a structure are:

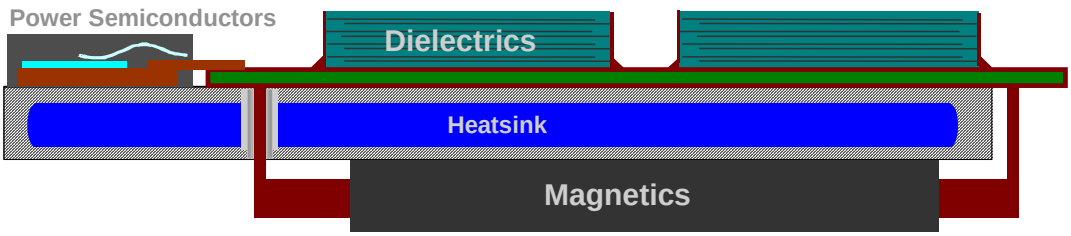


Fig. 9: Integration concept for high density power electronics

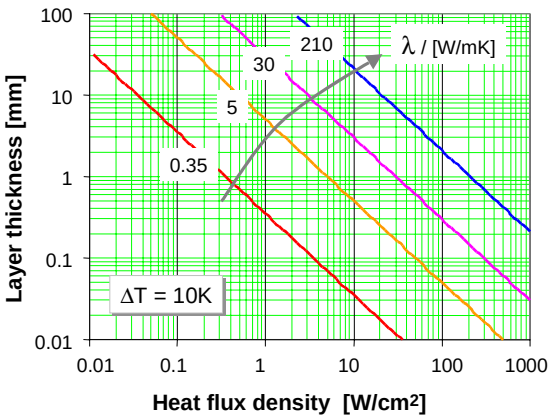


Fig. 10: Allowable thickness of heat conducting layer depending on heat flux density and thermal conductivity

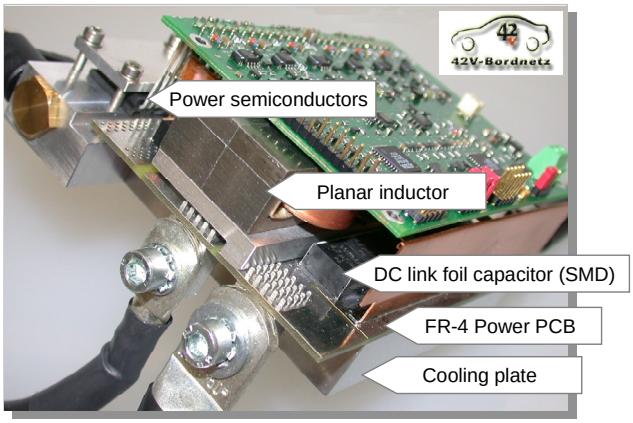


Fig. 11: 2kW DC/DC converter for automotive powernet

- optimal cooling of all active and passive power components
- very low dead volumes, high power density
- very low circuit parasitics, good EMI behaviour
- high mechanical stability and vibration immunity.

Fig. 11 shows the prototype of a water-cooled 2kW DC/DC converter which has been realized following roughly the described principles. The converter allows a bidirectional power transfer between 12V and 42V and achieves its nominal output power with a coolant temperature of up to 105°C. All power components are thermally coupled to the heatsink, the power board (FR-4) with double-sided 105µm copper conducts currents of more than 200A. The efficiency exceeds 90% over a wide power range. The power density is about 3.5W/cm^3. Only inexpensive standard components are used, the d.c. link capacitors are e.g. standard foil types in the SMD package size 6560.

5. Conclusions

A sophisticated thermal management can considerably improve the power density and reliability of power electronic systems. Existing packaging and mounting techniques still offer a large potential for intelligent optimization. In near future, power densities of up to 10W/cm^3 will become standard for isolating DC/DC converter. Single commercial products with up to 50W/cm^3 are already available.

Each thermal design must be verified by simulations and measurements. Here thermal imaging is an enormously powerful tool, e.g. in detecting hidden hot spots. Thermal impedance (Z_{th}) measurements allow the parameterization of lumped equivalent networks for thermal-electric modeling [6]. With that the verification of device temperatures under complex load profiles is possible by means of circuit simulators like Spice.

Beside all thermal optimizations on a board and system level one must never forget, however, that the by far most effective measure in thermal management is to avoid heat generation. In many cases, money spent on better components or more intelligent circuit topologies (e.g. synchronous MOSFET instead of Schottky rectifier) is payed back by less expensive heatsinks, improved reliability, and – in the long term – less energy costs.

6. Acknowledgment

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7. References

[1] Coombs´, C.F.: *Printed Circuits Handbook.* 15th edition, McGraw-Hill

[2] Klein J., Marx F.: *Silicon and packaging for DC/DC applications.* PCIM Europe 7 (2000), pp. 30-34

[3] Norley J., et al.: *Developments in Natural Graphite Heat Spreaders and Heatsink for Power Electronics Applications.* Proc. of 24th Intern. PCIM Conference (2003), Nuremberg

[4] van Wyk J.D., et al.: *Review of the Development of High Density Integrated Technology for Electromagnetic Power Passives.* Proceedings of 2nd Intern. Conference on Integrated Power Systems, CIPS 2002, pp. 25-34

[5] Ferreira J.A., Gerber M.: *Three dimensional Integration based on Power Module Technology.* Proceedings of 2nd Intern. Conference on Integrated Power Systems, CIPS 2002, pp. 35-41

[6] März M., Nance P.: *Thermal Modeling of Power Electronic Systems.* PCIM Europe 2 (2000), pp. 20-27