ECHELON

PL 3120® / PL 3150® Power Line Smart Transceiver Data Book

Version 2

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Introduction

Overview

This manual provides detailed technical specifications on the electrical interfaces, mechanical interfaces, and operating environment characteristics for the PL 3120® and PL 3150® Power Line Smart Transceivers. This manual also provides guidelines for migrating applications to the PL Smart Transceiver using the NodeBuilder® Development Tool.

In some cases, vendor sources are included in this manual to simplify the task of integrating the PL Smart Transceivers with application electronics. A list of related documentation is provided in section 1.5, Related Documentation, at the end of this chapter. The documents listed in this section can be found on the Echelon Web site at `www.echelon.com` unless otherwise noted.

Product Overview

The PL Smart Transceivers provide a simple, cost-effective method of adding LONWORKS® power line signaling and networking to everyday devices. Compliant with the open ANSI/EIA standards, the smart transceivers are ideal for networked appliance, audio/video, lighting, heating/cooling, security, metering, and irrigation applications.

Representing a breakthrough in price, performance and packaging size, the PL Smart Transceivers integrate a Neuron® processor core with a power line transceiver that is fully compatible with the LONMARK® PL-20 channel type. Essentially a system-on-a-chip, the smart transceivers feature a highly reliable ANSI/EIA 709.2 compliant, narrow-band power line transceiver, an ANSI/EIA 709.1 compliant Neuron processor core for running applications and managing network communications, a choice of on-board or external memory, and an extremely small form factor. A wide variety of pre-designed, low-cost coupling circuit designs enable the PL Smart Transceivers to communicate over virtually any AC or DC power mains, as well as over an unpowered twisted pair.

LONWORKS Networks

In almost every industry today, there is a trend away from proprietary control schemes and centralized systems. The migration towards open, distributed, peer-to-peer LONWORKS networks is being driven by the interoperability, robust technology, faster development time, and scale economies afforded by LONWORKS based solutions. All of the everyday devices in a LONWORKS network communicate using the ANSI/EIA 709.1 protocol standard. This seven-layer OSI protocol provides a set of services that allow the application program in a device to send and receive messages from other devices in the network without needing to know the topology of the network or the functions of the other devices.

LONWORKS networks provide a complete suite of messaging services, including end-to-end acknowledgement, authentication, and priority message delivery. Network management services allow network tools to interact with devices over the network, including local or remote reconfiguration of network addresses and parameters, downloading of application programs, reporting of network problems, and start/stop/reset of device application programs.

Neuron Chips, a family of microprocessors originally designed by Echelon and licensed to third party semiconductor manufacturers, combine an ANSI/EIA 709.1 compliant processor core for running applications and managing the network communications, with a media-independent communication port, memory, I/O, and a 48-bit identification number (Neuron ID) that is unique to every device. The communication port permits short distance Neuron Chip-to-Neuron Chip communications, and can also be used with external line drivers and transceivers of almost any type.

The Neuron 3120 Chip family includes self-contained application program memory (no external memory bus) and the real-time operating system (RTOS) and application libraries pre-programmed in ROM. The Neuron 3150 Chip family includes both internal memory and an external memory bus.

The PL Smart Transceivers integrate a Neuron processor core with an ANSI/EIA 709.2 compliant power line transceiver within a single IC, eliminating the need for an external transceiver. Two variants of PL Smart Transceivers are available:

- The **PL 3120** chip includes self-contained application program memory, RTOS, and application library pre-programmed in ROM.
- The **PL 3150** chip includes both internal memory and an external memory bus.

Two Product Families

Two versions of the PL Smart Transceivers are available to meet a wide range of applications and packaging requirements.

	Model Number	Maximum Input Clock	EEPROM	RAM	ROM	External Memory Interface	IC Package
PL 3120- E4T10	15311R-1000	10 MHz	4 Kbytes	2 Kbytes	24 Kbytes	No	38 TSSOP
PL 3150-L10	15321R-960	10 MHz	0.5 Kbytes	2 Kbytes	N/A	Yes	64 LQFP

The PL 3120 Smart Transceivers are targeted at small form factor designs that require up to 4KB of application code. The PL 3120 operates at either 6.5536MHz (A-band) or 10.0MHz (C-band), and includes 4KB of EEPROM and 2KB of RAM. Neuron system firmware (RTOS) along with application libraries is contained in on-chip ROM.

For applications that require more memory, the PL 3150 Smart Transceivers operate at either 6.5536MHz (A-band) or 10.0MHz (C-band), provide 0.5KB of EEPROM and 2KB of RAM, and use a 64 LQFP package. Through an external memory bus, the PL 3150 Smart Transceiver can address up to 58KB of external memory, of which 16KB is dedicated to Neuron system firmware.

The embedded EEPROM in both the PL Smart Transceivers can be written up to 10,000 times with no data loss. Data stored in the EEPROM will be retained for at least 10 years.

Both PL Smart Transceivers have 12 I/O pins which can be configured to operate in one or more of 38 predefined standard input/output modes. Combining a wide range of I/O models with two on-board timer/counters and a hardware SCI/SPI UART enables the PL Smart Transceivers to interface to application circuits with minimal external logic or software development.

Revision B of both PL Smart Transceivers (identified by a “B” in the lower right-hand corner of the package marking) includes an on chip crystal oscillator. This eliminates the need for the previously required off-chip inverter (see the section *Clock Input* in Chapter 2 for more information).

Power Line Signaling

The underlying signaling technology used in the PL Smart Transceivers was developed and optimized through more than ten years of field-testing. Over 20 million of the Echelon narrow band transceivers have been deployed in a wide range of consumer, utility, building, industrial, and transportation applications worldwide. Features such as narrow-band BPSK signaling, dual carrier frequency operation, adaptive carrier and data correlation, impulse noise cancellation, tone rejection and low-overhead error correction provide superior reliability in the face of interfering noise sources.

Dual Carrier Frequency Operation

The PL Smart Transceivers utilize a dual-carrier frequency signaling technology to provide superior communication reliability in the face of interfering noise sources. In the case of acknowledged messaging, packets are initially transmitted on the primary frequency and if an acknowledgement is not received the packet is retransmitted on the secondary frequency. In the case of unacknowledged-repeat messaging, packets are alternately transmitted on the primary and secondary frequencies. In utility applications the primary and secondary communication frequencies lie within the A-band shown in Figure 1.1. In non-utility applications, the primary communication frequency lies in the C-band shown in Figure 1.1 while the secondary frequency actually lies in what is called the B-band in CENELEC nomenclature. Figure 1.2 illustrates how the primary and secondary communications fit into the various frequency bands.

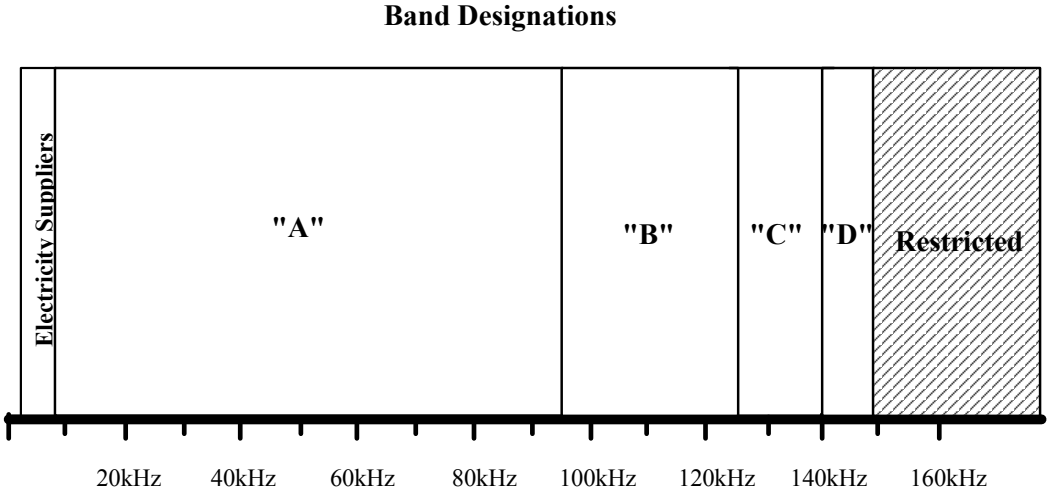


Figure 1.1 CENELEC Frequency Band Designations

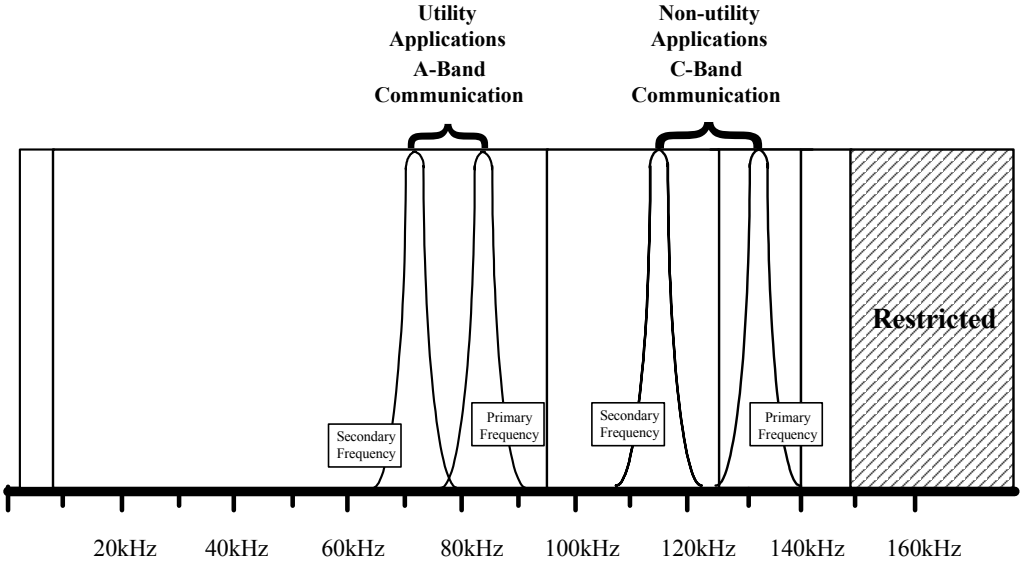


Figure 1.2 Dual-Carrier Frequency Operation

Forward Error Correction

Many noise sources interfere with power line signaling by corrupting data packets. The PL Smart Transceivers use a highly efficient, low-overhead forward error correction (FEC) algorithm in addition to a cyclical redundancy check (CRC) to overcome packet errors.

Powerful Output Amplifier

The external, high performance amplifier design developed for use with the PL Smart Transceivers provides a 1 Ohm output impedance and 1Ap-p current capability to drive high output levels into low impedance circuits, while maintaining the extremely low signal distortion levels necessary to meet stringent international EMC regulations. For applications requiring even more output power an optional higher power design is available that provides up to 2Ap-p of output current.

Wide Dynamic Range

Dynamic range relates to the sensitivity of the receiver. The PL Smart Transceivers have a dynamic range of > 80dB. On a quiet line the Power Line Smart Transceivers can receive signals that have been attenuated by a factor of more than 10,000.

Low Current Consumption

The PL Smart Transceivers and their associated power amplifier circuitry are powered by user-supplied +8.5 to +18VDC (V_A) and +5VDC (V_{DD5}) power supplies. Built-in power management features, combined with a wide supply range, are key benefits when designing inexpensive power supplies. Power management is especially useful for high volume, low cost consumer products such as electrical switches, outlets, and incandescent light dimmers.

Very low receive mode current consumption of just 350µA typical from the V_A supply and 9mA typical from the V_{DD5} supply reduces power supply size and cost.

The PL Smart Transceivers communicate at a raw bit rate of 5.4kbps (C-band) or 3.6kbps (A-band), corresponding to maximum packet rates of 20 and 13 packets per second, respectively. This high throughput makes the transceivers well suited for residential, commercial, and industrial automation applications.

Compliant with Regulations Worldwide

The PL Smart Transceivers are designed to comply with FCC [1], Industry Canada, Japan MPT, and European CENELEC EN50065-1 regulations [2], allowing them to be used in applications worldwide. The CENELEC communications protocol is fully implemented by the PL Smart Transceivers, eliminating the need for users to develop the complex timing and access algorithms mandated under CENELEC EN50065-1. Additionally, the PL Smart Transceivers can operate in either the CENELEC utility (A-band) or consumer (C-band) bands.
Figure 1.1 above shows the CENELEC frequency restrictions that are mandatory in EU countries and are observed in many non-EU countries as well. FCC, Industry Canada and the Japan MPT regulations are less strict than the CENELEC requirements. The frequency allocations for these countries are summarized in Figure 1.3.

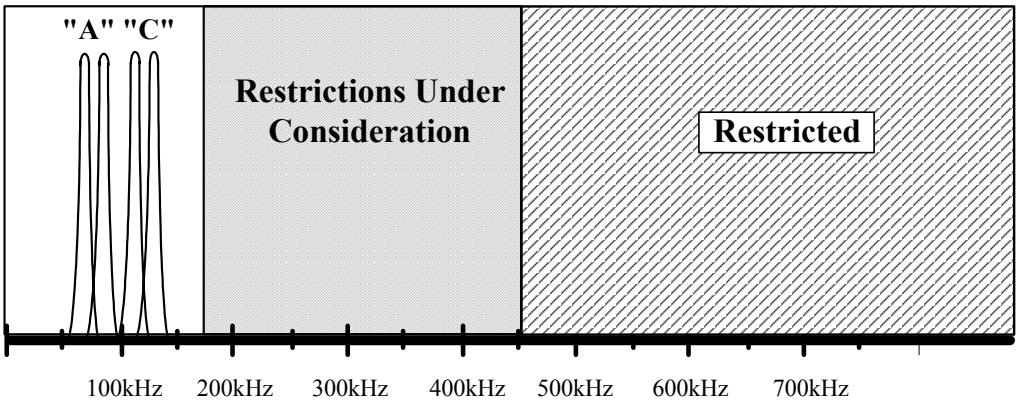


Figure 1.3 FCC, Industry Canada, Japan MPT Power-line Signaling

Integrated, Low-Cost and Small Form Factor Design

A small number of inexpensive external components are required to create a complete PL Smart Transceiver-based device. Figure 1.4 illustrates the block diagram of a PL Smart Transceiver based device. Available from Echelon is a comprehensive Development Support Kit (DSK) that includes sample PL Smart Transceivers, schematics, printed circuit board (PCB) layouts, bills of materials, and technology emulation hardware with sample application code (see *Note*) that customers can use to implement this interface circuitry.

Note: The emulation hardware and sample application code will be available beginning in Q4 of 2004.

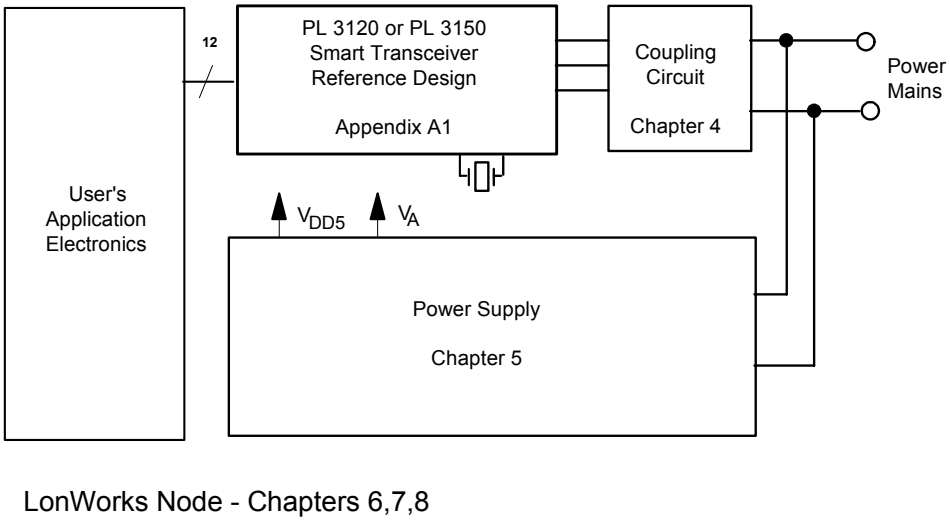


Figure 1.4 LONWORKS Device Block Diagram

Electric Utility vs. Home/Commercial/Industrial Applications

The PL Smart Transceivers are designed to operate in one of two frequency ranges (LONWORKS channels) depending on the end application. When configured for use in electric utility applications, the smart transceivers communicate in the A-band frequency range. In home/commercial/industrial applications, they communicate in the C-band frequency range. The use of separate operating frequency bands for utility and non-utility applications originated in Europe and has because become a de facto standard because of the numerous benefits it provides in terms of bandwidth management, security and privacy.

Extensive Development Resources

A wide assortment of technical documentation, diagnostic tools, support programs, and training courses are available to assist customers with their projects. Additionally, Echelon offers fee-based pre-production design reviews of customer's products, schematics, PCB layouts, and bills of material to verify that they comply with published guidelines. Communication performance-verification testing is provided to customers who submit working devices.

Audience

The *PL 3120/PL 3150 Power Line Smart Transceiver Databook* provides specifications and user instructions for PL Smart Transceiver customers.

Content

This User's Guide describes the use of the PL Smart Transceivers in both utility (A-band) and home/commercial/industrial (C-band) applications.

Related Documentation

The following documents are suggested reading:

PL 3120 and PL 3150 Smart Transceiver Data Sheet (003-0378-01)

Neuron C Programmer's Guide (078-0002-02)

Neuron C Reference Guide (078-0140-02)

Neuron 3150 Chip External Memory Interface Engineering Bulletin (005-0013-01)

LONWORKS Microprocessor Interface Program User's Guide (078-0017-01)

NodeBuilder User's Guide (078-0141-01)

Parallel I/O Interface to the Neuron Chip Engineering Bulletin (005-0021-01)

PLCA-22 Power Line Communication Analyzer User's Guide (078-0147-01)

LONWORKS PCLTA-20 PCI Interface User's Guide (078-0179-01)

Neuron Chip Quadrature Input Function Interface Engineering Bulletin (005-0003-01)

Power Line SLTA Adapter and Power Line PSG/3 Users's Guide (078-01188-01)

2

Hardware Resources

Overview

The PL 3120 Smart Transceiver is a complete SoC (system-on-a-chip) for designs that require up to 4kB of memory while the PL 3150 Smart Transceiver supports external memory for more complex applications. The major hardware blocks of both processors are the same, except where noted; see Table 2.1 and Figure 2.1.

Table 2.1 Comparison of PL Smart Transceivers

Characteristic	PL 3150 Smart Transceiver	PL 3120 Smart Transceiver
RAM Bytes	2,048	2,048
ROM Bytes	—	24,576
EEPROM Bytes	512	4,096
General purpose I/O pins	12	12
16-Bit Timer/Counters	2	2
External Memory Interface	Yes	No
Package	64 pin LQFP	38 pin TSSOP

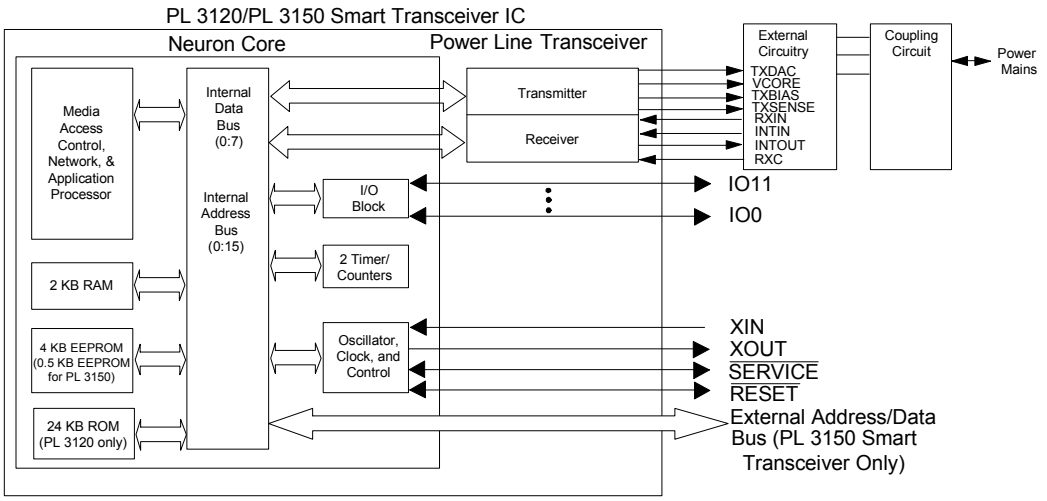


Figure 2.1 PL Smart Transceiver Block Diagram

Neuron Processor Architecture

The Neuron core is composed of three processors. These processors are assigned to the following functions by the Neuron firmware.

Processor 1 is the MAC layer processor that handles layers 1 and 2 of the 7-layer LonTalk® protocol stack. This includes driving the communications subsystem hardware and executing the media access control algorithm. Processor 1 communicates with Processor 2 using network buffers located in shared RAM memory.

Processor 2 is the network processor that implements layers 3 through 6 of the LonTalk protocol stack. It handles network variable processing, addressing, transaction processing, authentication, background diagnostics, software timers, network management, and routing functions. Processor 2 uses network buffers in shared memory to communicate with Processor 1, and application buffers to communicate with Processor 3. These buffers are also located in shared RAM memory. Access to them is mediated with hardware semaphores to resolve contention when updating shared data.

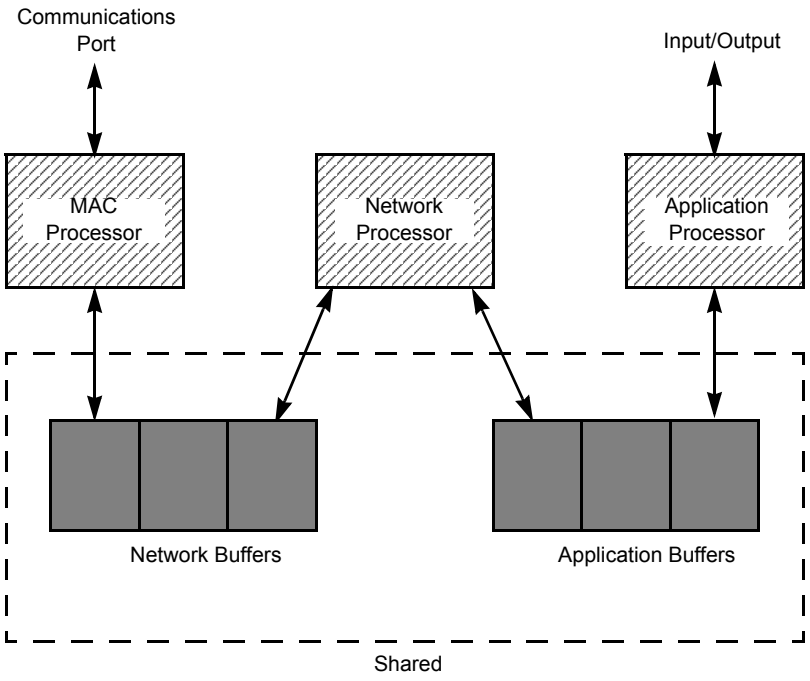


Figure 2.2 Processor Shared Memory Allocation

Processor 3 is the application processor. It executes the code written by the user, together with the operating system services called by user code. The primary programming language used by applications is Neuron C, a derivative of the ANSI C language optimized and enhanced for LONWORKS distributed control applications. The major enhancements are the following (see the *Neuron C Programmer's Guide* for details):

- A network communication model, based on *functional blocks* and *network variables*, that simplifies and promotes data sharing between like and disparate devices.
- A network configuration model, *based on functional blocks and configuration properties*, that facilitates interoperable network configuration tools.
- A type model based on standard and user *resource files* that expands the market for interoperable devices by simplifying the integration of devices from multiple manufacturers.
- An extensive set of I/O drivers that support the I/O capabilities of the Neuron core.
- Powerful event driven programming extensions that provide easy handling of network, I/O, and timer events.

The support for all these capabilities is part of the Neuron firmware, and does not need to be written by the programmer.

Each of the three identical processors has its own register set (Table 2.2), but all three processors share data, ALUs (arithmetic logic units) and memory access circuitry (Figure 2.3). On the PL 3150 Smart Transceiver, the internal address, data, and R/$\overline{W}$ signals are reflected on the corresponding external lines when utilized by any of the internal processors. Each CPU *minor* cycle consists of *three system clock* cycles, or phases; each system clock cycle is two input clock cycles. The minor cycles of the three processors are offset from one another by one system clock cycle, so that each processor can access memory and ALUs once during each instruction cycle. Figure 2.3 shows the active elements for each processor during one of the three phases of a minor cycle. Therefore, the system pipelines the three processors, reducing hardware requirements without affecting performance. This allows the execution of three processes in parallel without time-consuming interrupts and context switching.

Table 2.2 Register Set

Mnemonic	Bits	Contents
FLAGS	8	CPU Number, Fast I/O Select, and Carry Bit
IP	16	Next Instruction Pointer
BP	8	Address of 256-byte Base Page
DSP	8	Data Stack Pointer Within Base Page
RSP	8	Return Stack Pointer Within Base Page
TOS	8	Top of Data Stack, ALU Input

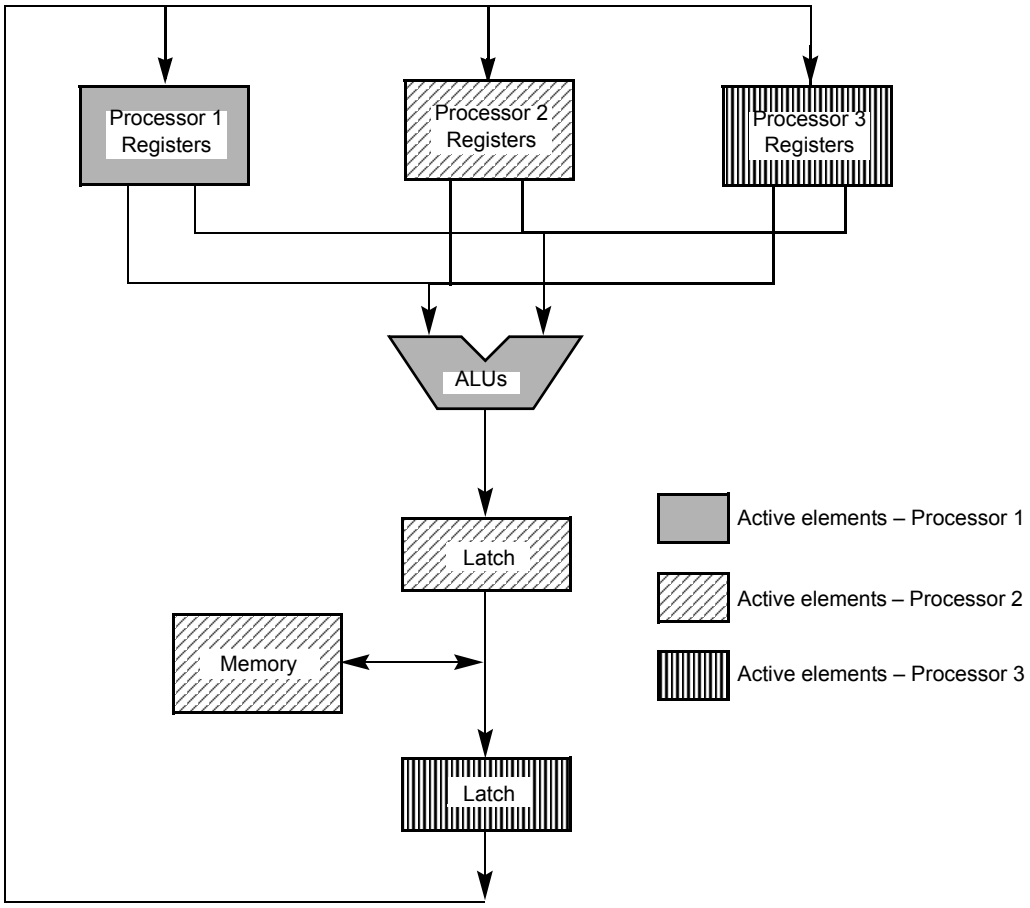


Figure 2.3 Processor/Memory Activity During One of the Three System Clock Cycles of a Minor Cycle

The architecture is stack-oriented; one 8-bit wide stack is used for data references, and the ALU operates on the TOS (Top of Stack) register and the next entry in the data stack which is in RAM. A second stack stores the return addresses for CALL instructions, and can also be used for temporary data storage. This stack architecture leads to very compact code. Tables 2.3, 2.42.4, and 2.5 outline the instruction set.

Figure 2.4 shows the layout of a base page, which can be up to 256 bytes long. Each of the three processors uses a different base page, whose address is given by the contents of the BP register of that processor. The top of the data stack is in the 8-bit TOS register, and the next element in the data stack is at the location within the base page at the offset given by the contents of the DSP register. The data stack grows from low memory towards high memory. The assembler shorthand symbol NEXT refers to the contents of the location (BP+DSP) in memory, which is not an actual processor register.

Pushing a byte of data onto the data stack involves the following steps: incrementing the DSP register, storing the current contents of TOS at the address (BP+DSP) in memory, and moving the byte of data to TOS.

Popping a byte of data from the data stack involves the following steps: moving TOS to the destination, moving the contents of the address (BP+DSP) in memory to TOS, and decrementing the DSP register.

The return stack grows from high memory towards low memory. Executing a subroutine call involves the following steps: storing the high byte of the instruction pointer register IP at the address (BP+RSP) in memory, decrementing RSP, storing the low byte of IP at the address (BP+RSP) in memory, decrementing RSP, and moving the destination address to the IP register.

Similarly, returning from a subroutine involves the following steps: incrementing RSP, moving the contents of (BP+RSP) to the low byte of the IP register, incrementing RSP, and moving the contents of (BP+RSP) to the high byte of IP.

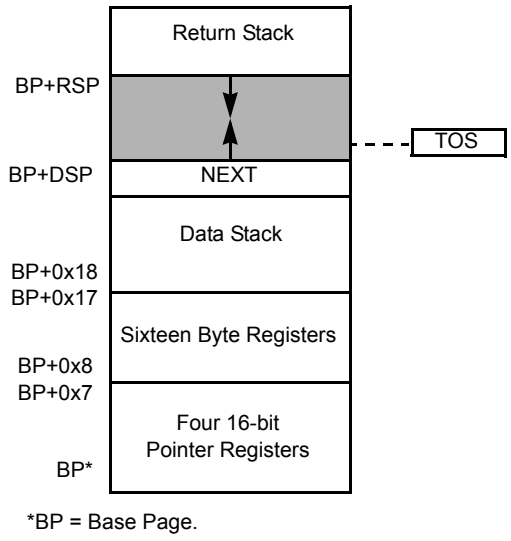


Figure 2.4 Base Page Memory Layout

A processor instruction cycle is three system clock cycles, or six input clock (XIN) cycles. Most instructions take between one and seven processor instruction cycles. At an input clock rate of 10MHz, instruction times vary between 0.6 μs and 4.2 μs. Execution time scales inversely with the input clock rate. The formula for instruction time is:

```
(Instruction Time) = (# Cycles) x 6 / (Input Clock)
```

Tables 2.3, 2.4, and 2.5 list the processor instructions, their timings (in cycles) and sizes (in bytes). This is provided for purposes of calculating the execution time and size of code sequences. All programming of the PL Smart Transceiver is done with Neuron C using the NodeBuilder development tool. The Neuron C compiler can optionally produce an assembly listing, and examining this listing can help the programmer to optimize the Neuron C source code.

Table 2.3 Program Control Instructions

Mnemonic	Cycles	Size (bytes)	Description	Comments
NOP	1	1	No operation	
SBR	1	1	Short unconditional branch	Offset 0 to 15
BR/BRC/BRNC	2	2	Branch, branch on (not) carry	Offset -128 to +127
SBRZ/SBRNZ	3	1	Short branch on TOS (not) zero	Offset 0 to 15. Drops TOS
BRF	4	3	Unconditional branch far	Absolute address
BRZ/BRNZ	4	2	Branch on TOS (not) zero	Offset -128 to +127. Drops TOS
RET	4	1	Return from subroutine	Drops two bytes from return stack
BRNEQ	4/6	3	Branch if TOS not equal (taken/not taken)	Offset -128 to +127. Drops TOS if equal
DBRNZ	5	2	Decrement [RSP] and branch if not zero	Offset -128 to +127. If not taken, drops one byte from return stack
CALLR	5	2	Call subroutine relative	Offset -128 to +127. Pushes two bytes to return stack
CALL	6	2	Call subroutine	Address in low 8KB. Pushes two bytes to return stack
CALLF	7	3	Call subroutine far	Absolute address. Pushes two bytes to return stack

Table 2.4 Memory/Stack Instructions

Mnemonic	Cycles	Size (bytes)	Comments / Effective Address (EA)
PUSH TOS	3	1	Increment DSP, duplicate TOS into NEXT
DROP TOS	3	1	Move NEXT to TOS, decrement DSP
DROP_R TOS	6	1	Move NEXT to TOS, decrement DSP, return from call
PUSH (NEXT, DSP, RSP, FLAGS)	4	1	Push processor register
POP (DSP, RSP, FLAGS)	4	1	Pop processor register
DROP NEXT	2	1	Decrement DSP
DROP_R NEXT	5	1	Decrement DSP and return from call
PUSH/POP !D	4	1	Byte register [8 to 23]
PUSH !TOS	4	1	EA = BP + TOS, push byte to NEXT

POP !TOS	4	1	EA = BP + TOS, pop byte from NEXT
PUSH [RSP]	4	1	Push from return stack to data stack, RSP unchanged
DROP [RSP]	2	1	Increment RSP
PUSHS #literal	4	1	Push short literal value [0 to 7]
PUSH #literal	4	2	Push 8-bit literal value [0 to 255]
PUSHPOP	5	1	Pop from return stack, push to data stack
POPPUSH	5	1	Pop from data stack, push to return stack
LDBP address	5	3	Load base page pointer with 16-bit value
PUSH/POP [DSP][-D]	5	1	EA = BP + DSP - displacement [1 to 8]
PUSHD #literal	6	3	16-bit literal value (high byte first)
PUSHD [PTR]	6	1	Push from 16-bit pointer [0 to 3], high byte first
POPD [PTR]	6	1	Pop to 16-bit pointer [0 to 3], low byte first
PUSH/POP [PTR][TOS]	6	1	EA = (16-bit pointer) + TOS
PUSH/POP [PTR][D]	7	2	EA = (16-bit pointer) + displacement [0 to 255]
PUSH/POP absolute	7	3	Absolute memory address
IN/OUT	7 + 4n	1	Fast I/O instruction, transfer *n* bytes

Table 2.5 ALU Instructions

Mnemonic	Cycles	Size (bytes)	Operation
INC/DEC/NOT	2	1	Increment/decrement/negate TOS
ROLC/RORC	2	1	Rotate left/right TOS through carry
SHL/SHR	2	1	Unsigned left/right shift TOS, clear carry
SHLA/SHRA	2	1	Signed left/right shift TOS into carry
ADD/AND/OR/XOR/ADC	4	1	Operate with NEXT on TOS, drop NEXT
ADD/AND/OR/XOR #literal	3	2	Operate with literal on TOS
(ADD/AND/OR/XOR)_R	7	1	Operate with NEXT on TOS, drop NEXT and return
ALLOC #literal	3	1	Add [1 to 8] to data stack pointer
DEALLOC_R #literal	6	1	Subtract [1 to 8] from data stack pointer and return
SUB NEXT,TOS	4	1	TOS = NEXT - TOS, drop NEXT
SBC NEXT, TOS	4	1	TOS = NEXT - TOS - carry, drop NEXT
SUB TOS,NEXT	4	1	TOS = TOS - NEXT, drop NEXT
XCH	4	1	Exchange TOS and NEXT
INC [PTR]	6	1	Increment 16-bit pointer [0 to 3]

Memory

Memory Allocation Overview

PL 3150 Smart Transceiver Memory Allocation

See Figure 2.5 for a memory map of the PL 3150 Smart Transceiver.

- 512 bytes of in-circuit programmable EEPROM that store the following:
  - — Network configuration and addressing information.
  - — Unique 48-bit Neuron ID — written at the factory.
  - — User-written application code and read-mostly data. See Table 2.6 for available EEPROM space.
- 2,048 bytes of static RAM that store the following:
  - — Stack segment, application, and system data.
  - — Network and application buffers.
- The processor can access 59,392 bytes of the available 65,536 bytes of memory address space via the external memory interface. The remaining 6,144 bytes of the memory address space are mapped internally.
- 16,384 bytes of the external memory (59,392 bytes total) are required to store the following:
  - — The Neuron firmware, including the system firmware executed by the MAC and Network processors, and the executive supporting the application program.
- The rest of the external memory (43,008 bytes) is available for:
  - — User-written application code.
  - — Additional application read/write and non-volatile data.
  - — Additional network buffers and application buffers.

PL 3120 Smart Transceiver Memory Allocation

See Figure 2.6 for a memory map of the PL 3120 Smart Transceiver.

- 4,096 bytes of in-circuit programmable EEPROM that store:
  - — Network configuration and addressing information.
  - — Unique 48-bit Neuron ID — written at the factory.
  - — User-written application code and read-mostly data.
- 2,048 bytes of static RAM that store the following:
  - — Stack segment, application, and system data.
  - — Network buffers and application buffers.
- 24,576 bytes of ROM that store the following:
  - — The Neuron firmware, including the system firmware executed by the MAC and network processors, the executive supporting the application program, and application libraries.

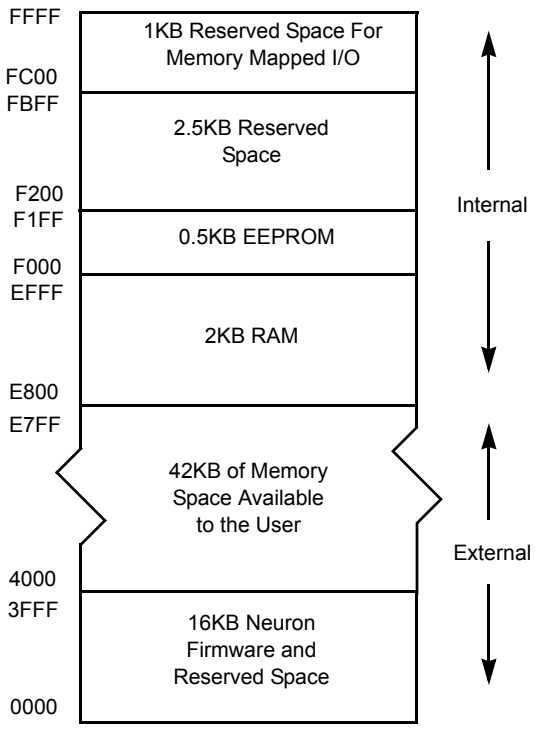


Figure 2.5 PL 3150 Smart Transceiver Memory Map

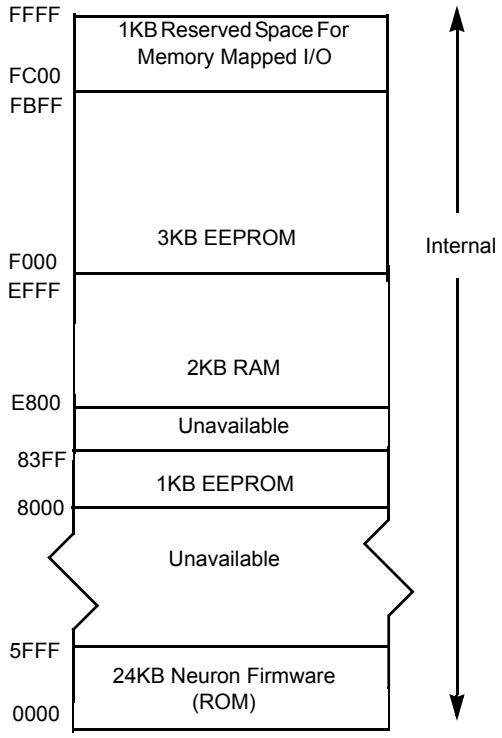


Figure 2.6 PL 3120 Smart Transceiver Memory Map

EEPROM

Both versions of the PL Smart Transceiver have internal EEPROM containing:

- Network configuration and addressing information.
- Unique 48-bit Neuron ID.
- Optional user-written application code and data tables.

All but 8 bytes of the EEPROM can be written under program control using an on-chip charge pump to generate the required programming voltage. The charge pump operation is transparent to the user. The remaining 8 bytes are written during manufacture, and contain a unique 48-bit identifier for each part called the *Neuron ID*, plus 16 bits for the chip manufacturer's device code. Each byte in the EEPROM region can be written up to 10,000 times. For both the PL 3120 and the PL 3150 Smart Transceivers, the EEPROM stores the installation-specific information such as network addresses and communications parameters. For the PL 3120 Smart Transceiver, the EEPROM also stores the application program generated by the NodeBuilder development tool. The application code for the PL 3150 Smart Transceiver can be stored either on-chip in the EEPROM memory or off-chip in external memory depending on the size of the application code. See Table 2.6 for available EEPROM space.

For all write operations to the internal EEPROM, the Neuron firmware automatically compares the value in the EEPROM location with the value to be written. If the two are the same, the write operation is not performed. This prevents unnecessary write cycles to the EEPROM, and reduces the average EEPROM write cycle latency.

When the PL Smart Transceiver is not within the specified power supply voltage range, a pending or on-going EEPROM write is not guaranteed. The PL Smart Transceiver contains a built-in low-voltage interruption (LVI) circuit that holds the chip in reset when V_{DD5} is below a certain voltage. See the *PL 3120 and PL 3150 Smart Transceiver Datasheet* for LVI trip points. This reduces the risk of EEPROM data corruption. For PL 3150 Smart Transceiver devices with external FLASH memory an external pulse stretching LVI is required. See the section *RESET Pin* for more information on LVI circuitry.

In the event of a fault, the on-chip EEPROM of the PL 3150 Smart Transceiver can be reset to its factory default state by executing the EEBLANK program. To do so, program the appropriate EEBLANK file into an external memory device, temporarily replace the application's external ROM or flash with the chip that has EEBLANK loaded, and power up the device. The EEBLANK files are named eeb<n>.nri where <n> is the Neuron input clock rate in kHz and is one of the following: 20000, 10000, 05000, 02500, 01250, or 00625. If you are using an input clock between two of these speeds, select the next slower version of EEBLANK.

After around 20 seconds (or less depending on clock speed), the device's service LED should come on solid, indicating that the EEPROM has been blanked. Then replace the original application ROM or flash. The EEBLANK files are distributed with NodeBuilder 3.1 and newer development tools. Versions of EEBLANK distributed with prior releases of the LonBuilder® and NodeBuilder tools should not be used with the PL 3150 Smart Transceiver.

The `set_eeprom_lock()` function can also be used for additional protection against accidental EEPROM data corruption. This function allows the application program to set the state of the lock on the checksummed portion of the EEPROM. Refer to the *Neuron C Reference Guide* for more information.

The internal EEPROM of a PL Smart Transceiver will contain a fixed amount of overhead and a network image (configuration), in addition to user code and user data. The following table shows the maximum amount of EEPROM space available for user code and user data assuming a minimally-sized network image. Also shown is the minimum segment size for user data. Constant data is assumed to be part of the code space.

Table 2.6 Memory Usage

Device	Firmware Version	EEPROM Space (Bytes)	Segment Size (Bytes)
PL 3120 Smart Transceiver	14	3969	8
PL 3150 Smart Transceiver	14 or newer	384	2

EEPROM must be allocated in increments of the device's segment size, the smallest unit of EEPROM that can be allocated for variable space. For example, if there are three 3-byte variables used, there must be 9 bytes of variable space. For a PL 3120 Smart Transceiver, this would result in the allocation of 16 bytes for variable space, as 16 bytes is the lowest increment of the device segment size (8 bytes) that can store the three 3-byte variables. For a PL 3150 Smart Transceiver, this would result in the allocation of 10 bytes for variable space, as 10 bytes is the lowest increment of the device segment size (2 bytes) that can store the three 3-byte variables.

Static RAM

The PL Smart Transceivers contain 2048 bytes of static RAM.

The RAM is used to store the following:

- Stack segment, application, and system data
- Network buffers and application buffers

The RAM state is retained as long as power is applied to the device. After reset, releasing the PL Smart Transceiver initialization sequence will clear the RAM (see the section *Reset Processes and Timing* for more information).

Pre-programmed ROM

The PL 3120 Smart Transceiver contains 24,576 bytes of pre-programmed ROM. This memory contains the Neuron firmware, including the LonTalk protocol stack, real time task scheduler, and system function libraries. The Neuron firmware for the PL 3150 Smart Transceiver is stored in external memory. The object code is supplied with the NodeBuilder tool.

PL 3150 Smart Transceiver External Memory Interface

The external memory interface of the PL 3150 Smart Transceiver (the PL 3120 Smart Transceiver has no external memory interface) supports up to 42K Bytes of external memory space for additional user program and data. The total address space is 64K Bytes. However, the upper 6k of address space is reserved for internal RAM, EEPROM, and memory-mapped I/O (see Figures 2.5 and 2.6), leaving 58K Bytes of external address space. Of this space, 16K Bytes is used by the Neuron firmware. The external memory space can be populated with RAM, ROM, PROM, EPROM, EEPROM, or flash memory in increments of 256 bytes. The memory map for the PL 3150 Smart Transceiver is shown in Figure 2.5. The bus has 8 bidirectional data lines and 16 address lines driven by the processor. Two interface lines (R/$\overline{W}$ and $\overline{E}$) are used for external memory access. Refer to the *PL 3150 Smart Transceiver Datasheet* for the required access times for the external memory used. The input clock rates supported by the PL 3150 Smart Transceiver are 10MHz and 6.5536MHz. The Enable Clock ($\overline{E}$) runs at the system clock rate, which is one-half the input clock rate. All memory, both internal and external, can be accessed by any of the three processors at the appropriate phase of the instruction cycle. BecauseBecause the instruction cycles of the three processors are offset by one-third of a cycle with respect to each other, the memory bus is used by only one processor at a time.

The *Neuron 3150 Chip External Memory Interface* engineering bulletin provides guidelines for interfacing the PL 3150 Smart Transceiver to different types of memory. A minimum hardware configuration would use one external ROM (PROM or EPROM), containing both the Neuron firmware and user application code. This configuration would **not** allow the system engineer to change the *application code* over the network after installation. The *network image* (*network address* and *connection* information) however, could be altered because this information resides in internal EEPROM. If application downloads over the network are a requirement for maintenance or upgrade and the application code will not fit into the internal EEPROM, then external EEPROM or flash will be necessary. Refer to the *Neuron C Programmer's Guide* for guidelines to reduce code size.

The pins used to interface with external memory are listed in Table 2.7. The $\overline{E}$ clock signal is used to generate read (or write) signals to external memory. The A15 (address line 15) or a programmable array logic (PAL) decoded signal gated with R/$\overline{W}$ can be used to generate read signals to external memory.

Table 2.7 External Memory Interface Pins

Pin Designation	Direction	Function
A0 - A15	Output	Address Pins
D0 - D7	Input/Output	Data Pins
E	Output	Enable Clock
R/W	output	Read/Write Select Low

The preferred method of interfacing the PL Smart Transceiver to another MPU is through the 12 I/O pins using a serial or parallel connection, or through a dual-ported RAM device such as the Cypress CY7C144, CY7C138, or CY7C1342. There are pre-defined serial and parallel I/O models for this purpose which are easily implemented using the Neuron C programming language or MIP firmware can be used to simplify the interface. For more details of dual-ported RAM interfacing, see Appendix B of the *LONWORKS Microprocessor Interface Program User's Guide* (Echelon 078-0017-01).

Input/Output

Twelve Bidirectional I/O Pins

These pins are usable in several different configurations to provide flexible interfacing to external hardware and access to the internal timer/counters. The logic level of the output pins can be read back by the application processor.

Pins IO4 – IO7 and IO11 have programmable pull-up current sources. They are enabled or disabled with a compiler directive (see the *Neuron C Reference Guide*). Pins IO0 – IO3 have high current sink capability (20 mA @ 0.8 V). The others have sink capability of 1.4 mA @ 0.5 V. All pins (IO0 – IO11) have TTL level inputs with hysteresis. Pins IO0 – IO7 also have low level detect latches.

Two 16-Bit Timer/Counters

The timer/counters are implemented as a load register writable by the processor, a 16-bit counter, and a latch readable by the processor. The 16-bit registers are accessed 1 byte at a time. Both the PL 3150 and PL 3120 Smart Transceivers have one timer/counter whose input is selectable among pins IO4 – IO7, and whose output is pin IO0, and a second timer/counter with input from pin IO4 and output to pin IO1 (Figure 2.7). No I/O pins are dedicated to timer/counter functions. If, for example, Timer/Counter 1 is used for input signals only, then IO0 is available for other input or output functions. Timer/counter clock and enable inputs can be from external pins, or from scaled clocks derived from the system clock; the clock rates of the two timer/counters are independent of each other. External clock actions occur optionally on the rising edge, the falling edge, or both rising and falling edges of the input.

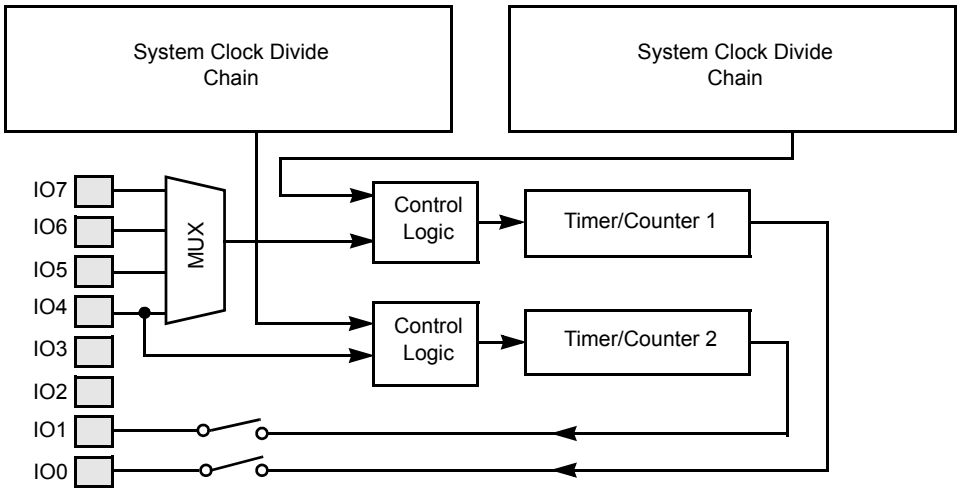


Figure 2.7 Timer/Counter Circuits

Clock Input

The PL Smart Transceivers require an input clock of 6.5536MHz for A-band operation and 10.0000MHz for C-band operation. The input clock can be provided by connection of the appropriate parallel resonant crystal to the XIN and XOUT pins of the PL Smart Transceiver as shown in Figure 2.8.

The Revision B PL 3150 and PL 3120 Smart Transceiver chips (identified by the letter “B” in the lower right hand corner of the package marking) do not require the use of an external inverter, as was required with Revision A parts. New reference layouts, provided as part of current Development Support Kits (DSKs), no longer include this inverter. Refer to Appendix A for more information regarding the current PL Smart Transceiver DSK.

Current reference designs include the optional capacitors indicated in Figure 2.8. These capacitors are not needed if the load capacitance of the crystal is matched to the capacitance provided by the combination of the PL Smart Transceiver chip and the PCB traces. The schematic for each reference design includes a table listing the required crystal load capacitance both with and without these optional load capacitors. These tables cover crystal load capacitance values ranging from 15pF to 20pF.

Crystals with a load capacitance greater than 20pF should not be used with the PL Smart Transceiver chips. Even though the optional capacitors would allow centering the frequency of oscillation with higher load capacitance crystals, doing so could prevent the oscillator from starting under worst-case conditions. To further ensure proper oscillator startup, the ESR specification for the crystal should be $\leq$100Ω for A-band and $\leq$60Ω for C-band operation.

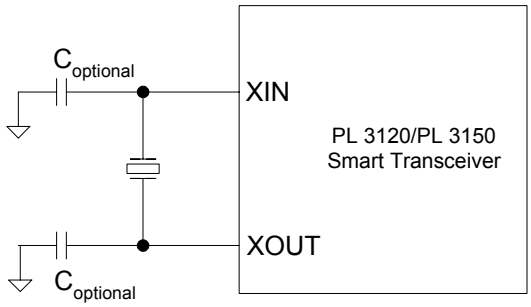


Figure 2.8 PL Smart Transceiver crystal clock connections

The PL Smart Transceiver requires a frequency accuracy of ±200ppm over the full range of component tolerances and operating conditions. Variation within the PL Smart Transceiver IC uses a portion of the overall ±200ppm budget. The remaining portion of the error budget allocated for total crystal uncertainty is ±85ppm (assuming that the selected crystal has a load capacitance specification which matches the circuit loading as described above). Total crystal uncertainty is the combination of the crystal's initial frequency tolerance plus its temperature and aging tolerances.

If the load capacitance specification of the crystal is not matched to the circuit then there will be a nominal frequency error that will reduce the portion of the error budget that is available for crystal uncertainty. For example, using a 20pF crystal in a circuit designed for 18pF of load capacitance results in a nominal frequency of oscillation about 40ppm above the specified frequency. Thus using a crystal with a load capacitance 2pF different from the actual circuit load constrains the total available crystal tolerance to just +45/-125ppm.

In order to achieve proper frequency centering for PL Smart Transceivers starting with Rev B (and later), the following guidelines must be followed.

- Rev B PL Smart Transceivers can be used with older reference designs, which include the off-chip inverter, as long as the inverter is still installed.
- Do not use Rev B PL Smart Transceivers with older reference designs, which include an off-chip inverter, without installing the off-chip inverter.
- Rev B PL Smart Transceivers can be used with new reference designs (which do not include an off-chip inverter).

If a 10.0000MHz clock signal is already available elsewhere on a C-band circuit board (6.5536MHz for an A-band board) then it can be used as a clock source for the PL Smart Transceiver as long as the clock signal meets several requirements. First the clock must have an accuracy of ±200ppm over all operating conditions. Its duty cycle symmetry must be no worse than 60/40% when connected to a 33pF load and measured using a 0.9V threshold. In addition the voltage swing of the clock signal must be within the GND and V_{DD5} supply rails of the PL Smart Transceiver. To use this clock option, the appropriate clock signal should be connected to the XIN pin of the PL Smart Transceiver and the XOUT pin of the PL Smart Transceiver should be left open. Note also that appropriate high frequency clock distribution techniques must be used to ensure that a clean clock signal is present at the XIN pin of the PL Smart Transceiver.

The accuracy of any clock oscillator should be checked during the design verification phase of every PL Smart Transceiver based product. This measurement must be made without adding any capacitance to either the XIN or XOUT pins of the PL Smart Transceiver. Holding a probe near but not touching the clock lines and then connecting

this probe to a spectrum analyzer with an accurate time-base provides one way to make this measurement without affecting the frequency of oscillation.

Band-In-Use (BIU) and Packet Detect (PKD) LED Connections

The PL Smart Transceiver supplies two output signals, PKD and BIU, that are intended to drive low-current light-emitting diodes (LEDs). Both signals are active-high and must be connected to separate LEDs, with series current-limiting resistors added between the LEDs and ground.

A Band-In-Use detector, as defined under CENELEC EN 50065-1:2001, must be active whenever a signal that exceeds 86dBμV_{RMS} anywhere in the frequency range 131.5kHz to 133.5kHz is present for at least 4ms. The Band-In-Use detector is defined by CENELEC EN 50065-1:2001 as part of the CENELEC access protocol. The PL 3120 and PL 3150 Smart Transceiver incorporates the CENELEC access protocol, and the PL Smart Transceiver can be programmed to enable or disable its operation (See the *CENELEC Access Protocol* section in Chapter 8). When the PL Smart Transceiver is programmed such that the CENELEC access protocol is enabled, the BIU signal is active high whenever the CENELEC-defined conditions for Band-In-Use are met. When the CENELEC access protocol is disabled, an active BIU signal does not prevent the PL Smart Transceiver from transmitting.

The Band-In-Use function is defined for use in the CENELEC C-band and is not required for A-band operation. When the PL Smart Transceiver is programmed with proper A-band transceiver parameters, as described in Chapter 8, an active BIU signal does not prevent the PL Smart Transceiver from transmitting.

The PKD signal is active whenever a LonTalk packet addressed to any device is being received by the PL Smart Transceiver. The receive sensitivity of the transceiver is considerably greater than that of the BIU indicator. The PKD signal will go active when the PL Smart Transceiver receives packets whose signal level is as small as 36dBμV_{RMS}. Thus it is not uncommon for the PKD indicator to signal that a packet is present without the BIU indicator turning on; this occurs in cases where the received packet signal strength is less than the BIU threshold.

ESD protection diodes should be connected to BIU and PKD in applications where the BIU and PKD signals drive LEDs that could be subject to ESD exceeding 2kV. Refer to the *ESD Design Issues* section in Chapter 6 for recommendations regarding ESD protection. In applications where the LEDs are surrounded by a metallic ground plane, such as a hole in a grounded metal enclosure, the ESD diodes might not be necessary.

TXON Output Signal

TXON is a buffered version of the internal signal used to control the transceiver's output amplifier. The TXON signal output is active high when the PL Smart Transceiver transmits packets. TXON can be used to drive a low-current LED to indicate transmit activity. A series current-limiting resistor is required between the LED and ground. ESD protection diodes should be connected to this pin in applications where the TXON signal line could be subjected to ESD exceeding 2kV.

Additional Functions

Reset Function

The reset function is a critical operation in any embedded microcontroller. In the case of the PL Smart Transceivers, the reset function plays a key role in the following conditions:

- Initial V_{DD5} power up (ensures proper initialization of the PL Smart Transceiver).
- V_{DD5} power fluctuations (manages proper recovery of PL Smart Transceiver after V_{DD5} stabilizes).
- Program recovery (if an application gets lost due to corruption of address or data, an external reset can be used for recovery or the watchdog timer could timeout, causing a watchdog reset).
- V_{DD5} power down (ensures proper shut down).
- Helps protect the EEPROM from major corruption.

The PL Smart Transceivers have four mechanisms to initiate a reset:

- $\overline{\text{RESET}}$ pin is pulled low and then returned high.
- Watchdog timeout occurs during application execution (the timeout period is 840ms at 10MHz; this figure scales inversely with clock frequency).
- Software command either from the application program or from the network.
- LVI circuit detects a drop in the power supply below a set level.

When in reset, the pins of the PL Smart Transceiver go to the states described in the list below. Figure 2.10 shows the state of the pins during reset and the initialization sequence just after reset.

- Oscillator continues to run
- All processor functions stop
- $\overline{\text{SERVICE}}$ pin goes to high impedance
- I/O pins go to high impedance
- All address pins go to 0xFFFF (PL 3150 Smart Transceiver only)
- All data pins become outputs with low states (PL 3150 Smart Transceiver only)
- $\overline{\text{E}}$ clock goes high (PL 3150 Smart Transceiver only)
- R/$\overline{\text{W}}$ goes low (PL 3150 Smart Transceiver only)

When the $\overline{\text{RESET}}$ pin is released back to a high state, the PL Smart Transceiver begins its initialization procedure starting at address 0x0001. The time it takes the PL Smart Transceiver to complete its initialization differs between PL Smart Transceivers, the different firmware versions that are being run, and the memory space used by the application (code and data). This will be discussed later in this section.

$\overline{\text{RESET}}$ Pin

The $\overline{\text{RESET}}$ pin is both an input and an output. As an input, the $\overline{\text{RESET}}$ pin is internally pulled high by a current source acting as a pull-up resistor. The $\overline{\text{RESET}}$ pin becomes an output when any of the following events occur:

- Watchdog Timer timeout
- Software reset.
- Internal LVI detects a low voltage

In some cases, external circuitry might be required on the $\overline{\text{RESET}}$ line. If an additional device is connected to the $\overline{\text{RESET}}$ line, a capacitor of at least 100pF and less than 1000pF should be connected between RESET and ground to provide noise immunity. Examples of additional devices are push buttons, microcontrollers, and external pulse stretching LVIs. The capacitance must not exceed 1000pF in order to guarantee the PL Smart Transceiver can successfully drive RESET below 0.8V. For even greater noise immunity, two capacitors (totaling <1000pF) can be used with one from $\overline{\text{RESET}}$ to ground and the other from $\overline{\text{RESET}}$ to V_{DD5}. For in-circuitry test during manufacturing, a single test point is recommended with a very short trace length to control $\overline{\text{RESET}}$.

For a PL 3120 Smart Transceiver with no devices attached to the $\overline{\text{RESET}}$ pin, no external capacitance is required for noise immunity.

For a PL 3150 Smart Transceiver, an external pulse-stretching LVI of greater than 10 ms should be used (Echelon recommends using Dallas Semiconductor Part No. DS1233-5). A capacitor of at least 100pF and less than 1000pF should also be connected between $\overline{\text{RESET}}$ and ground to provide noise immunity. Figure 2.9 shows a typical circuit for a PL 3150 Smart Transceiver.

Important: The $\overline{\text{RESET}}$ pin should be hard wired to ground via a “pogo pin” during all board level testing such as ICT (in circuit testing). The PL Smart Transceivers are sensitive to disruptions in V_{DD5} and transients on the $\overline{\text{RESET}}$ pin during the time it is performing its initial (one time) boot initialization sequence.

WARNING: If the proper external reset circuitry is not used, the PL Smart Transceiver can go applicationless or unconfigured. The applicationless or unconfigured state occurs when the checksum error verification routine detects corruption in memory which could have falsely been detected due to an improper reset sequence or noise on the power supply. Several programming options are provided in the NodeBuilder tool to implement a reboot on checksum failure.

Power Up Sequence

During power up sequences, the $\overline{\text{RESET}}$ pin will be held low by the internal LVI until the power supply is stable, to prevent start-up malfunctioning. Likewise, when powering down, the PL Smart Transceiver $\overline{\text{RESET}}$ pin will go to a low state when the power supply goes below the minimum operating voltage of the PL Smart Transceiver.

Software Controlled Reset

When the CPU watchdog timer expires, or a software command to reset occurs, the $\overline{\text{RESET}}$ pin is pulled low for 256 XIN clock cycles.

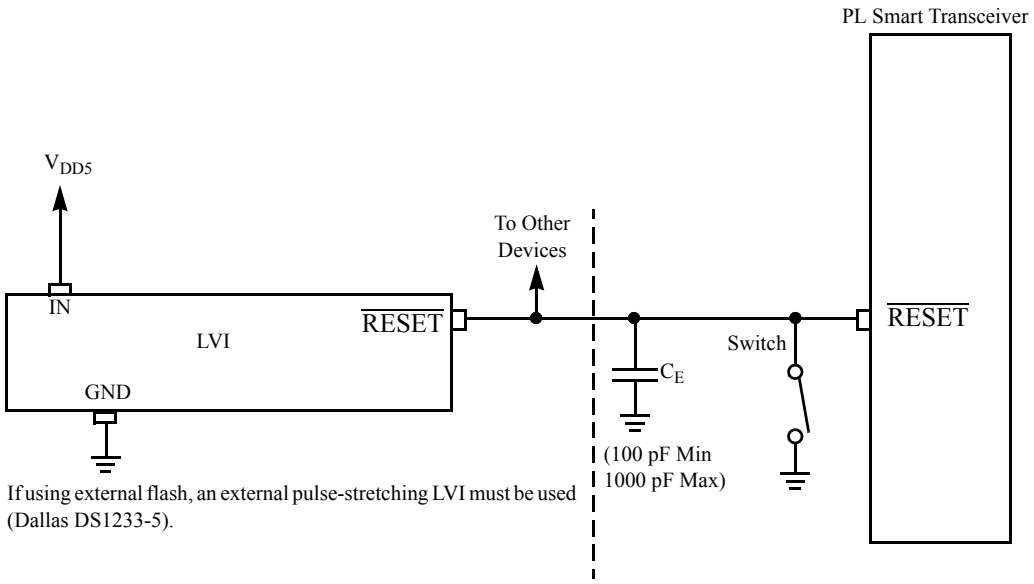


Figure 2.9 Reset Circuit Example

Watchdog Timer

The PL Smart Transceivers are protected against malfunctioning software or memory faults by three watchdog timers, one for each processor that makes up the Neuron core. If application or system software fails to reset these timers periodically, the entire PL Smart Transceiver is automatically reset. The watchdog period is approximately 840 ms at a 10MHz input clock rate and scales inversely with the input clock rate.

The Watchdog Timer circuit cannot be disabled.

LVI Considerations

The PL Smart Transceivers include an internal LVI to ensure that they only operate above the minimum voltage threshold. See the *PL 3120 and PL 3150 Smart Transceiver Datasheet* for LVI trip points.

When using an external oscillator to drive the XIN pin of the PL 3150 or PL 3120 Smart Transceivers, a power-on-pulse-stretching LVI might be needed to ensure that the external oscillator has stabilized before the PL Smart Transceiver is released from reset.

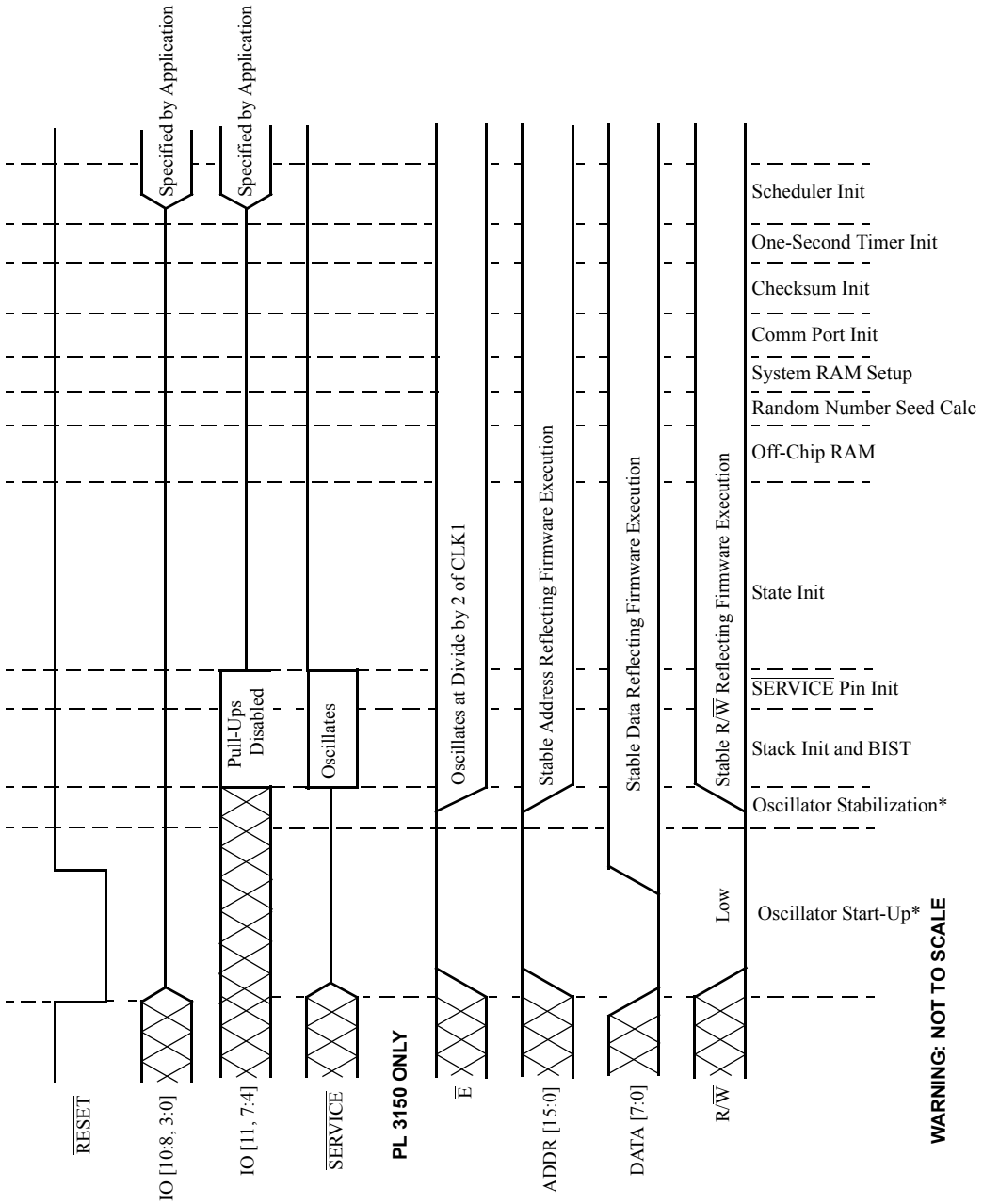
Because the $\overline{\text{RESET}}$ pin of the PL Smart Transceiver is bidirectional, an external LVI must have an open-drain or open-collector output. If an external LVI actively drives the $\overline{\text{RESET}}$ pin high, then the PL Smart Transceiver will not be able to reliably assert the $\overline{\text{RESET}}$ pin (low) during internal resets. This contention on the PL Smart Transceiver $\overline{\text{RESET}}$ pin can cause anomalous behavior, from applicationless errors to physical damage to the PL Smart Transceiver reset circuitry.

Reset Processes and Timing

During the reset period, the I/O pins are in a high-impedance state. The PL 3150 Smart Transceiver address lines A15 – A0 are forced to 0xFFFF, R/$\overline{W}$ is forced to 0, and $\overline{E}$ is forced to 1. The data lines are driven low, so they will not float and draw excess current. The $\overline{SERVICE}$ pin is high impedance during reset and the internal pull-up is disabled. Reset overrides the effect of $\overline{E}$ clock on data lines in that, in normal operations the data bus is only driven in a write cycle during the $\overline{E}$ clock low portion of the bus cycle, while reset forces the data bus to be driven. The steps followed in preparing the PL Smart Transceiver to execute the application code are discussed below. These steps are summarized in Figure 2.10.

After the $\overline{RESET}$ pin is released, the PL Smart Transceiver performs hardware and firmware initialization before executing application programs. These tasks are:

- Oscillator start-up
- Oscillator stabilization
- Stack initialization and built-in self-test (BIST)
- $\overline{SERVICE}$ pin initialization
- State initialization
- Off-chip RAM initialization
- Random number seed calculation
- System RAM setup
- Communication port initialization
- Checksum initialization
- One-second timer initialization
- Scheduler initialization



*NOTE: On power up, the oscillator will start running before $\overline{\text{RESET}}$ is released.

Figure 2.10 RESET Timeline for PL Smart Transceivers

During internal oscillator start up (after power up), the PL Smart Transceiver waits for the oscillator signal amplitude to grow before using the oscillator waveform as the system clock. This period depends on the type of oscillator used and its frequency, and begins as soon as power is applied to the oscillator and is independent of the $\overline{\text{RESET}}$ pin.

After the oscillator has started up, the PL Smart Transceiver counts additional transitions on XIN to allow the oscillator's frequency to stabilize. From the time $\overline{\text{RESET}}$ is asserted until the end of the oscillator stabilization period,

the I/O pins are in a high-impedance state. The $\overline{E}$ signal goes inactive (high) immediately after reset goes low, and the address bus becomes high (0xFFFF) to deselect external devices.

The stack initialization and BIST task tests the on-chip RAM, the timer/counter logic, and the counter logic. For the test to pass, all three processors and the ROM must be functioning. A flag is set to indicate whether the PL Smart Transceiver passed or failed the BIST. The RAM is cleared to all 0s by the end of this step. The $\overline{\text{SERVICE}}$ pin oscillates between a solid low and a weak high. The memory interface signals reflect execution of these tasks.

If the RAM self-test fails, the device goes offline, the service LED comes on solid, and an error is logged in the device's status structure.

Self-test results are available in the first byte of RAM (0xE800) as follows:

Value	Description
0	No Failure
1	RAM failure
2	Timer/counter failure
3	Counter failure
4	Configured input clock rate exceeds the chip maximum

The $\overline{\text{SERVICE}}$ pin initialization task turns off the $\overline{\text{SERVICE}}$ pin (high state).

The state initialization task determines if a PL Smart Transceiver boot is required (PL 3150 Smart Transceiver only), and performs the boot if it is required. The PL Smart Transceiver decides to perform a boot if it is blank, or if the boot ID does not match the boot ID in ROM.

The off-chip RAM initialization task checks the memory map to determine if any off-chip RAM is present and then either tests and clears all of the off-chip RAM or, optionally, clears the application RAM area only. This choice is controlled by the application program via a Neuron C compiler directive. This task applies only to the PL 3150 Smart Transceiver.

The random number seed calculation task creates a seed for the random number generator.

The system RAM setup task sets up internal system pointers as well as the linked lists of system buffers.

The checksum initialization task generates or checks the checksums of the nonvolatile writable memories. If the boot process was executed for the configured or unconfigured states, in the state initialization task, then the checksums are generated; otherwise, they are checked. This process includes on-chip EEPROM, off-chip EEPROM, flash, and off-chip nonvolatile RAM. There are two checksums, one for the configuration image and one for the application image. In each case, the checksum is a negated two's complement sum of the values in the image.

The one-second timer initialization task initializes the one-second timer. At this point, the network processor is available to accept incoming packets.

The scheduler initialization task allows the application processor to perform application-related initialization as follows:

- **State wait** — Wait for the device to leave the applicationless state.
- **Pointer initialization** — Perform a global pointer initialization.

- **Initialization step** — Execute initialization task, which is created by the compiler/linker to handle initialization of static variables and the timer/counters.
- **I/O pin initialization step** — Initialize I/O pins based on application definition. Prior to this point, I/O pins are high impedance.
- **State wait II** — Wait for the device to leave the unconfigured or hard-offline state. If waiting was required, a flag is set to indicate that the device should come up offline.
- **Parallel I/O synchronization** — Devices using parallel I/O attempt to execute the master/slave synchronization protocol at this point.
- **Reset task** — Execute the application reset task (`when (reset){}`).
- If the offline flag was set, go offline and execute the offline task (`when(offline){}`). If the BIST flag indicated a failure, then the $\overline{\text{SERVICE}}$ pin is turned on and the offline task is executed. Otherwise, the scheduler starts its normal task scheduling loop.

The amount of time required to perform these steps depends on many factors, including: PL Smart Transceiver model; input clock rate; whether or not the device performs a boot process; whether the device is applicationless, configured, or unconfigured; amount of off-chip RAM; whether the off-chip RAM is tested or simply cleared; the number of buffers allocated; and application initialization. Tables 2.8 and 2.9 summarize the number of input clock cycles (XIN) required for each of these steps for the PL 3120 and the PL 3150 Smart Transceivers. The times are approximate and are given as functions of the most significant application variables.

Table 2.8 PL 3120 Smart Transceiver Reset Sequence Time

Step	Number of XIN Cycles	Notes
Stack Initialization and BIST	386,000	
$\overline{\text{SERVICE}}$ Pin Initialization	1000	
State Initialization	250 (for no boot) 2,275,000 (for boot)	
Off-Chip RAM Initialization	0	
Random Number Seed Calculation	0	1
System RAM Set-up	21,000 + 600*B	2
Communication Port Initialization	0	1
Checksum Initialization	3400 + 175*M	3
One-Second Timer Initialization	6100	
Scheduler Initialization	≥ 7400	4

Notes:

1) These tasks run in parallel with other tasks.

2) B is the number of application and/or network buffers allocated.

3) M is the number of bytes to be checksummed.

4) Assumes a trivial initialization task, no reset task and the configured state.

For example, the timing of each of these steps is shown for a PL 3120 Smart Transceiver application with the following parameters:

- 10MHz input clock
- Crystal oscillator
- No boot required, at least 10 application and/or network buffers

- 500 bytes of EEPROM checksummed.

Stack Initialization and BIST	38.6000 ms
$\overline{\text{SERVICE}}$ Pin Initialization	0.1000 ms
State Initialization	0.0250 ms
Off-Chip RAM Initialization	0 ms
Random Number Seed Calculation	0 ms
System RAM Setup	2.7000 ms
Communication Port Initialization	0.0000 ms
Checksum Initialization	10.8000 ms
One-Second Timer Initialization	0.6100 ms
Scheduler Initialization	0.7400 ms
Total	53.5757 ms

Table 2.9 PL 3150 Smart Transceiver Reset Sequence Time

Step	Number of XIN Cycles	Notes
Stack Initialization and BIST	425,000	
$\overline{\text{SERVICE}}$ Pin Initialization	1000	
State Initialization	1300 (for no boot) 70,000 + 25 ms*E (for boot)	1
Off-Chip RAM Initialization	24,000 + 214*R (for test and clear) 24,000 + 152*R_a (for clear only)	2 3
Random Number Seed Calculation	50,000 max	
System RAM Setup	27,000 + 1500*B	4
Communication Port Initialization	0	5
Checksum Initialization	7200 + 175*M (for no boot) 82,000 + 100 ms + 175*M (for boot)	6, 7
One-Second Timer Initialization	6100	
Scheduler Initialization	≥ 7400	8

***Notes*:**

1) E is the number of non-zero bytes being written (ranges from 10 to 504).

2) R is the number of off-chip RAM bytes.

3) R_a is the number of non-system off-chip RAM bytes.

4) B is the number of application and/or network buffers allocated.

5) These tasks run in parallel with other tasks.

6) M is the number of bytes to be checksummed.

7) Only if booting to the configured or unconfigured state; if booting to the applicationless state, use the “no boot” equation.

8) Assumes a trivial initialization task, no reset task, and the configured state.

For example, the timing of each of these steps is shown for a PL 3150 Smart Transceiver application with the following parameters: 10MHz input clock, crystal oscillator, no boot required, 16k bytes external RAM, test and clear external RAM, at least 10 application and/or network buffers, and 500 bytes of EEPROM checksummed.

Stack Initialization and BIST	42.50 ms
$\overline{\text{SERVICE}}$ Pin Initialization	0.10 ms
State Initialization	0.13 ms
Off-Chip RAM Initialization	353.00 ms
Random Number Seed Calculation	5.00 ms
System RAM Setup	4.20 ms
Communication Port Initialization	0 ms
Checksum Initialization	12.50 ms
One-Second Timer Initialization	0.61 ms
Scheduler Initialization	0.74 ms
Total	418.78 ms

Use the following compiler directive to disable testing of off-chip RAM:

```
# pragma ram_test_off
```

$\overline{\text{SERVICE}}$ Pin

The $\overline{\text{SERVICE}}$ pin alternates between input and open-drain output at a 76 Hz rate with a 50% duty cycle with a 10MHz input clock. At 6.5536MHz, the $\overline{\text{SERVICE}}$ pin alternates at a 50 Hz rate. When it is an output, it can sink 20 mA for use in driving a LED. When it is used exclusively as an input, it has an optional on-chip pull-up to bring the input to an inactive-high state for use when the LED and pull-up resistor are not connected. Under control of the Neuron firmware, this pin is used during configuration, installation, and maintenance of the device containing the PL Smart Transceiver. The firmware flashes the LED at a 1/2 Hz rate when the PL Smart Transceiver has not been configured with network address information. Grounding the $\overline{\text{SERVICE}}$ pin causes the PL Smart Transceiver to transmit a network management message containing its unique 48-bit Neuron ID and the application's program ID on the network. This information can then be used by a network tool to install and configure the device. A typical circuit for the $\overline{\text{SERVICE}}$ pin LED and push-button is shown in Figure 2.11. During reset the $\overline{\text{SERVICE}}$ pin state is indeterminate. The default state of the $\overline{\text{SERVICE}}$ pin pull-up is enabled.

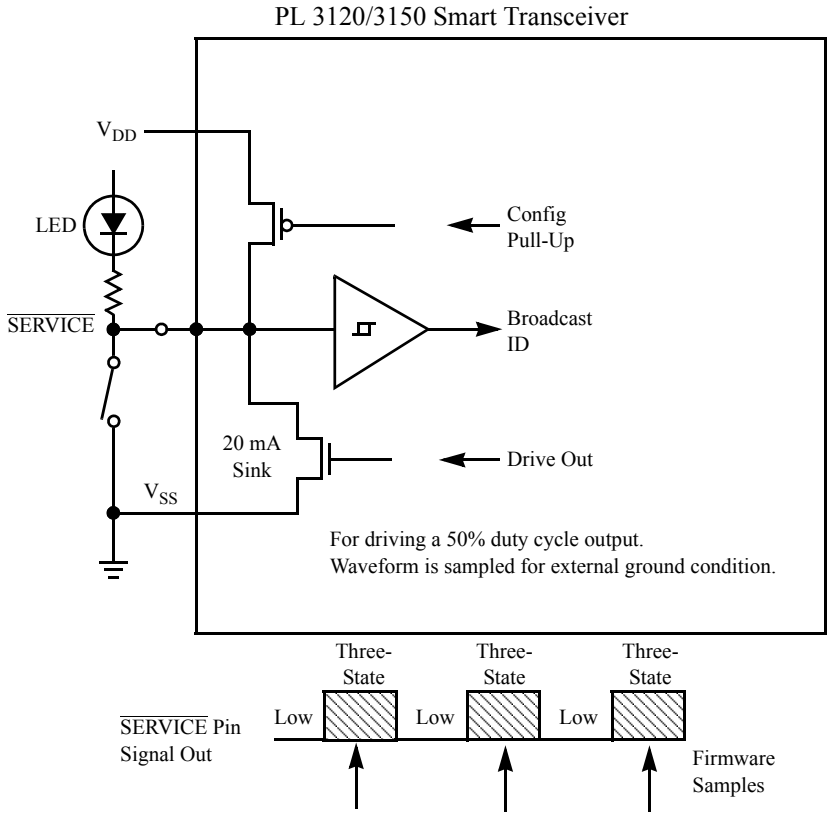


Figure 2.11 PL Smart Transceiver SERVICE Pin Circuit

Table 2.10 Service LED Behavior During Different States

Device State	0xF015 State Code	Service LED
Applicationless and Unconfigured	3	On
Unconfigured (but with an Application)	2	Flashing
Configured, Hard Offline	6	Off
Configured	4	Off
PL 3150 Defective External Memory	—	On

The SERVICE pin is active low and the service pin message is sent at maximum once per SERVICE pin transition. The service pin message goes into the next available priority or non-priority output network buffer. Devices in the applicationless state that do not have an external pullup will transmit the SERVICE pin message after every reset.

Integrity Mechanisms

Memory Integrity Using Checksums

To ensure the integrity of the memory of the PL Smart Transceiver, the Neuron firmware maintains a number of checksums. Each checksum is a single byte and is the two's complement of the sum of all bytes it covers. These checksums are verified during reset processing and also on a continual basis via a background diagnostic process. There are three main checksums used to verify the integrity of the PL Smart Transceiver's memory:

- Configuration image checksum
- Application image checksum
- System image checksum (off-chip system image only)

The configuration image checksum covers the network configuration information and communication parameters residing in the on-chip EEPROM. The default behavior is that a configuration checksum error causes the device to go to the unconfigured state. Refer to Table 2.12 for other options.

The application image checksum covers the application code in both on-chip EEPROM and any application code in off-chip EEPROM, NVRAM, or flash memory. This checksum can optionally be extended to cover any application code in off-chip ROM as well. The default behavior is that an application checksum error causes the device to go to the applicationless state. Application read/write data residing in EEPROM, NVRAM, or flash is not checksummed. Refer to Table 2.12 for other options.

Table 2.11 Checksum Coverage of PL Smart Transceiver Memory Areas

Memory Area	Checksum
System image (optionally covered by application checksum on the PL 3150)	System
Any off-chip ROM code (optionally covered by Application checksum on the PL 3150)	Application
Any off-chip flash, EEPROM, or NVRAM code	Application
Any off-chip RAM code	Application
Configuration image	Configuration
All on-chip EEPROM code	Application

In the PL 3150 Smart Transceiver, all memory areas listed in Table 2.11 except for on-chip EEPROM code have their own checksum so that checksum errors can be further isolated. An unconfigured or configured device continually checks its application checksum in the background at the rate of 1 byte per iteration through the network processor's main loop (3 bytes per millisecond when running at 10MHz with no network activity).

The system image checksum covers the system image. It is only available when the system image resides in off-chip memory and its use is optional. A system image checksum error always forces the device to the applicationless state.

No checksum is computed if the device is in the applicationless state.

The checksums are all verified during reset processing by the network processor and as part of the background diagnostic process. The background diagnostic process causes the device to reset when an error is detected; no state change occurs. It is assumed that any persistent error will be found by the reset processing.

Upon detecting a checksum error, the reset process will force the appropriate state and log an error in the error log. For the PL 3150 Smart Transceiver, a checksum must fail twice during reset processing in order for it to be deemed bad.

Reboot and Integrity Options Word

A PL 3150 Smart Transceiver has a number of options for actions taken following a checksum error or other memory related fatal errors. The 16-bit word that controls these options resides in the system image and is defined as part of the device's export options in the NodeBuilder tool.

The recovery process relies on the fact that the initial on-chip EEPROM image for the application, configuration, and communication parameter data reside in the off-chip system image. During initial power up, the system image data is copied (booted) to on-chip EEPROM. The recovery process recopies or reboots the suspect areas as dictated by the error and the recovery options. **Any changes made to the on-chip EEPROM (e.g., a network application load or network tool initiated reconfiguration) after the initial boot are lost in the recovery process.** The recovery action is defined by setting a combination of bits as defined by the following bit masks (Table 2.12).

Table 2.12 Recovery Action Bit Masks

Recovery Word	Description
0x0001	Reboot application if application fatal error.
0x0002	Always reboot application on reset (see note).
0x0004	Reboot configuration if configuration checksum fails.
0x0008	Reboot configuration on an application fatal error.
0x0010	Always reboot configuration on reset.
0x0020	Reboot communication parameters if configuration checksum fails.
0x0040	Reboot communication parameters if type or rate mismatch.
0x0080	Always reboot communication parameters on reset.
0x0100	Reboot EEPROM variables when rebooting application.
0x0200	Applicationless state is considered to be an application fatal error. If option 0x0001 or 0x0008 is set, applicationless state will result in a reboot. Application fatal errors are defined below (see note).
0x0400	Checksum all code, including system image.

Note: Applications exported with these options cannot be loaded over the network.

In the above options, "configuration" does not include the communication parameters because their recovery is governed separately. Also, fatal application errors refer to application image checksum errors, memory allocation failures, and memory map failures. Refer to *Loading an Application Image* in the *NodeBuilder User's Guide* (Release 3 Revision 2 or later) for more information.

The configuration will be rebooted independently of the application only if all the configuration table sizes match between EEPROM and ROM. This avoids a situation where a new application with different table sizes is loaded over the network, and a reboot of the configuration corrupts the program.

When an EEPROM recovery occurs due to a checksum failure or other error, the event will be logged in the error table of the Smart Transceiver. A test command will show **EEPROM recovery occurred** as the last error logged.

Reset Processing

During reset processing, the configuration checksum is checked first. If bad, and no configuration recovery options are set, then a configuration checksum error is logged, the checksum repaired, and the device state is changed to unconfigured. If the configuration recovery option is set, the configuration is recovered.

Next, the application checksum is checked. If bad, and the checksum error is in the system image, then a system image checksum error is logged and the device state is changed to applicationless.

If the application checksum is bad, and no application recovery options are set, an application checksum error is logged and the device state is changed to applicationless.

If the application checksum is bad and an application recovery option is set and the boot application does not contain references to any off-chip ROM, flash, EEPROM, NVRAM, or RAM code, or there are no checksum errors in any of these regions, then the application is recovered. Otherwise, an application checksum error is logged and the device goes applicationless.

Signatures

All off-chip code areas have a 2-byte cyclic redundancy check (CRC) called the **signature**, immediately following the area checksum. Signatures are stored in the code area and in the memory map. Mismatches between the area signature and memory map copy of the signature result in the device going applicationless. This mechanism prevents a partial application load over the network which is incompatible with any unloaded code (such as code in ROM).

3

Input/Output Interfaces

Introduction

The PL 3120 and PL 3150 Power Line Smart Transceivers connect to application-specific external hardware via 12 pins, named IO0-IO11. These pins can be configured in numerous ways to provide flexible input and output functions with minimal external circuitry. The programming model (Neuron C language) allows the programmer to declare one or more pins as I/O objects. An I/O object provides programmable access to an I/O driver for a specified on-chip I/O hardware configuration and a specified input or output waveform definition. With the exception of the SCI (UART) model, the user's program can then refer to these objects in `io_in` and `io_out()` system calls to perform the actual input/output function during execution of the program. Certain events are associated with changes in input values. The task scheduler can thus execute associated application code when these changes occur.

There are many different I/O objects available for use with the PL Smart Transceivers. Most I/O Objects are available in the PL 3150 and PL 3120 Smart Transceiver system images by default. If an object that is not included in the default system image is required by an application, the development tool will link the appropriate object(s) into available memory space. For PL 3120 Smart Transceiver designs, this means that internal EEPROM space must be used for the additional object. For PL 3150 Smart Transceiver designs, the object will be added to an external flash or ROM region beyond the 16KB space reserved for the system image.

PL Smart Transceivers have two 16-bit timer/counters on-chip (see Figure 2.7 and 3.1). The input to timer/counter 1, also called the *multiplexed timer/counter,* is selectable among pins IO4 – IO7, via a programmable multiplexer (MUX) and its output can be connected to pin IO0. The input to timer/counter 2, also called the *dedicated timer/counter,* can be connected to pin IO4 and its output to pin IO1. The timer/counters are implemented as a 16-bit load register writable by the CPU, a 16-bit counter, and a 16-bit latch readable by the CPU. The load register and latch are accessed a byte at a time. No I/O pins are dedicated to timer/counter functions. If, for example, timer/counter 1 is used for input signals only, then IO0 is available for other input or output functions. Timer/counter clock and enable inputs can be from external pins, or from scaled clocks derived from the system clock; the clock rates of the two timer/counters are independent of each other. External clock actions occur optionally on the rising edge, the falling edge, or both rising and falling edges of the input.

Multiple timer/counter input objects can be declared on different pins within a single application. By calling the `io_select()` function, the application can use the first timer/counter to implement up to four different input objects. If a timer/counter is configured to implement one of the output objects, or is configured as a quadrature input object, then it can not be reassigned to another timer/counter object in the same application program.

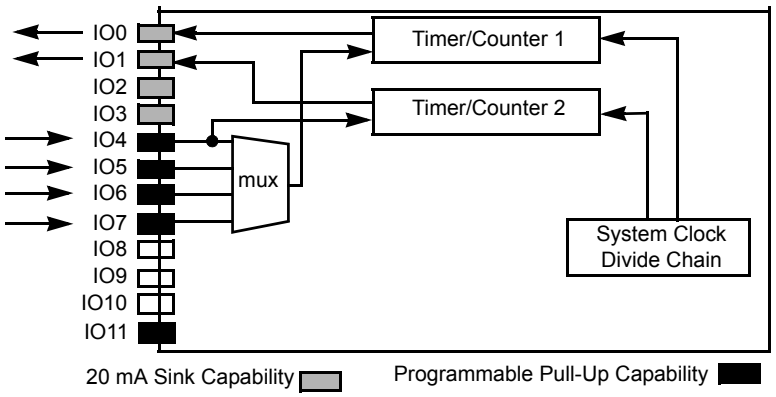


Figure 3.1 PL Smart Transceiver Timer/Counter External Connections

Hardware Considerations

Tables 3.1 through 3.5 list the available I/O objects. Various I/O objects of different types can be used simultaneously. Figure 3.3 summarizes the pin configuration for each of the I/O objects. For the electrical characteristics of these pins, refer to the *PL 3120 and PL 3150 Smart Transceiver Datasheet*. The following sections contain detailed descriptions of all the I/O objects. The application program can optionally specify the initial values of digital outputs. Pins configured as outputs can also be read as inputs, returning the value "at the I/O pin". Pins IO4 – IO7 and IO11 have optional pull-up current sources that act like pull-up resistors (see Figure 3.1). These are enabled with a Neuron C compiler directive (`#pragma enable_io_pullups`). Pins IO0 – IO3 have high sink capability. The others have standard sink capability. Pins IO0 – IO7 have low-level detect latches. **The latency and timing values described later in this section are typical at 10MHz.** The accuracy of these values is ± 10%. Most latency values scale inversely with clock rate.

The I/O pull-ups are not enabled during the stack initialization and BIST task. I/O pull-ups are only enabled if `#pragma enable_io_pullups` is specified in the Neuron C application. If an I/O pin is not used by the application, it must either be tied high or low on the PC board or left unconnected and configured as a bit output by the application in order to prevent unnecessary power consumption. This is particularly important for devices with energy storage power supplies (See Chapter 5 for more information).

Table 3.1 Summary of Direct I/O Objects

I/O Object	Applicable I/O Pins	Input/Output Value	Page
Bit Input	IO0 – IO11	0, 1 binary data	46
Bit Output	IO0 – IO11	0, 1 binary data	46
Byte Input	IO0 – IO7	0 – 255 binary data	48
Byte Output	IO0 – IO7	0 – 255 binary data	48
Leveldetect Input	IO0 – IO7	Logic 0 level detected	49
Nibble Input	Any adjacent 4 in IO0 – IO7	0 – 15 binary data	50
Nibble Output	Any adjacent 4 in IO0 – IO7	0 – 15 binary data	50

Table 3.2 Summary of Parallel I/O Objects

I/O Object	Applicable I/O Pins	Input/Output Value	Page
Muxbus I/O	IO0 – IO10	Parallel bidirectional port using multiplexed addressing	51
Parallel I/O	IO0 – IO10	Parallel bidirectional handshaking port	51

Table 3.3 Summary of Serial I/O Objects

I/O Object	Applicable I/O Pins	Input/Output Value	Page
Bitshift Input	Any adjacent pair (except IO7 + IO8 & IO10 + IO11)	Up to 16 bits of clocked data	59
Bitshift Output	Any adjacent pair (except IO7 + IO8 & IO10 + IO11)	Up to 16 bits of clocked data	59
I^2C	IO8 + IO9 or IO0 + IO1	Up to 255 bytes of bidirectional serial data	61
Magcard Input	IO8 + IO9 + (one of IO0 – IO7)	Encoded ISO7811 track 2 data stream from a magnetic card reader	63
Magtrack1	IO8 + IO9 + (one of IO0 – IO7)	Encoded ISO3554 track 1 data stream from a magnetic card reader	65
Magcard Bitstream	IO8 + IO9 + (one of IO0 – IO7)	Unprocessed serial data stream from a magnetic card reader	66
Neurowire I/O	IO8 + IO9 + IO10 + (one of IO0 – IO7)	Up to 256 bits of bidirectional serial data	66
Serial Input	IO8	8-bit characters	70
Serial Output	IO10	8-bit characters	70
Touch I/O	IO0 – IO7	Up to 2048 bits of input or output bits	72
Wiegand Input	Any adjacent pair in IO0 – IO7	Encoded data stream from Wiegand card reader	74
SCI (UART)	IO8 + IO10	Up to 255 bytes input and 255 bytes output	75
SPI	IO8 + IO9 + IO10 + (IO7)	Up to 255 byes of bidirectional data	76

Table 3.4 Summary of Timer/Counter Input Objects

I/O Object	Applicable I/O Pins	Input Signal	Page
Dualslope Input	IO0, IO1 + (one of IO4 – IO7)	Comparator output of the dualslope converter logic	83
Edgelog Input	IO4	A stream of input transitions	84
Infrared Input	IO4 – IO7	Encoded data stream from an infrared demodulator	86
Ontime Input	IO4 – IO7	Pulse width of 0.2 µs – 1.678 s	87
Period Input	IO4 – IO7	Signal period of 0.2 µs – 1.678 s	87
Pulsecount Input	IO4 – IO7	0 – 65,535 input edges during 0.839 s	89
Quadrature Input	IO4 + IO5, IO6 + IO7	± 16,383 binary Gray code transitions	90
Totalcount Input	IO4 – IO7	0 – 65,535 input edges	92

Table 3.5 Summary of Timer/Counter Output Objects

I/O Object	Applicable I/O Pins	Output Signal	Page
Edgedivide Output	IO0, IO1 + (one of IO4 – IO7)	Output frequency is the input frequency divided by a user-specified number	93
Infrared Pattern Output	IO0, IO1	Series of timed repeating square wave output signals	96
Frequency Output	IO0, IO1	Square wave of 0.3 Hz to 2.5MHz	95
Oneshot Output	IO0, IO1	Pulse of duration 0.2 µs to 1.678 s	97
Pulsecount Output	IO0, IO1	0 – 65,535 pulses	98
Pulsewidth Output	IO0, IO1	0 – 100% duty cycle pulse train	99
Triac Output	IO0, IO1 + (one of IO4 – IO7)	Delay of output pulse with respect to input edge	100
Triggered-Count Output	IO0, IO1 + (one of IO4 – IO7)	Output pulse controlled by counting input edges	102

To maintain and provide consistent behavior for external events and to prevent metastability, all 12 I/O pins of the PL Smart Transceiver, when configured as inputs, are passed through a hardware synchronization block sampled by the internal system clock. This is always the input clock divided by two (e.g. 10MHz ÷ 2 = 5MHz). For any signal to be reliably synchronized with a 10MHz input clock, it must be at least 220ns in duration (see Figure 3.2).

All inputs are software sampled during `when` statement processing. The latency in sampling is dependent on the I/O object which is being executed (see I/O timing specification and the *Neuron C Programmer's Guide* for more information). These latency values scale inversely with the input clock. Thus, any event that lasts longer than 220ns will be synchronized by hardware, but there will be latency in software sampling resulting in a delay detecting the event. If the state changes at a faster rate than software sampling can occur, then the interim changes will go undetected.

There are three exceptions to the synchronization block. First, the chip select ($\overline{CS}$) input used in the slave B mode of the parallel I/O object; this input will recognize rising edges asynchronously. Second, the leveldetect input is latched by a flip-flop with a 200ns clock. The level detect transition event will be latched, but there will be a delay in software detection. Third, the SCI (UART) and SPI objects are buffered on byte boundaries by the hardware and are transferred to memory using an interrupt mechanism. The input timer/counter functions are also different, in that events on the
I/O pins will be accurately measured and a value returned to a register, regardless of the state of the application processor. However, the application processor can be delayed in reading the register. Consult the *Neuron C Programmer's Guide* for detailed programming information.

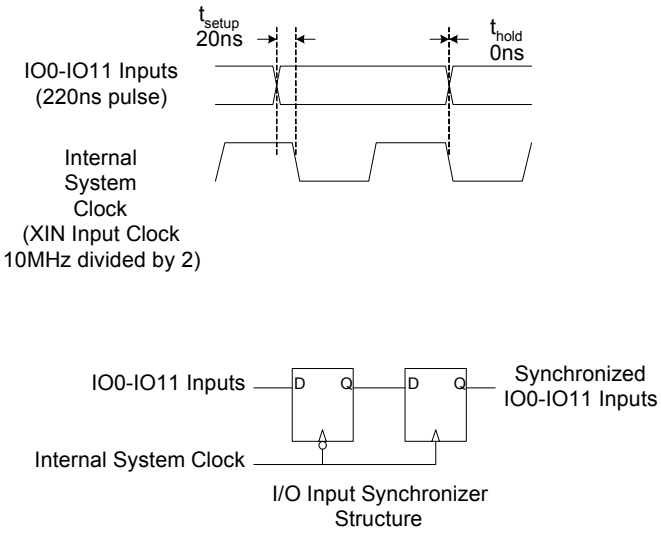


Figure 3.2 Synchronization of External Signals

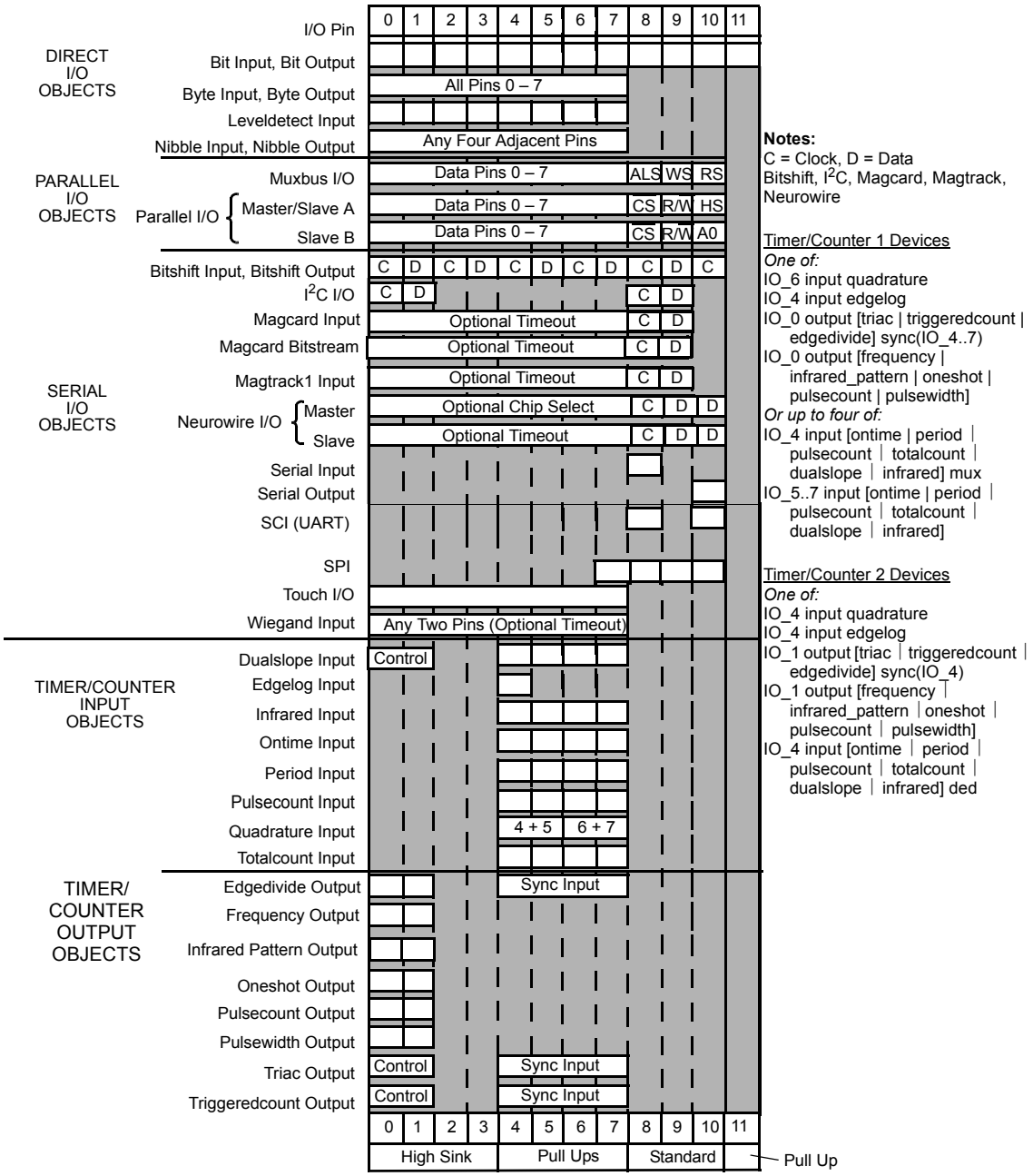


Figure 3.3 Summary of I/O Objects

I/O Timing Issues

The PL Smart Transceiver I/O timing is influenced by four separate, yet overlapping areas of the overall chip architecture:

- The scheduler
- The I/O object's firmware
- The PL Smart Transceiver hardware
- Interrupts

The contribution of the scheduler to the overall timing characteristic is approximately uniform across all I/O function blocks because its contribution to the overall I/O timing is at a relatively high functional level.

The contribution of firmware and hardware varies from one I/O object to another (for example, Bit I/O versus Neurowire I/O).

The contribution of interrupts varies with the nature of the data interrupting the processor. See the SCI (UART) and SPI section for details.

Scheduler-Related I/O Timing Information

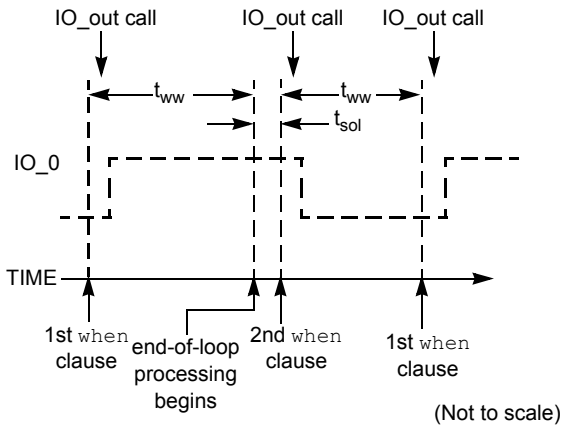
As part of the PL Smart Transceiver firmware, the scheduler provides an orderly and predictable means to facilitate the evaluation of user-defined events. The **`when`** clause, provided by the Neuron C language, is used to specify such events. For more information on the operation of the scheduler, refer to the *Neuron C Programmer's Guide.*

There is a finite latency associated with the operation of the scheduler. The time required for the scheduler to evaluate the same `when` clause in a particular user application code is, to a large extent, a function of the size of the user code, the total number of `when` clauses, and the state of the events associated with those `when` clauses. Therefore, it is impossible to specify a nominal value for this latency, as each application will have its own distinct behavior under different circumstances.

The best case latency can be viewed in several ways, each exposing a different aspect of the scheduler operation. A simple example consists of having an application program consisting of two `when` clauses, both of which always evaluate to TRUE, as shown below.

```
IO_0 output bit testbit;
when (TRUE) {
    io_out(testbit, 1);
}
when (TRUE) {
    io_out (testbit, 0);
}
```

Processing of `when` clauses is done in a round-robin fashion; therefore, the Neuron C code above performs alternating activation of the IO0 pin in order to isolate and extract the timing parameters associated with the scheduler. The waveform seen on pin IO0 of the PL Smart Transceiver, as a result of the above code, is shown in Figure 3.4.



Symbol	Description	Typ @ 10MHz
t_{ww}	when-clause to when-clause latency	940 µs
t_{sol}	Scheduler overhead latency (see text)	54 µs

Figure 3.4 when-Clause to when-Clause and Scheduler Overhead Latency

The when-clause to when-clause latency, t_{ww}, in this case includes the execution time of one io_out() function (65 µs latency at 10MHz) and is for an event that always evaluates to TRUE. The actual t_{ww} for a given application is driven by the actual task within the when statement as well as the when event which is evaluated.

The above example not only measures the best-case minimum latency between consecutive when clauses (whose events evaluate to TRUE), t_{ww}, but also reveals the scheduler's end-of-loop overhead latency, t_{sol}. As shown in Figure 3.4, t_{ww} is the off-time period of the output waveform and t_{sol} is the on-time of the output waveform, minus t_{ww}. This shows that the scheduler overhead latency, or the scheduler end-of-loop latency, occurs just before the execution of the last when clause in the program.

The latency associated with the return from the io_out() function is small, relative to that of the execution of the function call itself.

Note: Some I/O objects suspend application processing until the task is complete. This is because they are firmware-driven. These are bitshift, Neurowire, parallel, software serial I/O objects, I^2C, magcard, magtrack, Touch I/O, and Wiegand. They do not suspend network communication as this is handled by the network processor and the media access processor.

Firmware and Hardware Related I/O Timing Information

All I/O updates in the PL Smart Transceiver are performed by the Neuron firmware using system image function calls.

The total latency for a given function call, from start to end, can be broken down into two separate parts. The first is due to the processing time required before the actual hardware I/O update (read or write) occurs. The second delay is associated with the time required to finish the current function call and return to the application program.

Overall accuracy is always related to the accuracy of the XIN input of the PL Smart Transceiver. Timing diagrams are provided for all non-trivial cases to clarify the parameters given.

For more information on the operation of each of the I/O objects, refer to the *Neuron C Reference Guide.*

Direct I/O Objects

The timing numbers shown in this section are valid for both an explicit I/O call or an implicit I/O call through a **`when`** clause, and are assumed to be for a PL Smart Transceiver running at 10MHz.

Bit Input/Output

Pins IO0 – IO11 can be individually configured as single-bit input or output ports. Inputs can be used to sense TTL-level compatible logic signals from external logic, contact closures, and the like. Outputs can be used to drive external CMOS and TTL level compatible logic, switch transistors and very low current relays to actuate higher-current external devices such as stepper motors and lights. The high (20mA) current sink capability of pins IO0 – IO3 allows these pins to drive many I/O devices directly (refer to Figure 3.5). Figures 3.6 and 3.7 show the bit input and bit output latency times, respectively. These are the times from which `io_in()` or `io_out()` is called, until a value is returned. The direction of bit ports can be changed between input and output dynamically under application control. (`io_set_direction()`)

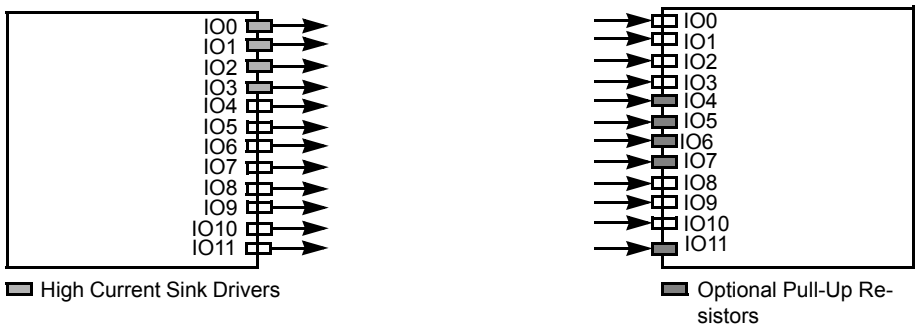
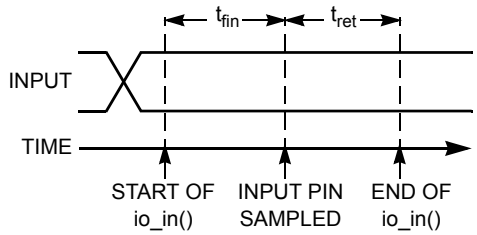


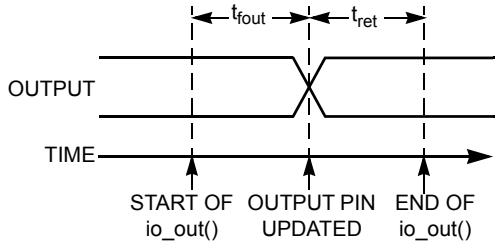
Figure 3.5 Bit I/O

***Note*:** After a reset, the PL Smart Transceiver disables the IO4-IO7 and IO11 pull-up resistors. The pull-up resistors are not turned on until application initialization. Pull-ups are only enabled when specified in the application configuration using a Neuron C directive (`#pragma enable_io_pullups`).



Symbol	Description	Typ @ 10MHz
t_{fin}	Function call to sample	
	IO0 – IO10	41 µs
	IO11	8.4µs
t_{ret}	Return from function	
	IO0	19 µs
	IO1	23.4 µs
	IO2	27.9 µs
	IO3	32.3 µs
	IO4	36.7 µs
	IO5	41.2 µs
	IO6	45.6 µs
	IO7	50 µs
	IO8	19 µs
	IO9	23.4 µs
	IO10	27.9 µs
	IO11	7.8 µs

Figure 3.6 Bit Input Latency Values



Symbol	Description	Typ @ 10MHz
t_{fout}	Function call to update	
	IO3 – IO5, IO11	69 µs
	All others	60 µs
t_{ret}	Return from function	
	IO0 – IO11	5 µs

Figure 3.7 Bit Output Latency Values

Byte Input/Output

Pins IO0 – IO7 can be configured as a byte-wide input or output port, which can be read or written using integers in the range 0 to 255. This is useful for driving devices that require ASCII data, or other data, eight bits at a time. For example, an alphanumeric display panel can use byte function for data, and use pins IO8 – IO11 in bit function for control and addressing. See Figures 3.8, 3.9, and 3.10. IO0 represents the LSB of data. The direction of a byte port can be changed between input and output dynamically under application control. (`io_set_direction()`)

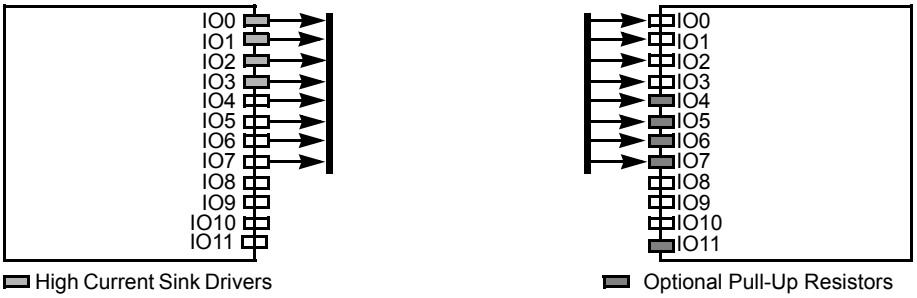
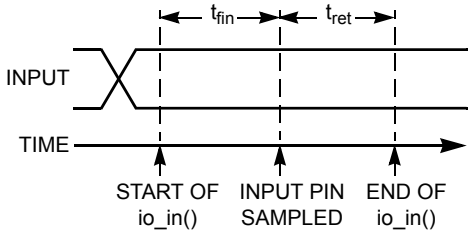
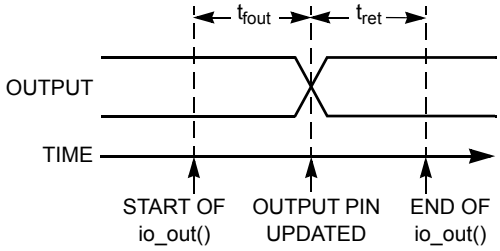


Figure 3.8 Byte I/O



Symbol	Description	Typ @ 10MHz
t_{fin}	Function call to input sample	24 µs
t_{ret}	Return from function	4 µs

Figure 3.9 Byte Input Latency Values

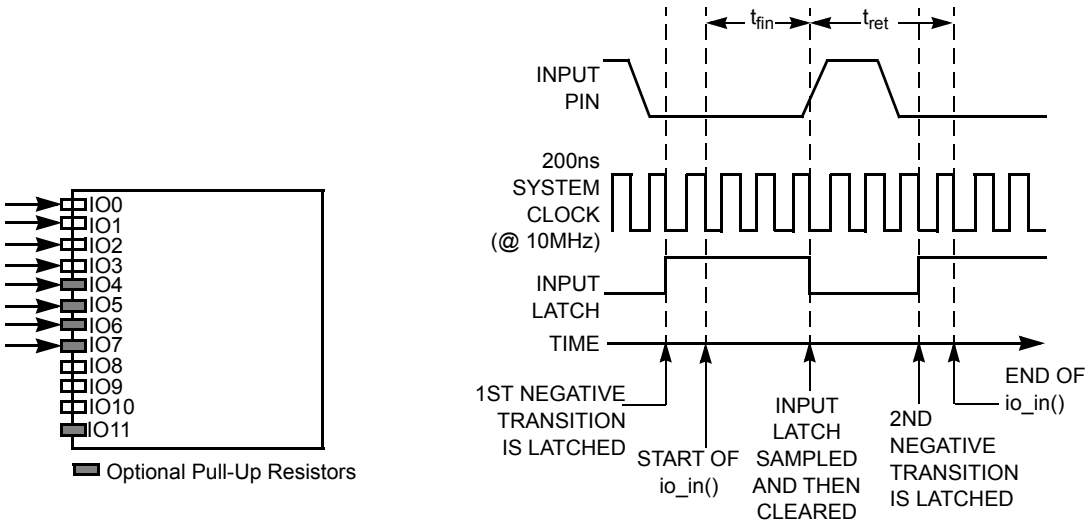


Symbol	Description	Typ @ 10MHz
t_{fout}	Function call to update	57 µs
t_{ret}	Return from function	5 µs

Figure 3.10 Byte Output Latency Values

Leveldetect Input

Pins IO0 – IO7 can be individually configured as leveldetect input pins, which latch a negative-going transition of the input level with a minimal low pulse width of 200ns, with a PL Smart Transceiver clocked at 10MHz. The application can therefore detect short pulses on the input which might be missed by software polling. This is useful for reading devices, such as proximity sensors. **This is the only direct I/O object which is latched before it is sampled.** The latch is cleared during the `when` statement sampling and can be set again immediately after, if another transition should occur (see Figure 3.11).



Symbol	Description	Typ @ 10MHz
t_{fin}	Function call to sample	
	IO0	35 µs
	IO1	39.4 µs
	IO2	43.9 µs
	IO3	48.3 µs
	IO4	52.7 µs
	IO5	57.2 µs
	IO6	61.6 µs
	IO7	66 µs
t_{ret}	Return from function	32 µs

Figure 3.11 Leveldetect Input Latency Values

Nibble Input/Output

Groups of four consecutive pins between IO0 – IO7 can be configured as nibble-wide input or output ports, which can be read or written to using integers in the range 0 to 15. This is useful for driving devices that require BCD data, or other data four bits at a time. For example, a 4x4 key switch matrix can be scanned by using one nibble to generate an output (row select — one of four rows), and one nibble to read the input from the columns of the switch matrix. See Figures 3.12, 3.13, and 3.14.

The direction of nibble ports can be changed between input and output dynamically under application control (see the *Neuron C Programmer's Guide*). The LSB of the input data is determined by the object declaration and can be any of the IO0 – IO4 pins.

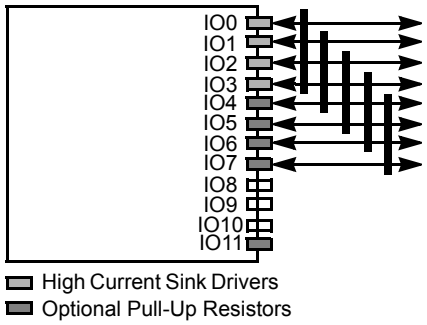
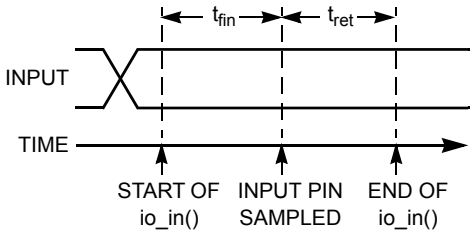
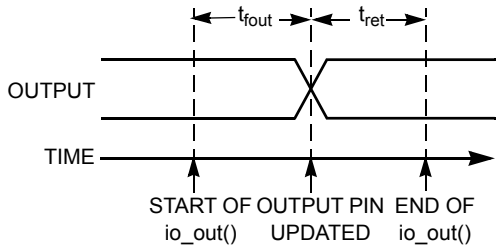


Figure 3.12 Nibble I/O



Symbol	Description	Typ @ 10MHz
t_{fin}	Function call to sample IO0 – IO4	41 µs
t_{ret}	Return from function	
	IO0	18 µs
	IO1	22.8 µs
	IO2	27.5 µs
	IO3	32.3 µs
	IO4	37 µs

Figure 3.13 Nibble Input Latency Values



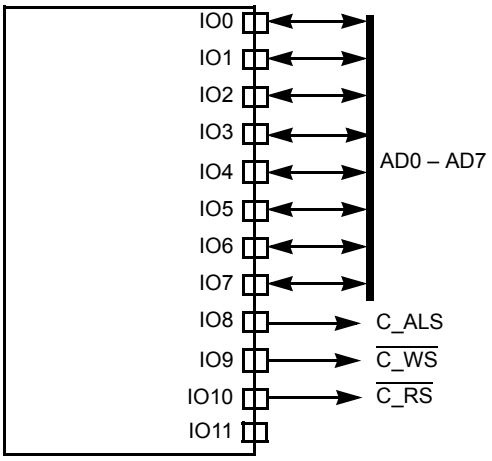
Symbol	Description	Typ @ 10MHz
t_{fout}	Function to update	
	IO0	78 µs
	IO1	89.8 µs
	IO2	101.5 µs
	IO3	113.3 µs
	IO4	125 µs
t_{ret}	Return from function	
	IO0 – IO4	5 µs

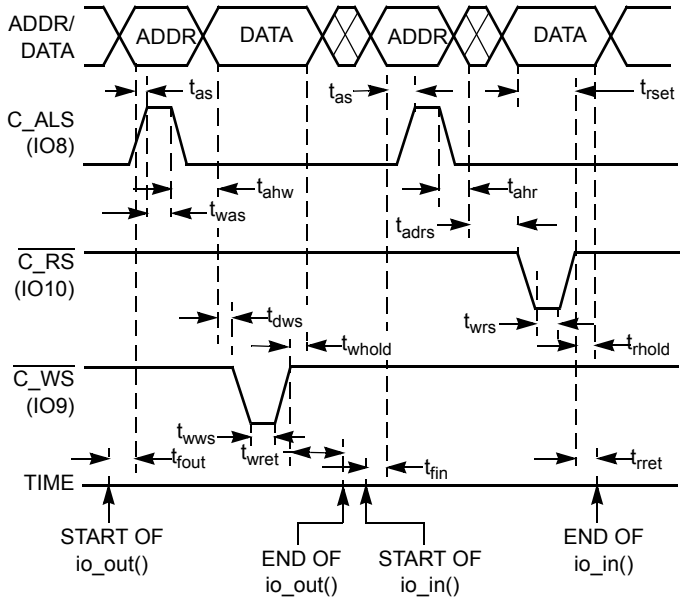
Figure 3.14 Nibble Output Latency Values

Parallel I/O Objects

Muxbus Input/Output

This I/O object provides a means of performing parallel I/O data transfers between the PL Smart Transceiver and an attached peripheral device or processor (see Figure 3.15). Unlike the parallel input/output object, which makes use of a token-passing scheme for ensuring synchronization, the muxbus input/output enables the PL Smart Transceiver to essentially be in control of all read and write operations at all times. This relieves the burden of protocol handling from the attached device and results in an easier-to-use interface at the expense of data throughput capacity. The data bus remains in the last state used.





NOTE: Data is latched 4.8 µs after the falling edge of $\overline{C\_RS}$.

Symbol	Description	Min	Typ	Max
t_{fout}	`io_out()` to valid address	—	26.4 µs	—
t_{as}	Address valid to address strobe	—	10.8 µs	—
t_{ahw}	Address hold for write	—	4.8 µs	—
t_{ahr}	Address hold for read	—	6.6 µs	—
t_{was}	Address strobe width	—	6.6 µs	—
t_{wrs}	Read strobe width	—	10.8 µs	—
t_{wws}	Write strobe width	—	10.8 µs	—
t_{dws}	Data valid to write strobe	—	6.6 µs	—
t_{rset}	Read setup time	10.8 µs	—	—
t_{whold}	Write hold time	4.2 µs	—	—
t_{rhold}	Read hold time	0 µs	—	—
t_{adrs}	Address disable to read strobe	—	7.2 µs	—
t_{fin}	`io_in()` to valid address	—	26.4 µs	—
t_{rret}	Function return from read	—	4.2 µs	—
t_{wret}	Function return from write	—	4.2 µs	—

Figure 3.15 Muxbus I/O Object

Parallel Input/Output

Pins IO0 – IO10 can be configured as a bidirectional 8-bit data and 3-bit control port for connecting to an external processor. The other processor can be a computer, microcontroller, or another PL Smart Transceiver (for gateway applications). The parallel interface can be configured in master, slave A, or slave B mode. Typically, two PL Smart Transceivers interface in master/slave A mode and a PL Smart Transceiver interfaces with another microprocessor in the slave B configuration, with the other microprocessor as the master. Handshaking is used in both modes to control the instruction execution, and application processing is suspended for the duration of the transfer (up to 255 bytes/transfer). Consult the *Neuron C Reference Guide* for detailed programming instructions.

Upon a reset condition, the master processor monitors the low transition of the handshake (HS) line from the slave, then passes a CMD_RESYNC (0x5A) for synchronization purposes. This must be done within 0.84 seconds after reset goes high with a PL Smart Transceiver slave running at 10MHz, to avoid a watchdog reset error condition (see the *Neuron C Programmer's Guide*). The CMD_RESYNC is followed by the slave acknowledging with a CMD_ACKSYNC (0x07). This synchronization ensures that both processors are properly reset before data transfer occurs. When interfacing two PL Smart Transceivers, these characters are passed automatically (refer to the flow table illustrated later in this section). However, when using parallel I/O to interface the PL Smart Transceiver to another microprocessor, that microprocessor must duplicate the interface signals and characters that are automatically generated by the parallel I/O function of the PL Smart Transceiver.

For additional information, see the *Parallel I/O Interface to the Neuron Chip* engineering bulletin.

The timing numbers shown in this section are valid for both an explicit I/O call or an implicit I/O call through a `when` clause, and are assumed to be for a PL Smart Transceiver running at 10MHz.

Master/Slave A Mode

This mode is recommended when interfacing two PL Smart Transceivers. In a master/slave A configuration, the master drives IO8 as a chip select and IO9 to specify a read or write cycle, and the slave drives IO10 as a handshake (HS) acknowledgment (see Figure 3.16). The maximum data transfer rate is 1 byte per 4 processor instruction cycles, or 2.4 µs per byte at a 10MHz input clock rate. The data transfer rate scales proportionally to the input clock rate (a master write is a slave read). Timing for the case where the PL Smart Transceiver is the master (Figure 3.17), refers to measured output timing at 10MHz. After every byte write or byte read, the HS line is monitored by the master, to verify the slave has completed processing (when HS = 0) and the slave is ready for the next byte transfer. This is done automatically in PL Smart Transceiver-to-PL Smart Transceiver (master/slave A mode) data transfers. **The HS line should be pulled up (inactive) with a 10kΩ resistor to ensure proper resynch behavior after the slave resets.** Slave A timing is shown in Figure 3.18.

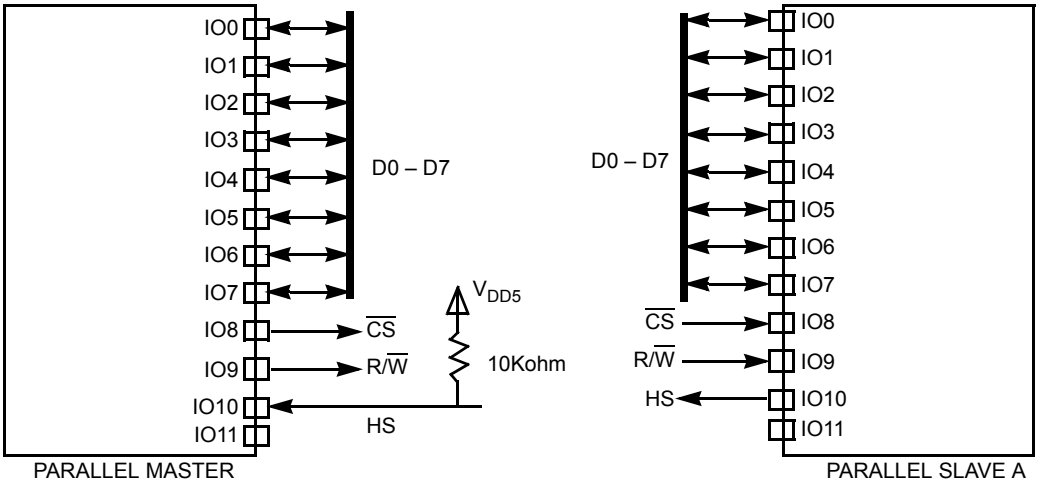
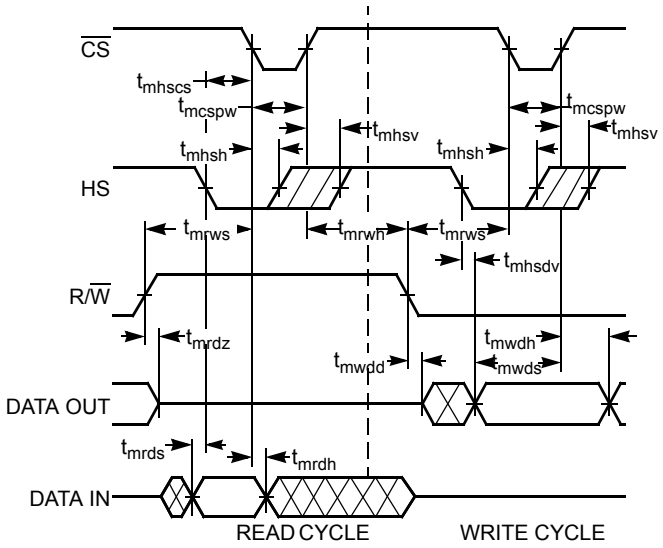


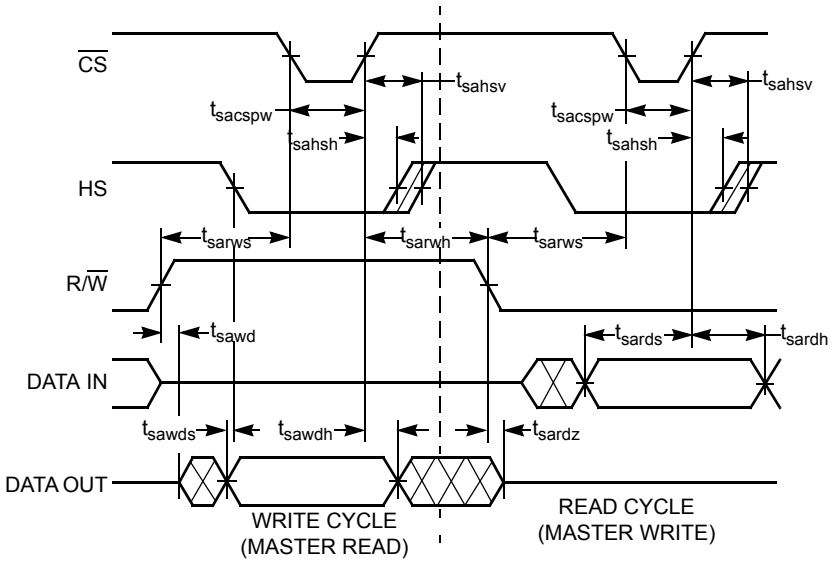
Figure 3.16 Parallel I/O — Master and Slave A



Symbol	Description	Min	Typ	Max
t_{mrws}	R/$\overline{W}$ setup before falling edge of $\overline{CS}$ (Note 6)	150 ns	3 XIN	—
t_{mrwh}	R/$\overline{W}$ hold after rising edge of $\overline{CS}$	100 ns	—	—
t_{mcspw}	$\overline{CS}$ pulse width (Note 6)	150 ns	2 XIN	—
t_{mhsh}	HS hold after falling edge of $\overline{CS}$	0 ns	—	—
t_{mhsv}	HS checked by firmware after rising edge of $\overline{CS}$ (Note 6)	150 ns	10 XIN	—
t_{mrdz}	Master three-state DATA after rising edge of R/$\overline{W}$ (Notes 1, 2)	—	0	25 ns
t_{mrds}	Read data setup before falling edge of HS (Note 3)	0 ns	—	—
t_{mhscs}	HS low to falling edge of $\overline{CS}$ (Notes 4,6)	2 XIN	6 XIN	—
t_{mrdh}	Read data hold after falling edge of $\overline{CS}$	0 ns	—	—
t_{mwdd}	Master drive of DATA after falling edge of R/$\overline{W}$ (Notes 1,6)	150 ns	2 XIN	—
t_{mhsdv}	HS low to data valid (Note 4)	—	50 ns	—
t_{mwds}	Write data setup before rising edge of $\overline{CS}$ (Note 6)	150 ns	2 XIN	—
t_{mwdh}	Write data hold after rising edge of $\overline{CS}$ (Note 5)	Note 5	—	—

Figure 3.17 Master Mode Timing

Notes:
1. Refer to the *PL 3120 and PL 3150 Smart Transceiver Datasheet* for detailed measurement information.
2. For PL Smart Transceiver-to-PL Smart Transceiver operation, bus contention (t_{mrdz}, t_{sawdd}) is eliminated by firmware, ensuring that a zero state is present when the token is passed between the master and slave. See *Parallel I/O Interface to the Neuron Chip* engineering bulletin for further information.
3. HS high is used as a slave busy flag. If HS is held low, the maximum data transfer rate is 24 XIN (2.4µs @ 10MHz) per byte. If HS is not used for a flag, caution should be taken to ensure the master does not initiate a data transfer before the slave is ready.
4. Parameters were added in order to aid interface design with the PL Smart Transceiver.
5. Master will hold output data valid during a write until the Slave device pulls HS high.
6. XIN represents the period of the PL Smart Transceiver input clock (100ns at 10MHz).
7. In a master read, $\overline{CS}$ pulsing low acts like a handshake to flag the slave that data has been latched in.



Symbol	Description	Min	Typ	Max
t_{sarws}	R/$\overline{W}$ setup before falling edge of $\overline{CS}$	25 ns	—	—
t_{sarwh}	R/$\overline{W}$ hold after rising edge of $\overline{CS}$	0 ns	—	—
t_{sacspw}	$\overline{CS}$ pulse width	45 ns	—	—
t_{sahsh}	HS hold after rising edge of $\overline{CS}$	0 ns	—	—
t_{sahsv}	HS valid after rising edge of $\overline{CS}$	—	—	50 ns
t_{sawdd}	Slave A drive of DATA after rising edge of R/$\overline{W}$ (Notes 1, 2)	0 ns	5 ns	—
t_{sawds}	Write data valid before falling edge of HS (Note 4)	150 ns	2 XIN	—
t_{sawdh}	Write data valid after rising edge of $\overline{CS}$ (Note 4)	150 ns (Note 3)	2 XIN	—
t_{sardz}	Slave A three-state DATA after falling edge of R/$\overline{W}$ (Note 1)	—	—	50 ns
t_{sards}	Read data setup before rising edge of $\overline{CS}$	25 ns	—	—
t_{sardh}	Read data hold after rising edge of $\overline{CS}$	10 ns	—	—

Figure 3.18 Slave A Mode Timing

Notes:
1. Refer to the *PL 3120 and PL 3150 Smart Transceiver Datasheet* for detailed measurement information.
2. For PL Smart Transceiver-to-PL Smart Transceiver operation, bus contention (t_{mrdz}, t_{sawdd}) is eliminated by firmware, ensuring that a zero state is present when the token is passed between the master and slave. See *Parallel I/O Interface to the Neuron Chip* engineering bulletin for further information.
3. If $t_{sarwh} < 150$ns, then $t_{sawdh} = t_{sarwh}$.
4. XIN represents the period of the PL Smart Transceiver input clock (100ns at 10MHz).
5. In slave A mode, the HS signal is high a minimum of 4 XIN periods. The typical time HS is high during consecutive data reads or consecutive data writes is also 4 XIN periods.

Slave B Mode

The slave B mode is recommended for interfacing a PL Smart Transceiver acting as the slave to another microprocessor acting as the master. When configured in slave B mode, the PL Smart Transceiver accepts IO8 as a chip select and IO9 to specify whether the master will read or write, and accepts IO10 as a register select input. When $\overline{CS}$ is asserted and either IO10 is low or IO10 is high and R/$\overline{W}$ is low, pins IO0 – IO7 form the bidirectional data bus. When IO10 is high, R/$\overline{W}$ is high, and $\overline{CS}$ is asserted, IO0 is driven as the HS acknowledgment signal to the master.

The PL Smart Transceiver can appear as two registers in the master's address space; one of the registers being the read/write data register, and the other being the read-only status register. Therefore, reads by the master to an odd address access the status register for handshaking acknowledgments and all other reads or writes access the data register for I/O transfers. The LSB of the control register, which is read through pin IO0, is the HS bit. The master reads the HS bit after every master read or write. **The D0/HS line should be pulled up (inactive) with a 10kΩ resistor to ensure proper resynch behavior after resets.**

When acting as a slave to a different microprocessor, the PL Smart Transceiver slave B mode handles all handshaking and token passing automatically. However, the master microprocessor must read the HS bit after each transaction and must also internally track the token passing. This mode is designed for use with a master processor that uses memory-mapped I/O, as the LSB of the master's address bus is typically connected to the IO10 pin of the PL Smart Transceiver. This is illustrated in Figures 3.19 and 3.20.

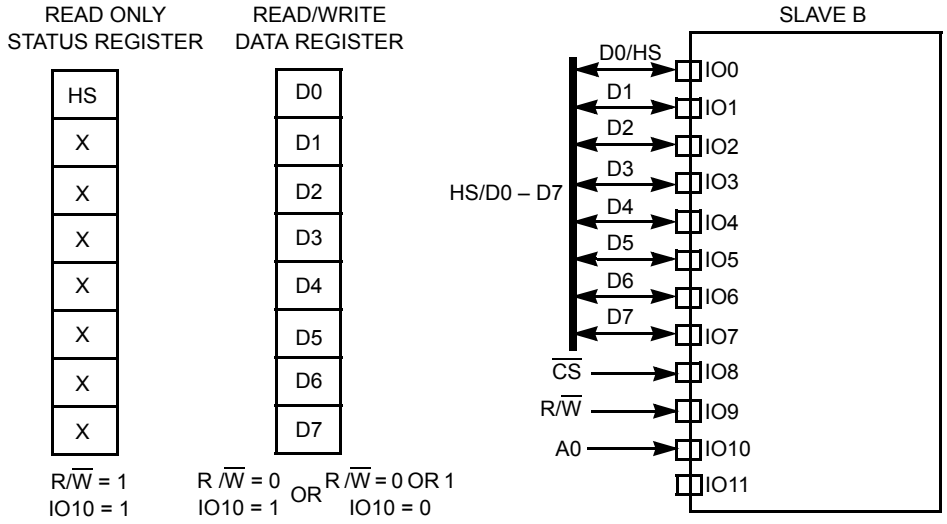
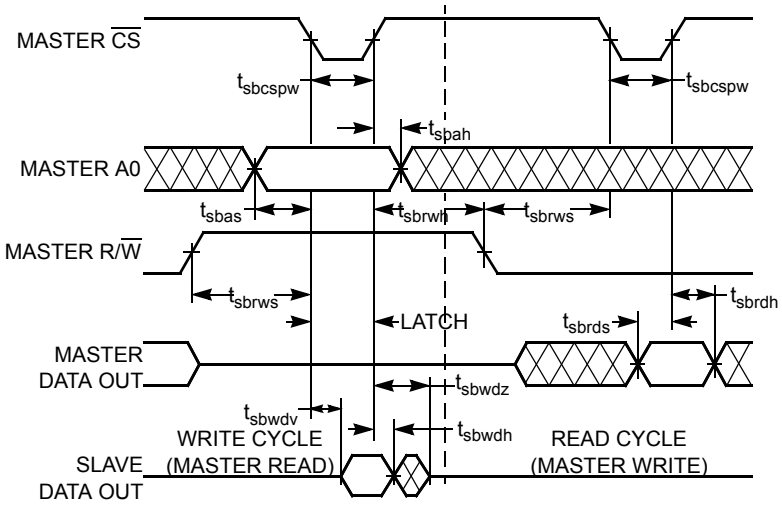


Figure 3.19 Parallel I/O Master/Slave B (PL Smart Transceiver as Memory-Mapped I/O Device)



Symbol	Description	Min	Typ	Max
t_{sbrws}	R/$\overline{W}$ setup before falling edge of $\overline{CS}$ PL 3150 and PL 3120 Smart Transceivers	0 ns	—	—
t_{sbrwh}	R/$\overline{W}$ hold after rising edge of $\overline{CS}$	0 ns	—	—
t_{sbcspw}	$\overline{CS}$ pulse width	Note 1	—	—
t_{sbas}	A0 setup to falling edge of $\overline{CS}$	10 ns	—	—
t_{sbah}	A0 hold after rising edge of $\overline{CS}$	0 ns	—	—
t_{sbwdv}	$\overline{CS}$ to write data valid	—	—	50 ns
t_{sbwdh}	Write data hold after rising edge of $\overline{CS}$ (Notes 2, 3)	0 ns	30 ns	—
t_{sbwdz}	$\overline{CS}$ rising edge to Slave B release data bus (Note 2)	—	—	50 ns
t_{sbrds}	Read data setup before rising edge of $\overline{CS}$	25 ns	—	—
t_{sbrdh}	Read data hold after rising edge of $\overline{CS}$	10 ns	—	—

Figure 3.20 Slave B Mode Timing

***Notes*:**

1. The slave B write cycle (master read) $\overline{CS}$ pulse width is directly related to the slave B write data valid parameter and master read setup parameter. To calculate the write cycle $\overline{CS}$ duration needed for a special application use:
   $t_{sbcspw} = t_{sbwdv}$ + master's read data setup before rising edge of $\overline{CS}$
   Refer to the master's specification data book for the master read setup parameter. The slave read cycle minimum $\overline{CS}$ pulse width = 50 ns.
2. Refer to the *PL 3120 and PL 3150 Smart Transceiver Datasheet* for detailed measurement information.
3. The data hold parameter, t_{sbwdh}, is measured to the disable levels shown in the *PL 3120 and PL 3150 Smart Transceiver Datasheet*, rather than to the traditional data invalid levels.
4. In a slave B write cycle the timing parameters are the same for a control register (HS) write as for a data write.
5. Special applications: Both the state of $\overline{CS}$ and R/$\overline{W}$ determine a slave B write cycle. If $\overline{CS}$ can not be used for a data transfer, then toggling the R/$\overline{W}$ line can be used with no changes to the hardware. In other words, if $\overline{CS}$ is held low during a slave B write cycle, a positive pulse (low to high to low) on R/$\overline{W}$ can execute a data transfer. The low to high transition on R/$\overline{W}$ causes slave B to drive data with the same timing parameters as t_{sbwdv} (redefined R/$\overline{W}$ to write data valid). Likewise, the falling edge of R/$\overline{W}$ causes slave B to release the data bus with the same timing limits as the $\overline{CS}$ rising edge in t_{sbwdz}. This scenario is only true for a slave B write cycle and is not applicable to a slave B read cycle or any slave A data transitions. This application can be helpful if the master has separate read and write signals but no $\overline{CS}$ signal. Caution must be taken to ensure the bus is free before transfers to avoid bus contention.

Serial I/O Objects

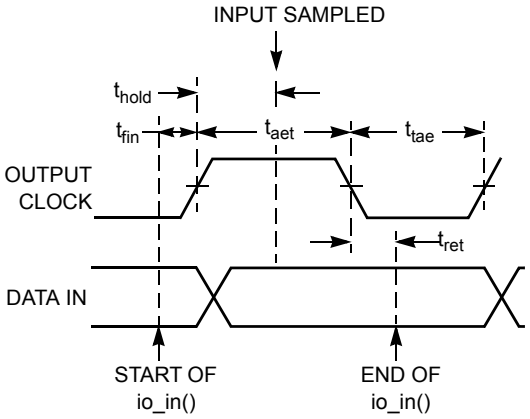
The timing numbers shown in this section are valid for both an explicit I/O call or an implicit I/O call through a **`when`** clause, and are assumed to be for a PL Smart Transceiver running at 10MHz.

Bitshift Input/Output

Pairs of adjacent pins can be configured as serial input or output lines. The first pin of the pair can be IO0-IO6, IO8, or IO9, and is used for the clock (driven by the PL Smart Transceiver). The adjacent higher-numbered I/O pin is then used for up to 16 bits of serial data. The bit rate can be configured as 1kbps, 10kbps, or 15kbps at a 10MHz input clock rate. The bit rate scales proportionally to the input clock rate. The active clock edge can be specified as either rising or falling. This object is useful for transferring data to external logic employing shift registers. This function suspends application processing until the operation is complete (see Figures 3.21, 3.22, and 3.23).

Figure 3.21 Bitshift I/O Examples

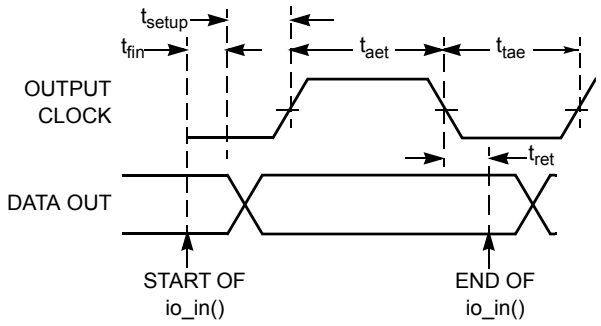
For bitshift input, the clock output is deasserted (to the inactive level) at the same time as the start of the first bit of data. For bitshift output, the clock output is initially inactive prior to the first bit of data (unless overridden by a bit output overlay).



Active clock edge assumed to be positive in the above diagram

Symbol	Description	Typ @ 10MHz
t_{fin}	Function call to first edge	156.6 µs
t_{ret}	Return from function	5.4 µs
t_{hold}	Active clock edge to sampling of input data 15 kbps bit rate 10 kbps bit rate 1 kbps bit rate	 9 µs 40.8 µs 938.2 µs
t_{aet}	Active clock edge to next clock transition 15 kbps bit rate 10 kbps bit rate 1 kbps bit rate	 31.8 µs 63.6 µs 961 µs
t_{tae}	Clock transition to next active clock edge 15 kbps bit rate 10 kbps bit rate 1 kbps bit rate	 14.4 µs 14.4 µs 14.4 µs
f	Clock frequency = $1/(t_{aet} + t_{tae})$ 15 kbps bit rate 10 kbps bit rate 1 kbps bit rate	 21.6 kHz 12.8 kHz 1.03 kHz

Figure 3.22 Bitshift Input Latency Values



Active clock edge assumed to be positive in the above diagram

Symbol	Description	Typ @ 10MHz
t_{fin}	Function call to first data out stable	
	16-bit shift count	185.3 µs
	1-bit shift count	337.6 µs
t_{ret}	Return from function	10.8 µs
t_{setup}	Data out stable to active clock edge	
	15 kbps bit rate	10.8 µs
	10 kbps bit rate	10.8 µs
	1 kbps bit rate	10.8 µs
t_{aet}	Active clock edge to next clock transition	
	15 kbps bit rate	10.2 µs
	10 kbps bit rate	42 µs
	1 kbps bit rate	939.5 µs
t_{tae}	Clock transition to next active clock edge	
	15 kbps bit rate	34.8 µs
	10 kbps bit rate	34.8 µs
	1 kbps bit rate	34.8 µs
f	Clock frequency = $1/(t_{aet} + t_{tae})$	
	15 kbps bit rate	22 kHz
	10 kbps bit rate	13 kHz
	1 kbps bit rate	1.02 kHz

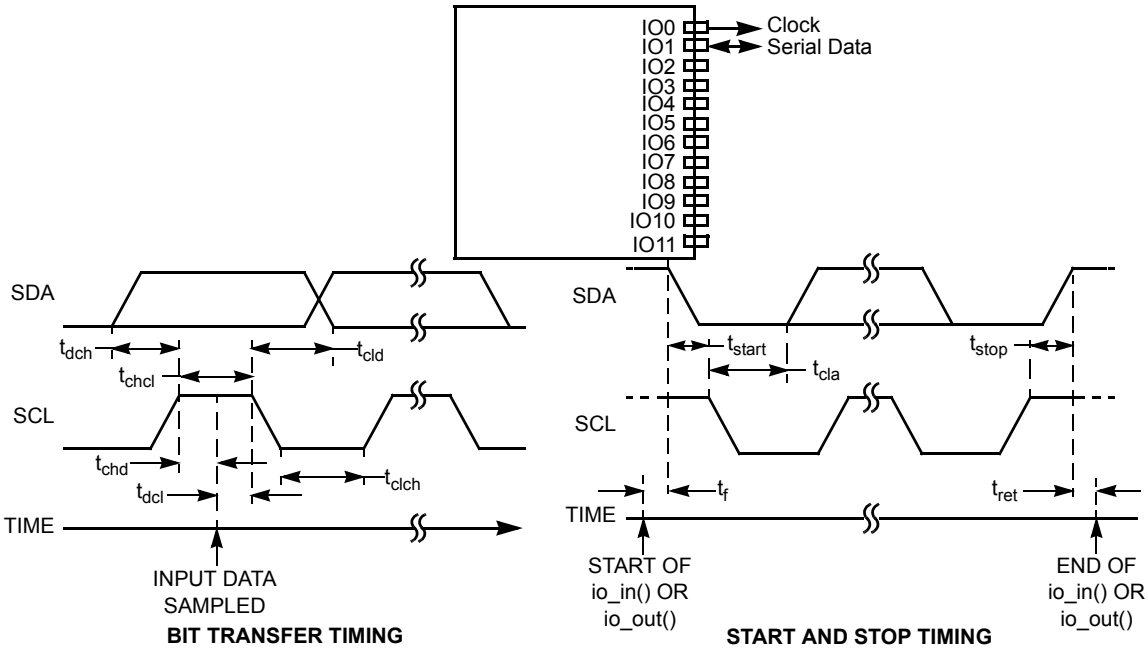
Figure 3.23 Bitshift Output Latency Values

I²C Input/Output

This I/O object is used to interface the PL Smart Transceiver to any device which adheres to Philips Semiconductor's Inter-Integrated Circuit (I^2C) bus protocol. The PL Smart Transceiver is always the master, with IO8 being the serial clock (SCL) and IO9 the serial data (SDA). Alternatively, IO0 can be used as the serial clock (SCL) and IO1 as the serial data (SDA). These I/O lines are operated in the open-drain mode in order to accommodate the special requirements of the I^2C protocol. With the exception of two pull-up resistors, no additional external components are necessary for interfacing the PL Smart Transceiver to an I^2C device.

Up to 255 bytes of data can be transferred at a time. At the start of all transfers, a right-justified 7-bit I^2C address argument is sent out on the bus immediately after the I^2C "start condition."

For more information on this protocol, refer to Philips Semiconductor's I^2C documentation.



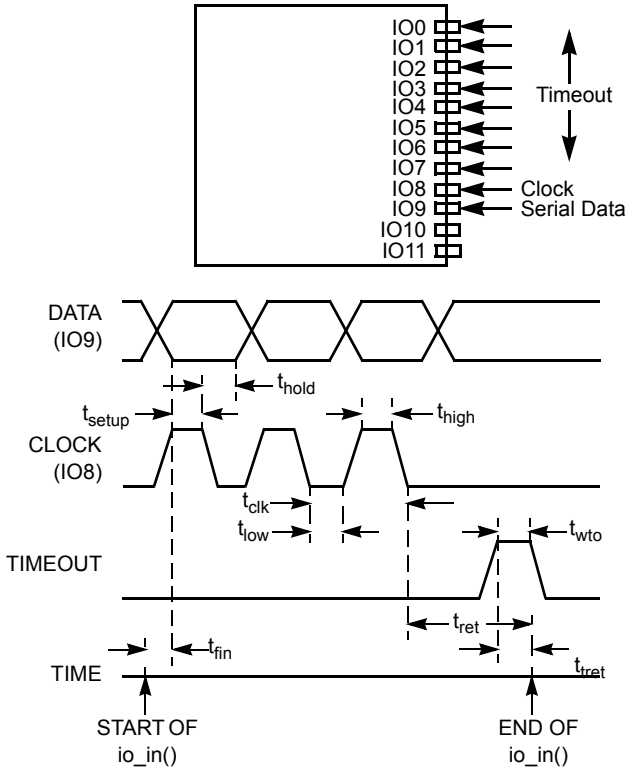
Parameter	Description	Min	Typ	Max
t_f	I/O call to start condition			
	`io_in()`	—	54.6 µs	—
	`io_out()`	—	43.4 µs	—
t_{start}	End of start condition			
	`io_in()`	5.4 µs	—	—
	`io_out()`	5.4 µs	—	—
t_{cla}	End of start to start of address			
	`io_in()`	24.0 µs	—	—
	`io_out()`	24.0 µs	—	—
t_{cld}	SCL low to data for `io_out()`	24.6 µs	—	—
t_{dch}	Data to SCL high for `io_out()`	7.2 µs	—	—
t_{chcl}	Clock high to clock low for `io_out()`	12.6 µs	—	—
t_{chd}	SCL high to data sampling for `io_in()`	13.2 µs	—	—
t_{dcl}	Data sample to SCL low for `io_in()`	7.2 µs	—	—
t_{clch}	Clock low to clock high for `io_in()`	24.0 µs	—	—
t_{stop}	Clock high to data			
	`io_in()`	12.6 µs	—	—
	`io_out()`	12.6 µs	—	—
t_{ret}	SDA high to return from function			
	`io_in()`	—	—	4.2 µs
	`io_out()`	—	—	4.2 µs

Figure 3.24 I^2C I/O Object

Magcard Input

This I/O object is used to transfer synchronous serial data from an ISO 7811 Track 2 magnetic stripe card reader in real time. The data is presented as a data signal input on pin IO9, and a clock, or a data strobe, signal input on pin IO8. The data on pin IO9 is clocked on or just following the falling (negative) edge of the clock signal on IO8, with the LSB first. In addition, any one of the pins IO0 – IO7 can be used as a timeout pin to prevent lockup in case of abnormal abort of the input bit stream during the input process.

Up to 40 characters can be read at one time. Both the parity and the Longitudinal Redundancy Check (LRC) are checked by the PL Smart Transceiver.



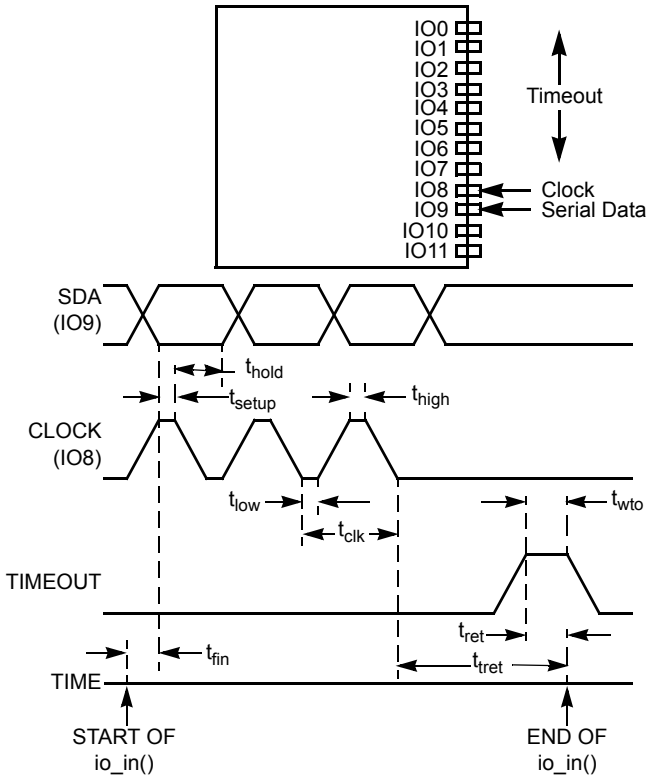
Symbol	Description	Min	Typ	Max
t_{fin}	Function call to first clock input	—	45.0 µs	—
t_{hold}	Data hold	0 µs	—	—
t_{setup}	Data setup	0 µs	—	—
t_{low}	Clock low width	60 µs	—	—
t_{high}	Clock high width	60 µs	—	—
t_{wto}	Width of timeout pulse	60 µs	—	—
t_{clk}	Clock period	120 µs	—	—
t_{tret}	Return from timeout	21.6 µs	—	81.6 µs
t_{ret}	Return from function	—	—	301.8 µs

Figure 3.25 Magcard Input Object

A PL Smart Transceiver operating at 10MHz can process a bit rate at up to 8334 bits/second (of a bit density of 75 bits/inch). This equates to a card velocity of 111 inches/second. Most magnetic card stripes contain a 15-bit sequence of zero data at the start of the card, allowing time for the application to start the card reading function. At 8334 bits/second, this period is about 1.8ms. If the scheduler latency is greater than the 1.8ms value, the `io_in()` function will miss the front end of the data stream. The bit rate processing capability scales with input clock rate.

Magtrack1 Input

This input object type is used to read synchronous serial data from an ISO3554 magnetic stripe card reader. The data input is on pin IO9, and the clock, or data strobe, is presented as input on pin IO8. The data on pin IO9 is clocked in just following the falling edge of the clock signal on IO7, with the LSB first.



Symbol	Description	Min	Typ	Max
t_{fin}	Function call to first clock input	—	45.0 µs	—
t_{hold}	Data hold	t_{low}	—	t_{clk}
t_{setup}	Data setup	0 µs	—	—
t_{low}	Clock low width	31 µs	—	—
t_{high}	Clock high width	31 µs	—	—
t_{wto}	Width of timeout pulse	60 µs	—	—
t_{clk}	Clock period	138 µs	—	—
t_{tret}	Return from timeout	21.6 µs	—	81.6 µs
t_{ret}	Return from function	—	—	301.8 µs

Figure 3.26 Magtrack1 Input Object

The minimum period for the entire bit cycle (t_{clk}) is greater than the sum of t_{low} and t_{high}. The t_{setup} and t_{hold} times should be such that the data is stable for the duration of t_{low}.

Data are recognized in the IATA format as a series of 6-bit characters plus an even parity bit per character. The process begins when the start sentinel (hex 05) is recognized, and continues until the end sentinel (0x0F) is recognized. No more than 79 characters, including the 2 sentinels and the LRC character, will be read. The data is stored as right-justified bytes in the buffer space pointed to by the buffer pointer argument in the `io_in()` function with the parity stripped, and includes the start and end sentinels. This buffer should be 78 bytes long.

The magtrack1 input object optionally uses one of the I/O pins IO0 – IO7 as a timeout/abort pin. Use of this feature is suggested because the `io_in()` function will update the watchdog timer during clock wait states, and could result in a lockup if the card were to stop moving in the middle of the transfer process. If a logic 1 level is detected on the I/O timeout pin, the `io_in()` function will abort. This input can be a oneshot timer counter output, an R/C circuit, or a $\overline{\text{DATA\_VALID}}$ signal from the card reader.

A PL Smart Transceiver with a clock rate of 10MHz can process an incoming bit rate of up to 7246 bits/second when the strobe signal has a 1/3 duty cycle (t_{high} = 46µs, t_{low} = 92µs). At a bit density of 210 bits/inch, this translates to a card speed of 34.5 inches/second. The bit rate processing capability scales with PL Smart Transceiver input clock rate.

Magcard Bitstream Input

A **magcard_bitstream** I/O object provides the ability to read unprocessed serial data streams from most magnetic stripe card readers in real time. This function can be used to read magnetic card data in either direction, forward or reverse, because the data does not need to follow any specific format.

This I/O object can read up to 65,535 bits of data, stored in 8192 bytes of data, from a magnetic stripe card reader.

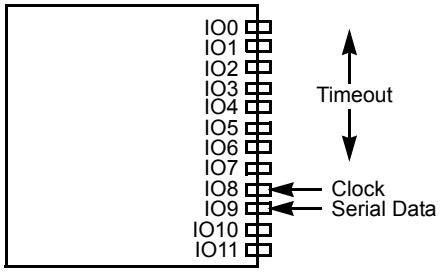


Figure 3.27 Magcard Bitstream Input

Neurowire Input/Output Object

The Neurowire object implements a full-duplex synchronous transfer of data to some peripheral device. It can operate as the master (drive a clock out) or as the slave (accept a clock in). In both master and slave modes, up to 255 bits of data can be transferred at a time. The Neurowire I/O suspends application processing until the operation is completed. The Neurowire object is useful for external devices, such as A/D, D/A converters, and display drivers incorporating serial interfaces that conform with Motorola's SPI or National Semiconductor MICROWIRE™ interface.

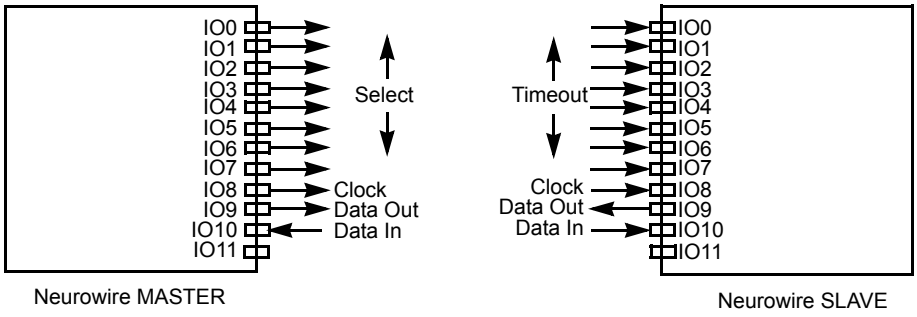
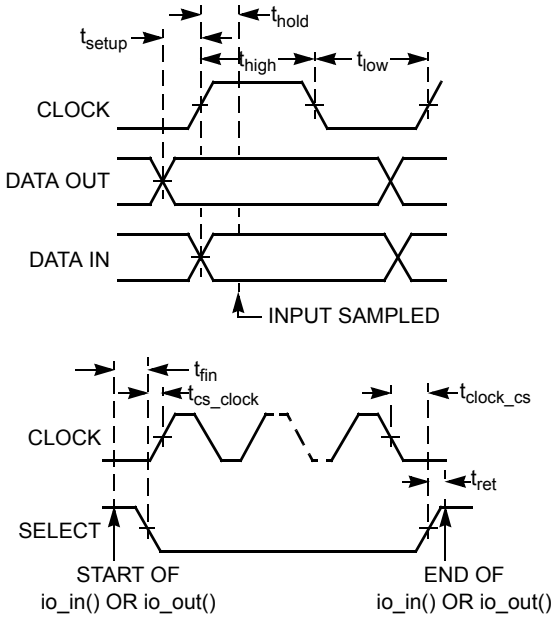


Figure 3.28 Neurowire Input/Output

Neurowire Master Mode

The Neurowire master mode I/O object is still provided for legacy support. Echelon recommends using the hardware SPI instead of the legacy software I/O object (See the *SPI Input/Output* section later in this manual). The hardware SPI provides much higher performance with lower software overhead.

In Neurowire master mode, pin IO8 is the clock (driven by the PL Smart Transceiver), IO9 is the serial data output, and IO10 is the serial data input. Serial data is clocked out on pin IO9 at the same time as data is clocked in from pin IO10. Data is clocked by the rising edge of the clock signal by default. The *clockedge* keyword changes the active edge of the clock to negative. In addition, one or more of the IO0 – IO7 pins can be used as a chip select, allowing multiple Neurowire devices to be connected on a three-wire bus. The clock rate can be specified as 1kbps, 10kbps, or 20kbps at an input clock rate of 10MHz; these scale proportionally with input clock (see Figure 3.29).



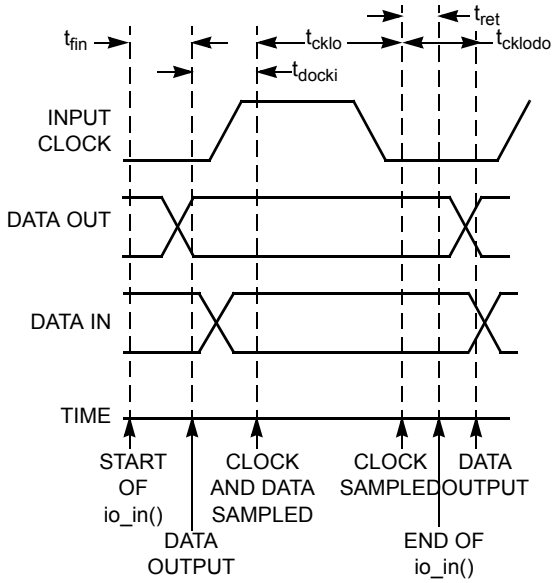
Parameter	Description	Typ
t_{fin}	Function call to $\overline{CS}$ active	69.9 µs
t_{ret}	Return from function	7.2 µs
t_{hold}	Active clock edge to sampling of input data 20 kbps bit rate 10 kbps bit rate 1 kbps bit rate	 11.4 µs 53.4 µs 960.6 µs
t_{high}	Period, clock high (active clock edge = 1) 20 kbps bit rate 10 kbps bit rate 1 kbps bit rate	 25.8 µs 67.8 µs 975.0 µs
t_{low}	Period, clock low (active clock edge = 1)	33.0 µs
t_{setup}	Data output stable to active clock edge	5.4 µs
t_{cs_clock}	Select active to first active clock edge	91.2 µs
t_{clock_cs}	Last clock transition to select inactive	81.6 µs
f	Clock frequency = $1/(t_{high} + t_{low})$ 20 kbps bit rate 10 kbps bit rate 1 kbps bit rate	 17.0 kHz 9.92 kHz 992 Hz

Figure 3.29 Neurowire Master Timing

Neurowire Slave Mode

The Neurowire slave mode I/O object is still provided for legacy support. Echelon recommends using the hardware SPI instead of the legacy software I/O object (See SPI Input/Output section). The hardware SPI provides much higher performance with lower software overhead.

In Neurowire slave mode, pin IO8 is the clock (driven by the external master), IO9 is the serial data output, and IO10 is the serial data input. Serial data is clocked out on pin IO9 at the same time as data is clocked in from pin IO10. Data is clocked by the rising edge of the clock signal (default), which can be up to 18kbps at 10MHz. This data rate scales with PL Smart Transceiver input clock rate. The **`invert`** keyword changes the active clock edge to negative. One of the IO0 – IO7 pins can be designated as a timeout pin. A logic 1 level on the timeout pin causes the Neurowire slave I/O operation to be terminated before the specified number of bits has been transferred. This prevents the PL Smart Transceiver watchdog timer from resetting the chip in the event that fewer than the requested number of bits are transferred by the external clock (see Figure 3.30).



Parameter	Description	Typ
t_{fin}	Function call to data bit out	41.4 µs
t_{ret}	Return from function	19.2 µs
t_{docki}	Data out to input clock and data sampled	4.8 µs
t_{cklo}	Data sampled to clock low sampled	24.0 µs
t_{cklodo}	Clock low sampled to data output	25.8 µs
f	Clock frequency (max)	18.31 kHz

Figure 3.30 Neurowire Slave Timing

The algorithm for each bit of output/input for the Neurowire slave objects is described below. In this description, the default active clock edge (positive) is assumed; if the `invert` keyword is used, all clock levels stated should be reversed.

1. Set IO9 to the next output bit value.
2. Test pin IO8, the clock input, for a high level. This is the test for the rising edge of the input clock. If the input clock is still low, sample the timeout event pin and abort if high.
3. When the input clock is high, store the next data input bit as sampled on pin IO10.

4. Test the input clock for a low input level. This is the test for the falling edge of the input clock. If the input clock is still high, sample the timeout event pin and abort if high.
5. When the input clock is low, return to step 1 if there are more bits to be processed.
6. Else return the number of bits processed.

When either clock input test fails (that is, the clock is sampled *before* the next transition), there is an additional timeout check time of 19.8µs (wait for clock high) or 19.2µs (wait for clock low) added to that stage of the algorithm.

The chip select logic for the Neurowire slave can be handled by the user through a separate bit input object, along with an appropriate handshaking algorithm implemented by the user application program. In order to prevent unnecessary timeouts, the setup and hold times of the chip select line, relative to the start and end of the external clock, must be satisfied.

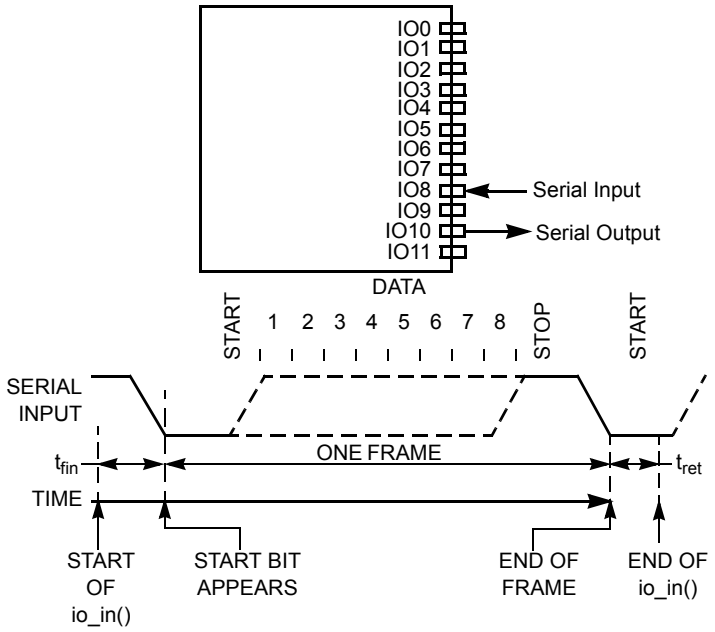
The timeout input pin can either be connected to an external timer or to an output pin of the PL Smart Transceiver that is declared as a oneshot object.

Serial Input/Output

The Serial I/O object is still provided for legacy support. Echelon recommends using the SCI (UART) instead of the legacy software I/O object (See SCI (UART) Input/Output section). The hardware UART provides much higher performance with lower software overhead.

Pin IO8 can be configured as an asynchronous serial input line, and pin IO10 can be configured as an asynchronous serial output line. The bit rates for input and for output can be independently specified to be 600, 1200, 2400, or 4800 bits/second at a 10MHz input clock rate. The data rate scales proportionally to the input clock rate.

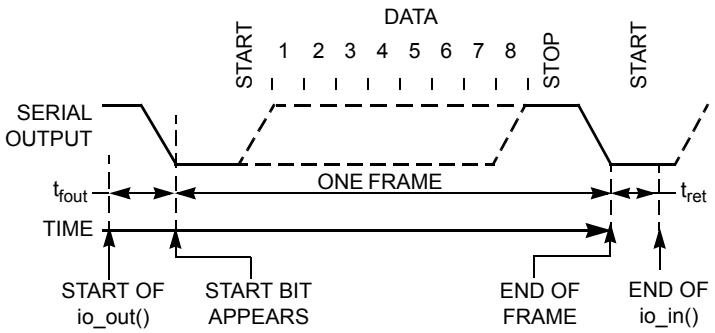
The frame format is fixed at 1 start bit, 8 data bits, and 1 stop bit; and up to 255 bytes can be transferred at a time. Either a serial input or a serial output operation (but not both) can be in effect at any one time. The interface is half-duplex only. This function suspends application processing until the operation is completed. On input, the `io_in()` request will time out after 20 character times if no start bit is received. If the stop bit has the wrong polarity (it should be a 1), the input operation is terminated with an error. The application code can use bit I/O pins for flow control handshaking if required. This function is useful for legacy applications that transfer data to serial devices such as terminals, modems, and computer serial interfaces (see Figures 3.31 and 3.32).



Symbol	Description	Typ @ 10MHz
t_{fin}	Function call to input sample Min (first sample) Max (timeout)	 67 µs 20 byte frame
t_{ret}	Return from function	10 µs

Figure 3.31 Serial Input Object

The duration of this function call is a function of the number of data bits transferred and the transmission bit rate. t_{fin} (max) refers to the maximum amount of time this function will wait for a start bit to appear at the input. After this time, the function will return a 0 as data. t_{fin} (min) is the time to the first sampling of the input pin. As an example, the timeout period at 2400 bits/second is (20 x 10 x 1/2400) + t_{fin} (min).



Symbol	Description	Typ @ 10MHz
t_{fout}	Function call to start bit	79 µs
t_{ret}	Return from function	10 µs

Figure 3.32 Serial Output

The duration of this function call is a function of the number of data bits transferred and the transmission bit rate. As an example, to output 100 bytes at 300 bits/second would require a time duration of (100 x 10 x 1/300) + t_{fout} + t_{ret}.

Touch Input/Output

The Touch I/O object enables easy interface to any slave device which adheres to Dallas Semiconductor's 1-Wire® Memory standard. This interface is a one-wire, open-drain, bidirectional connection.

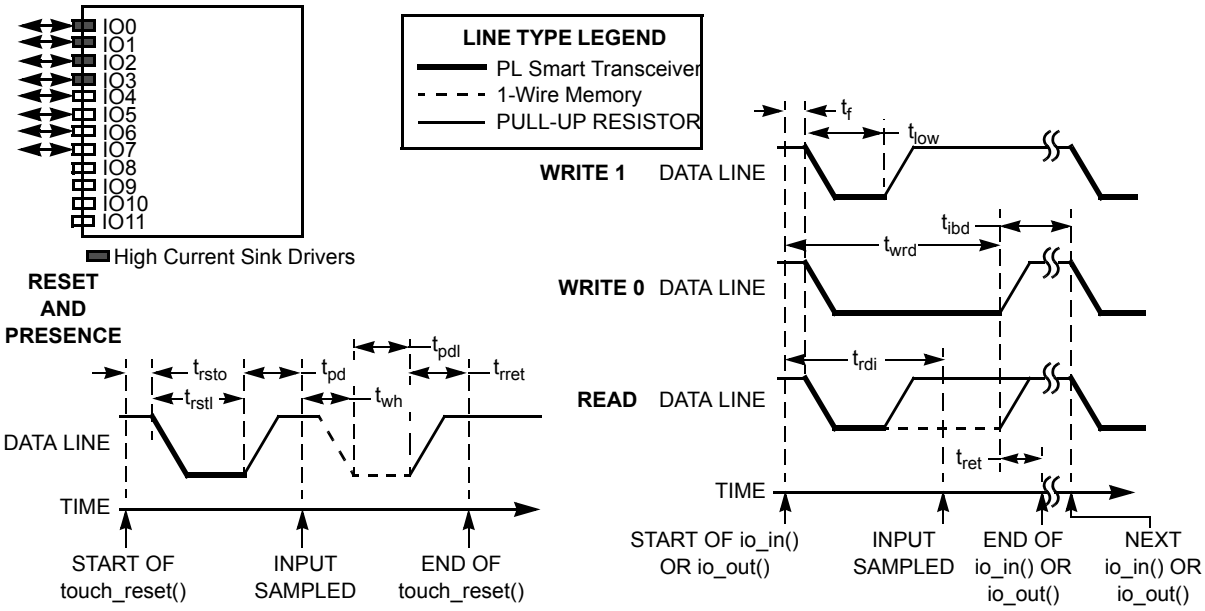
Up to eight 1-Wire Memory busses can be connected to a PL Smart Transceiver through the use of the first eight I/O pins, IO0 – IO7. The only additional component required for this is a pull-up resistor on the data line (refer to the 1-Wire Memory specification below on how to select the value of the pull-up resistor). The high current sink capabilities of IO0 – IO3 pins of the PL Smart Transceiver can be used in applications where long wire lengths are required between the 1-Wire Memory device and the PL Smart Transceiver.

The slave acquires all necessary power for its operation from the data line. Upon physical connection of a 1-Wire Memory device to a master (in this case the PL Smart Transceiver), the 1-Wire Memory generates a low presence pulse to inform the master that it is awaiting a command. The PL Smart Transceiver can also request a presence pulse by sending a reset pulse to the 1-Wire Memory device.

Commands and data are sent bit by bit to make bytes, starting with the LSB. The synchronization between the PL Smart Transceiver and the 1-Wire Memory devices is accomplished through a negative-going pulse generated by the PL Smart Transceiver.

Figure 3.33 shows the details of the reset pulse in addition to the read/write bit slots.

Note: NodeBuilder version 3.1 and later will feature the ability to adjust the t_{low}, t_{wrd}, and t_{rdi} timing values.



Symbol	Description	Min	Typ	Max
t_{rsto}	Reset call to data line low	—	60.0 µs	—
t_{rstl}	Reset pulse width	—	500 µs	—
t_{pdh}	Reset pulse release to data line high 10MHz	4.8 µs	—	275 µs
t_{pdl}	Presence pulse width	—	120.0 µs	—
t_{wh}	Data line high detect to presence pulse	—	80 µs	—
t_{rret}	Return from reset function	—	12.6 µs	—
t_f	I/O call to data line low (start of bit slot)	—	125.4 µs	—
t_{low}	Start pulse width 10MHz	—	4.2 µs	—
t_{rdi}	Start pulse edge to sampling of input (read operation) 10MHz	—	15.0 µs	—
t_{wrd}	Start pulse edge to PL Smart Transceiver releasing the data line 10MHz	—	66.6 µs	—
t_{ibd}	Inter-bit delay 10MHz	—	61.2 µs	—
t_{ret}	Return from I/O call	—	42.6 µs	—

Figure 3.33 Touch Input/Output Object

The leveldetect input object can be used for detection of asynchronous attachments of 1-Wire Memory devices to the PL Smart Transceiver. In such a case, the leveldetect input object is overlaid on top of the Touch I/O object. Refer to the *Neuron C Programmer's Guide* for information on I/O object overlays.

The Touch I/O object can run at PL Smart Transceiver clock rates of 6.5536MHz and 10MHz only. This is because the Touch I/O object is designed to meet the 1-Wire Memory timing specification at those PL Smart Transceiver clock speeds only.

For more specific information on the mechanical, electrical, and protocol specifications, refer to the 1-Wire device information available from Dallas Semiconductor Corporation.

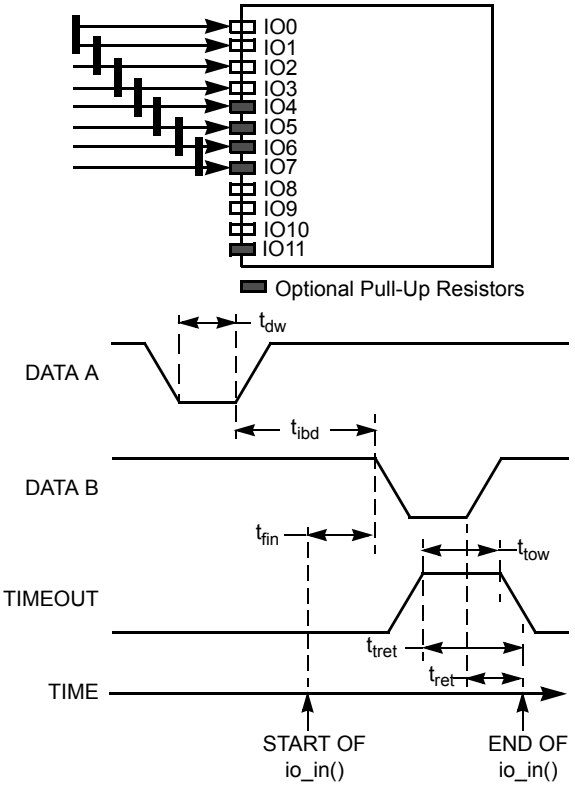
Wiegand Input

This input object provides an easy interface to any card reader supporting the Wiegand standard. Data from the reader is presented to the PL Smart Transceiver through the use of two of its first eight I/O pins, IO0 – IO7. Up to four Wiegand devices can be connected to the PL Smart Transceiver. Data is read MSB first.

Wiegand data starts as a negative-going pulse on one of the two pins selected. One input represents a logical 0 bit and the other pin a logical 1, as selected through the I/O declaration. The bit data on the two lines are mutually exclusive and are spaced at least 150µs apart. Figure 3.34 shows the timing relationship of the two data lines with respect to each other and the PL Smart Transceiver.

Any unused I/O pin from IO0 to IO7 can be optionally selected as the timeout pin. When the timeout pin goes high, the function aborts and returns. The application processor's watchdog timer is automatically updated during the operation of this input object.

Incoming data on any of the Wiegand input pins is sampled by the PL Smart Transceiver every 200ns at a 10MHz clock (scales inversely with the clock frequency). because the Wiegand data is usually asynchronous, care must be taken in the application program to ensure that this function is called in a timely manner in order that no incoming data is lost.



Symbol	Description	Min	Typ	Max
t_{fin}	Function call to start of second data edge	—	75.6 µs	—
t_{dw}	Input data width (at 10MHz)	200 ns	100 µs	880 ms
t_{ibd}	Inter-bit delay	150 µs	—	900 µs
t_{tow}	Timeout pulse width	—	39 µs	—
t_{tret}	Timeout to function return	—	18.0 µs	—
t_{ret}	Last data bit to function return	—	74.4 µs	—

Figure 3.34 Wiegand Input Object

SCI (UART) Input/Output

Pins IO8 and IO10 can be configured as asynchronous SCI (serial communications interface) input and output lines, respectively. The SCI object model supports the following bit rates for half-duplex transfers when operating at 10MHz: 300, 600, 1200, 2400, 4800, 9600, 19200, 38400, 57600, and 115200 bits per second. The effective transmitted data rate for half-duplex transfers corresponds to the bit rate at all speeds. There are no inter-byte idle periods and the bit rate of the input and output can not be independently specified.

For full-duplex transfers, when data is being received and transmitted at the same time, the effective bit rate will be 60% at 57600 bits per second, and 30% at 115200 bits per second. All other bit rates specified above for half-duplex

transfers are also supported for full-duplex transfers. No errors are introduced (other than inter-byte spacing of transmitted data) under these conditions.

For 6.5536MHz operation, the bit rates are limited to a maximum of 19200 bits per second for both half and full-duplex transfers.

The frame format is one start bit, eight data bits and one or two stop bits. Up to 255 output bytes and 255 input bytes can be transferred at a time. If an input stop bit has the wrong polarity, the interface will attempt to recover and re-synchronize. However, a framing error will be flagged in the status register. If necessary, the application code can use other bit I/O pins for flow-control handshaking.

This I/O model depends on interrupts to receive data at high speed. Once reception has be set up, control will be returned to the application immediately and the application will need to poll the I/O model for reception completion. Reception can be suspended and resumed by disabling and enabling interrupts. Turning off interrupts might be required when going off-line, or for ensuring that other time-critical application execution is not disturbed by background interrupts. Additionally, SCI reception can also be aborted. Note that sustained reception at 115,200bps can starve the application processor. Care must be given to allow the PL Smart Transceiver to process received bytes in a timely manner and update the watchdog timer.

However, data transmission is NOT handled by interrupts; control will be returned to the application only after the last byte has been placed in the transmission shift register. It is important to note that if previously set up, reception interrupts will work even while transmission is taking place. This provides a **full duplex interface**.

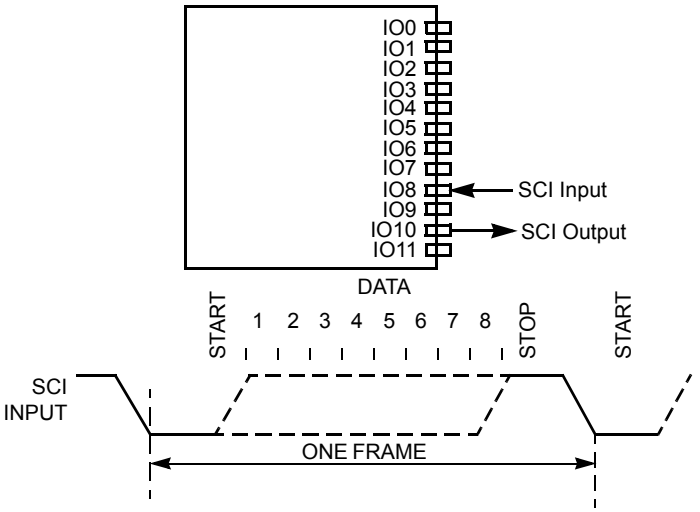


Figure 3.35 SCI Input/Output

SPI Input/Output

Pins IO8, IO9 and IO10 can be configured as a serial peripheral interface (SPI) port. The directions of the pins vary with the configuration. In master mode, pin IO8 is the clock (driven by the PL Smart Transceiver), IO9 is serial data input (Master In Slave Out or MISO) and IO10 is serial data output (Master Out Slave In or MOSI). In slave mode, pin IO8 is the clock input, IO9 is serial data output (MISO) and IO10 is serial data input (MOSI). If the **`Neurowire`** keyword is used, the pins assume a Neurowire compatible direction in which IO9 is always output and IO10 is always input. Serial data is clocked out on the output pin at the same time as it is clocked in on the input pin. In SPI master mode, no other masters are allowed on the bus. IO7 can be used as a select pin in slave mode, allowing the PL Smart

Transceiver to coexist with other slave mode devices on a 3 wire bus. A logic one level on the select line disables the output drivers of the output pins and puts them in a high impedance state.

If the PL Smart Transceiver is the only slave device on the SPI bus and the master device does not drive the **Slave Select** ($\overline{SS}$) signal, then either

Pin IO7 should be declared as an input pin and externally grounded.

OR

Pin IO7 must be declared in the following order:

```
IO_7 output bit io_p7_out = 1;     // initialize to '1'
IO_7 input bit io_p7_in;
```

As long as the IO7 output bit is initialized to a 1 and the $\overline{SS}$ is disabled, IO7 can be used as an input. Note that $\overline{SS}$ should be used whenever possible to ensure proper synchronization and recovery in the event of framing errors from the master device.

The bit rates supported by the SPI port are summarized in Tables 3.6 and 3.7

Table 3.6 Master mode

Clock	10MHz	6.5536MHz	
7	19.531kbps	12.8kbps	
6	39.063kbps	25.6kbps	
5	78.125kbps	51.2kbps	See *Note*
4	156.250kbps	102.4kbps	See *Note*
3	312.500kbps	204.8kbps	See *Note*
2	625.000kbps	409.6kbps	See *Note*
1	1250.000kbps	819.2kbps	See *Note*
0	2500.000kbps	1638.4kbps	See *Note*

Note: For Clock 5 and higher bit rates, the bit rate shown is the peak rate. The data is burst out in pairs of bytes and the overall average data rate is limited to approximately 40kbps and 25kbps for 10MHz and 6.5536MHz input clocks, respectfully.

Table 3.7 Slave mode

	10MHz	6.5536MHz	
Max burst rate	1250kbps	819.2kbps	
Max burst size	2 bytes	2 bytes	
Min burst spacing	400us	640us	From start of one burst to next.
Max sustained data rate	40kbps	25kbps	

Sustained reception in slave mode at maximum bit rate can starve the application processor and cause overruns and presents a possible risk of watchdog timeout. Care must be given to allow the PL Smart Transceiver to process received bytes in a timely manner. Master mode has no such restriction because the PL Smart Transceiver regulates the data transfer.

The **`clockedge`** and **`invert`** keywords are used to determine the point at which data is sampled and the idle level of the clock signal. The clock signal is idle at the logic 1 level. The `invert` keyword could be used to change the idle state to correspond to a logic 0 level. Common SPI implementations use the terms clock phase (**CPHA**) and

clock polarity (**CPOL**) to determine the behavior of the clock signal during SPI transmissions. These terms relate directly to the `clockedge` and `invert` keywords used in this data book as follows:

CPHA

```
1 = clockedge(+)
0 = clockedge(-)
```

CPOL

```
1 = [default]
0 = invert
```

The active edge of the clock is determined by the `clockedge` and `invert` keywords. If the clock signal is idle at logic 1 (default), then `clockedge(-)` indicates that the falling edge of the clock signal is active. If the `invert` keyword is used, the rising edge of the clock signal would be active (see Figures 3.36 and 3.37).

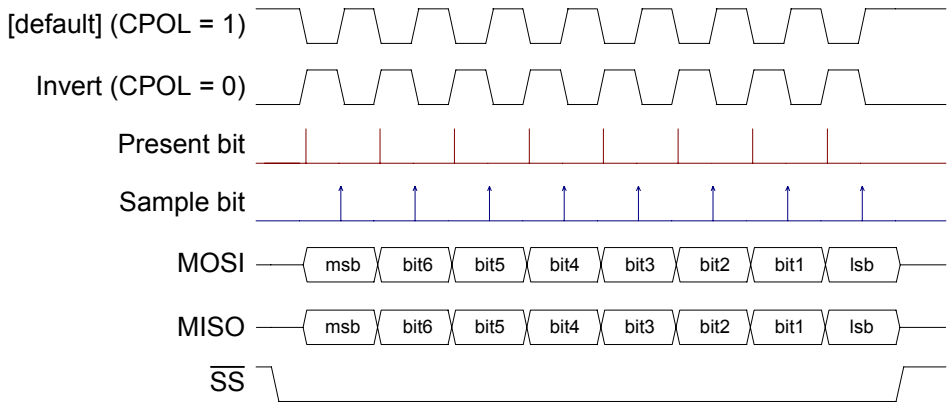


Figure 3.36 Transmission Timing for Clockedge(-) (CPHA : 0)

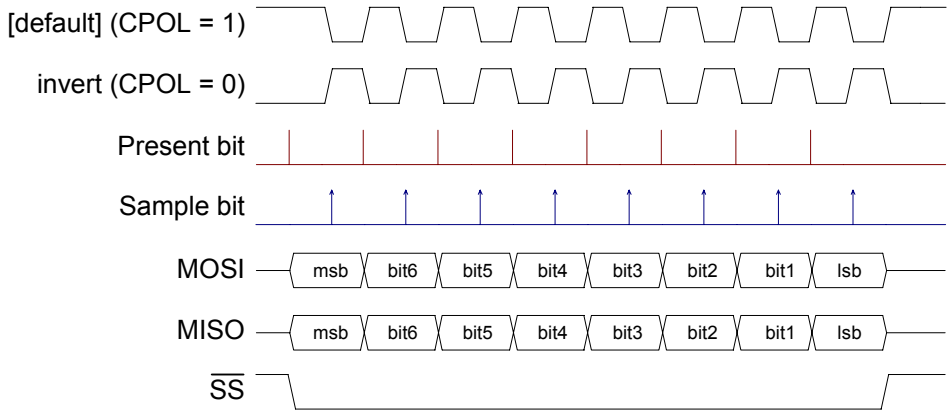
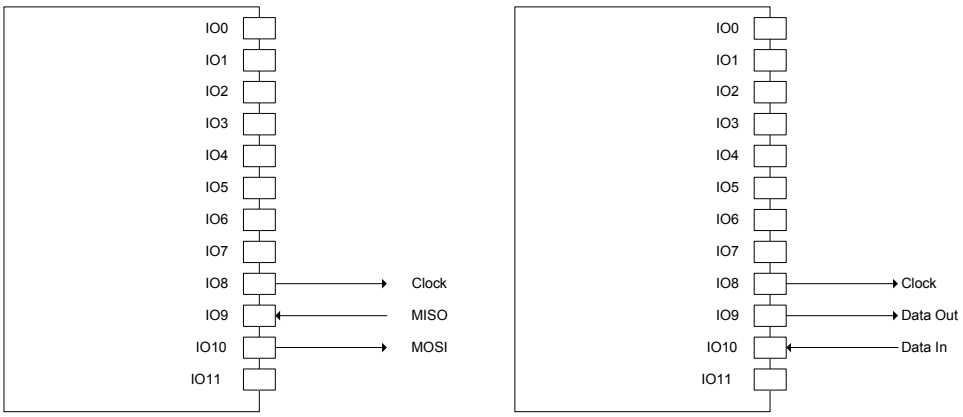


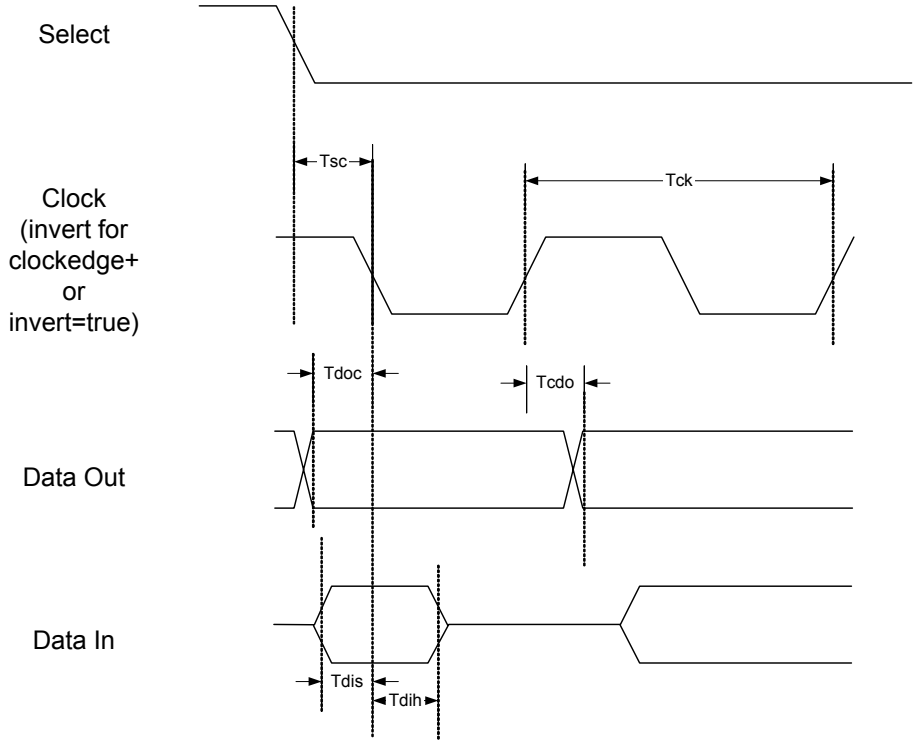
Figure 3.37 Transmission Timing for Clockedge(+) (CPHA : 1)

Up to 255 bytes can be bi-directionally transferred at a time. This I/O model depends on interrupts to process data at high speed and does not use the `io_in()` and `io_out()` function calls. Once transfer is initiated, control will be returned to the application immediately and the application will need to poll the I/O model for completion. Transfers can be suspended and resumed by disabling and enabling interrupts. Turning off interrupts might be required when going off-line, or for assuring that other time-critical application execution is not disturbed by background interrupts. Additionally, transfers can also be aborted.



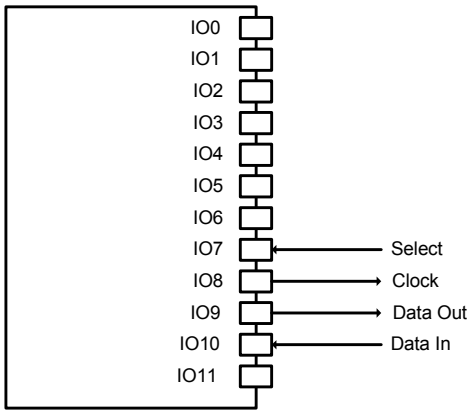
SPI Master

SPI Master (Neurowire pin mode)

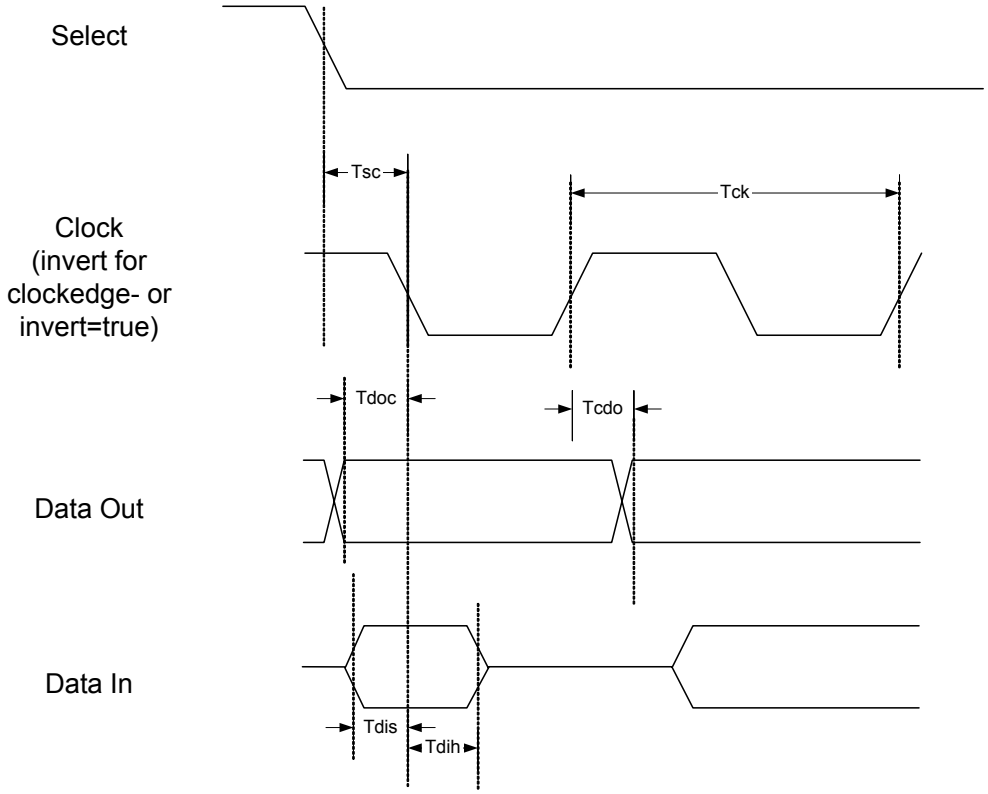


Param	Description	Min	Typ	Max	Units
Tck	Clock cycle (user specified)				
Tsc	Select low to Clock transition	4.8			µs
Tdoc	Data out to Clock (1st bit of invert mode)	0.5*Tck			ns
Tcdo	Clock to data out			5	ns
Tdis	Data in setup	10			ns
Tdih	Data in hold	10			ns

Figure 3.38 SPI Master Mode Timing



SPI Slave



Param	Description	Min	Typ	Max	Units
Tck	Clock cycle (user specified)			1.25	
Tsc	Select low to Clock transition	220			µs
Tdoc	Data out to Clock (1st bit of invert mode)	440			ns
Tcdo	Clock to data out			45	ns
Tdis	Data in setup	10			ns
Tdih	Data in hold	10			ns
Tsdz	Select high to data in high impedance			220	ns

Figure 3.39 SPI Slave Mode Timing

Timer/Counter Input Objects

The PL Smart Transceivers have two 16-bit timer/counters. For the first timer/counter, IO0 is used as the output, and a multiplexer selects one of pins IO4 – IO7 as the input. The second timer/counter uses IO1 as the output and IO4 as the input (see Figure 2.7). Multiple timer/counter input objects can be declared on different pins within a single application. By calling the `io_select()` function, the application can use the first timer/counter in up to four different input functions. If a timer/counter is configured in one of the output functions, or as a quadrature input, then it can not be reassigned to another timer/counter object in the same application program.

The timing numbers shown in this section are valid for both an explicit I/O call or an implicit I/O call through a **`when`** clause, and are assumed to be for a PL Smart Transceiver running at 10MHz.

Input timer/counter objects have the advantage (over non-timer/counter objects) in that input events will be captured even if the application processor is occupied doing something else when the event occurs. A true `when` statement condition for an event being measured by a timer/counter is the completion of the measurement and a value being returned to an event register. If the processor is delayed due to software processing and cannot read the register before another event occurs, then the value in the register will reflect the status of the last event. The timer/counters are automatically reset upon completion of a measurement. **The first measured value of a timer/counter is always discarded to eliminate the possibility of a bad measurement after the chip comes out of a reset condition.** Single events can not be measured with the timer/counters. Figure 3.40 shows an example of how the timer/counter objects are processed with a Neuron C `when` statement.

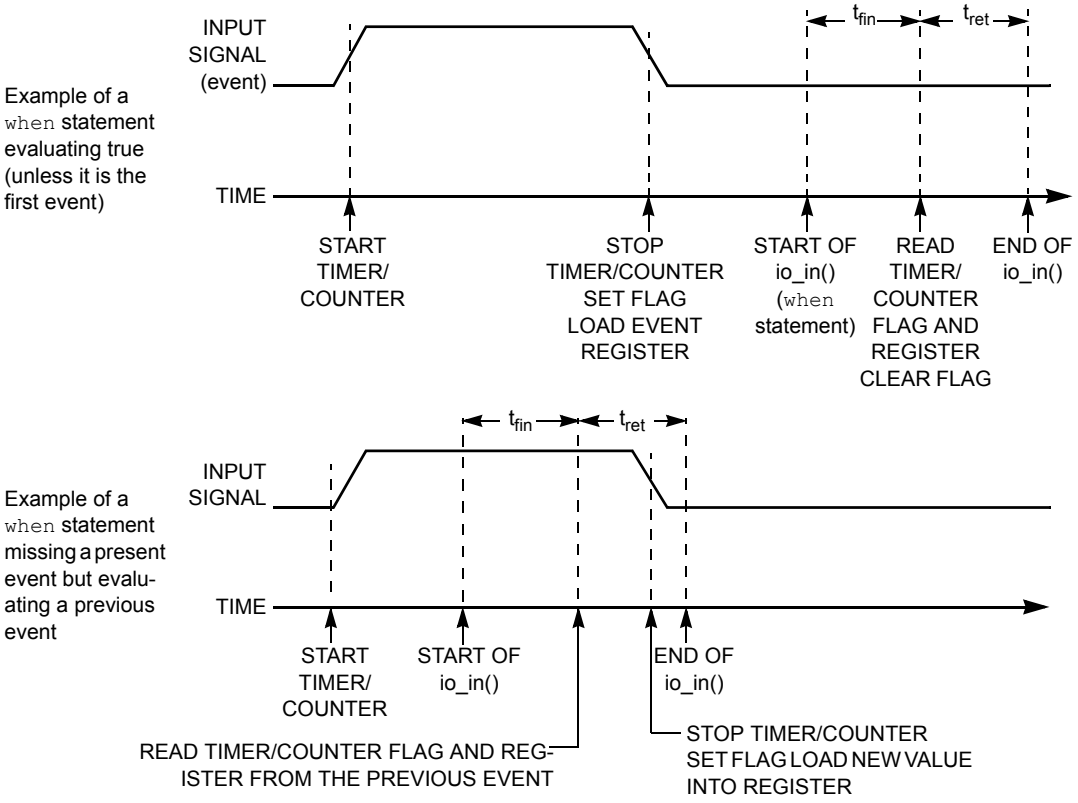
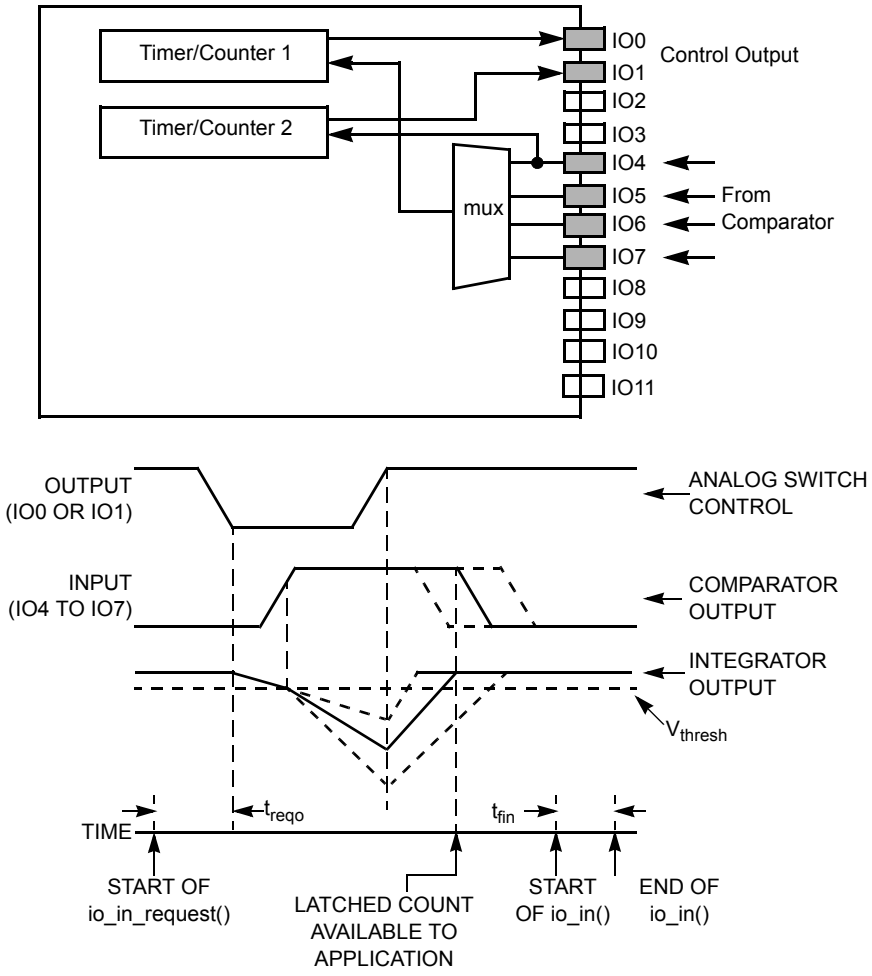


Figure 3.40 Example of `when` Statement Processing Using the Ontime Input Function

Dualslope Input

This input object uses a timer/counter to control and measure the integration periods of a dualslope integrating analog to digital converter (see Figure 3.41). The timer/counter provides the control output signal and senses a comparator output signal. The control output signal controls an external analog multiplexer which switches between the unknown input voltage and a voltage reference. The timer/counter's input pin is driven by an external comparator which compares the integrator's output with a voltage reference. At the end of conversion, the external comparator will drive a low level to one of pins IO4 – IO7. If external circuitry indicates "end of conversion" with a high level, use the **`invert`** keyword in the I/O declaration.

The resolution and range of the timer/counter period options is shown by Table 3.8 in the *Notes* section at the end of this chapter.



Symbol	Description	Min	Typ	Max
t_{reqo}	`io_in_request()` to output toggle	—	75.6 µs	—
t_{fin}	Input function call and return	—	82.8 µs	—

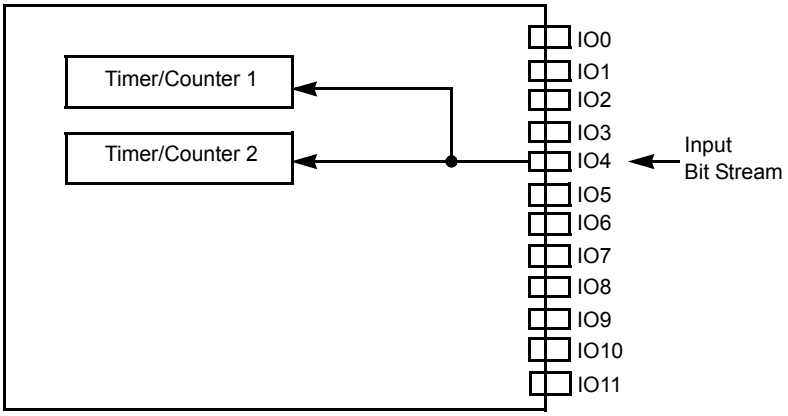
Figure 3.41 Dualslope Input Object

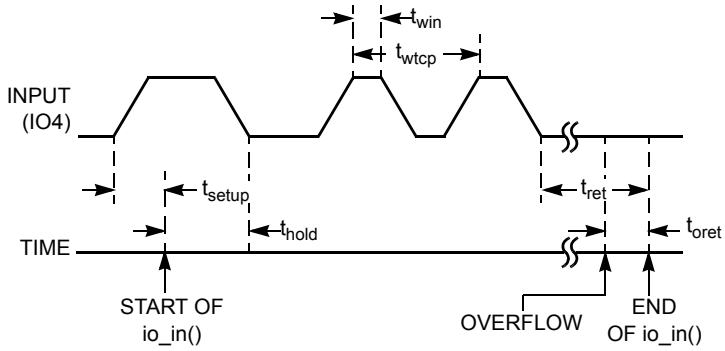
Edgelog Input

The edgelog input object can record a stream of input pulses measuring the consecutive low and high periods at the input and storing them in user-defined storage (see Figure 3.42). The values stored represent the units of clock period between rising and falling input signal edges. Both timer/counters of the PL Smart Transceiver are used for this object.

The measurement series starts on the first rising (positive) edge, unless the **`invert`** keyword is used in the I/O object declaration. The measurement process stops whenever an overflow condition is sensed on either timer/counter.

The resolution and range of the timer/counter period options are shown in Table 3.8 in the *Notes* section at the end of this chapter. This object is useful for analyzing an arbitrarily-spaced stream of input edges (or pulses), such as the output of a UPC bar-code reader or infrared receiver.





Symbol	Description	Min	Typ	Max
t_{setup}	Input data setup	0	—	—
t_{win}	Input pulse width	1 T/C clk	—	65,534 T/C clks
t_{hold}	`io_in()` call to data input edge for inclusion of that pulse	26.4 µs	—	—
t_{wtcp}	Two consecutive pulse widths	104 µs	—	—
t_{oret}	Return on overflow	—	42.6 µs	—
t_{ret}	Return on count termination	—	49.6 µs	—

Figure 3.42 Edgelog Input Object

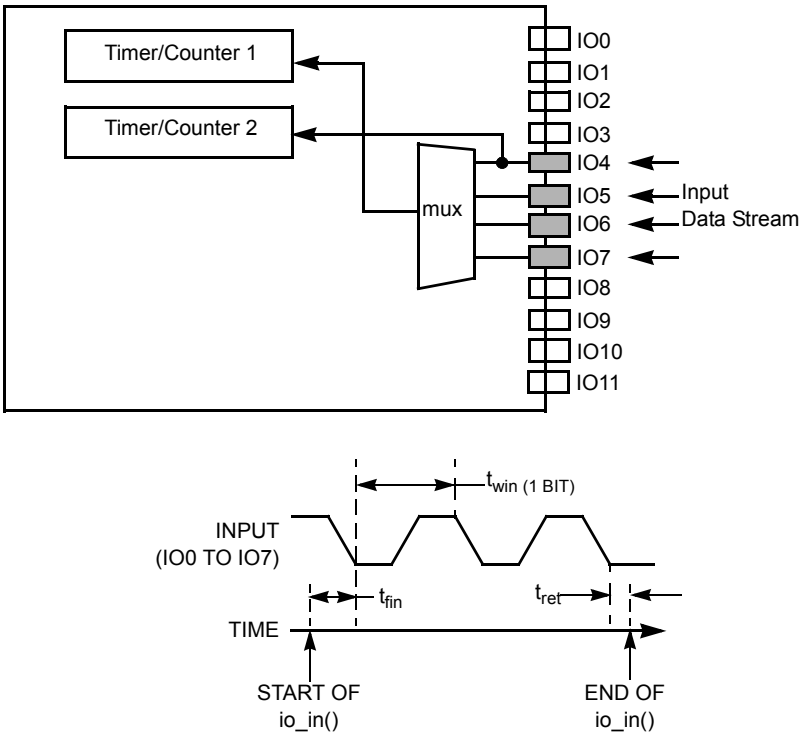
***Note*:** T/C clk represents the period of the clock used during the declaration of the I/O object.

Infrared Input

The infrared input object is used to capture a stream of data generated by a class of infrared remote control devices (see Figure 3.43). The input to the object is the demodulated series of bits from infrared receiver circuitry. The period of the on/off cycle determines the data bit value, a shorter cycle indicating a one, and a longer cycle indicating a zero. The actual threshold for the on/off determination is set at the time of the call of the function. The measurements are made between the negative edges of the input bits unless the **`invert`** keyword is used in the I/O declaration.

The infrared input object, based on the input data stream, generates a buffer containing the values of the bits received. The resolution and range of the timer/counter period options is shown in Table 3.8 in the *Notes* section at the end of this chapter.

This function can be used with an off-the-shelf IR demodulator such as an NEC µPD1913 or Sharp GP1U50X to quickly develop an infrared interface to the PL Smart Transceiver. The edgelog input object can also be used for this purpose. However, this requires more code.



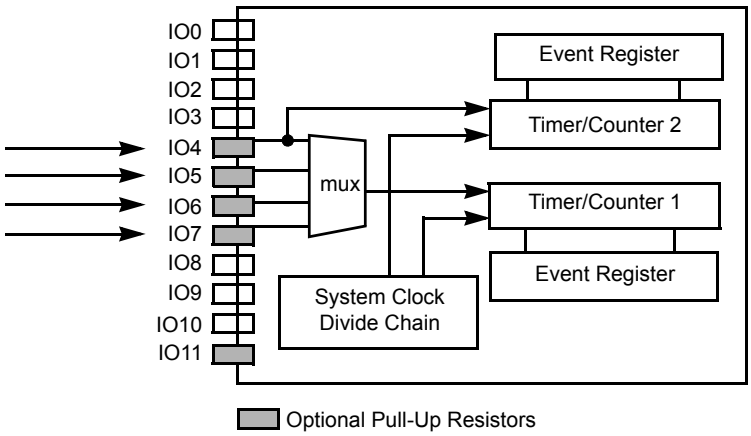
Symbol	Description	Min	Typ	Max
t_{fin}	Function call to start of input sampling	—	82.2 µs	—
t_{ret}	End of last valid bit to function return	max-period	max-period	—
t_{win}	Minimum input period width	—	93 µs	—

Note: max-period is the timeout period passed to the function at the time of the call.

Figure 3.43 Infrared Input Object

Ontime Input

A timer/counter can be configured to measure the time for which its input is asserted. Table 3.8 shows the resolution and maximum times for different I/O clock selections. Assertion can be defined as either logic high or logic low. This object can be used as a simple analog-to-digital converter with a voltage-to-time circuit, or for measuring velocity by timing motion past a position sensor (see Figures 3.40 and 3.44).



Reference Figure 3.40

Symbol	Description	Typ @ 10MHz
t_{fin}	Function call to input sample	86 µs
t_{ret}	Return from function	52/22 µs*

*If the measurement is new, t_{ret} = 52µs. If a new time is not being returned, t_{ret} = 22µs.

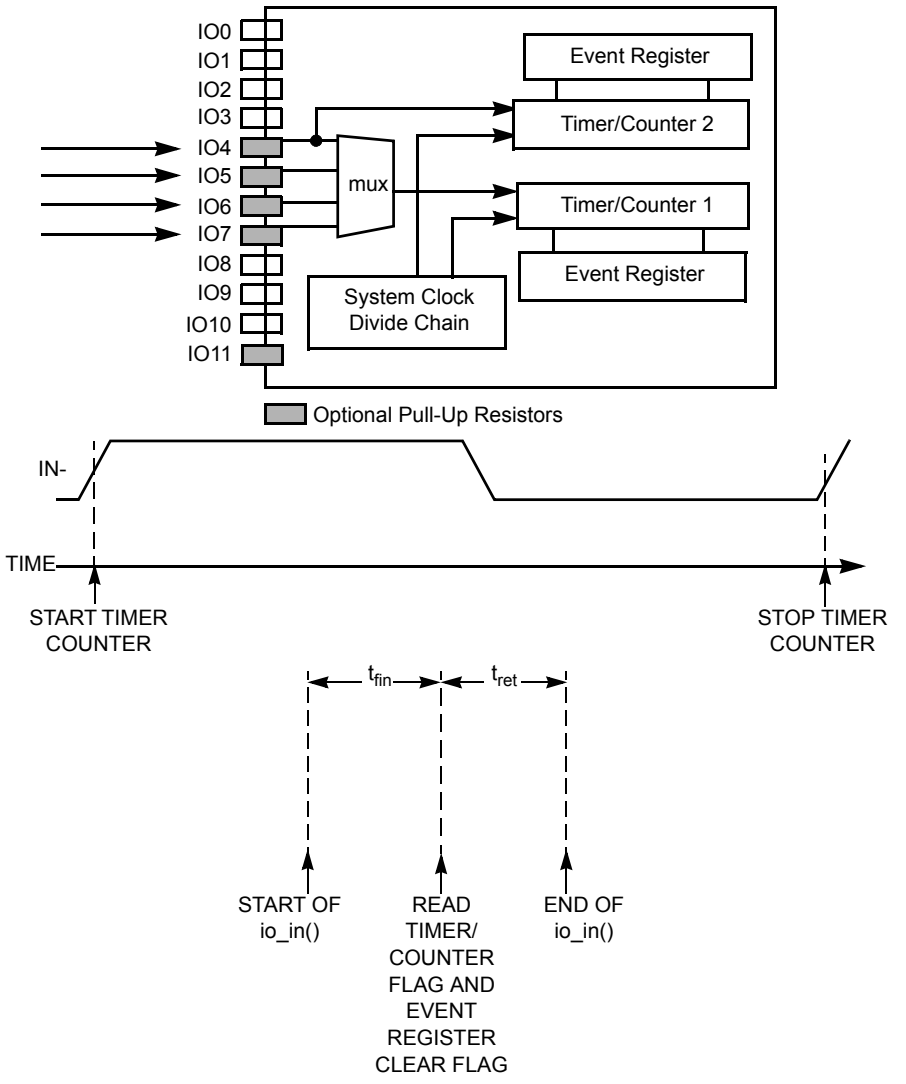
Figure 3.44 Ontime Latency Values

This is a level-sensitive function. The active level of the input signal gates the clock driving the internal counter in the PL Smart Transceiver.

The actual active level of the input depends on whether or not the `invert` option was used in the declaration of the function block. The default is the high level.

Period Input

A timer/counter can be configured to measure the period from one rising or falling edge to the next corresponding edge on the input. Table 3.8 shows the resolution and maximum time measured for various clock selections. This object is useful for instantaneous frequency or tachometer applications. Analog-to-digital conversion can be implemented using a voltage-to-frequency converter with this object (see Figure 3.45).



Reference Figure 3.40

Symbol	Description	Typ @ 10MHz
t_{fin}	Function call to input sample	86 µs
t_{ret}	Return from function	52/22 µs*

*If the measurement is new, t_{ret} = 52µs. If a new time is not being returned, t_{ret} = 22µs.

Figure 3.45 Period Input Latency Values

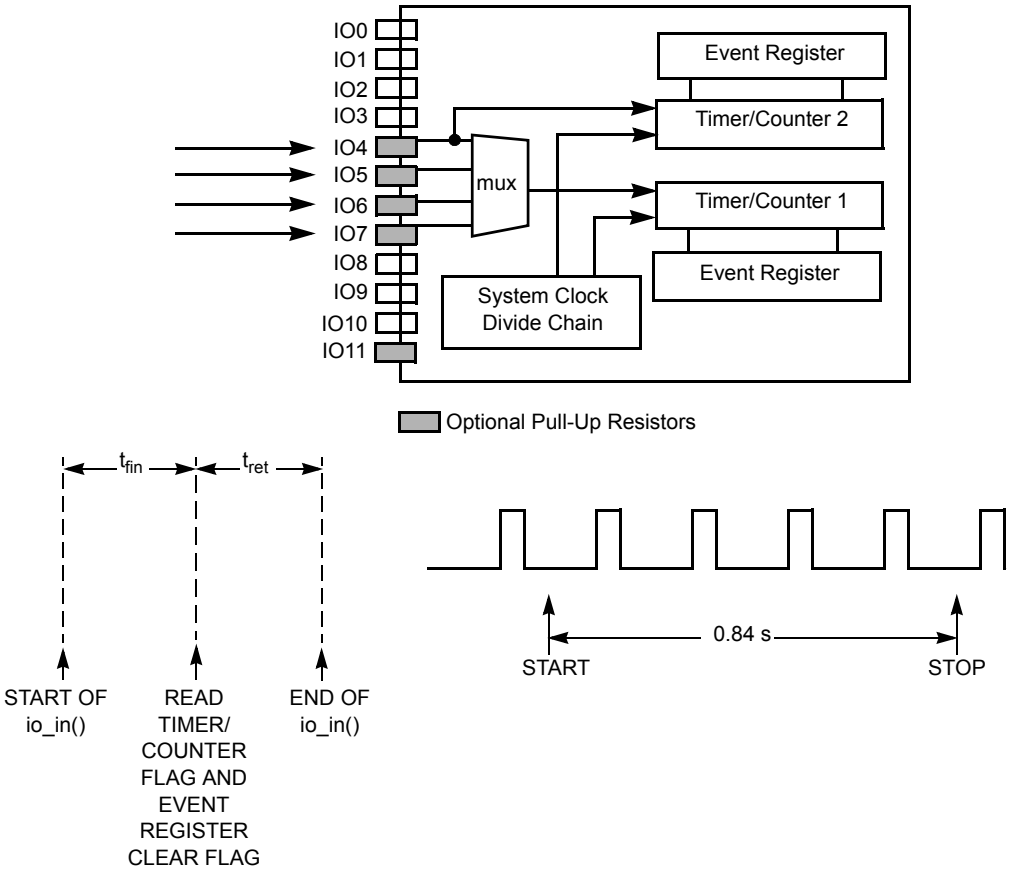
This is an edge-sensitive function. The clock driving the internal counter in the PL Smart Transceiver is free running. The detection of active input edges stops and resets the counter each time.

The actual active edge of the input depends on whether or not the `invert` option was used in the declaration of the function block. The default is the negative edge.

Because the period function measures the delay between two consecutive active edges, the `invert` option has no effect on the returned value of the function for a repeating input waveform.

Pulsecount Input

A timer/counter can be configured to count the number of input edges (up to 65,535) in a fixed time (0.8388608 second) at all allowed input clock rates. Edges can be defined as rising or falling. This object is useful for average frequency measurements, or tachometer applications (see Figure 3.46).



Reference Figure 3.40

Symbol	Description	Typ @ 10MHz
t_{fin}	Function call to input sample	86 µs
t_{ret}	Return from function	52/22 µs*

*If the measurement is new, t_{ret} = 52µs. If a new time is not being returned, t_{ret} = 22µs.

Figure 3.46 Pulse Count Input Latency Values

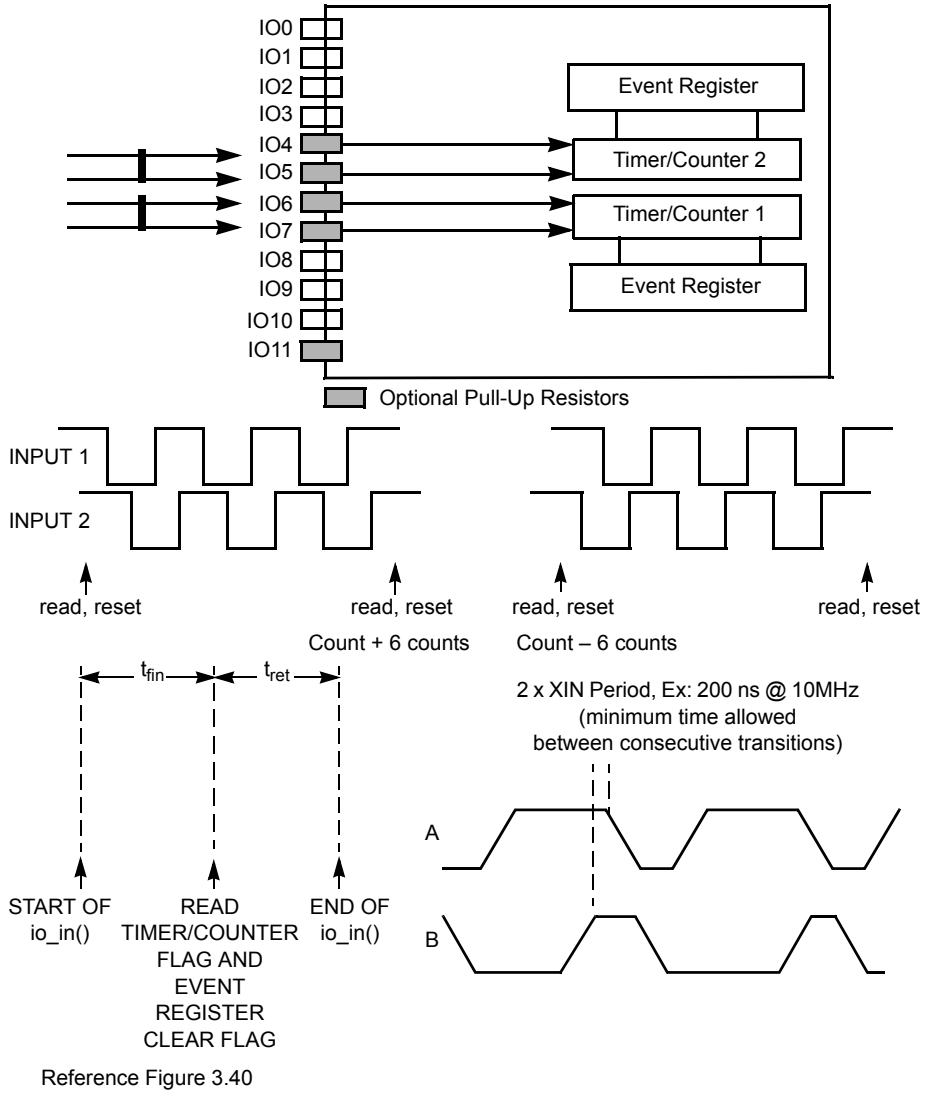
This is an edge-sensitive function. The clock driving the internal counter in the PL Smart Transceiver is the actual input signal. The counter is reset automatically every 0.839 second.

The internal counter increments with every occurrence of an active input edge. Every 0.839 second, the content of the counter is saved and the counter is then reset to 0. This sequence is repeated indefinitely.

The actual active edge of the input depends on whether or not the `invert` option was used in the declaration of the function block. The default is the negative edge.

Quadrature Input

A timer/counter can be configured to count transitions of a binary Gray code input on two adjacent input pins. The Gray code is generated by devices such as shaft encoders and optical position sensors which generate the bit pattern (00,01,11,10,00, …) for one direction of motion and the bit pattern (00,10,11,01,00, …) for the opposite direction. Reading the value of a quadrature object gives the arithmetic net sum of the number of transitions because the last time it was read (-16,384 to 16,383). The maximum frequency of the input is one-quarter of the input clock rate, for example 2.5MHz with a 10MHz PL Smart Transceiver input clock. Quadrature devices can be connected to timer/counter 1 via pins IO6 and IO7, and timer/counter 2 via pins IO4 and IO5 (see Figure 3.47). If the second input transitions low while the first input is low and high while the first input is high, the counter counts up. Otherwise, the count is down.



Reference Figure 3.40

Symbol	Description	Typ @ 10MHz
t_{fin}	Function call to input sample	90 µs
t_{ret}	Return from function	88 µs

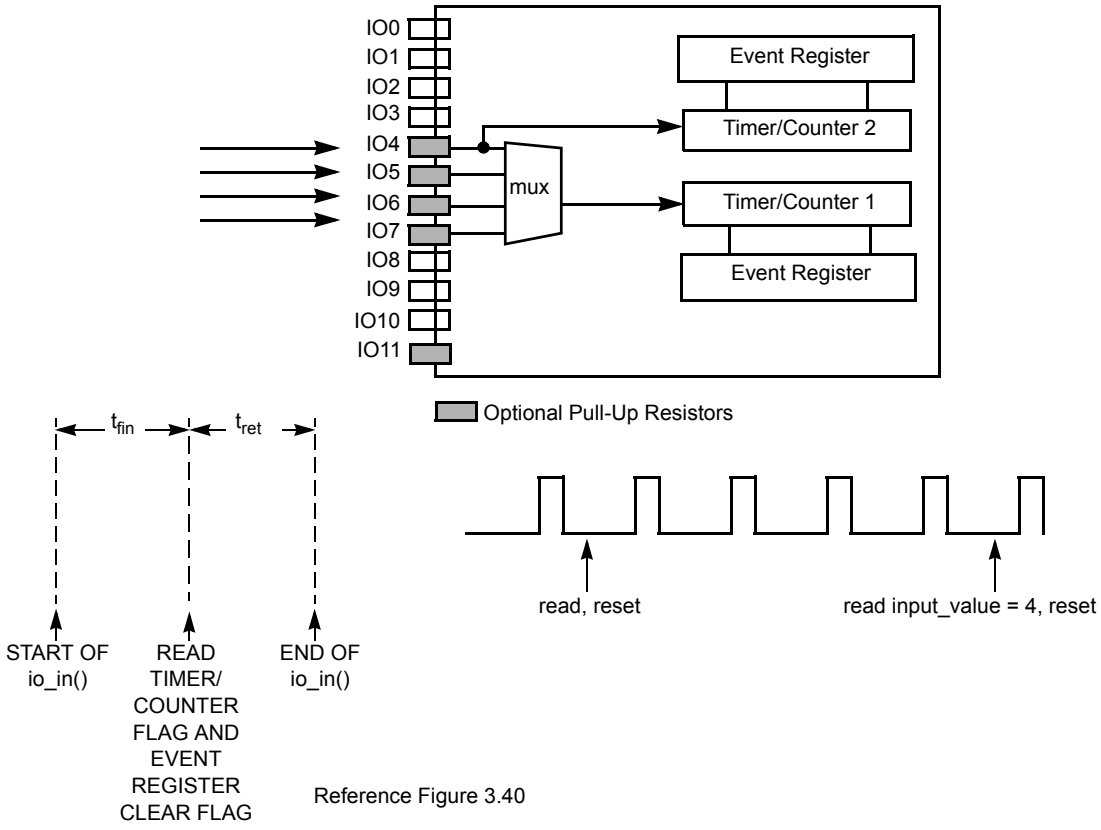
Figure 3.47 Quadrature Input Latency Values

A call to this function returns the current value of the quadrature count because the last read operation. The counter is then reset and ready for the next series of input transitions. The count returned is a 16-bit signed binary number, capped at ±16K.

The number shown in the diagram above is the minimum time allowed between consecutive transitions at either input of the quadrature function block. For more information, see the, *Neuron Chip Quadrature Input Function Interface* engineering bulletin.

Totalcount Input

A timer/counter can be configured to count either rising or falling input edges, but not both. Reading the value of a totalcount object gives the number of transitions because the last time it was read (0 to 65,535). Maximum frequency of the input is one-quarter of the input clock rate, for example 2.5MHz at a maximum of 10MHz PL Smart Transceiver input clock. This object is useful for counting external events such as contact closures, where it is important to keep an accurate running total (see Figure 3.48).



Symbol	Description	Typ @ 10MHz
t_{fin}	Function call to input sample	92 µs
t_{ret}	Return from function	61 µs

Figure 3.48 Totalcount Input Latency Values

A call to this function returns the current value of the totalcount value corresponding to the total number of active clock edges because the last call. The counter is then reset, and ready for the next series of input transitions.

The actual active edge of the input depends on whether or not the `invert` option was used in the declaration of the function block. The default is the negative edge.

Timer/Counter Output Objects

Edgedivide Output

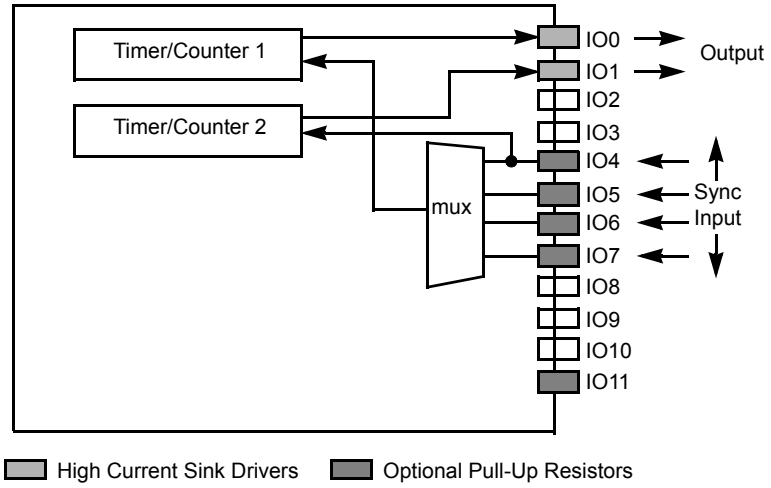
This output object acts as a frequency divider by providing an output frequency on either pin IO0 or IO1. The output frequency is a divided-down version of the input frequency applied on pins IO4 – IO7. The object is useful for any divide-by-n operation, where *n* is passed to the timer/counter object through the application program and can be from 1 to 65,535. The value of 0 forces the output to the off level and halts the timer/counter.

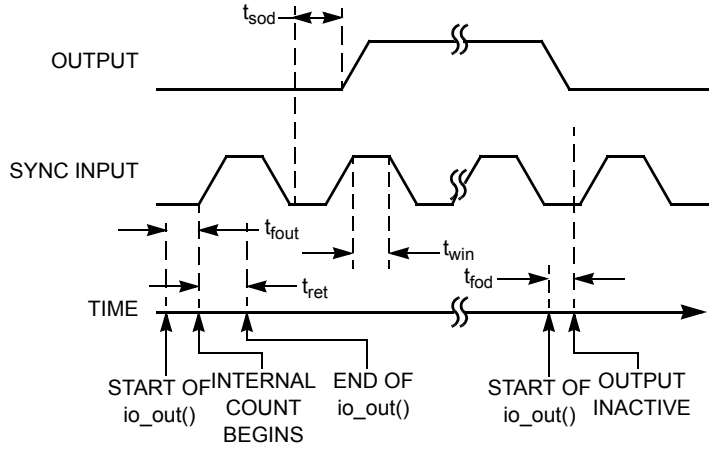
A new divide value will not take effect until after the output toggles, with two exceptions: if the output is initially disabled, the new (non-zero) output will start immediately after t_{fout}; or, for a new divide value of 0, the output is disabled immediately.

Normally the negative edges of the input sync pulses are the active edge. Using the **`invert`** keyword in the object declaration makes the positive edge active.

The initial state of the output pin is logic 0 by default. This can also be changed to logic 1 through the object declaration.

Figure 3.49 shows the pinout and timing information for this output object.



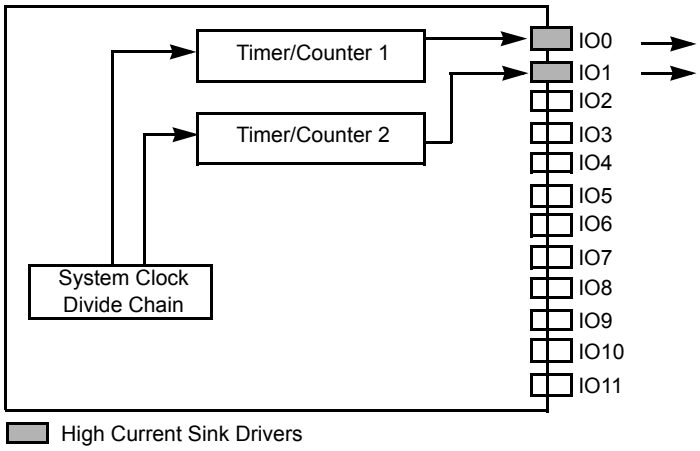


Symbol	Description	Min	Typ	Max
t_{fout}	Function call to start of timer	—	96 µs	—
t_{fod}	Function to output disable	—	82.2 µs	—
t_{sod}	Active sync edge to output toggle	550 ns	—	750 ns
t_{win}	Sync input pulse width (10MHz)	200 ns	—	—
t_{ret}	Return from function	—	13 µs	—

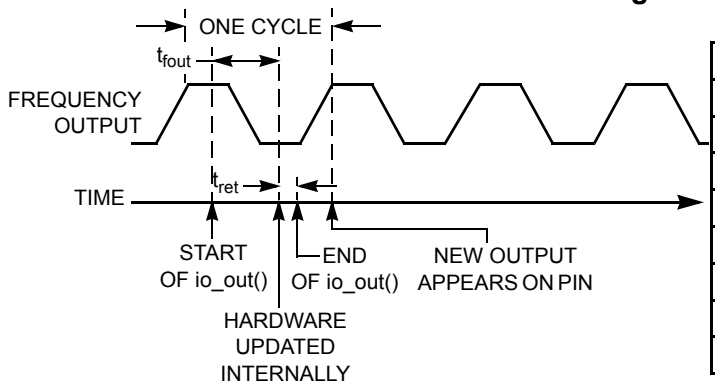
Figure 3.49 Edgedivide Output Object

Frequency Output

A timer/counter can be configured to generate a continuous square wave of 50% duty cycle. Writing a new frequency value to the device takes effect at the end of the current cycle. This object is useful for frequency synthesis to drive an audio transducer, or to drive a frequency to voltage converter to generate an analog output (see Figure 3.50).



Frequency Resolution and Maximum Range at 10MHz



CLK	Resolution	Range	Unit
0	0.4	26.21	µs
1	0.8	52.42	µs
2	1.6	104.86	µs
3	3.2	209.71	µs
4	6.4	419.42	µs
5	12.8	838.85	µs
6	25.6	1677	µs
7	51.2	3355	µs

Symbol	Description	Typ @ 10MHz
t_{fout}	Function call to output update	96 µs
t_{ret}	Return from function	13 µs

Figure 3.50 Frequency Output Latency Values

A new frequency output value will not take effect until the end of the current cycle. There are two exceptions to this rule. If the output is disabled, the new (non-zero) output will start immediately after t_{fout}. Also, for a new output value of zero, the output is disabled immediately and not at the end of the current cycle.

A disabled output is a logic zero by default unless the **invert** keyword is used in the I/O object declaration. The resolution and range for this object scale with PL Smart Transceiver input clock rate.

Infrared Pattern Output

An **`infrared_pattern`** I/O object produces a series of timed repeating square wave output signals. The frequency of the square wave output is controlled by the application. Normally, this frequency is the modulation frequency used for infrared transmission.

The pattern of this modulation frequency is controlled by an array of unsigned long timing values. The first value in this array controls the length of the first burst of modulation frequency signal output. The output is active for this period. The second value in this array controls the length of an absence of the modulation frequency signal. The output is idle for this period. This pattern is then repeated by subsequent values in the array in order to produce a sequence of frequency output bursts separated by idle periods. This array is similar to the array generated by the **edgelog** input object.

This I/O object is useful for driving an infrared LED to provide infrared control of devices that support infrared remote control.

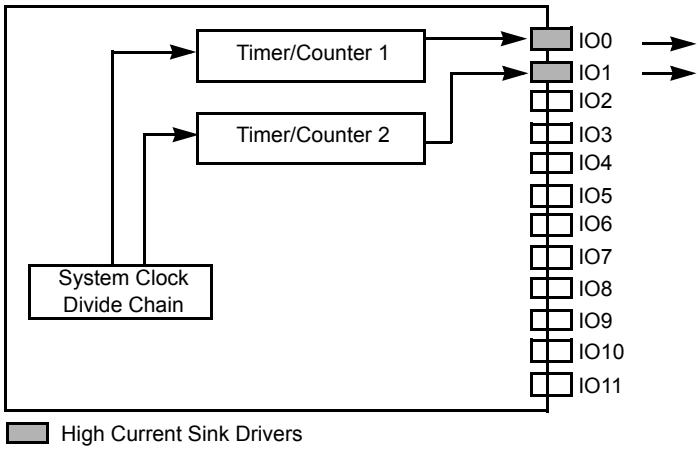
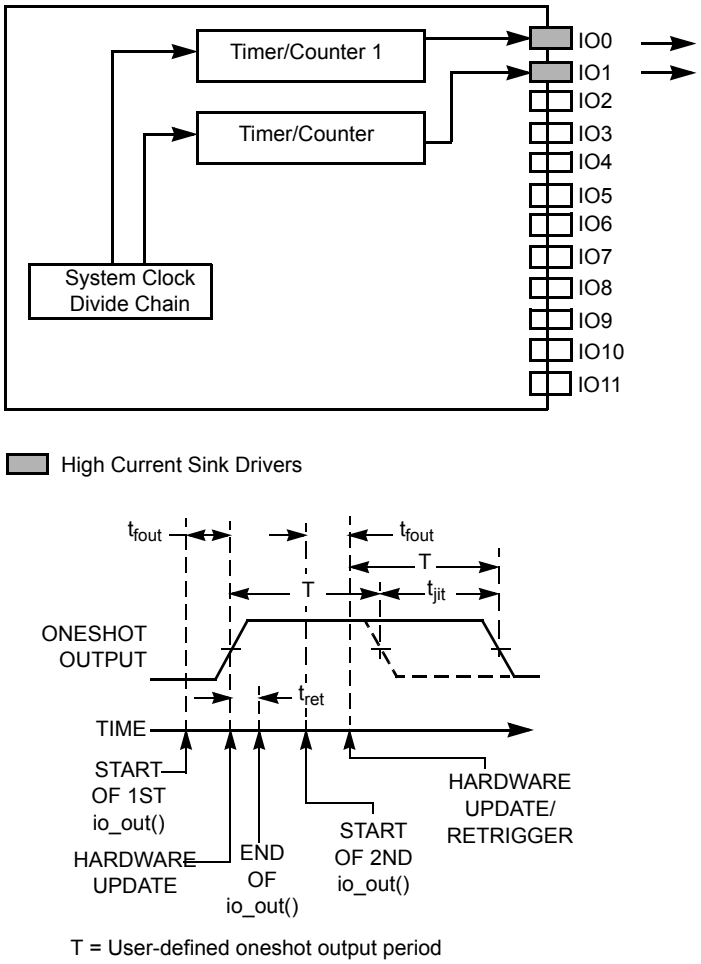


Figure 3.51 Infrared Pattern I/O

Oneshot Output

A timer/counter can be configured to generate a single pulse of programmable duration. The asserted state can be either logic high or logic low. Retriggering the oneshot before the end of the pulse causes it to continue for the new duration. Table 3.8 in the *Notes* section at the end of this chapter gives the resolution and maximum time of the pulse for various clock selections. This object is useful for generating a time delay without intervention of the application processor (see Figure 3.52).



Symbol	Description	Typ @ 10MHz	Max
t_{fout}	Function call to output update	96 µs	—
t_{ret}	Return from function	13 µs	—
t_{jit}	Output duration jitter	—	1 timer/counter clock period*

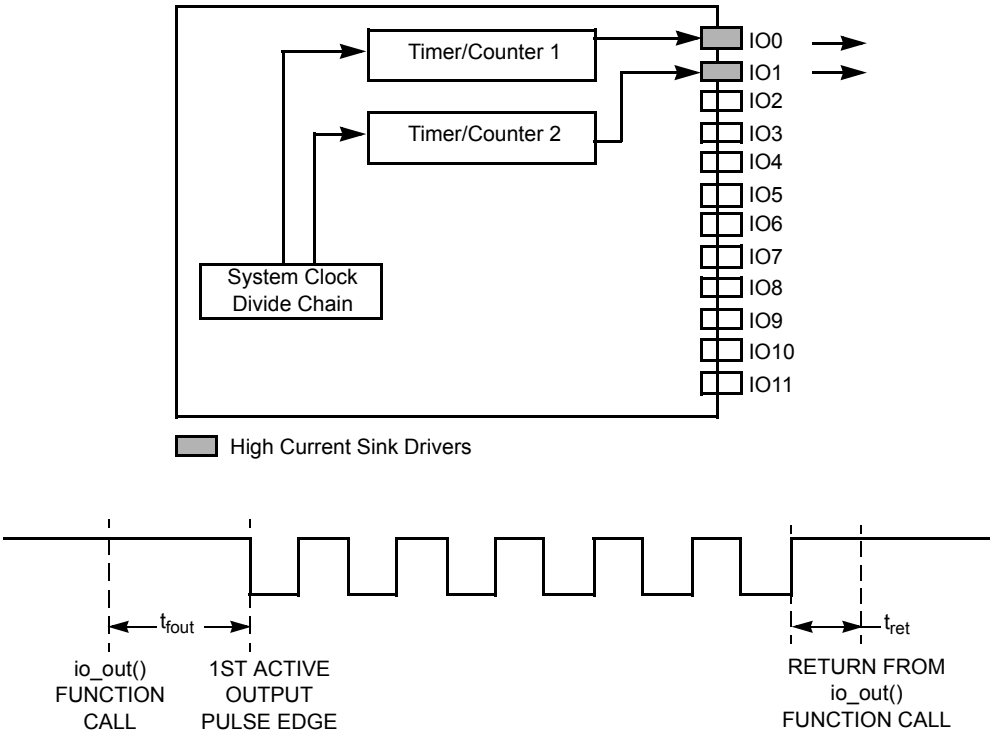
Figure 3.52 Oneshot Output Latency Values

*Timer/counter clock period = (2000ns * 2^(clock))/(input clock in MHz).

While the output is still active, a subsequent call to this function will cause the update to take effect immediately, extending the current cycle. This is, therefore, a retriggerable oneshot function.

Pulsecount Output

A timer/counter can be configured to generate a series of pulses. The number of pulses output is in the range 0 to 65,535, and the output waveform is a square wave of 50% duty cycle. This function suspends application processing until the pulse train is complete. The frequency of the waveform can be one of eight values given by Table 3.9 in the *Notes* section at the end of this chapter with clock select values of 0 through 7. This object is useful for external counting devices that can accumulate pulse trains, such as stepper motors (see Figure 3.53).



Symbol	Description	Typ @ 10MHz
t_{fout}	Function call to first active output pulse edge	115 µs
t_{ret}	Return from function	5 µs

Figure 3.53 Pulsecount Output

The return from this function does not occur until all output pulses have been produced.

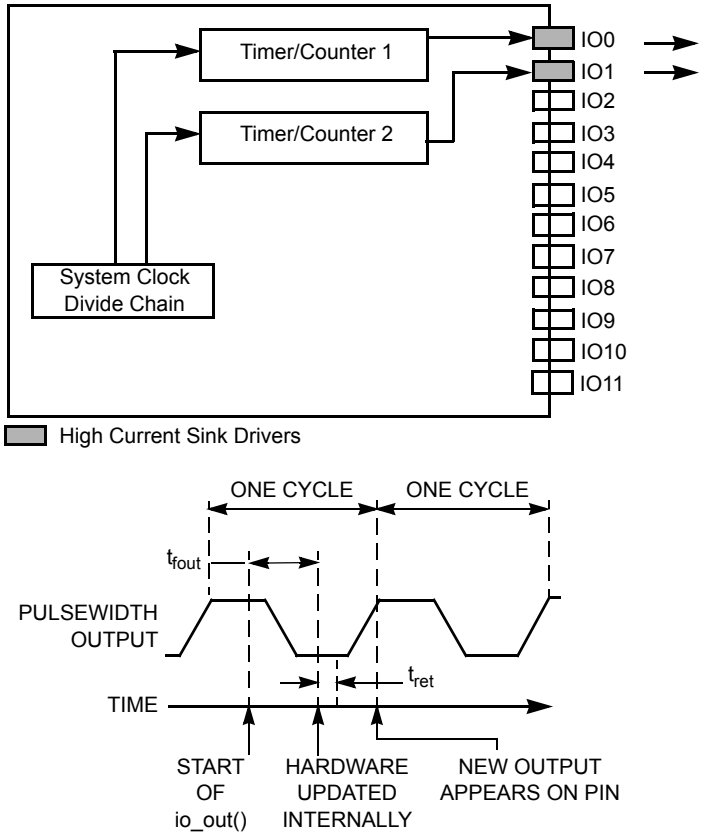
t_{fout} is the time from function call to first output pulse. Therefore, the calling of this function ties up the application processor for a period of N x (pulse period) + t_{fout} + t_{ret}, where N is the number of specified output pulses.

The polarity of the output depends on whether or not the **`invert`** option was used in the declaration of the function block. The default is low with high pulses.

Pulsewidth Output

A timer/counter can be configured to generate a pulsewidth modulated repeating waveform. In pulsewidth short function, the duty cycle ranges from 0% to 100% (0/256 to 255/256) of a cycle in steps of about 0.4% (1/256). The frequency of the waveform can be one of eight values given by Table 3.9.

In pulsewidth long function, the duty cycle ranges from 0% to almost 100% (0/65,536 to 65,535/65,536) of a cycle in steps of 15.25 ppm (1/65,536). The frequency of the waveform can be one of eight values given by Table 3.10 in the *Notes* section at the end of this chapter. The asserted state of the waveform can be either logic high or logic low. Writing a new pulsewidth value to the device takes effect at the end of the current cycle. A pulsewidth modulated signal provides a simple means of digital-to-analog conversion (see Figure 3.54).



Symbol	Description	Typ @ 10MHz
t_{fout}	Function call to output update	101 µs
t_{ret}	Return from function	13 µs

Figure 3.54 Pulsewidth Output Latency Values

The new output value will not take effect until the end of the current cycle. There are two exceptions to this rule. If the output is disabled, the new (non-zero) output will start immediately after t_{fout}. Also, for a new output value of zero, the output is disabled immediately and not at the end of the current cycle.

A disabled output is a logic 0 by default unless the **`invert`** keyword is used in the I/O object declaration.

Triac Output

On the PL Smart Transceiver, a timer/counter can be configured to control the delay of an output signal with respect to a synchronization input. This synchronization can occur on the rising edge, the falling edge, or both the rising and falling edges of the input signal. For control of AC circuits using a triac device, the sync input is typically a zero-crossing signal, and the pulse output is the triac trigger signal. Table 3.8 shows the resolution and maximum range of the delay (see Figure 3.55).

The output gate pulse is gated by an internal clock with a constant period of 25.6µs at 10MHz (39.062µs at 6.5536MHz). because the input trigger signal (zero crossing) is asynchronous relative to this internal clock, there is a jitter, t_{jit}, associated with the output gate pulse.

The actual active edge of the sync input and the triac gate output can be set by using the **`clockedge`** or **`invert`** parameters, respectively.

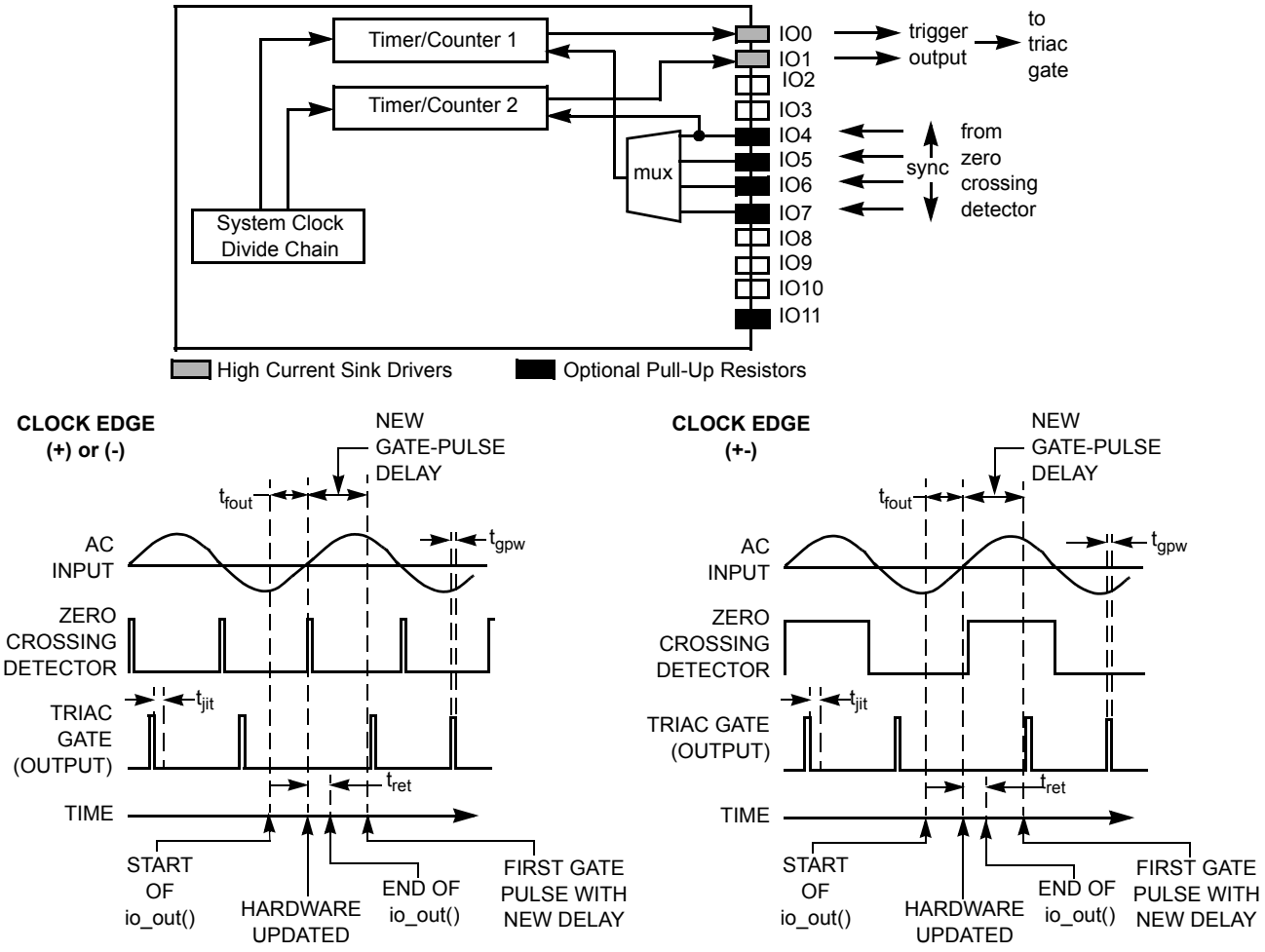


Figure 3.55 Triac Output Latency Values

The hardware update does not happen until the occurrence of an external active sync clock edge. The internal timer is then enabled and a triac gate pulse is generated after the user-defined period has elapsed. This sequence is repeated indefinitely until another update is made to the triac gate pulse delay value.

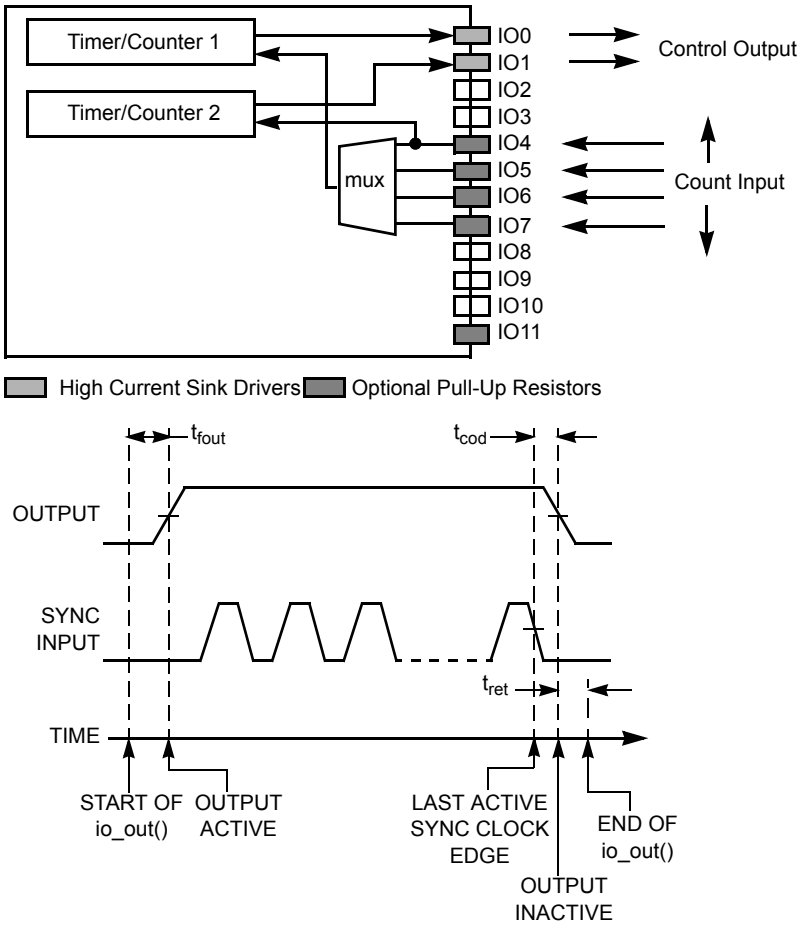
t_{fout} (min) refers to the delay from the initiation of the function call to the first sampling of the sync input. In the absence of an active sync clock edge, the input is repeatedly sampled for 10ms (1/2 wave of a 50Hz line cycle time), t_{fout} (max), during which the application processor is suspended.

The output gate pulse is gated by an internal clock with a constant period of 25.6µs at 10MHz (39.062µs at 6.5536MHz). because the input trigger signal (zero crossing) is asynchronous relative to this internal clock, there is a jitter, t_{jit}, associated with the output gate pulse.

The actual active edge of the sync input and the triac gate output can be set by using the `clockedge` or `invert` parameters, respectively.

Triggered Count Output

A timer/counter can be configured to generate an output pulse that is asserted under program control, and de-asserted when a programmable number of input edges (up to 65,535) has been counted on an input pin (IO4 – IO7). Assertion can be either logic high or logic low. This object is useful for controlling stepper motors or positioning actuators which provide position feedback in the form of a pulse train. The drive to the external device is enabled until it has moved the required distance, and then the device is disabled (see Figure 3.56).



Symbol	Description	Typ @ 10MHz
t_{fout}	Function call to output pulse	109 µs
t_{cod}	Last negative sync Clock edge to output inactive	min 550 ns max 750 ns
t_{ret}	Return from function	7 µs

Figure 3.56 Triggered Count Output Latency Values

The active output level depends on whether or not the **`invert`** option was used in the declaration of the function block. The default is high.

Notes

Various combinations of I/O pins can be configured as basic inputs or outputs. The application program can optionally specify the initial values of basic outputs. Pins configured as outputs can also be read as inputs, returning the value last written.

The gradient behavior of the timing numbers for different PL Smart Transceiver pins for some of the I/O objects is due to the shift-and-mask operation performed by the Neuron firmware.

For dualslope input, edgelog input, ontime input, and period input, the timer/counter returns a value (or a table of values, in the case of edgelog input) in the range 0 to 65,535, representing elapsed times from 0 up to the maximum range given in Table 3.8.

For ontime input, period input, dualslope, edgelog, and infrared; the timer/counter returns a number in the range 0 to 65,535, representing elapsed times from 0 up to the maximum range given in Table 3.8.

For oneshot output, frequency output, and triac output; the timer/counter can be programmed with a number in the range 0 to 65,535. This number represents the waveform ontime for oneshot output, the waveform period for frequency output, and the control period from sync input to pulse/level output for the triac output. Table 3.8 gives the range and resolution for these timer/counter objects at 10MHz. The clock select value is specified in the declaration of the I/O object in the Neuron C application program, and can be modified at runtime.

Table 3.8 Timer/Counter Resolution and Maximum Range

	Oneshot and Triac Outputs; Dualslope, Edgelog, Ontime, and Period Inputs		**Frequency Output**	
Clock Select	**Resolution (µs)**	**Maximum Range (ms)**	**Resolution (µs)**	**Maximum Range (ms)**
0	0.2	13.1	0.4	26.2
1	0.4	26.2	0.8	52.4
2	0.8	52.4	1.6	105
3	1.6	105	3.2	210
4	3.2	210	6.4	419
5	6.4	419	12.8	838
6	12.8	839	25.6	1,678
7	25.6	1,678	51.2	3,355

Note: This table is for a 10MHz input clock. Scale appropriately for other clock rates:

Resolution (µs) = $2^{(\text{Clock Select} + n)}$/(Input Clock in MHz)

Maximum Range (µs) = 65535 x Resolution (µs) x n

n = 1 for oneshot and triac output, and dualslope, edgelog, ontime, and period input

n = 2 for frequency output.

For pulsewidth short output and pulsecount output, Table 3.9 gives the possible choices for pulsetrain repetition frequencies. Pulsecount can not be used with clock select 0.

Table 3.9 Timer/Counter Square Wave Output

Clock Select (System Clock ÷)	Repetition Rate (Hz)	Repetition Period (µs)	Resolution of Pulse (µs)
0 (÷1) (5MHz)	19,531	51.2	0.2
1 (÷ 2) (2.5MHz)	9,766	102.4	0.4
2 (÷ 4) (1.25MHz)	4,883	204.8	0.8
3 (÷ 8) (625 kHz)	2,441	409.6	1.6
4 (÷ 16) (312.5 kHz)	1,221	819.2	3.2
5 (÷ 32) (156.25 kHz)	610	1,638.4	6.4
6 (÷ 64) (78.125 kHz)	305	3,276.8	12.8
7 (÷ 128) (39.06 kHz)	153	6,553.6	25.6

This table is for 10MHz input clock. Scale appropriately for other clock rates:
Period (µs) = 512 x $2^{\text{Clock Select}}$ / (Input Clock in MHz)
Frequency (Hz) = 1,000,000 / Period (µs).

For pulsewidth long output, the table below gives the possible choices for pulsetrain repetition frequencies.

Table 3.10 Timer/Counter Pulsetrain Output

Clock Select	Frequency (Hz)	Period (ms)
0	76.3	13.1
1	38.1	26.2
2	19.1	52.4
3	9.54	105
4	4.77	210
5	2.38	419
6	1.19	839
7	0.60	1,678

This table is for 10MHz input clock. Scale appropriately for other clock rates:
Period (ms) = 131.072 x $2^{\text{Clock Select}}$ / (Input Clock in MHz)
Frequency (Hz) = 1,000 / Period (ms)

As with all CMOS devices, floating I/O pins can cause excessive current consumption. To avoid this, declare all unused I/O pins as bit output. Alternatively, unused I/O pins can be connected to + V_{DD5} or GND.

4

Coupling Circuits

Introduction

This chapter includes a technical discussion about the means by which the PL 3120 or 3150 Power Line Smart Transceiver communication signals are coupled to power mains. Coupling circuit designs, including schematics and electrical safety issues, are included.

Power Line Communications

The PL Smart Transceivers employ sophisticated digital signal processing techniques, a transmit power amplifier with a very low output impedance, and a very wide (>80dB) dynamic range receiver to overcome the signal attenuation and noise inherent in power mains communication. Maintaining the full communication capability of the PL Smart Transceivers requires careful selection and implementation of the mains coupling circuitry associated with those transceivers. This section gives an overview of the sources of signal attenuation as a basis for understanding choices in selecting and implementing mains coupling circuits.

Attenuation is the difference between the signal level at the output of the power line transmitter and the level of that same signal at the input of the intended receiver. While attenuation is often defined as the ratio of power levels, it is referred to in this document as the ratio of the transmitted signal voltage (unloaded) to the voltage of that same signal at the receiver input. A voltage ratio is more convenient to measure because power measurements require knowledge of the circuit impedance which, in the case of the power mains, varies with both location and time.

In power mains communications the attenuation of transmitted signals spans a wide range and is most conveniently denoted in decibels (dB), where voltage attenuation is defined in dB as $20\log_{10}(V_{transmit}/V_{receive})$. Thus 20dB of attenuation means that the signal was reduced by a factor of 10 by the time it arrived at the receiver, 40dB of attenuation corresponds to a factor of 100, 60dB a factor of 1000, and so on. A PL Smart Transceiver is capable of reliably communicating on a low-noise line, such as a dedicated twisted wire pair, when the transmit signal is attenuated by 80dB (a factor of 10,000). Thus a signal transmitted at 7Vp-p ($2.5V_{RMS}$) can be received when reduced to less than 700µVp-p ($250\mu V_{RMS}$).

To better understand the sources of attenuation in a network of power mains, it is helpful to look at a simplified model of a power distribution network. This example is based on an installation having one power distribution panel and two phases of mains power. While many applications for power line communication employ different numbers of phases, different topologies, voltages, and wire types, this example illustrates some of the key issues affecting the successful application of the PL Smart Transceiver.

Figure 4.1 depicts the path that a power line communication signal might traverse, starting from a wall socket and passing through the building's electrical wiring and circuit breaker panel, across power phases, and ultimately to another wall socket. Each socket in the power network can power a device that generates noise and loads the transmitted signal. For clarity, neutral and earth wires have not been shown.

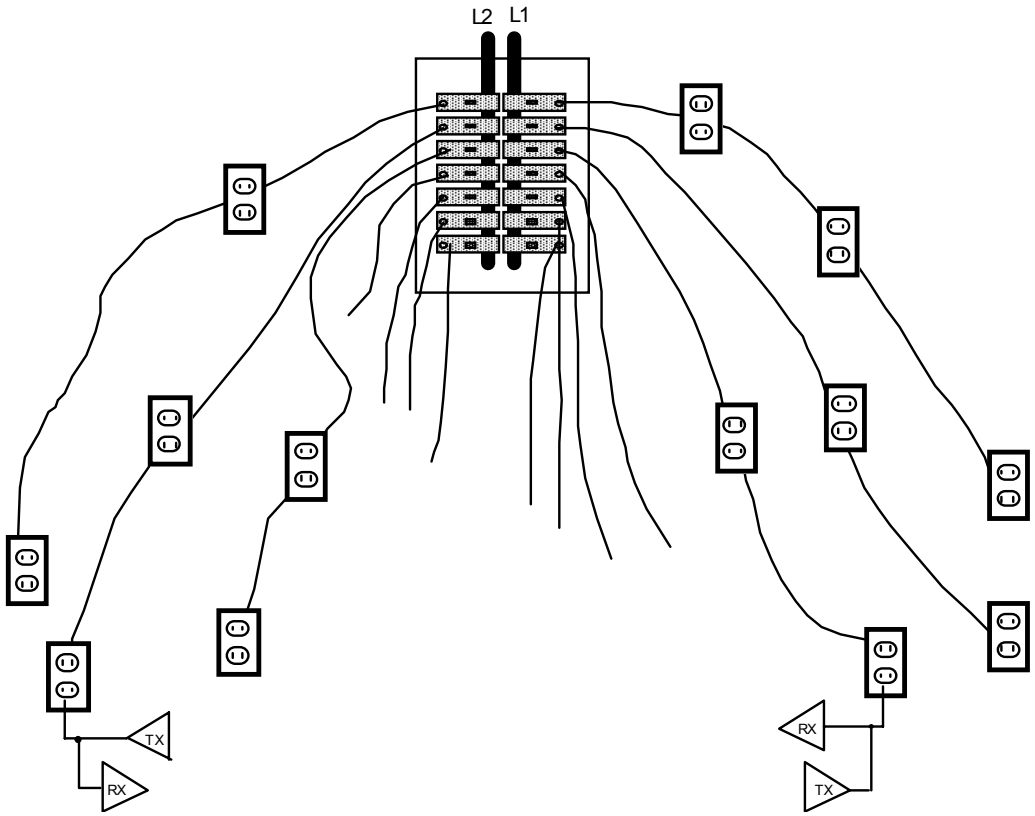


Figure 4.1 Power Distribution Model

Attenuation is most easily understood in terms of a voltage-divider circuit formed by the output impedance of the transmitter, the impedance of the various mains circuit branches, and any loads present on the mains branch circuits. At the communication frequencies of the PL Smart Transceiver (70kHz to 138kHz), the significant impedances are due to the series inductance of the mains wiring itself, capacitive loads between line and neutral, resistive loads between line and neutral, and the coupling between L1 and L2 which occurs due to mutual inductance and parasitic capacitance between phases. If these distributed impedances are lumped together and treated as if a single frequency is being transmitted, a simple attenuation model results as shown in Figure 4.2.

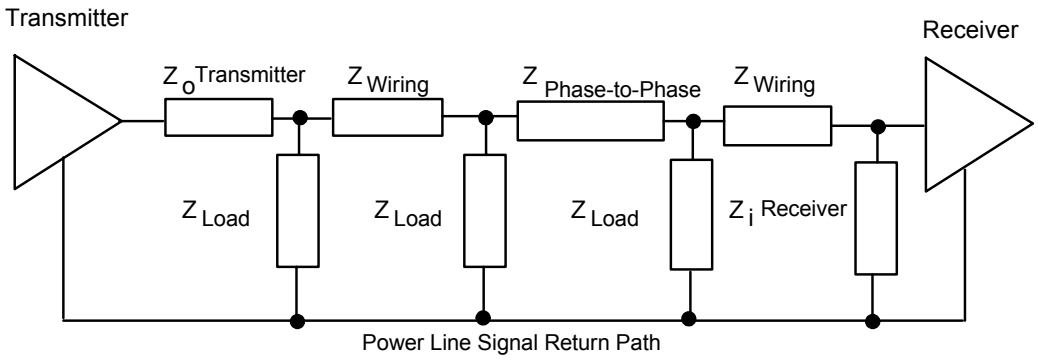


Figure 4.2 Power Mains Attenuation Model

This model illustrates that minimizing the series impedances and maximizing the line-to-return path impedances reduces the attenuation of the transmitted signal.

Coupling Techniques

Power Line Coupling Basics

Injecting a communication signal into a power mains circuit is normally accomplished by capacitively coupling the output of a transceiver to the power mains. In addition to the coupling capacitor, an inductor or transformer is generally present. The coupling capacitor and the inductor or transformer together act as a high-pass filter when receiving the communications signal. The high-pass filter attenuates the large AC mains signal (at either 50Hz or 60Hz), while passing the communication signal of the transceiver. Figure 4.3 shows a basic mains coupling circuit. The value of the capacitor is chosen to be large enough so that its impedance at the communication frequencies is low, yet small enough that its impedance at the mains power frequency (50Hz or 60Hz) is high. The impedance of the capacitor can be considered as part of the transmitter's output impedance ($Z_{oTransmitter}$) shown in Figure 4.2. Keeping the impedance of the coupling capacitor low minimizes the **signal injection loss** caused by the voltage divider formed between the output impedance of the amplifier and the mains loading (Z_{Load}).

The value of the inductor is chosen to have a relatively high impedance at the communication frequencies of the PL Smart Transceiver. The inductor impedance can be considered part of the receiver input impedance ($Z_{i\ Receiver}$) shown in Figure 4.2. Keeping the inductor impedance high helps minimize any signal loss at the receiver due to the voltage divider formed by the wiring impedance and the receiver input impedance.

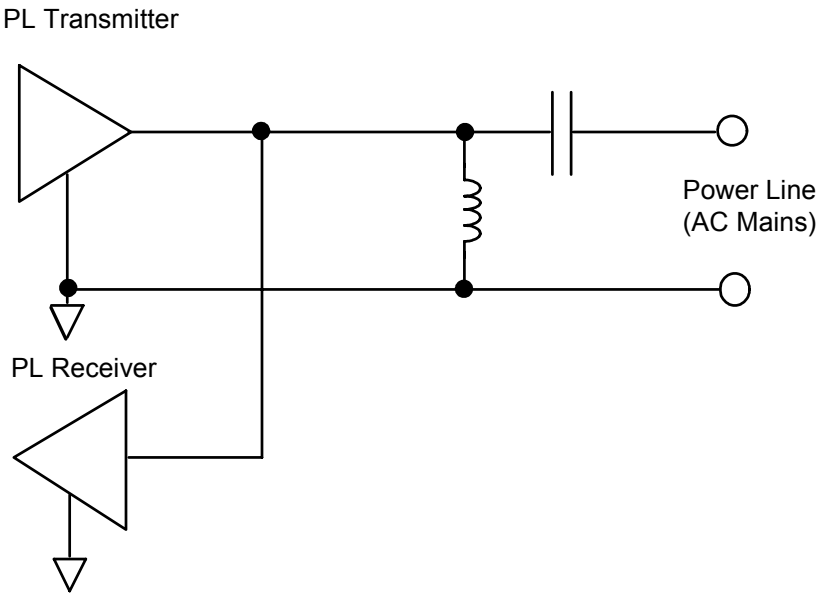


Figure 4.3 Basic Mains Coupling Circuit

A key factor affecting the type of mains coupling circuit to be used is the wiring style of the power distribution system to which the coupling circuit will be connected. Wiring topologies vary from application to application, e.g., homes versus commercial buildings, as well as from country to country. Wiring styles can be divided into two major categories: wiring systems where a separate earth conductor is present and accessible (i.e., safety ground, which is not the same as a neutral wire with an earth bond), and wiring systems where there is no earth conductor.

When an earth conductor is always present, a coupling method known as **line-to-earth** coupling is preferred. In line-to-earth coupling, the communications signal is coupled to the line wire relative to earth, and earth is used as the communications signal return path. This coupling technique is also referred to as **earth-return** coupling. Local restrictions might apply to the use of line-to-earth coupling (see *Ground Leakage Currents* in the *Safety Issues* section of this chapter for more information). As a general rule, line-to-earth coupling is only used in commercial applications in North America and non-EU countries where local electrical codes require the presence of an earth safety ground and permit the associated 50/60Hz leakage current. Figure 4.4 illustrates a simple example of a line-to-earth coupling circuit.

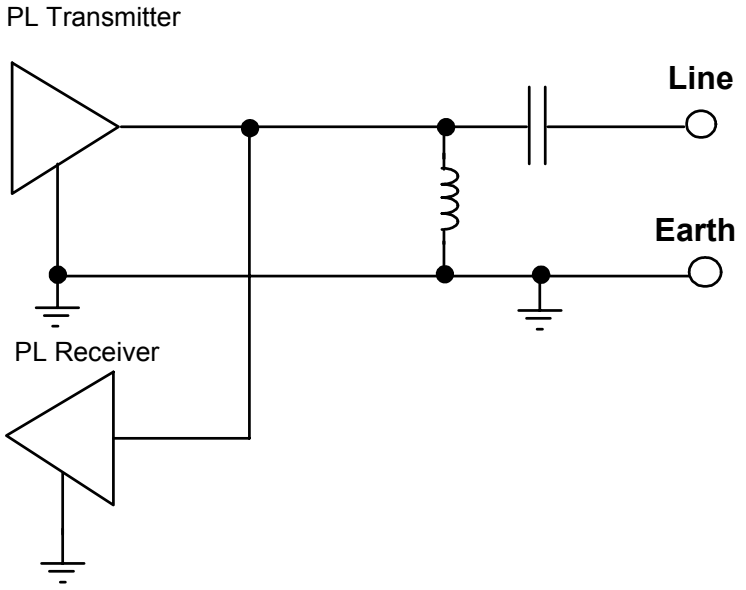


Figure 4.4 Line-to-Earth Coupling Method

To understand the advantage of line-to-earth coupling, recall that a major component of signal attenuation is due to the loads presented by devices that are connected to the power mains between the line and neutral wires. These loads do not affect signal attenuation when line-to-earth coupling is used. Field measurements have shown consistent improvements in received signal-to-noise ratios of more than 15dB for transceivers using line-to-earth coupling, relative to transceivers using non-earth-return coupling. For this reason, when a safety ground connection is known to be available throughout the wiring system, a line-to-earth coupling scheme is preferred.

In applications where a safety ground connection is not always available, or where line-to-earth coupling is precluded by local regulations, the coupling circuit must be connected between the line and neutral wires. This style of coupling is known as either **line-to-neutral** or **neutral-return** coupling. Line-to-neutral coupling is recommended for in-home applications and utility applications world wide, and is illustrated in Figure 4.5.

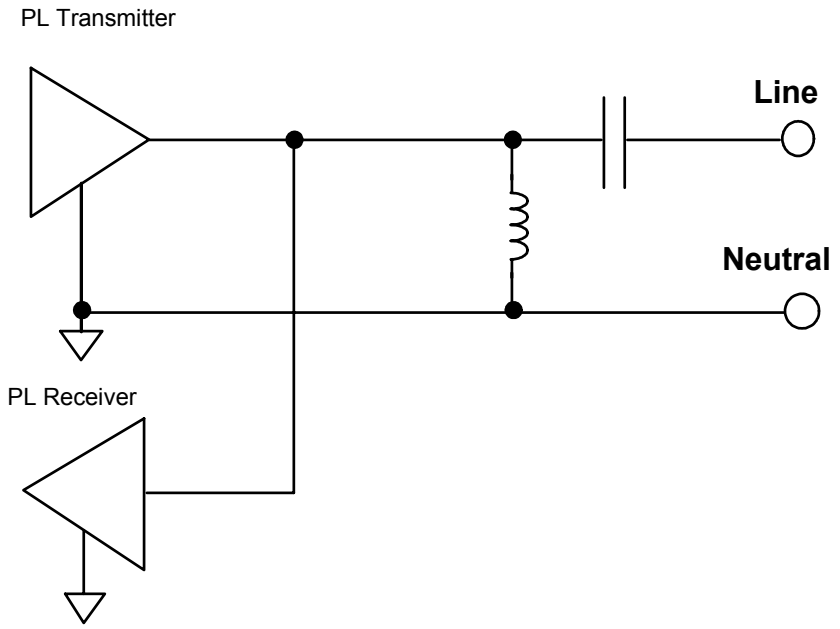


Figure 4.5 Line-to-Neutral Coupling Style

In the following section the simple circuits shown in Figures 4.4 and 4.5 are expanded to make them practical in real applications. The following discussion applies to both line-to-neutral coupling and line-to-earth coupling, as the coupling circuit topology for each is the same. However, in addition to the different mains connections, the required component values differ for line-to-neutral coupling and line-to-earth coupling. At the end of this chapter, recommended coupling circuit schematics and component specifications are provided for both line-to-neutral coupling and line-to-earth coupling.

Power Line Coupling Details

The coupling circuits shown in Figures 4.4 and 4.5 require the addition of a small number of components to make them practical. Figure 4.6 shows the addition of an AC coupling capacitor (C2) to prevent the inductor from shorting the DC bias voltage of the transmit amplifier.

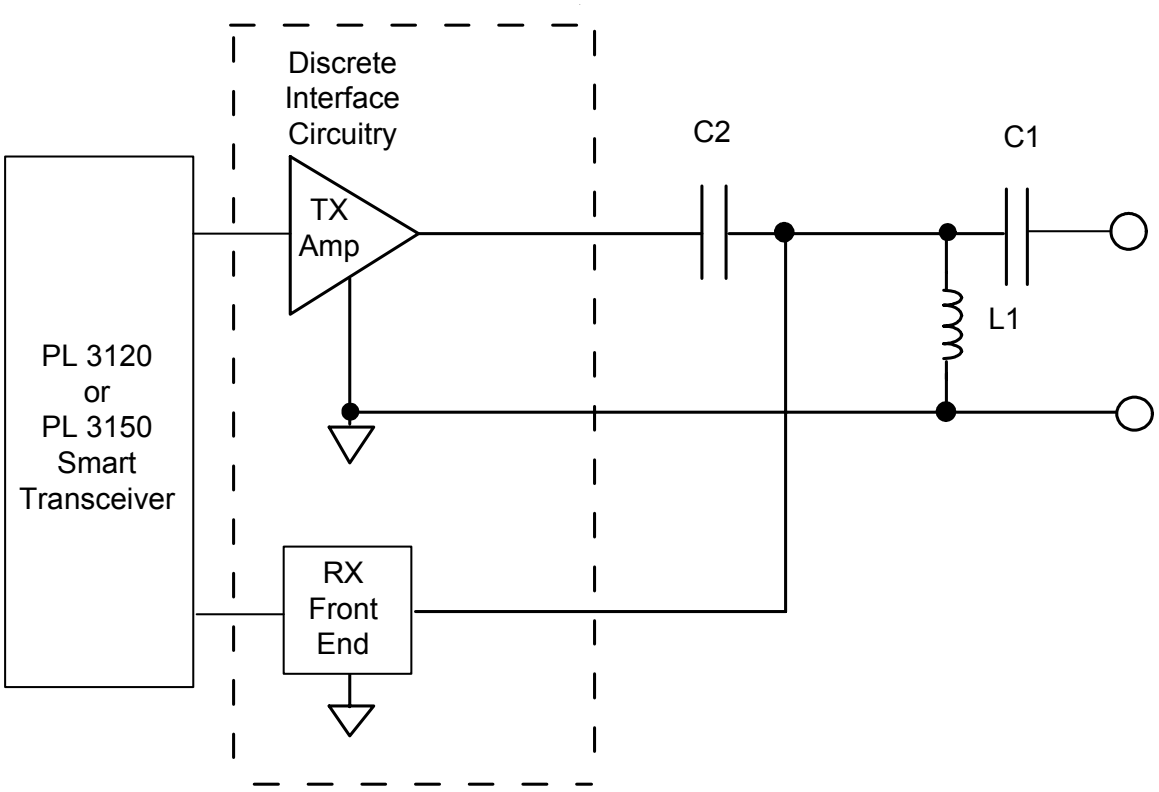


Figure 4.6 Simplified Coupling Circuit with DC Blocking Capacitor

Given the attenuation model presented earlier in Figure 4.2, one critical design constraint is that the series combination of C1 and C2 must have a low impedance at the communication frequencies of the PL Smart Transceiver. The impedance of these capacitors, along with the PL Smart Transceiver transmit amplifier's output impedance, corresponds to "Z_o Transmitter" in Figure 4.2. Because the equivalent load impedance of the power line can in some cases be as low as 1-2 ohms, and because the output impedance of the PL Smart Transceiver transmit amplifier is less than 1 ohm, the impedance of these capacitors should be on the order of 1 ohm so that they do not add significantly to "Z_o Transmitter". While the values of C1 and C2 could be set high enough to meet this goal, doing so would significantly increase the cost of the high-voltage capacitor C1. Because C2 is connected only to low voltage, and thus is lower cost for a given value, its value can be set higher relative to the value of the high-voltage capacitor C1.

A simple and cost-effective way to achieve low transmit impedance with modest size capacitors is to add inductor L2, as shown in Figure 4.7. This inductor forms a series-resonant circuit with C1 and C2, and its value can therefore be chosen to optimize coupling at the communication frequencies of the PL Smart Transceiver while minimizing the cost of C1 and C2. Different values of C1 and L2 are needed for A-band and C-band operation to optimize the performance of a coupler in its respective band. The component values listed with the example coupling circuits documented later in this chapter include values optimized for each application and band of operation.

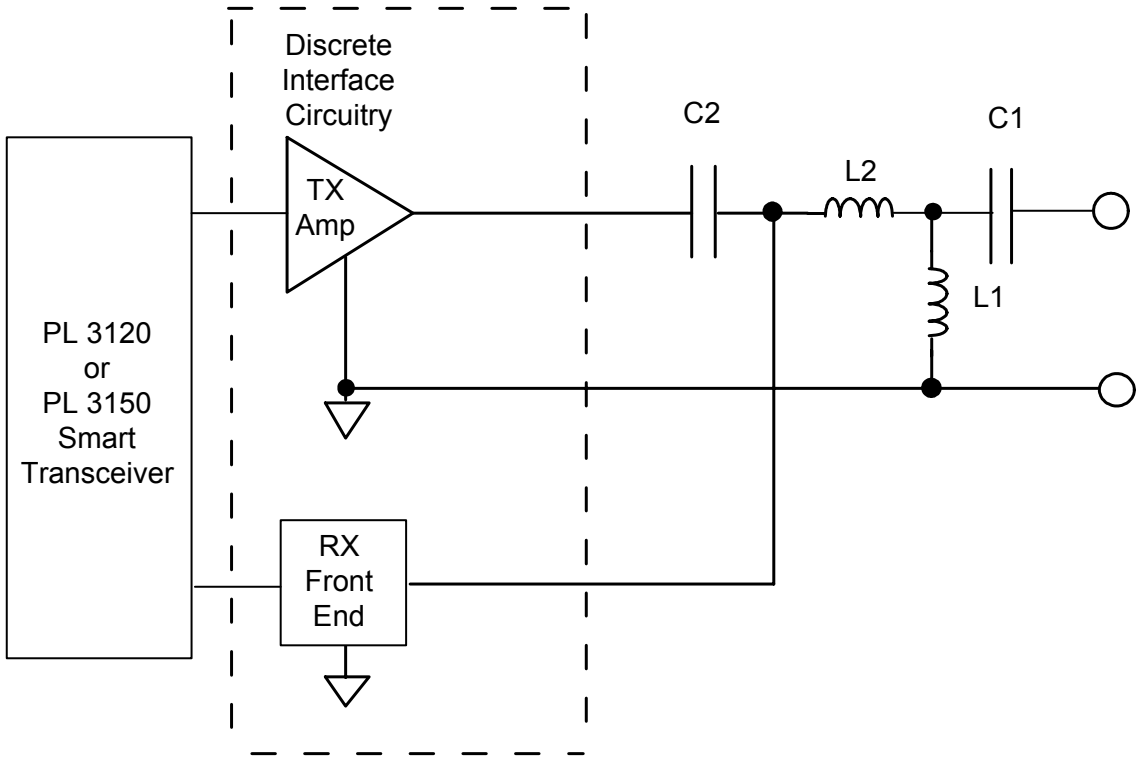


Figure 4.7 Simplified Coupling Circuit with Resonant Inductor

An important design constraint on L2 is that its DC resistance must be kept very low because it is in the transmit signal path and effectively part of the transmitter's output impedance. Low-cost inductors with DC resistance on the order of 0.2 ohms are widely available.

It is critical that no additional series impedance be added in the signal path between the PL Smart Transceiver transmit amplifier and the power mains (or in the return path from the power mains to the ground pins of the PL Smart Transceiver) unless verified to be significantly less than 1 ohm between 70 and 138kHz.

To illustrate the importance of maintaining a low impedance signal path, consider the example of a ferrite bead with an impedance of 9 ohms at 100kHz added in series with the line. In this case the signal injected into a 1 ohm power line would be reduced *by a factor of 10*. Under typical conditions, the end product would still function, however, communication margin and reliability over a full range of power line environments would be severely compromised. For the same reason, the impedance of series circuit protection elements must also be kept very low. Low current fuses (<2A) and protection devices that can be reset generally add unacceptable series impedance to the signal path. Ferrite beads, unless carefully selected to be a low impedance at 100kHz, offer too much series impedance.

Most devices built with the PL Smart Transceiver do no need ferrite beads in order to pass EMC regulations. If, due to other noise generating circuitry ferrite beads are required, then refer to the end of Chapter 6 for a discussion of acceptable topologies.

To maintain a low impedance signal path, all of the circuit board traces between the output of the transmit amplifier and the AC mains wiring should be at least 1.3mm (50 mils) wide and less than 13cm (5 inches) long. The corresponding signal return path should either be a copper plane or a trace that is at least 1.3mm wide.

Capacitors C1 and C2 should be of metallized film construction in order to minimize equivalent series resistance and provide adequate surge immunity.

Figure 4.8 shows additions to the coupling circuit which are required to make it fully functional. The first is an inductor, L3, connected to the PL Smart Transceiver receive filtering circuitry. The DC resistance of L3 can be up to 55 ohms. The second consists of diodes, D1 and D2, connected from the transmitter to the amplifier supply rails to protect the inputs of the PL Smart Transceiver from large (>18V) transients. Bypass capacitor C3 also has been added to emphasize the fact that it is an integral part of the coupling circuit. One of the functions of this capacitor is to protect the V_A supply line from excessive overshoot when positive going line surges discharge through diode D1. Because positive polarity surge events cause high currents to flow through D1 and C3 back to ground, the trace between D1 and C3 should be at least 1.3mm (50 mils) wide and no more than 1.3cm (0.5 inches) long. To properly control ripple on the V_A supply of the transmit amplifier, the trace between the V_A input of the transmit amplifier and C3 should also be at least 1.3mm wide and no more than 2.5cm long (see the dotted-line arrows at the top of Figure 4.8).

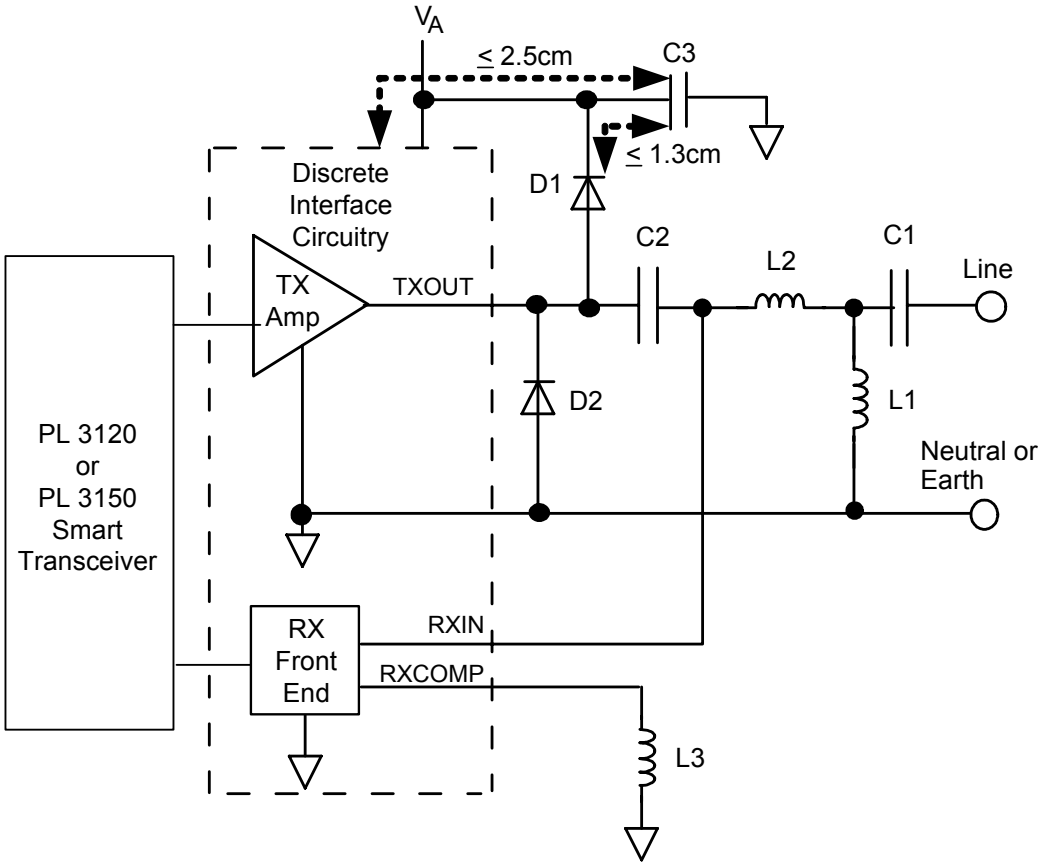


Figure 4.8 Functional Line-to-Neutral or Line-to-Earth Coupling Circuit

In instances where large ambient magnetic fields might be present (such as from switched mode power supply open frame magnetic elements), it is possible that one or more of the PL Smart Transceiver coupling circuit inductors might pick up these stray fields and conduct them onto the power mains. Depending on the frequency and amplitude of these fields they could result in failure to meet CENELEC or FCC conducted emission regulations.

If noise from parasitic coupling is suspected, it can be confirmed by inserting a 10cm (4 inch) twisted wire pair in series with one of the inductors in question. If the conducted noise spectrum varies by more than a few dB when this inductor is moved closer to, and farther from, other components, then parasitic coupling might be the source of the problem.

If stray coupling is a problem, regulations can usually be met by adjusting the location or orientation of the radiating device relative to the coupling circuit inductors. Alternately, shielded or toroidal inductors can be used to reduce coupling as long as all electrical parameters specified in the example coupling circuit tables given later in this chapter are met. If, however, a toroidal or shielded inductor is used in place of L2, then the selected part must handle the maximum output current of the PL Smart Transceiver transmit amplifier without approaching saturation. If L2 even approaches saturation it can add harmonics of the PL Smart Transceiver transmit signal which might result in failure to meet CENELEC or FCC emission regulations (in this instance, due to inductor distortion instead of a stray pickup). For this reason, a shielded or toroidal inductor used for L2 should have DC current rating two or three times higher than listed in the example circuits given later in this chapter. The recommended open frame axial inductors do not need this extra operating margin due to the linearity provided by a magnetic path that is partly in air.

Coupling Circuit Receive Impedance

To avoid attenuating receive signals, the transmit amplifier of the PL Smart Transceiver is switched to a high impedance state (approximately 500 ohms) when it is not transmitting. The receive-mode impedance of the PL Smart Transceiver circuitry, in conjunction with the coupling circuits recommended in this chapter, is greater than 250 ohms in the band of communication (70kHz to 90kHz for A-band and 110kHz to 138kHz for C-band).

Regulations in some countries might set a lower limit on receive-mode impedance outside the communication frequency range. The receive-mode impedance of most coupling circuits dips near 10kHz due to a series resonant effect between the line coupling capacitor (C1) and the coupling inductor (L1). This dip in receive-mode impedance near 10kHz does not have any adverse effect on the communication performance of the PL Smart Transceivers. If local regulations require a minimum out of band receive impedance of 5 ohms, then this can be accomplished by selecting an inductor, L1, which has more than 5 ohms of DC resistance. In order to meet conducted emission regulations, the DC resistance of this inductor should not exceed 14 ohms, as specified in the example coupling circuits shown later in this chapter.

Safety Issues

This guide is intended only as an introduction to some of the safety issues associated with designing circuits using the PL Smart Transceiver. This document is not a primer on electrical safety or electrical codes, and it is the responsibility of the user to familiarize himself or herself with any applicable safety rules or regulations. A review of all designs by competent safety consultants and the pertinent regulatory or safety agencies is strongly recommended.

Safety Isolation Considerations

Many products include an isolation barrier in the form of an insulated enclosure between a user and any hazardous conductors. A typical product of this type is a light switch in which the PL Smart Transceiver and all of the associated electrical components are contained inside the switch enclosure. The type of coupling circuit that can be used in these applications is called a *non-isolated coupling circuit*. A non-isolated coupling circuit generally requires lower cost components, making it especially desirable for use in price-sensitive consumer products and wiring devices. All of the coupling circuit examples that have been shown so far are of the non-isolated type.

Some products cannot rely on their enclosure as a safety isolation barrier and an alternate method of safety isolation must then be provided. For example, a circuit board that used a non-isolated line-to-neutral coupling circuit in conjunction with a PL Smart Transceiver whose I/O pins are user-accessible would present a potential electrical shock hazard. Because the mains neutral lead is connected directly to the circuit board common, the user could be exposed to a hazardous voltage at the I/O connector, especially if the line and neutral connections are accidentally reversed. Additional circuitry is needed in such a product to provide a safety isolation barrier between the user-accessible I/O connector and the mains line and neutral conductors.

The most common solution is to provide isolation in the coupling circuit by modifying the simple coupling circuit described earlier. This style of coupling circuit is referred to as an **isolated coupling circuit**.

The preferred isolated coupling circuit uses **transformer-isolation**. Transformer-isolation requires substituting a safety agency-approved transformer having the appropriate communication characteristics in place of L1 (see Appendix C). Transformer-isolation can be used for both line-to-neutral and line-to-earth coupling. Transformer-isolated coupling has the advantage that the resonant inductor L2 can be incorporated into the isolation transformer by designing the leakage inductance of the transformer to match the value of L2. A transformer-isolated coupling circuit is shown in Figure 4.9, where it can be seen that the transformer isolates the PL Smart Transceiver from the line conductor and the neutral or earth conductor.

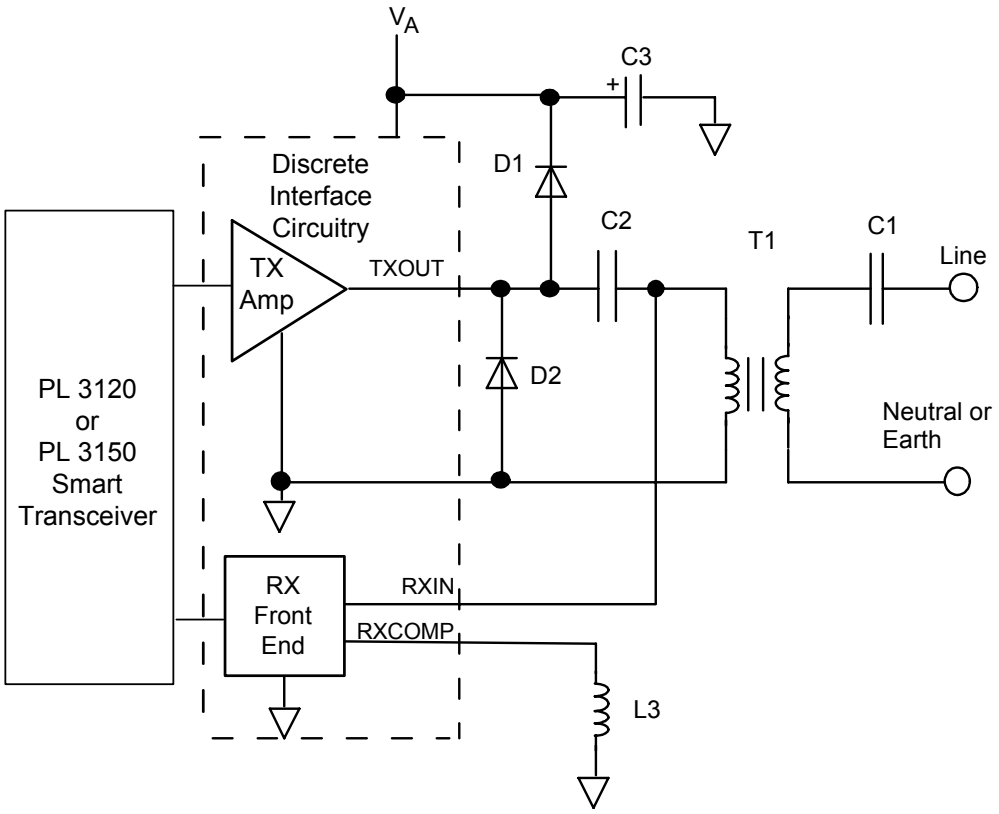


Figure 4.9 Functional Transformer-Isolated Coupling Circuit

The receive-mode impedance of this circuit dips near 10kHz due to the series resonant effect between C1 and T1. This dip in out-of-band impedance does not have any adverse effect on communication performance. If local regulations require a minimum receive impedance at this resonant frequency of greater than 5 ohms, then an optional series RLC circuit can be added as shown in Figure 4.10.

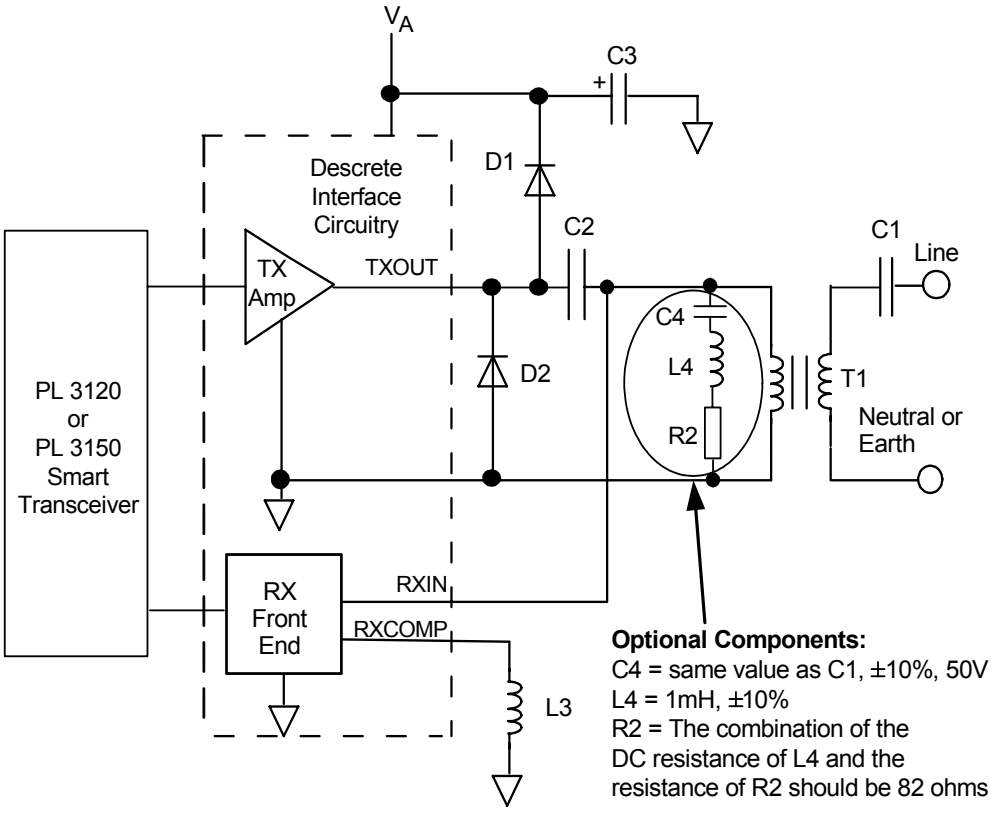


Figure 4.10 Transformer-Isolated Coupling Circuit with Optional RLC Circuit

Ground Leakage Currents

In power line systems that use line-to-earth coupling, there are both safety and practical limits on the level of ground leakage currents that are permitted. In the case of products intended for use in commercial buildings and homes, many safety agency standards set a maximum limit of 3.5mA of ground leakage current. This leakage limit determines the maximum value of C1 (in Figures 4.8 and 4.9) for line-to-earth coupling circuits. In the application schematics that follow, the value of C1 has been chosen to limit the ground leakage current to less than 3.5mA.

A practical limit on the use of line-to-earth coupling also exists. Many single circuit ground fault interrupters (GFIs), also known as residual current devices (RCDs), can be triggered with ground currents as low as 4mA. If each PL Smart Transceiver employing line-to-earth coupling generates about 3mA of ground current, then only one such transceiver can be installed on each GFI-protected circuit. For this reason line-to-earth coupling might not be suitable for some applications with low-current GFIs, and line-to-neutral coupling should be used instead. Local regulations also might prohibit the use of earth as the return path for a signaling system.

Capacitor Charge Storage

The coupling capacitors depicted in the earlier figures can retain substantial charge even after a PL Smart Transceiver-based device has been disconnected from the power mains. This can be of significant concern in applications where a line cord could be touched by a user after being disconnected from the power mains. To minimize potential shock hazard, coupling circuits should include a large value bleeder resistor to discharge the coupling capacitors following disconnection from the mains. Even in applications where the connection to the mains is permanently wired, it is good practice to include the resistor to protect service personnel. The coupling circuit schematics shown later in this chapter include appropriate bleeder resistors. If an alternate path to discharge this capacitor exists (such as the primary winding of a linear power supply transformer) then this bleeder resistor can be eliminated.

Fuse Selection

Safety considerations might require a fuse in series with the mains connection. For an end product to continue to function (without user intervention) it is necessary that the selected fuse not open following a specified line surge. A minimum 6A time-lag (“slow blow”) rating has been shown to be necessary to avoid unintentional fusing action at “high system exposure” surge levels specified by IEEE C62.41-1991.

If a coupling circuit that incorporates varistor protection is selected, the recommendations of the varistor manufacturer for maximum fuse current should be followed. Several varistor manufactures recommend a maximum fuse rating of 6A to 6.3A for use with 1200A surge-rated varistors and a maximum rating of 18A for use with 4500A surge-rated varistors.

A 6A or 6.3A time-lag fuse is specified in all of the coupling circuit examples shown later in this chapter because it satisfies all of the above criteria, as well as the critical requirement that it add very little resistance (<0.1 ohms) to the transmit signal path. If a current rating greater than 6.3A is required by the application then a varistor with a surge rating of >2000A is recommended.

3-Phase Coupling Circuits

When power line communication devices are located on different AC power phases, a significant portion of the overall attenuation between these devices is caused by loss in crossing phases (typically 10-20dB). Most of this loss can be avoided if one of two communicating nodes connects to all power phases as illustrated in Figure 4.11. If all communications are to (and from) a device located at a central distribution panel, then the use of a 3-phase coupling circuit in that device is recommended to maximize communication distance. Due to the fact that this central device must drive the parallel combined impedance of from all three phases, a higher current transmit amplifier is recommended for use in these locations.

The standard transmit amplifier recommended for use in most PL Smart Transceiver-based products includes circuitry to limit output current to 1Ap-p (so that the amplifier will not be damaged when driving very low impedance lines). An alternate transmit amplifier, which can provide 2Ap-p of output is recommended for use with 3-phase couplers. The appropriate transmit amplifier can be implemented using an optional discrete interface circuit with the PL Smart Transceiver. Reference design implementations for both the 1Ap-p and 2Ap-p interface circuitry are available, and are summarized in Appendix A.

Note that the return path for a 3-phase coupling circuit can be either neutral or earth, whichever is appropriate for the application. Note also that a 3-phase earth-return coupling circuit does not result in the same ground leakage current as a single-phase line-to-earth coupling circuit. The ground leakage current of a 3-phase earth-return coupling circuit is nominally zero. This is due to the cancelling effect of the three leakage currents through C1A, C1B, and C1C, which are 120 degrees out of phase with each other.

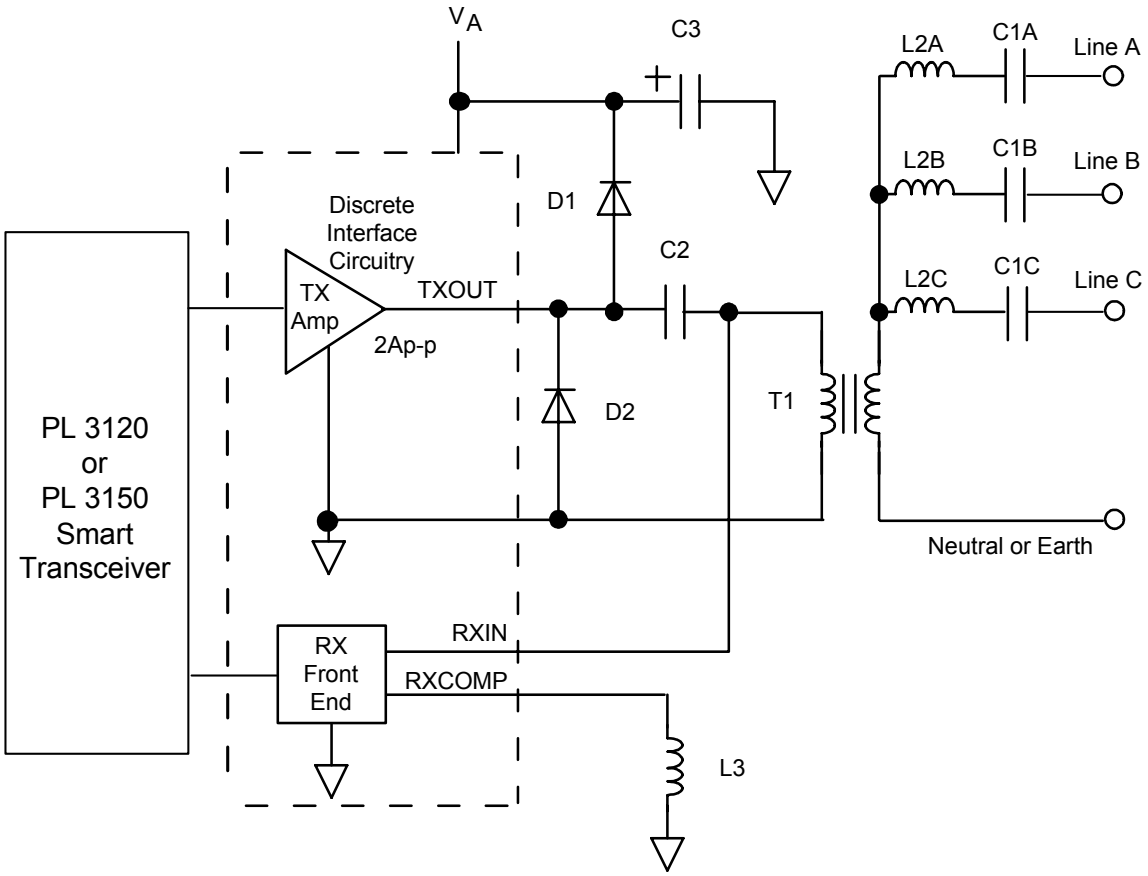


Figure 4.11 Transformer Isolated 3-Phase Coupling Circuit

"2-Phase" Coupling Circuits

Utility service to homes in North America and Japan is typically provided by two hot lines that are 180 degrees out of phase with each other (as well as a neutral return lead). This type of distribution is accomplished by use of a neighborhood transformer, whose primary winding is connected to one phase of a several thousand volt 3-phase distribution system (see Figure 4.12). The secondary winding of this transformer has a center tap that is referenced to ground while the ends of the secondary winding provide the two out-of-phase hot lines that feed each home. This type of distribution system is sometimes referred to as "2-phase" distribution wiring because the 2 hot lines are out of phase with each other.

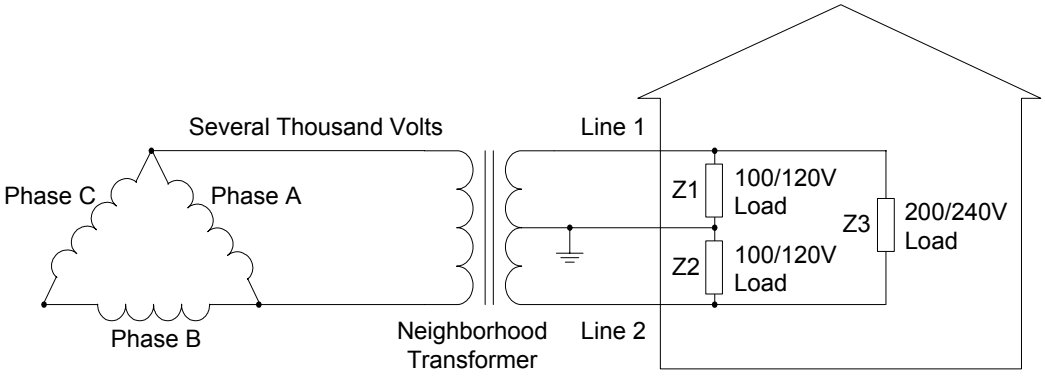


Figure 4.12 2-Phase Power Distribution

In a 2-phase system the majority of devices are connected between one of the two hot lines and the neutral line, while higher power loads are connected between both hot lines. Figure 4.13 illustrates the wiring in a typical North American or Japanese home. North American homes built after the 1960s would have a safety connection (E) available at every outlet. North American homes built before 1960 typically have only Neutral (N) and either L1 or L2 available at each 120VAC outlet. 240VAC outlets generally have E available but N is often not available. Note that N and E are bonded together near the electricity meter.

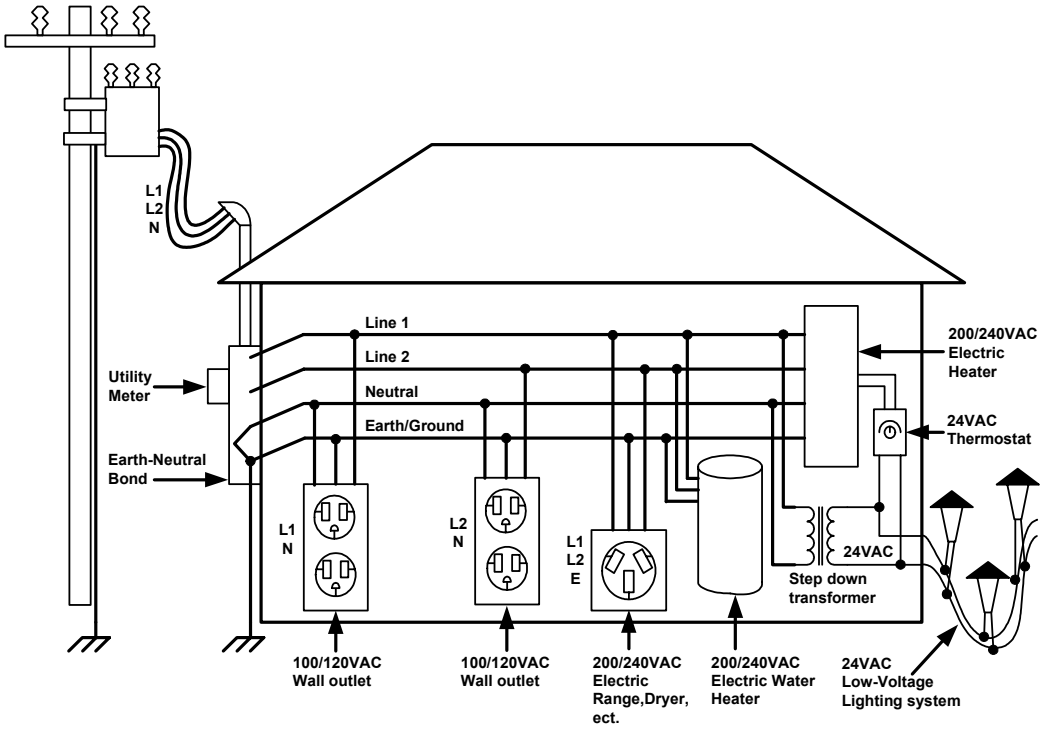


Figure 4.13 2-Phase Home Wiring

The recommended coupling circuits for 2-phase applications are based on the assumption that 2-phase applications require a very high degree of customer satisfaction and thus signal loss between devices on different phases (or between single-phase and 2-phase devices) must be minimized. Coupling the communication signal to both L1 and L2 relative to earth and taking advantage of the Neutral to Earth bond provides robust communication between a 2-phase load and a single phase device (see Figure 4.14). This method of coupling avoids significant signal loss that would otherwise occur when communicating between 2-phase and single-phase devices. Most 2-phase devices have an Earth wire readily available.

In the case of an electricity meter, a "Neutral pigtail" from the meter can be screwed into the sheet metal box that the meter plugs into. This has been found to be the best system level solution for 2-phase applications. Adding one additional capacitor, C4, between L1 and L2 further improves system reliability by minimizing signal loss between single-phase devices connected to opposite phases. Component values and part numbers for isolated and non-isolated versions of this circuit are shown in Examples 7 and 8 later in this chapter.

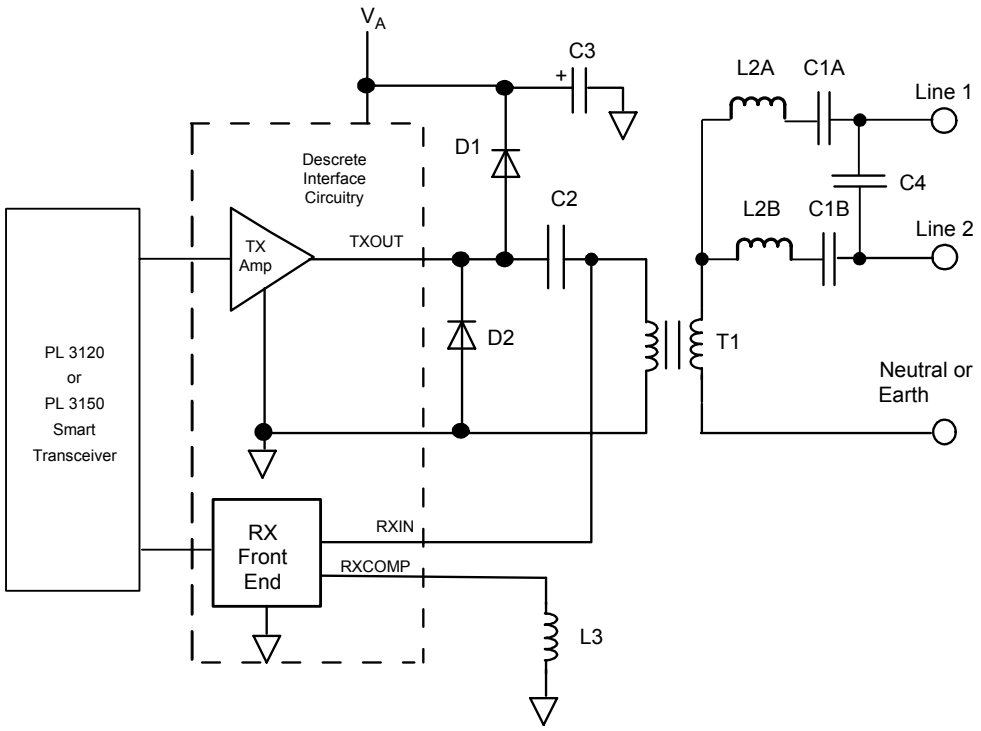


Figure 4.14 Transformer Isolated 2-Phase Coupling Circuit

Note that the return path for a 2-phase circuit can be either neutral or earth, whichever is appropriate for the application. Note also that a 2-phase earth-return coupling circuit does not result in the same ground leakage current as a single-phase line-to-earth coupling circuit. The ground leakage current of a 2-phase earth-return coupling circuit is nominally zero. This is due to the cancelling effect of the two leakage currents through C1A and C1B, which are 180 degrees out of phase with each other.

Line Surge Protection

Coupling circuits that connect the PL Smart Transceiver to the power mains require the addition of one or more components to provide protection for the PL Smart Transceiver from the high-voltage surges that occur on power distribution systems. Primarily lightning induced, these surges can present voltages of up to 6kV at very high current levels, for brief periods, to the coupling circuits inside buildings and homes. Even higher voltages can be seen on mains wiring outside of buildings.

The level of surge protection required for a given product often depends on the installed location of the product to be protected. Devices connected to branch circuits within a building or home are typically subject to the lowest level of surge stress. Devices connected at, or close to, the power entry point of a building or home (for example, electrical meters and main breaker panels) are subject to higher levels of surge stress. Devices connected to outdoor wiring are subjected to the highest levels of surge stress.

Standard tests for surge immunity are defined in **IEEE C62.41-1991**[8]and **CEI/IEC 61000-4-5**[7]. Both documents classify levels of surge stress by the type of surge waveform (either Ring wave or Combination wave), surge voltage, and surge current. In addition to describing standard test methods, both documents also suggest surge immunity levels based on the application environments described above.

The recommended test procedures described in the two documents are the same, but the suggested immunity levels called out in IEEE C62.41-1991 substantially exceed the suggested immunity levels of CEI/IEC 61000-4-5. The more severe (and thus more conservative) immunity levels called out in IEEE C62.41-1991 were used in characterizing the recommended surge protection circuitry shown in the PL Smart Transceiver coupling circuit examples of this chapter (up to the limits of available test equipment).

Surge protection with earth-return coupling is often constrained by the need to maintain low leakage current. A varistor connected between line and earth adds leakage current that might result in violation of applicable safety standards. For this reason the use of a varistor for surge protection in single-phase line-to-earth coupling circuits is often prohibited. Adequate surge immunity in single-phase branch circuit applications can be achieved without varistors by the use of an X2-type capacitor in the C1 location. Surge immunity of single-phase line-to-earth coupling circuits can be increased to provide protection for power entry and outside wiring applications by the use of a gas tube surge arrester between line and earth. Varistors can be used in 3-phase and 2-phase earth-return applications because the leakage current from each of the phases cancels.

If a gas tube surge arrestor or varistor is used between line and earth, it will have to be loaded on the PCB after hi-pot testing. Hi-pot testing between line and earth is usually performed at voltages above the break-down voltage of gas tube surge arrestors (or the clamp voltage of varistors). The hi-pot test will fail if a gas tube surge arrestor fires (or the varistor clamps) during the testing.

Low-Voltage Coupling Circuits

The following sections discuss low-voltage (≤48Vpk) AC and DC coupling circuits.

Low-Voltage AC Coupling Circuits

For applications where power line communication on ≤48Vpk low-voltage AC power lines (for example, the thermostat or low-voltage lighting system of Figure 4.13) the size and cost of several of the coupling components can be reduced. Component values and part numbers for simplified low-voltage AC coupling circuits are shown in Examples 9 and 10 later in this chapter.

Low-Voltage DC Coupling Circuits

For applications where power line communication on ≤48V low-voltage DC power lines is required (for example, 12V automotive systems) the coupling circuit can be simplified by removing the high-pass filter components L1 and C1 as shown in Figure 4.15. Component values and part numbers for this circuit are shown in Example 11 later in this chapter.

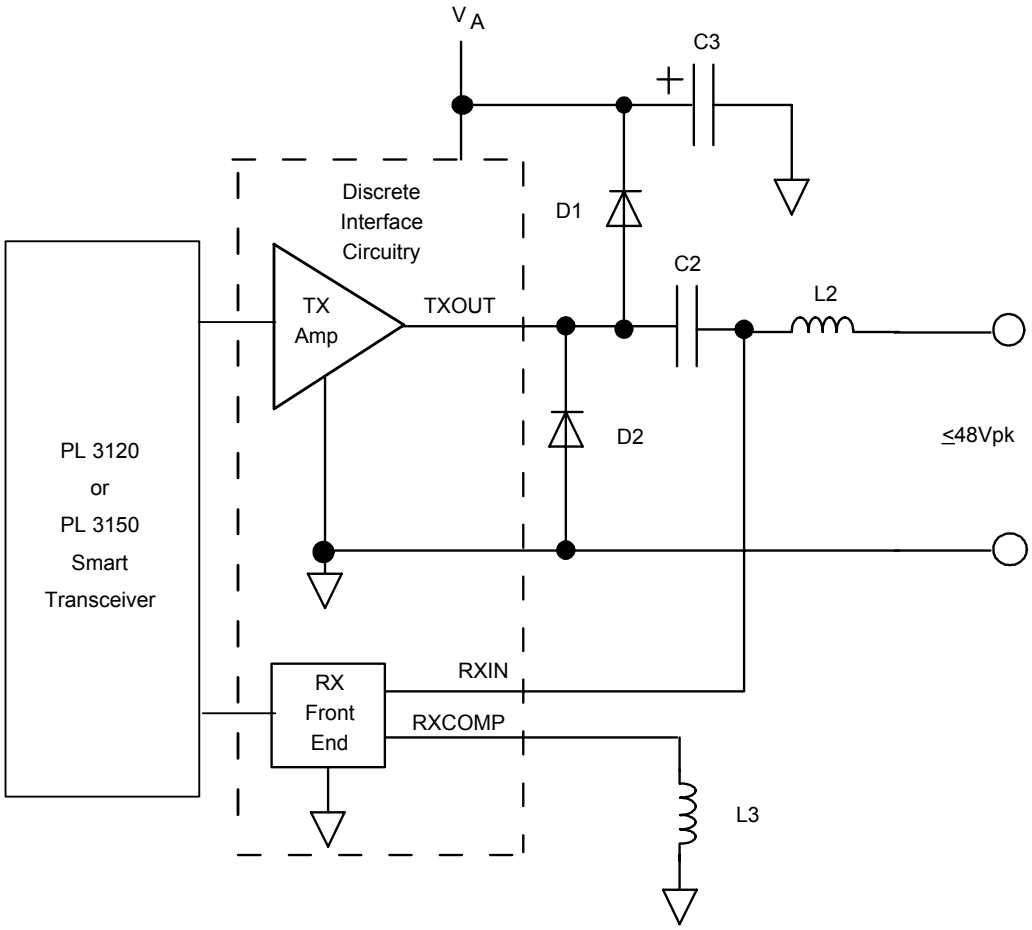


Figure 4.15 Low-Voltage DC Coupling Circuit

Low-Voltage Coupling Circuit Component Reduction

Bleeder resistors and varistors can also be eliminated from both low-voltage AC and DC coupling circuits if the line voltage is less than 48Vpk. The user needs to determine the appropriate surge requirements for their particular low-voltage environment and then perform surge testing applicable to that environment.

Wall-Plug Coupler and Power Supply

One very convenient coupling circuit implementation combines a L-N coupling circuit with a 50/60Hz wall-plug power supply as shown in Figure 4.16. The 50/60Hz transformer inside the Wall-Plug Coupler/Power Supply provides power for the PL Smart Transceiver-based product while the communication transformer couples the communication signal to the product over a common pair of low-voltage wires. Inside the PL Smart Transceiver-based product the power and communication signals are separated to perform their respective functions. Inductor L6 is used to prevent the low impedance of C3 from shorting out the communication signal. The purpose for zener diode Z3 is to prevent the V_A supply voltage from exceeding 18V with high AC line voltage and light load. Ferrite bead L2 has been added to ensure stability of the transmit amplifier with the coupling transformer being remotely located from the PL Smart Transceiver. The particular bead that is specified has been selected to have less or equal to 0.5 ohms of impedance at 100kHz so that a low value of transmit-mode impedance is maintained at communication frequencies. Tamura Corporation makes both a 120VAC and 230VAC Wall-Plug Power Supply/Coupler to support this design. Component values and part numbers for this circuit are shown later in this chapter.

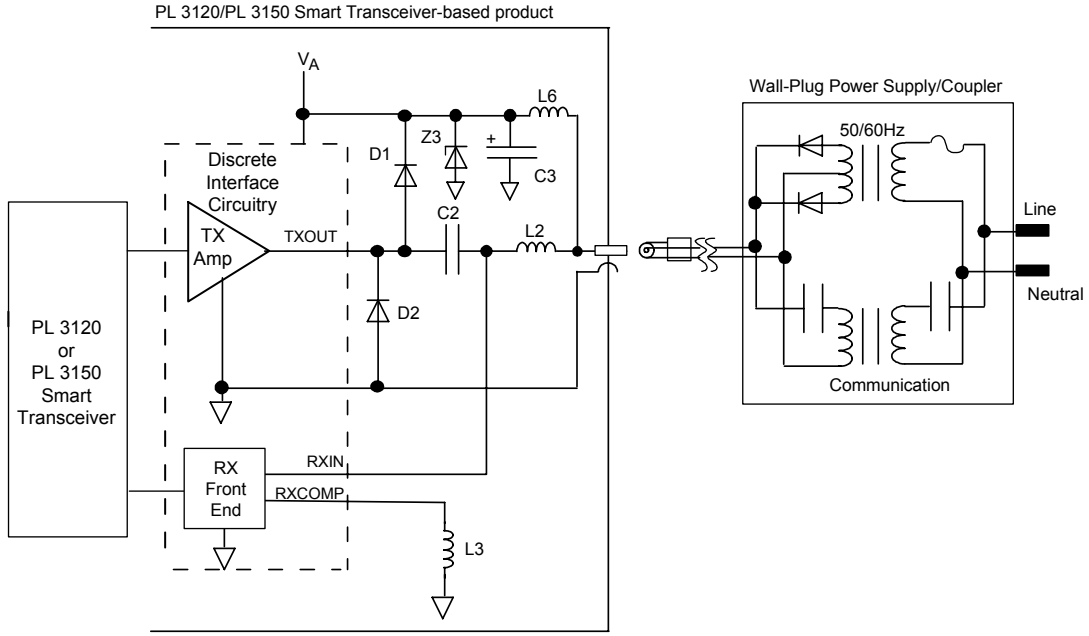


Figure 4.16 Wall-Plug Power Supply with Coupler

Recommended Coupling Circuit Schematics

This section provides schematics and component information for coupling the PL Smart Transceiver to the power mains. Note that these coupling circuits have been optimized for lower cost than the equivalent circuits in earlier versions of this data book. The user can either continue to use earlier versions or change to these new cost-optimized versions. The schematics are divided into classes based on coupling type, isolation and application. Table 4.1 provides a summary which can be used as a guide to determine the appropriate coupling circuit for a given application.

For each schematic, required component specifications and example suppliers/part numbers are provided. Vendor part number information is provided as a way to reduce component selection times, because the suggested parts have already been verified to meet all required specifications. Alternate component suppliers can be used provided that ***all*** of the required specifications listed for each component are met. While surge testing must be performed for every new product design, using the suggested vendor part numbers listed in the table for each of the examples has the additional advantage that they were the parts used for circuit verification by Echelon.

Table 4.1 Coupling Circuit Selection Guide

Example	Connection Type	Line Voltage	Isolated/ Non-Isolated	Freq. Band	Typical Application(s)	Page
1	1-Phase L-N	50-240VAC/ DC	Non-Isolated	A	Electric utility meters world-wide	126
				C	Consumer, residential devices world-wide, Commercial devices in CENELEC countries	
2	1-Phase L-N	50-240VAC/ DC	Isolated	A	Utility in-home devices world-wide	128
				C	Consumer residential devices world-wide, Commercial devices in CENELEC countries	
3	1-Phase L-E	100-277VAC	Non-Isolated	C	Commercial devices in North America	130
4	1-Phase L-E	100-277VAC	Isolated	C	Commercial devices in North America	132
5	3-Phase	100-277VAC	Non-Isolated	A	3-Phase utility devices world-wide	134
				C	Commercial panel devices world-wide	
6	3-Phase	100-277VAC	Isolated	A	3-Phase utility devices world-wide	136
				C	Commercial panel devices world-wide	
7	“2-Phase”	200-240VAC	Non-Isolated	A	2-Phase electric utility devices in North America and Japan	138
				C	2-Phase consumer devices in North America and Japan	
8	“2-Phase”	200-240VAC	Isolated	A	2-Phase utility devices in North America and Japan	140
				C	2-Phase consumer devices in North America and Japan	
9	Low-Volt AC	≤48Vpk	Non-Isolated	C	HVAC and irrigation devices world-wide	142
10	Low-Volt AC	≤48Vpk	Isolated	C	HVAC and irrigation devices world-wide	144
11	Low-Volt DC	≤48Vpk	Non-Isolated	C	Automotive wiring world-wide	146
12	1-Phase L-N Wall Plug	120VAC	Isolated	C	Consumer residential devices, North America	148
13	Long-Haul	≤240VAC/DC	Isolated	C	300m-20km dedicated lines world-wide	See *Note*
14	Current-loop	N/A	Isolated	C	Airport lighting devices world-wide	See *Note*

Note: Contact the Echelon LonSupport™ group for additional information.

Example 1. Line-to-Neutral, Non-Isolated Coupling Circuit

Figure 4.17 presents a schematic for a line-to-neutral (L-N), non-isolated mains coupling circuit. Table 4.2 lists component values and example suppliers/part numbers for coupling to the AC mains with a nominal line voltage in the range 100-240VAC. This schematic can also be used for coupling to wiring other than AC mains with AC or DC voltages of $250V_{RMS}$ or less.

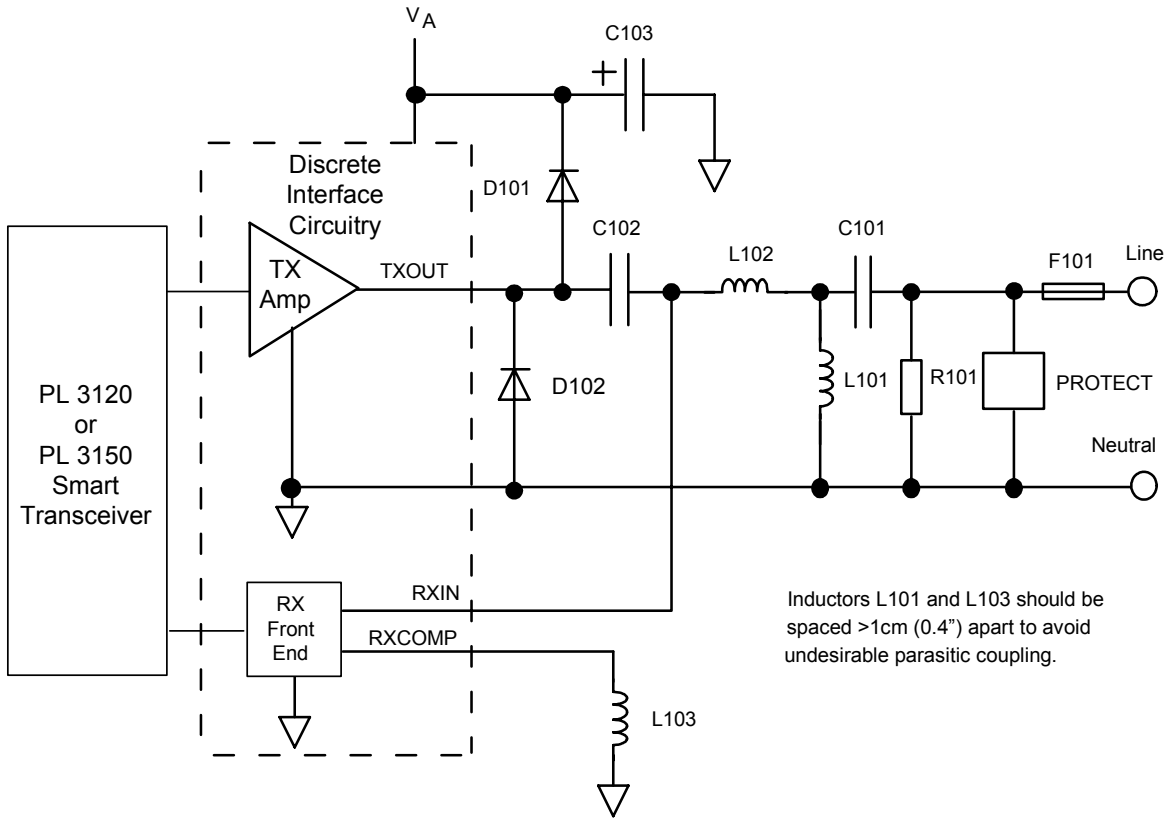


Figure 4.17 L-to-N, Non-Isolated Coupling Circuit Schematic

Table 4.2 100-240 VAC L-to-N, Non-Isolated Coupling Circuit Component Values

Comp	Value		Required Specifications	Example Vendor/Part#	
	A-band	C-band		A-band	C-band
C101	0.15µF	0.10µF	±10%, ≥250VAC, X2 type (1)	Panasonic/ ECQ-U2A154KL	Panasonic/ ECQ-U2A104KL
C102	1.0µF	1.0µF	±10%, ≥50VDC, metallized polyester	AVX/ BF074D0105K	AVX/ BF074D0105K
C103	≥120µF	≥120µF	±20%, ≥16VDC, aluminum electrolytic, ≤0.35Ω ESR @100kHz/20C, ≥290mA$_{RMS}$ ripple current @105C	Nichicon/ UHE1C121MED	Nichicon/ UHE1C121MED
D101	1A	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.3V @1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤200ns, reverse current ≤100µA @100C, typical capacitance ≤40pF @4V	Vishay General Semi/ 1N4935	Vishay General Semi/ 1N4935
D102	1A	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.0V @1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤25ns, reverse current ≤100µA @100C, typical capacitance ≤40pF @4V	Fairchild/ ES1B	Fairchild/ ES1B
F101	6A or 6.3A	6A or 6.3A	250VAC slow blow (1), (2)		
L101	1.0mH	1.0mH	±10%, Imax ≥30mA, R_{DC} ≤14Ω	Taiyo Yuden/ LAL04TB102K/ or CTC Coils Limited/ CH Series	Taiyo Yuden/ LAL04TB102K/ or CTC Coils Limited/ CH Series
L102	27µH	12µH	±10%, Imax ≥700mA, R_{DC} ≤0.3Ω	Taiyo Yuden/ LAL05TB270K/ or CTC Coils Limited/ CH Series	Taiyo Yuden/ LAL05TB120K/ or CTC Coils Limited/ CH Series
L103	1.5mH	820µH	±10%, Imax ≥30mA, R_{DC} ≤55Ω, 1kHz≤ Test Frequency ≤400kHz	RCD/ AL05 1500µH KT/ or CTC Coils Limited/ CH Series	ACT/ DD821K/ or CTC Coils Limited/ CH Series
R101	1MΩ	1MΩ	±5%, 1/4W, max working volt ≥360VDC (1), (3)		
PROTECT	300VAC (470VDC)	300VAC (470VDC)	For indoor branch circuits, ≥1250A surge current, 8x20µs, 2 times	AVX/ VE09P00301K	AVX/ VE09P00301K
	300VAC (470VDC)	300VAC (470VDC)	For power entry, ≥4500A surge current, 8x20µs, 2 times	AVX/ VE17P00301K	AVX/ VE17P00301K
	300VAC (470VDC)	300VAC (470VDC)	For outdoor use, ≥7000A surge current, 8x20µs, 2 times	AVX/ VE24P00301K	AVX/ VE24P00301K

NOTES:

1. For nominal line voltages of 120VAC or less, the voltage rating on these parts can be lowered to reduce cost and space.
2. In some applications, a fuse might not be required. Consult applicable safety standards.
3. The working voltage rating of R101 can be achieved by using two 470kΩ resistors in series, each with a working voltage rating of at least half of the value listed above.

Example 2. Line-to-Neutral, Transformer-Isolated Coupling Circuit

Figure 4.18 presents a schematic for a line-to-neutral (L-N), transformer-isolated coupling circuit. Table 4.3 lists component values and example suppliers/part numbers for coupling to AC mains with a nominal line voltage in the range 100-240VAC. This schematic can also be used for coupling to wiring other than AC mains with AC or DC voltages of $250V_{RMS}$ or less or for coupling to an un-powered wire pair.

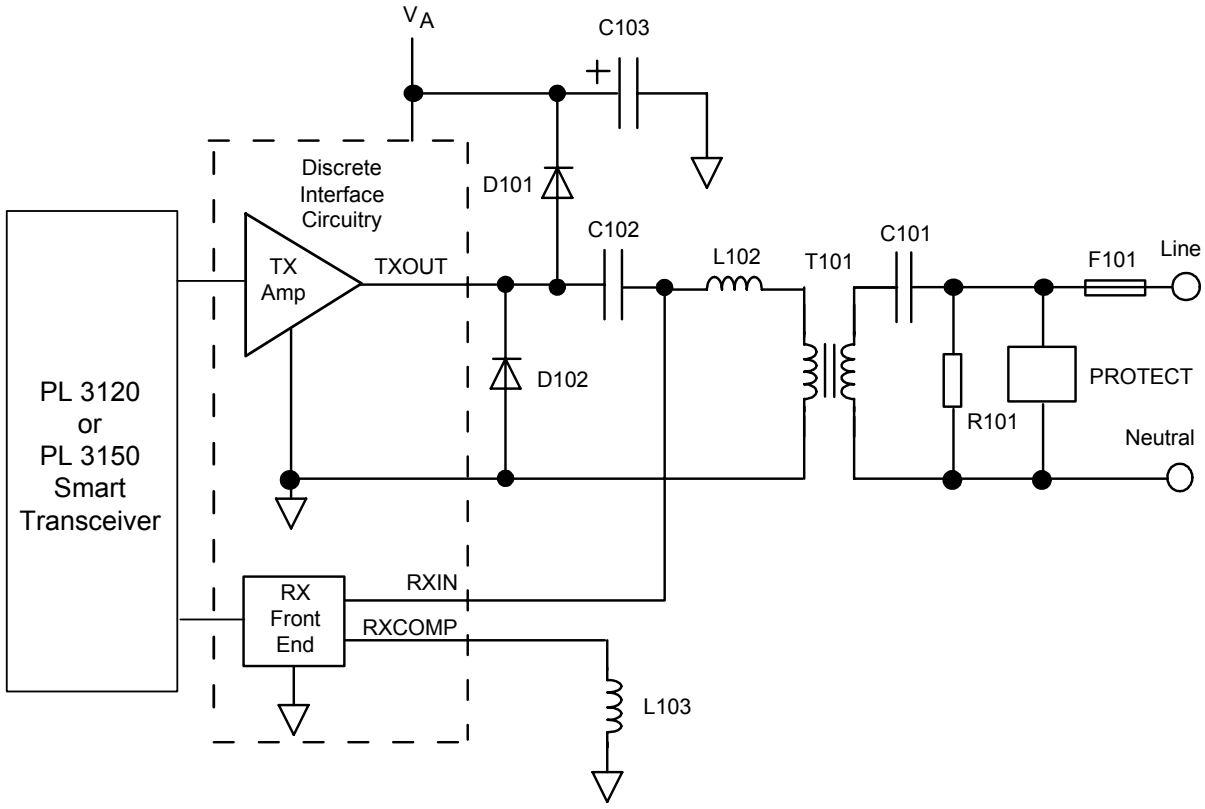


Figure 4.18 L-to-N, Transformer-Isolated Coupling Circuit Schematic

Table 4.3 100-240 VAC L-to-N Isolated Coupling Circuit Component Values

Comp	Value		Required Specifications	Example Vendor/Part#	
	A-band	C-band		A-band	C-band
C101	0.15µF	0.10µF	±10%, ≥250VAC, X2 type (1)	Panasonic/ ECQ-U2A154KL	Panasonic/ ECQ-U2A104KL
C102	1.0µF	1.0µF	±10%, ≥50VDC, metallized polyester	AVX/ BF074D0105K	AVX/ BF074D0105K
C103	≥120µF	≥120µF	±20%, ≥16VDC, aluminum electrolytic, ≤0.35Ω ESR @100kHz/20C, ≥290mA_{RMS} ripple current @105C	Nichicon/ UHE1C121MED	Nichicon/ UHE1C121MED
D101	1A	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.3V @1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤200ns, reverse current ≤100µA 100C, typical capacitance ≤40pF @4V	Vishay General Semi/ 1N4935	Vishay General Semi/ 1N4935
D102	1A	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.0V @1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤25ns, reverse current ≤100µA @100C, typical capacitance ≤40pF @4V	Fairchild/ ES1B	Fairchild/ ES1B
F101	6A or 6.3A	6A or 6.3A	250VAC slow blow (1), (2)		
L102	15µH	None	±10%, Imax ≥700mA, R_{DC} ≤0.3Ω	Taiyo Yuden/ LAL05TB150K/ or CTC Coils Limited/ CH Series	N/A
L103	1.5mH	820µH	±10%, Imax ≥30mA, R_{DC} ≤55Ω, 1kHz≤ Test Frequency ≤400kHz	RCD/ AL05 1500µH KT/ or CTC Coils Limited/ CH Series	ACT/ DD821K/ or CTC Coils Limited/ CH Series
R101	1MΩ	1MΩ	±5%, 1/4W, max working volt ≥360VDC (1), (3)		
PROTECT	300VAC (470VDC)	300VAC (470VDC)	For indoor branch circuits, ≥1250A surge current 8x20µs 2 times	AVX/ VE09P00301K	AVX/ VE09P00301K
	300VAC (470VDC)	300VAC (470VDC)	For power entry, ≥4500A surge current, 8x20µs, 2 times	AVX/ VE17P00301K	AVX/ VE17P00301K
	300VAC (470VDC)	300VAC (470VDC)	For outdoor use, ≥7000A surge current, 8x20µs, 2 times	AVX/ VE24P00301K	AVX/ VE24P00301K
T101	12µH-leakage trans-former		See Appendix C	See Appendix C	

NOTES:

1. For nominal line voltages of 120VAC or less, the voltage rating on these parts can be lowered to reduce cost and space.
2. In some applications, a fuse might not be required. Consult applicable safety standards.
3. The working voltage rating of R101 can be achieved by using two 470kΩ resistors in series, each with a working voltage rating of at least half of the value listed above.

Example 3. Line-to-Earth (L-to-E), Non-Isolated Coupling Circuit

Figure 4.19 presents a schematic for a line-to-earth, non-isolated mains coupling circuit. Table 4.4 lists component values and example suppliers/part numbers for coupling to the AC mains with a nominal line voltage in the range 100-277VAC.

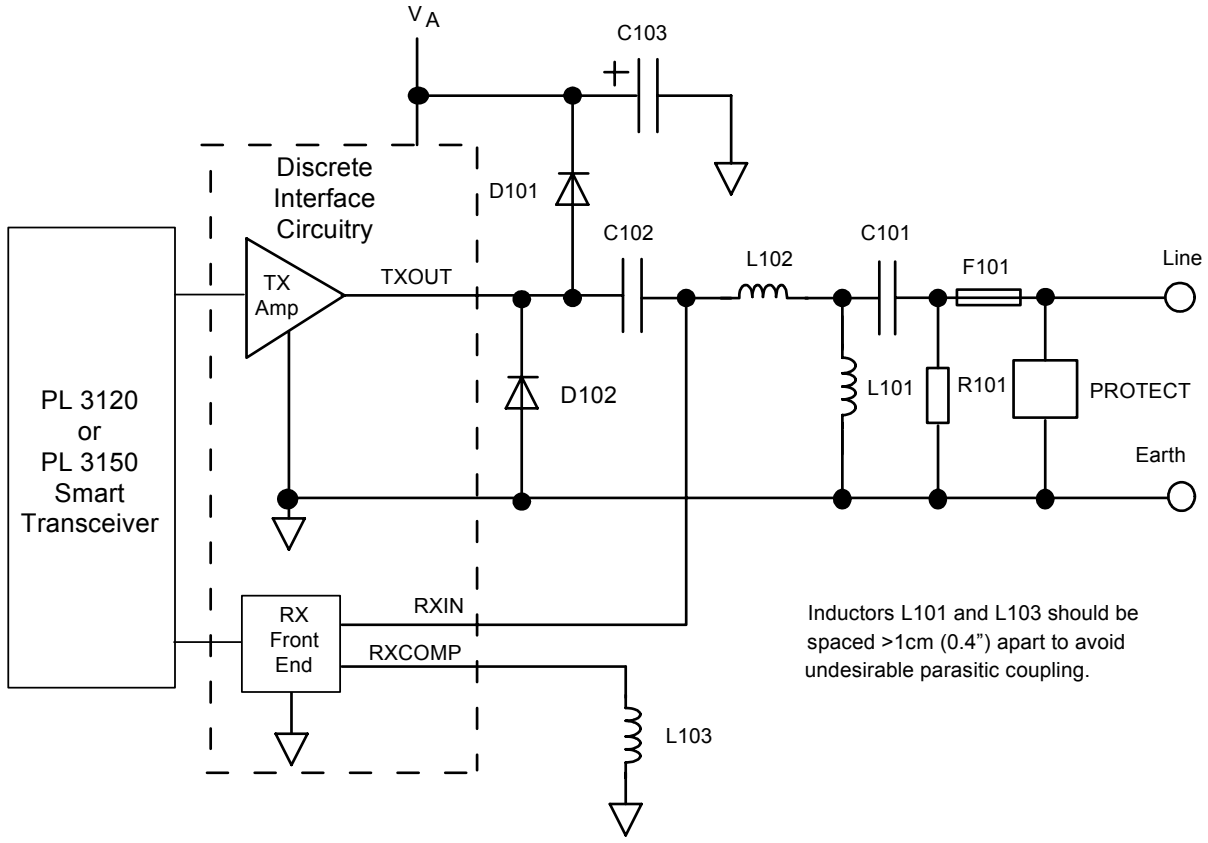


Figure 4.19 L-to-E, Non-Isolated Coupling Circuit Schematic

Table 4.4 100-277 VAC L-to-E Non-Isolated Coupling Circuit Component Values

Comp	Value		Required Specifications	Example Vendor/Part#	
	C-band 100-120VAC	C-band 200-277VAC		C-band 100-120VAC	C-band 200-277VAC
C101	0.068µF, ≥120VAC	0.033µF, ≥300VAC	±10%, X2 type (1)	Panasonic/ ECQ-U2A683KL	Evox-Rifa/ PHE840 EA 5330M A02
C102	1.0µF	1.0µF	±10%, ≥50VDC, metallized polyester	AVX/ BF074D0105K	AVX/ BF074D0105K
C103	≥120µF	≥120µF	±20%, ≥16VDC, aluminum electrolytic, ≤0.35Ω ESR @100kHz/20C, ≥290mA$_{RMS}$ ripple current @105C	Nichicon/ UHE1C121MED	Nichicon/ UHE1C121MED
D101	1A	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.3V @1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤200ns, reverse current ≤100µA @100C, typical capacitance ≤40pF @4V	Vishay General Semi/ 1N4935	Vishay General Semi/ 1N4935
D102	1A	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.0V@1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤25ns, reverse current ≤100µA @100C, typical capacitance ≤40pF @4V	Fairchild/ ES1B	Fairchild/ ES1B
F101	6A or 6.3A, ≥125VAC	6A or 6.3A, ≥300VAC	slow blow (2)		
L101	1.0mH	1.0mH	±10%, Imax ≥30mA, R_{DC} ≤14Ω	Taiyo Yuden/ LAL04TB102K/ or CTC Coils Limited/ CH Series	Taiyo Yuden/ LAL04TB102K/ or CTC Coils Limited/ CH Series
L102	18µH	39µH	±10%, Imax ≥500mA, R_{DC} ≤0.3Ω	Taiyo Yuden/ LAL05TB180K/ or CTC Coils Limited/ CH Series	Taiyo Yuden/ LAL05TB390K/ or CTC Coils Limited/ CH Series
L103	820µH	820µH	±10%, Imax ≥30mA, R_{DC} ≤55Ω, 1kHz≤ test frequency ≤400kHz	ACT/ DD821K/ or CTC Coils Limited/ CH Series	ACT/ DD821K/ or CTC Coils Limited/ CH Series
R101	1MΩ, ≥200VDC	1MΩ, ≥450VDC	±5%, 1/4W (3)		
PROTECT	N/A	N/A	For indoor branch circuits no component is required	N/A	N/A
	120VAC	300VAC	For power entry use AC gas discharge tube (4)	SRC Devices/ AC240L	
	120VAC	300VAC	For outdoor use AC gas discharge tube (4)	SRC Devices/ AC240L	

NOTES:
1. An X2 capacitor is required for adequate surge immunity in branch circuit applications.
2. In some applications, a fuse might not be required. Consult applicable safety standards.
3. The working voltage rating of R101 can be achieved by using two 470kΩ resistors in series, each with a working voltage rating of at least 1/2 of the value listed above. Also, peak power and voltage ratings of R101 must be chosen to meet the high-pot testing requirements of the application.
4. High-pot manufacturing tests must be performed prior to installation of this gas discharge tube. High-pot testing between line and earth is usually performed at voltages above the gas tube arc-over voltage, and the test will fail if the gas tube arcs during testing. In addition, a DC high-pot tester must be used to avoid excess current flow through C101.

Example 4. Line-to-Earth (L-E), Transformer-Isolated Coupling Circuit

Figure 4.20 presents a schematic for a line-to-earth, transformer-isolated coupling circuit. Table 4.5 lists component values and example suppliers/part numbers for coupling to AC mains with a nominal line voltage in the range 100-277VAC.

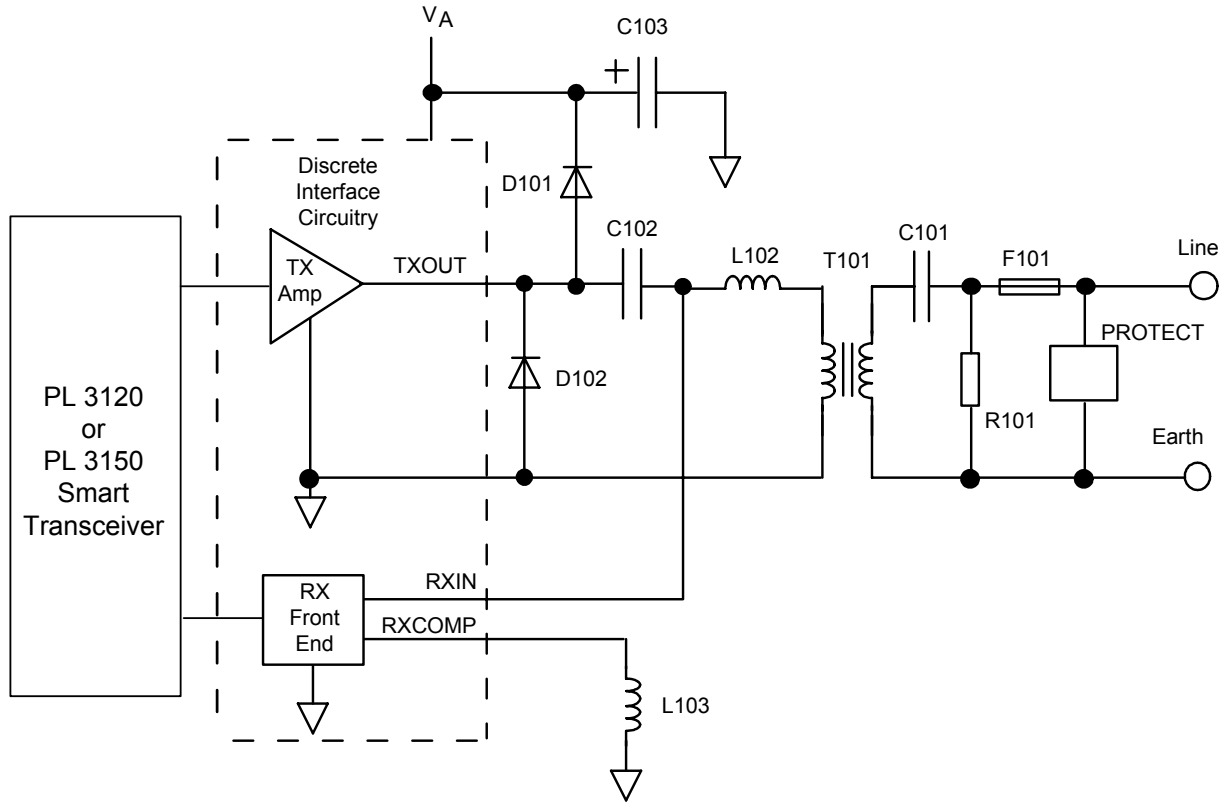


Figure 4.20 L-to-E, Transformer-Isolated Coupling Circuit Schematic

Table 4.5 100-277 VAC L-to-E Isolated Coupling Circuit Component Values

Comp	Value		Required Specifications	Example Vendor/Part#	
	C-band 100-120VAC	C-band 200-277VAC		C-band 100-120VAC	C-band 200-277VAC
C101	0.068µF, ≥120VAC	0.033µF, ≥300VAC	±10%, X2 type (1)	Panasonic/ ECQ-U2A683KL	Evox-Rifa/ PHE840 EA 5330M A02
C102	1.0µF	1.0µF	±10%, ≥50VDC, metallized polyester	AVX/ BF074D0105K	AVX/ BF074D0105K
C103	≥120µF	≥120µF	±20%, ≥16VDC, aluminum electrolytic, ≤0.35Ω ESR @100kHz/20C, ≥290mA$_{RMS}$ ripple current @105C	Nichicon/ UHE1C121MED	Nichicon/ UHE1C121MED
D101	1A	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.3V @1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤200ns, reverse current ≤100µA @100C, typical capacitance ≤40pF @4V	Vishay General Semi/ 1N4935	Vishay General Semi/ 1N4935
D102	1A	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.0V @1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤25ns, reverse current ≤100µA @100C, typical capacitance ≤40pF @4V	Fairchild/ ES1B	Fairchild/ ES1B
F101	6A or 6.3A, ≥125VAC	6A or 6.3A, ≥300VAC	slow blow (2)		
L102	5.6µH	27µH	±10%, Imax ≥500mA, R_{DC} ≤0.4Ω	Taiyo Yuden/ LAL04TB5R6K/ or CTC Coils Limited/ CH Series	Taiyo Yuden/ LAL05TB270K/ or CTC Coils Limited/ CH Series
L103	820µH	820µH	±10%, Imax ≥30mA, R_{DC} ≤55Ω, 1kHz≤ Test Frequency ≤400kHz	ACT/ DD821K/ or CTC Coils Limited/ CH Series	ACT/ DD821K/ or CTC Coils Limited/ CH Series
R101	1MΩ, ≥200VDC	1MΩ, ≥450VDC	±5%, 1/4W (3)		
PROTECT	N/A	N/A	For indoor branch circuits no component is required	N/A	N/A
	120VAC	300VAC	For power entry use AC gas discharge tube (4)	SRC Device/ AC240L	
	120VAC	300VAC	For outdoor use AC gas discharge tube (4)	SRC Device/ AC240L	
T101	12µH-leakage transformer		See Appendix C	See Appendix C	

NOTES:
1. An X2 capacitor is required for adequate surge immunity in branch circuit applications.
2. In some applications, a fuse might not be required. Consult applicable safety standards.
3. The working voltage rating of R101 can be achieved by using two 470kΩ resistors in series, each with a working voltage rating of at least 1/2 of the value listed above. Also peak power and voltage ratings of R101 must be chosen to meet the high-pot testing requirements of the application.
4. High-pot manufacturing tests must be performed prior to installation of this gas discharge tube. High-pot testing between line and earth is usually performed at voltages above the gas tube arc-over voltage, and the test will fail if the gas tube arcs during testing. In addition, a DC high-pot tester must be used to avoid excess current flow through C101.

Example 5. 3-Phase, Non-Isolated Coupling Circuit

Figure 4.21 presents a schematic for a non-isolated 3-phase coupling circuit. Table 4.6 lists component values and example suppliers/part numbers for coupling to AC mains with a nominal line voltage in the range 100-277VAC.

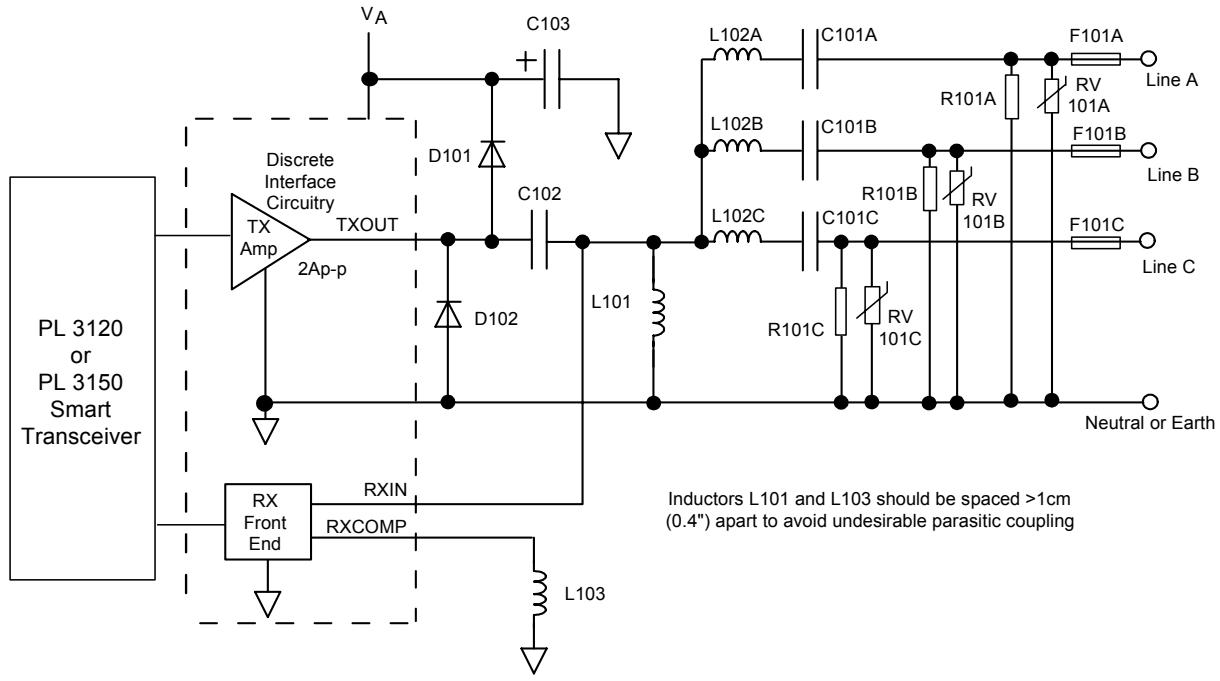


Figure 4.21 3-Phase Non-Isolated Coupling Circuit Schematic

Table 4.6 100-277 VAC, 3-Phase, Non-Isolated Coupling Circuit Component Values

Comp	Value		Required Specifications	Example Vendor/Part#	
	A-band	C-band		A-band	C-band
C101A-C	0.15µF	0.10µF	±10%, X2 type (1)	Panasonic/ ECQ-U2A154KL	Panasonic/ ECQ-U2A104KL
C102	1.0µF	1.0µF	±10%, ≥100VDC, metallized polyester	Panasonic/ ECQ-E1105KF	Panasonic/ ECQ-E1105KF
C103	≥220µF	≥220µF	±20%, ≥16VDC, aluminum electrolytic, ≤0.15Ω ESR @100kHz/20C, ≥550mA$_{RMS}$ ripple current @105C	Nichicon/ UHE1C331MPD	Nichicon/ UHE1C331MPD
D101, D102	1A	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.0V @1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤25ns, reverse current ≤100µA @100C, typical capacitance ≤40pF @4V.	Fairchild/ ES1B	Fairchild/ ES1B
F101A-C	6A or 6.3A	6A or 6.3A	250VAC slow blow (1), (2)		
L101	1.0mH	1.0mH	±10%, Imax ≥30mA, R_{DC} ≤14Ω	Taiyo Yuden/ LAL04TB102K/ or CTC Coils Limited/ CH Series	Taiyo Yuden/ LAL04TB102K/ or CTC Coils Limited/ CH Series
L102A-C	27µH	18µH	±10%, Imax ≥1.5A, R_{DC} ≤0.1Ω	Taiyo Yuden/ LHL08TB270K/ or CTC Coils Limited/ CH Series	Taiyo Yuden/ LHL08TB180K/ or CTC Coils Limited/ CH Series
L103	1.5mH	820µH	±10%, Imax ≥30mA, R_{DC} ≤55Ω, 1kHz≤ Test Frequency ≤400kHz	RCD/ AL05 1500µH KT/ or CTC Coils Limited/ CH Series	ACT/ DD821K/ or CTC Coils Limited/ CH Series
R101A-C	1MΩ	1MΩ	±5%, 1/4W, max working volt ≥360VDC (1), (3)		
RV101A-C	700VAC (1000 VDC)	700VAC (1000 VDC)	≥4500A surge current, 8x20µs, 2 times (1), (4)	Panasonic/ ERZ-V14D102	Panasonic/ ERZ-V14D102

NOTES:

1. For 277VAC nominal line voltage operation, the voltage rating of these components must be increased.
2. In some applications, fuses might not be required. Consult applicable safety standards.
3. The voltage rating of R101A-C can be achieved by using two 470kΩ resistors in series, each with a working voltage rating of at least half of the value listed above. For earth-return coupling, the peak power and peak voltage ratings of R101A-C must be chosen to meet high-pot testing requirements of the application.
4. The voltage rating indicated is necessary to prevent damage to the varistor should the neutral (or earth) connection be lost while all three phases are connected and live. For earth-return coupling, high-pot testing must be performed prior to installation of these varistors. High-pot testing between line and earth is usually performed at voltages above the varistor clamp voltage, and the test will fail if the varistors clamp during testing.

Example 6. 3-Phase, Transformer-Isolated Coupling Circuit

Figure 4.22 presents a schematic for a transformer-isolated 3-phase coupling circuit. Table 4.7 lists component values and example suppliers/part numbers for coupling to AC mains with a nominal line voltage in the range 100-277VAC.

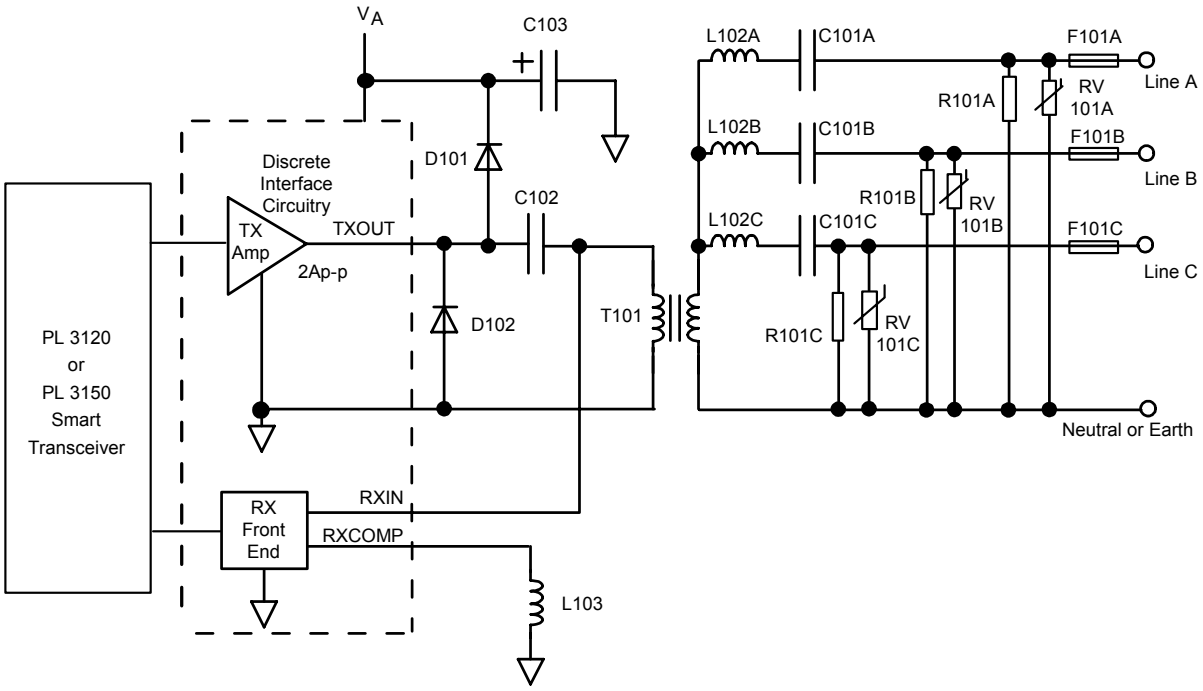


Figure 4.22 3-Phase Transformer-Isolated Coupling Circuit Schematic

Table 4.7 100-277 VAC, 3-Phase, Isolated Coupling Circuit Component Values

Comp	Value		Required Specifications	Example Vendor/Part#	
	A-band	C-band		A-band	C-band
C101A-C	0.15µF	0.10µF	±10%, X2 type (1)	Panasonic/ ECQ-U2A154KL	Panasonic/ ECQ-U2A104KL
C102	1.0µF	1.0µF	±10%, ≥100VDC, metallized polyester	Panasonic/ ECQ-E1105KF	Panasonic/ ECQ-E1105KF
C103	≥220µF	≥220µF	±20%, ≥16VDC, aluminum electrolytic, ≤0.15Ω ESR @100kHz/20C, ≥550mA$_{RMS}$ ripple current @105C	Nichicon/ UHE1C331MPD	Nichicon/ UHE1C331MPD
D101, D102	1A	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.0V @1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤25ns, reverse current ≤100µA @100C, typical capacitance ≤40pF @4V.	Fairchild/ ES1B	Fairchild/ ES1B
F101A-C	6A or 6.3A	6A or 6.3A	250VAC slow blow (1), (2)		
L102A-C	27µH	18µH	±10%, Imax ≥1.5A, R_{DC} ≤0.1Ω	Taiyo Yuden/ LHL08TB270K/ or CTC Coils Limited/ CH Series	Taiyo Yuden/ LHL08TB180K/ or CTC Coils Limited/ CH Series
L103	1.5mH	820µH	±10%, Imax ≥30mA, R_{DC} ≤55Ω, 1kHz≤ Test Frequency ≤400kHz	RCD/ AL05 1500µH KT/ or CTC Coils Limited/ CH Series	ACT/ DD821K/ or CTC Coils Limited/ CH Series
R101A-C	1MΩ	1MΩ	±5%, 1/4W, max working volt ≥360VDC (1), (3)		
RV101A-C	700VAC (1000VDC)	700VAC (1000VDC)	≥4500A surge current, 8x20µs, 2 times (1), (4)	Panasonic/ ERZ-V14D102	Panasonic/ ERZ-V14D102
T101	Low-leakage transformer		See Appendix C	See Appendix C	

NOTES:

1. For 277VAC nominal line voltage operation, the voltage rating of these components must be increased.
2. In some applications, fuses might not be required. Consult applicable safety standards.
3. The working voltage rating of R101A-C can be achieved by using two 470kΩ resistors in series, each with a working voltage rating of at least half of the value listed above. For earth return coupling, the peak power and peak voltage ratings of R101A-C must be chosen to meet high-pot testing requirements of the application.
4. The voltage rating indicated is necessary to prevent damage to the varistor should the neutral (or earth) connection be lost while all three phases are connected and live. For earth-return coupling, high-pot testing must be performed prior to installation of these varistors. High-pot testing between line and earth is usually performed at voltages above the varistor clamp voltage, and the test will fail if the varistors clamp during testing.

Example 7. 2-Phase, Non-Isolated Coupling Circuit

Figure 4.23 presents a schematic for a non-isolated 2-phase coupling circuit. Table 4.8 lists component values and example suppliers/part numbers for coupling to AC mains with a nominal line voltage in the range 100-240VAC.

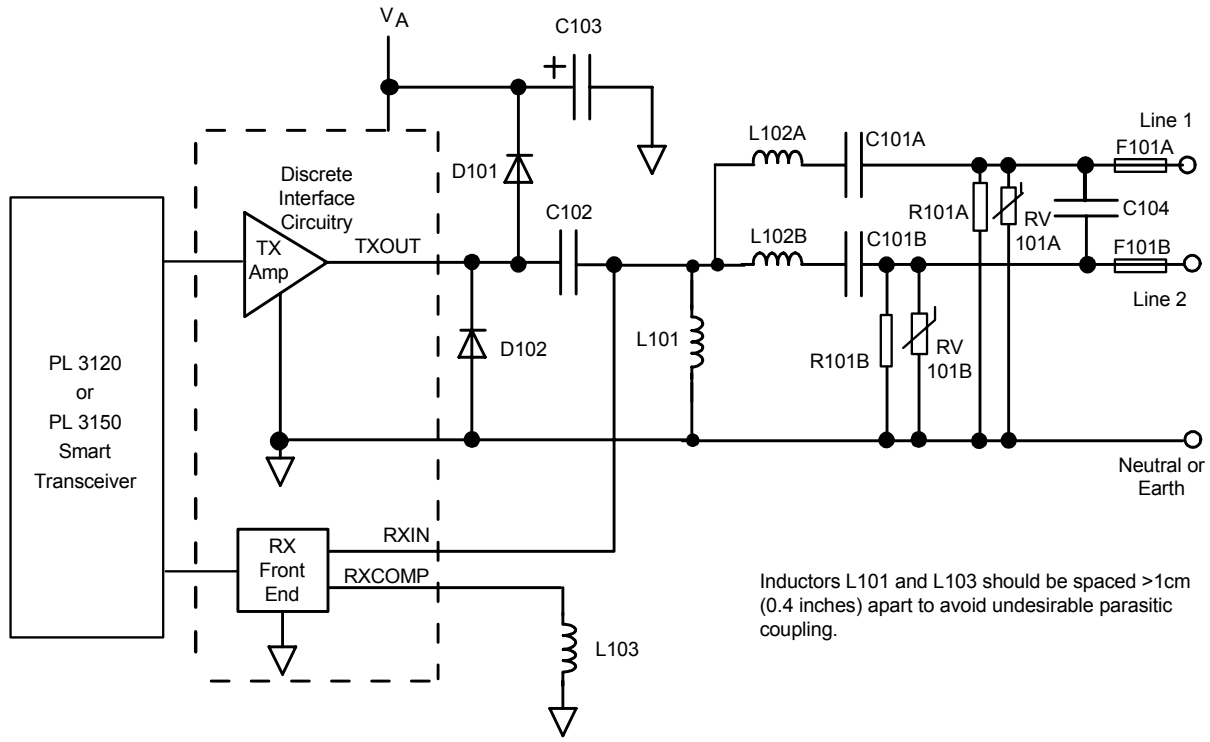


Figure 4.23 2-Phase Non-Isolated Coupling Circuit Schematic

Table 4.8 100-240 VAC, 2-Phase, Non-Isolated Coupling Circuit Component Values

Comp	Value		Required Specifications	Example Vendor/Part#	
	A-band	C-band		A-band	C-band
C101A-B	0.15µF	0.10µF	±10%, ≥250VAC, X2 type	Panasonic/ ECQ-U2A154KL	Panasonic/ ECQ-U2A104KL
C102	1.0µF	1.0µF	±10%, ≥100VDC, metallized polyester	Panasonic/ ECQ-E1105KF	Panasonic/ ECQ-E1105KF
C103	≥120µF	≥120µF	±20%, ≥16VDC, aluminum electrolytic, ≤0.35Ω ESR @100kHz/20C, ≥290mA$_{RMS}$ ripple current @105C	Nichicon/ UHE1C121MED	Nichicon/ UHE1C121MED
C104	0.47µF	0.47µF	±20%, ≥250VAC, X2 type	Panasonic/ ECQ-U2A474ML	Panasonic/ ECQ-U2A474ML
D101	1A	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.3V @1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤200ns, reverse current ≤100µA @100C, typical capacitance ≤40pF @4V	Vishay General Semi/ 1N4935	Vishay General Semi/ 1N4935
D102	1A	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.0V@1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤25ns, reverse current ≤100µA @100C, typical capacitance ≤40pF @4V	Fairchild/ ES1B	Fairchild/ ES1B
F101A-B	6A or 6.3A	6A or 6.3A	250VAC slow blow(1)		
L101	1.0mH	1.0mH	±10%, Imax ≥30mA, R_{DC} ≤14Ω	Taiyo Yuden/ LAL04TB102K/ or CTC Coils Limited/ CH Series	Taiyo Yuden/ LAL04TB102K/ or CTC Coils Limited/ CH Series
L102A-B	27µH	18µH	±10%, Imax ≥700mA, R_{DC} ≤0.1Ω	Taiyo Yuden/ LHL08TB270K/ or CTC Coils Limited/ CH Series	Taiyo Yuden/ LHL08TB180K/ or CTC Coils Limited/ CH Series
L103	1.5mH	820µH	±10%, Imax ≥30mA, R_{DC} ≤55Ω, 1kHz≤ Test Frequency ≤400kHz	RCD/ AL05 1500µH KT/ or CTC Coils Limited/ CH Series	ACT/ DD821K/ or CTC Coils Limited/ CH Series
R101A-B	1MΩ	1MΩ	±5%, 1/4W, max working volt ≥360VDC (2)		
RV101A-B	300VAC (470 VDC)	300VAC (470 VDC)	≥4500A surge current, 8x20µs, 2 times (3)	AVX/ VE17P00301K	AVX/ VE17P00301K

NOTES:

1. In some applications, fuses might not be required. Consult applicable safety standards.
2. The voltage rating of R101A-B can be achieved by using two 470kΩ resistors in series, each with a working voltage rating of at least half of the value listed above. For earth return coupling, the peak power and peak voltage ratings of R101A-B must be chosen to meet high-pot testing requirements of the application.
3. For earth-return coupling, high-pot testing must be performed prior to installation of these varistors. High-pot testing between line and earth is usually performed at voltages above the varistor clamp voltage, and the test will fail if the varistors clamp during testing.

Example 8. 2-Phase, Transformer-Isolated Coupling Circuit

Figure 4.24 presents a schematic for a transformer-isolated 2-phase coupling circuit. Table 4.9 lists component values and example suppliers/part numbers for coupling to AC mains with a nominal line voltage in the range 100-240VAC.

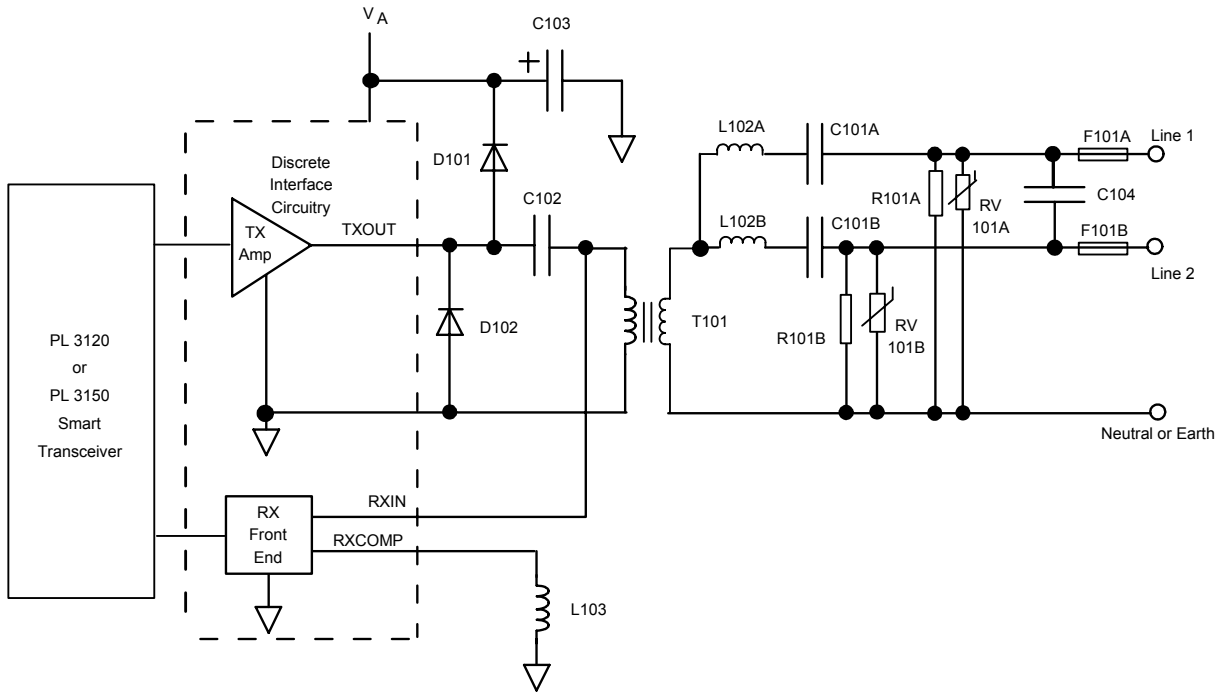


Figure 4.24 2-Phase Transformer-Isolated Coupling Circuit Schematic

Table 4.9 100-240 VAC, 2-Phase, Isolated Coupling Circuit Component Values

Comp	Value		Required Specifications	Example Vendor/Part#	
	A-band	C-band		A-band	C-band
C101A-B	0.15µF	0.10µF	±10%, ≥250VAC, X2 type	Panasonic/ ECQ-U2A154KL	Panasonic/ ECQ-U2A104KL
C102	1.0µF	1.0µF	±10%, ≥100VDC, metallized polyester	Panasonic/ ECQ-E1105KF	Panasonic/ ECQ-E1105KF
C103	≥120µF	≥120µF	±20%, ≥16VDC, aluminum electrolytic, ≤0.35Ω ESR @100kHz/20C, ≥290mA$_{RMS}$ ripple current @ 105C	Nichicon/ UHE1C121MED	Nichicon/ UHE1C121MED
C104	0.47µF	0.47µF	±20%, ≥250VAC, X2 type	Panasonic/ ECQ-U2A474ML	Panasonic/ ECQ-U2A474ML
D101	1A	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.3V @1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤200ns, reverse current ≤100µA @100C, typical capacitance ≤40pF @4V	Vishay General Semi/ 1N4935	Vishay General Semi/ 1N4935
D102	1A	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.0V @1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤25ns, reverse current ≤100µA @100C, typical capacitance ≤40pF @4V.	Fairchild/ ES1B	Fairchild/ ES1B
F101A-B	6A or 6.3A	6A or 6.3A	250VAC slow blow(1)		
L102A-B	27µH	18µH	±10%, Imax ≥700mA, R_{DC} ≤0.1Ω	Taiyo Yuden/ LHL08TB270K/ or CTC Coils Limited/ CH Series	Taiyo Yuden/ LHL08TB180K/ or CTC Coils Limited/ CH Series
L103	1.5mH	820µH	±10%, Imax ≥30mA, R_{DC} ≤55Ω, 1kHz≤ Test Frequency ≤400kHz	RCD/ AL05 1500µH KT/ or CTC Coils Limited/ CH Series	ACT/ DD821K/ or CTC Coils Limited/ CH Series
R101A-B	1MΩ	1MΩ	±5%, 1/4W, max working volt ≥360VDC (2)		
RV101A-B	300VAC (470 VDC)	300VA (470 VDC)	≥4500A surge current, 8x20µs, 2 times (3)	AVX/ VE17P00301K	AVX/ VE17P00301K
T101	Low-leakage transformer		See Appendix C	See Appendix C	

NOTES:

1. In some applications, fuses might not be required. Consult applicable safety standards.
2. The voltage rating of R101A-B can be achieved by using two 470kΩ resistors in series, each with a working voltage rating of at least half of the value listed above. For earth return coupling, the peak power and peak voltage ratings of R101A-B must be chosen to meet high-pot testing requirements of the application.
3. For earth-return coupling, high-pot testing must be performed prior to installation of these varistors. High-pot testing between line and earth is usually performed at voltages above the varistor clamp voltage, and the test will fail if the varistors clamp during testing.

Example 9. Low-Voltage AC, Non-Isolated Coupling Circuit

Figure 4.25 presents a schematic for a low-voltage AC, non-isolated mains coupling circuit. Table 4.10 lists component values and example suppliers/part numbers for coupling to AC circuits with voltages of ≤48Vpk.

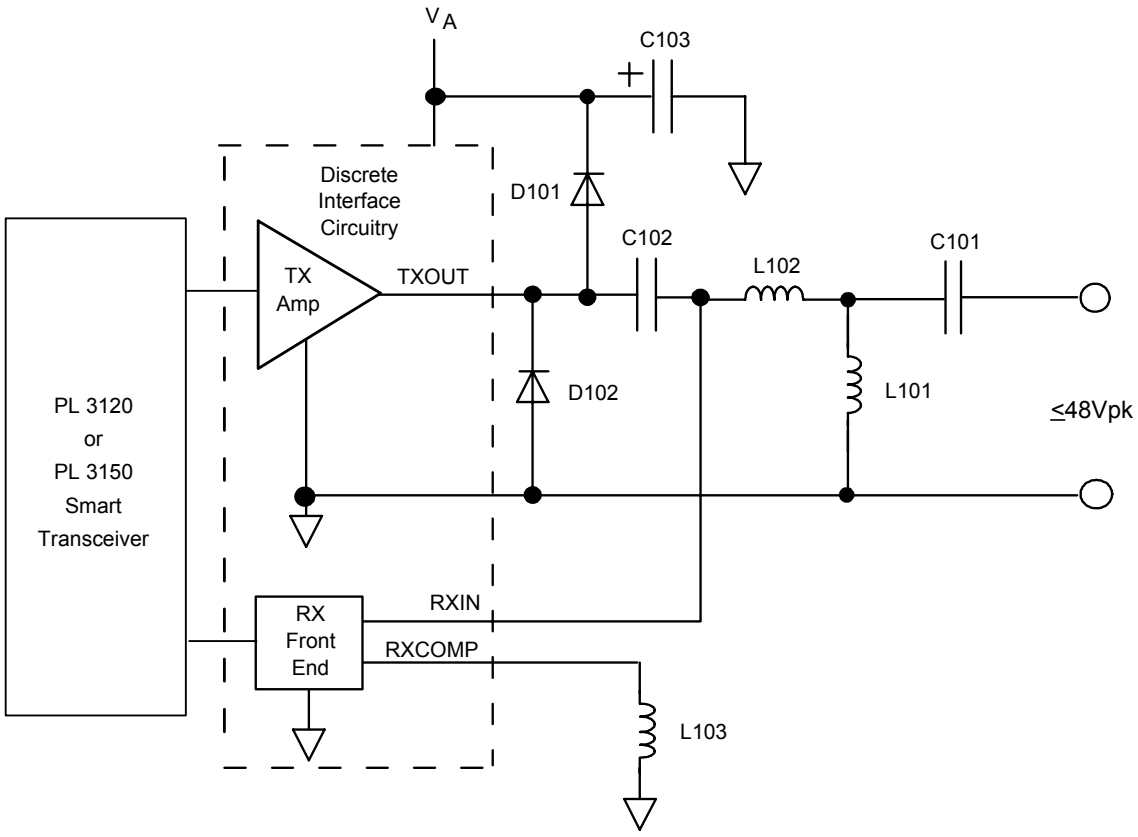


Figure 4.25 Low-Voltage AC, Non-Isolated Coupling Circuit Schematic

Table 4.10 Low-Voltage AC, Non-Isolated Coupling Circuit Component Values

Comp	Value		Required Specifications	Example Vendor/Part#	
	A-band	C-band		A-band	C-band
C101	0.47µF	0.47µF	±10%, ≥50VAC, metallized polyester	AVX/ BF074D0474K	AVX/ BF074D0474K
C102	1.0µF	1.0µF	±10%, ≥50VDC, metallized polyester	AVX/ BF074D0105K	AVX/ BF074D0105K
C103	≥120µF	≥120µF	±20%, ≥16VDC, aluminum electrolytic, ≤0.35Ω ESR @100kHz/20C, ≥290mA$_{RMS}$ ripple current @105C	Nichicon/ UHE1C121MED	Nichicon/ UHE1C121MED
D101	1A	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.3V @1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤200ns, reverse current ≤100µA @100C, typical capacitance ≤40pF @4V.	Vishay General Semi/ 1N4935	Vishay General Semi/ 1N4935
D102	1A	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.0V @1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤25ns, reverse current ≤100µA @100C, typical capacitance ≤40pF @4V.	Fairchild/ ES1B	Fairchild/ ES1B
L101	1.0mH	1.0mH	±10%, Imax ≥30mA, R_{DC} ≤14Ω	Taiyo Yuden/ LAL04TB102K/ or CTC Coils Limited/ CH Series	Taiyo Yuden/ LAL04TB102K/ or CTC Coils Limited/ CH Series
L102	Bead	Bead	≤0.5Ω @100kHz, ≥20Ω @10MHz, Imax ≥2A	Steward/ HI1206P121R-00	Steward/ HI1206P121R-00
L103	1.5mH	820µH	±10%, Imax ≥30mA, R_{DC} ≤55Ω, 1kHz≤ Test Frequency ≤400kHz	RCD/ AL05 1500µH KT/ or CTC Coils Limited/ CH Series	ACT/ DD821K/ or CTC Coils Limited/ CH Series

Example 10. Low-Voltage AC, Transformer-Isolated Coupling Circuit

Figure 4.26 presents a schematic for a low-voltage AC, transformer-isolated coupling circuit. Table 4.11 lists component values and example suppliers/part numbers for coupling to AC circuits with voltages of ≤48Vpk.

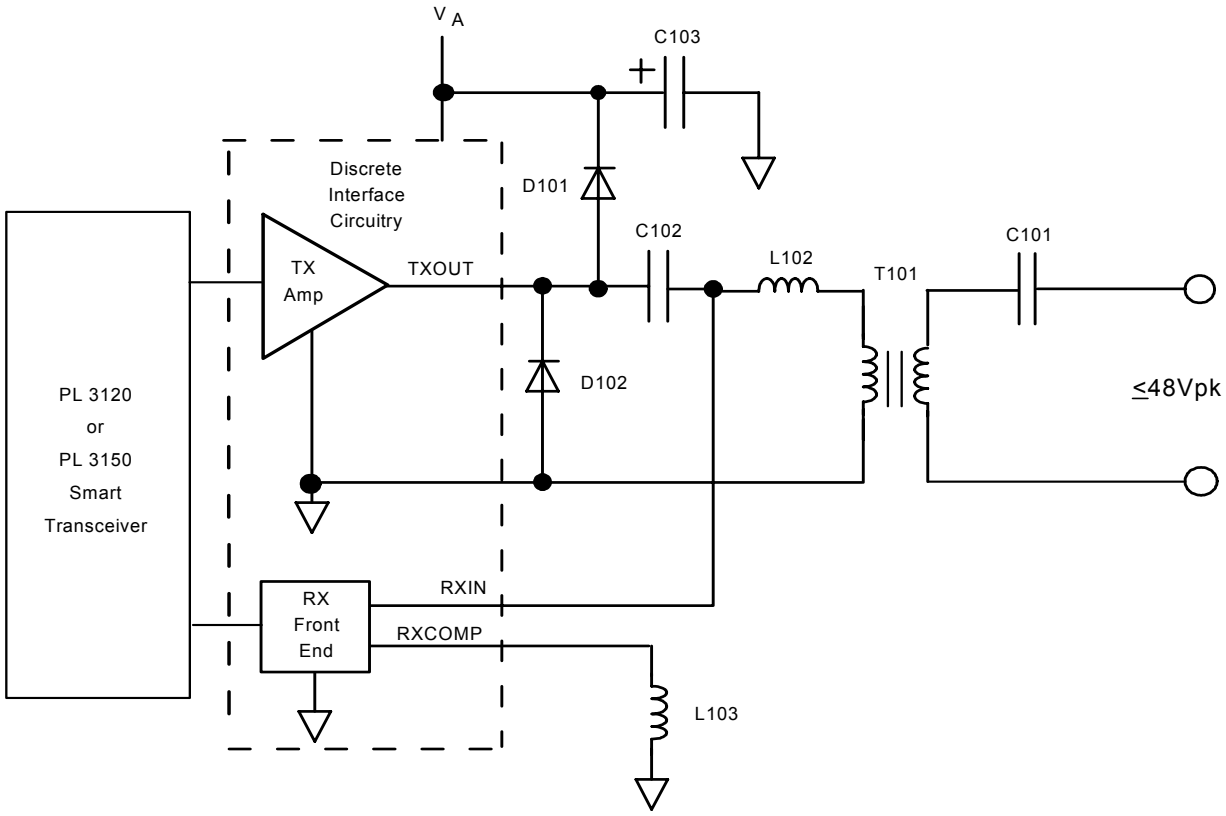


Figure 4.26 Low-Voltage AC, Transformer-Isolated Coupling Circuit Schematic

Table 4.11 Low-Voltage AC Isolated Coupling Circuit Component Values

Comp	Value		Required Specifications	Example Vendor/Part#	
	A-band	C-band		A-band	C-band
C101	0.47µF	0.47µF	±10%, ≥50VDC, metallized polyester	AVX/ BF074D0474KL	AVX/ BF074D0474KL
C102	1.0µF	1.0µF	±10%, ≥50VDC, metallized polyester	AVX/ BF074D0105K	AVX/ BF074D0105K
C103	≥120µF	≥120µF	±20%, ≥16VDC, aluminum electrolytic, ≤0.35Ω ESR @100kHz/20C, ≥290mA$_{RMS}$ ripple current @105C	Nichicon/ UHE1C121MED	Nichicon/ UHE1C121MED
D101	1A	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.3V@1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤200ns, reverse current ≤100µA 100C, typical capacitance ≤40pF@4V	Vishay General Semi/ 1N4935	Vishay General Semi/ 1N4935
D102	1A	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.0V @1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤25ns, reverse current ≤100µA @100C, typical capacitance ≤40pF @4V	Fairchild/ ES1B	Fairchild/ ES1B
L102	Bead	Bead	≤0.5Ω @100kHz, ≥20Ω @10MHz, Imax ≥2A	Steward/ HI1206P121R-00	Steward/ HI1206P121R-00
L103	1.5mH	820µH	±10%, Imax ≥30mA, R_{DC} ≤55Ω, 1kHz≤ Test Frequency ≤400kHz	RCD/ AL05 1500µH KT/ or CTC Coils Limited/ CH Series	ACT/ DD821K/ or CTC Coils Limited/ CH Series
T101	Low-leakage transformer		See Appendix C	See Appendix C	

Example 11. Low-Voltage DC, Non-Isolated Coupling Circuit

Figure 4.27 presents a schematic for a low-voltage DC, non-isolated mains coupling circuit. Table 4.12 lists component values and example suppliers/part numbers for coupling to DC circuits with voltages of ≤48Vpk.

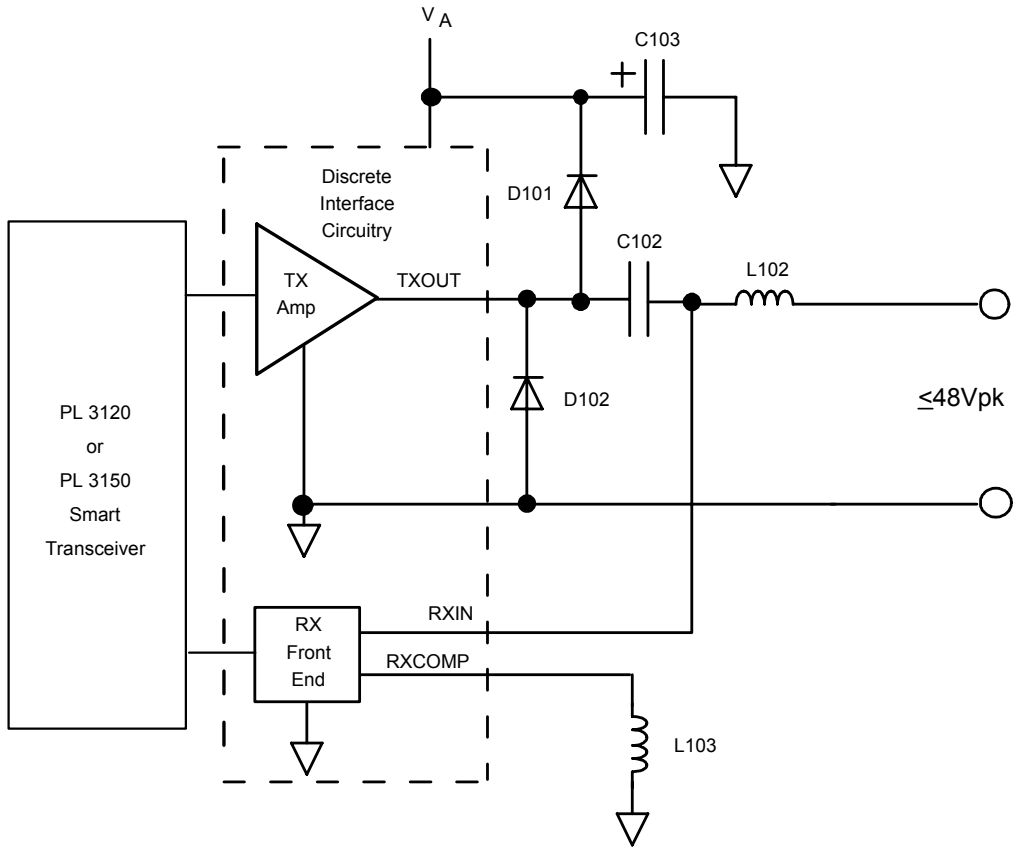


Figure 4.27 Low-Voltage DC, Non-Isolated Coupling Circuit Schematic

Table 4.12 Low-Voltage DC, Non-Isolated Coupling Circuit Component Values

Comp	Value		Required Specifications	Example Vendor/Part#	
	A-band	C-band		A-band	C-band
C102	1.0µF	1.0µF	±10%, ≥50VDC, metallized polyester	AVX/ BF074D0105K	AVX/ BF074D0105K
C103	≥120µF	≥120µF	±20%, ≥16VDC, aluminum electrolytic, ≤0.35Ω ESR @100kHz/20C, ≥290mA$_{RMS}$ ripple current @105C	Nichicon/ UHE1C121MED	Nichicon/ UHE1C121MED
D101	1A	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.3V @1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤200ns, reverse current ≤100µA @100C, typical capacitance ≤40pF @4V	Vishay General Semi/ 1N4935	Vishay General Semi/ 1N4935
D102	1A	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.0V @1A 25C, surge current ≥30A for 8.3ms, reverse recovery ≤25ns, reverse current ≤100µA @100C, typical capacitance ≤40pF @4V	Fairchild/ ES1B	Fairchild/ ES1B
L102	Bead	Bead	≤0.5Ω @100kHz, ≥20Ω @10MHz, Imax ≥2A	Steward/ HI1206P121R-00	Steward/ HI1206P121R-00
L103	1.5mH	820µH	±10%, Imax ≥30mA, R_{DC} ≤55Ω, 1kHz≤ Test Frequency ≤400kHz	RCD/ AL05 1500µH KT/ or CTC Coils Limited/ CH Series	ACT/ DD821K/ or CTC Coils Limited/ CH Series

Example 12. Line-to-Neutral (L-to-N), Isolated Wall-Plug Power Supply/ Coupler

Figure 4.28 presents a schematic for using a communication coupler combined with a wall-plug power supply. Both 120VAC/60Hz and 230VAC/50Hz versions of the Wall-Plug Power Supply/Coupler shown in the figure are available from Tamura Corporation. These Wall-Plug Power Supply/Couplers incorporate line-to-neutral coupling. With nominal AC line voltage, the power supply portion of the circuit provides a V_A supply voltage of 10.8V to 17V with load currents from 0 to 360mADC. With worst case AC line voltage tolerance of ±10% the V_A supply is 8.5V to 18V with an output current of up to 360mADC. Table 4.13 lists component values and recommended suppliers/part numbers for this design.

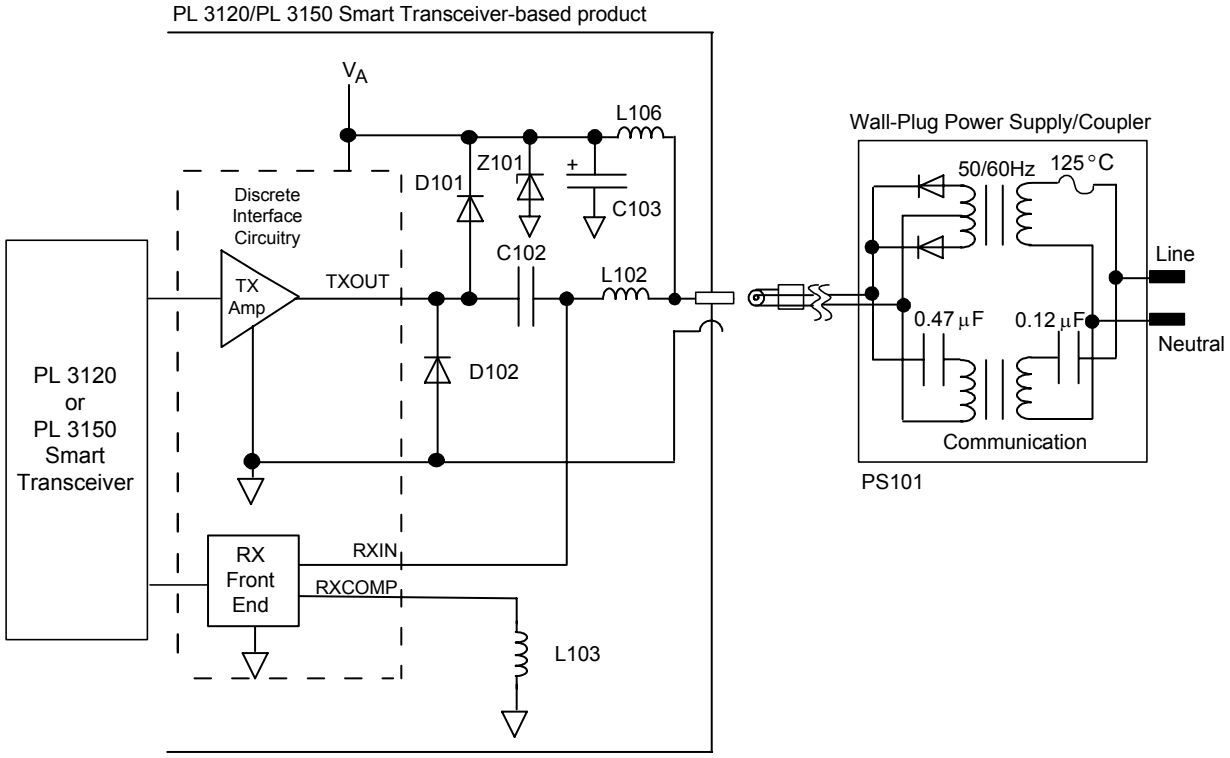


Figure 4.28 L-to-N Isolated Wall-Plug Power Supply/Coupler Schematic

Table 4.13 120, 230 VAC L-to-N, Wall-Plug Coupling Circuit Component Values

Comp	Value	Required Specifications	Example Vendor/Part#
	C-band		C-band
C102	1.0µF	±10%, ≥50VDC, metallized polyester	AVX/ BF074D0105K
C103	≥820µF	±20%, ≥25VDC, aluminum electrolytic, ≤0.3Ω ESR @100kHz	Nichicon/ UHE1E821MPD
D101	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.3V @1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤200ns, reverse current ≤100µA @100C, typical capacitance ≤40pF @4V	Vishay General Semi/ 1N4935
D102	1A	Reverse breakdown ≥50VDC, forward voltage ≤1.0V @1A/25C, surge current ≥30A for 8.3ms, reverse recovery ≤25ns, reverse current ≤100µA @100C, typical capacitance ≤40pF @4V	Fairchild/ ES1B
Z101	17V	±5%, 5W, Zener	IN5354B
L102	Bead	≤0.5Ω @100kHz, ≥20Ω @10MHz, Imax ≥2A	Steward/ HI1206P121R-00
L103	820µH	±10%, Imax ≥30mA, R_{DC} ≤55Ω, 1kHz≤ test frequency ≤400kHz	ACT/ DD821K/ or CTC Coils Limited/ CH Series
L106	220µH	±10%, Imax ≥500mA, R_{DC} ≤1.0Ω	Taiyo Yuden/ LHL08TB221K/ or CTC Coils Limited/ CH Series
PS101	120VAC	120VAC±10%, 60Hz, 12VDC, 400mA	Tamura (1)/ 425A12400P
	230VAC	230VAC±10%, 50Hz, 12VDC, 400mA	Tamura (1)/ 425F12400P

NOTES:

1. Tamura Corporation Industrial Device B.U.
   Telephone: +81-492-84-5721 (Japan)
   +1-800-472-6624 (USA)
   Fax: +81-492-84-9106
   www.tamuracorp.com

Surge Immunity of Example Circuits

The recommendations for the surge protection components that are included in the example circuits documented in this chapter are based on testing performed on a particular PCB layout. The efficacy of the surge protection implemented in each product containing the PL Smart Transceiver must always be verified empirically using the final product design because factors such as PCB layout and packaging can influence the results as much as the choice of protection components.

Table 4.14 lists the surge levels that the coupling circuits in this chapter can withstand without any damage to the coupling circuit, the PL Smart Transceiver chip, or the PL Smart Transceiver interface circuitry. This criterion of "no damage" is the one most commonly applied for surge testing. A simple and practical way to determine if a device has been damaged after surge testing is to use the production test method described in Appendix D of this data book. Each of the AC mains coupling circuits documented in this chapter was subjected to a sequence of surge events followed by an Appendix D production test to verify that neither the coupling circuit, the Smart Transceiver chip nor the associated discrete interface circuitry were damaged. The surge waveform type and levels used to test each circuit are listed in Table 4.14 along with the corresponding IEEE C62.41-1991 system exposure rating.

The surge test for each circuit consisted of a minimum of 4 Ring wave and 4 Combination wave surge events. Each group of 4 events were then split into groups of 2 events at 90° with negative polarity (phase measured relative to the AC mains zero-cross rising edge) and 2 events at 270° with positive polarity. These phase and polarity settings were previously determined to provide the greatest level of stress to the most sensitive circuit components. Multi-phase coupling circuits were tested both with a single phase connected to the surge generator and then again with all phases connected to the generator in parallel.

If the surge requirements for the product under test are different from those listed below, then it is up to the developer to perform testing in accordance with their particular requirements. As mentioned above, the efficacy of any surge protection plan must always be verified using samples of the final product because the results can vary with circuit layouts.

Table 4.14 Surge Levels of the Example Coupling Circuits

Example	Coupling Type	Location Type	Ring Wave (0.5µs-100kHz)		Combination Wave (1.2/50µs-8/20µs)	
			Surge Level Tested	**IEEE C62.41 Exposure Level**	**Surge Level Tested**	**IEEE C62.41 Exposure Level**
1	1-phase, L-N, non-isolated	branch circuit	6kV/200A	high	6kV/500A	no spec
		power entry	6kV/500A	high	6kV/3000A	high
		outdoor	6kV/500A	low (see *Note*)	6kV/3000A	low (see *Note*)
2	1-phase, L-N, isolated	branch circuit	6kV/200A	high	6kV/500A	no spec
		power entry	6kV/500A	high	6kV/3000A	high
		outdoor	6kV/500A	low (see *Note*)	6kV/3000A	low (see *Note*)
3	1-phase, L-E, non-isolated	branch circuit	4kV/130A	medium	3kV/250A	no spec
		power entry	6kV/500A	high	6kV/3000A	high
		outdoor	6kV/500A	no spec	6kV/3000A	low (see *Note*)
4	1-phase, L-E, isolated	branch circuit	4kV/130A	medium	3kV/250A	no spec
		power entry	6kV/500A	high	6kV/3000A	high
		outdoor	6kV/500A	no spec	6kV/3000A	low (see *Note*)
5	3-phase, non-isolated	power entry	6kV/500A	high	6kV/3000A	high
6	3-phase, isolated	power entry	6kV/500A	high	6kV/3000A	high
7	2-phase, non-isolated	power entry	6kV/500A	high	6kV/3000A	high
8	2-phase, isolated	power entry	6kV/500A	high	6kV/3000A	high
12	wall-plug, L-N, isolated	branch circuit	4kV/130A	medium	3kV/250A	no spec

Note: The surge level tested for this entry is the maximum level that is supported by available test equipment. Testing outdoor products to the IEEE medium exposure level requires a surge generator that supports 10kV/5000A (20kV/10,000A for outdoor high system exposure).

It is important to be aware that the PL Smart Transceiver used in conjunction with some of the coupling circuits listed in this chapter might experience a reset event when subjected to higher surge levels. The system designer must determine if their application can tolerate a reset event under high surge conditions.

Samples of the AC mains coupling circuits documented in this chapter have been demonstrated to operate without reset when subjected to surge levels of at least 2kV. This level of immunity to reset events under surge conditions will vary with circuit layout. The greatest immunity levels can generally be achieved by locating D1 and C3 such that positive surge currents return to ground without passing close to the PL Smart Transceiver.

If a non-isolated coupling application requires greater reset immunity then the optional components shown in Figure 4.29 can be added. The corresponding optional components to increase reset immunity with isolated coupling circuits are shown in Figure 4.30. Coupling circuits that include these optional components have been demonstrated to not reset when subjected to 6kV surge events.

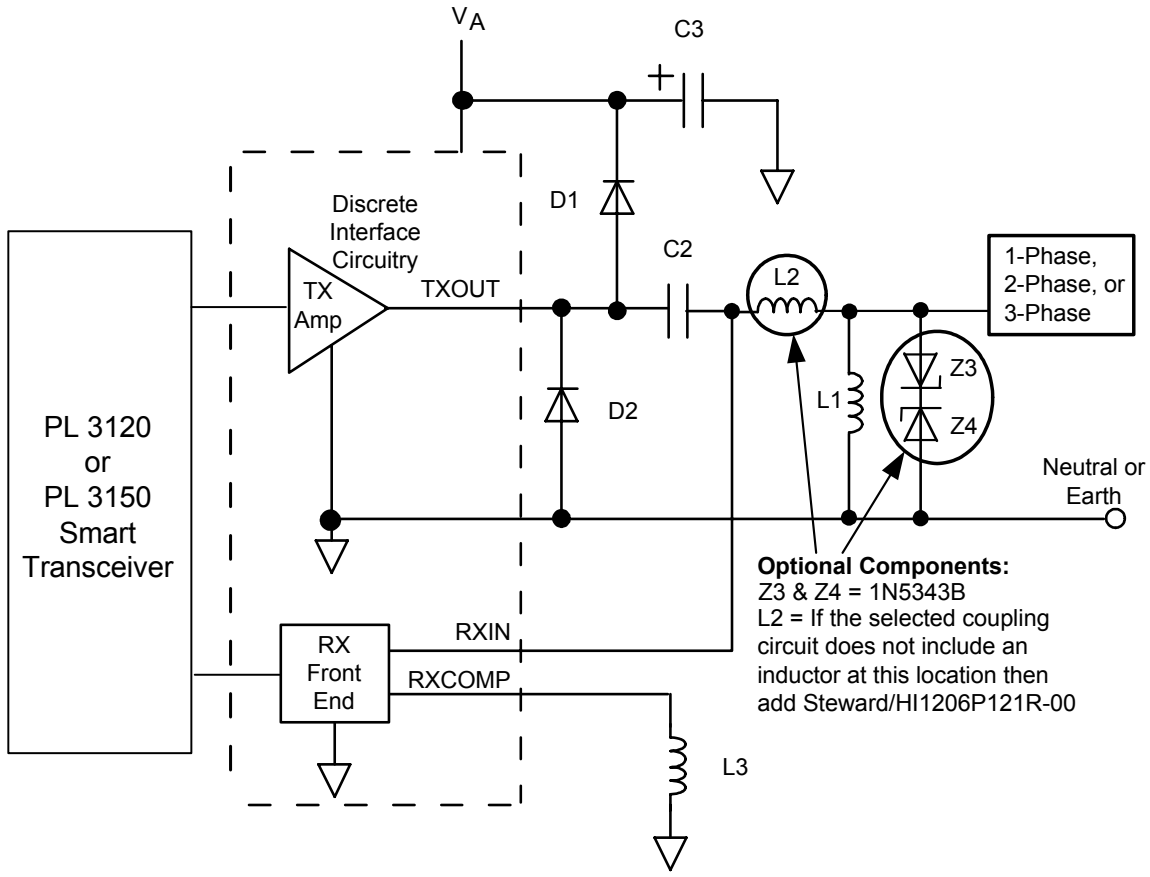


Figure 4.29 Optional Components for Non-Isolated Coupling Circuits

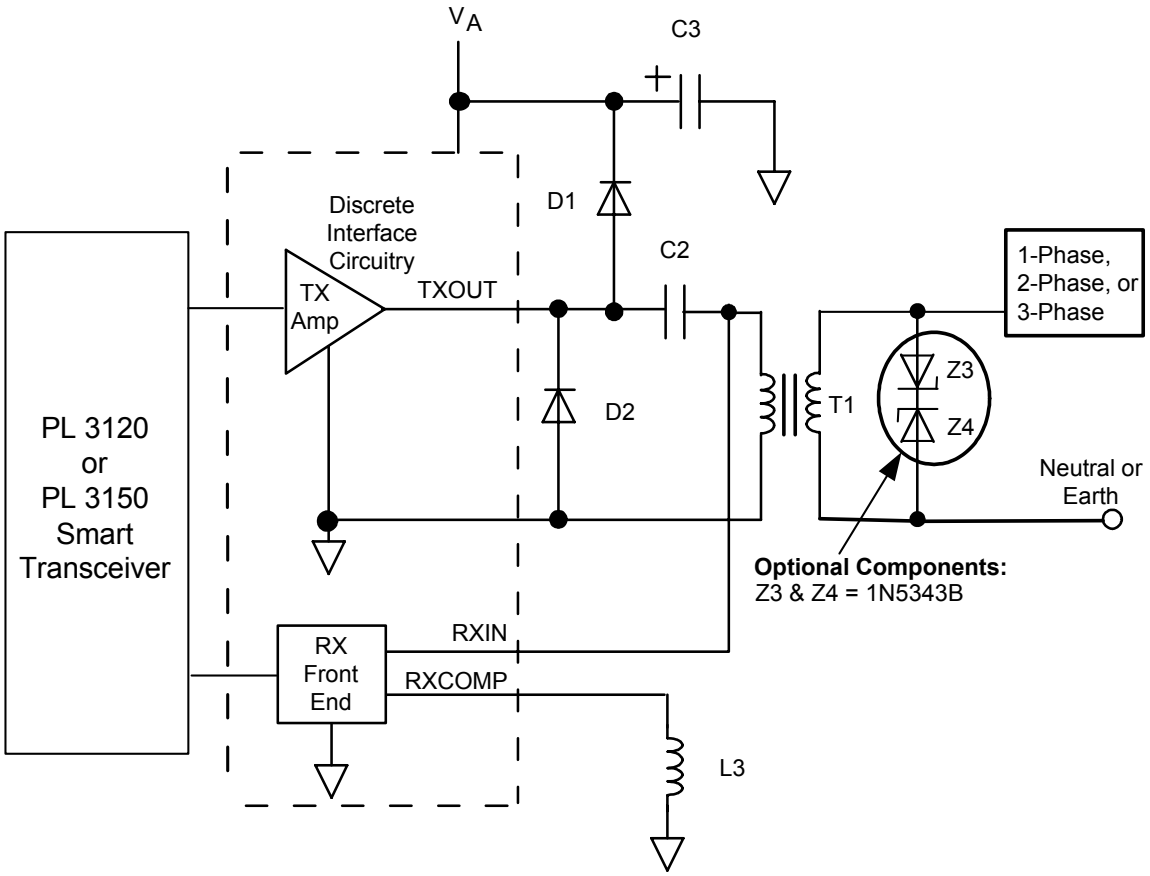


Figure 4.30 Optional Components for Isolated Coupling Circuits

5

Power Supplies for PL Smart Transceivers

Introduction

There are a number of power supply options available for use with the PL 3120 and PL 3150 Smart Transceivers. These various options differ in key characteristics such as size and cost. The following table is designed to aid in the selection of the optimal supply type.

Table 5.1 Power Supply Options

Power Supply Type	Application Current	Chip Support	Safety-Isolated	Universal Input (see Note 1)	Relative Cost (see Note 2)	Relative Size (see Note 2)	Relative Design Effort (see Note 2)	Page
Energy Storage Capacitor Input	≥25mA	PL 3120 Smart Transceiver	No	No	1	1	2	158
Energy Storage Linear	≥10mA	PL 3120 Smart Transceiver	Yes	No	2	2	2	164
Traditional Linear	Any	PL 3120 and PL3150 Smart Transceivers	Yes	No	3	≥ 3	1	165
Wall-plug Supply and Coupler	≥150mA	PL 3120 and PL3150 Smart Transceivers	Yes	No	4	4	2	165
Pre-designed Energy Storage Switcher	≥10mA	PL 3120 Smart Transceivers	Yes	Yes	5	1	1	179
Pre-designed Switcher	≥100mA	PL 3120 and PL3150 Smart Transceivers	Yes	Yes	3	2	4	181
Off-the-shelf Switcher	Any	PL 3120 and PL3150 Smart Transceivers	Yes	Yes	10	≥ 5	4	185
Full Custom Switcher	Any	PL 3120 and PL3150 Smart Transceivers	Optional	Optional	4	≥ 3	10	185

Notes:

1. Multi-country line voltage support without switches
2. Relative here is 1 = low and 10 = high.

Power Supply Design Considerations

In order to realize the full communications capability of the PL Smart Transceivers, it is important to ensure that the power supply does not limit overall communication performance. Because the power supply input is directly connected to the communications channel, it has the potential both to attenuate the transmit signal and to couple noise into the input of the receiver. Likewise, the power supply outputs, V_{DD5} and V_A, have the potential to degrade performance by coupling noise into the PL Smart Transceiver. The design or selection of an appropriate power supply is critical in ensuring that neither power supply loading nor power supply noise degrades communications performance.

The following sections introduce some of the key design considerations in the selection or design of a power supply. For additional detail, consult the sections describing the specific power supply types.

Power Supply-Induced Attenuation

As discussed in Chapter 4, *Coupling Circuits,* attenuation of a power line communication signal can be a significant factor in overall system performance. A poorly chosen or poorly designed power supply can greatly increase signal attenuation. In particular, the input stage of a switching power supply can significantly attenuate both transmitted and received power line communication signals. Supplies which have a low input impedance at communication frequencies will require the addition of an inductor in series with the supply input. Optimal inductor selection will be covered in the section *Switching Power Supplies,* later in this chapter.

Power Supply Noise

Power supplies have the opportunity to introduce noise both at their inputs and outputs. Noise conducted out of the input onto the AC line can degrade communication performance as well as cause the device to violate emissions regulations. Similarly, output noise can couple into the transceiver and degrade communication performance.

Due to regulatory constraints, it is important to verify that the total noise conducted onto the AC mains is adequately contained. Some supplies might require the addition of an input filter, as shown in the section *Switching Power Supplies,* later in this chapter.

For information on conducted emissions test methodology, see Chapter 6, *Design and Test for Electromagnetic Compatibility.*

V_A Power Supply Voltage Range

When the PL Smart Transceiver is in receive mode, the allowed V_A supply range is 8.5V to 18V. When the PL Smart Transceiver is transmitting a message the V_A supply should be between 10.8V and 12.6V - unless the conditions described in this section are met. Under certain conditions the V_A supply range during transmission can be extended from a minimum of 8.5V to a maximum of 18V. These conditions, which are described below, allow the use of various types of unregulated power supplies thereby significantly reducing product cost.

The minimum V_A supply voltage while transmitting can be relaxed from 10.8V down to 8.5V when worst case line voltage, temperature, component tolerance and transmit power supply loading are present (including a maximum V_A transmit current of 250mA). This condition provides adequate headroom when the transmit amplifier is driving a low impedance line and its output voltage is somewhat less than 7Vpp. Note that any power supply design that takes advantage of the 8.5V lower limit on V_A must still maintain ≥10.8V under typical line voltage, current drain (including typical transmit current of 120mA from the V_A supply) and room temperature conditions. This condition

ensures adequate transmit amplifier headroom to drive the full 7Vpp signal onto the line under lighter load conditions.

Extending the maximum V_A range above 12.6V up to a maximum of 18V is allowed providing the thermal requirements of the transmit amplifier are met. The temperature of the amplifier depends on the on how frequently the device will be required to transmit, the ambient temperature and the power supply voltage. The key power supply parameter with regard to amplifier heating is the *average V_A supply voltage during transmission* (i.e., if a loosely regulated supply is used and the V_A supply droops during transmission the average V_A voltage over the duration of a transmission determines the heat generated by the amplifier). If we express how frequently the device is required to transmit in terms of maximum transmit duty cycle then the thermal requirements of the amplifier are met by satisfying the following formula:

$$V_{ATXAVE} < (150\text{-}T_{AMAX})/(8*D_{MAX});$$

Where:

V_{ATXAVE} = Average V_A supply voltage while transmitting

T_{AMAX} = Maximum ambient temperature inside the product enclosure (degrees C)

D_{MAX} = Maximum transmit duty cycle of the device (expressed as a decimal number)

The maximum transmit duty cycle generally does not exceed 64% because this is the largest value possible for a device that uses LONMARK® interoperable transceiver parameters and transmits messages of ≤ 34 Bytes (see the *Note* on page 158 in the *Energy Storage Power Supplies* section). Note that many products transmit infrequently and thus have much lower transmit duty cycle requirements than 64%.

Using the above formula several common options are shown in Table 5.2.

Table 5.2 Maximum V_A Vs. Temperature and Duty Cycle

T_{AMAX} (°C)	D_{MAX} (%)	Maximum V_{ATXAVE} (V)
85	64	12.7
85	45	18
70	64	15.6
70	55	18

Note: The above discussion applies to the standard 1Ap-p transmit amplifier. Refer to Appendix A for information if the optional 2Ap-p transmit amplifier is used.

Energy Storage Power Supplies

In cost or size-sensitive devices, it might be desirable to use an energy storage power supply. These supplies take advantage of the wide supply voltage range and the large difference between the transmit and receive current requirements of the transceiver, storing energy while the device is in receive mode and expending it during signal transmission. By using an energy storage system, the device can use a smaller, less expensive, power supply than a device with an equivalent "full power" supply. In this way, a low-current supply can be used which only has to supply the required receive mode current, plus an incremental current to recharge a capacitor between transmissions.

An energy storage power supply is generally designed so that its V_A supply voltage, while in receive mode, is above the 12V nominal specification (e.g., 15V). During packet transmission the voltage on the V_A supply is then allowed to drop, as energy from the capacitor is used for transmission. The value of the energy storage capacitor must be large

enough so that the V_A supply voltage is still sufficient for proper operation by the end of a single maximum-length packet transmission. Proper device operation is then maintained when the energy storage capacitor is selected such that the V_A power supply meets both of the following conditions:

- $V_A \geq 10.8V$ after the typical I_A transmit load of 120mA has been active for 140.7ms (see ***Note*** below) for an A-band device (92.2ms for a C-band device). This condition only needs to be met at room temperature with nominal AC line voltage.
- $V_A \geq 8.5V$ after the worst case I_A transmit load of 250mA has been active for 140.7ms (see ***Note*** below) for an A-band device (92.2ms for a C-band device). For proper node operation this condition must be met over the full range of worst-case component tolerances (including I_{DD5} drain), AC line voltage, and temperature.

Note: For the primary carrier frequency, a 32 byte packet corresponds to a maximum transmission duration of 113.8ms for an A-band device (74.6ms for a C-band device).

Calculating the maximum transmission duration for a packet at the secondary carrier frequency is somewhat more complicated due to the combination of error correction and data compression used with that carrier frequency. If we consider a case where message traffic satisfies the above condition plus three further common conditions, then the maximum transmission duration can be calculated to be 140.7ms for an A-band device (92.2ms for a C-band device). This maximum duration is applicable for applications where: 1) there are no priority packet transmissions from the energy storage device; 2) subnet and node numbers are in the range 0 through 15; and 3) if a six byte domain is used, it is assigned to be equal to a Neuron core ID number. For applications which do not meet the conditions listed in this note, contact Echelon LonSupport for maximum packet length calculations.

Having chosen a storage capacitor to provide adequate voltage after transmission of a single packet, the power management feature of the PL Smart Transceiver must also be enabled to ensure adequate supply voltage over the span of multiple packet transmissions. The power management feature prevents excessive power supply droop from transmission of multiple back-to-back packets under worst case conditions by monitoring the voltage on the energy storage capacitor and then, if required, regulating the time between transmissions so that the capacitor has time to recharge.

The power management feature is enabled by first connecting an appropriate resistor voltage divider between the V_A supply and the OOGAS pin of PL 3120/PL 3150 IC, as shown in reference schematic diagrams described in Appendix A. In addition, use of a standard transceiver type with a "-LOW" suffix is required to enable the power management feature, as described in Chapter 8, *PL Smart Transceiver Programming.*

Once enabled, the power management system detects any instance where the V_A supply drops below the lower power management threshold (nominally 7.9V). The PL Smart Transceiver then delays transmission until the energy storage capacitor has been recharged to allow transmission of a complete packet. The PL Smart Transceiver then transmits any waiting packets once the capacitor has fully charged.

If a high packet transmission duty cycle causes V_A to drop too low during packet transmission, such that a packet is aborted prior to completion, the PL Smart Transceiver will re-transmit that packet independent of the LonTalk protocol service in use. Even when unacknowledged service is employed, a packet that is interrupted by low supply voltage will be re-transmitted once the power management system determines that the supply is fully recharged.

The power management circuitry of the PL Smart Transceiver adjusts the amount of time that it inhibits transmission based on the device's actual recharge characteristics. This feature allows energy storage devices to typically transmit without intervention from the power management circuitry. When a device powered by an energy storage supply has worst case component tolerances and is exposed to worst case AC line conditions, the power management circuitry of the Smart Transceiver calculates a suitable transmit hold-off time by measuring the supply recharge rate. The formula used to make this calculation is three times the time required for the supply to charge from its lower power management threshold (nominally 7.9V) to its upper power management threshold (nominally 12.1V). Figure 5.1 illustrates examples of an energy storage node operating under both typical and worst case conditions.

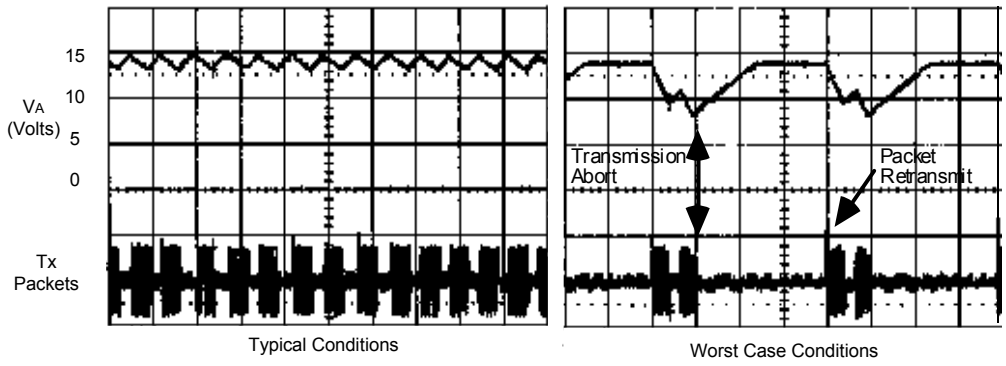


Figure 5.1 Supply Voltage vs. Packet Transmission

Energy Storage Capacitor-Input Power Supplies

A particularly cost-effective example of an energy storage power supply is the *capacitor-input power supply.* The most attractive feature of this supply is that both V_A and V_{DD5} supplies can be built with just a few components for approximately US$1.00.

Figure 5.2 illustrates the operation of a capacitor-input power supply. As shown in the figure, a capacitor in series with the AC mains causes AC current to flow through a zener diode, which acts as a shunt regulator. This regulator is selected to limit the V_A supply voltage to ≤16V. An energy storage capacitor is connected across the shunt regulator to provide current capacity required for transmission. Note that unused source current flows through the shunt regulator, maximizing the zener diode temperature when the supply load is at a minimum. Because the regulation voltages of zener diodes above 10V have strong positive temperature coefficients, a pair of forward-biased silicon diodes, which have negative temperature coefficients, have been added in series with a slightly lower-voltage zener diode. Note that this type of capacitor-input power supply would inherently attenuate communication signals if not for the addition of a series inductor, as shown in Figure 5.2

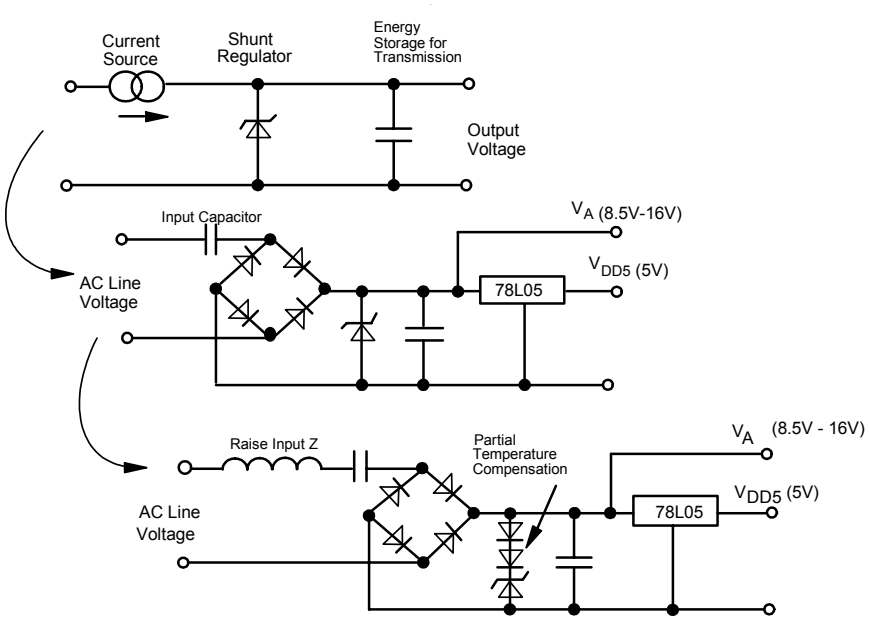


Figure 5.2 Capacitor-Input Power Supply Theory of Operation

Due to the low current available, the application of capacitor-input power supplies is generally limited to PL 3120 based devices which require minimal I/O application current (e.g., latching relays, SCR triggers, low-power LEDs). Figure 5.3 presents a schematic for an A-band device based on a PL 3120 Smart Transceiver IC powered by a capacitor-input power supply. Figure 5.4 shows the C-band version. These devices are designed to operate with an enclosure internal air temperature range of 0-70°C. The coupling circuit shown in these figures is different from those shown in Chapter 4 to accommodate the unique requirements of this capacitor-input node.

The A-band option provides enough stored energy to transmit a 140.7ms packet under worst-case conditions prior to recharging. Each of the C-band options provides sufficient stored energy to transmit one complete 92.2ms packet under worst-case conditions prior to recharging. Under typical conditions, A-band and C-band versions support a maximum transmit duty cycle of ≥65%. Under worst-case conditions, they each support maximum transmit duty cycles of ≥10%. Note that the use of any of these capacitor-input power supply options requires that the configuration data of the device be programmed to enable power management, as described in Chapter 8.

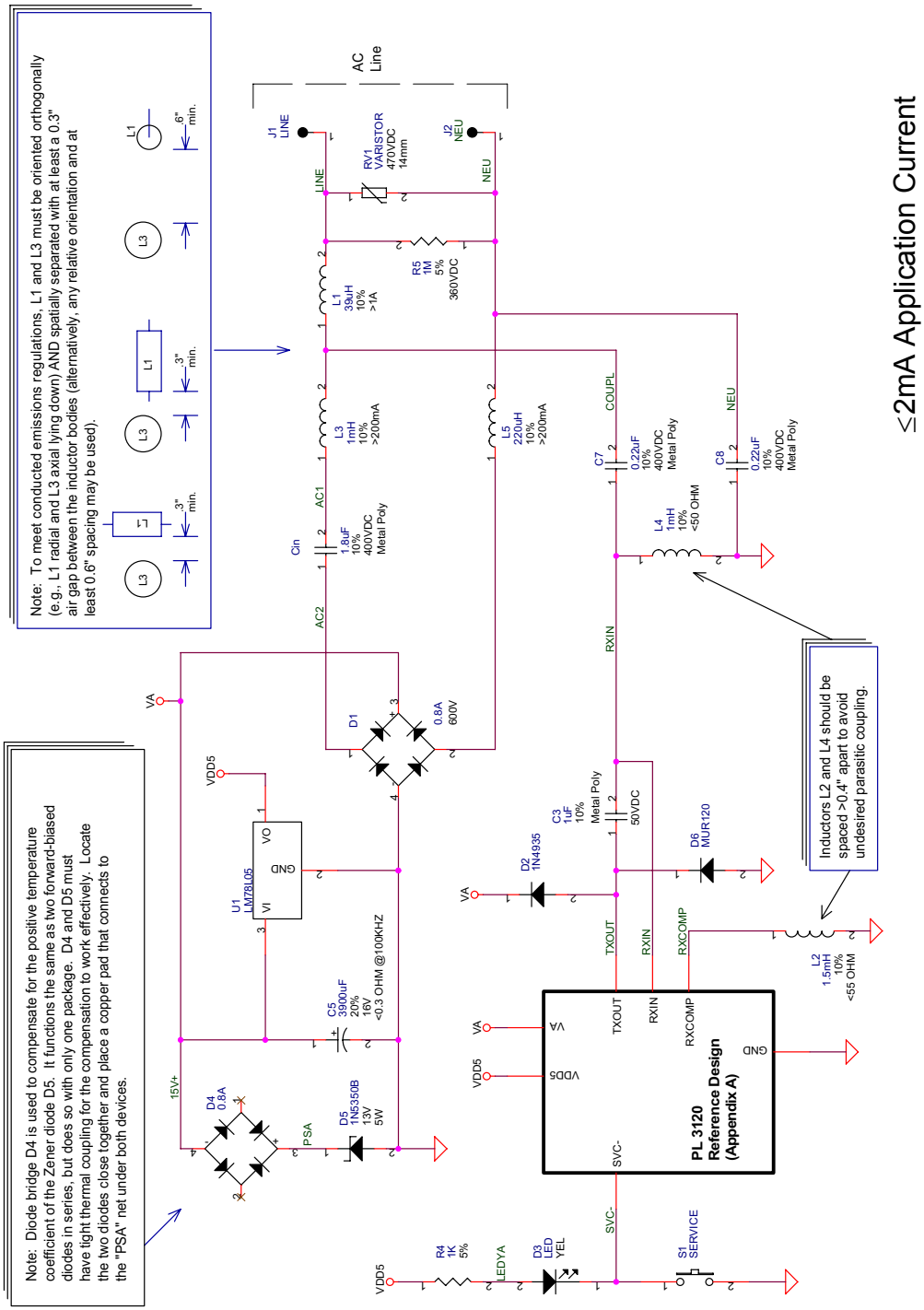
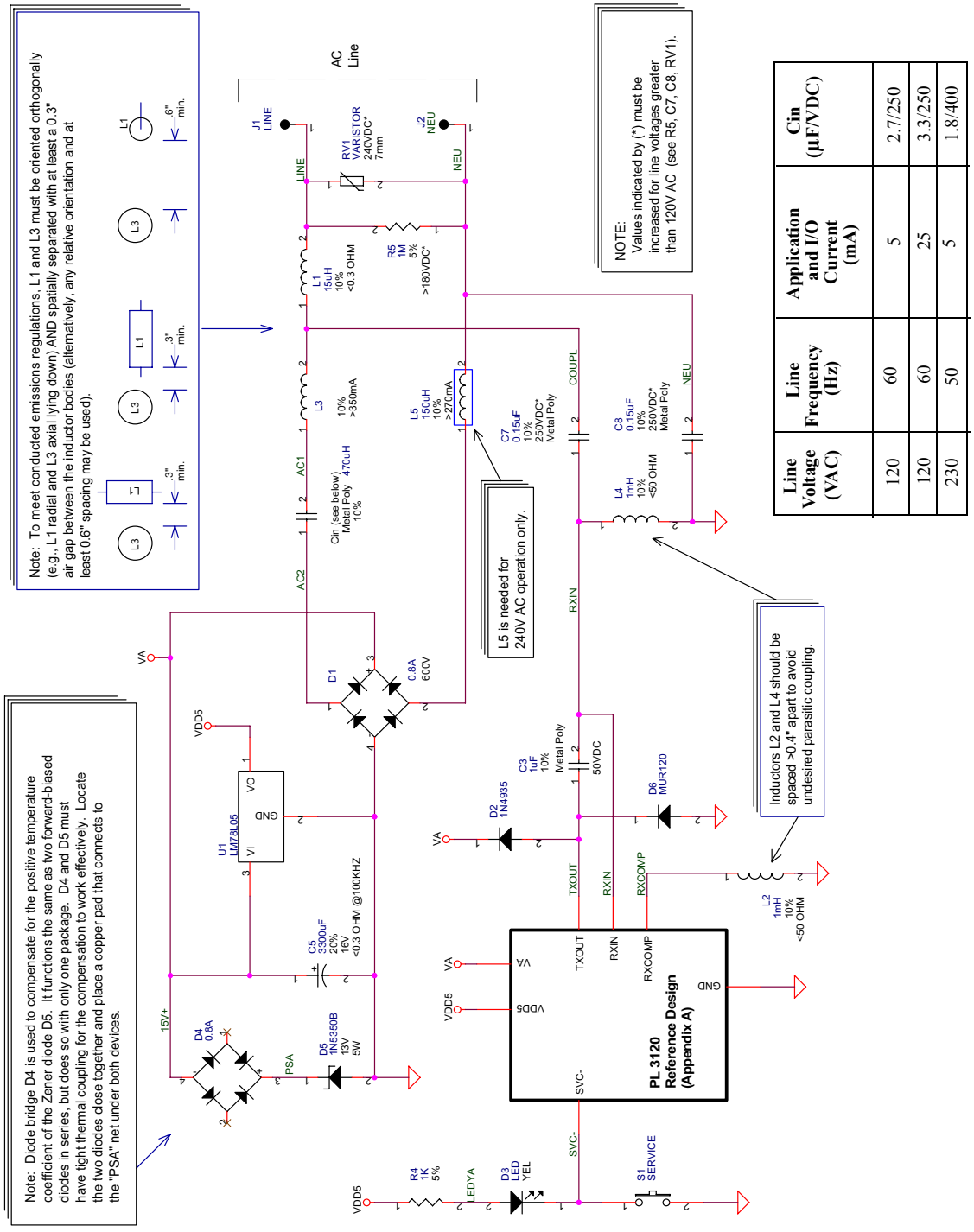


Figure 5.3 A-band Capacitor-Input Power Supply Schematic



Line Voltage (VAC)	Line Frequency (Hz)	Application and I/O Current (mA)	Cin (µF/VDC)
120	60	5	2.7/250
120	60	25	3.3/250
230	50	5	1.8/400

Figure 5.4 C-band Capacitor-Input Power Supply Schematic

Energy Storage Linear Supplies

For products requiring minimal application current and safety isolation, an energy storage linear supply might be the smallest and most cost effective option. Consider a device based on a PL 3120 Smart Transceiver consuming 10mA of application and I/O current. Using a linear V_A power supply and a linear regulator for the V_{DD5} supply, the worst case current requirements are presented in the table below.

Table 5.3 Example Worst-Case Node Current Consumption

	Transmit	Receive
V_A Current	250mA	0.5mA
PL 3120 Smart Transceiver V_{DD5} Current	13mA	13mA
Application & I/O Current	10mA	10mA
78L05 Regulator Current	5mA	5mA
Total	278mA	29mA

A traditional linear supply would require a transformer with an output current rating of ≥300mA. By taking advantage of the PL 3120 Smart Transceiver's power management feature, an energy storage linear supply can be built with a 100mA transformer.

Figure 5.5 shows an example of an energy storage linear supply. This example supply meets the criteria listed in the energy storage section of this chapter, for both A-band and C-band operation. With a transient load of 120mA for 140.7ms added to a constant 29mA receive load, this supply does not drop below 10.8V. This supply also maintains ≥9.0V after a 250mA load is added to the constant 29mA load for 140.7ms. Both of these criteria hold true even with an AC line voltage which is 10% low and an output capacitance value that is 20% low. In addition, this example supply supports duty cycles of ≥65% under typical transmission conditions and ≥10% over worst case line voltage and component tolerances.

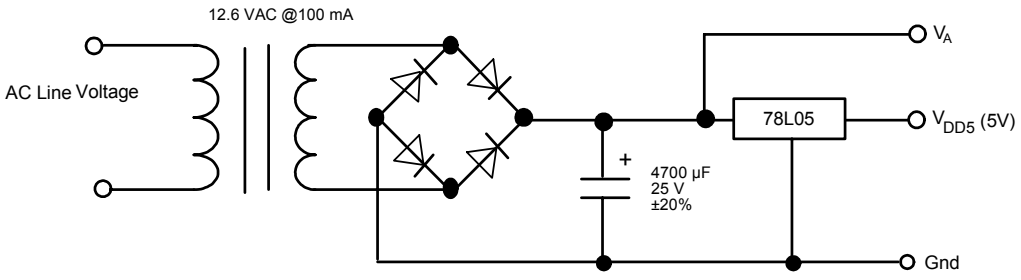


Figure 5.5 Energy Storage Linear Power Supply

In summary, an energy storage linear supply differs from a traditional linear supply in the following ways:

- Allows the use of a smaller transformer
- Requires more output capacitance for energy storage

- Requires that the device be programmed to enable power management, as described in Chapter 8.
- Under typical conditions, exhibits transmit duty cycles which are not limited. Over the full range of line voltage and component tolerance, the power management circuitry of the PL Smart Transceiver can act to regulate a particular transmit duty cycle (to ≥10% in the above example) of the device.

Traditional Linear Power Supplies

This option is usually suitable if the physical size of the power supply is not constrained in the application, because linear supplies tend to be physically larger than switching power supplies. Linear power supplies do not load the power line in the range of the PL Smart Transceiver communication frequencies, nor do they generate significant noise. For these reasons, a linear power supply can be used without concern that communication performance will be adversely affected.

Wall-Plug Power Supply/Coupler

One very convenient linear power supply implementation combines a 50/60Hz wall-plug power supply with a L-N coupling circuit. Refer to Figure 4.28 and Table 4.13 for detailed information regarding the use of this Wall-Plug Power Supply/Coupler available from Tamura Corporation. With nominal AC line voltage, a V_A supply voltage of 10.8V to 17V is provided with load currents from 0 to 360mADC. With a worst-case AC line voltage tolerance of ±10%, the V_A supply is 8.5V to 18V with up to 360mADC of output current. This supply is rated for operation over a temperature range of 0C to 40C.

Switching Power Supplies

While generally smaller than linear power supplies, switching power supplies can be a significant source of noise and power line signal attenuation. As a result the required design effort is significantly greater than that required for linear or capacitor-input power supplies.

Several design options are available for use if a switching power supply is required due to size or application current constraints. These options include several pre-designed switching supplies, an off-the-shelf switcher, and a custom-designed switcher. They are described following the discussion of switching supply design issues.

Power Supply-Induced Attenuation

The input stage of a switching power supply typically contains an EMC filter that includes one or more capacitors connected directly from line to neutral and, in many cases, additional capacitors from line and neutral to ground. When the AC line terminals of the switching power supply are connected to the AC mains (in parallel with the coupling circuit), additional signal attenuation occurs. This loss can be avoided by inserting a series inductor between the power supply input and the power line communication channel as shown in Figure 5.6.

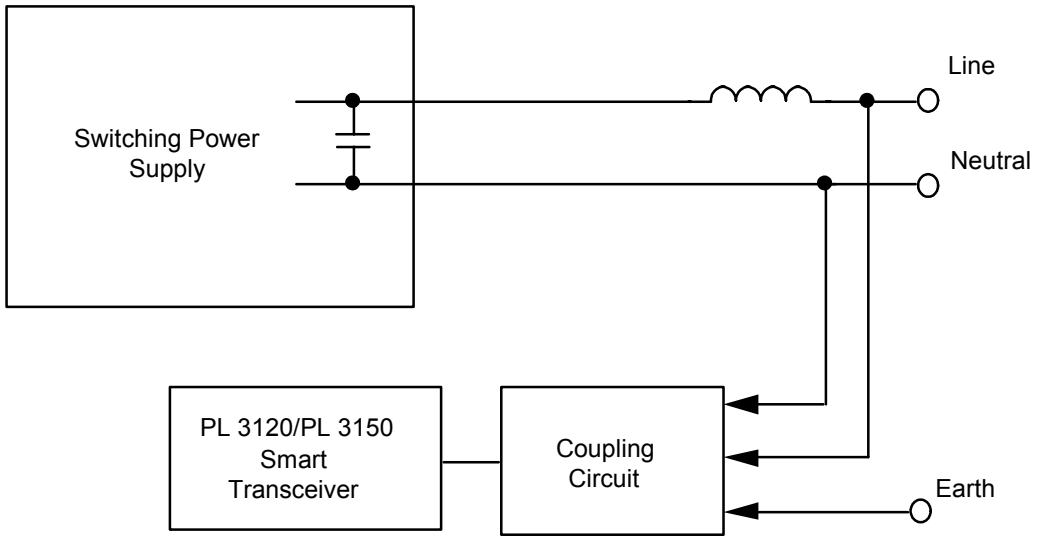


Figure 5.6 Reducing Attenuation Caused by a Switching Power Supply

Including this inductor is necessary because the increase in attenuation for a given load is much worse when the load, in this case the switching power supply, is connected directly to the transceiver. In contrast, the loading caused by a switching supply that is separated from the receiver is reduced by the series inductance of power line wiring.

The loading effect of a switching power supply almost always dictates the addition of the inductor for L-to-N coupling circuits. The inductor may or may not be required for L-to-E coupling circuits depending on the EMC filter topology of the switching power supply. In either case, the value of the inductor should be chosen such that the power supply does not impose a low impedance onto the power line in the communication frequency range. The appropriate value of inductance is a trade-off between required impedance, which is a function of system topology, and node cost. The selected inductor must have a current rating which is greater than the peak current drawn by the power supply in order to avoid impedance reduction due to inductor saturation. Higher impedances require larger inductance values which are more expensive for a given power supply input current.

For most AC mains distribution systems, where the line impedance at the PL Smart Transceiver communication frequencies is typically in the range of 1 to 20 ohms, a power supply input impedance of 100 ohms is sufficient to avoid added signal attenuation. To maximize communication distance on mains distribution systems between buildings where the system impedance can be as high as 50 ohms, a minimum power supply input impedance of 250 ohms is recommended.

An example of a system that would benefit from an input impedance >100 ohms would be one in which 100 or more PL Smart Transceiver-based devices were connected to a 1000m (3280ft) powered, twisted pair cable. In this case the input impedance of the power supply could limit either the maximum transmission distance and/or the maximum number of devices that could be connected to the cable. To maximize communication distance on dedicated twisted pair wiring where the system impedance is approximately 100 ohms, a minimum power supply input impedance of 500 ohms is recommended. For extreme cases with >100 nodes on dedicated lines longer than 1000m, a power supply input impedance of 2000 ohms might be needed to maximize communication distance. Table 5.4 shows the appropriate inductor value by application.

Table 5.4 Recommended Inductor Value vs. Application

Application	Network Impedance at Communication Frequencies	Inductor Impedance at Primary Communication Frequencies	A-band Inductor Value	C-band Inductor Value
Single building AC mains	1-20 ohms	≥100 ohms	≥220µH	≥150µH
Inter-building mains distribution	1-50 ohms	≥250 ohms	≥470µH	≥330µH
Dedicated cable ≤100 nodes ≤100m	50-100 ohms	≥500 ohms	≥1mH	≥680µH
Dedicated cable >100 nodes >100m	50-100 ohms	≥2000 ohms	≥3.9mH	≥2.4mH

There is one further constraint on the value of the inductor. When the inductor is combined with the input capacitance of the switching supply, the LC resonant frequency should be at least one octave away from the communication frequency range (70kHz-90kHz for A-band and 110kHz-138kHz for C-band). The unintentional series resonance between the inductor's reactance and the power supply's capacitive reactance can produce a low impedance at communication frequencies if this frequency range is not avoided.

One way to reduce the size and cost of an inductor used to raise a power supply's input impedance is to purposefully parallel resonate it at the communication frequency with a capacitor, as shown in Figure 5.7. If this option is chosen, resistive damping must be included so that impulsive power line noise does not excite excessive filter ringing, which could degrade the reception of weak signals. The parallel resistor has been selected to optimize receive impedance and impulsive noise damping. Note that even though only a 100µH inductor is shown in Figure 5.7, this circuit built with A-band values provides a series impedance of ≥150 ohms from 70kHz to 90kHz due to the parallel resonant effect. When built with C-band values the series impedance is ≥200 ohms from 125kHz to 138kHz. Also, note that the inductor must be rated for the peak AC current drawn by the power supply.

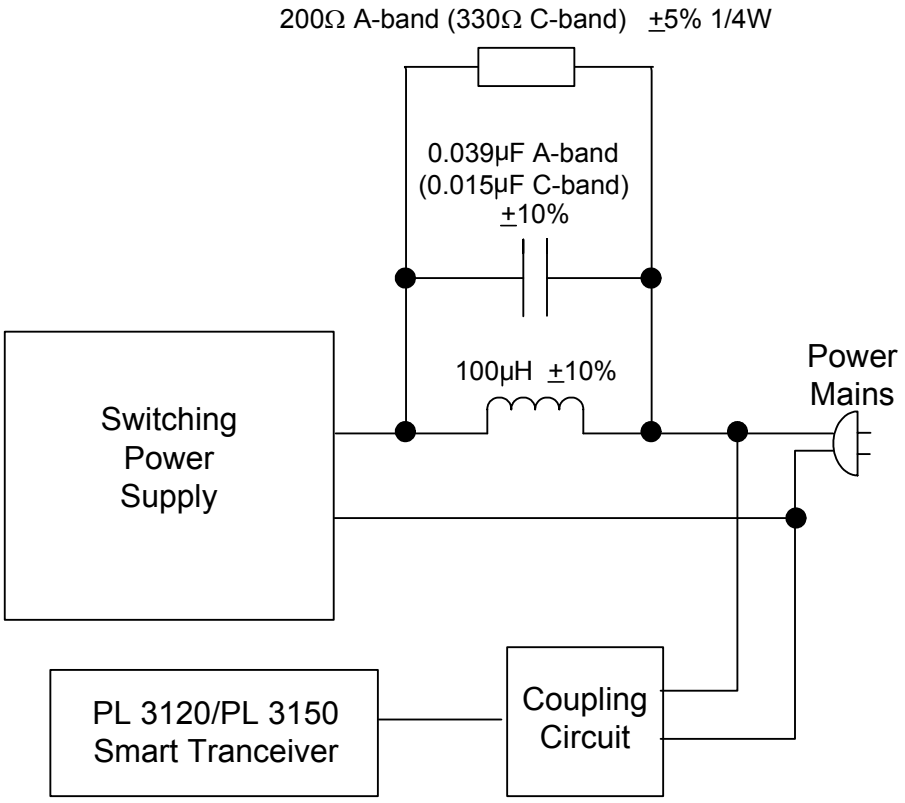


Figure 5.7 Reducing Attenuation Caused by a Switching Power Supply with a Resonant Circuit

Noise at the Power Supply Input

In order to achieve maximum communication performance and to comply with the conducted emissions specifications of CENELEC EN 50065-1 and FCC Part 15, the switching power supply input must not conduct excessive noise onto the power mains. A switching power supply contains an oscillator that operates at a frequency between 10kHz and several MHz. Depending on the power supply design, significant energy at the switching frequency fundamental and/or its harmonics can appear at the input (line side) of the power supply. If the amplitude of the signal is large enough in sensitive frequency ranges, the performance of the PL Smart Transceiver can be degraded.

While the PL Smart Transceiver is designed to operate reliably with a combination of attenuation and significant switching supply noise, noise from the switching power supply closest to the receiver will have the most deleterious effect on communication performance. Noise from more distant sources will be attenuated before reaching a receiver, minimizing its effect on reception.

Switching Power Supply Frequency Selection

Selection of an appropriate operating frequency for a switching power supply will minimize the effect of switching noise on the communication performance of the PL Smart Transceiver. By choosing an operating frequency such that the fundamental and harmonics of that switching supply avoid the transceiver's communication frequencies, the

amount and cost of additional circuitry to filter interference from the switching supply can be minimized. Table 5.5 below lists the recommended switching frequency ranges. The switching supply should be designed such that the fundamental switching frequency falls within the stated ranges under all line, load, environmental, and production conditions.

Table 5.5 Recommended Switching Power Supply Fundamental Operating Frequencies

Recommended Frequency Ranges
46kHz - 55kHz
90kHz - 110kHz
>155kHz

Switching Power Supply Input Noise Masks

The noise "masks" presented in Figures 5.8 through 5.11 show the maximum noise allowable at the input of a switching power supply such that optimum performance of the PL Smart Transceiver is achieved **and** the appropriate conducted emissions specification is met. Figure 5.8 defines the noise mask for A-band CENELEC EN 50065-1 [2] conducted emissions compliance. Figure 5.9 defines the noise mask for A-band FCC [1] conducted emissions compliance. Likewise Figure 5.10 defines the noise mask for C-band CENELEC EN 50065-1 conducted emissions compliance and Figure 5.11 defines the noise mask for FCC conducted emissions compliance. The limits assume that the PL Smart Transceiver is used in conjunction with one of the recommended coupling circuits shown in Chapter 4.

Measurements of a particular power supply should be made by connecting the supply to the artificial mains network as specified in subclause 8.2.1 of CISPR Publication 16, second edition [3]. Measurements should be made over the full range of anticipated loads on the supply because many switching supplies vary their switching frequency with load. Two different limits are shown for the CENELEC EN 50065-1 measurements. One limit is measured using a quasi-peak detector, the other using an average detector. Note that those limits are the same as required for any other CENELEC compliant product, except in the communication range of 90kHz and below for A-band devices (110kHz to 138kHz for C-band devices) where lower noise levels are specified.

For FCC applications, the limits of Figures 5.9 and 5.11corresponds to FCC Class B limits for frequencies above 450kHz. Below 450kHz, the limits are set such that the full communication performance of the PL Smart Transceiver is maintained. A quasi-peak detector should be used when verifying power supply noise against the limit lines of Figures 5.9 and 5.11.

For both CENELEC and FCC measurements, the measurement bandwidths are 200Hz for measurements below 150kHz, and 9kHz for measurements above 150kHz, as described in CISPR 16.

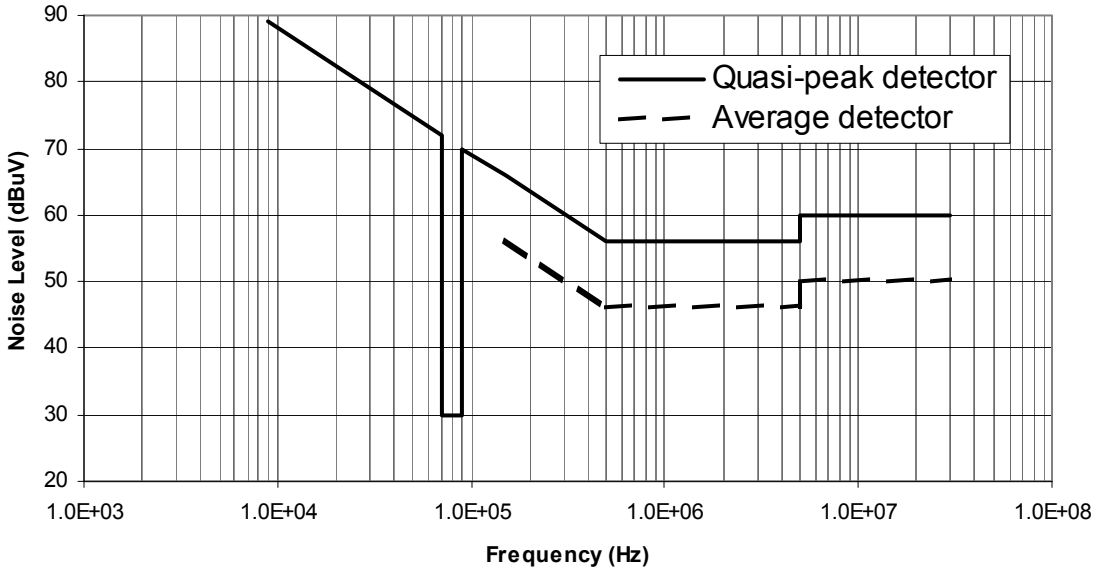


Figure 5.8 Switching Power Supply Input Noise Limits for A-band CENELEC Compliance

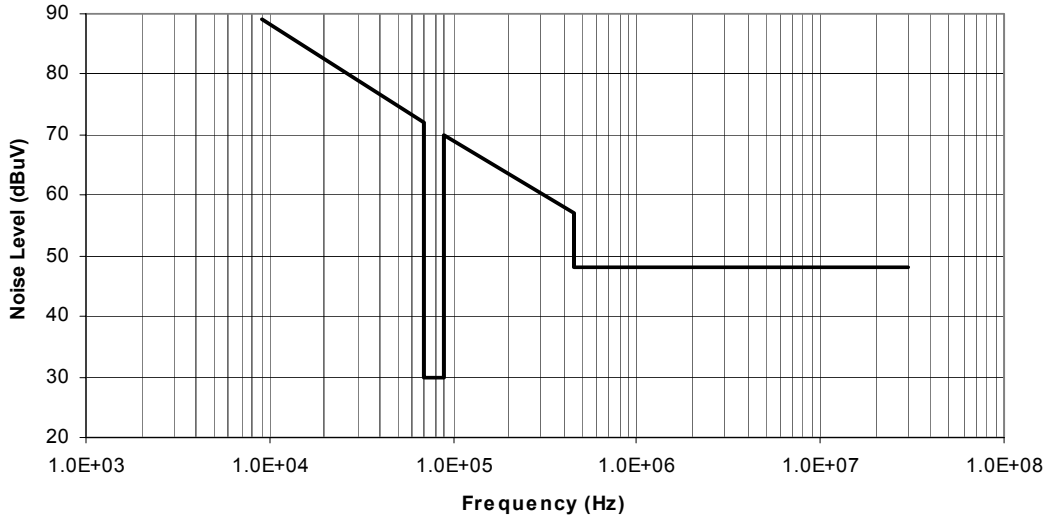


Figure 5.9 Switching Power Supply Input Noise Limits for A-band FCC Compliance

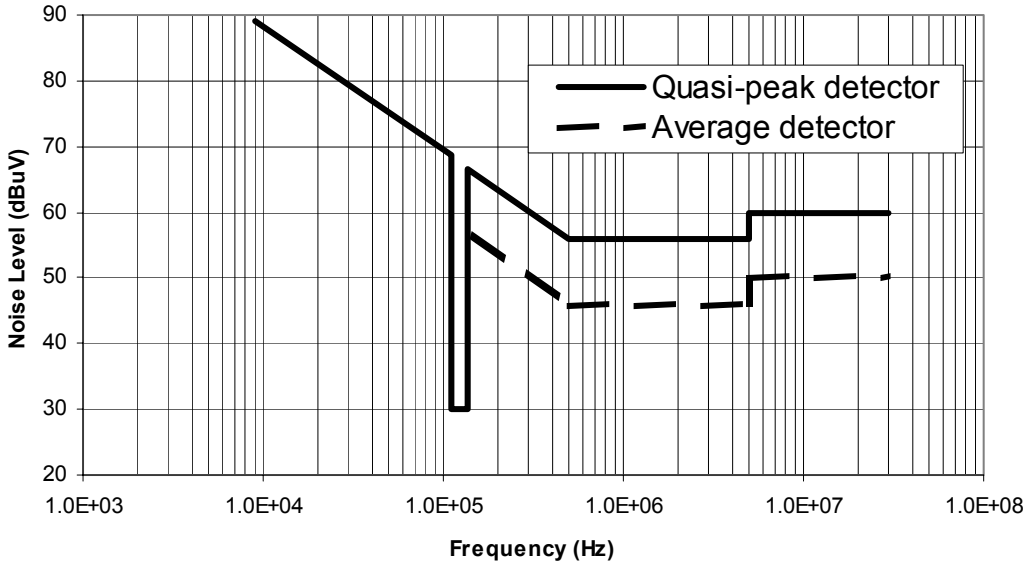


Figure 5.10 Switching Power Supply Input Noise Limits for C-band CENELEC Compliance

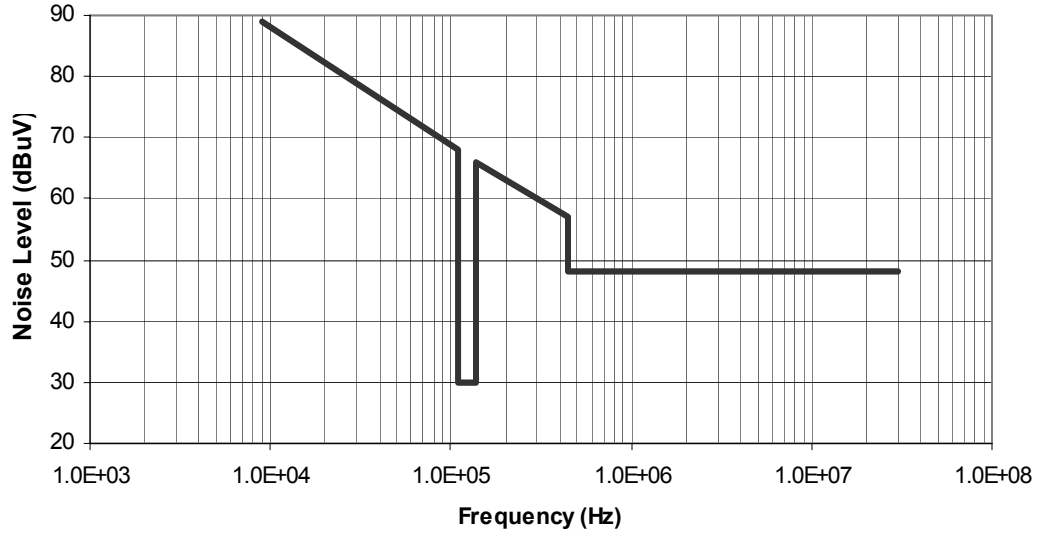


Figure 5.11 Switching Power Supply Input Noise Limits for C-band FCC Compliance

Table 5.6 lists the endpoints of the straight lines shown in Figure 5.8, and Table 5.7 lists those shown in Figure 5.9. Table 5.8 lists the end points of the straight lines shown in Figure 5.10. Table 5.9 lists the levels shown in Figure 5.11.

Table 5.6 Switching Power Supply Input Noise Limits for A-band CENELEC Compliance

Frequency (kHz)	Noise Level (dBμV): Quasi-Peak Detector	Noise Level (dBμV): Average Detector
9	89	N/A
70	72	N/A
70+	30	N/A
90	30	N/A
90+	70	N/A
150	66	56
500	56	46
5000	56	46
5000+	60	50
30000	60	50

Table 5.7 Switching Power Supply Input Noise Limits for A-band FCC Compliance

Frequency (kHz)	Noise Level (dBμV): Quasi-Peak Detector
9	89
70	72
70+	30
90	30
90+	70
450	57
450+	48
30000	48

Table 5.8 Switching Power Supply Input Noise Limits for C-band CENELEC EN 50065-1 Compliance

Frequency (kHz)	Noise Level (dBμV): Quasi-Peak Detector	Noise Level (dBμV): Average Detector
9	89	N/A
110	68	N/A
110+	30	N/A
138	30	N/A
138+	66	56
500	56	46
500+	56	46
5000	56	46
5000+	60	50
30000	60	50

Table 5.9 Switching Power Supply Input Noise Limits for C-band FCC Compliance

Frequency (kHz)	Noise Level (dBμV): Quasi-Peak Detector
9	89
110	68
110+	30
138	30
138+	66
450	57
450+	48
30000	48

A power supply that does not meet the appropriate noise mask for the power supply input might require a filter between the local switching power supply and the power mains.

An example of a filter which both attenuates switching supply noise and provides >200 ohm input impedance is shown in Figure 5.12. Note that both inductors must be rated for the peak AC current drawn by the power supply; the 3.3 ohm resistor should have a power rating consistent with the AC current drawn by the power supply, and its voltage drop should be verified as acceptable.

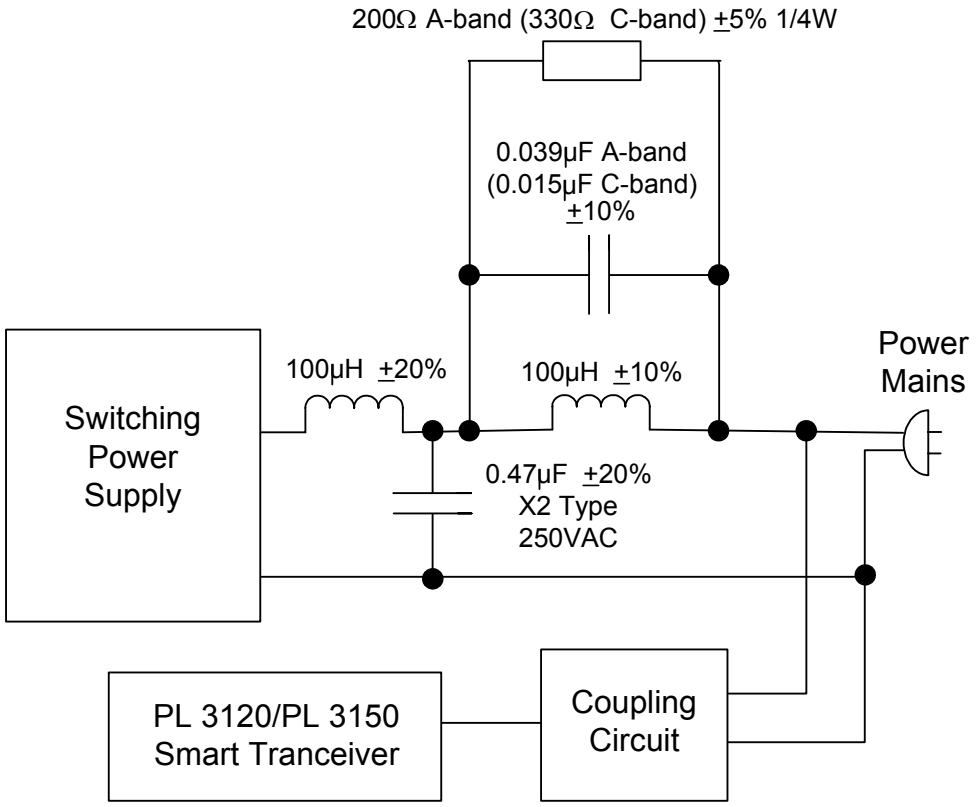


Figure 5.12 Optional Switching Power Supply LC Network

This A-band version of the filter has the attenuation characteristics shown in Figure 5.13, when connected to a 50Ω mains network. The characteristics of the C-band version of the filter into a 50Ω network are shown in Figure 5.14.

If the power supply noise drops by less than the values shown in the appropriate figure it is likely due to parasitic coupling between the two inductors. If this occurs, filtering close to the level shown in Figures 5.13 or 5.14 can usually be accomplished by adjusting the relative location and orientation of the inductors (orthogonal orientation typically reduces inductor coupling). Alternately, shielded or toroidal inductors can be used to reduce coupling.

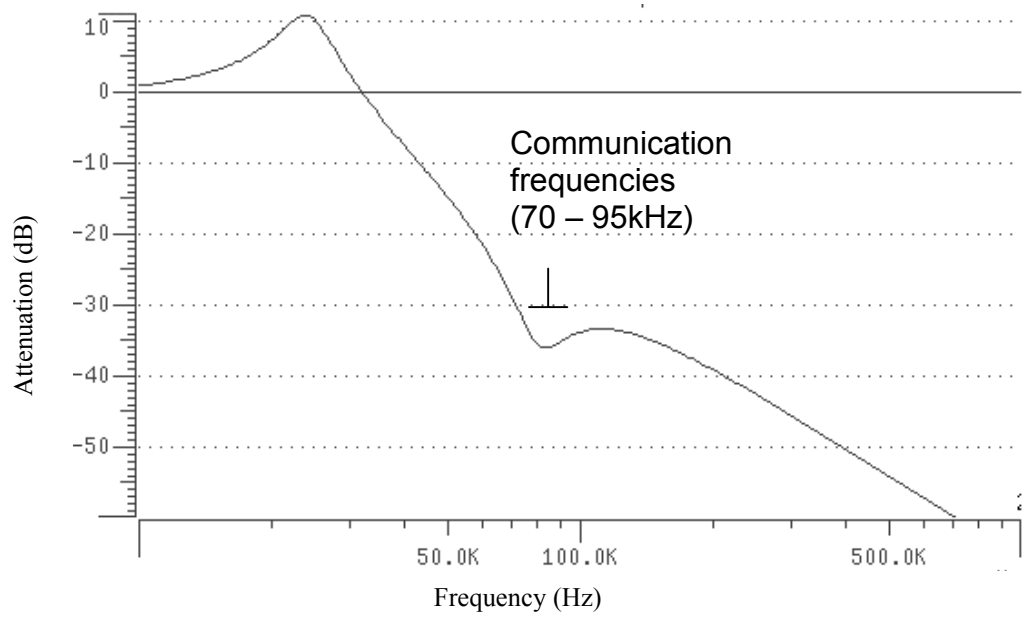


Figure 5.13 A-band Filter Frequency Response

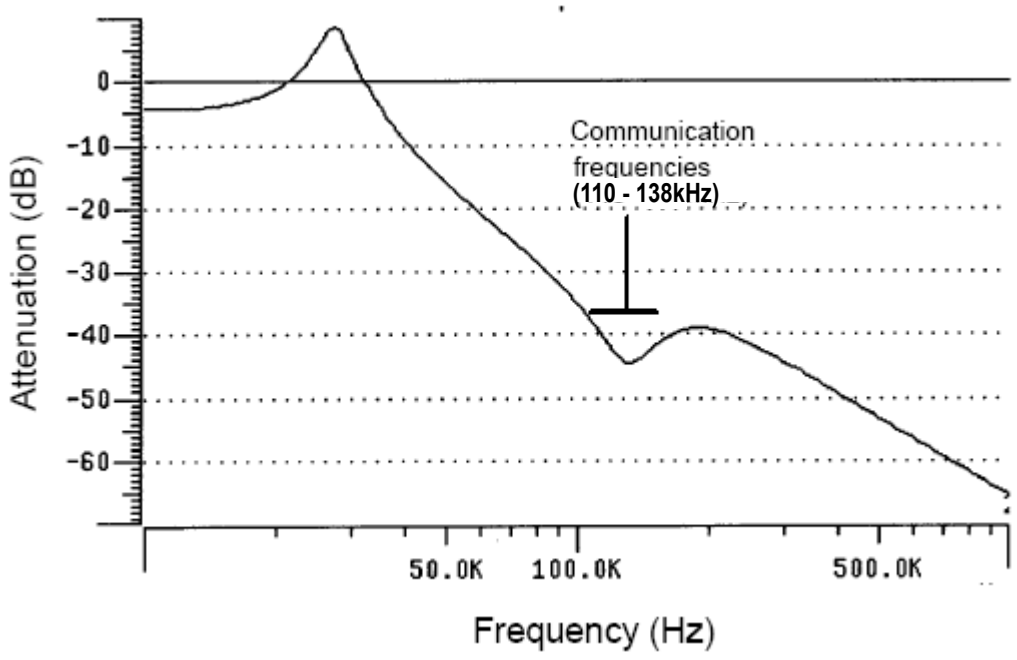


Figure 5.14 C-band Filter Frequency Response

In some instances it is possible that noise radiated from either the power supply or the supply filter can couple into the inductors of the coupling circuit of the PL Smart Transceiver. The coupling circuit can then couple this noise onto the power mains. This problem can be diagnosed by disconnecting the transceiver's coupling circuit and then analyzing the conducted line noise.

If noise from parasitic coupling is suspected, it can be confirmed by inserting a 10cm (4 inch) twisted wire pair in series with one of the inductors in question. If the conducted noise spectrum varies by more than a few dB when this inductor is moved closer to, and farther from, other components, then parasitic coupling might be the source of the problem.

There is a second, although less likely, potential cause for reduced filter effectiveness. It is possible for the inductive reactance of the filter components to be canceled by capacitive reactance from the input of the power supply. This problem is generally seen as narrow band noise which appears to pass through the filter unattenuated. This problem can be remedied by either damping the unintended resonance, or by adjusting the values of the filter inductor and capacitor to move the resonance to a non-interfering frequency. Damping can be accomplished by adding resistance in the range of 200 ohms to 5k ohms in parallel with the filter inductor closest to the power supply.

Switching Power Supply Output Noise Masks

Products incorporating a PL Smart Transceiver require a power supply with a 5V output (V_{DD5}) and a second higher output voltage (V_A, nominally 12V). The amplitude of the noise and ripple on these power supply outputs must be controlled in order to comply with CENELEC EN 50065-1 or FCC-conducted emission limits, as well as to achieve maximum communication performance. Noise “masks” are provided in Figures 5.16 and 5.17. Figure 5.16 shows the recommended noise (ripple) limits on the V_A and V_{DD5} supplies for A-band as does Figure 5.17 for C-band. In each band the same limit lines are used to comply with both CENELEC EN50065-1 and FCC conducted emissions.

Meeting this criteria ensures that full performance of both operating frequencies is available to overcome unexpected power line noise in either of the two frequency ranges.

Measurements should be made over the full range of anticipated loads on the supply, because many switching supplies vary their switching frequency with load. For all CENELEC EN 50065-1 and FCC power supply measurements a peak detector should be used. The measurement bandwidth for V_A should be 3kHz. For V_{DD5} the two separate measurements must be made each a using different measurement bandwidth and each having a separate noise mask. The measurements made using the 3kHz filter should be done at all frequencies while the measurements made using the $\leq$300Hz filter should only be done at frequencies in the 70-90kHz range for A-band and only frequencies in the 110-138kHz range for C-band. The video (post detection) bandwidth for all power supply output noise measurements should be 10Hz.

Figure 5.15 shows a probe that can be used to measure the noise on the power supplies. The twisted wires must be connected directly to the PL Smart Transceiver power and ground pins, and the coaxial cable must be connected to the 50Ω measuring equipment. Note that the 1/10 gain of the probe must be taken into account.

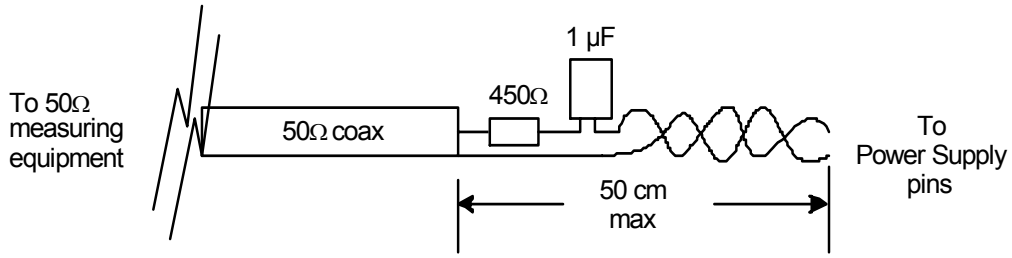


Figure 5.15 10X Power Supply Noise Probe

If the noise masks for either the V_A or V_{DD5} power supplies are not met, then additional filtering must be added to the offending supply in order to bring it into compliance. In the event that extra filtering is needed an inductor of about 10µH can be added in series with the supply line. When combined with a bulk bypass capacitor of >10µF (on the PL Smart Transceiver side of the inductor) the LC combination will provide >20dB of attenuation at communication frequencies. An alternate way to provide a low noise V_{DD5} supply is to use a dedicated 5V linear regulator to feed the PL Smart Transceiver circuitry. In this way noise from other devices on the PCB will be isolated from the V_{DD5} supply line of the PL Smart Transceiver. If the a switching power supply is used which meets the recommended operating frequencies of Table 5.5 then additional V_A and V_{DD5} filtering will typically not be required.

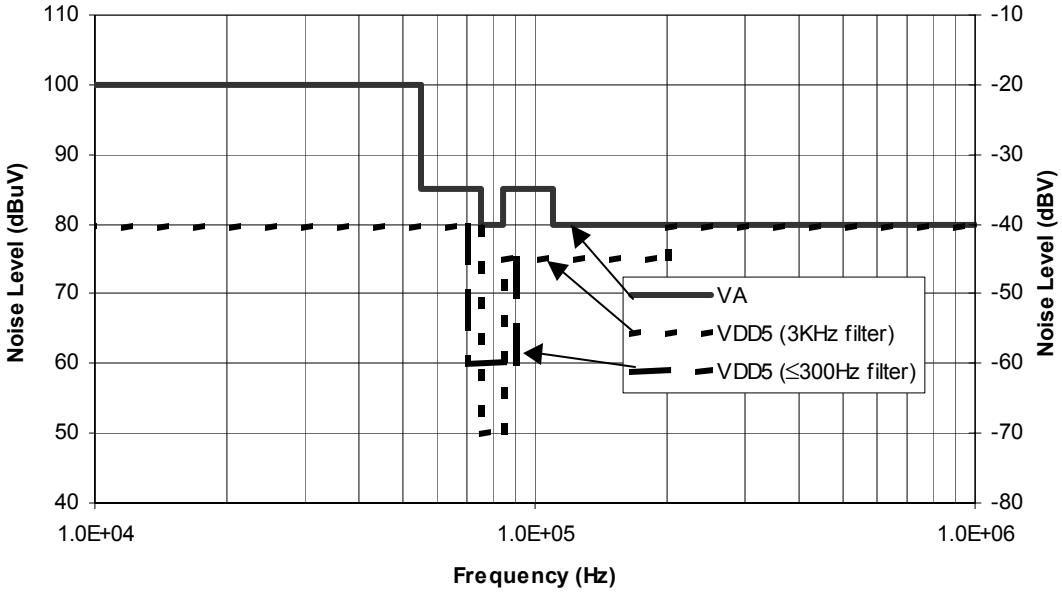


Figure 5.16 V_A and V_{DD5} Power Supply Output Noise Limits for A-band

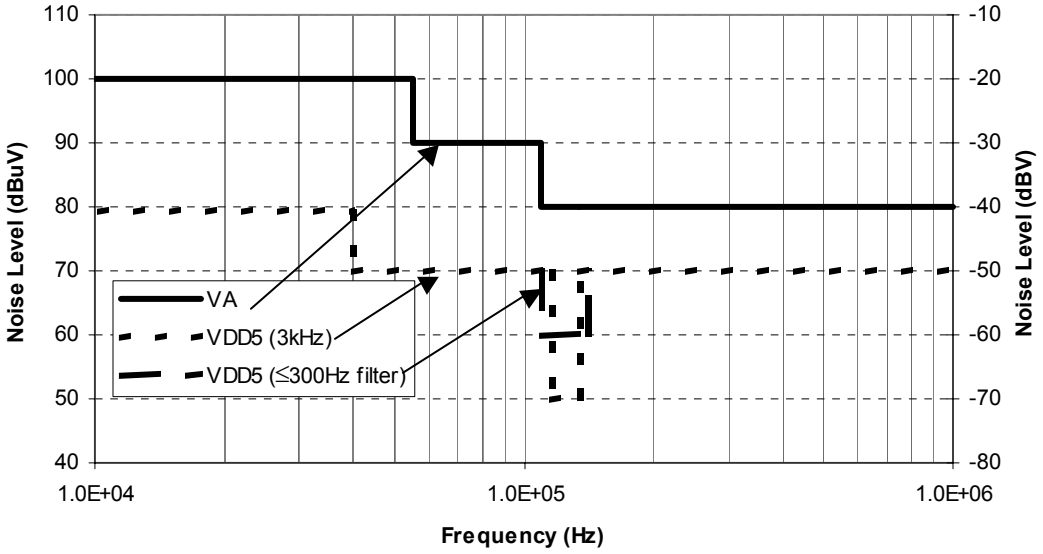


Figure 5.17 V_A and V_{DD5} Power Supply Output Noise Limits for C-band

Tables 5.10 and 5.11 list the levels shown in Figures 5.16 and 5.17 respectively.

Table 5.10 V_A and V_{DD5} Power Supply Output Noise Limits for A-band

Frequency (kHz)	V_A Noise Level (3kHz filter) (dBV)	V_{DD5} Noise Level (dBV)	Frequency (kHz)	V_{DD5} Noise Level (300 Hz filter) (dBuV)
10-55	-20	-40		
55-75	-35	-40		
75-85	-40	-70	70-90	-60
85-110	-35	-45		
110-200	-40	-45		
200-1000	-40	-40		

Table 5.11 V_A and V_{DD5} Power Supply Output Noise Limits for C-band

Frequency (kHz)	V_A Noise Level (3kHz filter) (dBV)	V_{DD5} Noise Level (dBV)	Frequency (kHz)	V_{DD5} Noise Level (300 Hz filter) (dBuV)
10-40	-20	-40		
40-55	-20	-50		
55-110	-30	-50		
110-115	-40	-50		
115-135	-40	-70	110-138	-60
135-1000	-40	-50		

Options for Switching Power Supplies

The following switching power supply options are currently available and are discussed below:

- Pre-designed Energy Storage Switching Supplies
- Pre-designed Switching Supplies
- Off-the-shelf Switching Supplies
- Custom Switching Supplies

Pre-designed Energy Storage Switching Supplies

Bias Power LLC has developed a small (26.0 x 22.6mm), switching power supply module that has been tested for compatibility with the PL 3120 Smart Transceiver. This power supply option is a good choice when the benefits of a switching supply (small size, universal input, safety isolation, and good efficiency) are needed but simplicity of design is also a priority.

The Bias Power LLC BPS 1-14-00 power supply module provides approximately 1 watt of output power at 14VDC. It must be operated as an energy storage supply by the addition of an output energy storage capacitor. Figure 5.18 illustrates the required application schematic for use of the BPS 1-14-00 module with the PL 3120 Smart Transceiver. Note that a simple RC circuit has also been added to the input of the Bias Power module in order to avoid any degradation of power line communication signals due to excessive noise or loading. Note also that because this is an

energy storage design the power management feature of the PL 3120 Smart Transceiver must be enabled as described in Chapter 8.

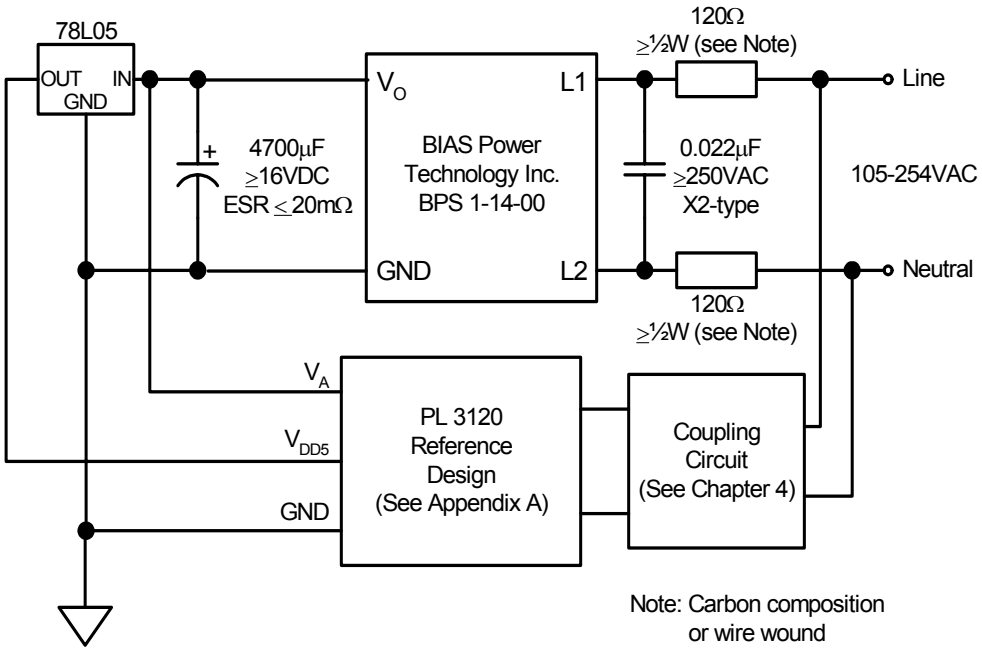


Figure 5.18 Pre-designed Energy Storage Switching Supply Schematic

The circuit in Figure 5.18 supports the power requirements of the PL 3120 Smart Transceiver in conjunction with 10mA of application current. The design has been verified to meet the energy storage power supply requirements described earlier in this chapter. Specifically, it provides ≥10.8V after a transient load of 120mA for 140.7ms has been added to a 19mA static load (9mA PL 3120 typical I_{DD5} + 10mA application current) under conditions of nominal AC line voltage and room temperature. In addition it has been verified to provide ≥8.5V after a 250mA load has been added for 140.7ms to a 23mA static load (13mA PL 3120 maximum I_{DD5} + 10mA application current) with 105VAC line voltage, -20% output capacitor tolerance and either 0C or 70C ambient temperatures. It supports typical transmit duty cycles of >65% and worst case transmit duty cycles of ≥30%.

This combination of Bias Power BPS 1-14-00 module and Echelon PL 3120 Smart Transceiver has been verified to pass all of the communication performance tests described in Chapter 7. In addition, a sample of the BPS 1-14-00 used with the application schematic of Figure 5.18, has been verified to pass EN50065-1 and FCC regulations for conducted emissions. The user of this circuit must perform their regulatory qualification of their own particular circuit layout, but this design has been found to be relatively insensitive to layout variations. The user must also verify communication performance as described in Chapter 7 in order to validate that the particular layout implementation still satisfies the requirements of that chapter.

Further information regarding the Bias Power BPS 1-14-00 module contact:

Bias Power LLC
330 West Colfax Street
Palatine, IL 60067 USA
Phone: 847-358-1259
Fax: 847-358-1346
www.biaspower.com

Pre-designed Switching Supplies

This power supply option is a good choice when significant application current, small size, universal input, safety isolation and/or good efficiency are needed. Echelon has developed this power supply to specifically meet the noise and impedance requirements of the PL 3120 and PL 3150 Smart transceivers. The design is based on the STMicroelectronics VIPer®20A off-line switch-mode power supply IC.

This pre-designed power supply provides a total output current of 363mA at 12V. It thus supports 100mA of application and I/O current after allowing for 250mA of the worst case V_A current and 13mA of worst case V_{DD5} current of a PL 3120 reference design from Appendix A. The specifications for this supply are listed in Table 5.12, the application schematic is provided in Figure 5.19, and the bill of material (BOM) is provided in Table 5.13.

Table 5.12 Pre-designed switch supply specifications

Parameter	Min	Typ	Max	Units
Input voltage	90	230	254	VAC
V_A output voltage	10.8	12.4	14.0	VDC
V_{DD5} output voltage	4.75	5.0	5.25	VDC
Output load current (V_A+V_{DD5})	10	150	363	mA
Switching frequency	46	51	55	kHz
Ambient operating temperature	-40	25	85	C

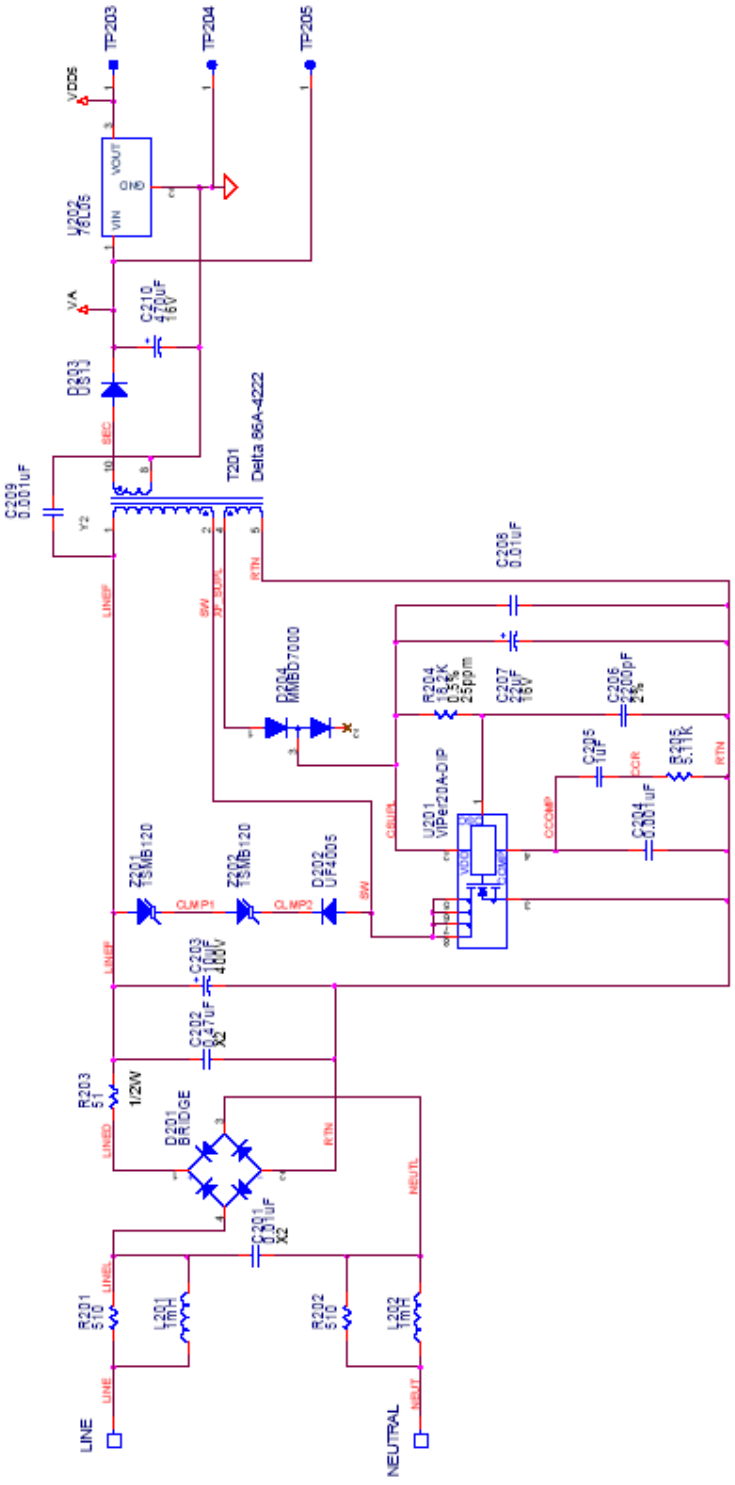


Figure 5.19 Pre-designed switching supply schematic

Table 5.13 Pre-designed switch supply bill of materials (BOM)

Component	Value	Required Specifications	Example Vendor/Part #
R201, R202	510Ω	±5%, ≥1/4W, overload voltage ≥500V	Generic
R203	51Ω	±5%, ≥1/2W, carbon composition or wire-wound	Xicon/30BJ500-51
R204	18.2kΩ	±0.5%, ≥1/16W, ≤25ppm/C, 0603	Susumu/RR0816P-1822-D
R205	5.11kΩ	±1%, ≥1/16W, 0603	Generic
C201	0.01uF	±20%, ≥250VAC, class X2	Panasonic/ECQ-U2A103ML
C202	0.47µF	±20%, ≥250VAC, class X2	Panasonic/ECQ-U2A474ML
C203	10µF	±20%, ≥400VDC, aluminum electrolytic	Nichicon/UPW2G100MHD
C204	0.001µF	±10%, ≥25VDC, X7R, 0603	generic
C205	1/0µF	±10%, ≥10VDC, X7R, 0805	Kemet/C0805C105K8RAC
C206	2200pF	±2%, ≥25VDC, NPO, 0603	Generic
C207	22µF	±20%, ≥16VDC, tantalum, EIA size B	Kemet/T491B226M016AS
C208	0.01µF	±10%, ≥25VDC, X7R, 0603	Generic
C209	0.001µF	±20%, ≥250VAC, class Y2	Vishay/WYO102MCMBF0K
C210	470µF	±20%, ≥16VDC, aluminum electrolytic, ≤0.1Ω ESR @100kHz/25C, ≥290mA_{RMS} ripple current @105C	Nichicon/UHE1C471MED
D201	0.8A	V_R ≥600VDC, bridge rectifier	Shindengen/S1ZB60
D202	1A	V_R ≥600VDC, V_F ≤1.7V@1A/25C, reverse recovery ≤25ns	Generic/UF4005
D203	1A	V_R ≥50VDC, V_{Fmax}=1.7V@1A/25C, reverse recovery ≤75ns, SMA	Generic/US1J
D204	Dual Diode	Reverse breakdown ≥100VDC, I_F ≥100mA, 550 ≤1V_F≤700mVA1mA, trr≤4ns, SOT-23	Generic/MMBD7000
Z201, Z202	120V	600 watt peak power, zener transient voltage suppressor, SMB	ON Semi/1SMB120AT3
L201, L202	1.0mH	±10%, Imax ≥250mA	Taiyo Yuden//LHL08TB102J or CTC Coils Limited/CH Series
T201	Transformer	Delta 86A-4222 isolation transformer	Delta/86A-4222A
U201	VIPer20A	VIPer20A off-line switch-mode power supply IC, DIP-8	ST Microelectronics/VIPer20A
U202	5V regulatator	LM78L05 or equivalent, SOT-89	Generic/LM78L05

The only custom part for this design is transformer T201 which can be obtained by contacting:

Delta Electronics Inc.
Telephone: +1-886-3-3591968 Extension 2228
FAX: +1-886-3-3591991
www.delta.com.tw1

The performance of this power supply is somewhat sensitive to layout. Minimizing the length of the net from the Drain of the VIPer20A IC is of particular importance in controlling conducted emissions. In order to reduce the development time required to successfully implement this supply, a recommended layout is provided in figure 5.20.

Building this pre-designed power supply as documented here greatly simplifies the task of developing a switching supply-based Smart Transceiver device. This is because an instance of this design has been verified to meet all of the impedance and noise requirements described elsewhere in this chapter.

Furthermore, testing of this supply has also been conducted in combination with PL 3120 Smart Transceiver reference design #1217 from Appendix A and the isolated Line-to-Neutral coupling circuit Example #2 from Chapter 4. This combination passed EN50065-1 and FCC regulations for conducted emissions with 8dB of margin and was also verified to pass all of the communication performance tests of Chapter 7. In addition, this supply in combination with coupling circuit Example #2 passed the surge tests documented for that circuit in Table 4.14 on page 151.

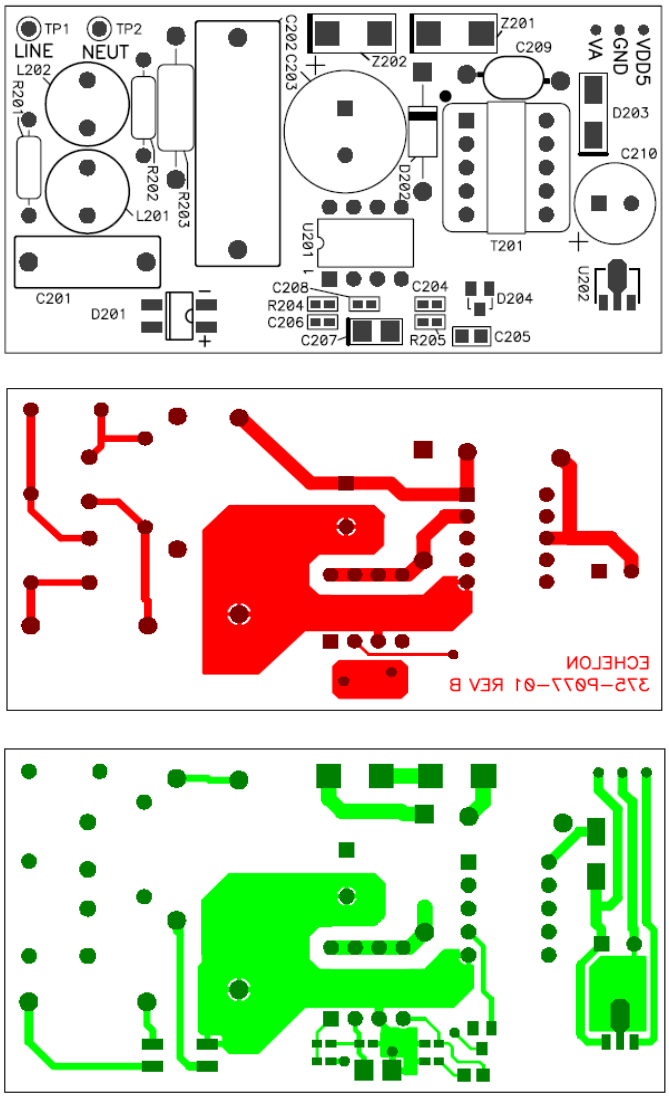


Figure 5.20 Recommeded layout of the pre-designed switching supply

Off-the-Shelf Switching Supplies

Most commercially available switching power supplies have been designed with some level of input noise filtering. Frequently this level of filtering is adequate if the supply's fundamental switching frequency is within the recommended ranges of Table 5.5 over all operating conditions and tolerances. Supplies with other fundamental operating frequencies might be able to meet the required noise masks of the previous sections with greater effort and/or cost; however, meeting the noise mask requirements with a power supply fundamental frequency (or second or third harmonic) in the 70kHz to 90kHz or 110kHz to 138kHz range is **very challenging and not recommended**.

Most off-the-shelf switching supplies have a very low input impedance and require the addition of an input inductor as shown in Figures 5.6 and 5.7.

Full Custom Switching Supplies

Design of a custom switching supply, even one which employs a commercially available controller chip, is **very** challenging and is only recommended if none of the other options outlined in this chapter are suitable. If this option is chosen, it is recommended that it only be pursued by experienced switching supply and electromagnetic compatibility experts. Even if such personnel are available, extra time must be allowed for design iterations during development. If this approach is chosen, it is absolutely essential that the supply is verified to meet the input and output noise masks of this chapter.

Many of the off-line switching regulators available from Power Integrations Inc. (for example, LinkSwitch® and TinySwitch® regulators) operate at frequencies which are not within the recommended range for use with the PL Smart Transceivers and are not recommended for use with PL Smart Transmitters. The TopSwitch® family of off-line switching regulators from Power Integrations operate within the recommended range of frequencies at room temperature but they do not stay within the recommended range over temperature. TopSwitch® regulators are therefore no longer recommended for powering PL Smart Transceiver-based devices.

Most 1st and 2nd generation SIMPLE SWITCHER® regulators from National Semiconductor Corporation operate at frequencies which are not within the recommended range for use with the PL Smart Transceivers (that is, most LM25xx parts). Use of any SIMPLE SWITCHER regulator with a nominal operating frequency of 52kHz, 100kHz or 150kHz is not recommended because these devices have a very wide frequency tolerance which could result in operation outside the recommend range.

Newer SIMPLE SWITCHER regulators (for example, 3rd generation LM26xx parts) with operating frequencies of ≥200kHz can be used, providing that the design has been verified to meet the noise mask requirements of this chapter over all operating conditions.

6

Design and Test for Electromagnetic Compatibility

Introduction

This chapter includes discussions of conducted and radiated electromagnetic interference (EMI) and electrostatic discharge (ESD) design practices for products containing the PL 3130 and 3150 Smart Transceivers. These design practices help the designer to create a product with the required Electromagnetic Compatibility (EMC).

EMI Design Issues

The high-speed digital signals associated with micro controller designs can generate unintentional electromagnetic interference (EMI). High-speed voltage transitions generate RF currents that can radiate from a product.

Products that use a PL Smart Transceiver will generally need to demonstrate compliance with EMI limits enforced by various regulatory agencies. In the USA, the FCC[6] requires that unintentional radiators comply with Part 15 level “A” for industrial products, and level “B” for consumer and household products. Most European countries require compliance to CENELEC EN 50065-1. Similar regulations are imposed in most countries throughout the world.

In addition to the following discussion, designers of PL Smart Transceiver-based devices are encouraged to read reference appendix entry [9] for a good treatment of EMC. The *EDN Designer's Guide to EMC*[10] is also a good source of design advice regarding EMC issues.

Designing Systems for Electromagnetic Compatibility (EMC)

Careful PCB layout is important to ensure that a PL Smart Transceiver-based device will achieve the desired level of EMC. Digital signal lines on a PL 3120/PL 3150-based device can generate both voltage noise near the signal traces, and current noise in the signal and power supply traces. The goal of good device design is to keep voltage and current noise from coupling out of the product enclosure.

It is very important to minimize the “leakage” capacitance from circuit traces in the node to any external metal near the node because this capacitance provides a path for the digital noise to couple out of the product enclosure. Figure 6.1 shows the leakage capacitances to earth ground from a node's logic ground ($C_{leak,GND}$) and from a digital signal line in the node ($C_{leak,SIGNAL}$). If the PL Smart Transceiver-based device is housed inside a metal chassis, then that metal chassis will probably have the largest leakage capacitance to other nearby pieces of metal. If the device is housed inside a plastic package, then PCB ground guarding must be used to minimize $C_{leak,SIGNAL}$. Effective guarding of digital traces with logic ground reduces $C_{leak,SIGNAL}$ significantly, which in turn reduces the level of common-mode RF currents driven onto the AC mains.

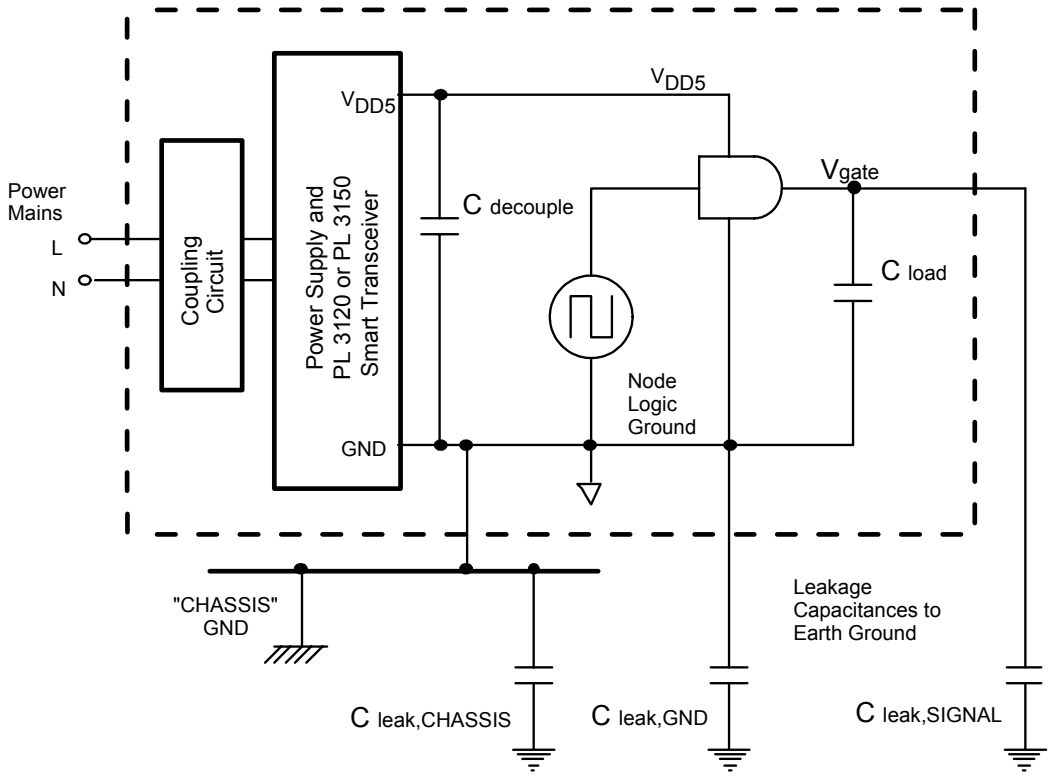


Figure 6.1 Parasitic Leakage Capacitances to Earth Ground

When a device is mounted near a piece of metal, especially metal that is earth grounded, any leakage capacitance from fast signal lines to that metal will provide a path for RF currents to flow. When V_{gate} is pulled down to logic ground, the voltage of logic ground with respect to earth ground will increase slightly. When V_{gate} pulls up to V_{DD5}, logic ground will be pushed down slightly with respect to earth ground. As $C_{leak,SIGNAL}$ increases, a larger current flows during V_{gate} transitions, generating more common-mode RF current. This common-mode RF current can generate EMI in the 500kHz-300MHz frequency band, potentially exceeding FCC/CENELEC conducted and radiated limits, even when $C_{leak,SIGNAL}$ from a clock line to earth ground is less than 1pF. This means that it is essential to guard the clock lines.

From this discussion, it is apparent that minimizing $C_{leak,SIGNAL}$ is very important. By using 0.1µF or 0.01µF decoupling capacitors at each digital IC power pin, V_{DD5} and logic ground noise can be reduced. Logic ground can then be used as a ground shield for other noisy digital signals and clock lines.

Because the PL 3150 Smart Transceiver IC has an external memory interface bus, there are more traces in a device using a PL 3150 Smart Transceiver that need to be guarded by logic ground than there are in a PL 3120-based device. Noise generated by the memory interface and external memory components requires more V_{DD5} decoupling, and generally requires a four-layer PCB to maintain RF-quiet V_{DD5} and logic ground lines.

In summary, the following general observations apply:

- Better V_{DD5} decoupling quiets RF noise at the sources (the digital ICs), which lowers EMI

- A four-layer PCB generates less EMI than a two-layer PCB because the extra layers facilitate better V_{DD5} decoupling and more effective logic ground guarding
- A four-layer PCB is recommended for use with the PL 3150 Smart Transceiver
- The PL 3120 Smart Transceiver generates less EMI than the PL 3150 Smart Transceiver because the PL 3120 Smart Transceiver has no external memory interface lines
- A two-layer PL 3120 Smart Transceiver-based device can meet FCC/CENELEC EMC if good decoupling and ground guarding are used

Early testing of prototype circuits at an EMI range should be used to determine the effectiveness of these EMC techniques.

ESD Design Issues

Electrostatic discharge (ESD) is encountered frequently in industrial and commercial use of electronic systems [11]. In addition, the European Community has adopted requirements for ESD testing in product qualifications analogous to the EMI requirements [4] under the EMC directive.

Reliable system designs must consider the effects of ESD and take steps to protect sensitive components. Static discharges occur frequently in low-humidity environments when operators touch electronic equipment. Keyboards, connectors, and enclosures can provide paths for static discharges to reach ESD sensitive components such as the PL Smart Transceiver. This section describes the issues involved in designing ESD immunity into PL Smart Transceiver-based products.

In addition to the following discussion, designers of PL Smart Transceiver-based devices are strongly encouraged to read in the references appendix entries [10] and [11]. The *EDN Designer's Guide to EMC*[10] is especially helpful in understanding the importance of managing ESD return currents.

Designing Systems for ESD Immunity

There are two general methods that are used to protect products from ESD. The first is to seal the product to prevent static discharges from reaching the sensitive circuits inside the package. The second method involves grounding circuits so that ESD hits to user-accessible metal parts can be shunted around any sensitive circuitry.

The product's package should be designed to minimize the possibility of ESD hits arcing into the device’s circuit board. If the product's package is plastic, then the PCB should be supported in the package so that unprotected circuitry on the PCB is not adjacent to any seams in the package. The PCB should not touch the plastic of an enclosure near a seam, because a static discharge can “creep” along the surface of the plastic through the seam and arc onto the PCB.

Once an ESD hit has arced to the product, the current from the discharge will flow through all possible paths back to earth ground. Proper use of ground traces combined with the protection of user-accessible circuitry will permit ESD return currents to flow back to earth ground without disrupting the normal operation of the PL Smart Transceiver or other device circuitry. Generally, this means that the ESD currents should be shunted around the PL Smart Transceiver and then out to a chassis or earth ground connection or back to the AC mains connections for a device that does not have an earth ground connection. The shunt path should be arranged such that the current doesn't pass through, or close to, the PL Smart Transceiver or other sensitive components. If the device is floating with respect to earth ground, then the ESD current will return capacitively to earth via the power supply wires and/or the PCB ground plane.

User accessible circuitry requires explicit diode clamping to shunt ESD currents from that circuitry to earth ground using a path that will not disturb sensitive circuitry. For example, if the Neuron core of a PL Smart Transceiver is

scanning a keypad using I/O lines, then the I/O lines to that keypad will need to be diode-clamped as shown in Figure 6.2. If a negative ESD hit discharges into the keypad, the diode clamps to ground shunt the ESD current into the ground plane. If a positive ESD hit discharges into the keypad, the V_{DD5} diodes shunt the current to the ground plane via a 0.1µF decoupling capacitor that is placed directly adjacent to the clamp diodes. The keypad connector, diodes and decoupling capacitor should all be located so that ESD current does not pass through sensitive circuitry as it exits from the PCB.

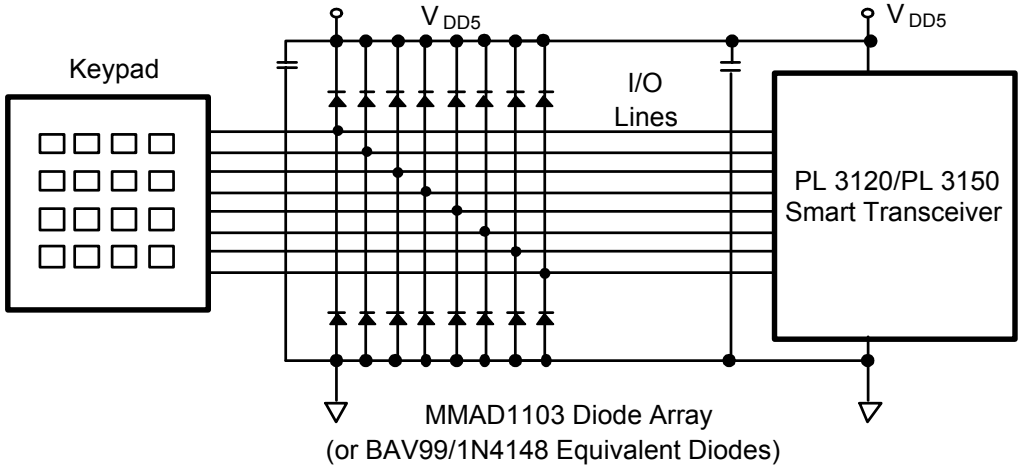


Figure 6.2 Illustration of I/O Line ESD Clamps

Conducted Emissions Testing

The PL Smart Transceiver is designed to comply with both FCC Section 15.107 “Limits for carrier current systems” [1] and CENELEC EN 50065-1 “Signaling on low-voltage electrical installations in the frequency range 3kHz to 148.5kHz” Part 1 “General requirements, frequency bands and electromagnetic disturbances” [2].

Many commercial testing laboratories lack experience measuring conducted emissions of intentional power line communicators, and commonly-applied testing procedures will give erroneous measurement results. Proper measurement of conducted emissions to verify compliance with FCC and CENELEC EN 50065-1 requires strict adherence to the following guidelines.

- Connect the product under test to the correct network for measurement. For both FCC and CENELEC EN 50065-1 measurements, use the 50Ω//(50µH+5Ω) Line Impedance Stabilization Network (LISN) as specified in CISPR Publication 16 [3], second edition.
- Care must be taken to ensure that the transmit signal of the PL Smart Transceiver does not overload the measurement apparatus. Typically, an attenuator must be installed at the input to the measuring receiver, i.e., spectrum analyzer, to avoid erroneous results due to instrumentation overload. A test for determining whether or not the results are being distorted due to overload is as follows: measure the emissions, then increase the attenuation between the product under test and the measuring receiver, and then re-measure emissions. There is an overload problem if the level of emissions at frequencies other than the main carrier has decreased by more than the increase in attenuation. Most spectrum analyzers have a built-in input attenuator. If this is the case, the attenuator setting is usually taken into account by the instrument. Consequently, the reported levels should not change when the spectrum analyzer input attenuation is changed. There is an overload problem if a level change is reported at frequencies other than the main carrier frequency.

- Care must be taken to ensure that the residual noise floor of the entire measurement set remains at least 10dB below the specification limit once the appropriate attenuator is installed. This is important because the process of adding attenuation to avoid instrumentation overload reduces the signal-to-noise ratio of the measurement. That is, a noise floor less than 38dBµV for FCC measurements, and a noise floor less than 36dBµV for CENELEC EN 50065-1 measurements.
- The measurements must be made with the specified detector. For both FCC and CENELEC EN 50065-1 measurements, use the quasi-peak detector and the average detector as specified in CISPR Publication 16. Although a scan with a peak detector is common because it can be performed quickly, the limits specified by FCC Section 15.107 and by CENELEC EN 50065-1 are for quasi-peak and average detectors only. For power line transceivers, peak measurements often appear erroneously high relative to the quasi-peak limits.
- The measurements must be made with the specified filter. For FCC measurements, a 9kHz bandwidth filter is specified. For CENELEC EN 50065-1 measurements, a 200Hz bandwidth filter is specified for measurements below 150kHz, and a 9kHz bandwidth filter is specified above 150kHz.
- For FCC measurements, an input filter which meets the requirements of CISPR 16 is suitable. The CENELEC EN 50065-1 specification requires that the filter inside the measuring receiver have even steeper filter skirts than the minimum required by CISPR 16.

CENELEC EN 50065-1 specifies a 9kHz filter for measurements above 150kHz. For C-band operation, the allowable transmit level is +122dBµV between 95kHz and 140kHz (+134dBµV in some applications). The CENELEC EN 50065-1 specification limit is +66dBµV quasi-peak at 150kHz. To make a proper measurement, the filter inside the measuring receiver must have filter skirts providing at least 64dB of attenuation 15kHz from its center (122dBµV - 66dBµV + 8dB margin).

The CENELEC EN 50065-1 sub-committee SC 105A (Mains Communicating Systems) recognized the need for a filter with steeper skirts than the minimum specified by CISPR Publication 16. As stated in the final draft of an amendment to
EN 50065-1 dated January, 1994, “the measuring instrument defined by the minimum requirements of CISPR 16 is unsuitable for the measurement of mains signaling equipment that uses a signaling frequency not far below 150kHz,” and the sub-committee SC 105A agreed that “the proper solution would be to specify the attenuation characteristic of the measuring receiver more closely, receivers being known to be available on the market.” EN 50065-1:2002 Annex E specifies a filter that still complies with CISPR 16 but which has steeper filter skirts. Many spectrum analyzers, even very expensive ones, do **not** meet this requirement [2].

The Rohde&Schwarz EMI Test Receiver ESHS30 has been found to have adequate filter skirts. Although its specification does not *guarantee* adequate filter skirts, two samples of the ESHS30 test receiver have been found to make the measurement reliably.

In addition, care must be taken in setting up the Rohde&Schwarz EMI Test Receiver ESHS30. The “automatic” mode for setting input attenuation selects an incorrect attenuation level that will result in an overload condition, which is not properly reported by the overload indicator on the Test Receiver. The proper attenuation must be selected using manual mode. A set-up program to accurately run scans for CENELEC EN 50065-1 compliance testing on the Rohde&Schwarz EMI Test Receiver ESHS30 is available from Echelon's LONWORKS Developer's Toolbox at www.echelon.com/downloads in the “OEM Components” download area.

An application note from Hewlett-Packard [12] describes a test method for performing EN 50065-1 conducted emissions tests using Hewlett-Packard EMI test receivers. The title of the application note is “Conducted Emissions Measurements on Power Line Transceiver Products.” This application note describes an “off-the-shelf” external filter and a methodology that allows the measurements specified in EN 50065-1 to be performed accurately.

If the unit under test is found to exceed the applicable conducted noise limit at frequencies above 500kHz, it might be the result of unintentional coupling of noise from the node's various digital circuits. If this occurs, improvements in

grounding and printed circuit layout are generally required. Refer to Chapter 4 for a discussion of how to avoid stray field pickup by coupling circuits.

In some instances conducted emissions above 500kHz can be adequately reduced by the addition of a **small** value capacitor (e.g., 470pF) either across the AC mains or from the line conductor to ground. While devices using the PL Smart Transceiver have been demonstrated to pass various limits without an additional capacitor, variations in node design and layout might require the addition of this small value capacitor. If a capacitor is added across the line it should be an X2 safety-rated type for maximum surge reliability. If capacitors are added from either line or neutral to earth, they should be Y safety rated. Alternately, this capacitor can be added across coupling circuit inductor L101 (see Figure 4.17) or across the line-side winding of transformer T101 (see Figure 4.18). If this option is chosen, either a metallized polyester capacitor of ≥250VDC, a ceramic 1000VDC capacitor, or a Y-type capacitor should be used for surge reliability. Note that this extra capacitance should only be added to the line side of the coupling transformer and not to the transceiver side of the transformer.

Adding capacitance in the above locations reduces the input impedance of the device and could therefore cause an increase in communication signal attenuation. The maximum value of capacitance which can be added without significantly affecting attenuation depends on the application. Table 6.1 shows the maximum value of added capacitance by application. **Under no circumstances should capacitors >4700pF be used because they will result in excessive signal attenuation.**

Table 6.1 EMC Suppression Capacitor Value vs. Application

Application	Network Impedance at Communication Frequencies	Capacitor Impedance at Primary Communication Frequencies	A-band Capacitor Value	C-band Capacitor Value
Single building AC mains	1-20 ohms	≥250 ohms	≤4700pF	≤4700pF
Inter-building mains distribution	1 - 50 ohms	≥500 ohms	≤3600pF	≤2200pF
Dedicated cable ≥100 devices ≥100m	50 - 100 ohms	≥1000 ohms	≤1800pF	≤1200pF
Dedicated cable >100 devices >100m	50 - 100 ohms	≥2500 ohms	≤680pF	≤470pF

Another common method of EMC suppression, the addition of ferrite beads, is generally unacceptable if they are placed anywhere in the transmit signal path. Most ferrite beads have several ohms of impedance at 100kHz. The impedance of any element placed in series with the transmit signal or return path must be significantly less than 1 ohm as described in chapter 4. There is, however, one means whereby a ferrite bead can be used to reduce common mode high frequency emissions without affecting the transmit signal. If both the communication signal and its return conductor (i.e., Line and Neutral for L-to-N coupling or Line and Earth for L-to-E coupling) pass through the same bead in a common-mode fashion, the bead will not add any series impedance to the transmitter. This is true because the signal currents in the two conductors produce opposite polarity (canceling) flux in the ferrite bead's core. Common mode noise of equal polarity on both conductors will produce additive flux in the ferrite bead's core and will thus be attenuated. Figure 6.3 illustrates both acceptable and unacceptable topologies for high-impedance ferrite beads.

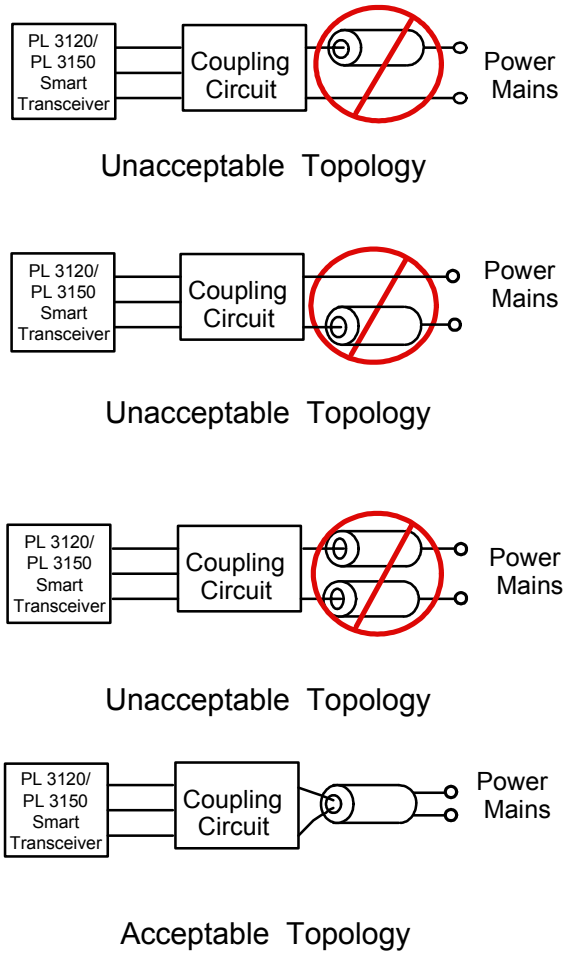


Figure 6.3 High-Impedance Ferrite Bead Topologies

7

Communication Performance Verification

Introduction

This chapter describes a simple “black box” testing methodology for determining whether or not the communication performance of a PL Smart Transceiver-based product has been compromised. This procedure works equally well for products employing L-N or L-E coupling.

Before starting the verification process it is essential that the checklist in Appendix B be completed in its entirety.

Reasons for Verifying Communication Performance

While each PL Smart Transceiver is thoroughly tested prior to shipment, circuitry external to the transceiver could compromise the communication performance of the device in which the transceiver is used. Ways in which communication performance could be compromised include mis-loaded components, inadequately filtered switching power supplies, circuitry improperly added between the coupling circuit of the transceiver and the power mains, and deviations from recommended part specifications. Due to the robust communication capability of the PL Smart Transceivers, it might not be obvious that communication performance has been compromised when testing in a nominal environment.

Because compromised performance is generally observable only under “corner-case” conditions, failure to verify performance prior to deployment could result in many marginal units in the field before a problem is detected. It is therefore essential that the communication performance of every PL Smart Transceiver design be verified prior to field deployment. This can be accomplished either by self verification, using the procedures given in this chapter, or by contacting your Echelon sales representative to make arrangements to send the device to Echelon for confidential evaluation.

Verification Procedure

The recommended verification procedure is as follows:

1. Create a controlled power line environment that is isolated from typical power mains noise and loading.
2. Provide known load impedances at the communication frequencies of the PL Smart Transceiver.
3. Use the PLCA-22 Power Line Communications Analyzer (model 58022) as a calibrated reference transmitter and receiver.
4. Test the performance independent of the product's application by making use of the service pin of the Smart Transceiver and internal statistics features. If the product under test does not have a service pin switch then it will need to be added to the product for testing purposes.
5. Test for unintentional noise injection and excessive loading by the product under test. This is to ensure that the device can behave as a “good citizen” on a power line network.
6. Verify that the product's transmit signal level is within acceptable limits. This is done by deliberately loading the isolated power mains on which the product under test is operating and comparing the output transmission level under load against a reference level.
7. Verify that the receive sensitivity of the product is within acceptable limits. This is performed using a pair of PLCA-22 analyzers. The communication signal level of the transmitting PLCA-22 analyzer is gradually decreased and the receive performance of the product under test is monitored and compared against reference performance levels.
8. All test results can be documented using Table 7.1 at the end of this chapter.

Power Line Test Isolator

The circuit shown in Figure 7.1 is used to create a power mains environment that is isolated from the noise and loading present on typical power mains. When properly constructed, the circuit provides 60 to 80dB of isolation between the power mains and the product under test at the communication frequencies of the PL Smart Transceiver. The effectiveness of the circuit should be verified by using a pair of PLCA-22 analyzers communicating between the power mains input and the output. To perform this verification, set the PLCA-22 analyzer that is connected to the input side of the isolator to send packets at 3.5Vpp in **UnackPri** mode in the **C-band**. The green bar graph meter on the receiving analyzer (connected to the "product under test" output) should indicate a signal strength no higher than –60dB. Without any packet transmission, no LEDs above the –78dB primary and secondary signal strength LEDs should be illuminated or flashing. Note that Neon power indicators should not be used on the isolated output, because they frequently produce noise in the –72dB range.

Because the isolator does not completely block communications from other PL 3120/ PL 3150 Smart Transceivers or older PLT-2X transceivers communicating on the power mains, receive testing must only be performed when there is no other packet activity on the power mains.

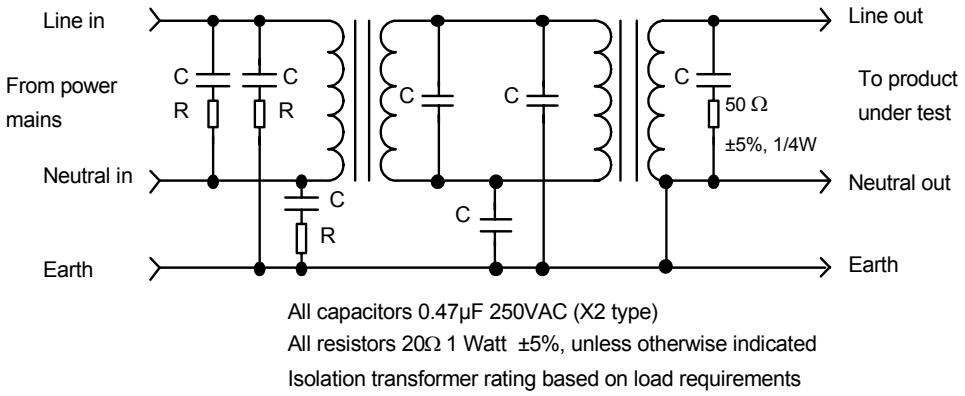


Figure 7.1 Power Mains Isolation Circuit

The transformers shown in the circuit are 50/60 Hz, 1:1 isolation transformers. The load (VA) rating of each transformer should be chosen based on the load requirements of the devices under test. Care should be taken when wiring the isolator to avoid inadvertent signal coupling between the input and output wiring by spacing the input and output wires at least 15cm (6 inches) apart.

Test Equipment

In addition to the power mains isolator described in the previous section, the following "off-the-shelf" equipment will be needed for testing:

- One pair of PLCA-22 Power Line Communications Analyzers (Model 58022). The older PLCA-21 is not suitable.
- Two PL-20 Line-to-Neutral power line couplers, Echelon model 78200-221.
- Two 50Ω coax cables approximately 30cm long with male BNC connectors on both ends (AMP 1-221128-x or equivalent).

- A four (or more) outlet power strip which does not include either surge protection, neon lights, or noise filtering circuitry.
- One Windows 98 or Windows XP-based computer configured with either a PCLTA-20 network interface and PLM-22 SMX transceiver or a PL-SLTA network interface.

Test Equipment to be Constructed

The following additional equipment will need to be constructed for testing:

"5Ω Load" Circuit

This circuit, as shown in Figure 7.2, should be built in a suitable enclosure and provided with an appropriate male AC mains plug. Note that the 1MΩ resistor's stand-off voltage should be greater than or equal to the peak line voltage.

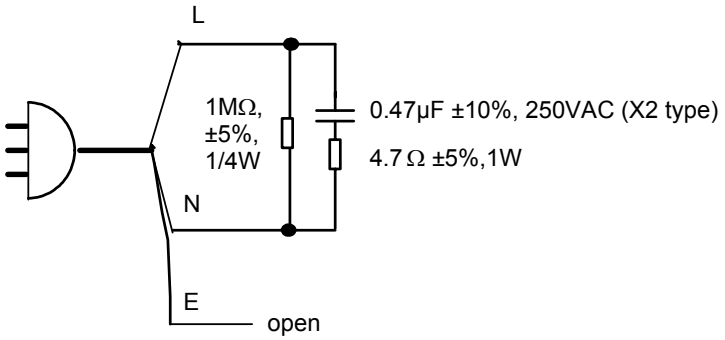


Figure 7.2 "5Ω Load" Circuit

"7Ω Load" Circuit

This circuit, as shown in Figure 7.3, should be built in a suitable enclosure and provided with an appropriate male AC mains plug. Note that the stand-off voltage of the 1MΩ resistor should be greater than or equal to the peak line voltage.

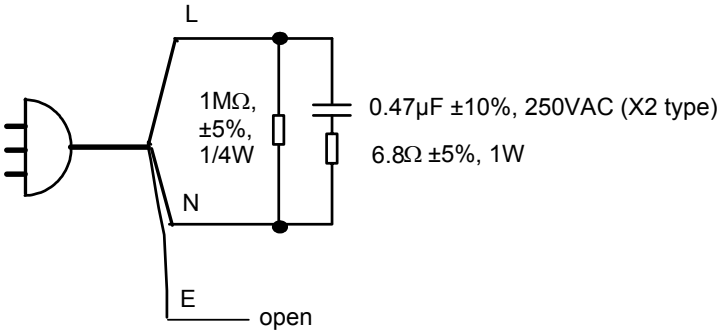


Figure 7.3 "7Ω Load" Circuit

Impedance Circuit

This circuit, as shown in Figure 7.4, should be built in a suitable enclosure with bulkhead BNC jacks (AMP 227755-x or equivalent). This impedance circuit, placed in series with the output path of a PLCA-22 analyzer, effectively increases its output impedance. This will allow for a more sensitive measurement of the receive mode impedance of the product under test.

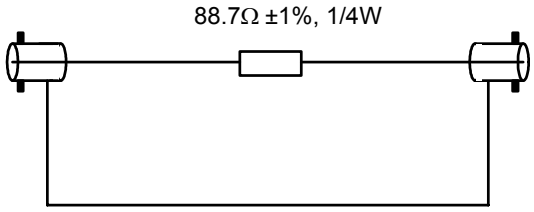


Figure 7.4 Impedance Circuit Used For Excessive Loading Verification

Attenuation Circuit

This circuit, as shown in Figure 7.5, should be built in a suitable enclosure with bulkhead BNC jacks (AMP 227755-x or equivalent). This attenuation circuit, or "pad", will provide approximately 60dB of attenuation when connected into the receive performance verification set-up of Figure 7.9.

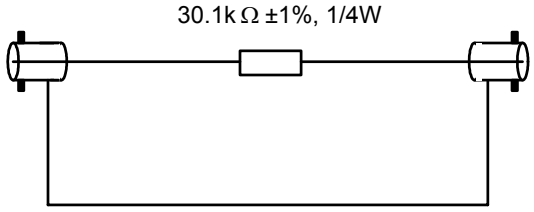


Figure 7.5 Attenuation Circuit Used For Receive Performance Verification

For the receive performance verification, a computer is required to be running **NodeUtil Node Utility** (`nodetuil.exe`). This utility is available on the Echelon Web site at `www.echelon.com/downloads` under **Development Tools**. The **`Node Status`** command is used to obtain a record of the number of uncorrupted packets received by the Unit Under Test (UUT). This set-up is described in detail in the *Packet Error Measurement with NodeUtil* section later in this chapter.

Good Citizen Verification

The following steps are used to verify that the Unit Under Test (UUT) does not inject unwanted noise onto the power mains or excessively load the power mains.

Unintentional Output Noise Verification

The following procedure determines if the UUT is generating unwanted noise which might hinder its communication performance or that of other devices on the power mains.

1. Connect a single PLCA-22 analyzer, the UUT, and the Isolator as shown in Figure 7.6 below. Verify that the analyzer is set for the same band of operation as the UUT (A-band or C-band) by observing the selected band in the upper right-hand corner of the LCD display (if its band setting does not match, then it must be changed using the Setup screen of the analyzer). Leave the PLCA-22 analyzer in idle mode (no packets being transmitted) and set it for Internal and Line-to-Neutral coupling (coupling mode switch to the right).
2. Verify that the UUT application program is not sending messages.
3. Observe the signal strength bar graph LEDs. The -72dB LED should not be on solid and the -66dB LED should not be flashing on either the primary or secondary bar graph meters. In addition, the Packet Detect (PKD) LEDs should not flash any more than once per minute.
4. Record the results from Step 3 in Table 7.1 at the end of this chapter.

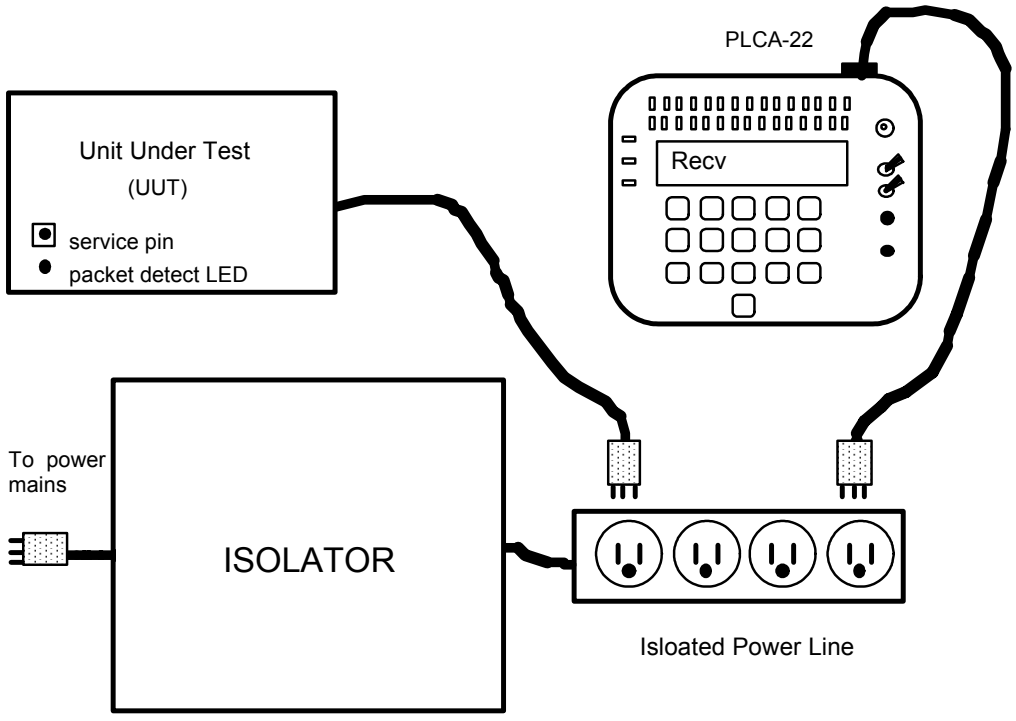


Figure 7.6 Unintentional Output Noise Verification

If either of the -72dB LEDs is on solid or if either of the -66dB LEDs flash or if the PKD LED flashes more than once per minute, then excessive noise or interference is present. This could be caused by one or more of the following sources:

- The UUT is generating unwanted noise internally. This is most often associated with on-board switching power supplies. If the UUT includes a switching power supply, verify that the power supply noise masks of Chapter 5 have been met.
- Power line communications signals present on the power input side of the isolator are not sufficiently attenuated. Ensure that no other power line signaling equipment is operating on the power mains when performing this test.
- The isolator is not completely isolating the test set-up from noise on the power mains. Verify the effectiveness of the isolator as described earlier.

The source of this noise or interference must be identified and eliminated before proceeding with verification testing.

Excessive Loading Verification

The procedure described in this section is used to determine if the receive mode impedance of the UUT is greater than approximately 100Ω at its primary communication frequency (as it should be). A receive mode impedance of less than 100Ω could cause excessive signal attenuation resulting in impaired reception by both the UUT and its neighboring nodes. For applications which require an even higher receive impedance, refer to discussions in Chapters 5 and 6.

The 10Vp-p output capability of the PLCA-22 analyzer is used to increase the sensitivity of the test. The higher output signal allows the 0dB, -3dB, and -6dB LEDs of the PLCA-22 analyzer signal strength meter to be used for observing signal strength. These LEDs, unlike the other LEDs in the signal strength meter, are only 3dB apart allowing for better measurement resolution.

A series impedance circuit (Figure 7.4) in the output path of the transmitting PLCA-22 analyzer is used to increase its effective output impedance, thereby preventing its normally low transmit output impedance from overshadowing the receive mode impedance of the product under test.

The recommended verification procedure is as follows:

1. Set a first PLCA-22 analyzer (referred to as the Recv PLCA-22 analyzer) to use the same band of operation as the UUT. Set it for `Recv` and `UnackPri` modes of operation and configure it for Internal and Line-to-Neutral coupling as shown in
   Figure 7.7.
2. Set a second PLCA-22 analyzer (referred to as the Send PLCA-22 analyzer) for the same band of operation as the UUT. Set it for `Send` and `UnackPri` modes of operation and configure it for External coupling. Connect the impedance circuit (88.7Ω resistor of Figure 7.4) and the coupling circuit as shown in Figure 7.7. This test is best conducted with the CENELEC protocol (an option for C-band operation) turned off in order to provide uninterrupted LED illumination (set on the send unit's setup screen if testing in C-band).
3. Verify that `Attn` on the Send PLCA-22 analyzer is set to 0. Set the number of packets to be transmitted to 9999k on that unit and set the packet length to 13 bytes. Set `TxVpp: 10`.
4. Without the UUT connected, press START on the Send PLCA-22 analyzer. A test should begin and the receive packet count on the Recv PLCA-22 analyzer should increment with a packet error rate very close to 0%. The signal strength meter on the Recv PLCA-22 analyzer should have the LEDs up to and including the -3dB primary signal strength LED illuminated. The 0dB primary LED may or may not be flashing.
5. Next, connect the UUT as shown in Figure 7.7. The -3dB primary signal strength LED on the Recv PLCA-22 analyzer either should be flashing or illuminated continuously. If the -3dB primary LED is extinguished, then the

input impedance of the UUT is excessively low (<100Ω). The impedance of the UUT must be corrected before proceeding; refer to the node checklist described in Appendix B for assistance.

6. Record the results of Step 5 in Table 7.1 at the end of this chapter.

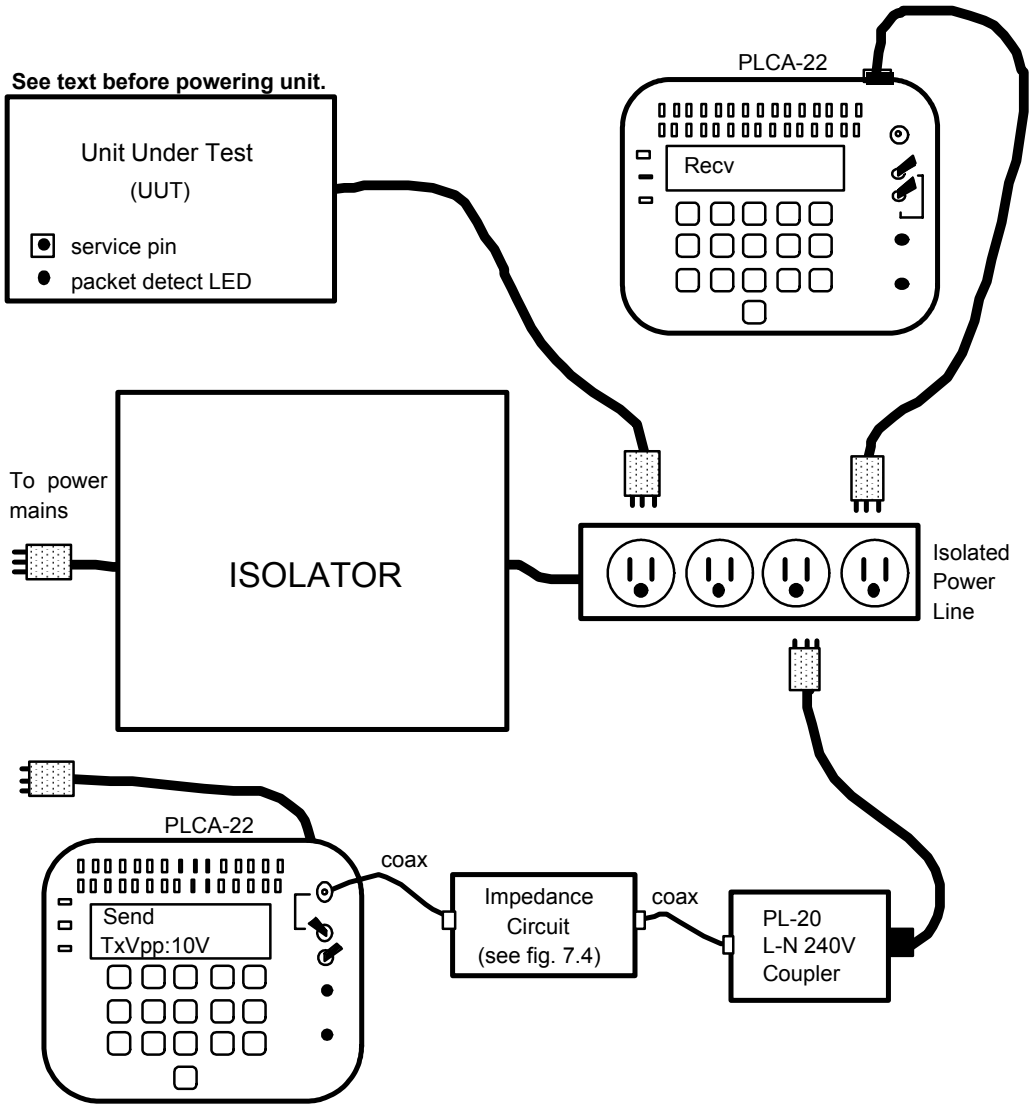


Figure 7.7 Excessive Loading Verification

Transmit Performance Verification

Use the following procedure to verify that the transmit output impedance of the UUT is low enough to adequately drive low impedance loads.

1. With a single PLCA-22 analyzer in idle mode (no packets being transmitted) and set for the same band of operation as the UUT, Internal and Line-to-Neutral coupling, connect the analyzer, the UUT, the "5Ω load", and the

Isolator as shown in Figure 7.8 (if the UUT uses Line-to-Earth coupling to a single power phase then the "7Ω load" should be used instead).

2. Verify that the UUT application program is not sending messages.
3. Press the service switch on the UUT.
4. Observe the primary signal strength LEDs on the PLCA-22 analyzer and check which of the primary LEDs illuminate. All primary LEDs up to, and including, the 0dB LED should flash for at least 6 out of 10 service pin messages from the UUT.
5. Record the result of Step 4 in Table 7.1 at the end of this chapter.

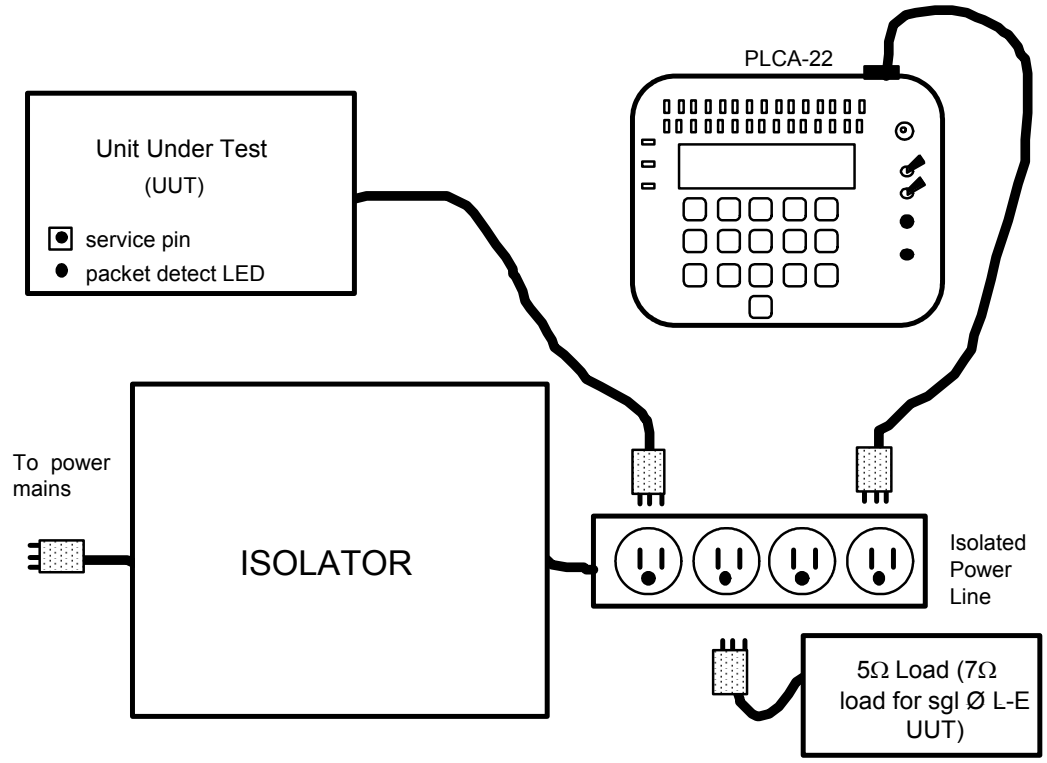


Figure 7.8 Transmit Performance Verification

If the correct LEDs do not illuminate, there might be a problem in the transmit path of the power mains coupling circuit of the UUT. Possible causes of a reduced transmit signal level include:

- Additional series impedance has been inadvertently added between the transmit amplifier of the PL Smart Transceiver and the mains connection.
- The DC resistance of the series resonant inductor in the coupling circuit (L2/L102 in Chapter 4 coupling circuit figures) is too high.
- The UUT contains a low-current line fuse that has high series resistance.
- A component of the wrong value has been inadvertently used in the UUT.

- Inadequate analog power supply (V_A) voltage under conditions of full transmit current loading.

Refer to the node checklist in Appendix B for more information about verifying the design of the UUT.

Receive Performance Verification

The receive performance verification procedure requires a software tool to measure the number of uncorrupted packets received by the UUT. Packet error rate is then calculated based on the number of packets sent and the number correctly received.

Packet Error Measurement with NodeUtil

A DOS utility called **NodeUtil** (`nodeutil.exe`) is used to measure packets correctly received by the UUT. The NodeUtil software allows a computer to remotely query the UUT and extract its status, including the number of uncorrupted packets received by the device. NodeUtil is available free of charge from the Echelon Web site at `www.echelon.com/downloads`. Select **Development Tools** from the *Search for software* drop-down menu.

Figure 7.9 illustrates the setup for the computer running the NodeUtil utility. The computer should contain an Echelon PCLTA-20 card equipped with a PLM-22 SMX transceiver. The PCLTA-20/PLM-22 is connected to the isolated power line via a PL-20 power line coupler. Ensure that the proper drivers for the PCLTA-20 and computer operating system are installed. Refer to the *LONWORKS PCLTA-20 PCI Interface User's Guide* for detailed driver setup and operation information.

NodeUtil runs on the computer (under DOS) and accesses the UUT over the power line. The verification procedure below describes how to use NodeUtil to access the UUT.

The startup screen for NodeUtil is shown below. Refer to the `nodeutil.txt` file for information on its proper setup.

```
Node Utility Release 1.82
Copyright (c) 1994, 2004 Echelon Corporation. All rights reserved.

Successfully installed network interface.
Welcome to the LONWORKS Node Utility application.
Activate the service pin on remote node to access it.

Enter one of the following commands by typing the indicated letter:
The NODEUTIL MAIN Menu

============================
The main command menu for NODEUTIL is as follows:
   A -- (A)dd node to list.
    C -- Set (C)lock rates of the network interface
    D -- Set the (D)omain of the network interface.
    E -- (E)xit this application and return to DOS.
    F -- (F)ind nodes in the current domain.
    G -- (G)o to node menu.............
    H -- (H)elp with commands.
    L -- Display node (L)ist.
    M -- Change node (M)ode or state.
    O -- Redirect (O)utput to a file.
    P -- Send a service (P)in message from a PCLTA.
```

```
R -- (R)eboot 3150 node.
S -- Report node (S)tatus and statistics.
V -- Control (V)erbose modes.
W -- (W)ink a node.
Z -- Shell out to DOS.
```

Receive Performance Verification Procedure

The following procedure is used to verify that the receive sensitivity of the UUT is correct. Determination of receive sensitivity is made by monitoring the physical layer error rate while increasing the level of signal attenuation between a reference transmitter and the UUT.

1. Verify that the UUT application program is not sending messages.
2. Set a first PLCA-22 analyzer (referred to as the Recv PLCA-22 analyzer) to the same band of operation as the UUT. Set it for `Recv` and `UnackPri` modes and configure it for Internal, Line-to-Neutral coupling as shown in Figure 7.9.
3. Set a second PLCA-22 analyzer (referred to as the send PLCA-22 analyzer) for the same band of operation as the UUT. Set it for `Send` and `UnackPri` modes of operation and configure it for External coupling. Connect the PLCA-22 analyzer using the attenuation circuit (30.1kΩ resistor of Figure 7.5) and the PL-20 Line-to-Neutral coupler as shown in Figure 7.9. Note that the line cord of the Send PLCA-22 analyzer is connected to the power mains on the input side of the isolator to prevent communications between the two PLCA-22 analyzers via parasitic line cord coupling.
4. Set the following parameters on the Send PLCA-22 analyzer:

Number of Packets	1000 (1k)
Packet Length	13 bytes
TxVpp	3.5V
Attn	0 dB

Note that 3.5Vp-p TxVpp is used for the Send PLCA-22 even though PL Smart Transceiver-based UUT's transmit using 7Vpp. Setting the Send PLCA-22 analyzer to 3.5Vp-p (6dB lower than the 7Vp-p transmit level of the UUT) provides the opportunity to test for 6dB more receive sensitivity when the analyzer's `Attn` is varied in later steps of this procedure.

5. Connect the UUT test setup as shown in Figure 7.9. Once NodeUtil is running correctly and the start-up screen shown above is displayed, press the service switch on the UUT. This will cause NodeUtil to register the service pin message received from the device. Select the "S" command to obtain the status from the UUT (the entry in the results screen named "Packets received by node" is the number of uncorrupted packets received by the UUT because the last time the statistics were cleared). Type "Y" at the prompt to clear the status of the UUT. The S command will be used in the next few steps to obtain the received packet count from the UUT. Be sure to clear the status of the UUT after each reading.
6. Press START on the Send PLCA-22 analyzer. The test will begin and the receive packet count on the Recv PLCA-22 analyzer should increment with a packet error rate very close to 0% (<1%). The -60dB LED on the primary frequency signal strength meter on the Recv PLCA-22 analyzer should illuminate, indicating that the received signal is approximately -60dB relative to the 3.5Vp-p transmit level (-66dB relative to a 7Vp-p transmit level). This level serves as a starting point; additional attenuation will be added via the `Attn` function of the Send PLCA-22 analyzer in Steps 8 and 9.
7. Once the Send PLCA-22 analyzer has transmitted 1000 packets, obtain the received packet count from the UUT using the NodeUtil **s** command. Record that value and the packet error rate of the Recv PLCA-22's analyzer in columns 4 and 5 primary frequency section of Table 7.1 at the end of this chapter. Calculate the error value as a

percentage by subtracting the number of packets received by the node from 1011 and then dividing by 10 (divide by 1000 then multiply by 100) and record the result in the right most column of Table 7.1. Refer to the notes at the end of these steps for details of this calculation.

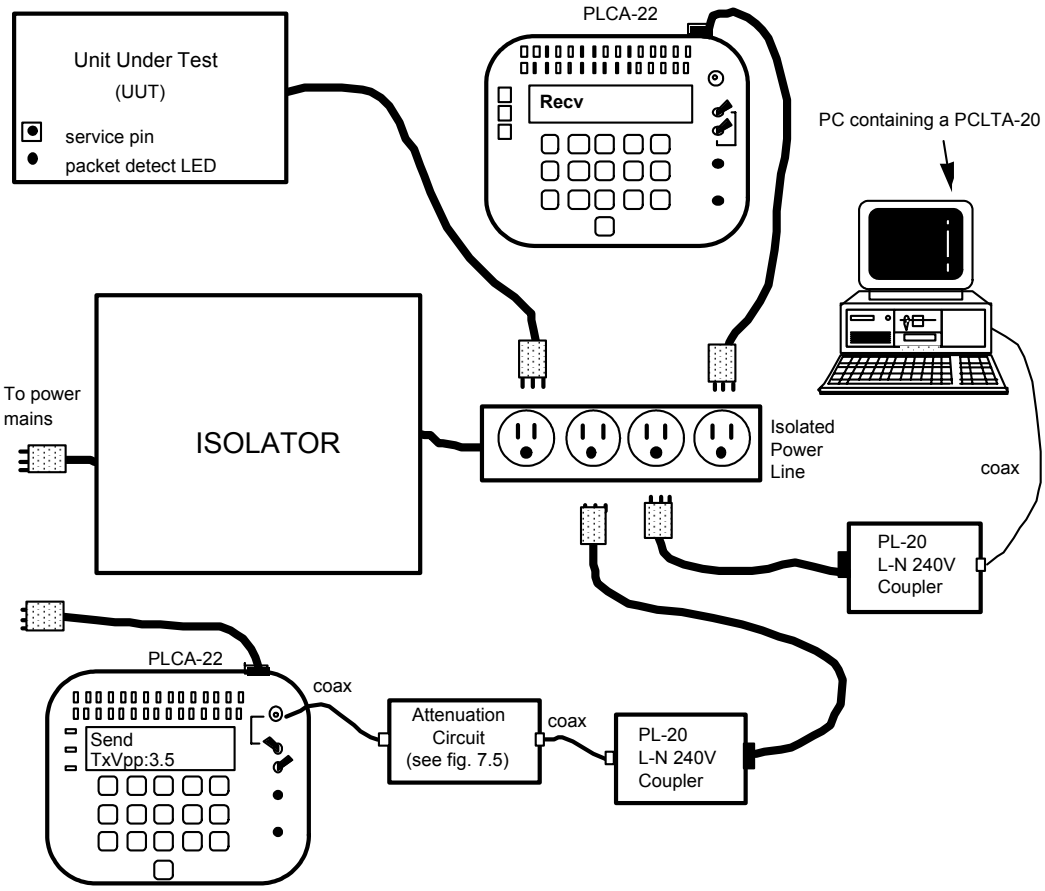


Figure 7.9 Receive Performance Verification

8. After moving the cursor to the `Attn` field, press the CHANGE and ENTER keys on the Send PLCA-22 analyzer to increment the `Attn` level by 6dB. Then clear the status on the UUT by responding with a "Y" to the NodeUtil prompt and then press START on the Send PLCA-22 analyzer.
9. Repeat Steps 7 through 8 above for all **Send Attn** levels up to, and including **24dB**, recording the results each time in theTable 7.1 at the end of this chapter.
10. To test the secondary operating frequency of the UUT, change the PLCA-22 analyzers from **UnackPri** to **Unack-Sec** mode. Repeat Steps 6 through 9, above, but record the results in the secondary frequency section of Table 7.1.

Notes:

The calculation of packet error rate used in the above verification procedure avoids inaccuracies which would result from the use of CRC error count to compute packet error rate. The material in this note is provided to explain how an accurate measure of packet error rate is determined.

Packet error rate actually includes both packets received with an incorrect CRC plus any packets which were so weak or corrupted they were not detected at all. These "missed packets" are, by definition, not included in the CRC error count of a node. For a physical layer packet error rate of 10%, the percentage of missed packets is generally negligible. Under

conditions where the packet error rate is greater than 10%, a significant portion of the error rate might be due to missed packets.

The “Packets received by node” field in NodeUtil software yields the actual number of packets correctly received by the node. Subtracting this number from the total number of packets sent gives the exact packet error count, including missed packets.

In addition to the number of test packets selected on the PLCA-22 analyzers, the total number of packets sent on the power line actually includes several control packets sent between the PLCA-22 analyzers. These control packets are used by the PLCA-22 analyzers to synchronize their settings before the test, and to exchange data related to the test immediately after the test. Additionally, querying the status of the UUT causes a few packets to be logged. The total overhead is generally 11 packets.

Given the above, a more accurate formula for calculating the physical layer packet error rate with 1000 test packets is then:

PER% = (1011 - # “Packets received by node”) x 100 / 1011

The overall signal attenuation between the Send PLCA-22 analyzer and Recv PLCA-22 analyzer shown in Table 7.1 is the sum of the attenuation level of the attenuator circuit and the **Attn** level of the Send PLCA-22 analyzer plus 6dB resulting from the use of a 3.5Vp-p transmit level on the Send PLCA-22 analyzer. A properly performing PL Smart Transceiver-based product will show a low packet error rate (<3%) up to an overall attenuation of 78dB r.e. 7Vpp (72dB for secondary frequency). Above these attenuations the error rate for the UUT can increase.

If the Recv PLCA analyzer and UUT error rates are not greater than 5% with 90dB of overall attenuation, then there is a problem with the test setup. Check that everything is setup as shown in Figure 7.9. Note that it is common for the UUT to work to approximately 6dB more overall attenuation than the Recv PLCA-22 analyzer due to enhancements in the PL Smart Transceivers.

If the results of this test are worse than expected, it is helpful to know if the problem affects only the performance of the UUT or if adjacent receivers are also impaired by the presence of UUT. If the receive performance of the Recv PLCA-22 analyzer was worse than expected, disconnect the UUT and recheck the PLCA-22 analyzer error rate versus attenuation. If it is determined that the presence of the UUT impairs the performance of the PLCA-22 analyzers then the UUT might be injecting noise back onto the power line. Note that the same symptoms would also be observed if no corrections were made to a UUT which previously failed the Excessive Loading Verification test.

If it is determined through a comparison of the UUT's expected and observed error rates that the UUT cannot reliably receive packets with an overall attenuation of at least 78dB r.e. 7Vp-p, then check the following:

- If the UUT includes a switching power supply, ensure that the power supply noise masks of Chapter 5 have been met.
- Compare the values of the coupling circuit components with those recommended in Chapter 4. It is possible that the wrong value component was inserted and partial, if compromised, receive performance was still possible.
- Re-verify the Unintentional Output Noise Verification test earlier in this chapter.
- Re-verify the receive mode impedance of the UUT by repeating the Excessive Loading Verification Test earlier in this chapter.

Refer to the node checklist in Appendix B for more information about verifying the design of the UUT.

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Table 7.1 PL 3120/PL 3150 Smart Transceiver Performance Verification			
Manufacturer		Test spec	Echelon 005-0154-0B V2 Ch 7
Product		Line voltage	_____VAC
Neuron Core ID	_____ _____ _____ _____ _____ _____	Line frequency	_____50Hz _____60Hz
Band	_____A-band _____C-band	Date tested	_____/_____/_____
Coupling type	_____1-Phase _____ 3-Phase	Tested by	

Preliminary Checks

		Fail	Pass
V_A power supply voltage	10.8V to 18.0V _____V		
V_{DD5} power supply voltage	4.75V to 5.25V _____V		
Oscillator frequency	(6.5523 to 6.5549 or 9.9980 to 10.0020MHz) _____MHz		

Good Citizen Verification

Unintentional Output Noise Verification-UUT and RX analyzer with no packet transmission		Fail	Pass
Primary signal LEDs	-72dB not "on" solid and -66dB not flashing _____dB_____		
Secondary signal LEDs	-72dB not "on" solid and -66dB not flashing _____dB_____		
Packet Detect LED	must not flash more than once per minute _____/min		

Excessive Loading Verification - Send 10Vpp through 88.7Ω and external coupler		Fail	Pass
RX analyzer primary LEDs	-3dB LED must be "on" or flashing ____dB____on____Flash		

Transmit Performance Verification - RX analyzer reading UUT svc pin msg. 5/7Ω load		Fail	Pass
RX analyzer primary LEDs	0dB LED must flash ≥6/10 tries ____dB____/10 tries		

Receive Performance Verification - Send 1kpkts at 3.5Vpp through 30.1kΩ attenuator	Fail	Pass

Primary Frequency

Send PLCA Transmit Attenuation (Attn)	Overall Attenuation (Attn + 66)	Recv PLCA UnackPri Error% (expected)	Recv PLCA UnackPri Error% (observed)	UUT #Pkts Received (observed)	UUT Pri Error% (expected)	UUT Pri Error% (1011-#Rcvd)/10
0 dB	66 dB	<1%	%		<1%	%
6 dB	72 dB	<3%	%		<2%	%
12 dB	78 dB	any	%		<3%	%
18 dB	84 dB	any	%		any	%
24 dB	90 dB	≥5%	%		≥5%	%

Secondary Frequency

Send PLCA Transmit Attenuation (Attn)	Overall Attenuation (Attn + 66)	Recv PLCA UnackSec Error% (expected)	Recv PLCA UnackSec Error% (observed)	UUT #Pkts Received (observed)	UUT Sec Error% (expected)	UUT Sec Error% (1011-#Rcvd)/10
0 dB	66 dB	<1%	%		<1%	%
6 dB	72 dB	any	%		<3%	%
12 dB	78 dB	any	%		any	%
18 dB	84 dB	any	%		any	%
24 dB	90 dB	≥5%	%		≥5%	%

8

PL Smart Transceiver Programming

Introduction

Certain parameters of PL 3120 and 3150 Smart Transceivers are programmed by the developer. This chapter provides an explanation of the various choices and how they are programmed by way of the NodeBuilder® Development Tool version 3.1 (or later).

The factory default transceiver type for the PL 3120 Smart Transceiver is PL-20N. This allows programming PL 3120 Smart Transceiver chips in system through the power line network without having to pre-program the parts using a programmer.

Dual Carrier Frequency Mode

Each PL Smart Transceiver incorporates dual carrier frequency capability which allows it to communicate with other PL Smart Transceiver and PLT-22-based devices, even if noise is blocking its primary communication frequency range. If impairments prevent communication in this range, a PL Smart Transceiver based device can automatically switch to a secondary carrier frequency to complete a transaction with other PL Smart Transceiver or PLT-22-based devices.

With the dual carrier frequency feature the last two retries of acknowledged service messages are sent using the secondary carrier frequency. Thus, in A-band and when acknowledged service is used with three retries (four total tries), the first two tries are sent using the 86kHz primary carrier frequency. If the last two tries are needed to complete the transaction, they are sent (and acknowledged) using the 75kHz secondary carrier frequency. Similarly, for C-band operation the primary and secondary frequencies are 132kHz and 115kHz respectively. A minimum of two retries must be used if the PL Smart Transceiver is to be able to use both carrier frequency choices. For optimum reliability and efficiency, Echelon recommends the use of three retries when using acknowledged service messaging with the PL Smart Transceiver.

When unacknowledged repeat message service is used, the PL Smart Transceiver leverages the reliability of both carrier frequencies by alternating between them. In this case, an unacknowledged repeat message with three repeats results in the first and third packets being sent using the primary carrier frequency, while the second and fourth packets are sent using the secondary carrier frequency. A minimum of one repeat must be used for the PL Smart Transceiver to use both carrier frequency choices.

In the C-band mode of operation, every PL Smart Transceiver transmission at the secondary carrier frequency is accompanied by a simultaneous 132kHz “pilot” signal which older PLT-20 and PLT-21-based devices can use to recognize that the channel is busy. This pilot signal prevents PLT-20- or PLT-21-based devices (which cannot detect the 115kHz secondary carrier frequency) from transmitting at the same time that a PL Smart Transceiver is transmitting on its 115kHz secondary carrier frequency.

CENELEC Access Protocol

To allow multiple power line signaling devices from different manufacturers to operate on a common AC-mains circuit, the CENELEC EN 50065-1 standard specifies an access protocol for the C-band (125kHz to 140kHz). The frequency 132.5kHz is designated as the primary band-in-use frequency that indicates when a transmission is in progress.

Every CENELEC compliant C-band device must both monitor the 132.5kHz band-in-use frequency and be able to detect the presence of a signal of at least 86dBμV_{RMS} anywhere in the range from 131.5kHz to 133.5kHz which has a duration greater than or equal to 4 milliseconds. A power line signaling device is permitted to transmit if the band-in-use detector shows that the band has been free for at least 85 milliseconds. Each device must randomly choose an interval for transmission, and at least seven evenly distributed intervals must be available for selection. A group of

power line signaling devices is allowed to transmit continually for a period less than or equal to one second, after which it must cease transmitting for at least 125 milliseconds.

The PL Smart Transceivers incorporate the CENELEC access protocol and the user can enable or disable the CENELEC access protocol at the time of channel definition. When enabled, the PL Smart Transceiver enforces the CENELEC access protocol while still maintaining the benefits of the LonTalk protocol. When the CENELEC access protocol is enabled, overall network throughput is reduced by 11%.

The CENELEC access protocol must be enabled to meet regulatory requirements in countries that follow CENELEC regulations (i.e., most European countries). It is recommended that the CENELEC access protocol be disabled on products that will be used in any country that does not follow CENELEC regulations, in order to maximize throughput. Note that devices that have the CENELEC protocol enabled should not be installed on the same network with devices that have the CENELEC protocol disabled. In this instance the devices with the CENELEC protocol enabled would be prevented from transmitting whenever there was heavy traffic from the CENELEC protocol disabled devices. Thus all of the devices on a single network should either have their CENELEC protocol enabled or they should all have it disabled. CENELEC regulations do not specify an access protocol for use in the CENELEC A-band. When programmed with the A-band transceiver parameters described later in this chapter, the internal CENELEC access protocol for the PL Smart Transceiver is disabled. With this selection, an active Band-In-Use signal will not prevent a PL Smart Transceiver from transmitting.

Power Management

PL Smart Transceivers incorporate a power management feature that supports the design of low cost power supplies in very cost sensitive consumer applications such as networked light dimmers, switches, and household appliances. This class of application typically requires only occasional, or low duty cycle, transmission from the consumer device. Power supplies for these devices can take advantage of the very low receive-mode current of the PL Smart Transceivers as well as wide V_A supply operating range (+8.5VDC to +18VDC) to reduce power supply cost.

A low transmit duty cycle implies that the device transmits packets infrequently, e.g., the product waits for a minimum of 10 packet times between transmitting each packet - a 10% transmit duty cycle. A power supply design that takes advantage of this duty cycle can store energy on a capacitor during the relatively long period between transmissions, when the Smart Transceiver draws very little current, and then consume the stored energy to transmit a packet. This type of power supply, referred to as an “energy storage power supply,” stores energy by charging an energy storage capacitor to a relatively high voltage (e.g., 15V) while in receive mode. The voltage on the capacitor then falls or “droops” toward a lower limit (e.g., 9.0V) while transmitting. The energy storage capacitor is then slowly recharged to the higher voltage during the relatively long time between transmissions. Traditionally, the proper design of such a power supply required knowledge of the maximum transmit duty cycle to be supported, and an implementation that accounted for all worst case operating conditions (temperature, line voltage, component variation and transmitter loading).

The cost of such a power supply can be significantly reduced if, instead of designing the supply for the maximum possible transmit duty cycle and for the worst case environmental conditions, the supply can be designed for typical operating conditions. However, designing for typical operating conditions implies that a mechanism is needed to “manage” the worst case operating conditions such that reliable operation is assured. This management feature must also address products whose operating conditions (especially transmit duty cycle) are not known in advance.

The power management feature of PL Smart Transceiver implements the needed management functionality by intelligently monitoring the energy storage power supply. Should the device attempt to transmit too frequently, the power management feature enforces a limit on the transmit duty cycle by preventing the PL Smart Transceiver from transmitting until the power supply of the device recovers to the point that sufficient energy is available to transmit a packet. Details of this feature and application examples are provided in Chapter 5.

The user can enable or disable power management by selecting how the Out-Of-Gas pin (OOGAS) of the PL Smart Transceiver is connected and by the "standard transceiver type" that is selected at the time of channel definition. If the OOGAS pin of the PL Smart Transceiver is connected directly to its VCORE pin then power management is disabled independent of the standard transceiver type that is used. If the OOGAS pin of the PL Smart Transceiver is connected to the specified V_A resistive voltage divider, then the user can enable power management at the time of channel definition by choosing a standard transceiver type with a "LOW" suffix. The only difference between a set of standard transceiver parameters with the "LOW" suffix and the corresponding set without the "LOW" suffix is whether the power management feature is selected or not. Enabling power management requires both, use of the specified OOGAS voltage divider and a standard transceiver type with a "LOW" suffix.

When power management is enabled, PL Smart Transceivers require a V_A supply voltage of 13.0V before they can be assured of transmitting a packet. A product with a fixed V_A power supply less than or equal to 13.0V should never have power management enabled because it might not be allowed to transmit. Likewise a device whose power supply relies on power management to operate correctly should never have the power management feature disabled. Table 8.1 summarizes these points.

Table 8.1 Power Management Requirements Vs. Type of Power Supply

Power Management	Fixed V_A Power Supply ≤13.0V	Energy Storage V_A Power Supply >13.0V in Receive Mode
Disabled	OK	Not allowed if the power supply design relies on power management for worst case duty cycle and load conditions.
Enabled	Not allowed: device might not transmit	OK

Note that some legacy network tools load a device's communication parameters as part of the installation and replacement process and calculate those parameters based on the channel (rather than the particular device). Such tools can not be used for systems that contain a mixture of devices with and without power management enabled on the same channel.

Tools based on the LNS™ network operating system, such as the LonMaker™ Integration Tool, correctly support all configurations of PL Smart Transceiver based devices with or without power management. For a tool not based on LNS, contact your tool vendor to determine if it can support a mixture of power management and non-power management nodes on the same channel.

Standard Transceiver Types

Two standard transceiver types are defined for the PL Smart Transceivers operating in A-band and four are defined for C-band operation. These standard transceiver types specify communications parameters for a PL Smart Transceiver (or PLT-22, PLT-21, or PLT-20) based device.

In A-band, the two available communication parameters differ only with regard to selection of the power management feature.

In C-band, the communication parameters of the four standard types are identical except for the state of the CENELEC protocol and selection of the power management feature.

Table 8.2 shows how the various features of the PL Smart Transceiver are selected using the six standard transceiver types and OOGAS IC pin.

Table 8.2 Standard PL Smart Transceiver Types

Standard Transceiver Type	Band	CENELEC Protocol	Power Management	
			OOGAS Pin Connected to VCORE Pin	OOGAS Pin Connected to Specified Resistors
PL-20A	A	Disabled	Disabled	Disabled
PL-20A-LOW	A	Disabled	Disabled	Enabled
PL-20C	C	Enabled	Disabled	Disabled
PL-20N	C	Disabled	Disabled	Disabled
PL-20C-LOW	C	Enabled	Disabled	Enabled
PL-20N-LOW	C	Disabled	Disabled	Enabled

NodeBuilder Tool Support

PL Smart Transceivers are supported by the NodeBuilder version 3.1 (or later) Development Tool. They are not supported by the LonBuilder Developer's Workbench or older versions of the NodeBuilder Development Tool.

PL Smart Transceiver Channel Definitions

The appropriate standard transceiver type (PL-20N, PL-20C, PL-20N-LOW, PL-20C-LOW, PL-20A or PL-20A-LOW) is selected on the NodeBuilder Hardware Template Properties page, as shown in the figure below:

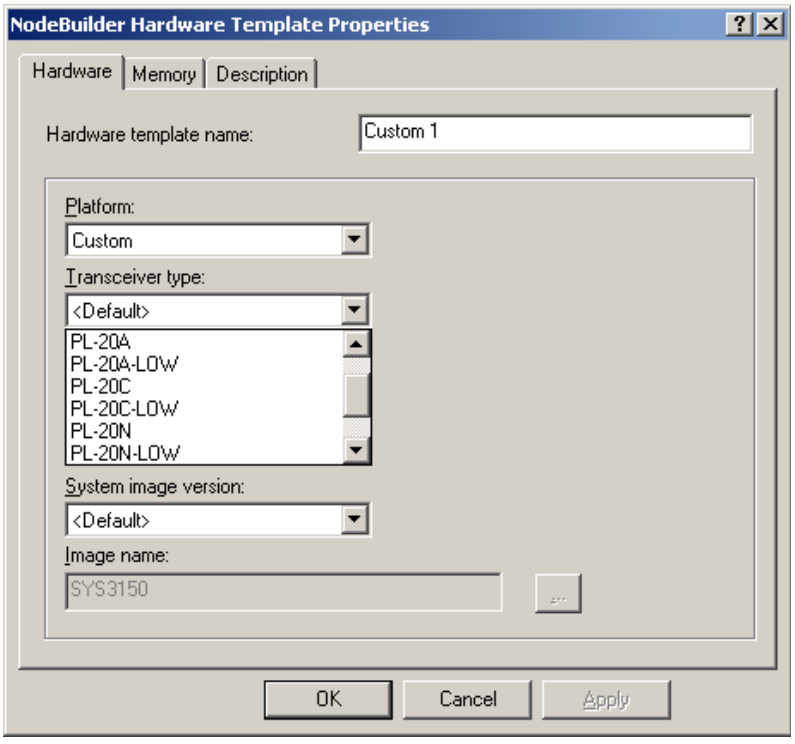


Figure 8.1 Choosing the Standard Transceiver Type in NodeBuilder Tool

PL Smart Transceiver Clock Speed Selection

When operating in A-band the PL 3120 Smart Transceiver uses a 6.5536MHz crystal and thus a clock speed of 6.5536MHz must be selected on the NodeBuilder Hardware Template Properties page as shown on the left of Figure 8.2. For C-band operation where a 10MHz crystal is used a clock speed of 10MHz must be selected as shown on the right of Figure 8.2.

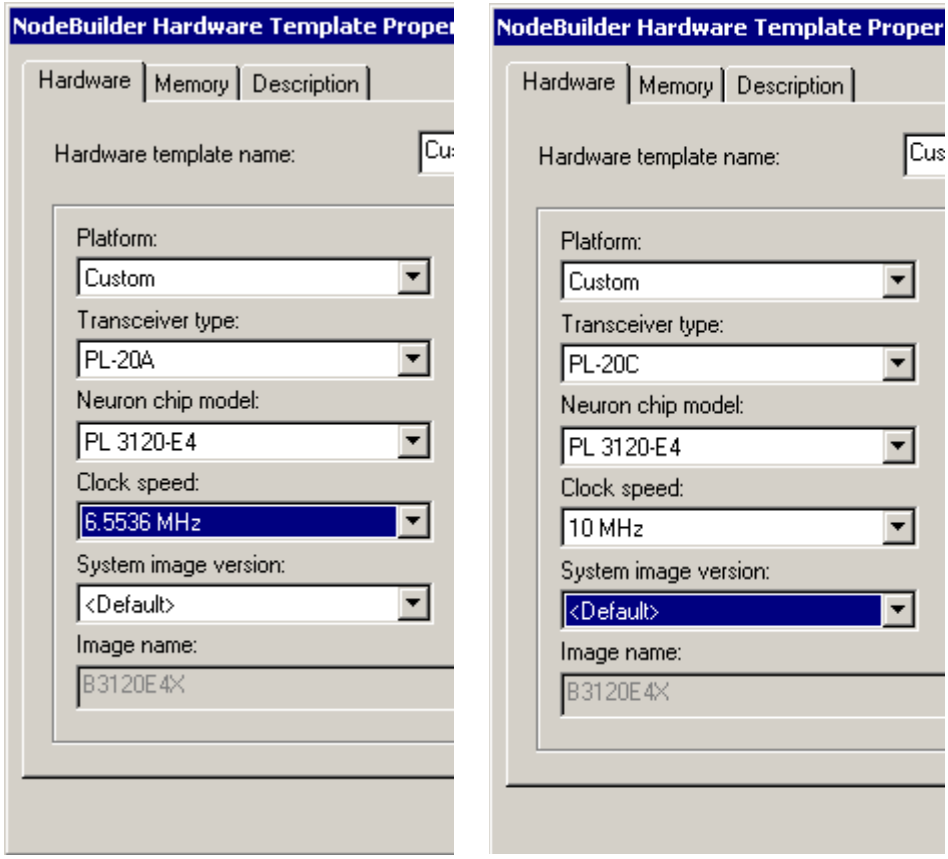


Figure 8.2 Choosing the Clock Speed in NodeBuilder

Downloading Application and Transceiver Type Parameters

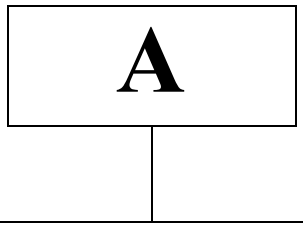
As the developer, you can solder the PL 3120 Smart Transceiver into a device and load applications and different transceiver parameters using the **NodeLoad** command-line application (available as a free download from the Echelon Web site at `www.echelon.com/downloads`. Select **OEM Components** from the *Search for software* drop-down menu).

The NodeLoad application allows you to change the PL 3120 Smart Transceiver parameters from the PL-20N default parameters to any of the other supported parameters. It is possible, for example, to change from PL-20N parameters to PL-20A. PL-20A devices with PL-20N parameters will communicate on the A-band network because the crystal frequency of 6.5536MHz determines the communication band.

Note: If you do change the parameters to the PL-20A, be sure the change the parameters for all your PL 3120 Smart Transceiver-based devices before shipping to the final customer.

When building devices with energy storage supplies, you must take care to insure the power supply does not drop below 10 volts during programming or before the LOW transceiver parameters are loaded. This can be accomplished by using a higher voltage on the power line input or by directly applying the V_A voltage using pogo pins into the device. The first step when using NodeLoad should be to download the PL 3120 Smart Transceiver parameters. See the NodeLoad user's guide for how to download these parameters.

NodeLoad supports the Echelon standard power line network interfaces. The maximum download time is about 30 seconds for an application that consumes all available EEPROM memory in the PL 3120 Smart Transceiver. If your production line is capable of producing one completed device every 10 seconds, then 3 NodeLoad stations will be required to keep up with the production volume. Isolators will be required at each NodeLoad station to prevent communications between different stations. See the *Power Line Test Isolator* section in Chapter 7 for details on how to build your own isolator.



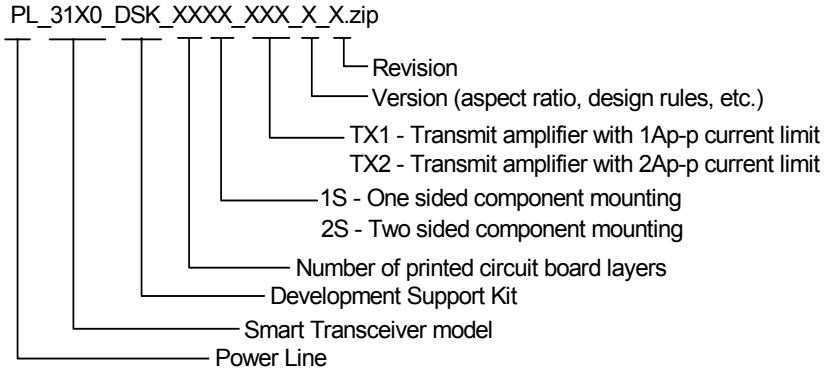
PL Smart Transceiver Reference Designs

Introduction

This appendix describes the implementation of the external, discrete interface circuitry for the PL 3120 and PL 3150 Smart Transceivers. The interface circuitry includes the front-end filter for the receiver and the power amplifier for the transmitter. The interface is comprised of roughly fifty components, primarily resistors and capacitors. Echelon provides a comprehensive **PL Development Support Kit** (DSK) for implementing the interface circuitry. The section that follows lists the contents of the DSK. Contact your Echelon salesperson for details about purchasing the DSK.

Reference designs are provided with the DSK to address applications requiring different numbers of printed circuit board (PCB) trace layers, single or double sided component assembly, various aspect ratios, and transmit current requirements. Each PL Smart Transceiver reference design package consists of a zip archive file that contains all of the relevant files for that design. The naming convention used for these zip files is shown in the figure below.

Figure A.1 Reference Design Naming Convention



Development Support Kit Contents

The PL Smart Transceiver DSK includes the following reference designs:

Reference Design Number	PL Smart Transceiver Model	Description	Zip File Name
1200	PL3120-E4T10	2 layer 23x63mm PCB layout with 1-sided component mounting and 1Ap-p transmit amplifier	PL_3120_DSK_2L1S_TX1_1_R.zip
1201	PL3120-E4T10	4 layer 20x38mm PCB layout with 2-sided component mounting and 1Ap-p transmit amplifier	PL_3120_DSK_4L2S_TX1_1_R.zip
1204	PL3120-E4T10	2 layer 33x38mm PCB layout with 1-sided component mounting and 1Ap-p transmit amplifier	PL_3120_DSK_2L1S_TX1_2_R.zip
1205	PL3150-L10	4 layer 36x49mm PCB layout with 2-sided component mounting and 1Ap-p transmit amplifier	PL_3150_DSK_4L2S_TX1_1_R.zip
1209	PL3120-E4T10	4 layer 31x53mm PCB layout with 2-sided component mounting and 2Ap-p transmit amplifier	PL_3120_DSK_4L2S_TX2_1_R.zip
1217	PL3120-E4T10	4 layer 17x38mm PCB layout with 2-sided component mounting and 1Ap-p transmit amplifier (**SIP Design**)	PL_3120_DSK_4L2S_TX1_2_R.zip
1218	PL3150-L10	4 layer 48x66mm PCB layout with 2-sided component mounting and 2Ap-p transmit amplifier	PL_3150_DSK_4L2S_TX2_1_R.zip

Reference Design Files

For each reference design the following files are provided.

File Name	Description
Using the Reference Layouts.pdf	Explains how to use the reference layout files
Using the Viewer.txt	Text file describing how to obtain and use a free P-CAD® viewer
012-xxxx-01_R_Schematic.dsn	Schematic design file in OrCAD® format
012-xxxx-01_R_Schematic.pdf	Schematic design file in PDF format
012-xxxx-01_R_BOM.doc	Bill of materials in MS Word format
012-xxxx-01_R_BOM.pdf	Bill of materials in PDF format
373-xxxx-01_R_Layout_PCAD.pcb	Layout design file in P-CAD format
373-xxxx-01_R_Layout_PCAD_Graphic.pcb	Traceable layout image in P-CAD format
373-xxxx-01_R_Layout_PADS_Graphic.pcb	Traceable layout image in PADS/PowerPCB format
373-xxxx-01_R_Layout_OrCAD_Graphic.max	Traceable layout image in OrCAD format
373-xxxx-01_R_Layout_DXF.zip	Layout layer plots in DXF format (zip file)
373-xxxx-01_R_Layout_ASCII.pcb	Layout design in ASCII format
373-xxxx-01_R_Layout_PDIF.zip	Layout design in P-CAD Database Interchange (PDIF) format (zip file)
373-xxxx-01_R_Layout_Gerbers.zip	Layout layer plots in Gerber format (zip file)
373-xxxx-01_R_Layout.pdf	Layout layer plots in PDF format

Reference Design Specifications

Recommended Operating Conditions for Reference Designs with 1Ap-p Transmit Amplifier

Symbol	Parameter	Min	Typ	Max	Unit
V_{ARX}	V_A Supply Voltage - Receive Mode	8.5	12.0	18.0	V
V_{ATX}	V_A Supply Voltage - Transmit Mode (1)	10.8	12.0	18.0	V
T_A	Ambient Temperature (1)	-40	25	85	°C

Electrical characteristics of Reference Designs with 1Ap-p Transmit Amplifier (over recommended operating conditions)

Symbol	Parameter	Min	Typ	Max	Unit
I_{ARX}	V_A Supply Current - Receive Mode		350	500	μA
I_{ATX}	V_A Supply Current - Transmit Mode		120	250	mA
V_{OTX}	Transmit Output Voltage		7		Vp-p
I_{TXLIM}	Transmit Output Current Limit		1.0		Ap-p
Z_{INRX}	Input Impedance - Receive Mode (with recommended RXCOMP inductor)		500		Ω
Z_{OTX}	Output Impedance - Transmit Mode		0.9		Ω
V_{PMU}	Power Management - Upper V_A Threshold	11.2	12.1	13.0	V
V_{PML}	Power Management - Lower V_A Threshold	7.3	7.9	8.6	V

NOTE: Minimum value can be 8.5V under certain conditions (refer to Chapter 5 for details).
The following formula must also be satisfied: $V_{ATXAVE} < (150-T_{AMAX})/(8*D_{MAX})$;
Where: V_{ATXAVE} = Average V_A supply voltage while transmitting
T_{AMAX} = Maximum ambient temperature (degrees C)
D_{MAX} = Maximum transmit duty cycle of the device (expressed as a decimal number)

Recommended Operating Conditions for Reference Designs with 2Ap-p Transmit Amplifier

Symbol	Parameter		Min	Typ	Max	Unit
V_{ARX}	V_A Supply Voltage - Receive Mode	A-band C-band	12.0 14.25	15.0 15.0	18.0 18.0	V
V_{ATX}	V_A Supply Voltage - Transmit Mode (1)	A-band C-band	12.0 14.25	15.0 15.0	18.0 18.0	V
T_A	Ambient Temperature (1)		-40	25	85	°C

Electrical characteristics of Reference Designs with 2Ap-p Transmit Amplifier (over recommended operating conditions)

Symbol	Parameter		Min	Typ	Max	Unit
I_{ARX}	V_A Supply Current - Receive Mode			350	500	μA
I_{ATX}	V_A Supply Current - Transmit Mode			160	500	mA
V_{OTX}	Transmit Output Voltage	A-band C-band		8 10		Vp-p
I_{TXLIM}	Transmit Output Current Limit			2.0		Ap-p
Z_{INRX}	Input Impedance - Receive Mode (with recommended RXCOMP inductor)			500		Ω
Z_{OTX}	Output Impedance - Transmit Mode			0.7		Ω
V_{PMU}	Power Management - Upper V_A Threshold		11.2	12.1	13.0	V
V_{PML}	Power Management - Lower V_A Threshold		7.3	7.9	8.6	V

Note: The following formula must also be satisfied: $V_{ATXAVE} < (150\text{-}T_{AMAX})/(5.6*D_{MAX})$;

Where: V_{ATXAVE} = Average V_A supply voltage while transmitting

T_{AMAX} = Maximum ambient temperature (degrees C)

D_{MAX} = Maximum transmit duty cycle of the device (expressed as a decimal number)

The Importance of Using Development Support Kit (DSK) Reference Designs

Each DSK reference design implements a very wide dynamic range circuit that is sensitive to layout variations in the same way that a high-performance radio is sensitive to circuit changes. With proper layout, each Smart Transceiver will be capable of receiving signals measured in hundreds of micro-volts (millionths of a volt). Layout errors can severely compromise receive capability and render the device unsuitable for many applications.

Every Power Line Smart Transceiver transmits signals on the order of several volts and is capable of driving 1 to 2 amperes of current into a low-impedance power line. Careful circuit layout is required to ensure that heat is properly dissipated and amplifier stability ensured across the range of operating temperatures. Ordinary circuit layout techniques are not suitable for delivering >100kHz modulated signals at high current. The combination of voltage and current produced by the transmit amplifier generates significant heat and dictates very careful component placement and PCB copper design.

The DSK reference designs have been subjected to thorough electrical and thermal analysis which address all of the above issues. DSK reference designs thoroughly validated by Echelon have:

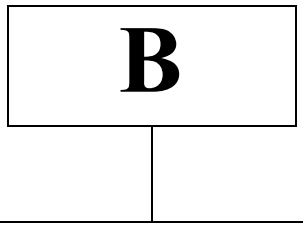
- Passed hundreds of hours of validation testing at voltage and temperature extremes;
- Been verified to comply with a twenty-six point checklist based on knowledge drawn from dozens of smart transceiver implementations; and
- Completed thousands of Monte Carlo simulation runs to ensure that all critical performance parameters are maintained over the full range of component tolerance and environmental conditions.

Any deviation from DSK reference layouts will very likely result in degraded performance in one or more of the areas described in the table below.

Critical Area	**Consequences of not following Guidelines**	**Causes for Consequence(s)**	**Solutions**
Electromagnetic Compliance (e.g., conducted emissions, surge, or ESD)	- Multiple PCB layout iterations - Field failures due to degraded surge immunity - Intermittent operation due to degraded ESD immunity	- Deviating from DSK reference layouts - Ignoring the coupling circuit and power supply recommendations in Chapters 4 and 5	- Use an approved DSK reference design without modification - Follow the recommendations in Chapters 4 and 5 - Conduct a design review with Echelon
Heat Management	- Premature field failure	- Changing the relative position of components on the reference layout - Reducing the quantity or location of copper on the reference layout - Adding “thermal reliefs” to the reference design copper	- Use an approved DSK reference design without modification - Conduct a design review with Echelon
Communication Performance	- Devices that function under typical laboratory conditions may not be able to communicate under worst case field conditions	- Changing the relative proximity or dimensions of certain PCB tracks on the reference design - Ignoring the coupling circuit and power supply recommendations in Chapters 4 and 5	- Use an approved DSK reference design without modification - Follow recommendations in Chapters 4 and 5 - Verify that the frequency of the crystal oscillator is centered as described in Chapter 2 - Verify communication performance as described in Chapter 7 - Conduct a design review with Echelon

All of the above issues can be avoided by using DSK reference designs without modification, and by following the coupling circuit, power supply, and crystal oscillator recommendations in Chapters 2, 4, and 5.

Echelon offers a comprehensive design review service to assist developers with respect to adherence to the DSK and Data Book requirements. Contact your local distributor or Echelon sales person to arrange for a design review.



PL Smart Transceiver-Based Device Checklist

Introduction

This appendix includes a checklist to ensure that devices that use PL 3130 and 3150 Smart Transceivers perform to their full capability. All pages of Appendix B can be copied.

Device Checklist

PL Smart Transceiver DSK (Development Support Kit) reference design layout and components

Item	Check When Completed	Description
1		Reference design used:_____ Use the name of the ZIP archive file containing the reference design document. For example, `PL_3120_DSK_2L1S_TX1_1_R`.
2		Describe deviations, if any, in implementing Reference Design Layout: **Note:** Only special and well justified cases can have deviations from the reference layout.
3		Check that the fabrication notes from the reference design package have been followed with regard to the PCB material, layer thickness, plating and via clearance.
4		If physical unit is available, the product has been verified to meet communication performance capabilities per Chapter 7.
5		If device utilizes power management OOGAS pin has been connected to appropriate voltage divider to V_A.
6		For non-power management devices OOGAS is connected to VCORE and R24 and R25 are not loaded. **Note:** If the design needs to support enabling and disabling power management, then do not connect OOGAS to VCORE directly, just place R24 and R25 as shown in the reference design. The power management feature will be enabled/disabled by choosing the right communication channel when building the device with NodeBuilder.
7		The PL Smart Transceiver operating clock frequency has been measured and is sufficiently close to nominal (6.5536MHz for A-band or 10.0000MHz for C-band) such that when accounting for crystal variation and temperature variation, the total frequency deviation from nominal will not exceed ±200ppm.
8		If used, the transceiver BIU, PKD, and TXON signals are connected to low-current (≤12mA) LEDs via series current-limiting resistors connected to ground.
9		If used, the transceiver BIU, PKD, and TXON signals are connected to ESD protection diodes if a plastic or metal enclosure without a good ground connection is used.

10		CLKSEL pin is tied high.
11		For PL 3120 Smart Transceiver-based devices, ICTMode pin is tied to ground.
12		For PL 3150 Smart Transceiver-based devices, ICTMode pin is tied low via a 5k ohm resistor if the ICTMode tri-state control is required for ICT of the device PCB.
13		A Low Voltage Interrupt (LVI) circuit with open collector output (such as the Dallas Semiconductor DS1233-5) is used to supply a reset signal to the PL 3150 Smart Transceiver if flash memory is used.
14		A Low Voltage Interrupt (LVI) circuit with open collector output (such as the Dallas Semiconductor DS1233-5) is used to supply a reset signal to either the PL 3150 or PL 3120 Smart Transceiver if an external oscillator is used.
15		If any additional open drain device is connected to the reset line, a capacitor of at least 100pF and less than 1,000pF is connected between $\overline{\text{RESET}}$ and ground. The capacitor should be placed as close as possible to the PL Smart Transceiver $\overline{\text{RESET}}$ pin.

PL 3120 and PL 3150 Smart Transceiver Programming

16		The correct standard transceiver type is defined for the transceiver by way of NodeBuilder 3.1 or later: 1. A-band Power management disabled: PL-20A Power management enabled: PL-20A-LOW 2. C-band Power management disabled: CENELEC disabled: PL-20N CENELEC enabled: PL-20C Power management enabled: CENELEC disabled: PL-20N-LOW CENELEC enabled: PL-20C-LOW

PL 3120 and PL 3150 Smart Transceiver Coupling Circuit General

17		A coupling circuit that is suitable for the intended application is selected, and coupling circuit components meet the specifications shown in Chapter 4 (as appropriate).
18		The maximum value of C101 for Line-to-Earth coupling circuits results in a maximum of 3.5mA ground leakage current (or as required by local electrical codes and the presence of GFIs/RCDs.)
19		No filters or power supply transformers are in the coupling circuit path. If a ferrite bead is in the coupling circuit path it is either a common mode connected (see Chapter 6) or has been verified to be <0.5Ω @100kHz.
20		Circuit traces between the output of the transmit amplifier and the AC mains are ≥1.3mm wide and ≤13cm long.
21		The signal return traces from the AC mains connection to the transmit amplifier are a copper plane or ≥1.3mm wide.
22		The trace between C103 and D101 is ≥1.3mm wide and ≤1.3cm long.
23		The trace between C103 and the V_A input of the transmit amplifier is ≥1.3mm wide and ≤2.5cm long.

24		Capacitors added for EMI suppression (if needed) meet the requirements of Table 6.1.

PL 3120 and PL 3150 Smart Transceiver Coupling Circuit Components Key Specifications

25		Fuse F101 6A or 6.3A rating (DC resistance ≤0.1Ω) Time lag (slow blow type) Proper voltage rating
26		Capacitor C101 Proper value selected 10% (or better) tolerance Proper voltage rating (including AC or DC) Safety listing, if applicable
27		Capacitor C102 Metallized polyester (required for surge immunity) Proper value selected Proper tolerance Proper voltage rating
28		Inductor L101 (for a non-transformer isolated coupling circuit) 1.0mH value DC current rating ≥30mA DC resistance ≤14Ω 10% (or better) tolerance
29		Inductor L103 Proper value DC current rating ≥30mA DC resistance ≤55Ω 10% (or better) tolerance
30		L101 and L103 spaced > 1cm (0.4 inches) apart (for a non-transformer isolated coupling circuit)
31		Inductor L102 (if needed) Proper value selected per Chapter 4 Proper DC current rating Proper DC resistance 10% (or better) tolerance If toroidal inductor is used, select current rating to avoid saturation (2-3X that of the example inductor)
32		Transformer T101 (for a transformer isolated coupling circuit) Transformer with correct specification is selected See Appendix C
33		Resistor R101 Proper value for discharge time requirements Proper voltage rating (>1.4*AC_{RMS} line voltage) Proper power rating for hi-pot test (if applicable)
34		Capacitor C103 Proper value Voltage rating ≥16VDC Proper ESR@100kHz Verify suitable lifetime rating

35		PROTECT circuit If Varistor used: Proper AC or DC voltage rating Surge rating for application requirements, see Chapter 4 No varistor to earth unless hi-pot testing is performed prior to insertion of varistor and ground leakage current is not an issue. If gas-discharge tube used place on line side of fuse
36		Diode D101 Reverse breakdown ≥50V forward voltage ≤1.3V@1A@25C surge current ≥30A for 8.3ms reverse recovery ≤200ns reverse current ≤100uA@100C typical capacitance ≤40pF@4V
37		Diode D102 Reverse breakdown ≥50V forward voltage ≤1.0V@1A@25C surge current ≥30A for 8.3ms reverse recovery ≤25ns reverse current ≤100uA@100C typical capacitance ≤40pF@4V
38		If a linear supply has been used, skip the remaining power supply checklist sections.

PL 3120 and PL 3150 Smart Transceiver Power Supply - Switching Type

39		The preferred operating frequency of the switching power supply is 46kHz - 55kHz, or 90kHz - 110kHz, or >155kHz under all line, load, environmental, and production conditions.
40		A series inductor is used between the power supply input and the power mains to avoid attenuation due to the input stage of a switching power supply.
41		The value of the series inductor has been selected for the application requirements as described in Chapter 5.
42		The inductor has a current rating adequate to support the peak currents drawn by the power supply without saturation.
43		The LC resonant frequency of the inductor is at least 1 octave from the communication frequency range (70kHz-90kHz for A-band and 110kHz-138kHz for C-band) when the inductor is combined with the input capacitance of the switching supply.
44		The power supply complies with the input noise masks shown in Chapter 5.
45		Measurements of the power supply are made by connecting the supply to the artificial mains network as specified in sub clause 8.2.1 of CISPR Publication 16, second edition. Measurements are made over the full range of anticipated loads on the supply and conducted in accordance with the CENELEC EN 50065-1 and FCC measurement standards with measurement bandwidths of 200Hz below 150kHz and 9kHz above 150kHz, as described in CISPR 16.

PL 3120 and PL 3150 Smart Transceiver Power Supply - General

46		If the power supply does not meet the appropriate noise mask for the power supply unit, a correct filter is installed between the local switching power supply and the power line.

47		All output noise masks shown in Chapter 5 are satisfied using measurements taken over the full range of anticipated loads on the supply.

EMI & ESD Design

48		The “leakage” capacitance from high-frequency circuit traces is controlled via guard traces.
49		The product’s package is designed to minimize the possibility of ESD hits arcing into the device’s circuit board. If the product’s package is plastic, then the PCB is supported in the package so that unprotected circuitry on the PCB is not adjacent to any seams in the package. The PCB is not touching the plastic enclosure near a seam.
50		Explicit clamping of user-accessible circuitry is used to shunt ESD currents from that circuitry away from sensitive components to ground.
51		The connector, diodes and decoupling capacitor are all located such that ESD currents are shunted around sensitive circuitry.
52		Proper measurement of conducted emissions is used to verify compliance with FCC Part 15 and/or CENELEC EN 50065-1 as described in Chapter 6.
53		A 50Ω//(50µH+5Ω)Line Impedance Stabilization Network (LISN) as specified in *CISPR Publication 16*, second edition is used for measurement.
54		The appropriate attenuator is used to ensure that the transceiver’s transmit signal does not overload the measurement apparatus. The residual noise floor of the entire measurement set is verified to be at leas 10dB below the specification limit (a noise floor less than 38dBµV for FCC measurements, and a noise floor less than 36dBµV for CENELEC EN 50065-1 measurements).
55		Measurements are made with a quasi-peak detector and the average detector as specified in *CISPR Publication 16*.
56		FCC measurements are made with a 9kHz bandwidth filter as specified. The CENELEC EN 50065-1 measurements are made with a 200Hz bandwidth filter for measurements below 150kHz, and a 9kHz bandwidth filter for measurements above 150kHz.
57		For EN 50065-1 verification, all testing is done with a Rohde & Schwarz EMI Test Receiver ESHS30 (or equivalent tester with proper filter skirts) set to manual mode using a setup program described in Chapter 5. Alternately, Hewlett Packard equipment is used with an appropriate external filter.

Product Qualification - Electromagnetic Immunity and Communication Performance

58		The product is tested to appropriate levels of either CEI/IEC 1000-4-5, or IEEE C62.41-1991.

PL 3150 External Memory Interface

59		For PL 3150-based devices, check that the memory load capacitance and time requirements have been met.

C

Isolation Transformer Specifications

12μH-Leakage Transformer Specifications

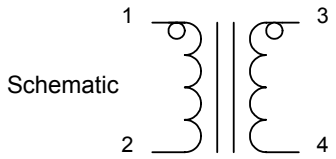


Table C.1 12μH-Leakage Transformer Electrical Specifications

Parameter	Min	Typ	Max	Units
Turns Ratio (1-2):(3-4)		1.0		
DC Resistance 1-2, 3-4			0.20	ohm
Magnetizing Inductance 1-2 Dry, @100kHz, $1V_{RMS}$	0.75	1.0	1.25	mH
Magnetizing Inductance 1-2, Wet, @100kHz, $1V_{RMS}$, plus 15mADC	0.75			mH
Leakage Inductance 1-2 (3-4 shorted) @100kHz, $1V_{RMS}$	10.8	12.0	13.2	μH
Winding Capacitance 1-2			30	pF
Winding-to-Winding Capacitance 1-2 shorted to 3-4 shorted			30	pF

Contact vendors for mechanical information, temperature ranges, safety agency compliance, and pricing information.

Table C.2 12μH-Leakage Transformer Vendors and Part Numbers

Vendor	Contact Information	Part Number(s)
EXCEL Electric Corporation www.excelelectriccorp.com	Telephone: +1-954-581-2330 Fax: +1-954-581-2355	EXL-324 EXL-165 EXL-165S
Precision Components, Inc. www.pcitransformers.com	Telephone: +1-630-462-9110 Fax: +1-630-469-9901	0505-0671
Tamura Corporation www.tamuracorp.com	Telephone: +81-492-84-5721 (Japan) +1-800-472-6624 (USA) Fax: +81-492-84-9106	PLP01
Transpower Technologies, Inc. www.trans-power.com	Telephone: +1-775-852-0140 Fax: +1-775-852-0145	TTI7143

Low-Leakage Transformer Specifications

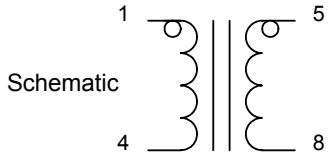


Table C.3 Low-Leakage Transformer Electrical Specifications

Parameter	Min	Typ	Max	Units
Turns Ratio (1-4):(5-8)		1.0		
DC Resistance 1-4, 5-8			0.35	ohm
Magnetizing Inductance 1-4 Dry, @100kHz, $1V_{RMS}$	0.75	1.45	1.8	mH
Magnetizing Inductance 1-4, Wet, @100kHz, $1V_{RMS}$, plus 30mADC	0.75			mH
Leakage Inductance 1-4 (3-4 shorted) @100kHz, $1V_{RMS}$			1.0	µH
Winding Capacitance 1-4			25	pF
Winding-to-Winding Capacitance 1-4 shorted to 5-8 shorted			50	pF

Contact vendors for mechanical information, temperature ranges, safety agency compliance, and pricing of their parts listed below.

Table C.4 Low-Leakage Transformer Vendors and Part Numbers

Vendor	Contact Information	Part Number
Precision Components, Inc. `www.pcitransformers.com`	Telephone: +1-815-476-9881 Fax: +1-815-476-2535	0505-0821
Transpower Technologies, Inc. `www.trans-power.com`	Telephone: +1-775-852-0140 Fax: +1-775-852-0145	TTI8231

D

Manufacturing Test and Handling Guidelines

Production Test Guidelines

This section describes suggested production test procedures associated with the physical layer functionality of the PL 3120 and PL 3150 Smart Transceivers as used in a typical device. The production test procedure described below is applicable for a PL Smart Transceiver-based device operating in either A-band or C-band.

Physical Layer Production Test

Production Test Strategy

The production test strategy described in this document is not intended as a design verification test. It is assumed that the communication performance of the product, in which the PL Smart Transceiver has been embedded, has been fully verified by other means (see Chapter 7 for more information). Rather, the production test is designed to:

- Identify devices with manufacturing defects in the components surrounding the PL Smart Transceivers.
- Identify component substitutions, made over the course of high volume manufacturing that inadvertently impair power line communication performance by a significant amount. Such detection is not meant to replace re-qualification of the product design after component substitution, which should be considered a mandatory process.

In-Circuit Test (ICT)

The basis for the physical layer performance verification test is the assumption of 100% ICT of the Unit Under Test (UUT) printed circuit board (PCB) prior to production functional test. All passive components are to be tested to the accuracy of the ICT equipment, all transistors have basic diode and beta tests, all ICs have solder junctions verified via input diode tests, and all PCB traces are verified for continuity and verified for shorts. The recommended PCB layouts supplied with the PL Smart Transceiver Development Support Kit (DSK) include test points to allow 100% ICT coverage.

Any deviation from 100% coverage will require an extended physical layer test different from the one described in this document.

The $\overline{\text{RESET}}$ pin of the PL Smart Transceiver should be grounded during ICT. This will prevent the chip from performing an initial boot sequence. An initial boot should only be allowed when the integrity of the VDD_5 supply and $\overline{\text{RESET}}$ signal can be assured for the entire boot sequence. See Chapter 2 for details of the boot process and timing.

Transmitter Performance Verification

Transmitter performance is verified by causing the unit under test to transmit a packet into a low impedance load (on the order of 5 ohms), and then verifying that an acceptable amplitude signal (V_{RMS}) is produced.

Initiating a Packet Transmission

A simple way of causing the PL Smart Transceiver in the device to transmit a packet is to communicate with it over the power mains connection using a standard network management command. For instance, if a Query ID message is sent to the device the PL Smart Transceiver will respond with an “ID Response” message over the mains connection. This approach always works if the PL Smart Transceiver is an un-configured state and authentication is not enabled. If the UUT is in a configured state and has authentication enabled an alternate method of initiating a packet must be used.

Measurement Time Window

The ID Response message consists of a preamble followed by the unique 48 bit Neuron ID (NID) that was programmed into the PL Smart Transceiver when it was manufactured. Because each NID is unique, the V_{RMS} value of the transmit signal from the PL Smart Transceiver will vary from unit to unit when averaged over the entire transmitted packet. In order to provide a reproducible test, the transmit signal amplitude (V_{RMS}) of the UUT should only be measured during the initial preamble of the ID Response message. The preamble spans the first 35 bit times of the ID Response message. The first 35 bit times of the packet will be identical for all UUTs, independent of their unique NID.

The duration of the first 35 bit times varies depending on whether the product is operating in the A- or C-band as follows:

A-band 35 bit times = 9.70ms

C-band 35 bit times = 6.36ms

Transmit Signal Amplitude

When transmitting into the ~5 ohm load (described later in this chapter), the PL Smart Transceiver should produce an output signal of approximately $1.00V_{RMS}$ during the first 35 bit times of the service pin message (see Table D.1 for suggested test limits). The suggested test limits allow for normal production variability and should not be further guard-banded.

Receiver Performance Verification

Receiver performance is verified by sending a highly attenuated message to the UUT and verifying that the device responds to that message. The attenuated message is transmitted from an appropriate D/A card (such as the National Instruments PXI-6070E) using a waveform file supplied by Echelon. The response by the UUT to the attenuated message can be used for transmitter performance verification. It is not necessary to validate the contents of the response packet. The fact that the response packet was transmitted by the UUT indicates that the attenuated message was correctly received.

In order to have reasonable assurance that the UUT can receive packets with acceptable sensitivity, the receive test message is attenuated by ~70dB using the interface circuit described below (where attenuation= $20\log_{10}(Vin/Vout)$).

A/D, D/A- based Test System

This section describes a practical test system that can perform both transmit and receive performance verification.

Hardware Description

The test system should have the following components.

- Data acquisition hardware
- Test interface board

Data Acquisition Hardware

- A 12-bit A/D channel with a throughput of at least 1 Ms/s that is configured for referenced single ended, ±10V range
- A 12-bit D/A channel with a throughput of at least 1Ms/s that is configured for ±10V range
- Data acquisition channels that have an external trigger capability

National Instruments multifunction cards, such as PXI-6070E or PCI-MIO-16E-1, are examples of data acquisition hardware that meet the requirements for the test system.

Test Interface Board

A custom interface board needs to be designed to provide 70dB attenuation, a ~5 ohm load, a coupling circuit, and a peak detector circuit that triggers on the UUT transmitted packets. Figure D.1 is a diagram of the needed test interface board.

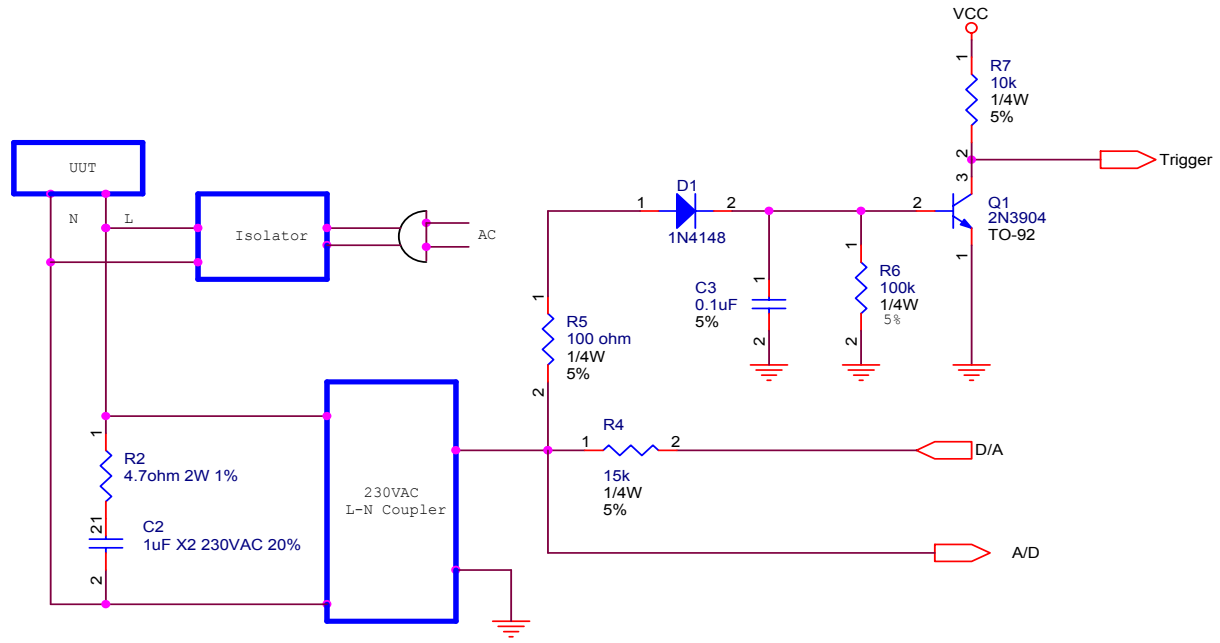


Figure D.1 Test Interface Board

The interface board performs three functions:

- The 4.7 ohm resistor in series with the 1uF X2 capacitor provides a low impedance load for the transmit level verification test.
- The 15k ohm resistor in conjunction with the 4.7 ohm resistor and 1uF X2 capacitor provide approximately 70dB of attenuation of the message generated by the D/A converter as part of the receive mode test.
- The 1N4148 diode, 0.1uF capacitor, 100k ohm resistor, 100 ohm resistor, and 2N3904 transistor provide a peak detect function to trigger the A/D converter when a packet is transmitted by the UUT in response to the message generated by the D/A converter.

A circuit such as the one described in Chapter 7, Figure 7.1, should be used for Isolation. An L-N coupler such as the one provided by Echelon (model number 78200-221) should be used for the power line coupling.

Software Description

Input file

A file containing either the A-band or C-band waveform that represents the Query ID broadcast message should be used as an input to the software. The file data represent amplitude in volts and interval between them is 1us. Any un-configured device with a PL Smart Transceiver will respond to the appropriate waveform by transmitting its Neuron ID. The files are available as a free download from the Echelon Web site (go to `www.echelon.com/downloads` and select **OEM Components** from the *Search for software* drop-down menu).

Test process

1. Read the waveform data into a buffer called `waveform[]`.
2. Scale the waveform by applying proper gain and offset in order to produce a 7V p-p waveform prior to the attenuation circuit. The waveform should be centered on zero volts.
3. Prepare the A/D channel to be ready for capturing the response of the UUT upon receiving a trigger signal from the interface board.
4. Output the `waveform[]` signal to the UUT through the A/D channel.
5. When the UUT receives the signal, it will respond with a message that contains the Neuron ID. This will take place in a few hundred milliseconds.
6. Capture the response and calculate the V_{RMS} value over the first 35 bits. The measurement window should be 9.7ms for A-band and 6.36ms for C-band.

The test limit for V_{RMS} value depends on the transceiver channel type and amplifier type that are used in the power line device. The table below lists suggested limits.

Table D.1 Test Limits of Different Transceiver Types

Transceiver Type used in the device	V_{RMS}
C-band 7V p-p/1A	0.8 (0.65 for 1-phase L-E coupling)
C-band 10V p-p/2A	1.3
A-band 7V p-p/1A	0.8
A-band 8V p-p/2A	1.2

Figure D.2 shows a complete test cycle with respect to transmit, receive, and trigger signals (the signal levels and timings in the figure are ***not to scale*** but are meant to illustrate the measurement concepts).

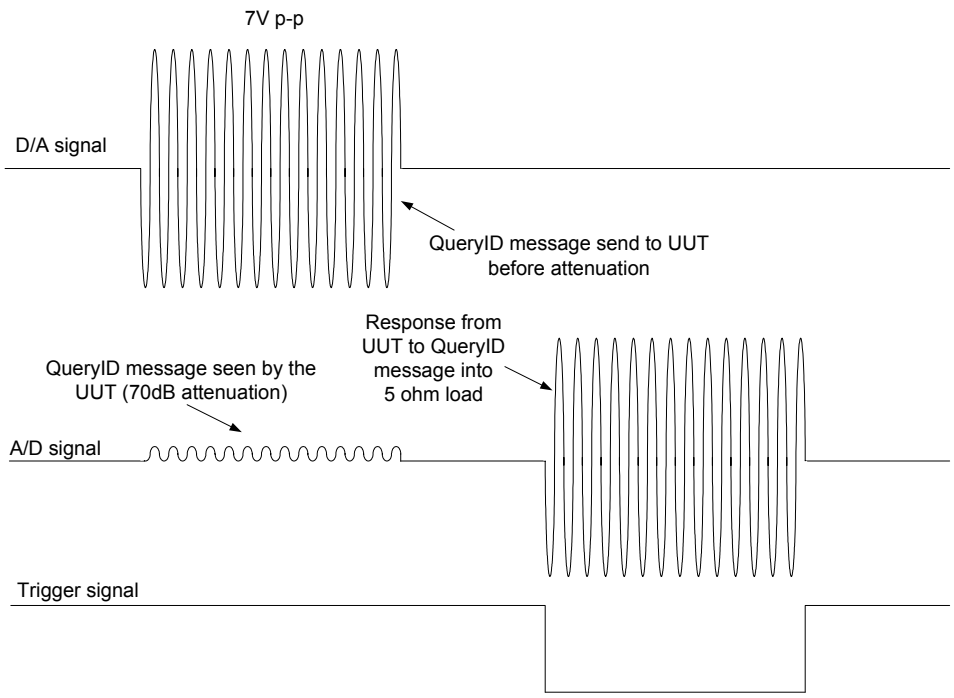


Figure D.2 Test Cycle Waveforms

Notes on Missed Messages

Due to the adaptive sensitivity algorithms in the PL Smart Transceivers, it is statistically possible for a good transceiver to miss a single packet. Therefore the test should be repeated two more times if the initial test fails. If the test passes in two out of three tries then the UUT is good. If the UUT passes in only one out of three tests then the UUT should be considered marginal and should be verified by way of the procedure in Chapter 7. A UUT that fails three or more tests is bad.

Test System Verification

This section is intended to describe a verification procedure that should be performed on a production test system in order to ensure repeatability of the power line physical layer test. The procedure includes:

- Verification of background noise in the test system
- Verification of Query ID message amplitude

Verification of Background Noise

One of the functions of the test system isolator is to prevent noise from either the power mains or other parts of the product test system from disturbing the test results. The test system is designed to transmit a Query ID message that has been attenuated by approximately 70dB referenced to the full amplitude transmission of the PL Smart Transceivers. The amplitude of the 70dB-attenuated message should be about 2mVp-p. In order to consistently verify that the UUT can receive this low level signal, the background noise level of the test system must be at least 6-9 dB lower in amplitude than that attenuated message. It is important to note that only noise at or near the PL 3150

Smart Transceivers communication frequencies can affect the reproducibility of the test. The power line isolator is designed to filter noise with frequencies near the PL Smart Transceivers communication frequencies. The isolator does not, however, filter out low frequency noise to a level that is 80dB below the PL Smart Transceivers transmit level. In fact it is not uncommon to observe low frequency noise on the order of 1Vp-p getting through the isolator. A consequence of this fact is that the background noise level must be measured with a frequency-selective instrument.

The simplest method of verifying the test system background noise is to connect one PLCA-22 (Power Line Communications Analyzer, Echelon Model 58022) to the mains connection of the UUT. The PLCA-22 can be used to monitor the noise level via its signal strength LED bar graph. The signal strength meter displays the mains signal levels after being filtered by the transceiver's internal digital signal processing. Thus the meter displays only the noise that will affect the PL Smart Transceiver. The background noise should read no higher than –78dB. That is, at most, only the –78dB LED on the signal strength meter should be illuminated. If additional LEDs are illuminated then the isolator should be verified as described in Chapter 7.

Verification of Query ID Message Amplitude

As described in the *Verification of Background Noise* section, the amplitude of the attenuated Query ID message should be about 2mVp-p and there will be low frequency noise present on the mains that will be much larger in amplitude. The consequence of this fact is that it is not practical to make a direct measurement of the attenuated message using a wide band instrument such as an oscilloscope. It will be very difficult to trigger on the packet given the noise present. The solution, once again, is to use a frequency-selective instrument.

The PLCA-22 can be used to verify the attenuation of the Query ID message and to monitor the amplitude of the Query ID message using the unit's signal strength meter. However, in this case the UUT must be disconnected from the test system so that only the Query ID message is observed and not the response to the Query ID from the UUT. Simply run the production test with the UUT disconnected and monitor the signal strength LEDs on the PLCA-22. The LEDs up to and including the –72dB LED should illuminate when the Query ID is transmitted. If more LEDs illuminate (for example, if the –66dB LED illuminates) then it indicates that the attenuation circuit is not operating properly. The key elements to verify are the 4.7 ohm resistor (R2), the 15k ohm resistor (R4), and the 50 ohm resistor in the isolator that sets the isolator output impedance.

Manufacturing Handling Guidelines

This section provides manufacturing guidelines regarding both soldering and handling of the PL Smart Transceivers.

Board Soldering Considerations

All PL Smart Transceiver chips have a Level 3 Classification in IPC/JEDEC Standard J-STD-020C. This means that parts have a 168-hour floor life at <30ºC and <60% R.H. once the parts have been removed from the moisture barrier bag. To prevent *pop-corning* during reflow, parts removed from the moisture barrier protection must be reflowed before 168 hours have passed. If they are not, then they must be drybaked. If drybaking is required, the parts should be baked for 24 hours at 125ºC or as required per IPC/JEDEC J-STD-033A. The tubes and reels that the PL 3120 Smart Transceivers are shipped in will not withstand the drybake. The trays that the PL 3150 Smart Transceiver is shipped in will withstand the drybake up to 125ºC.

The maximum peak temperature for PL Smart Transceivers is 235ºC for non-RoHS parts and 260ºC for RoHS parts. Consult the solder manufacturer's datasheet for recommendations on optimum reflow profile. The actual reflow profile chosen should consider the peak temperature limitations noted above.

The parts should, if possible, be handled only with properly calibrated mechanical pick and place equipment. Handling the parts manually increases the risk that the leads will become bent. Bent leads might then result in open or short circuits during the board-level assembly process.

Handling Precautions and Electrostatic Discharge

All CMOS devices have an insulated gate that is subject to voltage breakdown. The gate oxide for the PL Smart Transceiver breaks down at a gate-source potential of about 10V. The high-impedance gates on the devices are protected by on-chip networks. However, these on-chip networks do not make the IC immune to ESD. Laboratory tests show that devices can fail after one very high voltage discharge. They can also fail due to the cumulative effect of several discharges of lower potential.

Static-damaged devices behave in various ways, depending on the severity of the damage. The most severely damaged are the easiest to detect because the input or output has been completely destroyed and is shorted to V_{DD5}, shorted to GND, or is open-circuited. As a result of this, the device will no longer function. Less severe cases are more difficult to detect because they appear as intermittent failures or degraded performance. Static damage can often increase leakage currents.

CMOS devices are not immune to large static voltage discharges that can be generated while handling. For example, static voltages generated by a person walking across a waxed floor have been measured in the 4kV – 15kV range (depending on humidity, surface conditions, and so forth)

CMOS Devices

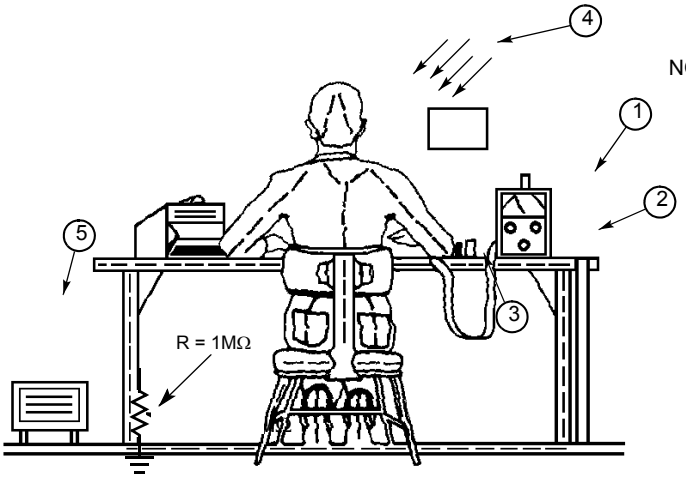
The following steps should be observed when working with CMOS devices.

- Do not exceed the maximum ratings specified by the data sheet.
- All unused digital device inputs should be connected to V_{DD5} or GND.
- All low-impedance equipment (pulse generators, etc.) should be connected to CMOS inputs only after the device is powered up. Similarly, this type of equipment should be disconnected before power is turned off.
- A circuit board containing CMOS devices is merely an extension of the device and the same handling precautions apply. Contacting connectors wired directly to devices can cause damage. Plastic wrapping should be avoided. When external connections to a PC board address pins of CMOS integrated circuits, a resistor should be used in series with the inputs or outputs. The limiting factor for the series resistor is the added delay caused by the time constant formed by the series resistor and input capacitance. This resistor will help limit accidental damage if the PC board is removed and is brought into contact with static-generating materials.
- All CMOS devices should be stored or transported in materials that are antistatic. Devices must not be inserted into conventional plastic “snow,” Styrofoam®, or plastic trays. Devices should be left in their original container until ready for use.
- All CMOS devices should be placed on a grounded bench surface and operators should ground themselves prior to handling devices, because a worker can be statically charged with respect to the bench surface. Wrist straps in contact with skin are strongly recommended. See Figure D.3.
- Nylon or other static-generating materials should not come in contact with CMOS circuits.
- If automatic handling is being used, high levels of static electricity can be generated by the movement of devices, belts, or boards. Reduce static build-up by using ionized air blowers or room humidifiers. All parts of machines which come into contact with the top, bottom, and sides of IC packages must be grounded metal or other conductive material.
- Cold chambers using CO_2 for cooling should be equipped with baffles, and devices must be contained on or in conductive material, or soldered onto a PCB.
- When lead-straightening or hand-soldering is necessary, provide ground straps for the apparatus used and be sure that soldering ties are grounded.

Wave-solder Operations

The following steps should be observed during wave-solder operations.

- The solder pot and conductive conveyor system of the wave-soldering machine must be grounded to an earth ground.
- The loading and unloading work benches should have conductive tops which are grounded to an earth ground.
- Operators must comply with precautions previously explained.
- Completed assemblies should be placed in antistatic containers prior to being moved to subsequent stations.



NOTES:
1. 1/16 inch conductive sheet stock covering bench-top work area.
2. Ground strap.
3. Wrist strap in contact with skin.
4. Static neutralizer. (Ionized air blower directed at work.) Primarily for use in areas where direct grounding is impractical.
5. Room humidifier. Primarily for use in areas where the relative humidity is less than 45%. Caution: building heating and cooling systems usually dry the air causing the relative humidity inside a building to be less than outside humidity.

Figure D.3 Typical Manufacturing Work Station

Board Cleaning Operations

The following steps should be observed during board cleaning operations.

- Vapor degreasers and baskets must be grounded to an earth ground. Operators must likewise be grounded.
- Brush or spray cleaning should not be used.
- Assemblies should be placed into the vapor degreaser immediately upon removal from the antistatic container.
- Cleaned assemblies should be placed in antistatic containers immediately after removal from the cleaning basket.
- High-velocity air movement or application of solvents and coatings should be employed only when module circuits are grounded and a static eliminator is directed at the module. The use of static-detection meters for line surveillance is highly recommended.
- The use of static-detection meters for line surveillance is highly recommended.
- Equipment specifications should alert users to the presence of CMOS devices and require familiarization with this specification prior to performing any kind of maintenance or replacement of devices or modules.
- Do not insert or remove CMOS devices from test sockets with power applied. Check all power supplies to be used for testing devices to be certain there are no voltage transients present.

- Double-check the equipment setup for proper polarity of voltage before conducting parametric or functional testing.
- Do not reuse shipping rails. Continuous use causes deterioration of their antistatic coating.
- Wrist straps and equipment logs should be maintained and audited on a regular basis. Wrist straps malfunction and can go unnoticed. Also, equipment gets moved from time to time and grounds cannot be reconnected properly.

Recommended Reading

Total Control of the Static in Your Business

Available from:

Static Control Systems Div.
Box ELB-3, 225-4S
3M Center
St. Paul, MN 55144

1-800-328-1368
1-612-733-9420 (in Minnesota)

E

References

This appendix provides a list of the reference material used in the preparation of this manual.

[1] 47CFR15, Subpart B (Unintentional Radiators), *U.S. Code of Federal Regulations*, (formerly known as FCC Part 15, Subpart J).

[2] *CENELEC EN 50065-1:2001 "Signaling on low-voltage electrical installations in the frequency range 3kHz to 148.5kHz" Part 1 "General requirements, frequency bands and electromagnetic disturbances,".*

[3] *CISPR 16, CISPR Specification for radio interference measuring apparatus and measurement methods*, International Electrotechnical Commission, Second edition, 1987.

[4] *IEC 61000-4-2 Electromagnetic compatibility, Part 4: Testing and measurement techniques - Section 2: Electrostatic discharge immunity test*, International Standard, First Edition, 1995-01.

[5] *IEC 61000-4-3 Electromagnetic compatibility, Part 4: Testing and measurement techniques - Section 3: Radiated, radio-frequency, electromagnetic field immunity test*, International Standard, First Edition, 1995-02.

[6] *IEC 61000-4-4 Electromagnetic compatibility, Part 4: Testing and measurement techniques - Section 4: Electrical fast transient/burst immunity test*, International Standard, First Edition, 1995-01.

[7] *IEC 61000-4-5 Electromagnetic compatibility, Part 4: Testing and measurement techniques - Section 5: Surge immunity test*, International Standard, First Edition, 1995-02.

[8] *IEEE C62.41-1991, IEEE Recommended Practice on Surge Voltage in Low-Voltage AC Power Circuits.*

[9] *Noise Reduction Techniques in Electronic Systems*, 2nd ed., by Henry W. Ott, John Wiley & Sons, 1988.

[10] "ESD as an EMI Problem....How to Prevent and Fix," *EDN Designer's Guide to Electromagnetic Compatibility*, EDN Supplement, pp. S23-S29, 1/20/94.

[11] *Protection of Electronic Circuits from Overvoltages*, by Ronald B. Standler, John Wiley & Sons, 1989.

[12] *Conducted Emissions Measurements on Power Line Transceiver Products: Test method for performing EN 50065-1 conducted emissions tests using Hewlett-Packard EMI test receivers, May 19, 1995.* A copy of this application note can be obtained by contacting:

Clay Bilby, EMC Applications Engineer
Santa Rosa Systems Division
Hewlett-Packard Company
1400 Fountaingrove Parkway
Santa Rosa, California, 95403
Main telephone number: 707/577-1414
Direct number: 707/577-3842
Fax: 707/577-5329

www.echelon.com