Cutting Edge 2

ELTRAN® ; Novel SOI Wafer Technology

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Abstract

ELTRAN®(Epitaxial Layer TRANsfer) wafers are the first and to date only manufacturable and commercially available SOI (silicon-on-insulator) wafers formed by bonding and etching-back porous Si in conjunction with hydrogen annealing. These wafers were developed and have been produced since 1990 by Canon Inc., Japan. The newest technique established for wafer fabrication is highly reproducible splitting within the porous Si layer by means of a water jet, which allows the seed wafer to be reused several times to reduce manufacturing costs. The thicknesses of both the SOI and the buried oxide layers are precisely controlled over a very wide range, from the extremely thin 10nm to as thick as 2-3μm, with thickness uniformity of less than ±5%. No COPs (Crystal-originated Particles or Pits) are generated in the active SOI layers by the epitaxial growth process. The buried oxides are thermally grown on epitaxial Si layers and have no pinholes. An atomically-flat surface is achieved in the SOI wafers by means of a newly developed process of annealing in hydrogen. Wafer sizes have been successfully expanded to 300-mm (12-inch) diameter; and SOI thickness uniformity of ±1.1%, which is even better than that of 8-inch wafers, has been achieved.

1. Introduction

SOI (silicon-on-insulator) technology has been at somewhat of a standstill for quite a long time, but now we are finally approaching a long-awaited period, with CMOS (complementary metal oxide semiconductor) applications of thin-film SOI wafers in particular about to reach a stage where they can be put to practical use. In the future it is anticipated that there will be new developments in the area of mainstream CMOS-LSI (large-scale integration) that will enable devices to be achieved for low power, high-speed logic and communications. Mass production trials of CMOS-LSIs employing SOI wafers were launched before the turn of the century for the purpose of enabling SOI to be adopted as the newest semiconductor IC technology for the 21st century.

SOI-Epi wafers™ of ELTRAN® (Epitaxial Layer TRANsfer) wafers are SOI wafers originally developed by Canon; they are BESOI (bond and etch-back SOI) wafers that make use of the selective etching of porous Si[1,2]. The fabrication method used involves combining the BESOI process with epitaxial growth on porous silicon that is capable of being etched with ultra-high selectivity and surface-smoothing achieved by hydrogen annealing. Another special feature of the method is that the bonded wafer is split into two at the porous Si layer, with one part becoming the ELTRAN® wafer and the other part being reused. This is important because along with product quality, reducing wafer manufacturing costs is one of the most important requirements for expanding the SOI market further.

At present, with the goal of showing the future potential of our SOI wafers, we are striving to develop 300mm-diameter wafers and sub-50nm ultra-thin films, as well as wafer recycling techniques aimed at reducing costs.

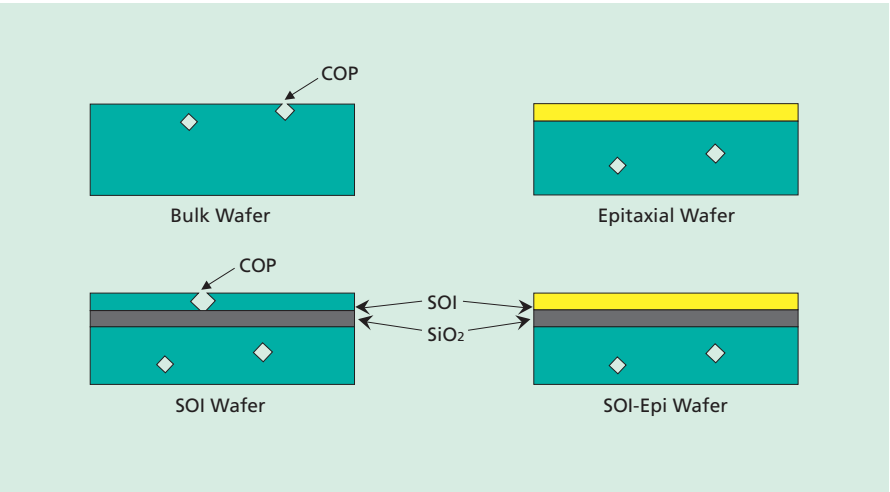

Fig.1 COPs in bulk wafer, epitaxial wafer, SOI wafer and SOI-Epi wafer.

2. Special Features of ELTRAN®

a. SOI-Epi Wafers™

Figure 1 shows the characteristic features of bulk wafers and epitaxial wafers used in current Si processes, along with SOI wafers and the SOI-Epi wafers™ that we have proposed. The reason that epitaxial wafers have come to be used is that the size of devices has approached that of COPs (0.1～0.2μm), and COPs cause degraded reliability of the gate oxide films of devices. In SOI devices, thin-film thicknesses have become comparable in size to, or even smaller than, COPs, and thus COPs are far more damaging to SOI devices than to bulk wafers. If an SOI wafer is immersed in HF solution, the buried oxide film underneath becomes directly etched through the COPs, which is easy to detect; such a defect is called an ***"HF defect"***. The density of HF defects must be no more than about 0.1 /cm^2. It is anticipated that this value will drop down to around 0.01 /cm^2 with further advances in miniaturization in the future. It is thus considered that technology

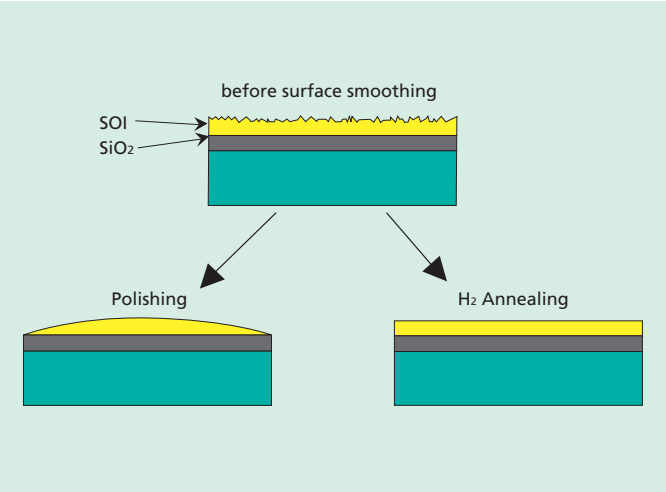

Fig.2 Surface smoothening of SOI wafers by polishing and H_2 annealing.

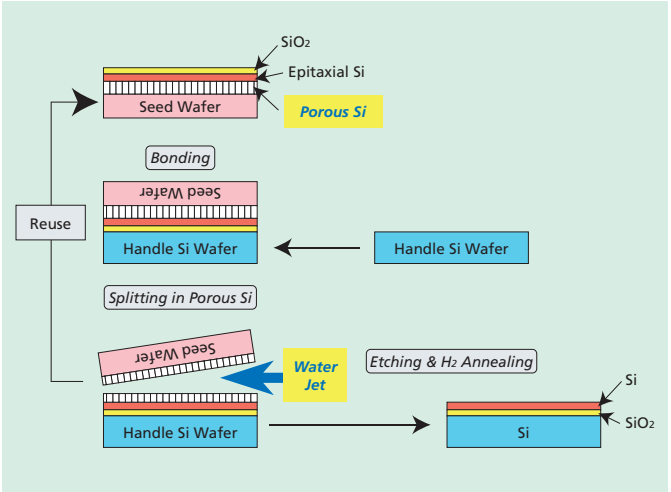

Fig.3 ELTRAN® process flow based on seed wafer reusage.

whereby an epitaxial layer is used as the SOI layer, i.e. COP-free SOI-Epi wafer™ technology, should be useful as far as thin-film SOI devices are concerned.

b. Surface-Smoothing Techniques

Figure 2 shows the surface smoothness of SOI wafers. Regardless of the manufacturing technique used, the surface just after the SOI structure has been formed is much rougher than that of a polished bulk wafer. This roughness could be removed by CMP (chemical mechanical polishing) to achieve a smoothness comparable to that of a polished bulk wafer. This would, however create problems of reduced film thickness, degraded wafer thickness uniformity, and less control stability during mass production. These problems would be particularly prominent in ultra-thin-film SOI wafers. With ELTRAN®, however, the hydrogen annealing process reduces the surface roughness (R_{rms}) of approximately 10nm by a factor of about 100, and as a result even the atomic steps can be observed[3]. Moreover, this new surface smoothing method enables the film thickness to be reduced to less than 1nm[4].

3. Process

Even though porous Si[5] was first discovered back in 1956[6], the ELTRAN® manufacturing process represents the only case where a use for porous Si in industrial manufacturing has been successfully found. This process comprises a number of sub-processes that harmoniously unite the three special features of porous Si, which are as follows:

1) Annealing porous Si in a hydrogen atmosphere[7] seals its surface pores and smoothes its surface, thus allowing a high quality epitaxial Si layer to be formed on top of it.

2) The enormous surface area[8] of porous Si contributes to extremely high etching selectivity of as high as 100,000.

3) The splitting plane can be specified by controlling the internal stress[9-11] of porous Si.

Figure 3 depicts the ELTRAN® process flow. The anodization involves passing a current through a solution of HF and ethanol with the single-crystal Si wafer as the anode in order to form microscopic pores of a few nm in diameter on the surface of the wafer at a density of $\sim 10^{11}$ /cm^2. The reaction occurs at the far end of the pores, meaning that the pores progressively elongate into the inside of the wafer. By varying the current density it is easy to create a porous layer that has a multi-layered structure, an example of which is shown in Fig. 4. In this example, the layer of porous Si closest to the surface was formed using a low current density, after which the current density was raised and a second layer of different porosity was formed. It can be seen from the figure that the first layer of porous Si contains microscopic pores of a few nm in diameter. A second layer containing pores with diameters 2 ~ 3 times greater is formed below this first layer.

Dry oxidation of the porous Si is then carried out at a low temperature of 400°C[12]. This results in oxidization of about 1~ 3nm of the inner walls of the pores, thus preventing the structure of the porous Si from changing under high-temperature treatment.

The porous Si is then baked at 1000 ~ 1100°C in a hydrogen atmosphere in a CVD (chemical vapor deposition) epitaxial reactor.

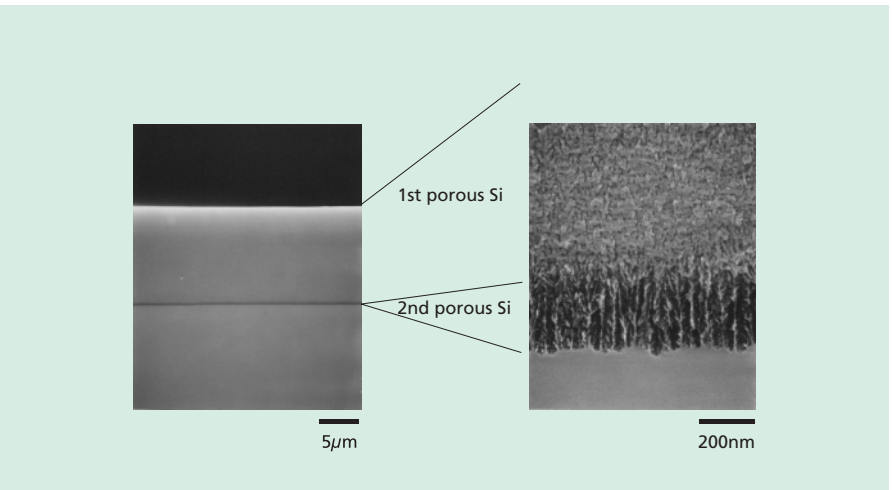

Fig.4 Cross-sectional micrographs of double-layered porous Si formed by changing anodic current.

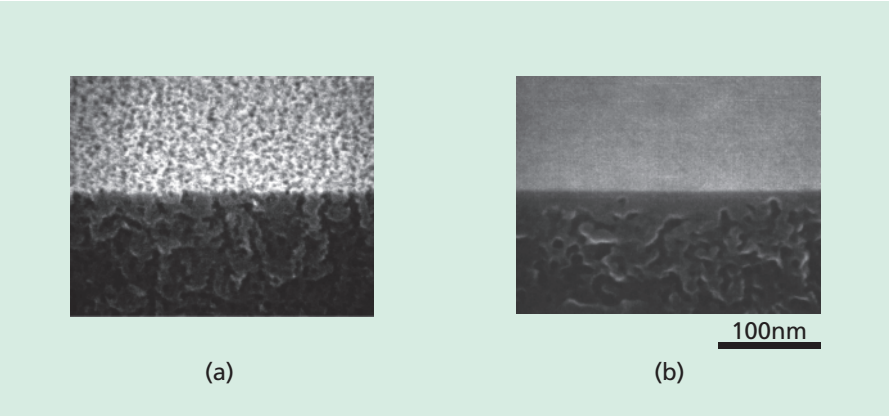

Fig.5 Porous Si surface (a) before and (b) after H_2 pre-baking.

Figure 5 shows SEM micrographs taken from an oblique angle before and after the hydrogen pre-baking[7]. It can be seen that the pre-baking causes the pores in the porous Si surface to close up to the extent that the pore density drops from about $10^{11}/cm^2$ to less than 10^4 $/cm^2$, and hence the surface is smoothed. The pre-baking enhances surface diffusion, which causes the surface pores to close up. A pre-injection method[13] was further devised whereby a small additional amount of Si is provided from the gas phase during the hydrogen pre-baking. As of the present, we have achieved a secco-etch defect density of the order of only $10^1/cm^2$. After the pre-injection, epitaxial growth is carried out at about 900 ~ 1000°C.

Next, the surface of the epitaxial Si layer is thermally oxidized. The resulting oxide film will become the BOX (buried oxide) film of the SOI wafer.

The surface of the thermally grown oxide film and the Si handle wafer that will become the supporting substrate are next cleaned, and then the surfaces of the two wafers are pushed together at room temperature, upon which they bond to one another by van der Waals forces. After that, heat treatment is carried out to form covalent bonds and thus strengthen the bonding between the two surfaces[14]. Moreover, using a quartz wafer as the handle wafer makes it possible to manufacture light-transparent ELTRAN® wafers.

The porous Si layer in the bonded wafer has a double-layer structure. A water-jet method[9-11, 15] is used to split the bonded wafer parallel to its surface close to the interface between the two layers This procedure is described in detail below.

After splitting, the first porous Si layer remains on the handle wafer side; this layer is uniform in thickness across the whole wafer. The handle wafer part is then etched using a solution containing a mixture of HF, H_2O_2 and H_2O[8]. The etching characteristics of porous Si and non-porous Si are shown in Fig. 6. It can be seen that with the use of the $HF/H_2O_2/H_2O$ mixture, once a certain incubation period has passed, the porous Si is etched virtually all at once. The selectivity of this etching is as high as 100,000, meaning that the etching does not cause any degradation of the thickness uniformity of the SOI layer. The etching solution penetrates into the pores of the porous Si by capillarity, and then etches the walls of the pores in a sideways direction. Eventually, the porous structure can no longer support itself and collapses. Since each wall between neighboring pores is etched from both sides, the thickness of epitaxial Si that must be etched is effectively half of the thickness of the wall, which is at most about 10nm. This means that it is possible to uniformly etch porous Si layers more than 10μm thick across the whole surface of the wafer, and since the selectivity is as high as 100,000, there is virtually no degradation of the thickness uniformity in the SOI layer.

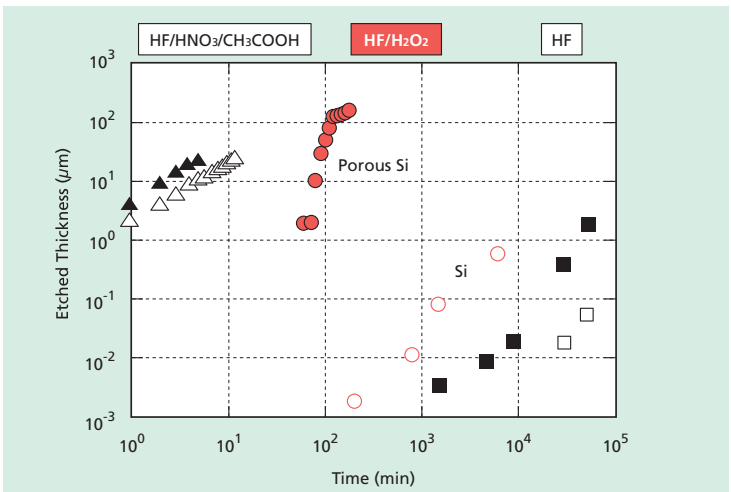

Fig.6 Etching characteristics of porous Si (closed symbols) and nonporous Si (open symbols) obtained through immersion in $HF/HNO_3/CH_3COOH$ (triangles), HF/H_2O_2 (circles) and HF (rectangles) as a function of etching period.

If heat treatment in a hydrogen-containing atmosphere is now carried out, the rough surface (Fig. 7(a)) just after selective etching becomes smoothed as shown in Fig. 7(b)[3]. The surface roughness was measured by AFM (atomic force microscopy). For a 1μm × 1μm region, the hydrogen annealing reduced the root mean square roughness to about 0.1nm, which is at least as good as that of the polished bulk wafer. Moreover, even the atomic steps could be seen, showing that smoothness down to the atomic scale was achieved.

After splitting, residual porous Si is removed from the seed wafer, which can then be recycled and put back into the ELTRAN® manufacturing process again and again. This is described in detail in the next section.

4. Seed Wafer Reusage

a. Cost Simulation

The basic ELTRAN® concept of 'split/recycle/reuse' involves reusage of the seed wafer. It can be seen from the ELTRAN® manufacturing process that the seed wafer itself is ultimately not used in any part of the SOI wafer. This is a special feature of ELTRAN® wafers not found in any other SOI wafers. This feature arises because 1) the seed wafer is not used as the handle wafer, and 2) the SOI layer comes from the epitaxial layer rather than from part of the seed wafer. The special features of SOI-Epi wafers™ come to the fore all the more due to this technique for reducing the manufacturing costs. Turning to the handle wafer, a new handle wafer is put into the manufacturing process each time an SOI wafer is produced; the epitaxial layer is also grown anew each time,

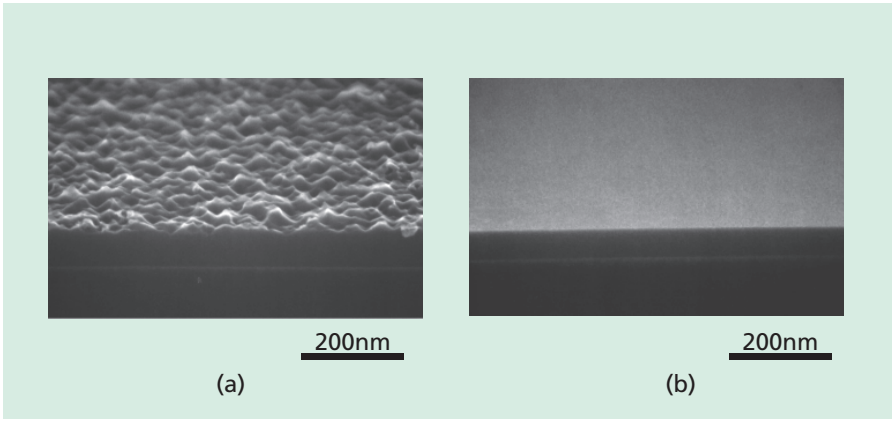

Fig.7 High-resolution, oblique-view micrographs of (a) as-etched ELTRAN® wafers and (b) H2-annealed ELTRAN® wafers.

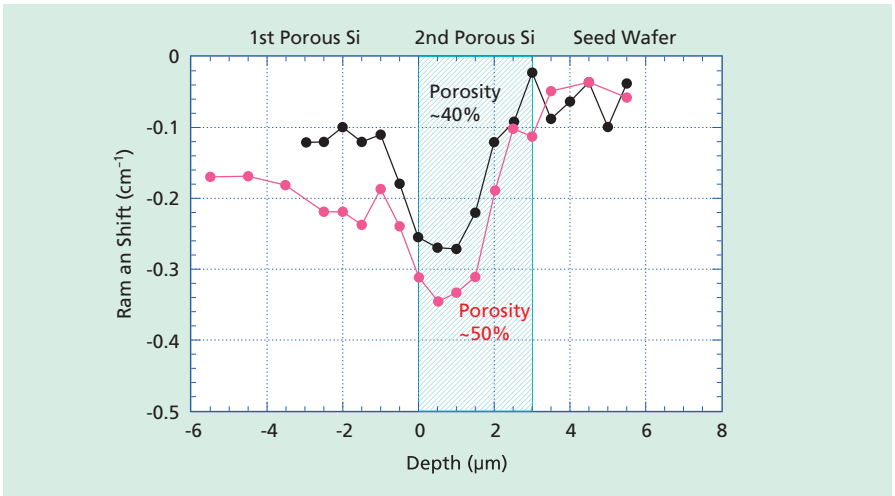

Fig.8 Raman shift depth profile around the 2nd porous Si with different porosity of 40% and 50% just before splitting.

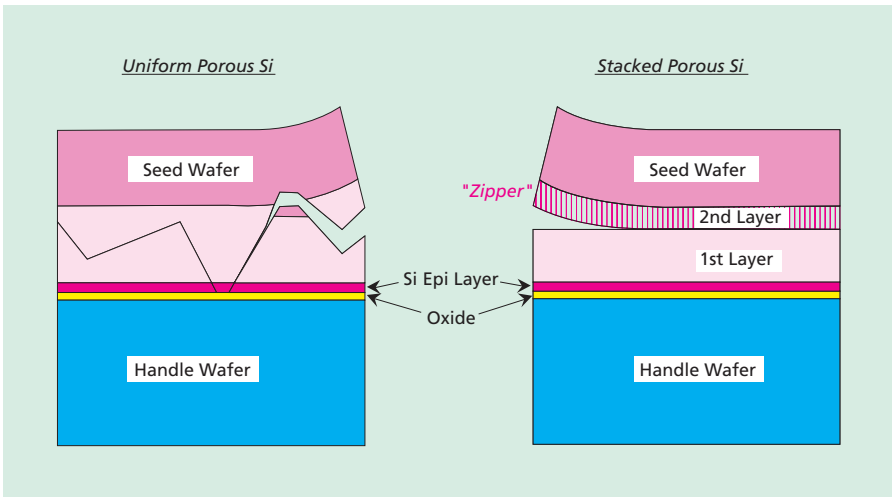

Fig.9 Schematic drawings of crack propagation in double- and single-layered porous Si.

and of course the thermally grown oxide film that becomes the BOX is formed anew each time by oxidizing the epitaxial layer. In this way, because each completed SOI wafer is always made entirely of new materials, there is no degradation in the product quality of the SOI wafers even if the seed wafer is reused again and again.

We next examine the extent of the reduction in wafer material costs due to this repeated reuse of the seed wafers. The following equation represents the wafer material costs when the ***'seed wafer reusage'*** concept is used[9].

$$Y = H + \frac{S + R \cdot (n-1)}{n} \qquad \text{(Eqn.1)}$$

Here, Y is the SOI wafer material cost, H is the price of the handle wafer, S is the price of the seed wafer, R is the price of reclaiming the seed wafer, and n is the number of times that the seed wafer is used.

As n increases, according to the above equation:

$$Y \longrightarrow H + R \qquad \text{(Eqn.2)}$$

In other words, the SOI wafer material cost becomes the price of the handle wafer plus the price of reclaiming the seed wafer, and the original price of the seed wafer is essentially irrelevant.

b. Double Porous Si Layers [9-11]

Raman spectroscopy was used to measure the strain around the second porous Si layer just before splitting for two wafers with second porous Si layers of different porosity (40% and 50%). The porosity of the first porous Si layer was the same for both wafers. The Raman shift depth-profiles observed in both wafers were similar (Fig. 8). It can be seen that the Raman shift showed a maximum negative value in the second porous Si layer close to the interface between the two layers. Moreover, this shift was larger in magnitude when the porosity of the second layer was the higher of the two values. The splitting plane corresponds to the position of maximum negative Raman shift in the depth direction. In other words, splitting occurs at the plane where the stress is at a maximum.

This shows that the porosity of the second porous Si layer is an extremely important factor in successfully restricting the splitting plane to be within a certain limited region. Figure 9 shows schematic drawings of the progression of the splitting plane for a single-layered porous Si of uniform porosity and double-layered porous Si comprising two layers of different porosity. Splitting can occur at any depth if the porosity is uniform throughout the porous Si layer, meaning that the progression of the splitting plane cannot be controlled and cracks may reach as far as the seed wafer or the epitaxial layer. With double-layered porous Si, however, splitting occurs close to the interface between the two layers. As a result, the layers act to protect the seed wafer and the epitaxial Si layer respectively, thus providing a definitive means for raising yield.

We next evaluated the stress values in the

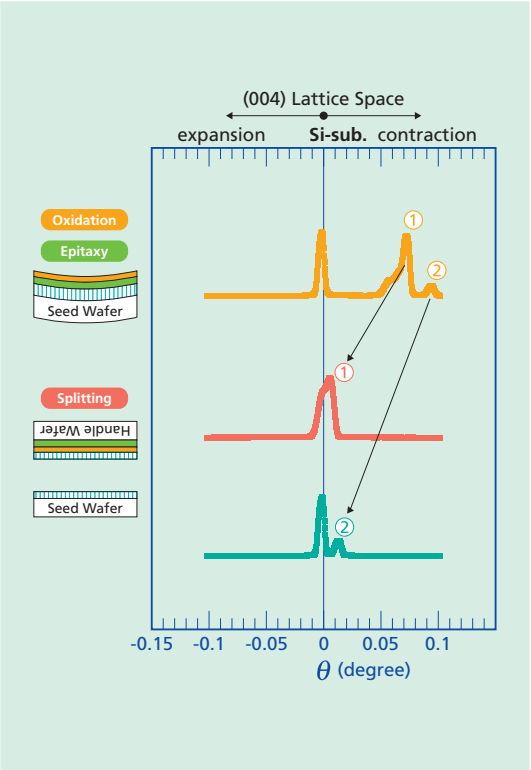

Fig.10 X-ray diffraction rocking curves of each wafer type before and after splitting processes.

two layers with the aim of understanding the splitting mechanism. Figure 10 shows the X-ray rocking curves before and after splitting. By splitting, the first and second porous Si layers go to the handle wafer side and the seed wafer side respectively. For both porous Si layers, the diffraction peak due to the layers approaches that of the respective substrate, showing that there is very little residual stress. It is thought that this is because the internal stress in each of the porous Si layers is released when the layers are split from one another and, as a result, the lattice strain is eased. It was found that after this release of stress, the 'in-plane stress' (here and in the following 'in-plane stress' refers to the stress in a plane parallel to the wafer surface) had dropped from 1.35×10^9 dyn/cm^2 to 1.31×10^8 dyn/cm^2 for the first layer and from 1.90×10^9 dyn/cm^2 to 2.88×10^8 dyn/cm^2 for the second layer.

The difference in stress between the first and second porous Si layers causes distortion in a confined region around the interface between the two, causing strain energy to accumulate and thus a high-energy state to be generated. Once splitting starts to occur in this region, the leading edge of the split progresses in such a way as to reduce the accumulated strain energy, and so the splitting plane remains close to the interface between the two layers. In other words, it is the 'force' to reduce this strain energy that is the 'driving force' that makes splitting progress uniformly with the splitting plane remaining close to the interface.

c. Water Jet Splitting[10,11,15)]

A water jet is used to split the bonded wafer near the interface between the first and second porous Si layers. We have tried a wide range of different splitting methods: thermal stress, oxidation from the edge of the porous Si, application of ultrasonic waves, insertion of a solid wedge, and insertion of a fluid wedge using a water jet. Of these methods, thermal stress had virtually no effect and oxidation caused serious warping of the wafer. With ultrasonic waves, splitting across the whole wafer was possible, but reproducibility and controllability were poor. Splitting across the whole wafer was also possible with both the solid wedge and the fluid wedge methods, but the use of a solid wedge caused wafer damage, as will be described in detail below. Considering the problems encountered with these methods, we decided to adopt the water jet method. It is thought that when the bonded wafer is split using a water jet, the primary mechanism is not cutting but rather peeling by the fluid wedge produced by the water jet. The setup we are currently using in actual practice involves a straight water jet designed for semiconductor manufacturing, in which only high-purity water may be used.

Splitting with a jet pressure of 20～60MPa is possible if the nozzle bore is designed to be 0.1mm. With this small a bore, however, the water hammer pressure is on the order of 0.24～0.43kgf, which is insufficient to cut through a Si wafer. This is why it is thought that the fluid wedge peeling effect is the dominant factor in the splitting of the bonded wafer. Due to the ability of a fluid to change its shape, the water jet penetrates as far as the periphery of the bonding interface and causes a buildup of pressure, meaning that the water hammer pressure is felt across a broad region of the wafer periphery. Unlike with a solid wedge, there is not a single point of contact with the wafer edge, and so splitting can take place without stress being concentrated in one particular place, meaning that cracking of the wafer periphery can be prevented.

In addition, with the solid wedge the mechanism is such that splitting is made to proceed by applying a force only to the wafer edge. This means that as the splitting proceeds, the wafer is forced to change shape excessively. This entails a risk of damage, in particular to the thin-film SOI layer and the buried oxide film layer. In the worst case, the wafer may even be broken during splitting. In contrast, with the water jet the mechanism is such that the wedge is constantly changing in shape, and thus pressure is exerted across the entire region where the splitting is proceeding. This means that the splitting can be made to proceed with virtually no deformation of the wafer. This will be an extremely advantageous feature when wafer diameters are increased to 300mm. For the reasons described above, we concluded that a water jet offered the optimum method for the bonded wafer splitting process, focusing on the ***'fluid wedge'*** effect of the water jet in reaching this decision.

Fig.11 Side-view photograph during splitting.

Table 1 ELTRAN® quality achieved (up to 3rd generation) by water jet splitting

	ELTRAN®	Water Jet		
		1st	2nd	3rd
Thickness (SOI/BOX) [nm]	100/100	100/100	100/100	100/100
LLS [/wafer]	21.0	19.4	32.8	21.4
Δt_{SOI} ±[%]	±2.37	±2.21	±2.68	±2.67
Δt_{BOX} ±[%]	±1.00	±1.08	±1.05	±0.80
Surface Roughness/Ra 1μm×1μm[nm]	0.107	0.106	0.101	0.121
HF Defect [cm^{-2}]	0.032	0.037	0.043	0.023
Secco Defect [cm^{-2}]	434	440	764	692

Since our wafers are disc-shaped, from the viewpoint of splitting process efficiency we decided to adopt a setup whereby the bonded wafer is clamped in a rotating holder and the water jet is projected while rotating the wafer. Figure 11 shows a photograph taken from the side during the splitting process. Due to the rotation, the splitting plane progresses in a spiral fashion. To control the progression of the splitting plane, the nozzle is gradually moved from the wafer periphery towards the center. This means that the splitting region can be prevented from progressing unnecessarily, and thus spiral splitting of high reproducibility can be achieved by incorporating a sequence whereby the nozzle is gradually moved towards the center of the wafer while controlling the splitting region.

The mass-production version of the water jet equipment (which uses the 'cassette-to-cassette' method) has been installed in the production line. The equipment consists of a wafer aligner, a wafer-flipping part, a wafer-cleaning part, a splitting chamber, a loader for loading the bonded wafers, two unloaders for the split wafers and a double-arm robot for transfering the wafers. The chamber contains a splitting part equipped with a rotating holder as described above. By combining such measures as high accuracy and cleanliness, it was possible to make the water jet splitting equipment such that it could withstand being used in the ELTRAN® manufacturing process.

Due to the precise control of the stress in the porous Si and the fluid wedge effect of the water jet described above, a bonded wafer splitting yield of a consistently high value was achieved even when each seed wafer was used three times, and in fact it has even become possible to use each seed wafer a fourth time.

5. Quality

Table 1 shows a list of parameters that are extremely important to the quality of SOI wafers and the corresponding values for ELTRAN® wafers. The ELTRAN® quality achieved in the past is shown along with that for three generations of ELTRAN® wafers made using the current splitting/recycling process. It can be seen that the numbers of HF defects for the three generations of wafers made using the current process (0.037, 0.043 and 0.023 /cm^2 respectively) are all under 0.05 /cm^2. Moreover, the numbers of secco-etch defects are 440, 764 and 692 /cm^2 respectively, which figures are comparable to those obtained in the past. It can thus be seen from the table that the quality of the ELTRAN® wafers produced using the current splitting/recycling process is by no means inferior to that achieved in the past. It can also be seen that there is no degradation in product quality even if splitting and recycling of the seed wafer is carried out repeatedly. This is due to the basic ***'seed wafer reusage'*** concept unique to ELTRAN®. Because ELTRAN® wafers, regardless of the generation, always consist of a handle wafer that is introduced into the manufacturing process anew every time and an epitaxial Si layer that is grown anew every time (along with an SiO_2 layer formed by thermal oxidation of the surface of this epitaxial Si layer), it has been possible to manufacture ELTRAN® wafers with a consistently high product quality.

Electrical properties using ELTRAN® wafers with such high qualities have been reported. For the ELTRAN® Epi-B-SOI wafer, a lifetime of a few hundred microseconds was obtained throughout the whole of the thin-film SOI layer, which value was much higher than those of other SOI wafers[18]. It has recently been reported that a ***"pure"*** 1/f noise characteristic is observed in partially depleted floating-body SOI-MOSFETs fabricated on ELTRAN® wafers, while floating-body induced pre-kink excess noise is found in devices formed on other commercially available bonded SOI wafers[19]. This difference is indicative of the higher quality of the ELTRAN® obtained by forming the surface and active SOI layers through epitaxial growth and hydrogen annealing.

6. Scalable Potential

We first reported that we had successfully smoothed our SOI wafers by hydrogen annealing to achieve a surface roughness comparable to that of commercially available Si wafers in 1994[3]. However, Si etching during the hydrogen annealing causes degradation of thickness uniformity in the SOI layer, and so it is necessary to restrict the amount of such etching. The etching rate is greatly affected by things like the equipment setup and the purity of the gas used. The use of a vertical-type annealing furnace holds the SOI layer thickness reduction during the hydrogen annealing to less than 1nm, and this makes it possible to manufacture SOI wafers with an extremely thin SOI layer (average thickness approximately 10 nm) having an excellent thickness uniformity of ±1.75nm. The SOI layer thickness uniformity is thus determined almost exclusively by that of the epitaxial Si layer, i.e. it remains more or less unchanged during the hydrogen annealing. The thickness uniformity of epitaxial Si layers produced by epitaxial reactors is being continually improved, due to the demands not only of SOI but of all Si processes, and it has been reported that film thickness uniformity of better than ±1% has been achieved with an epitaxial reactor designed for use with 300-mm Si wafers. It is expected that as wafers of increasingly larger diameters are produced, further improvements in thickness uniformity will be made.

As described above, ELTRAN® wafers are SOI-Epi wafers™ having the special feature of being COP-free, and their low HF defect density attests to this feature. Nevertheless, the number of HF defects increases when the HF solution permeates into any weak points in the SOI layer, and so it is expected that the number of such defects should vary according to

the thickness of the SOI layer. It has been confirmed that extremely high product quality of less than 0.05 HF defects/cm^2 is maintained for SOI layer thicknesses as low as 30nm[16]. This shows that we have already achieved product quality - in terms of both thickness uniformity and HF defect density - that will meet the needs of the new era of ultra-thin 20〜100nm films, this thickness range being the 2011 target indicated in the 2000 SIA-ITRS.

Device characteristics attesting to the excellent SOI layer thickness uniformity and high crystal product quality of ELTRAN® wafers have been reported in various journals and conferences[17]. For gate lengths of less than 0.1μm, ultra-thin (4nm) film MOSFETs can suppress threshold value roll-off and S-value degradation due to short channel effects. For this to be achieved, however, it is very important for ultra-thin films to be highly uniform in thickness.

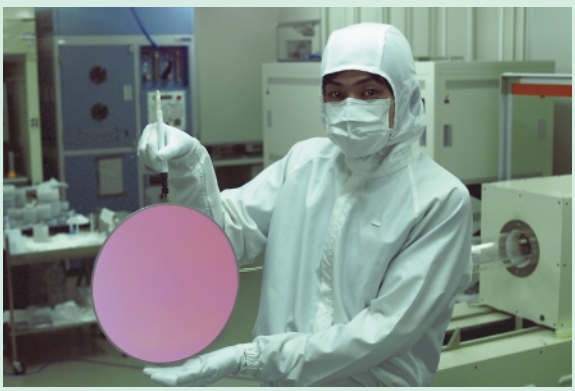

Fig.12 300mm-diameter ELTRAN® Wafer.

The usage of conventional equipment, i.e., an epitaxial reactor and an annealing furnace, means that the ELTRAN® manufacturing method can easily be applied to larger-diameter wafers. The anodization, bonding, splitting and etching equipment used in the manufacturing process, all of which we designed and developed ourselves, is now able to handle 300mm-diameter wafers. This has already been demonstrated by using it to manufacture 300mm ELTRAN® wafers (see Fig. 12). In manufacturing, moreover, we achieved thickness uniformity of 147nm±1.6nm[16], which is even better than that of our 200 mm wafers.

7. Summary

Since ELTRAN® wafers are COP-free SOI-Epi wafers™, they have an extremely low HF defect density. They also have SOI layers of highly uniform thickness, achieved through a combination of extremely good epitaxial Si layer thickness uniformity, selective etching of porous Si with remarkably high selectivity, and a dramatic reduction in the amount of Si etching that occurs during hydrogen annealing of the SOI surface. As a result, good thickness uniformity is achieved even in wafers with an SOI thickness of only 10 nm. We have successfully automated all of the ELTRAN® manufacturing equipment, and completed other preparations necessary for mass production. In so doing, we have achieved a consistent level of product quality. Moreover, we have determined that no new technical problems are incurred in applying the manufacturing process to 300mm-diameter wafers, because epitaxial-growth-based SOI technology can be adopted in existing and commonly used Si wafer manufacturing equipment.

In the future, to enable SOI to be widely used in mainstream CMOS and logic devices, analog devices, memories and systems on chips, we will need to achieve product quality comparable to that of conventional bulk and epitaxial wafers at a reasonable price-level so that sufficient device development can be carried out. At the same time, it will be necessary to allow for the risks associated with R&D activities and prior investment of SOI wafer producers. In other words, for the SOI market to expand, SOI wafer manufacturers and device manufacturers will need to join forces and work together to construct an effective mass production system. JSAP

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