Semiconductor Manufacturing Technology

Instructor's Manual

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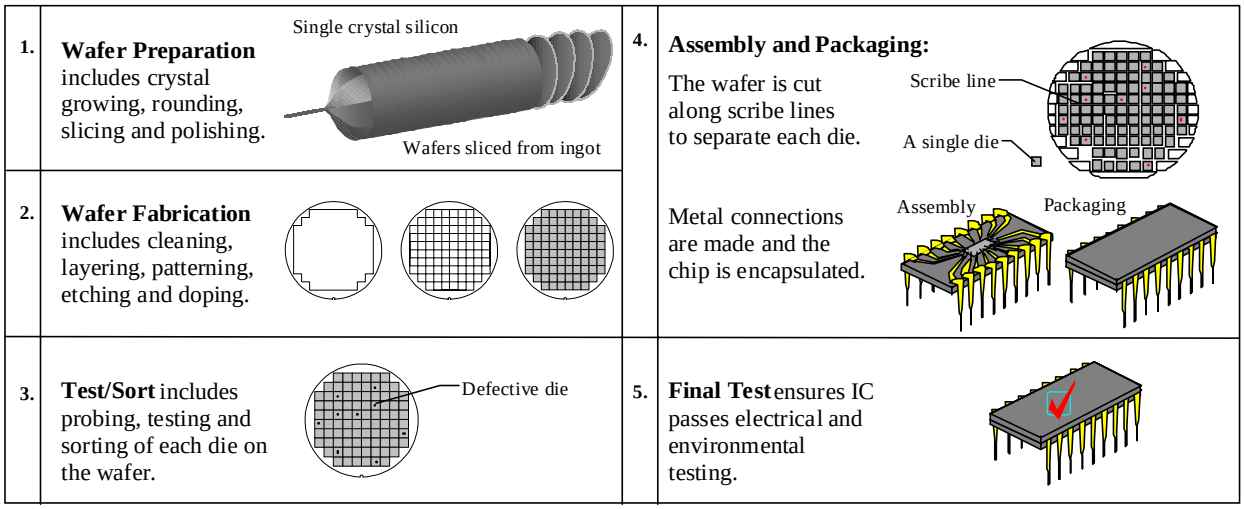
Notes to Instructors:

1) The chapter overview provides a concise summary of the main topics in each chapter.

2) The correct answer for each test bank question is highlighted in bold. Test bank questions are based on the end-of-chapter questions. If a student studies the end-of-chapter questions (which are linked to the italicized words in each chapter), then they will be successful on the test bank questions.

Chapter 1
Introduction to the Semiconductor Industry



Development of an Industry

- The roots of the electronic industry are based on the vacuum tube and early use of silicon for signal transmission prior to World War II. The first electronic computer, the ENIAC, was developed at the University of Pennsylvania during World War II.

- William Shockley, John Bardeen and Walter Brattain invented the solid-state transistor at Bell Telephone Laboratories on December 16, 1947. The semiconductor industry grew rapidly in the 1950s to commercialize the new transistor technology, with many early pioneers working in Silicon Valley in Northern California.

Circuit Integration

- The first integrated circuit, or IC, was independently co-invented by Jack Kilby at Texas Instruments and Robert Noyce at Fairchild Semiconductor in 1959. An IC integrates multiple electronic components on one substrate of silicon.

- Circuit integration eras are: small scale integration (SSI) with 2 - 50 components, medium scale integration (MSI) with 50 – 5k components, large scale integration (LSI) with 5k to 100k components, very large scale integration (VLSI) with 100k to 1M components, and ultra large scale integration (ULSI) with > 1M components.

IC Fabrication

- Chips (or die) are fabricated on a thin slice of silicon, known as a wafer (or substrate). Wafers are fabricated in a facility known as a wafer fab, or simply fab.

- The five stages of IC fabrication are:

    - Wafer preparation: silicon is purified and prepared into wafers.
    - Wafer fabrication: microchips are fabricated in a wafer fab by either a merchant chip supplier, captive chip producer, fabless company or foundry.
    - Wafer test: Each individual die is probed and electrically tested to sort for good or bad chips.
    - Assembly and packaging: Each individual die is assembled into its electronic package.
    - Final test: Each packaged IC undergoes final electrical test.

- Key semiconductor trends are:

    - Increase in chip performance through reduced critical dimensions (CD), more components per chip (Moore's law, which predicts the doubling of components every 18-24 months) and reduced power consumption.
    - Increase in chip reliability during usage.
    - Reduction in chip price, with an estimated price reduction of 100 million times for the 50 years prior to 1996.

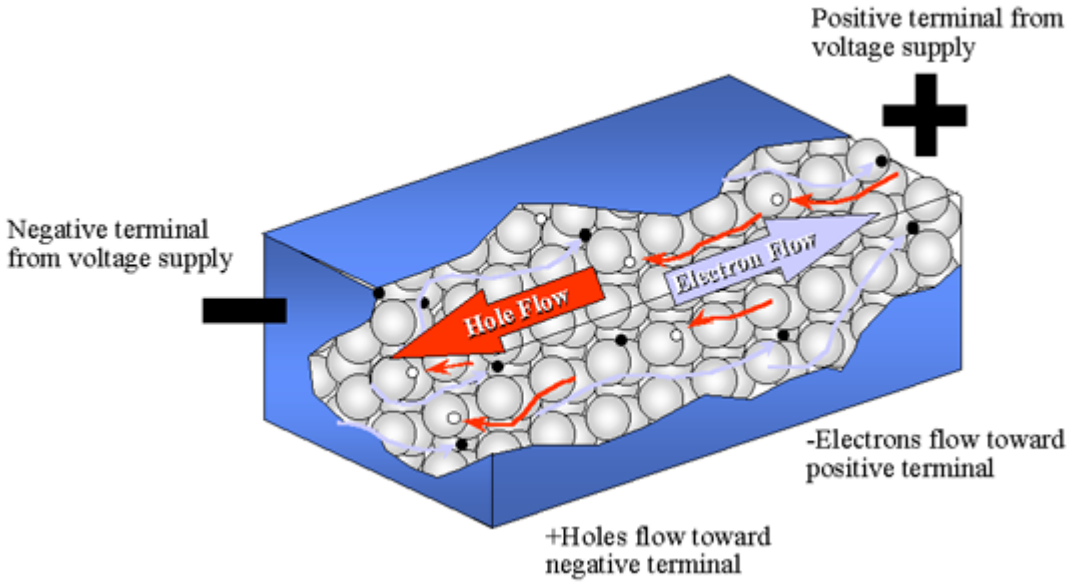
The Electronic Era

- The 1950s saw the development of many different types of transistor technology, and lead to the development of the silicon age.
- The 1960s were an era of process development to begin the integration of ICs, with many new chip-manufacturing companies.
- The 1970s were the era of medium-scale integration and saw increased competition in the industry, the development of the microprocessor and the development of equipment technology.
- The 1980s introduced automation into the wafer fab and improvements in manufacturing efficiency and product quality.
- The 1990s were the ULSI integration era with the volume production of a wide range of ICs with sub-micron geometries.

Career paths

- There are a wide range of career paths in semiconductor manufacturing, including technician, engineer and management.

Chapter 2
Characteristics of Semiconductor Materials



Atomic Structure

- The atomic model has three types of particles: neutral neutrons, positively charged protons in the nucleus and negatively charged electrons that orbit the nucleus. Outermost electrons are in the valence shell, and influence the chemical and physical properties of the atom. Ions form when an atom gains or loses one or more electrons.

The Periodic Table

- The periodic table lists all known elements. The group number of the periodic table represents the number of valence shell electrons of the element. We are primarily concerned with group numbers IA through VIIIA.

- Ionic bonds are formed when valence shell electrons are transferred from the atoms of one element to another. Unstable atoms (e.g., group VIIIA atoms because they lack one electron) easily form ionic bonds.

- Covalent bonds have atoms of different elements that share valence shell electrons.

Classifying Materials

- There are three difference classes of materials:
    - Conductors
    - Insulators
    - Semiconductors

- Conductor materials have low resistance to current flow, such as copper. Insulators have high resistance to current flow. Capacitance is the storage of electrical charge on two conductive plates separated by a dielectric material. The quality of the insulation material between the plates is the dielectric constant. Semiconductor materials can function as either a conductor or insulator.

Silicon

- Silicon is an elemental semiconductor material because of four valence shell electrons. It occurs in nature as silica and is refined and purified to make wafers.

- Pure silicon is intrinsic silicon. The silicon atoms bond together in covalent bonds, which defines many of silicon's properties. Silicon atoms bond together in set, repeatable patterns, referred to as a crystal.

- Germanium was the first semiconductor material used to make chips, but it was soon replaced by silicon. The reasons for this change are:
    - Abundance of silicon
    - Higher melting temperature for wider processing range
    - Wide temperature range during semiconductor usage
    - Natural growth of silicon dioxide

- Silicon dioxide (SiO_2) is a high quality, stable electrical insulator material that also serves as a good chemical barrier to protect silicon from external contaminants. The ability to grow stable, thin SiO_2 is fundamental to the fabrication of Metal-Oxide-Semiconductor (MOS) devices.

- Doping increases silicon conductivity by adding small amounts of other elements. Common dopant elements are from trivalent, p-type Group IIIA (boron) and pentavalent, n-type Group VA (phosphorus, arsenic and antimony).

- It is the junction between the n-type and p-type doped regions (referred to as a pn junction) that permit silicon to function as a semiconductor.

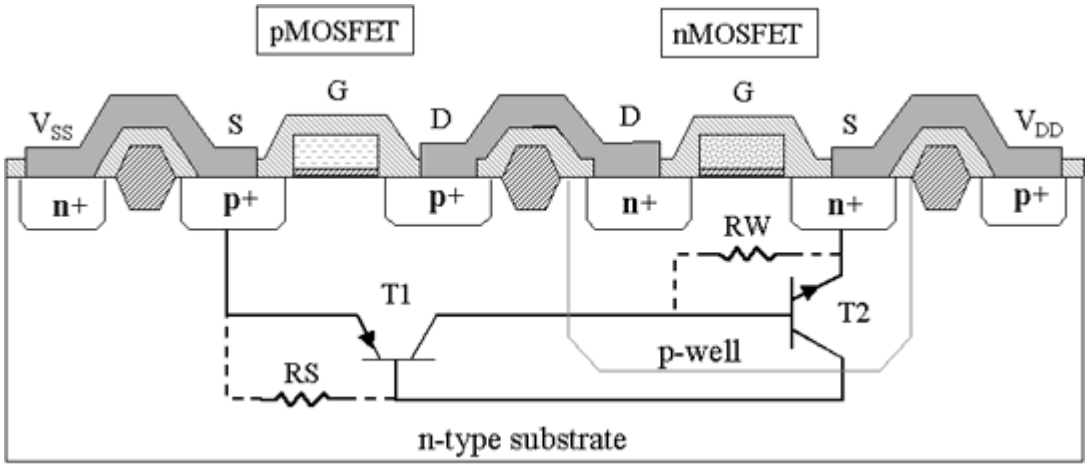
Alternative Semiconductor Materials

- The alternative semiconductor materials are primarily the compound semiconductors. They are formed from Group IIIA and Group VA (referred to as III-V compounds). An example is gallium arsenide (GaAs).

- Some alternative semiconductors come from Group IIA and VIA, referred to as II-VI compounds.

- GaAs is the most common III-V compound semiconductor material. GaAs ICs have greater electron mobility, and therefore are faster than ICs made with silicon. GaAs ICs also have higher radiation hardness than silicon, which is better for space and military applications. The primary disadvantage of GaAs is the lack of a natural oxide.

Chapter 3
Device Technologies



Circuit Types

- There are two basic types of circuits: analog and digital. Analog circuits have electrical data that varies continuously over a range of voltage, current and power values. Digital circuits have operating signals that vary about two distinct voltage levels – a high and a low.

Passive Component Structures

- Passive components such as resistors and capacitors conduct electrical current regardless of how the component is connected. IC resistors are a passive component. They can have unwanted resistance known as parasitic resistance. IC capacitor structures can also have unintentional capacitance

Active Component Structures

- Active components, such as diodes and transistors can be used to control the direction of current flow. PN junction diodes are formed when there is a region of n-type semiconductor adjacent to a region of p-type semiconductor. A difference in charge at the pn junction creates a depletion region that results in a barrier voltage that must be overcome before a diode can be operated. A bias voltage can be configured to have a reverse bias, with little or no conduction through the diode, or with a forward bias, which permits current flow.

- The bipolar junction transistor (BJT) has three electrodes and two pn junctions. A BJT is configured as an npn or pnp transistor and biased for conduction mode. It is a current-amplifying device.

- A schottky diode is formed when metal is brought in contact with a lightly doped n-type semiconductor material. This diode is used in faster and more power efficient BJT circuits.

- The field-effect transistor (FET), a voltage-amplifying device, is more compact and power efficient than BJT devices. A thin gate oxide located between the other two electrodes of the transistor insulates the gate on the MOSFET. There are two categories of MOSFETs, nMOS (n-channel) and pMOS (p-channel), each which is defined by its majority current carriers. There is a biasing scheme for operating each type of MOSFET in conduction mode.

- For many years, nMOS transistors have been the choice of most IC manufacturers. CMOS, with both nMOS and pMOS transistors in the same IC, has been the most popular device technology since the early 1980s.

- BiCMOS technology makes use of the best features of both CMOS and bipolar technology in the same IC device.

- Another way to categorize FETs is in terms of enhancement mode and depletion mode. The major different is in the way the channels are doped: enhancement-mode channels are doped opposite in polarity to the source and drain regions, whereas depletion mode channels are doped the same as their respective source and drain regions.

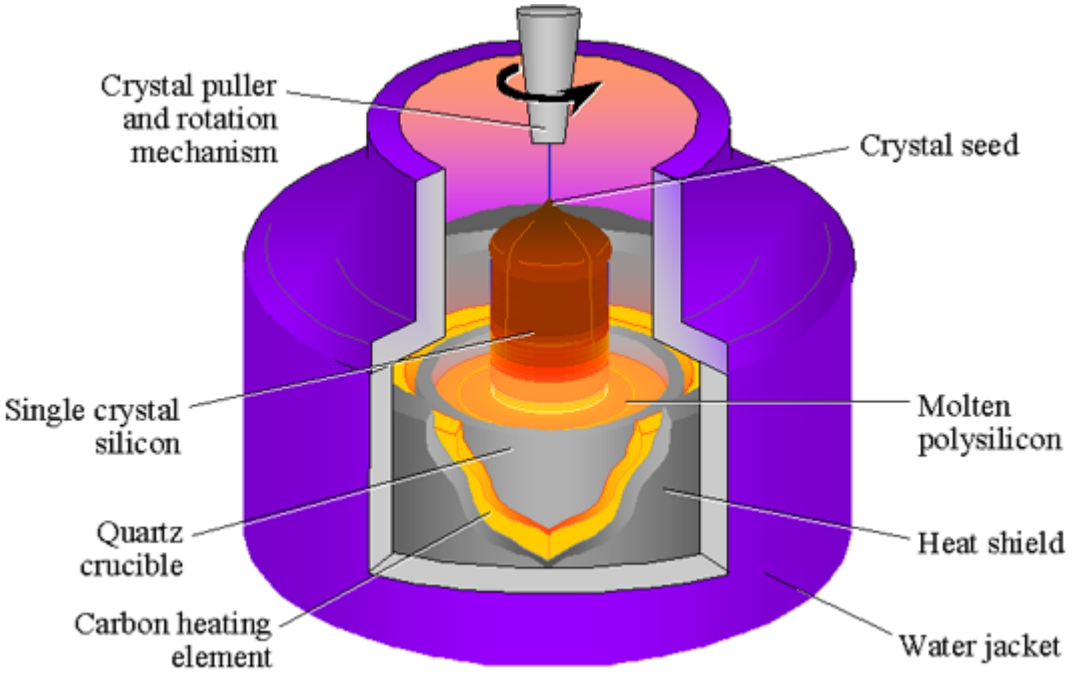
Latchup in CMOS Devices

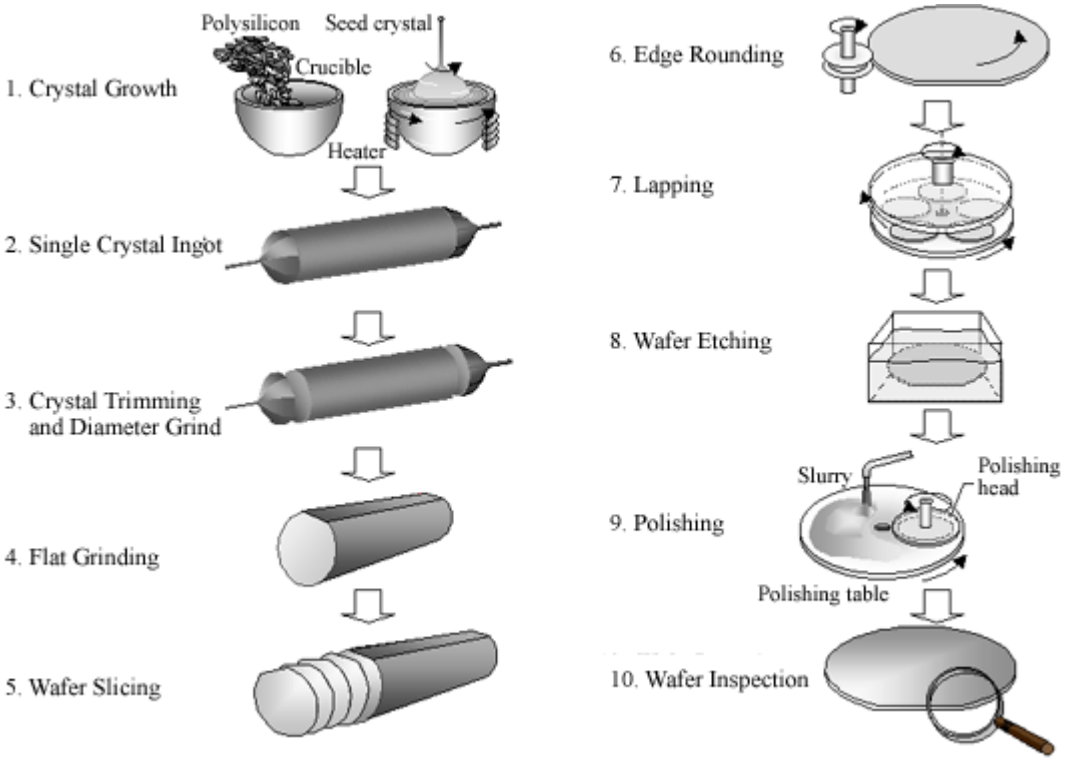
- Parasitic transistors can create a latchup condition in CMOS ICs that causes transistors to unintentionally turn on. To control latchup, an epitaxial layer is grown on the wafer surface and an isolation barrier is placed between the transistors. An isolation layer can also be buried deep below the transistors.

Integrated Circuit Products

- There are a wide range of semiconductor ICs found in electrical and electronic products. This includes the linear IC family, which operates primarily with analog circuit applications, and the digital IC family, which includes devices that operate with binary bits of data signals.

Chapter 4
Silicon and Wafer Preparation





Semiconductor-Grade Silicon

- The highly refined silicon used for wafer fabrication is termed semiconductor-grade silicon (SGS), and sometimes referred to as electronic-grade silicon. The ultra-high purity of semiconductor-grade silicon is obtained from a multi-step process referred to as the Siemens process.

Crystal Structure

- A crystal is a solid material with an ordered, 3-dimensional pattern over a long range. This is different from an amorphous material that lacks a repetitive structure.

- The unit cell is the most fundamental entity for the long-range order found in crystals. The silicon unit cell is a face-centered cubic diamond structure. Unit cells can be organized in a non-regular arrangement, known as a polycrystal. A monocrystal are neatly arranged unit cells.

Crystal Orientation

- The orientation of unit cells in a crystal is described by a set of numbers known as Miller indices. The most common crystal planes on a wafer are (100), (110), and (111). Wafers with a (100) crystal plane orientation are most common for MOS devices, whereas (111) is most common for bipolar devices.

Monocrystal Silicon Growth

- Silicon monocrystal ingots are grown with the Czochralski (CZ) method to achieve the correct crystal orientation and doping. A CZ crystal puller is used to grow the silicon ingots. Chunks of silicon are heated in a crucible in the furnace of the puller, while a perfect silicon crystal seed is used to start the new crystal structure.

- A pull process serves to precisely replicate the seed structure. The main parameters during the ingot growth are pull rate and crystal rotation. More homogeneous crystals are achieved with a magnetic field around the silicon melt, known as magnetic CZ.

- Dopant material is added to the melt to dope the silicon ingot to the desired electrical resistivity. Impurities are controlled during ingot growth. A float-zone crystal growth method is used to achieve high-purity silicon with lower oxygen content.

- Large-diameter ingots are grown today, with a transition underway to produce 300-mm ingot diameters. There are cost benefits for larger diameter wafers, including more die produced on a single wafer.

Crystal Defects in Silicon

- Crystal defects are interruptions in the repetitive nature of the unit cell. Defect density is the number of defects per square centimeter of wafer surface.

- Three general types of crystal defects are: 1) point defects, 2) dislocations, and 3) gross defects. Point defects are vacancies (or voids), interstitial (an atom located in a void) and Frenkel defects, where an atom leaves its lattice site and positions itself in a void. A form of dislocation is a stacking fault, which is due to layer stacking errors. Oxygen-induced stacking faults are induced following thermal oxidation. Gross defects are related to the crystal structure (often occurring during crystal growth).

Wafer Preparation

- The cylindrical, single-crystal ingot undergoes a series of process steps to create wafers, including machining operations, chemical operations, surface polishing and quality checks.

- The first wafer preparation steps are the shaping operations: end removal, diameter grinding, and wafer flat or notch. Once these are complete, the ingot undergoes wafer slicing, followed by wafer lapping to remove mechanical damage and an edge contour. Wafer etching is done to chemically remove damage and contamination, followed by polishing. The final steps are cleaning, wafer evaluation and packaging.

Quality Measures

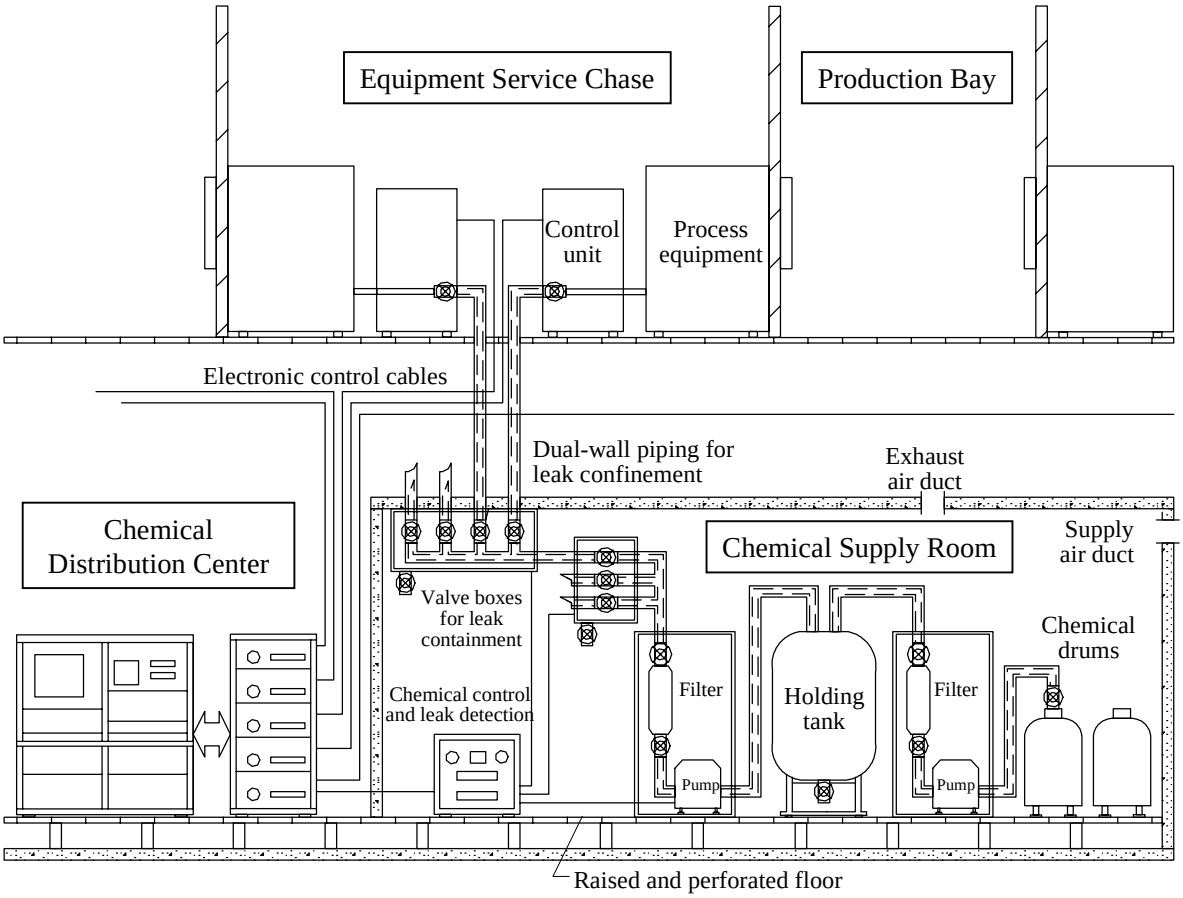
- Wafer suppliers must produce wafers to stringent quality requirements, including:

    - Physical dimensions: actual dimensions of the wafer (e.g., thickness, etc.).
    - Flatness: linear thickness variation across the wafer.
    - Microroughness: peaks and valleys found on the wafer surface.
    - Oxygen content: excessive oxygen can affect mechanical and electrical properties.
    - Crystal defects: must be minimized for optimum wafer quality.
    - Particles: controlled to minimize yield loss during wafer fabrication.
    - Bulk resistivity: uniform resistivity from doping during crystal growth is critical.

Epitaxial Layer

- An epitaxial layer (or epi layer) is grown on the wafer surface to achieve the same single crystal structure of the wafer with control over doping type of the epi layer. Epitaxy minimizes latch-up problems as device geometries continue to shrink.

Chapter 5
Chemicals in Semiconductor Fabrication



States of Matter

- Matter in the universe exists in 3 basic states: solid, liquid and gas. A fourth state is plasma.

Properties of Materials

- Material properties are the physical and chemical characteristics that describe its unique identity.

- Different properties for chemicals in semiconductor manufacturing are: temperature, pressure and vacuum, condensation, vapor pressure, sublimation and deposition, density, surface tension, thermal expansion and stress.

    - Temperature is a measure of how hot or cold a substance is relative to another substance.
    - Pressure is the force exerted per unit area. Vacuum is the removal of gas molecules.
    - Condensation is the process of changing a gas into a liquid. Vaporization is changing a liquid into a gas.
    - Vapor pressure is the pressure exerted by a vapor in a closed container at equilibrium.
    - Sublimation is the process of changing a solid directly into a gas. Deposition is changing a gas into a solid.
    - Density is the mass of a substance divided by its volume.
    - Surface tension of a liquid is the energy required to increase the surface area of contact.
    - Thermal expansion is the increase in an object's dimension due to heating.
    - Stress occurs when an object is exposed to a force.

Process Chemicals

- Semiconductor manufacturing requires extensive chemicals.

- A chemical solution is a chemical mixture. The solvent is the component of the solution present in larger amount. The dissolved substances are the solutes.

- Acids are solutions that contain hydrogen and dissociate in water to yield hydronium ions. A base is a substance that contains the OH chemical group and dissociates in water to yield the hydroxide ion, OH^-.

- The pH scale is used to assess the strength of a solution as an acid or base. The pH scale varies from 0 to 14, with 7 being the neutral point. Acids have pH below 7 and bases have pH values above 7.

- A solvent is a substance capable of dissolving another substance to form a solution.

- A bulk chemical distribution (BCD) system is often used to deliver liquid chemicals to the process tools. Some chemicals are not suitable for BCD and instead use point-of-use (POU) delivery, which means they are stored and used at the process station.

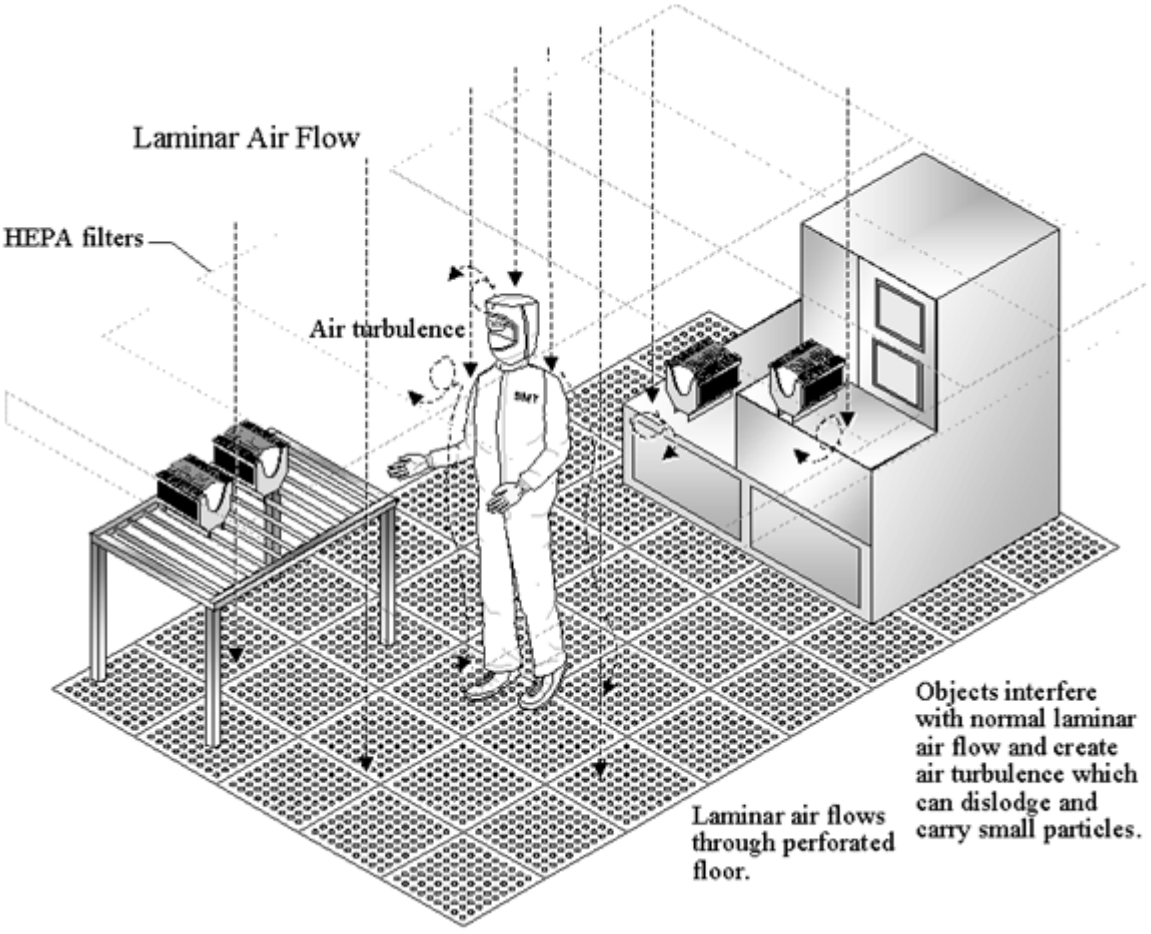
- Gases are generally categorized as bulk gases or specialty gases. Bulk gases are the relatively simple gases to manufacture and are traditionally oxygen, nitrogen, hydrogen, helium and argon. The specialty gases, or process gases, are other important gases used in a wafer fab, and usually supplied in low volume.

- Specialty gases are usually transported to the fab in metal cylinders.

- The local gas distribution system requires a gas purge to flush out undesirable residual gas. Gas delivery systems have special piping and connections systems. A gas stick controls the incoming gas at the process tool.

- Specialty gases may be classified as hydrides, fluorinated compounds or acid gases.

Chapter 6
Contamination Control in Wafer Fabs



Introduction

- Modern semiconductor manufacturing is performed in a cleanroom, isolated from the outside environment and contaminants.

Types of contamination

- Cleanroom contamination has five categories: particles, metallic impurities, organic contamination, native oxides and electrostatic discharge. Killer defects are those causes of failure where the chip fails during electrical test.
    - Particles: objects that adhere to a wafer surface and cause yield loss. A particle is a killer defect if it is greater than one-half the minimum device feature size.

- Metallic impurities: the alkali metals found in common chemicals. Metallic ions are highly mobile and referred to as mobile ionic contaminants (MICs).
- Organic contamination: contains carbon, such as lubricants and bacteria.
- Native oxides: thin layer of oxide growth on the wafer surface due to exposure to air.
- Electrostatic discharge (ESD): uncontrolled transfer of static charge that can damage the microchip.

Sources and Control of Contamination

- The sources of contamination in a wafer fab are: air, humans, facility, water, process chemicals, process gases and production equipment.

  - Air: class number designates the air quality inside a cleanroom by defining the particle size and density.
  - Humans: a human is a particle generator. Humans wear a cleanroom garment and follow cleanroom protocol to minimize contamination.
  - Facility: the layout is generally done as a ballroom (open space) or bay and chase design. Laminar airflow with air filtering is used to minimize particles. Electrostatic discharge is controlled by static-dissipative materials, grounding and air ionization.
  - Ultrapure deiniozed (DI) water: Unacceptable contaminants are removed from DI water through filtration to maintain a resistivity of 18 megohm-cm. The zeta potential represents a charge on fine particles in water, which are trapped by a special filter. UV lamps are used for bacterial sterilization.
  - Process chemicals: filtered to be free of contamination, either by particle filtration, microfiltration (membrane filter), ultrafiltration and reverse osmosis (or hyperfiltration).
  - Process gases: filtered to achieve ultraclean gas.
  - Production equipment: a significant source of particles in a fab.
  - Workstation design: a common layout is bulkhead equipment, where the major equipment is located behind the production bay in the service chase. Wafer handling is done with robotic wafer handlers. A minienvironment is a localized environment where wafers are transferred on a pod and isolated from contamination.

Wafer Wet Cleaning

- The predominant wafer surface cleaning process is with wet chemistry. The industry standard wet-clean process is the RCA clean, consisting of standard clean 1 (SC-1) and standard clean 2 (SC-2).

- SC-1 is a mixture of ammonium hydroxide, hydrogen peroxide and DI water and capable of removing particles and organic materials. For particles, removal is primarily through oxidation of the particle or electric repulsion.

- SC-2 is a mixture of hydrochloric acid, hydrogen peroxide and DI water and used to remove metals from the wafer surface.

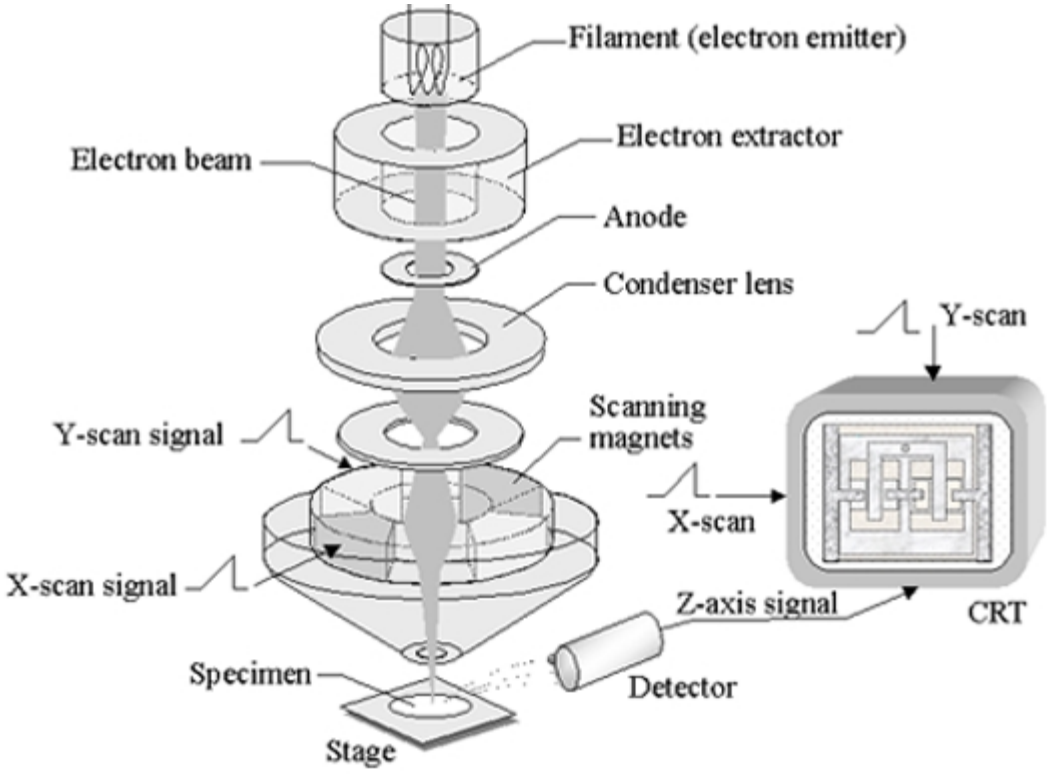
- RCA clean has been modified with diluted cleaning chemistries. The piranha cleaning mixture combines sulfuric acid and hydrogen peroxide to remove organic and metallic impurities. Many cleaning steps include an HF last step to remove native oxide.

- Megasonics is widely used for wet cleaning. It has ultrasonic energy with frequencies near 1 MHz. Spray cleaning will spray wet-cleaning chemicals onto the wafer. Scrubbing is an effective method for removing particles from the wafer surface.

- Wafer rinse is done with overflow rinse, dump rinse and spray rinse. Wafer drying is done with spin dryer or IPA vapor dry (isopropyl alcohol).

- Some alternatives to RCA clean are dry cleaning, such as with plasma-based cleaning, ozone and cryogenic aerosol cleaning.

Chapter 7
Metrology and Defect Inspection



IC Metrology

- In a wafer fab, metrology refers to the techniques and procedures for determining physical and electrical properties of the wafer.

- In-process data has traditionally been collected on monitor wafers. Measurement equipment is either stand-alone or integrated.

- Yield is the percent of good parts produced out of the total group of parts started. It is an indicator of the health of the fabrication process.

Quality Measures

- Semiconductor quality measures define the requirements for specific aspects of wafer fabrication to ensure acceptable device performance.

- Film thickness is generally divided into the measurement of opaque film or transparent film. Sheet resistance measured with a four-point probe is a common

method of measuring opaque films (e.g., metal film). A contour map shows sheet resistance deviations across the wafer surface.

- Ellipsometry is a nondestructive, noncontact measurement technique for transparent films. It works based on linearly polarized light that reflects off the sample and is elliptically polarized.

- Reflectometry is used to measure a film thickness based on how light reflects off the top and bottom surface of the film layer. X-ray and photoacoustic technology are also used to measure film thickness.

- Film stress is measured by analyzing changes in the radius of curvature of the wafer. Variations in the refractive index are used to highlight contamination in the film.

- Dopant concentration is traditionally measured with a four-point probe. The latest technology is the thermal-wave system, which measures the lattice damage in the implanted wafer after ion implantation. Another method for measuring dopant concentration is spreading resistance probe.

- Brightfield detection is the traditional light source for microscope equipment. An optical microscope uses light reflection to detect surface defects. Darkfield detection examines light scattered off defects on the wafer surface. Light scattering uses darkfield detection to detect surface particles by illuminating the surface with laser light and then using optical imaging.

- Critical dimensions (CDs) are measured to achieve precise control over feature size dimensions. The scanning electron microscope is often used to measure CDs.

- Conformal step coverage is measured with a surface profiler that has a stylus tip.

- Overlay registration measures the ability to accurately print photoresist patterns over a previously etched pattern.

- Capacitance-voltage (C-V) test is used to verify acceptable charge conditions and cleanliness at the gate structure in a MOS device.

Analytical Equipment

- The secondary-ion mass spectrometry (SIMS) is a method of eroding a wafer surface with accelerated ions in a magnetic field to analyze the surface material composition.

- The atomic force microscope (AFM) is a surface profiler that scans a small, counterbalanced tip probe over the wafer to create a 3-D surface map.

- Auger electron spectroscopy (AES) measures composition on the wafer surface by measuring the energy of the auger electrons. It identifies elements to a depth of about

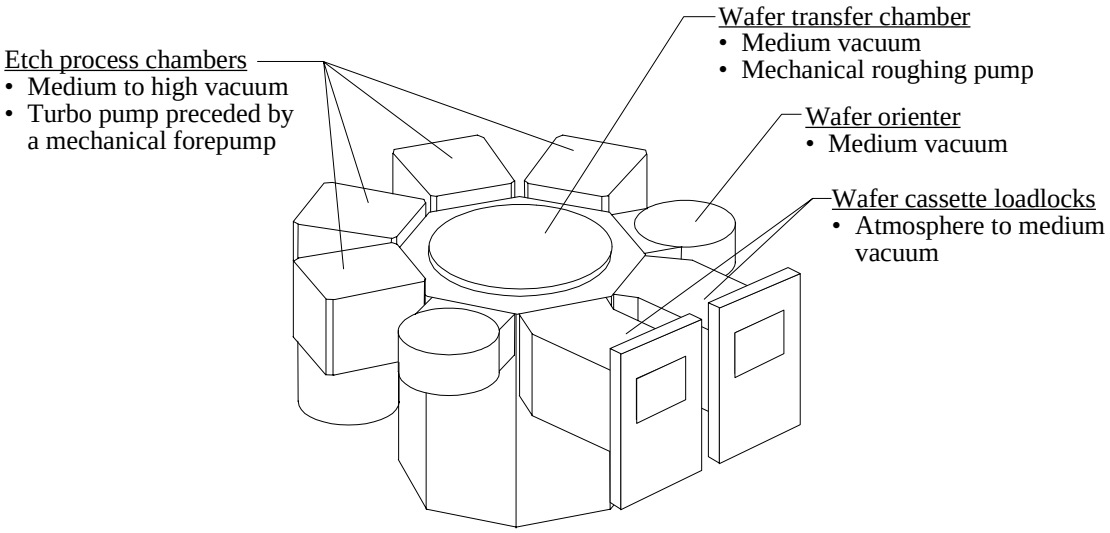
2 nm. Another instrument used to identify surface chemical species is X-ray photoelectron spectroscopy (XPS).

- Transmission electron microscopy (TEM) uses a beam of electrons that is transmitted through a thin slice of the wafer. It is capable of quantifying very small features on a wafer, such as silicon crystal point defects.

- Energy-dispersive spectrometer (EDX) is a widely used X-ray detection method for identifying elements. It is often used in conjunction with the SEM.

- A focused ion beam (FIB) system is a destructive technique that focuses a beam of ions on the wafer to carve a thin cross section from any wafer area. This permits analysis of the wafer material.

Chapter 8
Gas Control in Process Chambers



- The process chamber is a controlled vacuum environment where intended chemical reactions take place under controlled conditions. Process chambers are often configured as a cluster tool.

Vacuum

- Vacuum ranges are low (rough) vacuum, medium vacuum, high vacuum and ultrahigh vacuum (UHV). When pressure is lowered in a vacuum, the mean free path increases, which is important for how gases flow through the system and for creating a plasma.

Vacuum Pumps

- Roughing pumps are used to achieve a low to medium vacuum and to exhaust a high vacuum pump. High vacuum pumps achieve a high to ultrahigh vacuum.

- Roughing pumps are dry mechanical pumps or a blower pump (also referred to as a booster). Two common high vacuum pumps are a turbomolecular (turbo) pump and cryopump. The turbo pump is a reliable, clean pump that works on the principle of mechanical compression. The cryopump is a capture pump that removes gases from the process chamber by freezing them.

Process Chamber Gas Flow

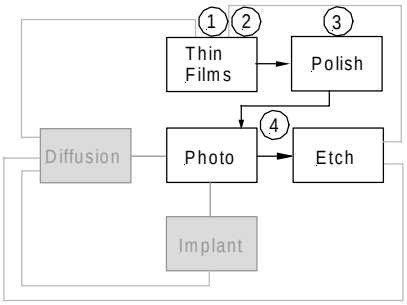
- The flow of gas into the process chamber is critical to attain the desired chemical reaction. Gas flow is controlled with the use of a mass flow controller (MFC). An MFC measures the mass flow rate instead of only controlling gas flow by volume.

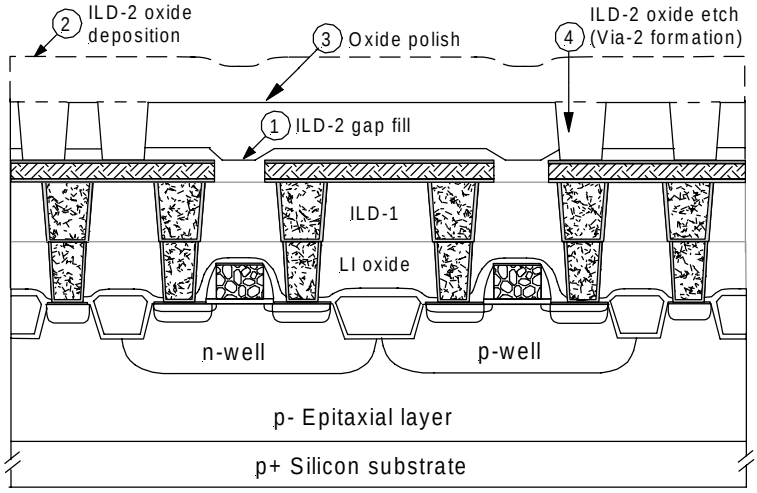
- A residual gas analyzer (RGA) identifies the types of gas molecules remaining in an evacuated system.

Plasma

- Plasma is a neutral, highly energized, ionized gas. It is used at various process steps in wafer fabrication because it supplies the energy needed to support a gas reaction near the wafer surface in a process chamber. The most common method to create a plasma glow discharge is with AC power in the radio frequency (RF) range.

Chapter 9
IC Fabrication Process Overview





CMOS Process Flow

- CMOS technology is a popular process and is used to describe the wafer fabrication process. The major process areas are:

    - Diffusion: area in the fab where high-temperature processing and film depositions are performed.
    - Photolithography: an image of a circuit pattern is transferred from a reticle to a photoresist pattern on the wafer surface.
    - Etch: where a permanent pattern on the wafer is created in areas not protected by the photoresist pattern.
    - Ion implanter: the most popular tool for doping wafers.
    - Thin films: the deposition of dielectric and metal layers on the wafer surface. Polish is the fab area where the top surface of the wafer is planarized by lowering the high topography.

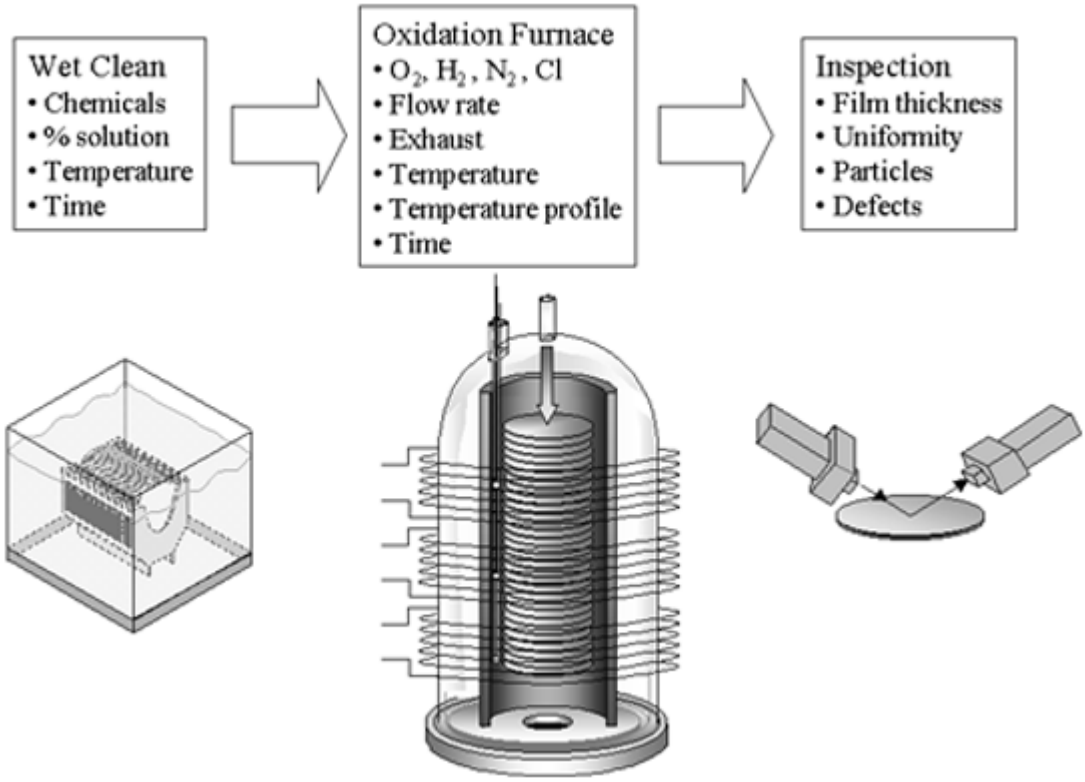
CMOS Manufacturing Steps

The CMOS manufacturing steps described are:

- Twin well process: defines the active regions of the nMOS and pMOS transistors.
- Shallow trench isolation process: creates isolation regions between active transistors.
- Poly gate structure process: formation of the polysilicon gate.

- Lightly doped drain implant process: implant process for shallow junctions and short channel length.
- Sidewall spacer formation: spacers along polysilicon gates to define edge of source/drain implants.
- Source/drain (S/D) implant process: formation of source and drain by ion implant.
- Contact formation: forms metal contacts on active regions.
- Local interconnect (LI) process: forms metal connecting lines between transistors.
- Via-1 and plug-1 formation: electrical connections to first metal layer.
- Metal-1 interconnect formation: deposition of three-layer metal film.
- Via-2 and Plug-2 formation: forms electrical connections from metal-1 to metal-2.
- Metal-2 interconnect formation: deposit metal-2 and form interconnections.
- Metal-3 to pad etch and alloy: formation of metal-3 and all following layers up to bond pads.
- Parametric testing: in-line testing and wafer sort.

Chapter 10
Oxidation



Introduction

- A grown oxide layer occurs on a wafer by providing high-purity oxygen in an elevated-temperature environment. A deposited oxide layer is formed on a wafer by reacting an external silicon source with oxygen to deposit a thin film.

Oxide Film

- An amorphous silicon dioxide film grows on a wafer with an atomic structure of a silicon atom surrounded by four oxygen atoms (tetrahedron cell). Thermally grown SiO_2 has strong adhesion to silicon and has excellent dielectric properties.

- Silicon dioxide is used in the following applications: 1) device scratch protection and contamination isolation, 2) field isolation (surface passivation), 3) gate dielectric material, 4) doping barrier, and 5) deposited dielectric layer between metal conductor layers.

Thermal Oxidation Growth

- Thermal oxide is grown by a chemical reaction between silicon and oxygen. This is done with dry oxidation or wet oxidation. Wet oxidation has a faster growth rate but the layer is less dense.

- Silicon dioxide grows by consuming silicon. The thickness of silicon consumed is 0.46 of the total oxide thickness. The growth of the oxidation layer is controlled and limited by the movement of oxygen through the oxide at the oxide-silicon interface. This oxide-silicon interface has an incomplete oxidation of silicon that causes an undesirable charge build-up that must be controlled. Use of a chlorine-containing gas during the oxidation process can neutralize the charge accumulation at the interface.

- The rate of oxidation growth has both a linear stage and parabolic stage. The linear stage is the initial growth (up to about 150 angstroms) and consumes silicon on the wafer surface as a linear function of time. This stage is reaction-rate controlled. The parabolic stage is the second phase and is much slower. This second phase is diffusion controlled (limited by the rate the oxygen diffuses through the oxide).

- Factors that affect oxide growth are: heavily doped silicon has increased oxidation, the (111) crystal oxidizes faster in the linear stage than the (100) crystal, increased pressure causes increased growth, and plasma can enhance oxidation.

- The selective oxidation of silicon is done to electrically isolate adjacent devices. The local oxidation of silicon (LOCOS) is the traditional method, but it has excessive lateral growth and is inadequate for 0.25 μm technology and below. Shallow trench isolation (STI) is the preferred method for device isolation in advanced wafer fabs.

Furnace Equipment

- The three types of furnace equipment are: horizontal furnace, vertical furnace and rapid thermal processor (RTP). The vertical furnace replaced the horizontal furnace in the 1990s as the primary furnace used in batch processing. The rapid thermal processor is a single-wafer system that has extremely rapid localized heating on the wafer surface.

Horizontal versus Vertical Furnaces

- The vertical furnace has many performance advantages over the horizontal furnace, including smaller footprint, parallel processing for throughput increase and improved gas flow dynamics.

- The five major control systems for a vertical furnace are: 1) process chamber, 2) wafer transfer system, 3) gas distribution system, 4) exhaust system and 5) temperature control system. High-temperature furnace materials are made of

amorphous quartz (referred to as quartzware) or silicon carbide. Furnaces have multiple heat zones with a sophisticated temperature control system based on multiple thermocouples. A typical ramp rate for a vertical furnace is 10°C/minute.

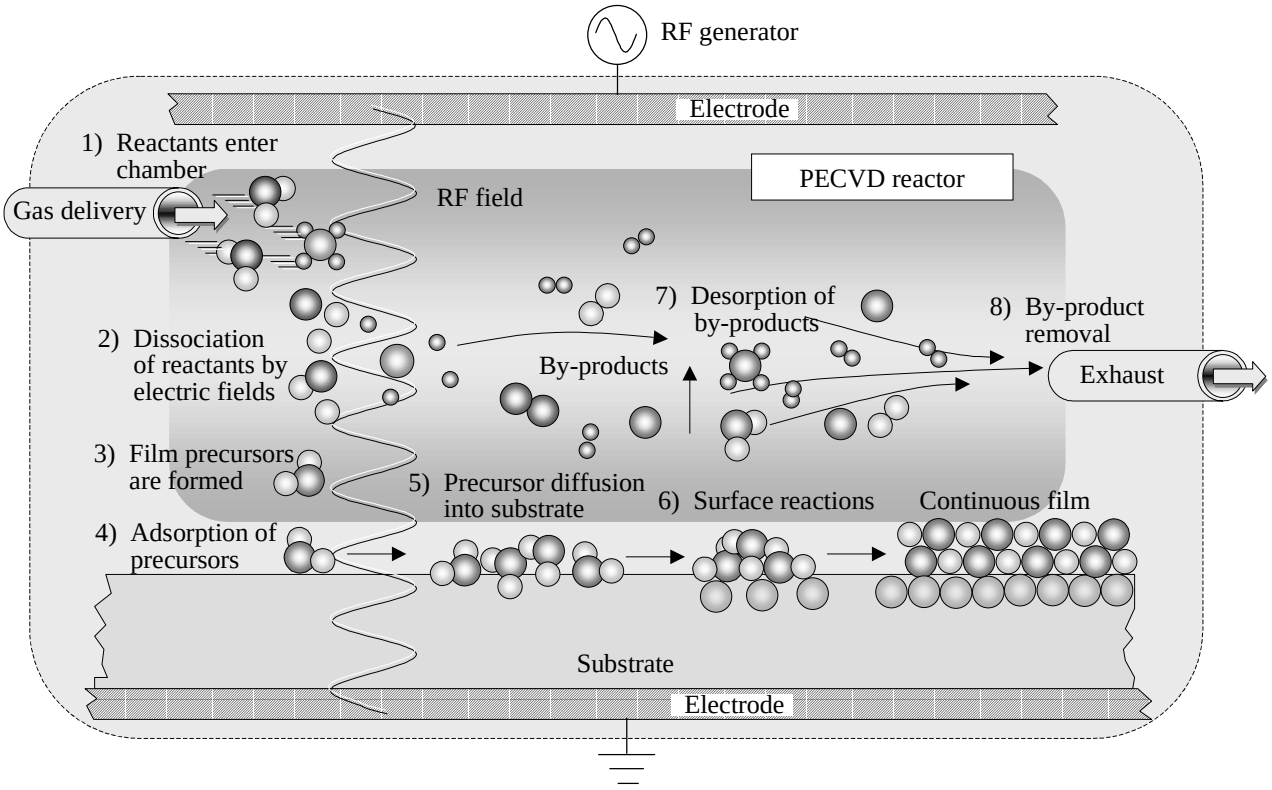
- A fast ramp vertical furnace is able to quickly raise the temperature of a batch of wafers, with a ramp rate up to 100°C/minute. A fast ramp vertical furnace has improved temperature control and thermal uniformity across the wafers.

- The rapid thermal processor (RTP) heats a single wafer to a temperature range of 400 to1300°C within a fraction of a second. Advantages are a reduced thermal budget, minimized dopant movement and shorter time to process a wafer. RTPs are cold wall systems that often use multiple tungsten halogen lamps for heating and an optical pyrometer for temperature measurement. Examples of RTP applications are implant anneal, densification of deposited films and silicide formation.

Oxidation Process

- The type of oxidation process at a particular wafer fab step depends on the oxide layer thickness and properties. Cleaning prior to oxidation is critical. A process recipe is loaded into the high-temperature furnace to control the oxidation parameters.

Chapter 11
Deposition



Film Deposition

- Multilevel metallization refers to the metal and dielectric layers needed to interconnect devices on the wafer. Aluminum metallization has been the traditional interconnect metal. The interlayer dielectric (ILD) is used between different metal layers has traditionally been silicon dioxide (doped or undoped).

- A thin film is a thin, solid layer of a material created on a substrate. Some properties of an acceptable thin film for wafer fabrication are good step coverage, ability to fill high aspect ratio gaps, good thickness uniformity, high purity and density, controlled stoichiometries and excellent adhesion.

- For a small gap or opening in a film, the aspect ratio is the ratio of its depth to width. Filling high aspect ratio gaps (> 3:1) is critical for advanced wafer fabrication.

- Deposited film grows in three distinct stages: 1) nucleation, 2) nuclei coalescence (island growth) and 3) continuous film. Deposited films can be amorphous, polycrystalline or single crystalline.

- Film deposition is generally categorized as a chemical process (chemical vapor deposition or plating) or a physical process (sputtering, evaporation or spin-on methods).

Chemical Vapor Deposition

- Chemical vapor deposition (CVD) is the process of depositing a solid film on the wafer surface through a chemical reaction of a gas mixture. All material for the thin film is supplied by an external source.

- The five basic chemical reactions that can be used in CVD are: pyrolosis, photolysis, reduction, oxidation or reduction-oxidation (redox).

- The CVD reaction steps are: 1) gas transport to the deposition zone, 2) formation of the film precursors, 3) film precursors at the wafer, 4) precursor adsorption, 5) precursor diffusion, 6) surface reactions, 7) by-product removal from the surface, and 8) by-product removal from the reactor.

- A mass-transport limited deposition process cannot proceed more rapidly than the mass-transport rate at which the reactant gases are supplied. A reaction-rate limited deposition process has a reduced reaction rate because there is less energy available to drive the reaction, typically at lower reaction temperatures and pressures.

- The introduction of dopants into SiO_2 during CVD can be beneficial by forming different types of glass, such as phosphosilicate glass (PSG), borophosphosilicate glass (BPSG), or fluorosilicate glass (FSG).

CVD Deposition Systems

- CVD reactors can be generally classified as atmospheric pressure CVD (APCVD), low pressure CVD (LPCVD) or plasma-assisted CVD. The plasma-assisted CVD is either plasma-enhanced CVD (PECVD) or high-density plasma CVD (HDPCVD).

- The first type of CVD reactor used in the semiconductor industry was atmospheric pressure CVD (APCVD). APCVD generally operates in the mass-transport limited regime, which requires a system design for optimal reactant gas flow to every wafer. An example of an APCVD application is SiO_2 deposition with TEOS-ozone.

- A common CVD reactor is low pressure CVD (LPCVD). This reactor operates in the reaction-rate limited regime. An LPCVD reactor is often hot-wall, which leads to particle deposits on the reactor wall. This requires frequent reactor cleaning. Examples of LPCVD applications are the deposition of SiO_2 and doped polysilicon.

- Plasma-assisted CVD equipment relies on plasma energy. The two types of plasma processes in CVD are plasma-enhanced CVD (PECVD) and high-density plasma

CVD (HDPCVD). For fine-geometry devices, HDPCVD is used because of its superior gap-fill properties.

Dielectrics and Performance

- The goal is to reduce the dielectric constant, *k*, between metal layers to decrease capacitive losses. Applications for a high-*k* dielectric are for DRAM storage capacitors and an eventual replacement for the thin gate oxide.

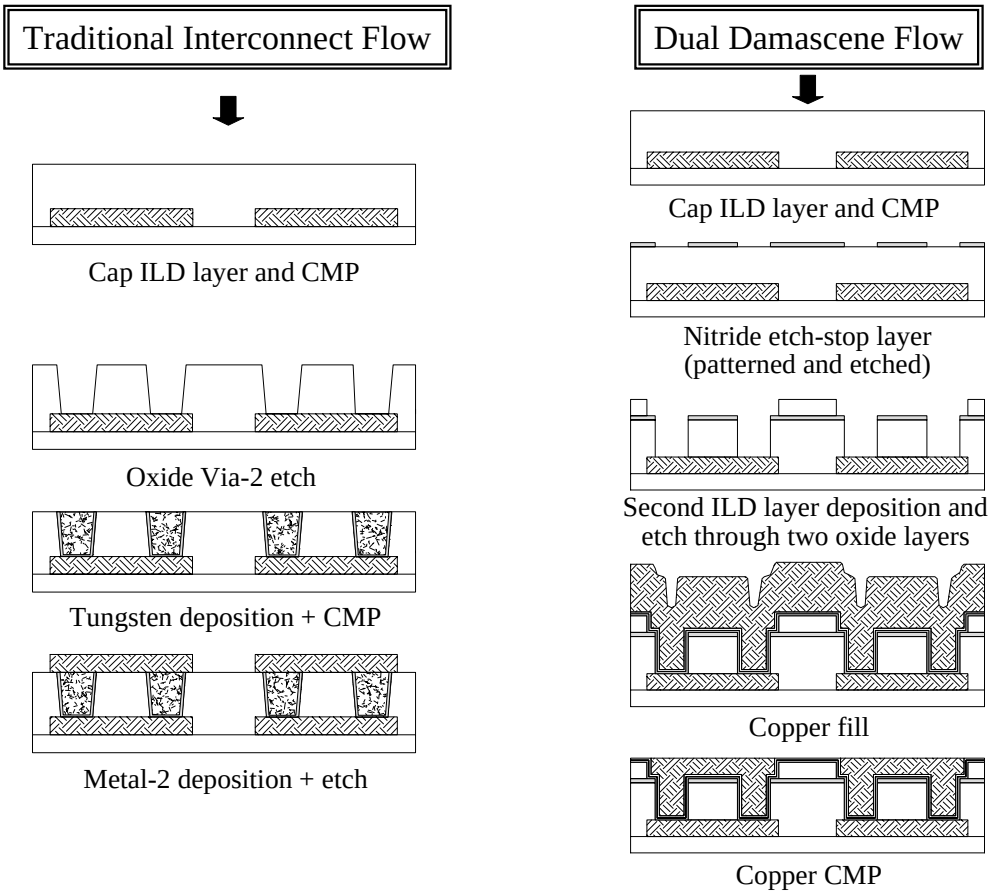
Spin-On-Dielectrics

- Dielectrics can also be applied using a spin-on technique. This method may become more widely used for some low-*k* dielectrics.

Epitaxy

- Epitaxy is the growth of a thin layer of single-crystal material on the surface of the wafer. Epitaxy growth methods are vapor-phase epitaxy (the most common method), metalorganic CVD and molecular-beam epitaxy.

Chapter 12
Metallization



Introduction

- Wafer metallization is the deposition of a thin film of conductive metal onto the wafer surface.

- There is traditional (aluminum) metallization and the new dual damascene (copper) metallization.

Types of Metals

- Requirements for a successful metal material are: 1) high conductivity, 2) good adhesion, 3) readily deposited, 4) high-resolution patterning and planarization, 5) reliability, 6) resistance to corrosion and 7) resistance to mechanical stress.

- Metals and metal alloys used in wafer fabrication are: aluminum, aluminum-copper alloys, copper, barrier metals, silicides and metal plugs.

- Aluminum is the traditional interconnect metal. Aluminum-copper alloys are used to reduce electromigration.

- Copper is the ideal interconnect metal. Its benefits are: 1) reduction in resistivity, 2) reduction in power consumption, 3) tighter packing density, 4) superior resistance to electromigration and 5) fewer process steps.

- A barrier metal is a thin layer of deposited metal that prevents intermixing of the materials above and below the barrier.

- Refractory metals react with silicon to form a silicide. A silicide is a metal compound that is thermally stable and has low electrical resistivity at the silicon/refractory metal interface. A salicide structure (self-aligned silicide) attains properly aligned source, drain and polysilicon gate in transistors.

- Metal plugs fill the via connections between two conductive layers.

Metal Deposition Systems

- Evaporation was the early system used for depositing metals, but it has been replaced by sputtering due to poor step coverage and gap-fill properties.

- Sputtering, a form of physical vapor deposition (PVD) is widely used for depositing aluminum metallization. It is a physical process that dislodges atoms from a metal target and deposits the atoms on the wafer surface. The advanced method of sputtering is ionized metal plasma PVD, which ionizes the metal in an RF plasma to obtain good step coverage.

- Metal CVD has superior step coverage and is most widely used for depositing tungsten plugs. A recent application is the copper seed layer for copper metallurgy.

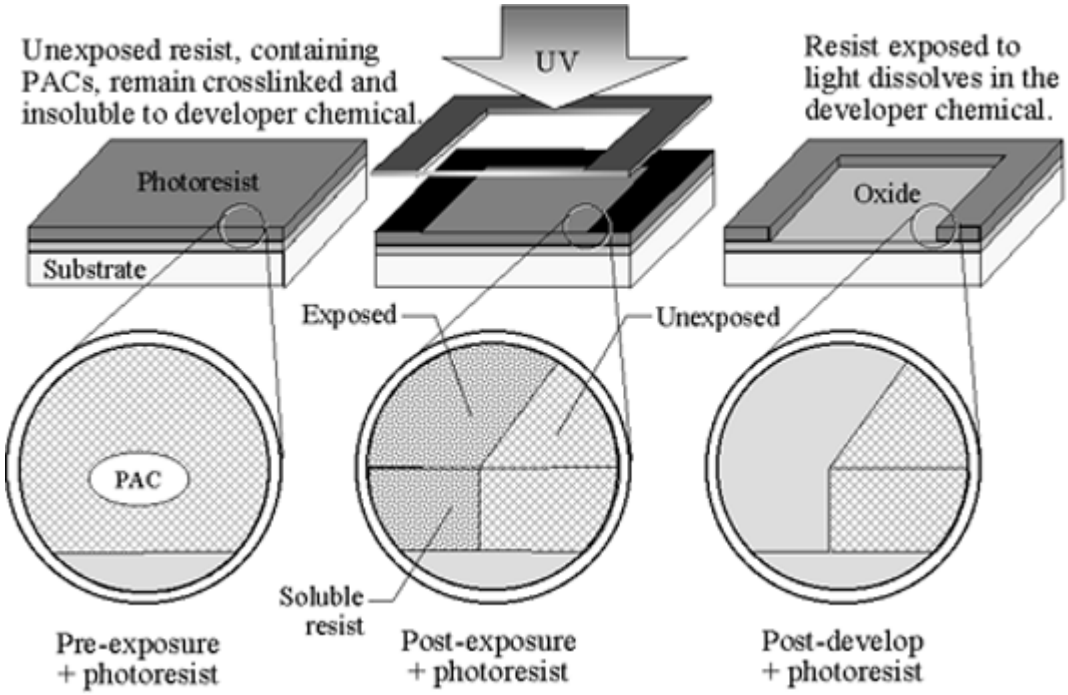
- Copper electroplating is used for depositing copper in the dual damascene metallization scheme. Electroplating configures the wafer as a cathode and immerses it into an electrolytic solution. Copper is deposited from a positive anode made of copper.

Metallization Schemes

- Metallization can be viewed as traditional metallization with aluminum and the new copper metallization scheme.

- Copper metallization is deposited using a dual damascene approach that is based on etching trenches and vias into the dielectric, filling the trenches and vias with copper and then planarizing the copper with chemical mechanical planarization.

Chapter 13
Photolithography
(Vapor Prime to Soft Bake)



Introduction

- Photolithography produces three-dimensional patterns on the wafer surface using a photoresist and exposure to light. Currently, photolithography is based on optical lithography.

- Resolution is the ability to differentiate between two closely spaced features. The energy from the light source is critical for patterning photoresist. Alignment during patterning is important for resolution requirements in advanced lithography.

Photolithography Processes

- Negative lithography uses negative resists, where the image in the resist is the negative of the pattern found on the reticle.

- Positive lithography uses positive resist, where the image formed in the resist is the same pattern formed in the reticle. Advanced lithography in sub-micron wafer fabs is done primarily with positive resist.

Eight Basic Steps of Photolithography

- Photolithography can be divided into eight basic steps:

    - Vapor prime: clean and prime the wafer surface.
    - Spin coat: apply photoresist.
    - Soft bake: drive off most photoresist solvent.
    - Alignment and exposure: align reticle with the wafer.
    - Post-exposure bake (PEB): bake step for deep UV photoresists.
    - Develop: create pattern in photoresist.
    - Hard bake: evaporate remaining solvent and improve resist adhesion.
    - Develop inspect: quality inspection.

Vapor Prime

- The wafer is cleaned and then undergoes a dehydration bake to remove moisture. Wafer priming uses the chemical HMDS to promote adhesion of the photoresist to the wafer surface. Wafer priming is done with either puddle, spray or vapor methods.

Spin Coat

- Photoresist is applied with a spin process, which has critical parameters to achieve the correct resist thickness and uniformity.

- There are different types of photoresist. Each resist has important physical properties, including resolution, contrast, sensitivity, viscosity, adhesion etch resistance, surface tension, storage and handling and contamination.

- Conventional i-line photoresists have three basic components: resin (polymer material), sensitizer and solvent. There also may be resist additives.

- Positive i-line photoresists are the most common resist for linewidths of 0.35 μm and larger. Positive i-line photoresist is based on novolak resin and DNQ sensitizer (which is the photoactive compound).

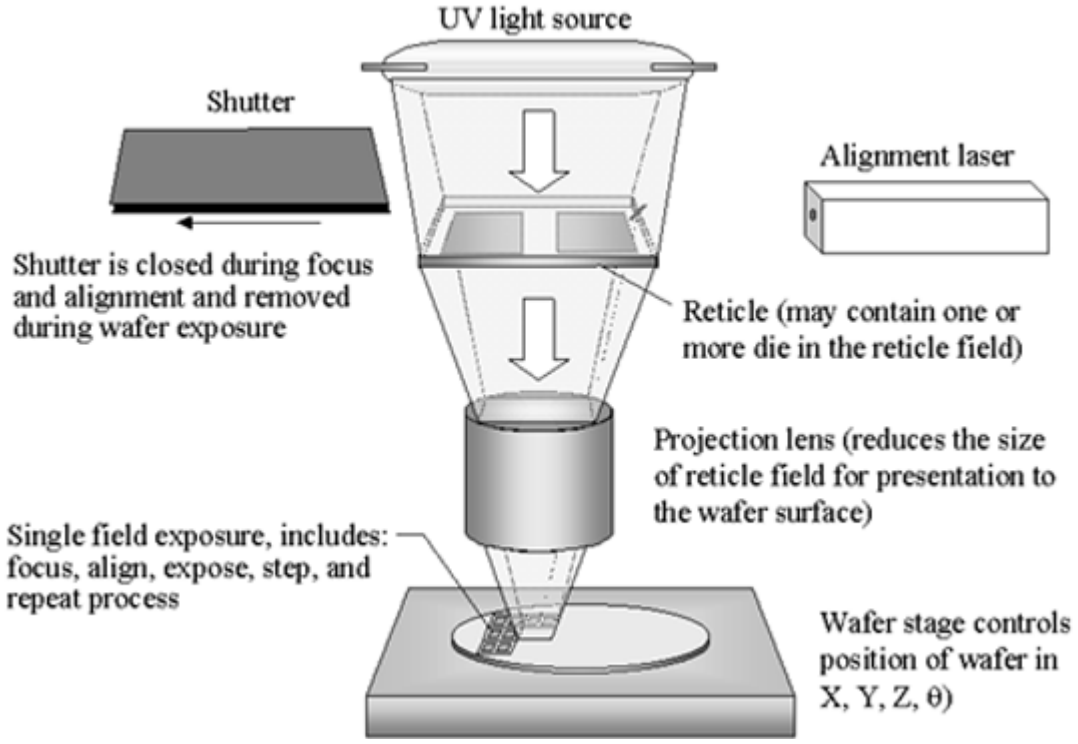
- At 0.25-μm linewidths and below, deep UV photoresist is necessary. Chemically amplified deep UV resist is widely used because it reacts at an accelerated rate to the deep UV light source based on an acid-catalyzed reaction. A post-exposure thermal bake is required for this reaction.

- Photoresist is dispensed by spin coating. The four steps of spin coating are: 1) dispense, 2) spin-up, 3) spin-off and 4) solvent evaporation.

Soft Bake

- A soft bake is done to drive off the solvent from the coated resist and improve adhesion. The preferred method for soft bake is heat conduction from a wafer on a vacuum hot plate.

Chapter 14
Photolithography
(Alignment and Exposure)



Introduction

- Modern photolithography is based on optical lithography, which consists of an ultraviolet light source, optical system, a reticle with a die pattern, an alignment system, and a wafer covered with a light-sensitive photoresist.

- Wafer steppers and step-and-scan systems have three basic purposes: 1) focus and align the wafer to the reticle, 2) reproduce a reticle image on the wafer through exposure of the resist, and 3) meet wafer throughput objectives. A general trend is the shorter the wavelength of the exposing light, the better resolution of the feature.

Optical Lithography

- An ultraviolet (UV) light source is required for optical lithography. Traditionally, this has been a mercury arc lamp at different wavelength intensity peaks (g-line of 436 nm, h-line at 405 nm and i-line at 365 nm).

- An excimer laser light source is used at UV wavelengths of 248 nm and below to achieve more light intensity. The laser sources used are krypton-fluoride (KrF) at a wavelength of 248 nm, argon-fluoride (ArF) at 193 nm and fluorine (F_2) at 157 nm.

- Optics is important because photolithography is based on an optical imaging process. Reflection and refraction of light are used in optics.

- Many different types of lenses are used in optics. Lens material is traditionally glass, with fused silica used in some 248 nm applications and calcium fluoride (CaF_2) used for shorter UV wavelengths (e.g., 193 nm and below).

- Diffraction is the bending of light as it passes through narrow openings, and is a concern in photolithography because of the small patterns on the reticle. Numerical aperture (NA) is the ability of a lens to collect and image diffracted light by converging the diffracted light to a single point. A larger NA is desirable.

- Antireflective coatings are used to reduce reflectivity from the surface below the resist. This controls problems from reflective notching and standing waves.

- The formula for resolution (R) is: $R = (k\lambda)/NA$. If the wavelength (λ) is decreased, then the resolution of the system will decrease (which is desirable). If NA is increased (to collect more diffracted light), then resolution will also decrease.

- Depth of focus (DOF) is the focal point over which the image is continuously in focus. It is desirable to have a large DOF. The DOF formula is: $DOF = \lambda/2(NA)^2$. It is seen that an increase in NA will increase the DOF, which is undesirable. The increased DOF due to decreased resolution has created the need for a planar wafer surface, thus justifying the need for chemical mechanical planarization.

Photolithography Equipment

- The contact aligner was the first alignment system. It used a 1X mask and is not widely used today. The proximity aligner was an improvement over the contact aligner because the mask did not contact the wafer. The latter is still used in low-volume laboratory applications.

- The scanning projection aligner (scanner) was developed in the late 1970s, and projects a full mask onto the wafer surface using a mirror system. It is still used today in older fabs with linewidths greater than 1 micron.

- The step-and-repeat aligner (stepper) was the mainstay of optical lithography in the 1990s. It is still widely used for CDs down to 0.35 μm. It projects one exposure field on the wafer and then steps to the next wafer location to repeat the exposure.

- The step-and-scan system is a hybrid tool that uses a scan approach (taken from the scanning projection aligner) along with a reduction lens and 4X reticle to step to exposure fields on the wafer surface. The scanning system has a simpler lens design.

- Reticles are a transparent plate that has the image pattern for an exposure field. They are used in steppers and step-and-scan systems. Reticles have a reduction ratio (typically 5:1 or 4:1) to permit a larger reticle pattern than what is imaged on the wafer. Reticles are fabricated with electron-beam lithography. A transparent pellicle is placed on the surface of the reticle to protect its surface from contamination.

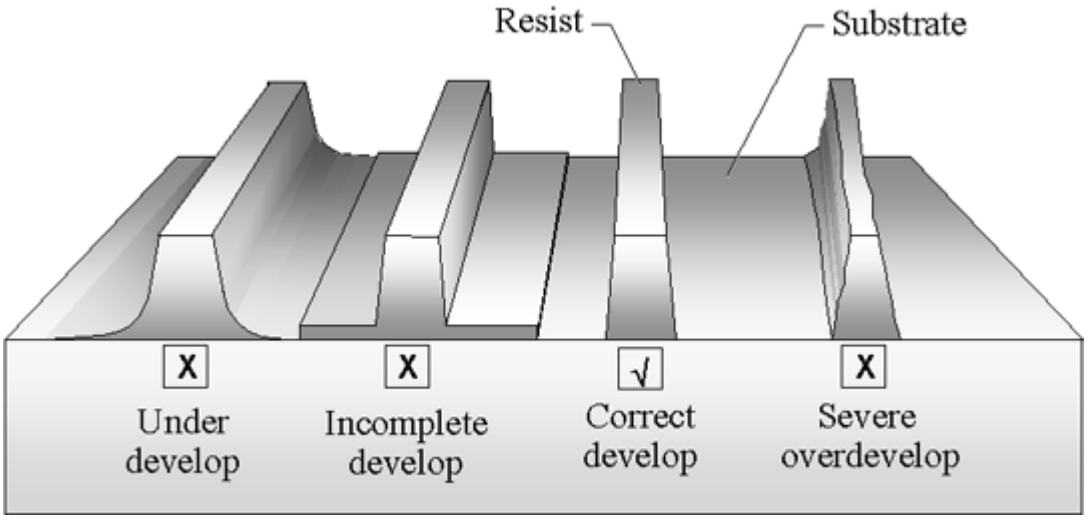
- An important optical enhancement technique is phase-shift mask, which overcomes light diffraction problems. Other enhancement techniques are optical proximity correction, off-axis illumination and print bias.

- A wide range of alignment marks and systems are used to ensure the wafer is properly aligned to the reticle.

Mix and Match

- A mix and match approach optimizes the type of lithography equipment (stepper or step-and-scan system) for the criticality of the wafer layer.

Chapter 15
Photolithography
Photoresist Development and Advanced Lithography



Introduction

- This chapter covers the final four steps of photolithography (post-exposure bake, develop, hard bake, and develop inspect) and new trends in advanced lithography.

Post-Exposure Bake

- A thermal post-exposure bake (PEB) is done for all chemically amplified deep UV resists to cause an acid-catalyzed reaction. This reaction makes the exposed resist soluble in the developer solution. The PEB is also done for i-line resists to reduce the standing waves effect.

Develop

- Photoresist development uses a liquid chemical developer to dissolve the soluble regions of the resist. Minimal chemical reaction is required for negative resist development.

- Positive resist development involves chemical reaction. The most common developer today for positive-tone i-line resist is TMAH. Standard TMAH developer formulations are common in the industry.

- The most common development techniques are continuous spray and puddle.

- Critical parameters for development are temperature, time, volume, wafer chuck, normality, rinse and exhaust flow.

Hard Bake

- A post-development thermal hard bake is done to evaporate any residual solvent and to harden the resist.

Develop Inspect

- A post-development inspection is done to find defects in the resist prior to the following operation (etch or ion implant).

Advanced Lithography

- Subwavelength lithography is a recent trend where the patterned images have critical dimensions that are significantly less than the exposure wavelength (e.g., a 248 nm exposure wavelength is used to pattern a 0.18 micron CD on the wafer surface).

- Next generation lithography is divided into four main research areas:

    - Extreme UV (EUV)
    - SCALPEL
    - Ion projection lithography (IPL)
    - X-ray

- Extreme UV employs optical lithography with a laser-produced plasma source to produce UV wavelengths of about 13 nm. There are many challenges to bring EUV into production.

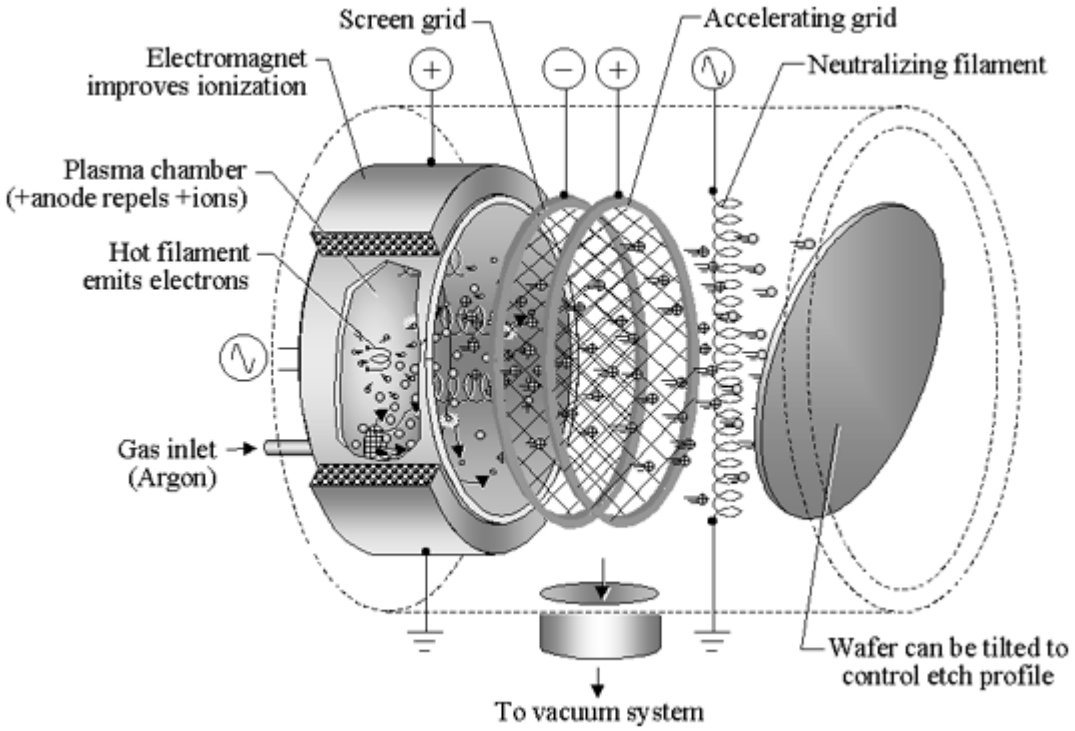
- SCALPEL (Scattering with Angular Limitation Projection Electron Beam Lithography) uses an established electron beam source to image a wafer pattern. This technology uses a 4X mask and does not require expensive optics.

- Ion projection lithography (IPL) uses ion beams to expose resists, either through a mask or by serially writing on the resist. Very high resolution is achievable.

- X-ray lithography is an established technology for patterning, used by one major IC manufacturer to produce microprocessors on 200-mm wafers in the 1990s. The short X-ray wavelengths (down to 10 nm) produce high resolution, but the required mask is difficult to build.

- Advanced resist processing include top-surface imaging, where the resist is only imaged at its top surface. This provides a wider process latitude for depth of focus.

Chapter 16
Etch



Introduction

- Etch is the process of selectively removing unneeded material from the wafer surface, using either chemical or physical means. Dry etch exposes the wafer to a plasma that interacts physically or chemically (or both) to remove the surface material. Wet etch uses liquid chemicals to chemically remove the wafer surface material.

Etch Parameters

- Critical etch parameters are:

  - Etch rate: the speed at which the material is removed.
  - Etch profile: shape of the sidewall of the etched feature. Isotropic etch profile has undercutting, whereas anisotropic etch is only in one direction.
  - Etch bias: a measure of the change in feature size after etch.
  - Selectivity: represents how much faster one film etches than another film.
  - Uniformity: capability of the process to etch uniformly across the entire surface.
  - Residues: the unwanted material remaining on the wafer after etch.
  - Polymer formation: a film deposited on the sidewalls to prevent lateral etching.
  - Plasma-induced damage: damage to sensitive devices on the wafer surface.
  - Particle contamination and defects: undesirable particles from plasma etching.

Dry Etch

- Dry etch is the primary etching method in advanced wafer fabrication. The etch profile is anisotropic with good CD control. The main disadvantage to dry etch is poor selectivity to the underlying layer, which requires effective endpoint control. The etching mechanism can be physical or chemical.

Plasma Etch Reactors

- The different types of dry plasma reactors are:
    - Barrel plasma etcher: an older reactor that is almost pure chemical.
    - Parallel plate (planar) reactor: two parallel plates with both physical and chemical etch mechanisms in either a plasma etch mode or reactive ion etch mode.
    - Downstream etch systems: a means of etching with reduced damage to the wafer surface. It typically uses a microwave source (2.45 GHz) for plasma.
    - Triode planar reactor: 3rd electrode for control over the ion bombardment.
    - Ion beam milling: physical etch mechanism with a strongly directional plasma.
    - Reactive ion etch (RIE): uses ion bombardment with both a reactive chemical process and a physical process to remove material.
    - High-density plasma etchers: the most common method for dry etching of critical layers. A high-density plasma is used to generate enough ions for an acceptable etch rate with a lower pressure. The lower pressure reduces ion collisions that cause loss of profile control (which gives excellent anisotropic sidewalls).

- Different types of high-density plasma etchers are: electron cyclotron resonance (ECR), inductively-coupled plasma (ICP), dual plasma source (DPS) and magnetically enhanced RIE (MERIE).

- Endpoint detection is required to monitor the etch process and stop etching to minimize overetching into the underlying layer. A common method of endpoint detection is optical emission spectroscopy, which measures the emitted light of an excited species to identify the material.

Dry Etch Applications

- Three main dry etch applications are: 1) dielectric, 2) silicon, and 3) metal.

- Oxide is a common dielectric dry etch application, and is typically based on fluorocarbon chemistry. High selectivity is required for the underlying material.

- Silicon dry etch is commonly done for polysilicon gate formation or silicon trench etch (for device isolation or capacitors structures). Silicon etch chemistry has traditionally been fluorine-based, but this has changed due to poor selectivity. Chlorine or bromine are common silicon etch chemistries today.

- Metal dry etch is done for aluminum alloy etching for interconnect wiring. A chlorine-based etch chemistry is often used. Tungsten metal is also dry etched.

Wet Etch

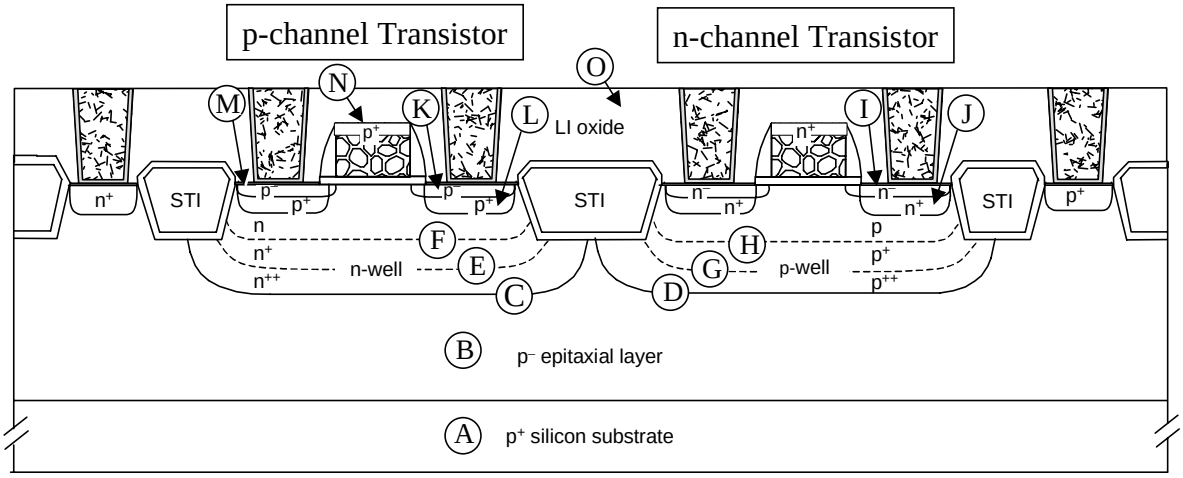
- Wet etch has been largely replaced by dry etch. Wet chemical strips are still used to remove layers, such as photoresist or a silicon nitride mask.

Photoresist Removal

- Dry plasma ashing is the removal of resist with oxygen, and is the dominant method for resist removal today. Atomic oxygen atoms are reacted with the resist material in a plasma environment. Typically a downstream reactor is used to minimize plasma damage to the wafer.

Chapter 17
Ion Implant

CMOS Structures with Doped Regions



Introduction

- Wafer doping is the introduction of a dopant into the crystal structure of a semiconductor material to modify its electronic properties. In advanced fabs, this is done primarily by ion implantation. The early doping method was thermal diffusion.

- There are a wide range of doping processes in the wafer fab. The control of the dopant profile in the doped region requires the control of both depth and concentration, which is best achieved with ion implant.

Diffusion

- Diffusion is the movement of one material through another from a region of relatively higher concentration into a region of lower concentration. There are three steps to thermal diffusion: predeposition, drive-in and activation.

Ion Implantation

- Ion implantation is a physical process. It is preferred over diffusion because of its excellent control over doping concentration and depth.

- An ion implanter creates positively-charged ions that are formed into a beam, accelerated in a voltage field, and implanted into the wafer

- The important ion implant parameters are dose and range. Dose (Q) is the number of implanted ions per unit area of wafer surface, with units of atoms/cm^2. Range is the total distance an ion travels in the silicon during ion implantation.

- The beam current is a key variable for defining the quantity (or dose) of ions implanted. The implanter energy is the key variable for defining the ion implant depth (range).

Ion Implanters

- The ion implant tool consists of five major subsystems:

    - Ion source: where ions are generated, commonly a Freeman ion source.
    - Extraction electrode and ion analyzer: positive ions are collected and formed into a beam.
    - Acceleration column: positive ions are accelerated in an electric field.
    - Scanning system: where the small-diameter ion beam is scanned across the entire wafer.
    - Process chamber: implantation takes place in this chamber, including the scanning system, the end station with vacuum load locks for loading and unloading, the wafer handler system and computer control system.

- There are different types of ion implanters depending on the application, including high-current and high-energy beams or low-energy beams (used for ultrashallow implants).

- Beam blow-up caused by only positively charged ions in the beam is controlled by space charge neutralization. A neutral beam trap is used to trap residual gas molecules.

- Different types of scanning systems are electrostatic scanning, mechanical scanning, hybrid scanning, and parallel scanning.

- A thermal anneal step is required after ion implantation to electrically activate implanted ions. The thermal anneal moves ions into lattice structure sites of the silicon. The anneal is often done with a rapid thermal anneal tool (RTA).

- Channeling is when implanted ions are not slowed by collisions with silicon atoms. It is controlled by three different techniques: wafer tilt, screen oxide layer or preamorphization.

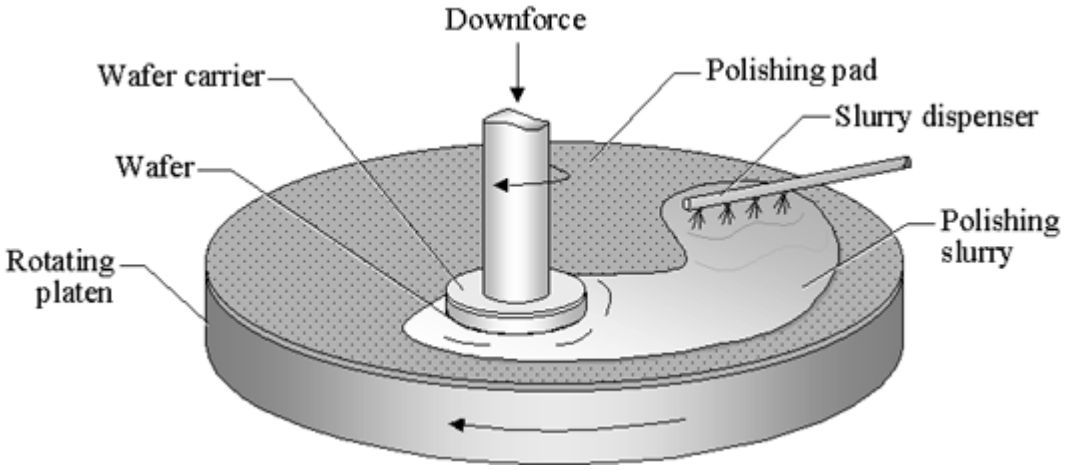
Ion Implant Trends in Process Integration

Examples of different ion implant process requirements in advanced fabrication are:

- Deep buried layers: buried layers implanted with high-energy implanters.

- Retrograde wells: peak implanted dopant profile buried at a certain depth.
- Punchthrough stoppers: necessary to minimize leakage in short channel lengths.
- Threshold voltage adjustment: dopant adjustment in channel region.
- Lightly doped drain (LDD): source/drain extension just to the edge of the channel region.
- Source/drain implants: high doped regions that interface to the lightly doped active channel and well regions.
- Polysilicon gate: doped to render it conductive.
- Trench capacitor: doping of capacitor sidewalls to attain sufficient capacitance.
- Ultrashallow junctions: doped regions with ultrashallow depth so that source and drain are in scale with the short channel length.
- Silicon-on-insulator (SOI): a form of vertical device isolation that places a buried layer within the silicon to effectively isolate devices on the silicon surface. The most promising technique is SIMOX (Separation by IMplanted OXygen), which as a horizontal oxide layer buried in the silicon.

Chapter 18
Chemical Mechanical Planarization



Introduction

- Topography describes the nonplanar surface of wafer layers during fabrication. A planarized wafer has a flat surface with minimal topography. The primary planarization process used since the mid-1990s is chemical mechanical planarization (CMP).

- Planarization terminology is:

  - Smoothing: topography is not significantly reduced.
  - Partial planarization: smoothing and a local step height reduction.
  - Local planarization: complete filling of smaller gaps or local areas.
  - Global planarization: local planarization plus a significant reduction in total step height across the entire wafer surface.

Traditional Planarization

- The three traditional planarization methods are: 1) etchback, 2) glass reflow, and 3) spin-on films. These techniques are not acceptable for sub-0.25 μm wafer fabrication.

Chemical Mechanical Planarization

- Chemical mechanical planarization (CMP) is a global planarization technique. It is often referred to as polish. The wafer is positioned in a wafer holder (or carrier) and held against a polishing pad on a platen. A slurry with chemistry and abrasive

particles is applied to the wafer. The rotary or orbital motion between the wafer and polishing pad is controlled to achieve precise planarization.

- CMP reduces the surface topography of the wafer, such as within-wafer nonuniformity (WIWNU) and wafer-to-wafer nonuniformity (WTWNU).

- There are many advantages to CMP, including global planarization, ability to planarize different materials and multimaterial surfaces.

- The CMP oxide polish mechanism is based on Cook's theory, where the water in the slurry reacts with the oxide to decrease its harness. This softer surface is removed by the mechanical actions of the abrasive slurry.

- The CMP mechanism for metal polish is not as well understood, and is based on both a chemical oxidation and mechanical abrasion.

- CMP has pattern density effects, where regions of narrowly spaced features often polish at a greater rate than widely spaced features. Defects are erosion in high wiring density and dishing in a large feature.

- The slurry is different depending on the surface being planarized. Oxide slurry is often an alkaline medium of aqueous potassium hydroxide or ammonium hydroxide with fine silica powder. Tungsten metal slurry is sometimes a mixture of fine alumina or silica powder in hydrogen peroxide. Copper metal slurry is still undergoing research, but one approach is a basic (pH) solution of ammonium hydroxide with alumina powder and an ammonia complexing agent to dissolve copper oxides.

- The polishing pad is often made of a porous polyurethane material. It requires regular conditioning to remove a glazed surface condition.

- Different factors affect the polish rate and uniformity. The polish rate of different materials is referred to as selectivity, which is important factor for uniformity and planarity. Overburden is the amount of excess material deposited on the wafer prior to polishing, which affects the total polish time.

- CMP tools often have multiple wafer carriers. Endpoint detection is important to detect when planarization has completed. The two common methods are motor current endpoint detection and optical endpoint detection.

- CMP cleaning is critical and has developed into a dry-in/dry-out process. Scrubbing with a double-sided brush scrub, often with through-the-brush chemical delivery of dilute ammonium hydroxide.

CMP Applications

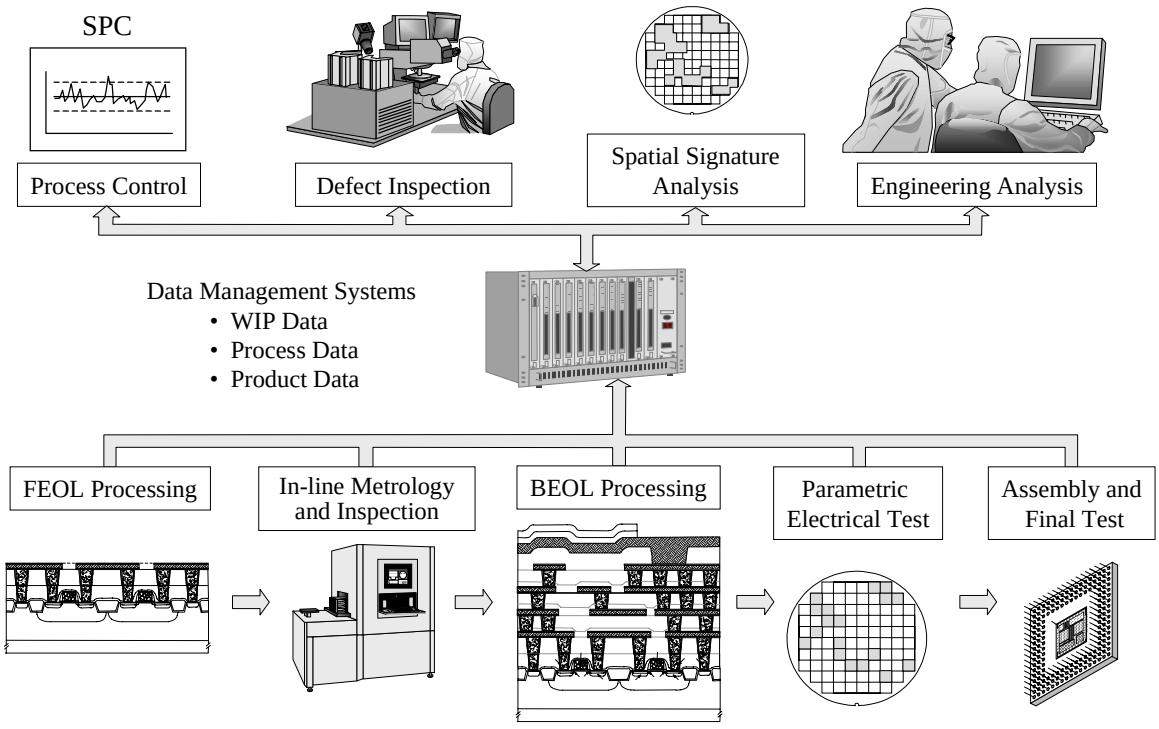
- Common CMP applications are:

    - STI oxide polish: CMP polish of oxide fill layer.
    - LI oxide polish: polish and patterning of LI oxide to form the local interconnect.
    - LI tungsten polish: polishing of blanket tungsten that fills the LI trenches and vias, using the oxide as a polish stop.
    - ILD oxide polish: oxide is polished with CMP to a specific target thickness.
    - Tungsten plug polish: polish of the blanket tungsten layer that is deposited to fill the vias, thus forming tungsten plugs.
    - Dual-damascene copper polish: polish of the copper that fills the vias and trenches used in the dual-damascene approach.

CMP Quality Measures

- Microscratching is a significant source of quality problems for CMP.

Chapter 19
Wafer Test



Introduction

- Wafer test is the measurement of electrical parameters on ICs at the wafer level to verify conformance to specifications.

- There are five different electrical tests: 1) IC design verification, 2) in-line parametric test (also known as wafer electrical test, or WET), 3) wafer sort (probe), 4) burn-in reliability and 5) final test. Tests number 2 & 3 are wafer-level electrical tests.

Wafer Test

- The in-line parametric test (also known as a DC test) is performed early in the process, usually after the first metal layer has been deposited and etched. A parametric test is done on test structures located on the wafer. This test will identify process problems, establish wafer pass/fail criteria, collect data, assess special tests and obtain wafer level reliability data.

- In-line parametric tests are usually done on test structures, also known as process control monitors (PCMs). Test structures are commonly located in the scribe line region and are used to test a wide range of parameters (e.g., leakage current, critical dimensions, threshold voltage, resistance, etc.).

- In-line parametric data is collected on a sample basis and interpreted by engineers to improve the fab process. An assessment of wafer level reliability can also be done to predict device quality.

- The four test subsystems for in-line parametric testers are: probe card interface, wafer positioning, tester instrumentation and a computer for system control. Probe card interfaces between the tester and the device under test (DUT). The wafer positioning system (prober) aligns the wafer for contact with the probe card. The instrumentation in automated test equipment (ATE) measures sub-picoamp current and picofarad-level capacitance.

- Wafer sort is done at the end of wafer fabrication to electrically test each die on the wafer. The objectives of wafer sort are: chip functionality, chip sorting, fab yield response and test coverage.

- The procedure for performing wafer sort is similar to in-line parametric test, except now every die on the wafer is tested. The electrical test is a functional test. Wafers are assigned a bincode number after wafer sort to categorize the test results.

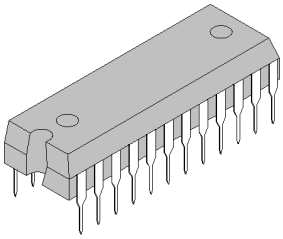
- The three types of wafer sort tests are: 1) DC tests (e.g., continuity, etc.), 2) output checks, and 3) functional tests.

- The issues at wafer sort testing are total test time, the use of different fault models, I_{DDQ} testing to predict reliability and guardbanding.

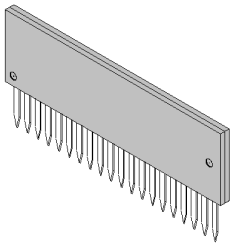
- Fabrication and design issues that affect wafer yield are larger wafer diameters, increased die size, increase in number of process steps, shrinking feature sizes, process maturity and crystal defects.

- Wafer sort yield models are used to predict the wafer sort yield. Three traditional yield models are Poisson's model, Murphy's model and Seed's model. The latter two are acceptable for VLSI and ULSI technology. A yield management system is used in the fab to assist in improving overall yield.

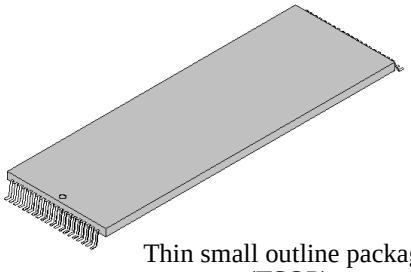
Chapter 20
Assembly and Packaging



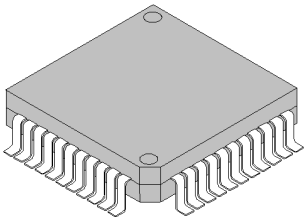
Dual in-line package
(DIP)



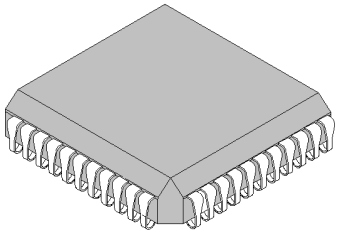
Single in-line package
(SIP)



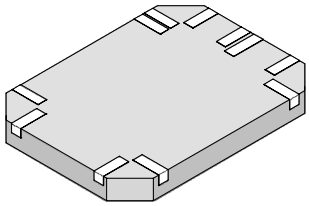
Thin small outline package
(TSOP)



Quad flat pack
(QFP)



Plastic leaded chip carrier
(PLCC)



Leadless chip carrier
(LCC)

Introduction

- Chips that pass the wafer sort test undergo final assembly and packaging. IC final assembly separates each good die from the wafer and attaches the die to a metal leadframe or substrate. IC packaging encloses the die in a protective package.

- IC packaging has four functions: protection from the environment/handling, signal interconnections, physical support and heat dissipation. There are two packaging levels: 1st level packaging involves the IC, whereas 2nd level packaging is placing the IC on a circuit board. There are numerous packaging design constraints.

Traditional Assembly

- IC final assembly consists of four steps: backgrind, die separation, die attach and wire bonding. Backgrind reduces the wafer thickness to the appropriate dimension. Die separation cuts each die from the wafer. Die attach is the physical attachment of the die to the leadframe or substrate. Wirebonding attaches fine-diameter wires between die bonding pads and the terminals of the leadframe to form electrical connections.

- Die attach is done by epoxy attach, eutectic attach and glass frit attach. The common epoxy attach method bonds the chip to the leadframe using epoxy. Eutectic attach,

common for bipolar ICs, uses a thin film of gold on the backside of the wafer that is alloyed with the metallized surface of the leadframe. Glass frit attach uses a mixture of silver and glass in an organic medium to attach chips in a ceramic package.

- The three basic types of wirebonding are: thermocompression bonding, ultrasonic bonding and thermosonic ball bonding. Thermal energy and pressure are used in thermocompression bonding. Ultrasonic bonding is based on ultrasonic energy and pressure to form a wedge bond between the wire and pad. Thermosonic ball bonding combines ultrasonic energy, heat and pressure to form a ball bond.

Traditional Packaging

- Traditional IC packaging materials are plastic packaging and ceramic packaging.

- Plastic packaging uses an epoxy polymer to encapsulate the wirebonded die and leadframe. This technology has many different types of plastic packages.

- Ceramic packaging is used for state-of-the-art IC packages that require either maximum reliability or high-power. The two main types of ceramic packaging are either a refractory (high temperature) ceramic or ceramic DIP (CERDIP) technology. Both have a hermetic seal (sealed against moisture).

- All assembled and packaged chips undergo a final electrical test for IC reliability.

Advanced Assembly and Packaging

- New packaging designs are being introduced to provide for more reliable, faster and higher-density circuits at lower cost. Advanced packaging designs include:

    - Flip chip
    - Ball grid array (BGA)
    - Chip on board (COB)
    - Tape automated bonding (TAB)
    - Multichip modules (MCM)
    - Chip scale packaging (CSP)
    - Wafer-level packaging

- Flip chip packaging mounts the active side of a chip toward the substrate. It uses bump technology (typically solder bumps) to form the interconnection between the chip and substrate. An epoxy underfill is used around the area-array of bumps to improve reliability.

- Ball grid array (BGA) uses a ceramic or plastic substrate with an area array of solder balls to connect the substrate to the circuit board. To lower costs, this technology is readily integrated into standard surface mount assembly.

- Chip on board (COB) mounts IC chips directly to the substrate, along side other surface mount (SMT) or pin-in-hole (PIH) components.

- Tape automated bonding (TAB) uses a plastic tape as a chip carrier. The tape has a thin copper foil that is etched to form the leads. The chip and leads are removed from the carrier prior to assembly onto the circuit board.

- Multichip module (MCM) has several die assembled onto one substrate. This permits a higher density of chips.

- Chip scale packaging (CSP) has an IC package that is about the same size as the silicon chip (< 1.2 times the footprint of the die). This is a fast growing method of advanced packaging, and provides for lower cost, lower weight and lower thickness.

- Wafer-level packaging places the 1^{st} level interconnections and package input/output terminals on the wafer before it is diced. It is typically done with a bump interconnect process. This will simplify the IC packaging process and lower cost.