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Smart Cut™

A guide to the technology, the process, the products

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What is Smart Cut?

Smart Cut is Soitec's patented process technology for creating "engineered" wafers. Engineered wafers (such as Silicon-On-Insulator, or SOI) consist of multiple layers of substrate materials.

Beginning in mainstream volume with the 130nm geometries of 2001 followed by the 90nm node being launched in 2003/2004, leading-edge IC manufacturers have used engineered wafers with specific electro-mechanical properties. With each subsequent generation, the wafer material properties are slated to become even more stringent. Smart Cut is a process technology that enables wafer suppliers to create the full range of engineered wafers for both current and future generations of electronics.

The Smart Cut technology was developed at CEA-LETI, one of the world's premier microelectronics research laboratories. It was made viable for high-volume commercial production by Soitec, which now owns the Smart Cut patents. Soitec uses the Smart Cut technology to fabricate engineered wafers for the world's leading manufacturers. The company's first wafer product family is called UNIBOND™. UNIBOND is a line of SOI wafers created using the Smart Cut process technology.

Soitec also has the exclusive right to sub-license the Smart Cut process technology to third-party material and process suppliers. Seiko-Epson has acquired a license for the manufacturing of silicon on quartz (SOQ), and leading wafer suppliers such as Shin Etsu Handotai have chosen to use the Smart Cut process in fabricating engineered wafers for their own customers.

Beyond SOI, Soitec is using the Smart Cut technology to develop new families of engineered wafers and custom-wafer solutions.

What are engineered substrates?

In contrast to the current generation of bulk wafers, which are typically pure silicon, "engineered" substrates contain several materials layered one on top of the other. The most common engineered solution currently on the market is the SOI wafer.

Advanced, engineered substrates use layering, implantation and/or bonding of advanced substrate materials into and onto a silicon wafer or other substrate (such as quartz). The result is that the bulk wafer is replaced by a stack of substrate layers on some kind of "handle" wafer. Currently for most applications, the top layer is still silicon, so that chip manufacturers can continue to use traditional manufacturing processes and equipment in the fabrication process.

The SOI wafer is a composite substrate with an active top Si layer decoupled from the support wafer. It is the first example of an engineered substrate addressing mainstream MOSFET performance requirements. SOI now has a well-proven record. It makes a major impact on partially and fully depleted devices in terms of performance enhancement, reduction of leakage currents and power consumption, suitability for low voltage device architectures and so forth.

Smart Cut is currently deployed commercially for SOI, SOQ (silicon-on-quartz or, more precisely, single crystalline Si on a fused silica substrate) and soon, strained silicon on insulator. It has also been successfully demonstrated for many other major engineered substrates, which are scheduled for commercial release in concert with customer needs and the industry roadmap.

What are the market and technology drivers?

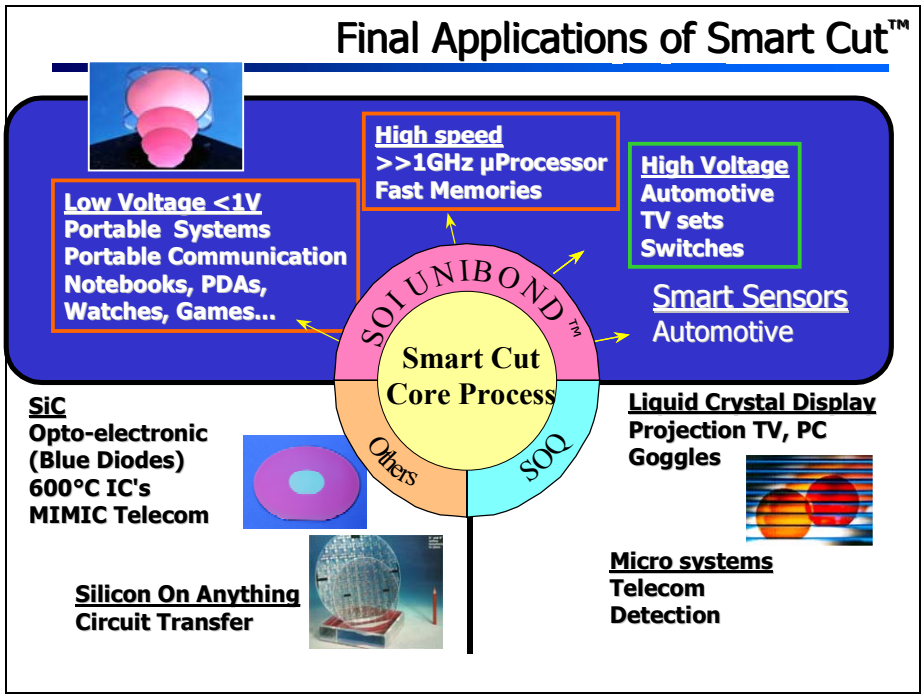


Figure 1. Smart Cut market and technology drivers

The need for engineered wafers is being driven on multiple fronts (Figure 1):

- *Faster, more powerful chips* – the need to pack more and more circuits onto a chip means that the line widths are ever narrowing, and they're packed in more densely. Power leakage between and within the circuits on a chip can lead to reliability problems. Since reduced parasitic capacitance is a key contributor to improved performance, engineered substrates—especially those that add an insulating layer—are a keystone in countering this problem.
- *Mobile applications* – DSPs and microprocessors destined for mobile products need to consume very little power, so they run cool and go easy on the battery. Engineered substrates enable highly efficient chips that require very low levels of power to drive them.
- *High-voltage* – chips for high-voltage applications (such as lighting or audio) or electrically challenging environments (inside an engine block, for example) are now possible thanks to the insulating properties of SOI.
- *System on a Chip (SoC)* – engineered substrates enable multiple technologies to be integrated on a single chip. SoC will enable product designers to create radically smaller, lighter and more powerful end-products. Products like cell phones that now require over half a dozen chips will be built around a single chip.
- *Biomedical* – rugged yet sensitive medical equipment and even bio-implants benefit in terms of safety and reliability when they use chips built on engineered substrates.
- *Sensors* – micro-machined sensors (MEMS) built on engineered substrates are attaining unmatchable sensitivity and accuracy.
- *Rad-hard* – the aerospace industry was the first to pioneer engineered substrates. Early chips bound for outer space were "radiation hardened", enabling them to withstand the grueling journey. Today's rad-hard chips and sensors are found both in aerospace and on the ground, since recent developments like Smart Cut make engineered substrates far more economical.
- *Moore's Law* – ever since 1965, when Intel co-founder Gordon E. Moore first predicted the almost annual doubling of the number of transistors that can be packed on a chip, the industry has found ways to make it happen. Until now, circuit designers and manufacturers have been able to keep up the pace. However, current indications suggest that below 90nm, the rate can only be sustained by using engineered substrates.

A brief history of SOI

SOI technology was first introduced in the 1970s as a niche substrate technology for military or space applications. In these early days, grind back (BESOI) and SIMOX (Separation by Implantation of Oxygen) were the dominant SOI fabrication technologies. However, they were not very well suited to high-volume, commercial production.

After a brief period using SIMOX implantation techniques to fabricate SOI wafers, the founders of Soitec pioneered a new wafer bonding technique, Smart Cut, which was developed at CEA-LETI. Smart Cut based manufacturing of Soitec's SOI wafers, which are sold under the tradename UNIBOND, ramped up in the mid 1990s.

With the new millennium, chip geometries moved rapidly from the 180nm node to the 130nm node and now to 90nm and beyond. The IC industry fully recognizes that SOI provides improved performance while reducing parasitic substrate capacitances and leakage currents. Commercial applications of SOI have grown exponentially, and entered the mainstream of Ultra Large Scale Integration (ULSI) ICs.

As the IC industry moves towards the development of the future 65nm, 45nm, 32nm, 22nm technology nodes, more innovations will be required at the substrate level. The primary driver is MOSFET design, as the synergy between device architectures and composite substrate engineering grows.

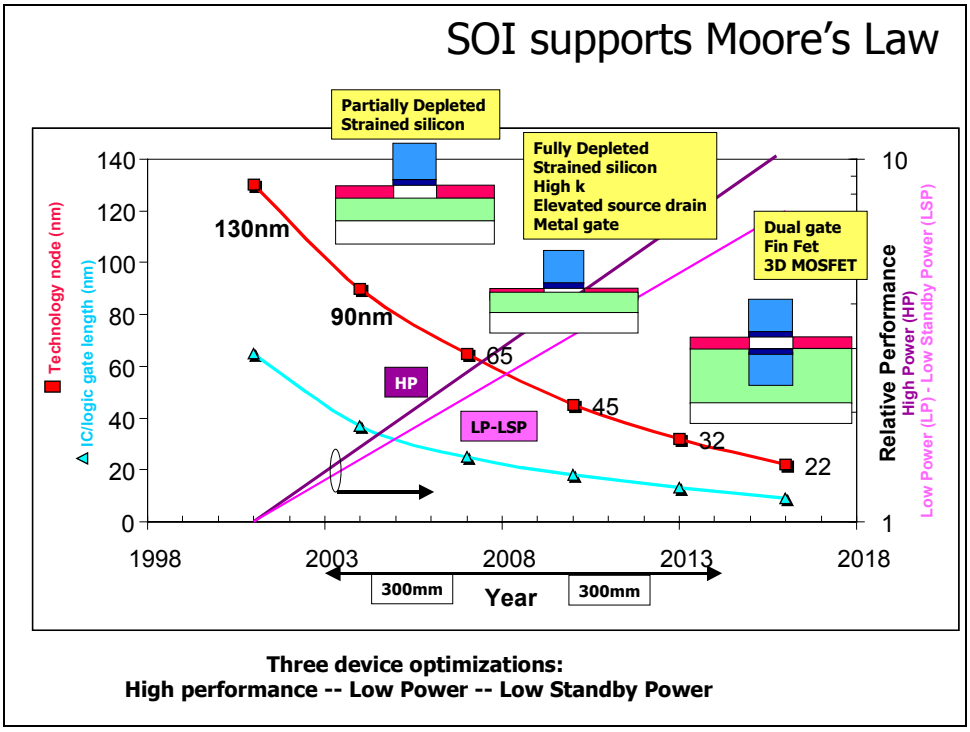


Figure 2. SOI fully supports future device generations

SOI in the overall manufacturing process flow

Silicon is the basic material used in making most of today's electronic components. The silicon chain begins with the pulling of monocrystalline ingots and the slicing of these ingots into wafers. This is traditionally done by players in the chemical industry (Shin Etsu Chemical, Wacker, Sumco, MEMC, and so forth).

The circular silicon wafers that are delivered to semiconductor manufacturers range in diameter from a few inches up to today's latest dimension of 300mm (12"). However, only a portion of one of the faces of the wafer is used for making the electronic components; the rest essentially serves as a mechanical support.

The creation of SOI material—Soitec's primary business—represents an intermediate step between the fabrication of the polished, bulk silicon wafers, and the creation of electronic components. The role of SOI is to electronically insulate a fine layer of the monocrystalline silicon from the rest of the silicon wafer.

Semiconductor manufacturers can then fabricate integrated circuits (ICs or chips) on the top layer of the

SOI wafers using the same processes they would use on plain, "bulk" silicon wafers. As always, the wafers are then cut up and the chips packaged for mounting on the cards that are integrated into electronic systems (PCs, game consoles, telecommunications devices, portable telephones, PDAs, servers, and so forth).

However, the embedded layer of insulation enables the SOI-based chips to function at significantly higher speeds while reducing electrical losses. The result is an increase in performance (30%) and a reduction in power consumption (2-3x)—a major industrial evolution in microelectronics.

Technical explanation of Smart Cut

Smart Cut is a revolutionary technique used to transfer ultra-thin single crystal layers of wafer substrate material (such as silicon) onto another surface. Differing from traditional layer-transfer techniques, which are based mainly on wafer bonding and etch-back or epitaxial lift-off, the Smart Cut approach uses a thermal activation process as an "atomic scalpel". It literally slices the wafer horizontally, lifting off a thin layer from the donor substrate and placing it onto a new substrate. Inherently, this process offers better control, and a single donor substrate can be reused many times for further layer transfers.

The transferred layer thickness is pre-determined by the cleavage zone created via ion implantation (of hydrogen, helium, argon, etc.). After the layer transfer and bonding, the cleaved surface of the thin film is treated, polished and annealed to ensure a silicon film (in the case of SOI) and surface quality comparable to silicon prime wafers.

Soitec uses Smart Cut technology to fabricate its UNIBOND SOI wafers. A schematic process flow indicating the role of Smart Cut in UNIBOND fabrication is shown in Figure 3.

The technological strength of Smart Cut technology is clearly demonstrated in UNIBOND SOI wafers:

- it is well-suited to high-volume manufacturing;
- the thicknesses of the top Si and buried oxide layers are widely flexible;
- the process is scalable to any wafer diameter;
- it uses standard IC manufacturing equipment.

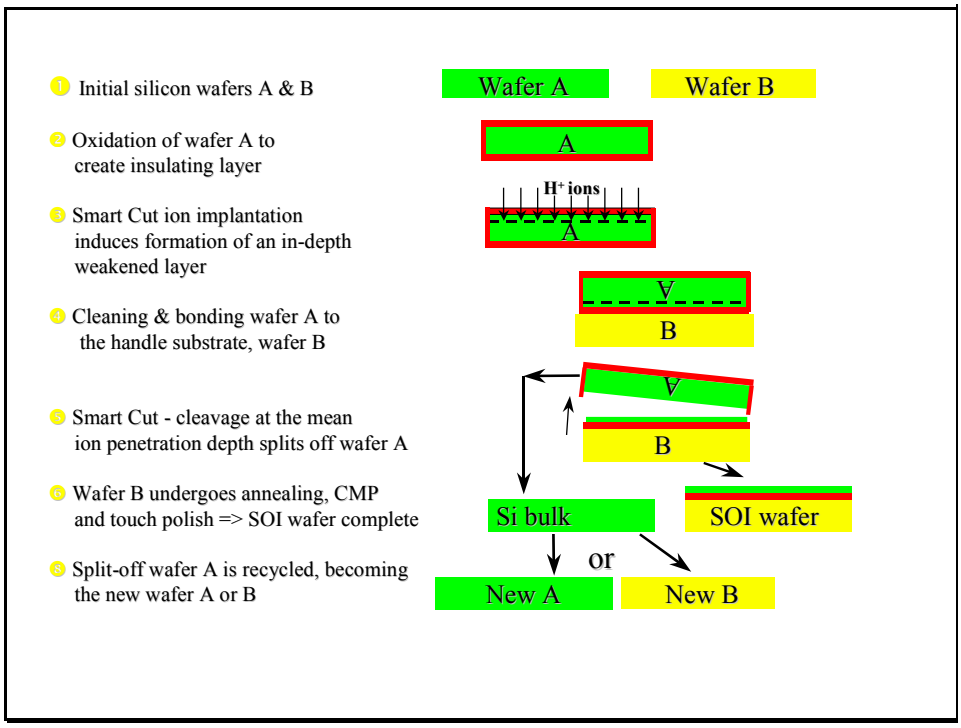


Figure 3: Smart Cut is at the heart of Soitec's UNIBOND SOI wafer fabrication. In this case, the process is based on Hydrogen implantation and wafer-bonding to a silicon handle substrate B.

Soitec's UNIBOND SOI and SOQ wafers

Smart Cut is currently the only industrial process capable of manufacturing SOI wafers at high volumes in all sizes, including: 100mm, 125mm, 150mm, 200mm and 300mm wafers. Soitec sells its SOI wafers under the tradename UNIBOND.

The thickness of the top Si layer as well as the thickness of the buried insulating layer can vary to cover the full range of customer applications. (See Figure 4.)

UNIBOND Thin-film SOI wafers

Developed to address the most advanced silicon devices, thin-film and ultra-thin film UNIBOND products are tailored for fully or partially depleted CMOS applications.

The wafers are available with top-layer thicknesses ranging from several microns down to 20nm, with thickness uniformity of ±5% (3 sigma). UNIBOND thin-film SOI wafers are available in both 200mm and 300mm wafer diameters. The thin- and ultra-thin SOI products are ideal for advanced, high-speed, low voltage, low-power consumption products such as microprocessors and complex wireless chips.

UNIBOND Thick-film SOI wafers

A broad range of made-to-order thicknesses are available with top-layer thicknesses ranging from 1.5 microns up to several tens of microns, with thickness uniformity of ±2% (3 sigma). Key applications for thick-film SOI products include high-voltage, power, and high-temperature devices, smart sensors and MEMS/ MOEMS.

UNIBOND High Resistivity SOI wafers

Available with top-layer thickness from 70nm up to 340nm, with thickness uniformity down to ±7.5nm, UNIBOND High Resistivity SOI wafers are designed for RF, mixed signal and SoC applications.

SOQ wafers

Silicon-on-Quartz (SOQ) wafers are manufactured using the same proprietary Smart Cut process technology to create a thin, monocrystalline silicon film on quartz handle wafers. They are used for applications requiring high resistivity or transparent substrates. (Note that while the generic term "quartz" is used in the industry, the substrate is really a fused silica.)

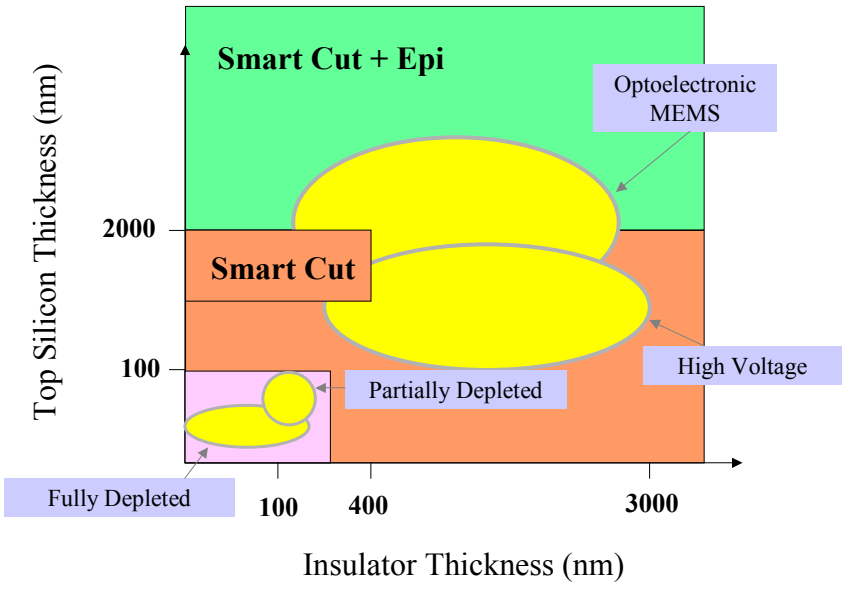


Figure 4: The UNIBOND SOI process technological strength is the compatibility with mass production, the wide flexibility in top Si and buried oxide thicknesses definition, the scalability to any wafer diameter, and the utilization of standard IC manufacturing equipment. The wafer size requirement for ULSI partially or fully depleted device architecture is 200 or 300mm, while for MEMS, MOEMS and Smart Power it is typically 100mm to 150mm.

Current and future engineered substrates

The Smart Cut process was originally developed to manufacture SOI and has achieved a high degree of maturity with UNIBOND mass production. But, in contrast to SIMOX, the potential of Smart Cut goes beyond SOI.

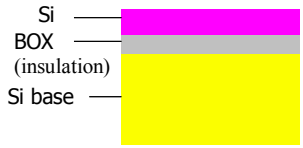
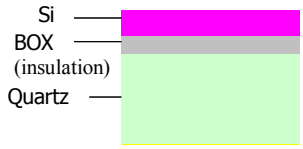
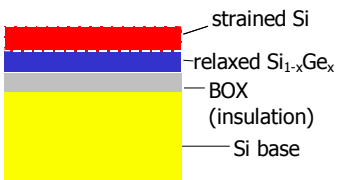
As a generic layer transfer technology, Smart Cut expands the range of applications from conventional hetero-epitaxy to single crystal thin film transfer to any type of substrate. It significantly enlarges the field of engineered composite substrates combining different thin layer materials on a given substrate to address the requirements of the most diverse applications. Smart Cut technology is today the subject of many studies and developments world wide

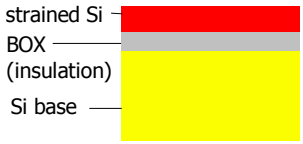
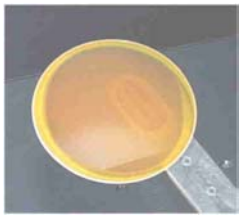
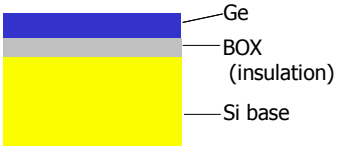
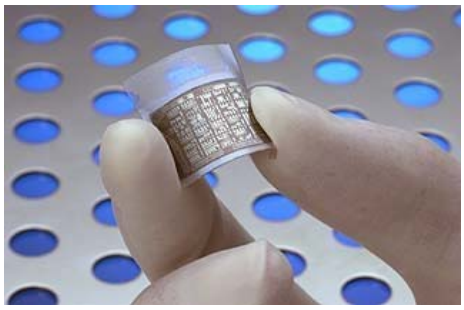
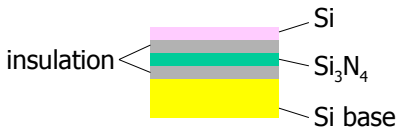
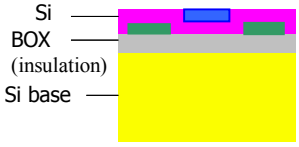
The flexibility of the Smart Cut technology extends beyond the silicon world to applications in photonics, opto-electronics, high frequency and high power devices, due to the development of hetero-composite substrates. The benefits of Smart Cut are numerous: it is scalable to any wafer size; it allows multiple exfoliations of a donor substrate; and it has the flexibility to combine single crystal thin films of a given material with another substrate material to engineer a wafer for a targeted application.

To broaden the domain of engineered substrates, Soitec has joined forces with CEA-LETI to create SCEALAB. This new R&D unit represents the first lab entirely devoted to Smart Cut and the development of leading edge materials for the most advanced integrated circuits. Researchers at the lab are working on several key applications that expand the patented Smart Cut technology for a new generation of substrate materials.

An overview of some of the current and potential substrates that can be engineered using Smart Cut follows in the table below.

Table 1. Examples of substrates that can be engineered using the Smart Cut process

	**SOI (Silicon-On-Insulator)** – used by most chip manufacturers at the 90nm node (2003), but planned by nearly all for the 65nm node (2006) and subsequent nodes (45nm in 2009, and so forth). In SOI, a layer of insulation is introduced between the top face of the silicon wafer, where the chips are fabricated, and the supporting base silicon. Soitec's line of SOI wafers is the UNIBOND family. Shin Etsu Handotai has also sub-licenced the Smart Cut process technology to use in producing SOI wafers for its customers.
	**SOQ (Silicon-On-Quartz)** – now is being used in substrates for specialized LCDs and high-frequency telecom applications. SOQ offers a single crystal silicon layer on a fused silica substrate, a development that will be extendable to Silicon-on-Glass. SOQ marks the first time the industry can couple the know-how behind state-of-the-art silicon IC integration with transparent substrates. Soitec has signed a long-term licensing agreement with Seiko-Epson for the production of SOQ wafers.
	**SGOI (Strained-Silicon-on-Silicon Germanium-On-Insulator)** – the first generation of strained silicon, SGOI is targeted for high-end logic applications (beginning in 2004). The production of strained Si substrates requires several Si and SiGe epitaxial steps to obtain the thin layer of strained silicon layer at the wafer surface. By transferring a thin layer of the relaxed $Si_{1-x}Ge_x$ from the starting epitaxial substrate to an oxidized handle wafer, an SOI-like structure is obtained. The strained Si film is epitaxially grown on relaxed $Si_{1-x}Ge_x$; the degree of strain achieved is a function of the germanium percentage. It has been shown that as a function of the level of the built-in strain in the Si lattice, a 50% enhancement of the electron and hole mobility can be achieved, which translates into improved MOSFET performance. Substrates with x=20% are available today with dislocation densities between 10^4 to 10^6 cm^{-2} and strained Si films of about 20nm.

	**sSOI (Strained Silicon-On-Insulator)** – in sSOI, the strained Si sits directly on the insulator – without the SiGe template. Since sSOI has the same basic structure as conventional SOI, it is expected that the film thicknesses will follow similar guidelines to those provided by the industry roadmap for SOI. While sSOI will likely be used for high performance logic applications, it is premature to speculate how the usage will be split between SGOI and sSOI. At the present time, sSOI is more complex to fabricate than SGOI; development efforts are currently establishing viable fabrication strategies for high-volume sSOI production.
 Example of SiCOI (SiC 6H on axis / oxide / poly SiC)	**SiCOI (Silicon Carbide-On-Insulator)** – Silicon Carbide (SiC) engineered substrates are attractive for the development of high-temperature, high-power, high-frequency and GaN-based optoelectronic devices. SiCOI is compatible with the very high temperature SiC and GaN epitaxial processes (>1000°C). The transfer of SiC thin films onto low-cost substrates such as silicon or poly-crystalline SiC wafers is an important characteristic of such composite substrates. However, some key substrate issues for wide band gap materials such as SiC and GaN are still under investigation.
	**GeOI (Germanium-On-Insulator)** – Germanium on a silicon substrate is another very promising development. Ge offers a higher mobility than Si and is better suited for the formation of high-k gate oxides, which are deposited in an oxygen rich atmosphere. In addition to microelectronics, GeOI is of interest for the manufacturing of solar cells (if combined with a GaAs epitaxial step). GeOI has been successfully demonstrated; research continues into high-volume manufacturing strategies.
 Example of Silicon-on-plastic	**Silicon-On-Anything (SOA) –** The know-how acquired in SOI development has opened another door: precise control of the bonding energy to allow post-processing debonding of the structure. The debonding technology of IC-processed silicon layers makes it possible to obtain silicon films 100 times thinner than those achieved by the state-of-the-art wafer thinning techniques. Fully processed IC wafers are commonly lapped down to a thickness of 100 to 150µm; the smart card industry requires wafer thinning down to 40-50µm, the state-of-the-art today. With debondable Smart Cut wafers, wafer-scale processed silicon films in the range of 0.2 to 1µm thickness can be obtained. The availability of this wafer technology will empower the IC industry with a wide range of totally new solutions and applications mainly in packaging, very flexible smart-cards, and 3D-SoC. It has been successfully demonstrated, and research continues.
	**Silicon-on-Insulating-Multilayers** – the possiblility of bonding two different buried layers (one silicon nitride and one silicon dioxide film, for example) to produce layer transferred silicon films over a multi-layer insulating structure has recently been demonstrated.
	**Patterned layer transfer** – SOI-like patterned layers are heterogeneous structures that may find a broad set of applications, ranging from double-gate transistors to System-on-Chip architectures. They may combine different technologies, such as fully depleted SOI, partially depleted SOI and bulk silicon, depending on the design requirements of a given chip. It is currently at the research stage.

About Soitec

Soitec was created in 1992 by two researchers from CEA-LETI in Grenoble (one of Europe's largest microelectronics research institutes). Their goal was to industrialize the SOI (Silicon On Insulator) processes and materials that had been developed for specific, low-volume applications, and make SOI viable for high-volume, commercial applications.

The company soon established itself as the industry's technological leader with its revolutionary and exclusive process for fabricating SOI wafers, Smart Cut. Today, the goal set forth by Soitec's founders has been realized: Soitec is now recognized by the principal players in the semiconductor industry as the international leader in SOI material for high-volume applications for commercial markets.

Soitec is the world's leading manufacturer and supplier of SOI wafers, with greater than 80-percent market share. Headquartered in Bernin, France, Soitec provides a broad range of advanced thin-film substrates for IC manufacturing, including bonded SOI (UNIBOND) and silicon-on-quartz (SOQ) wafers. Soitec is traded on the French "Nouveau Marché" Euronext Paris (Sicovam code 7206). Additional information is available on the Internet at www.soitec.com.

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