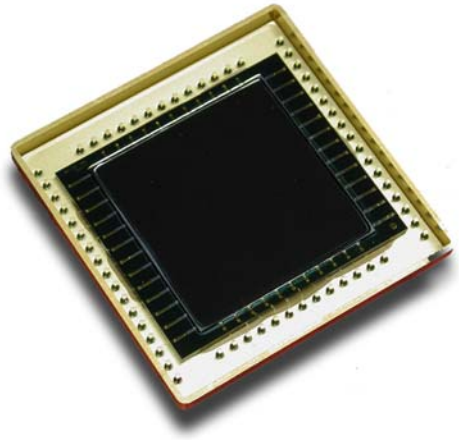
CCD447
2048 x 2048 Pixel Image Area
Full Frame CCD Image Sensor

FEATURES

- **2048 x 2048 Full Frame CCD Array**
- **15 µm x 15 µm Pixels**
- **30.72 mm x 30.72 mm Image Area**
- **100% Fill Factor**
- **Available in Front and Back Illuminated Formats**
- **Multi-Pinned Phase (MPP) Operation**
- **Readout Noise Less Than 4 e^- at 50k pixels/sec**
- **2 Low Noise Output Amplifiers (LR, UL)**
- **2 High Speed Output Amplifiers (LL, UR)**
- **Split Vertical Register**
- **Supports up to 2x2 Binning**



Back-illuminated CCD447 Mounted in Kovar Package

GENERAL DESCRIPTION

The CCD447 is a 2048 x 2048 active element solid state Charge Coupled Device (CCD) Full Frame sensor. The CCD is intended for advanced scientific, space, industrial, and commercial digital imaging applications. The CCD447 is organized as an array of 2048 horizontal by 2048 vertical imaging elements. The pixel pitch is 15µm with a 100% fill factor. Three-phase clocking is employed in the imaging area as well as in the serial readout registers. Image readout is performed via two serial registers containing 16 overscan pixels at each end. For added flexibility, each serial register is connected to a high speed on-chip output amplifier on one end and to a low-noise output amplifier on the other end. A split vertical register architecture allows the signal charge to be read out to the upper and the lower serial registers simultaneously. The imager is available in a frontside as well as back-illuminated configuration (as shown in photo at right).

The low-noise output amplifiers feature a single stage source follower design while a dual-stage design was chosen for the high-speed readout amplifiers. The nominal read noise of the low-noise and high-speed output amplifiers is respectively 3.6 e^- and 4.8 e^- at a pixel rate of 50 kHz.

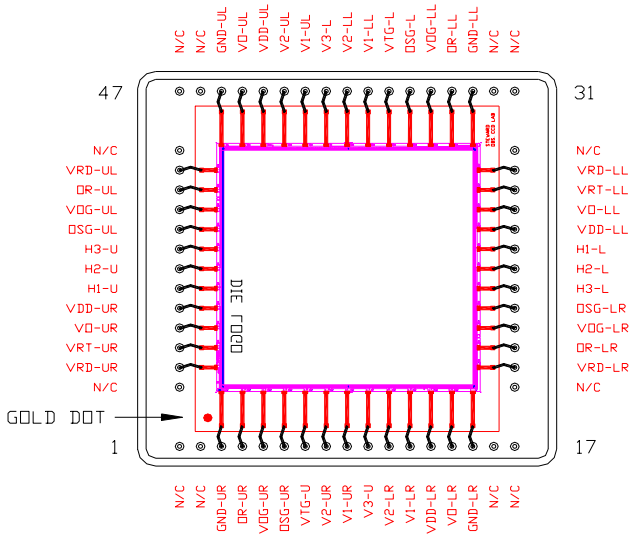
The CCD447 is normally available mounted in a solid-sidewall Kovar tub package with 56-pins (frontside) and 60-pins (backside). The pinout diagrams for the frontside and back-illuminated devices are shown below. The overall dimensions of the frontside and back-illuminated packages are 1.6” x 1.6” and 2.0” x 2.0”, respectively.

FUNCTIONAL DESCRIPTION

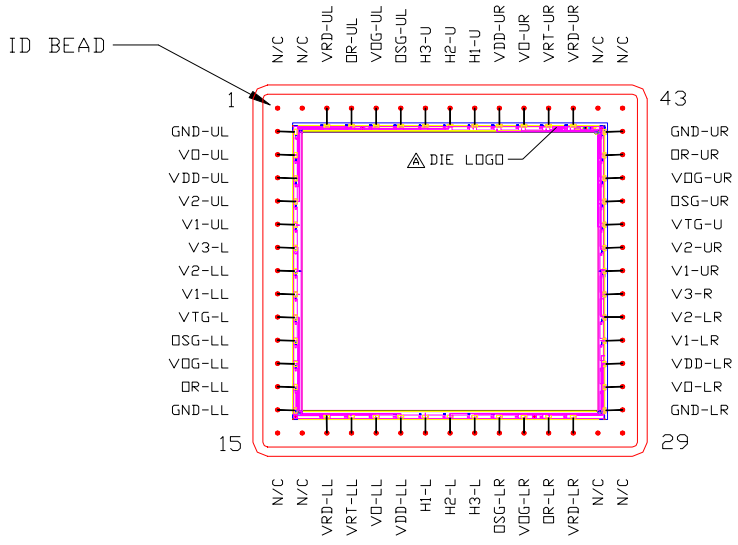
The following functional elements are illustrated in the block diagram:

Image Sensing Elements: In frontside illumination mode, incident photons pass through a transparent polycrystalline silicon gate structure creating electron hole pairs. The resulting photoelectrons are collected in the photosites during the integration period. The amount of charge accumulated in each photosite is a linear function of the localized incident illumination intensity and integration period.

In the backside illuminated mode, incident photons are collected on the backside of the CCD which has been thinned to about 12–18 microns. An accumulated surface potential helps direct the generated charge to the CCD depletion wells and is accomplished by applying a special surface treatment to the backside. The backside

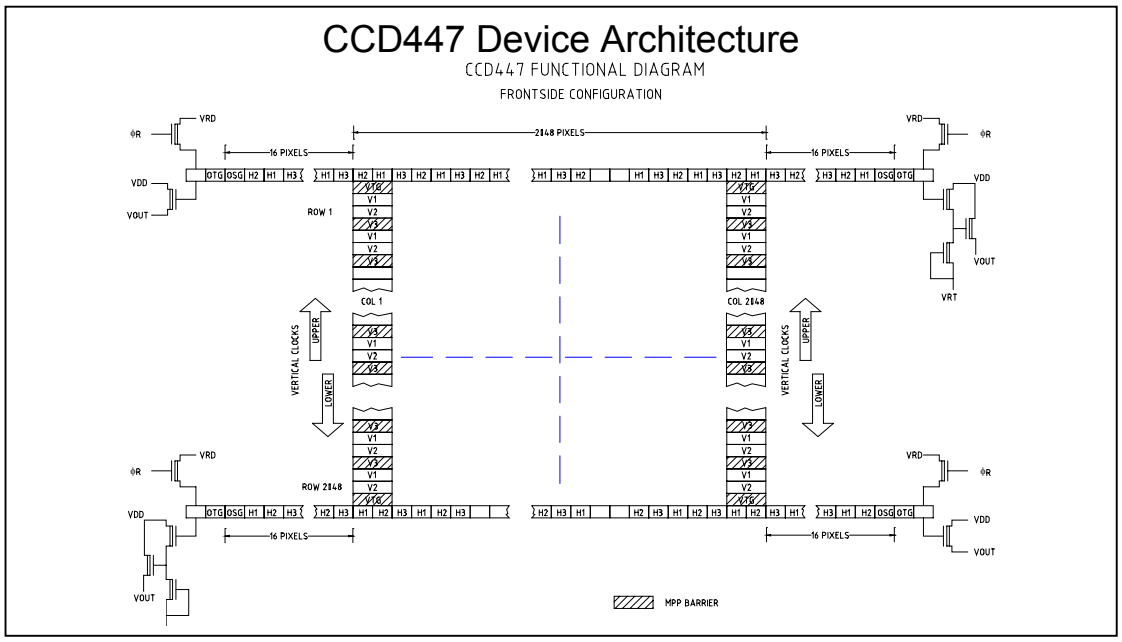


Back-illuminated CCD447 Pinout



Front-illuminated CCD447 Pinout

Fairchild Imaging, Inc., 1801 McCarthy Blvd, Milpitas 95035, (800) 325-6975, (408) 433-2500



antireflection coating can be tailored to optimize the device sensitivity over specific spectral regions.

The photosite structure is made up of contiguous CCD elements with no voids or inactive areas. In addition to sensing light, these elements are used to shift the image signal vertically. As a consequence, the device needs to be shuttered during readout.

Vertical Charge Shifting: The architecture of the CCD447 provides video information as a single sequential readout of 2048 lines containing 2048 photosensitive elements or 2 x 1024 lines of 2048 elements in split mode. At the end of an integration period, the ϕV_1, ϕV_2, and ϕV_3 clocks are used to transfer charge vertically through the CCD array to the horizontal readout register. Vertical columns are separated by a channel stop region to prevent charge migration.

The imaging area is divided into two equal sections. Each 1024 x 2048 section may be clocked independently or combined as required. Horizontal serial registers located at the top and bottom of the array permit simultaneous readout of the upper and lower halves. The CCD447 also may be clocked such that the entire array is read out from the upper or the lower serial registers.

The Vertical Transfer Gate (ϕVTG) is the final array gate before charge is transferred to the serial horizontal shift registers. For simplified operation ϕVTG may be tied to ϕV_3.

Horizontal Charge Shifting: ϕH_1, ϕH_2, and ϕH_3 are polysilicon gates used to transfer charge horizontally to the output amplifiers. The horizontal transport register is twice the size of the photosite to accommodate vertical binning. In binned mode, the array can be operated normally at full resolution, as a 1024 x 2048, or 1024 x 1024. The image may be read out to one output amplifier per serial register.

The transfer of charge into the horizontal register is the result of a vertical shift sequence. This register has 18 additional register cells between the first pixel of each line and the output gate. The output from these locations contains no signal and may be used as a dark level reference. (Note: The serial registers are not shielded, so care must be exercised to avoid exposure to incident illumination for proper operation.)

The last clocked gate in the horizontal registers is twice as large as the others and can be used to horizontally bin charge. This gate requires its own clock, which may be tied to ϕH_1 for normal full resolution readout. The output video is available following the high to low transition of ϕSG.

The reset FET in the horizontal readout, clocked appropriately with ϕR, allows binning of adjacent pixels.

Output Amplifier: The CCD447 has an output amplifier at each end of the horizontal registers for a total of four output ports. They are single-stage and dual-stage floating diffusion amplifiers with a reset MOSFET tied to the input gate.

Charge packets are clocked to a pre-charged capacitor whose potential changes linearly in response to the number of electrons delivered. This potential is applied to the input gate of an NMOS amplifier producing a signal at the output V_{out} pin. The capacitor is reset with ϕR to a pre-charge level prior to the arrival of the next charge packet except when horizontally binning. It is reset by use of the reset MOSFET.

The output amplifier drain is tied to VDD. The source is connected to an external load resistor to ground. The source constitutes the video output from the device.

Multi-Pinned Phase: MPP is a CCD technology which significantly reduces the dark current generation rate. CCDs are endowed with this capability by the addition of an ion implant step during the semiconductor manufacturing process.

This implant creates a virtual well in the array, which allows charge integration while maintaining pixel integrity with the vertical clocks in the low state. Leaving the vertical clocks in the low state during the integration cycle is the method used to implement MPP mode.

A drawback to utilizing the MPP mode is reduced full well capacity. The virtual well created by MPP implant does not hold as much charge as the normal buried channel operating mode which leaves one vertical clock in the high state during integration. The CCD447 may be operated in the conventional buried channel mode with an increase in charge capacity over the MPP mode.

DEFINITION OF TERMS

Charge-Coupled Device A charge-coupled device is a monolithic silicon structure in which discrete packets of electron charge are transported from position to position by sequential clocking of an array of gates.

Vertical Transport Clocks ϕV_1, ϕV_2, ϕV_3 the clock signals applied to the vertical transport register.

Horizontal Transport Clocks ϕH_1, ϕH_2, ϕH_3 the clock signals applied to the horizontal transport registers.

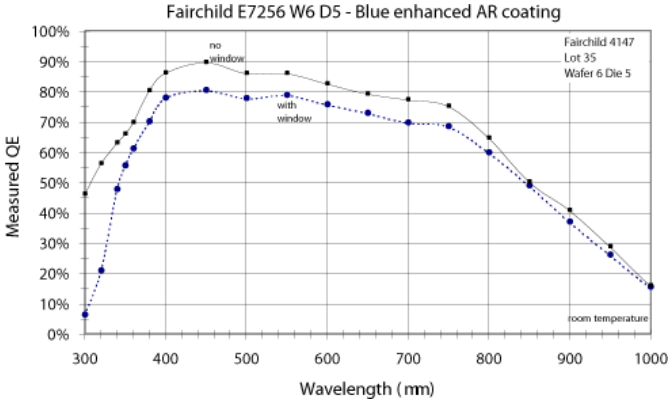
Reset Clock ϕR the clock applied to the reset switch of the output amplifier.

Dynamic Range The ratio of saturation output voltage to RMS noise in the dark. The peak-to-peak random noise is 4-6 times the RMS noise output.

Saturation Exposure The minimum exposure level that produces an output signal corresponding to the maximum photosite charge capacity. Exposure is equal to the product of light intensity and integration time.

Responsivity The output signal voltage per unit of exposure.

Spectral Response Range The spectral band over which the response per unit of radiant power is more than 10% of the peak response.



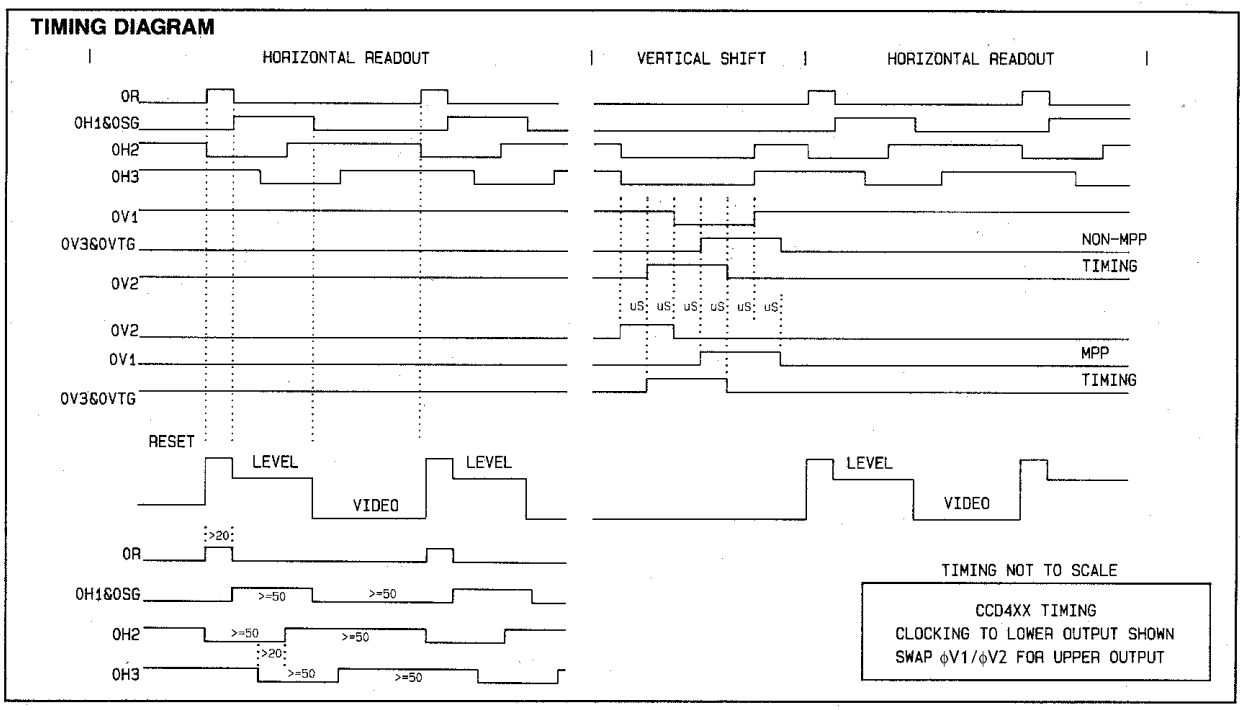
Quantum Efficiency Response of Back-illuminated CCD447

Photo-Response Non-Uniformity The difference of the response levels between the most and the least sensitive regions under uniform illumination (excluding blemished elements) expressed as a percentage of the average response.

Dark Signal The output signal in the dark which is caused by thermally generated electrons. Dark signal is a linear function of integration time and an exponential function of chip temperature.

Vertical Transfer Gate ϕVTG Gate structures adjacent to the end row of photosites and the horizontal transport registers. The charge packets accumulated in the photosites are shifted vertically through the array. Upon reaching the end row of photosites, the charge is transferred in parallel via the transfer gates to the horizontal transport shift registers whenever the transfer gate voltage goes low.

Pixel Picture element or sensor element, also called photoelement or photosite.



DC OPERATING CHARACTERISTICS

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT	REMARKS
V_{DD}	DC Supply Voltage	Low noise amp		24			
		High speed amp		24		V	
V_{RD}	Reset Drain Voltage	Low noise amp		17		V	
		High speed amp		17		V	
V_{OG}	Output Gate Voltage	Low noise amp		0		V	
		High speed amp		0		V	
VRT	Active load bias	High speed amp only		+2.5		V	
V_{SS}	Substrate Ground		`	0		V	

TYPICAL CLOCK VOLTAGES

SYMBOL	PARAMETER	HIGH	LOW	UNIT	REMARKS
$V\phi_{H(1,2,3)}$	Horizontal Multiplexer Clock	+5	-5	V	
$V\phi_{SG}$	Summing Gate Clock	+5	-5	V	
$V\phi_{V(1,2,3)}$	Vertical Array Clocks	+3	-8	V	
$V\phi_{R}$	Reset Array Clock	+8	0	V	
$V\phi_{VTG}$	Array Transfer Gate Clock	+3	-8	V	

Note 1: ϕH = 400 pF, ϕV = 60,000 pF. All clock rise and fall times should be > 10 ns.

AC CHARACTERISTICS Standard test conditions are nominal MPP clock and DC voltages, Horizontal clock frequency: 400 kHz, Vertical clock frequency: 2.5 kHz.

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT	REMARKS
R_{load}	Load Resistor	Low noise amp		12		KΩ	
		High speed amp		5		KΩ	

PERFORMANCE SPECIFICATIONS

SYMBOL	PARAMETER	MIN	NOM	MAX	UNIT	REMARKS
V_{SAT}	Saturation Output Voltage	160	250		mV	Note 2
FW	Full Well Capacity (MPP)	80	100		ke-	
OCG	Output Amplifier Conversion Gain	2	2.5		μV/e-	
VCTE	Vertical Charge Transfer Efficiency		99.9997		%	
HCTE	Horizontal Charge Transfer Efficiency		99.9995		%	
PRNU	Photo Response Non-Uniformity, Peak-to-Peak		10		$\%V_{SAT}$	
DSNU	Dark Signal Non-Uniformity, RMS		25	50	pA/cm^2	Excluding white defects
DC	Dark Current (MPP)		25	50	pA/cm^2	Note 1
R	Responsivity		5		$V\mu J/cm^2$	Peak (frontside-illuminated CCD)

Note 1: Values shown are at 25^0C. Dark current roughly doubles for every 7 ^{0}C change in temperature.

COSMETIC GRADING

Device grading helps to establish a ranking for the image quality that a CCD will provide. Blemish content is determined in the dark, at various illumination levels and at different operating temperatures.

		Blemish Specification		
		Total Array		
Product	**Grade**	**Point Defects**	**Column Defects/ Max Defective Column Width**	**Clusters Defects**
CCD447	1	50	3/2	5
2048 x 2048 CCD	2	100	6/3	10
15-um pixels	3	500	20/5	40

Cosmetic Specifications Definition	
Point Defect	A pixel which does not meet the PRNU specification. PRNU is measured at 50% of Vsat.
Cluster Defect	A grouping of < 9 adjacent point defects (excluding colum defects)
Column Defect	A grouping of > 10 contiguous point defects in a single column.

The CCD447 is available in several different grades, as well as custom selected grades. Consult with Sales representative for available grading information and custom selections.

WARRANTY

Within twelve months of delivery to the original customer, Fairchild Imaging will repair or replace, at our option, any Fairchild Imaging camera product if any part is found to be defective in materials or workmanship. Contact Customer Service for assignment of warranty return number and shipping instructions to ensure prompt repair or replacement.

CERTIFICATION

Fairchild Imaging certifies that all products are carefully inspected and tested at the factory prior to shipment and will meet all requirements of the specifications under which it is furnished

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This product is designed, manufactured and distributed utilizing the ISO 9000:2000 Business Management System.