Palladia™ 402

*Integrated CPE ADSL VoIP Gateway*

product brief

End users in DSL markets around the world are driving service providers to deploy high bandwidth content and services. These include VoIP (Voice over Internet Protocol), VoD (Video on Demand), Streaming Media, Security, and Online Gaming. There are a variety of Home Networking methodologies for local distribution of this rich content including Ethernet, USB and WiFi. As customers demand all that broadband access enables, service providers must deploy robust ADSL CPE solutions with the bandwidth and features to accommodate these services. Ikanos' Palladia™ family of high-performance, feature rich, ADSL/ADSL2/ADSL2+ CPE solutions deliver what customers and service providers demand from their ADSL/ADSL2/ADSL2+ equipment vendors.

The Palladia 402 ADSL2/2+ gateway processor with integrated VoIP DSP and robust SIP Software Stack is targeted at the burgeoning VoIP market. The Palladia 402 addresses the explosive growth in the ADSL and VoIP markets around the globe. This multi-services Gateway on a Chip solution provides a rich feature set for both VoIP and ADSL2/2+ while lowering costs and enabling fast time to market for equipment vendors and services providers.

- **Highly Integrated, High Performance ADSL/ADSL2/ADSL2+ CPE**
- **Integrated Voice DSP**
- **Robust SIP/Firewall/VPN/Router Stack**
- **Hardware Encryption Accelerator with Enhanced IPQoS**
- **Packet Header Processor**
- **PCI with Glueless Interface to most Mini-PCI WIFI Modules**
- **Two 10/100 Ethernet MAC Interfaces**

Application Diagram
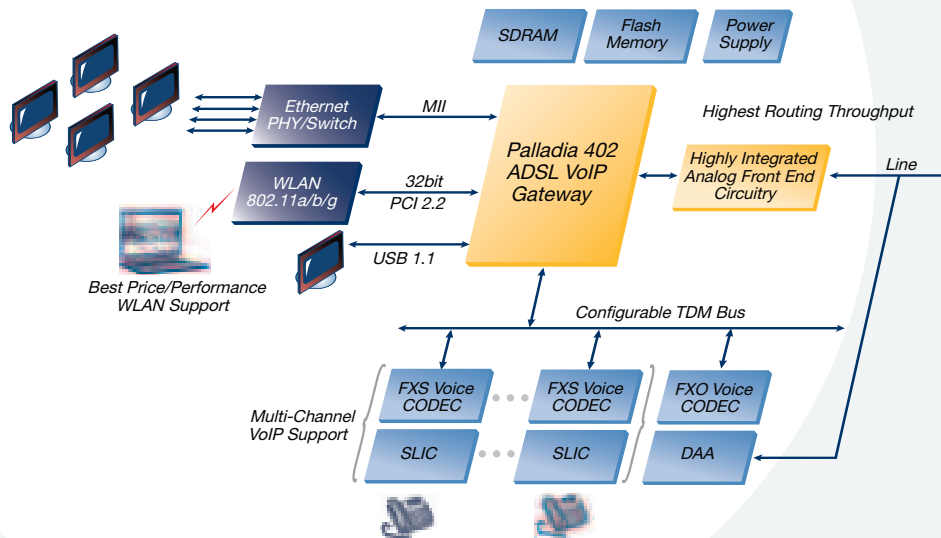
Palladia 402 Product Ordering Information

Product	VoIP Channels	Function	Part Number	Package
Palladia 402 ADSL + (Annex A/B)	1	Digital Chip	CT-P57DI12-PJ	256-pin LBGA
	2		CT-P57DI22-PJ	
	4		CT-P57DI42-PJ	
		Analog Chip	CT-P57DI12-TQ	80-pin TQFP-ep

NOTE: The chipset must be ordered in sets. Orders of individual components are filled as chipset orders.

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System Architecture

The Palladia 402 is a highly integrated solution for VoIP enabled ADSL2/2+ gateways and IADs. This solution integrates a highperformance 200 MHz network processor, a dedicated voice DSP, a hardware encryption accelerator, a packet header processor, a USB interface, a PCI interface, and two RMII interfaces. The Palladia 402 provides a completely integrated datapump for ADSL with speeds of up to 50 Mbps downstream and 5 Mbps upstream.

Voice Functionality

The Palladia 402 gateway integrates a 200 MHz DSP core for voice processing. The DSP core has four execution units with a VLIW architecture, 8-Kbyte I-cache and 16-Kbyte D-cache, and is supported by DMA and hardware messaging facilities. The DSP firmware is included with extensive voice compression and processing capabilities. The Palladia 402 software library provides a rich set of APIs for DSP, QoS, and a full suite of RTP/RTCP and SIP protocol stacks.

Hardware Encryption Accelerator

The Palladia 402 Hardware Encryption Accelerator supports three major VPN modules: IPSec, IKE, and L2TP. The IPSec module supports DES, 3DES, and AES encryption, as well as SHA1 and MD5 hashing in hardware.

Packet Header Processor

The PHP (packet header processor) assists the network processor by off-loading many of the routine packet pre-processing tasks. Many of these packet pre-processing tasks are not only done faster, but are done in an independent packet processor, which frees up CPU cycles.

For more information, contact Ikanos.

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Key Features and Benefits

- **Highly integrated ADSL2/2+ SoC for residential, SOHO, and SMB applications**
- Digital chip with integrated network processor, ADSL data pump, packet header processor, hardware encryption engine, and voice DSP
- AFE (analog front-end) chip includes integrated ADSL front end and line driver, High Level of Integration such as Analog EC, Analog Pre-emphasis ,internal active filter and adaptive Hybrid Impedance matching to eliminate sensitive components and lower the BOM cost

- **Palladia 402 integrates**
- ADSL modem Network processor
- Hardware AES, DES, and 3DES encryption
- Packet header processor
- Voice DSP and codec
- PCI
- USB
- Network interfaces (two Ethernet MACs)

- **Embedded ADSL2/2+ PHY with eXtremeDSLMAX feature set support**
- Quad, double, and single spectrum ADSL2/2+
- G.lite, G.dmt (ITU-T G.992.2 and G.992.1), and T1.413
- ADSL2 (G.992.3 and G.992.4)
- ADSL2+ (G.992.5)
- ADSL2++ (Quad spectrum downstream and double upstream)
- Annex A, B, C, M, and L
- TR048, TR067, TR100, and UR-2 Compliant
- ATM over DSL
- TC-layer hardware acceleration

- **Data support**
- Integrated RISC processor: 200MHz MIPS with 16-Kbytes instruction cache, 8-Kbytes data cache, 32- Kbytes boot RAM, and MMU
- Hardware AES, DES, 3DES, MD5, and SHA-1 encryption engine
- Two 10/100 Ethernet MAC interfaces with standard RMII or one MII
- USB interface
- Hardware traffic shaping for eight VCCs
- Packet-level traffic shaping as well as classification and marking

- **QoS support**
- Packet header processor with ingress queuing for fast incoming traffic preprocessing and TCP/IP functionality offload as well as IPQoS
- Hardware support for ATM VCC demultiplexing

- RFC 1483/RFC 2684 (routing or bridging; LLC or VC multiplexing)
- PPP-over-ATM (RFC 2364)
- CBR/UBR/UBR with PCR Shaping/VBR-rt/VBR-nrt
- Eleven VCCs supported in hardware, additional VCCs supported in software
- I.610 OAM F4/F5 loopback/AIS/RDI/continuity check
- ILMI and support for TR037
- RFC1577/RFC 2225 (classical IP over ATM) data networking and management
- SNMP v1/v2 (ADSL/ATM/MIB2)
- NAPT with over 50 ALGs
- TCP/IP with RIP1 and RIP2 (RFC 1058, RFC 1389)
- DHCP server and client (RFC 2131)/DHCP relay
- DNS

- **Voice features**
- Integrated DSP Processor: VLIW architecture 200 MHz voice DSP supports up to four channels of deep compression codecs
- Supports one FXO and four FXS channels
- G.711 (PCM), G.729a/b, G.726-32, and G.723.1 AMR narrowband codes
- Supports generic VAD (voice activity detection) and CNG (comfort noise generation)
- G.711 fax/modem pass-through (fax/modem detection and reversion to PCM 64 kbps)
- Supports T.38 fax
- Supports caller ID, including JCLIP
- Supports call forwarding and call waiting
- G.168 echo cancellation with programmable echo tail length from 8 to 128 ms
- DTMF tone generation and detection Q.21/Q.23/Q.24
- Adaptive and configurable jitter buffer
- Jitter buffer size of 300 ms
- Message waiting indicator and call hold
- Pulse dialing
- Dual FXS or FXS/FXO modes

- **Interfaces and memory**
- 16-bit PC Card and 32-bit PCI
- SPI interface with four chip selects for serial flash, Ethernet switches, and SLIC/SLACs
- PCM/IOM2 interface with programmable time slots
- Boot loading and configuration using either parallel flash on PC Card bus, serial flash on SPI bus, or external host on PCI bus
- Support for 16/32-bit wide SDRAM memory
- Two integrated Ethernet MACs with industry standard RMII interface or one MII
- USB