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Design of a Printed Card Capacitor Read-Only Store

Abstract: The Printed Card Capacitor Read-Only Store system is introduced as one of three Read-Only Store (ROS) technologies presently employed in the IBM System/360 computers. A detailed description is given of the elementary storage structure—a capacitor matrix with a novel arrangement for rapidly and economically changing the matrix configuration. The changeable element is an etched or printed Mylar card, prepared with standard IBM card-punch equipment. The assembly of storage structures into a compact 4032-word, 60-bit module is described. Considerations involved in the selection of matrix parameters are reviewed and a theoretical analysis of matrix performance is presented. It is shown that some of the limitations associated with a linear matrix are minimized by an incomplete integration of the matrix output. The impact on over-all ROS performance of factors external to the capacitor matrix is considered. These factors include the effects of a noisy drive system and the asymmetrical character of the matrix relative to the access circuitry. Computed and observed results are compared for typical System/360, Model 30 ROS operation. The actual matrix response amplitude is observed to be greater than the computed value due to the level of system background noise; however, computed and observed waveforms are otherwise in good agreement.

Introduction

Much interest has recently been shown in the computer art in incorporating a low-cost, mechanically changeable, read-only store in the control section of a central processing unit. Flexibility of organization and compatability with other systems can be built into a computer that has a readily changeable read-only store. The printed Card Capacitor Read-Only Store is one of three technologies selected for the ROS function in System/360[1,2] and is currently employed in the Model 30. Other technologies selected have been partially or fully described in previous papers.[3,4]

The ROS operation is based on the capacitor matrix. The pattern of line intersection coupling capacitors, Fig. 1, represents stored words of binary information. A pulse or sinusoidal voltage applied to any given address conductor or word line reads out the stored word by producing signals simultaneously on all sense conductors or bit lines coupled at the intersection with the addressed word line. Ideally, no signals appear on the uncoupled bit lines.

Gutenmakher[5] reported the use of a capacitor matrix for information storage in 1956. Subsequently, Van Goethem,[6] MacPherson and York,[7] and Foglia, McDermid, and Petersen[8] reported implementation of capacitor matrix information storage devices with various degrees of changeability.

The concept of a removable card to change the in-

formation content has occurred to many workers utilizing various ROS technologies.[6,8,9] Foglia, McDermid, and Petersen, in applying this concept, made a significant contribution by utilizing a thin, replaceable, electrostatic

Figure 1 Capacitor matrix for binary read-only information storage.
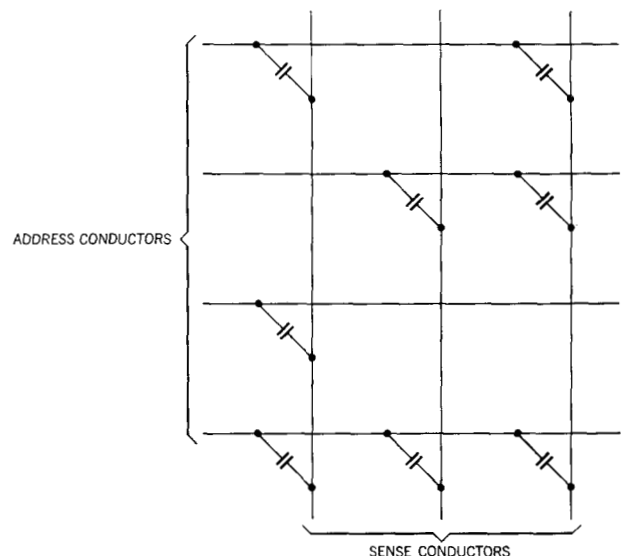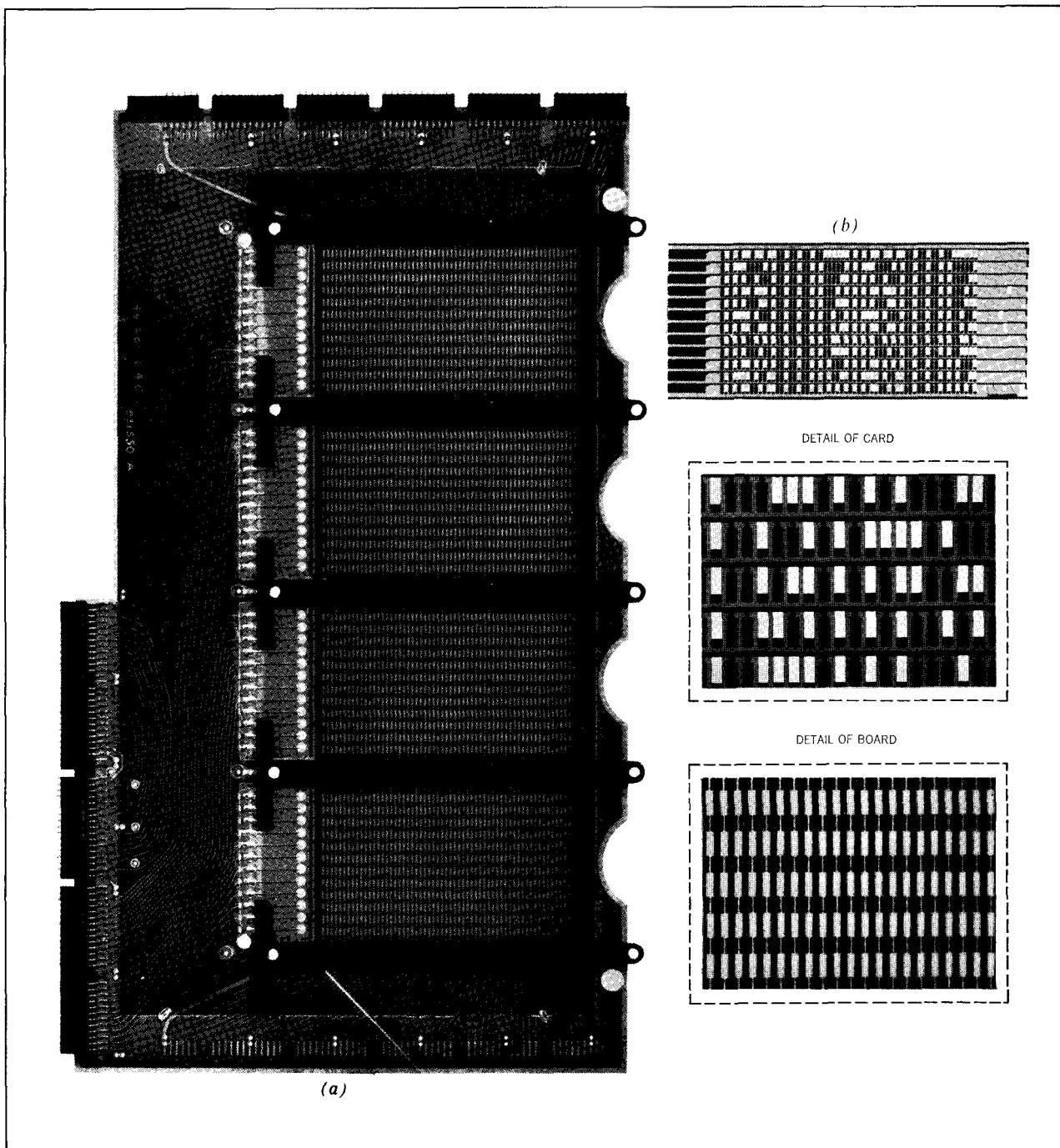
Figure 2 Basic structure of card-capacitor read-only store. (a)8-card storage board (4 cards per side) containing vertical bit-lines; (b) information document containing horizontal word-lines with punched-hole pattern. Holes represent binary ZERO's and unpunched positions represent binary ONE's.

shield and a capacitor matrix with dimensions compatible with the standard paper tabulating card. This permitted the electrostatic shield to be prepared for data storage by standard card-punch equipment.

The Printed Card Capacitor Read-Only Store also uses a replaceable element with tabulating card dimensions for convenience in data preparation; however, this element contains a printed or etched circuit rather than an electrostatic shield. A brief description of the storage element has been given in an earlier letter by Haskell.[10]

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The present paper gives a more detailed discussion of the problems involved in designing a storage unit that uses this element.

Description

The basic storage structure consists of two orthogonal sets of line conductors separated by a thin insulating film. These line sets are shown separately in Figs. 2a and 2b. All line conductors have rectangular enlargements or spots at regular intervals corresponding to the hole spacing of the IBM punched card system. When the horizontal set of lines is placed over the vertical set of lines in proper registration, the spots and the intervening film form the coupling elements of a capacitor matrix.

The set of vertical lines is etched on the surface of a copper-clad, epoxy-glass sheet, fixed in position on what is called a storage board. After the lines are etched, a layer of 5-mil Mylar* film is bonded to the surface. This film serves as the dielectric of the matrix coupling elements.

The set of horizontal lines is the removable or replaceable element, referred to as the information document. This document is a sheet of Mylar film cut to the dimensions of an ordinary 80-column paper card. One side of the film contains either etched copper lines or else silver ink printed lines. The large tabs at the end of the horizontal lines are gold-plated to assure contact with the connector wires adjacent to the vertical line set.

The dimensions and spacing of the pattern on the information document are such that holes can be punched at any spot so as to sever the connection between the spot and the horizontal feeder line (see detail, Fig. 2b). A "bottleneck" connection is used between spot and feeder line to allow for the tolerance on the punched hole position. The punched hole effectively eliminates one plate of the matrix coupling element.

It is essential in this linear matrix that the coupling capacitors represented by the intersections of the horizontal and vertical lines be extremely uniform. This requires the replaceable information document to be accurately positioned over the fixed set of lines and to be held in intimate, uniform contact with the insulating film. In the present design, the replaceable document is inserted manually between the card locators, and moved until the card comes in firm contact with the card stop. This assures correct card positioning.

To force the card into uniform contact with the insulating surface (and assure electrical contact between the opposing terminals) a plastic air cell, located above the card, is inflated. When the air cell is inflated to a pressure of a few pounds per square inch, it provides a uniform resilient pressure to the back of the card and accommodates itself to any variations in thickness of the various parts. A small air pump provides the static pressure required to keep the air cell inflated.

It is essential that the difference between coupling capacities of punched and unpunched intersections be at least one order of magnitude for a matrix of useful size. This requirement is met by closely sandwiching the line sets between two ground planes to suppress fringing effects. By this means an unpunched-to-punched intersection coupling-capacity ratio of 10 to 1 is attained. In addition, the closeness of the ground planes minimizes line-to-line coupling between adjacent lines of both input and output sets.

One plane is provided by an internal ground plane in the storage board, spaced 0.020 in. from the vertical line set. The second ground plane, spaced 0.010 in. from the horizontal line set, is provided by a sheet of 3-mil, copper-clad, Mylar film located between the back of the replaceable card and the air cell. This ground plane is made flexible to transmit the pneumatic pressure exerted by the air cell and also to permit easy insertion and removal of the information document when the air cell is deflated.

In addition to minimizing unwanted couplings, the ground planes also present a shunt capacitive load to both sets of lines. This is both an advantage and a disadvantage. The advantage is that in a matrix of linear coupling elements it is necessary to attenuate the signal passing through in order to discriminate between wanted and unwanted outputs. The additional shunt loading improves this signal discrimination. The disadvantage of this added shunt capacity, which presents approximately 50% of the total load on both sets of lines, is that it tends to limit the operating speed. It increases the drive requirements for the input lines and increases the recovery time for both input and output lines.

No reason has yet been given for the choice of input or output lines. Theoretically, either set of lines could be used for either function. Practical considerations, however, require that the fixed vertical lines be used for the output or bit lines and the movable horizontal lines be used for the input or word lines. This provides a relatively protected environment, a solid electrical path, and a fairly stable shunt capacitive load for the low-level output signals. The horizontal lines are more exposed because of their large end-tab connectors, and the shunt load varies widely according to the punched hole pattern. The decisive consideration is the required ROS word length of 60 bits which can be most conveniently accommodated by the horizontal card row. As shown in Fig. 2b, each replaceable card contains 12 words of 60 bits each. A drive signal applied to a word line provides parallel read-out of the 60 bits. ONE bits and ZERO bits are represented by unpunched and punched intersections, respectively.
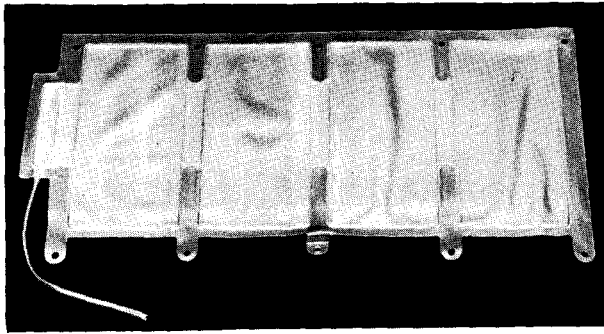
Figure 3 Storage board air cell for assuring contact between information document and storage board.

96 words of 60 bits each. The Model 30 ROS uses the latter arrangement with the output fed to 120 sense amplifiers arranged in 60 pairs for selective gating to 60 sense latches.

An important feature of the storage board construction is the use of adapter sockets at the input line terminals permitting packaged driver cards to be plugged directly to the board edge, thus eliminating the usual drive cables. This feature minimizes interaction between input lines, which can seriously degrade the performance of a linear matrix, and also brings in drive decode signals (described later).

The storage board air cell, fabricated from a flexible vinyl plastic, has four chambers (Fig. 3). The flexible ground plane, which encloses the air cell (not shown in the figure), is also in four segments corresponding to the air cell chamber dimensions.

The storage board, Fig. 2a, is a laminated double-sided structure with a set of 60 vertical lines on both sides, electrically isolated by an internal ground plane. The board is approximately 20 in. by 12 in. with positions for eight cards or information documents, four to a side. The 48 input lines per storage board side are connected to the corresponding lines on the opposite side by wires which are run through holes in the board. (Thus an input line drives two words.) Each storage board can therefore accommodate 48 inputs to provide the option of either 48 words of 120 bits each or, by means of output selection,

Storage structure of various word capacities is obtained by assembling the required number of storage boards and connecting the corresponding sense line of each board in parallel. At present, the most common module size built, Figs. 4a and 4b, has 43 boards and provides 4032 words of 60 bits each plus one spare board. Forty-four air cells are interleaved with the storage boards; individual air intake tubes are connected to an air manifold for simultaneous inflation or deflation.

The stacking density of the storage boards is determined chiefly by the 0.5 in. thickness dimension of the driver

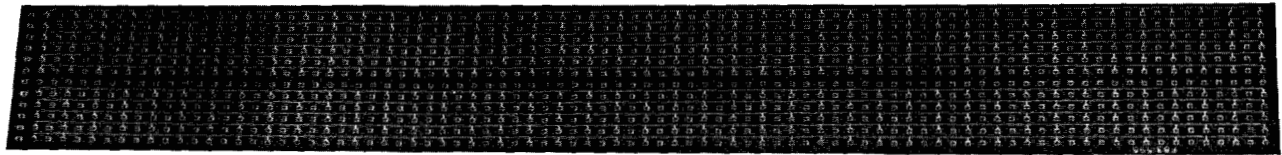**Figure 4** Laboratory model of 4032-word storage module. (a) front view; (b) rear view.
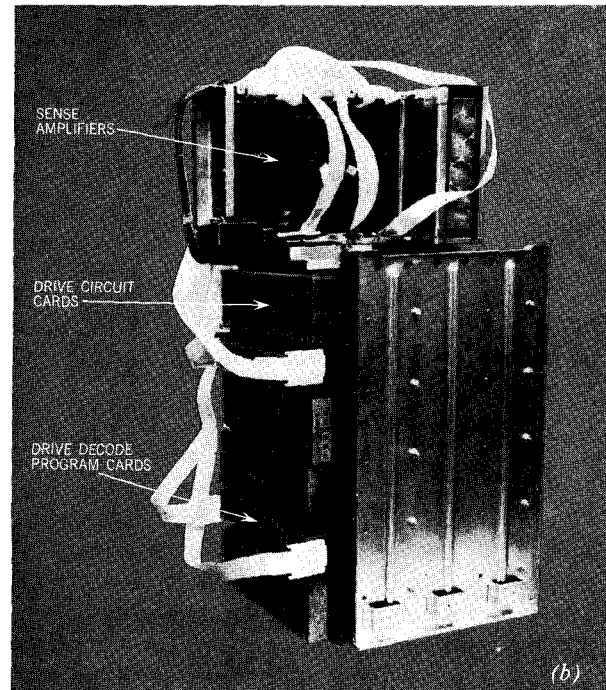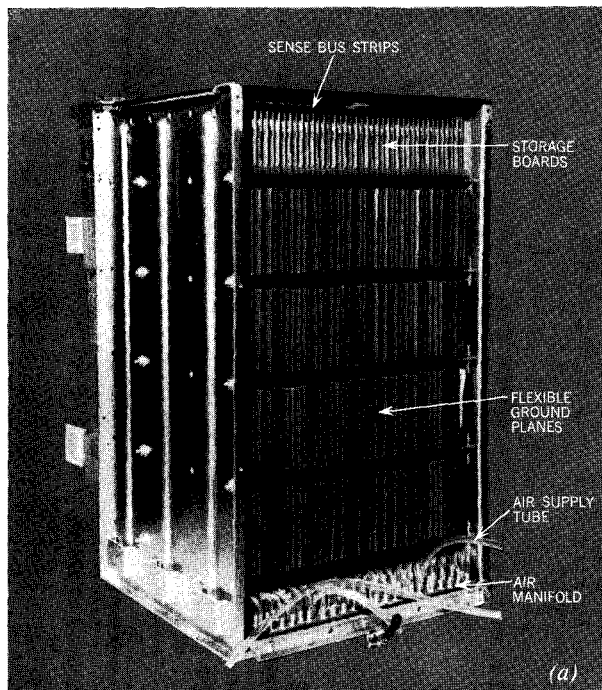
Figure 5 Sense bus strip.

sockets. To minimize this limitation, alternate boards are inverted in the assembly to stagger the adapter socket positions. This reduces the space between boards to 0.25 in. so that the 43-board structure, including end plates, has dimensions of approximately 20 in. × 12 in. × 12 in. To accommodate the board inversion, the vertical lines are extended to make either board end available for connection to a common sense bus.

The sense bus is constructed to parallel-connect the sense lines of each board by the shortest, most direct route possible. This is necessary to minimize signal transit time and line-to-line coupling. The sense bus for the 120 sense lines is made up of several laminated strips with internal ground planes similar in construction to the storage board. Each strip (Fig. 5) carries 22 etched lines, 11 to a side, with plated-through hole enlargements at 0.25 in. intervals corresponding to the storage board spacing. A line of plated-through holes down the middle of each strip provides connection to the internal ground plane. To assemble the strips to the board structure, adapter pins are attached to each storage board sense line and ground terminal, passed through the plated-through holes and soldered (Fig. 6). A shielded, twisted-pair cable, attached to the midpoint of the strips, connects the sense bus strips to the sense amplifiers.

Input to the ROS drivers is accomplished in a somewhat similar manner. The "next-word" address from the central processing unit is partially decoded by external circuitry; this partially decoded signal set is applied to two decode bus strips installed between the drive adapter sockets. At each storage board a pluggable wired circuit board called a program card is plugged onto the decode bus strip to direct the appropriate decode signals to each driver group. This feature permits great flexibility in drive addressing and, in the event of a board failure, minimizes the time required to disconnect the defective board and connect the spare board into the system.

Not all of the available area of the information document is used for information storage in the present application. This allows numbers and symbols to be punched in the blank area for visual or machine identification and sorting. In addition, the horizontal lines are extended along the full width of the card to provide a small tab at the right

end (see Fig. 2b) that is accessible for probing to facilitate checking the drive system.

An important feature of the Printed Card Capacitor Read-Only Store is the ease and rapidity with which the stored information may be changed. Only a few seconds are required to release the air pressure locking the cards in place. With the air pressure released the cards remain in place but can be freely removed or inserted. About two hours are required for one operator to replace the entire information document deck of 336 cards in the 4032 word module. Operation with a partial or incomplete deck is possible without any readjustments since the flexible ground plane provides equivalent loading to the output lines at all missing card positions.

The ROS in the present System/360, Model 30 operates on a cycle time of 0.75 μsec, although it is capable of higher speed. The input drive is nominally a 10-V, 75-mA

Figure 6 Cross section of storage board to sense bus connection.
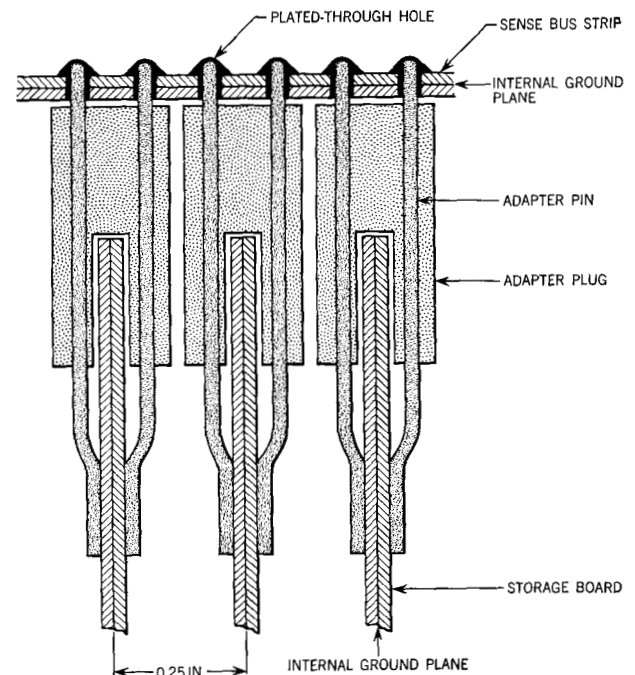
pulse of approximately 200 nsec duration. The matrix ONE signal output peak amplitude is nominally 1.7 mV at 140 μA. The ROS system over-all ONE/ZERO signal ratio is approximately 2 to 1.

Selection of matrix parameters

Performance specifications for the capacitor matrix are the following:

1. The peak input drive per 120-bit line shall not be more than 12 V or 150 mA.
2. The peak output ONE signal to sense amplifier shall not be less than 1 mV or 80 μA.
3. The basic matrix ONE/ZERO signal ratio shall not be less than 4 to 1.
4. Minimum matrix cycle time shall be less than 0.75 μsec.

The input and output requirements are set by the capabilities of economical drive and sense systems designed in SLT circuitry.[11] The basic ONE/ZERO ratio is chosen to allow for losses to be expected from system background noise and other external effects. The Model 30 operating conditions determine the cycle time.

The key matrix parameter is the line intersection coupling capacity. Since fringing effects are minor, the magnitude of this parameter is very nearly a linear function of plate area, plate separation, and dielectric constant of the intervening medium.

The plate configuration at the line intersections represents a compromise between the conflicting requirements of maximum area and minimum cross coupling between adjacent lines. Both plates have essentially the same dimensions with an area of 0.009 in.^{2}/plate at unpunched intersections. For a punched hole intersection the input plate area is reduced typically to 0.0008 in.^{2}

Present insulating films and bonding techniques combined with the given plate area allow the choice of intersection coupling to range up to about 5 pF. Cost consideration and uniformity requirements, however, limit the choice to certain discrete values corresponding to commercially available film thicknesses.

A value of 1 pF, obtained with 5-mil Mylar film, was chosen as the best compromise value of line intersection coupling. In combination with the glass-epoxy storage board material this provides a set of matrix parameters that satisfy the performance requirements. The matrix parameters of a 4032-word ROS are listed in Table 1.

The punch operation is responsible for the variation in shunt loading on the input and output lines. An apparent anomaly in the values requires explanation. For example, the input line load varies by a factor of 3 to 1. A small part of this is due to the unequal line lengths, but the major part is due to the punch operation which removes actual areas of the input line. The total shunt load per input line intersection is about 1.5 pF, so punching

Table 1 Matrix parameters

Parameter	Symbol	Value
Line intersection coupling	C_c	1.0 pF
Residual intersection coupling	C_r	0.1 pF
Input line-shunt load (max)	$C_{1(max)}$	310 pF
Input line-shunt load (min)	$C_{1(min)}$	107 pF
Input line-to-line coupling	$C_{L1(max)}$	7.1 pF
Output line-shunt load (max)	$C_{2(max)}$	5100 pF
Output line-shunt load (min)	$C_{2(min)}$	3700 pF
Output line-to-line coupling	$C_{L2(max)}$	120 pF
External resistive loading (input)	R_1	300 Ω
External resistive loading (output)	R_2	12 Ω

out all 120 spots (two card lines) removes 180 pF from the load seen by the driver.

The punch operation makes no change in the output line area; however, it replaces the 1.0 pF intersection coupling per spot by 0.35 pF shunt loading to the flexible ground plane which the output line spot "sees" through the punched hole. The shunt load per output line intersection can therefore vary from about 2.20 pF (no punch) to 1.55 pF (intersection punched).

Matrix performance

It is obviously impractical to determine the matrix performance for all possible punched hole patterns in the information documents. The analysis is therefore confined to certain patterns which, while unlikely to occur in practice, represent the limits within which all operation takes place. These extreme or worst-case patterns correspond to the maximum ONE, minimum ONE, and maximum ZERO matrix outputs.

Determination of the worst-case patterns is based on a lumped-parameter model of a complex-loaded capacitor matrix. Distributed-parameter effect and signal integration (discussed in later sections) modify the output wave shapes but do not appreciably affect the results obtained with the assumed model. The choice of patterns is further restricted by limiting the range of parameters to values known *a priori* to be compatible with the ROS structure. All coupling is considered to be capacitive. Since the input and output lines are at right angles, there will be negligible inductive intersection coupling; the line spacing, length, proximity of ground planes, and terminating loads are such as to reduce inductive line-to-line coupling to negligible values.

As a first step in determination of the worst case patterns, all possible paths or routes for signal feedthrough from input to output are considered. These routes are illustrated in Fig. 7 and identified as follows:

Route 1—Normal line intersection coupling at unpunched hole locations.

Route 2—Residual line intersection coupling at punched hole locations.

Route 3—Input line-to-line coupling.

Route 4—Output line-to-line coupling.

Route 5—Matrix or sneak path coupling.

The three worst-case patterns are presented in Fig. 8. The maximum ONE configuration has signal Routes 1 and 3 as a signal source and is based on the premise that the signal on a minimally loaded output line is greater than the signal on a maximally loaded line which also receives a contribution via signal Route 5. (No contribution is received via signal route 4 since all output lines are at the same potential) The minimum ONE configuration has maximum output line loading with only the normal line intersection coupling as a signal source. The maximum ZERO configuration receives contributions via all signal routes except Route 1. Equivalent circuits and transfer functions for all routes are developed in Appendix A.
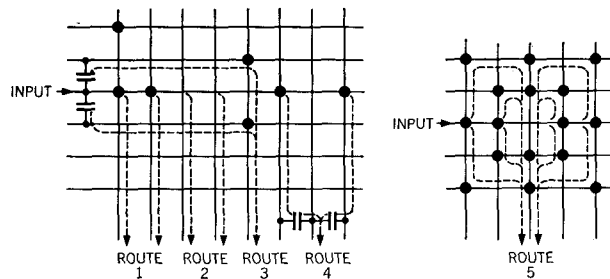
The matrix outputs for the three patterns are computed by applying an ideal ramp input function to each signal route separately, then combining the appropriate outputs. Figure 9a shows the results for an input of fixed amplitude and variable rise time.

It is evident that for the range of rise times given, the ONE/ZERO ratio is not adequate since under worst case it could fall to 2.5 to 1. Simple peak amplitude sensing would require either close control of input rise times, or else time sampling to blank out the first 50 nsec response.

An alternative is to sense the signal on some basis other than the instantaneous peak amplitude. The charge transferred from input to output via Route 1 is not a function of rise time or shunt loading but is proportional solely to the magnitude of the coupling capacity and the input voltage transition. Figure 9b shows the response for charge transferred, obtained by integrating the matrix outputs. It is evident that ONE/ZERO ratios up to about 10 to 1 can be obtained, provided sufficient time is allotted for sampling the matrix output.

The sampling time required for complete signal integration is too long for the ROS operation; however, by a judicious application of "incomplete" integration most of the improved signal discrimination is retained with only a moderate addition to the ROS access time. Figure 9c shows the results obtained with incomplete integration representative of the actual ROS operation. (The integration is equivalent to that provided by a single-stage RC filter with a 0.1 μsec time constant.) The ONE/ZERO ratio is more than required and is obtained at a cost of about 50 nsec additional access time. The relaxation of rise time requirements permits the use of a simple transistor switch to perform the input function.

Incomplete signal integration confers other benefits of importance, such as improved immunity to high frequency

Figure 7 Matrix signal routes. Dotted intersections represent normal coupling at unpunched bit positions, and undotted intersections represent residual coupling at punched-hole bit positions.

ROUTE 1   ROUTE 2   ROUTE 3   ROUTE 4   ROUTE 5

Figure 8 Worst-case patterns of information storage. (a) Maximum ONE, (b) Minimum ONE, (c) Maximum ZERO.

MAXIMUM ONE OUTPUT
(a)

MINIMUM ONE OUTPUT
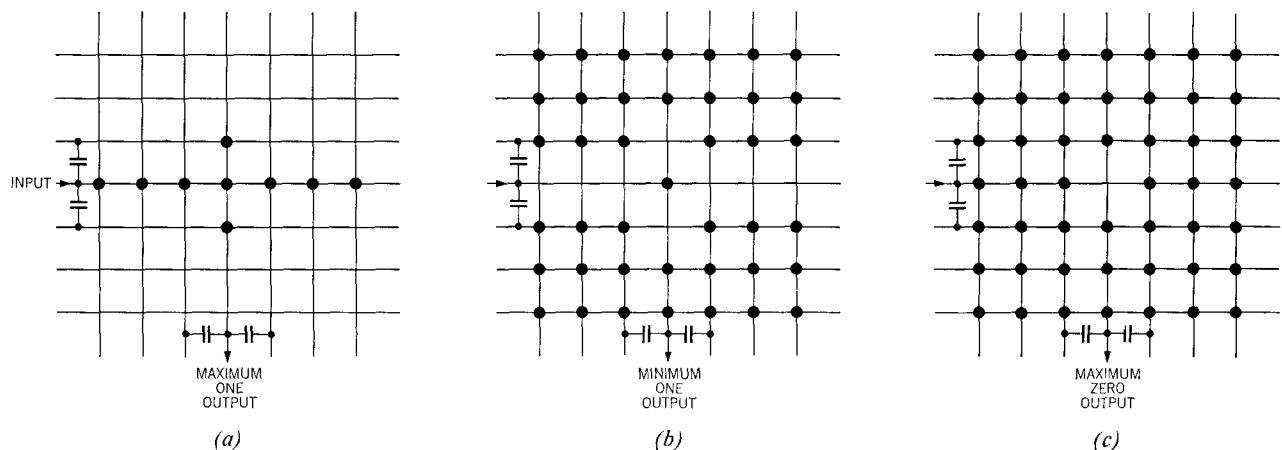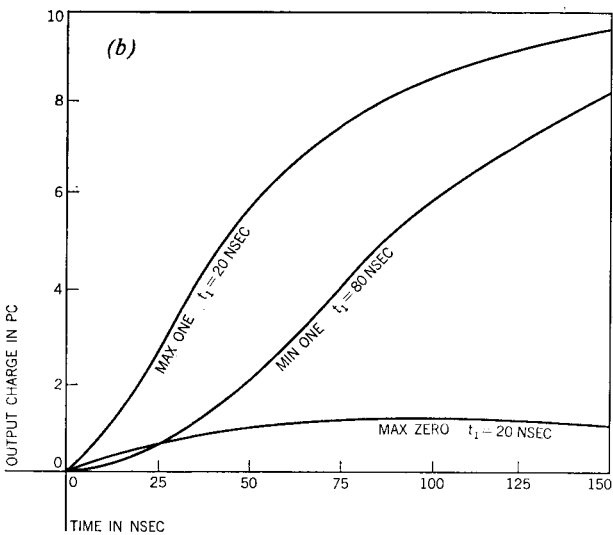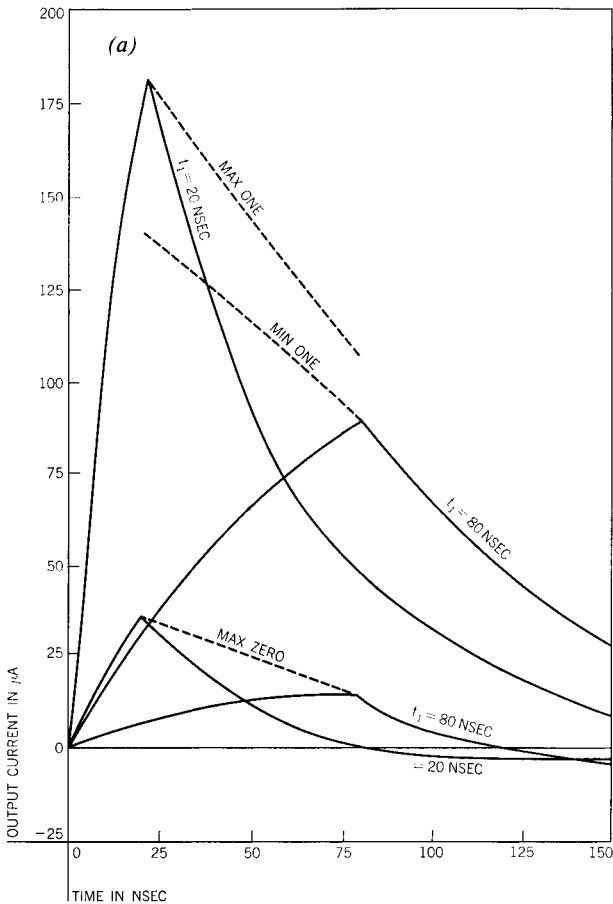(b)

MAXIMUM ZERO OUTPUT
(c)

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Figure 9 Computed matrix outputs for worst-case patterns with 0 to —10V ramp input signal. (a) direct output, (b) integrated output, (c) incompletely integrated output. Dotted lines represent envelopes of peaks for various rise times, t_1.

disturbances, relaxed tolerances on the matrix shunt loading, and absorption of distributed parameter effects due to the ROS structure.

Distributed parameter effects

The short ROS input lines contribute only minor transmission line effects. Time delay from driver to information document is computed to vary from 0.5 to 2.0 nsec. Somewhat longer delays occur in the line conductor on the information document. The transmission line equivalent of this conductor is considered in Appendix B, from which the maximum delays are estimated for the etched line card and the printed line card as 1.4 nsec and 5 nsec, respectively.

Each sense line on the storage board is also considered in Appendix B as a 48-section LC transmission line with an estimated maximum delay of 2.5 nsec. Compared to the total matrix response these delays are negligible.

On the other hand, appreciable time delay and distortion of the matrix signal is induced by the sense bus connecting the sense lines of the individual storage boards. This etched line bus (Fig. 5) is loaded at 0.25-in. intervals by the shunt capacity of the storage board sense lines. Each 0.25-in. line segment has a series inductance of 3 nH, which combines with a nominal 100-pF shunt load per board to form a 43 section LC transmission line with a transit time of 24 nsec and a characteristic impedance of 5.5 Ω. Since the structure is nondissipative it has resonance properties (Fig. 10) and is capable of supporting multiple reflections of the matrix signal or of any signal originating from localized ground shifts in the individual storage boards.

The effect of the sense bus transmission line characteristics is minimized by connecting the sense system to

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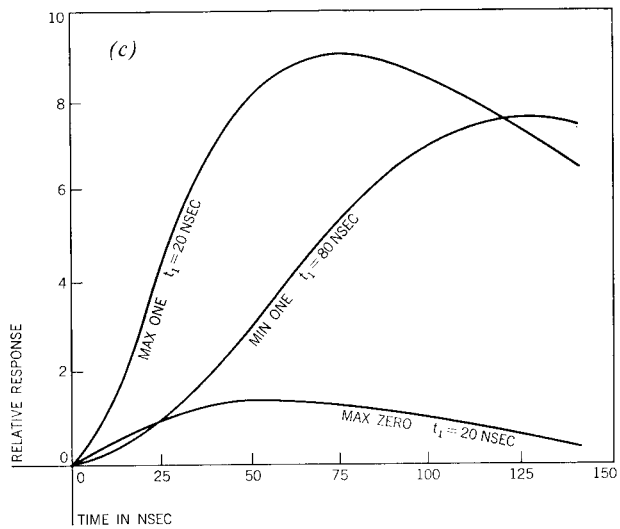
the midpoint of the sense bus where a voltage minima or null exists for the fundamental reflection mode. Voltage maxima exist at the midpoint for higher, even-order modes, but these frequencies are strongly attenuated by the integrating sense amplifier.

The resultant signal to the sense amplifier is essentially equivalent to a lumped-parameter response with a superimposed oscillation and a time delay of half the sense-bus transit time. The approximate waveform can be determined by considering the charge transferred to the sense bus by the line intersection capacity to be split into two equal components which are gradually absorbed by the load in the course of multiple reflections on the sense bus. Computations and expressions defining this action are developed in Appendix C.

The computed 4000-word matrix response is compared to the computed lumped-parameter response in Fig. 11 for both nominal values and extremes of the ROS drive. The 40-Mc/sec frequency of the superimposed oscillation is equal to the second harmonic of the sense bus reflection frequency, and its amplitude is seen to be proportional to the speed of transition of the input drive. Despite the distortion, delay, and dispersion introduced by the sense bus, the signal energy is unchanged so that, after undergoing incomplete integration in the sense system, the final result becomes almost identical to the lumped-parameter response.

Additional factors determining ROS performance

Various effects, most of which are external to the capacitor matrix, tend to degrade the basic ONE/ZERO signal ratio. Some of these (such as variation in the input drive amplitude, output signal amplification, and magnitude of the line intersection coupling) are susceptible to control by the establishment of suitable design and manufacturing tolerances. Two other factors, not as easily controlled are the effects of a noisy drive system and ground shifts between the matrix and the sense system.

An ideal drive system will maintain all unselected input lines absolutely quiet during the application of drive to the selected input line. In practice this ideal is difficult, if not impossible, to attain. The simple drive system used with this ROS permits some driver power bus noise and half-select decode noise to reach unselected input lines. The driver power bus noise is attenuated to a suitably low level by dividing the 2016 drivers into many small groups with individual power bus filters. Half-select noise is a more serious problem. Experimentally, the disturbance is observed to be typically a 22-mV peak-to-peak bipolar signal (Fig. 12).

The simple capacitor matrix is a three-terminal device, asymmetrical about ground. As such it is inherently susceptible to the effects of ground shift between matrix and sense system. Two techniques are used to minimize
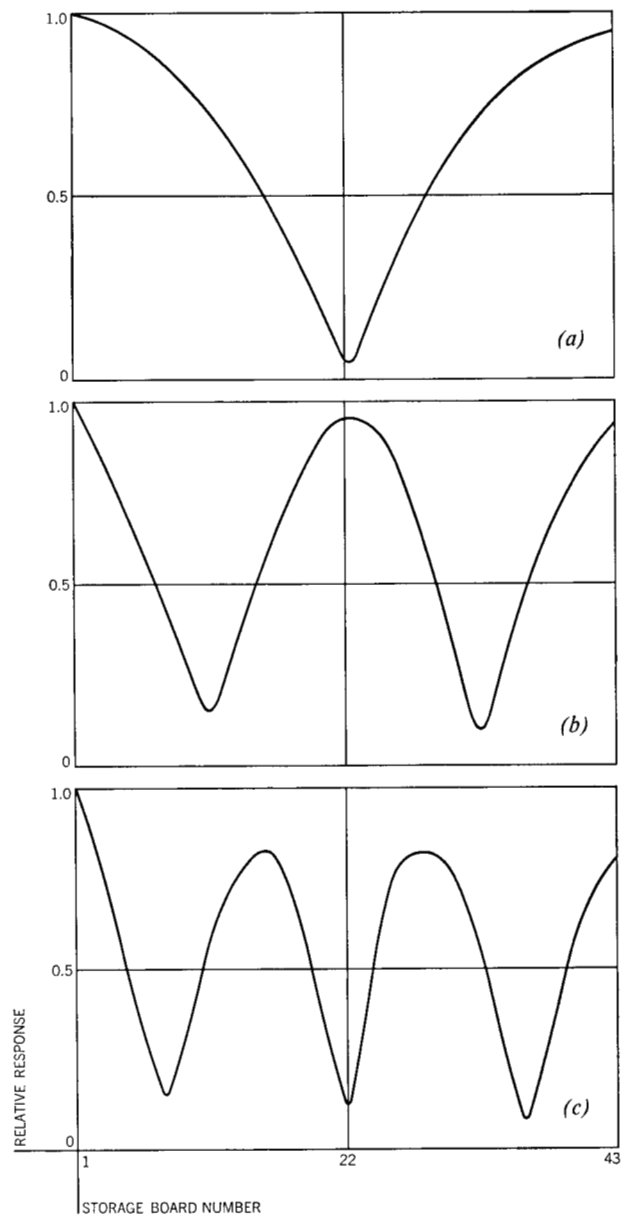

Figure 10 Sense bus resonance characteristics showing response to input sine wave at bus positions corresponding to storage board numbers. (a) fundamental mode at 20 Mc/sec, (b) second harmonic at 40 Mc/sec, (c) third harmonic at 60 Mc/sec.

this problem: (1) a differential sense system and (2) an equivalent RC network in the reference lead.

Figure 13a shows the elementary ground system for the capacitor matrix with the access circuitry utilizing a common power source. Ideally, all driver current, i_1, returns to the driver via the return lead l_1. In an actual situation, however, appreciable driver leakage current, i_3, returns via the sense and common power source ground systems. The potential developed across the matrix-to-

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(a)

Figure 12 Half-select drive noise.

Figure 13 ROS ground system used to minimize matrix-to-sense system ground shifts. (a) elementary system (b) differential sense system, (c) improved differential sense system.
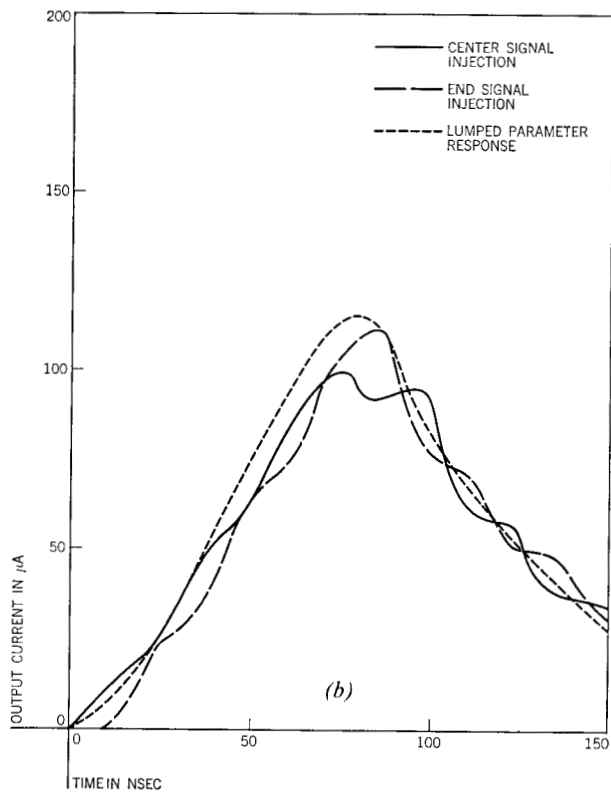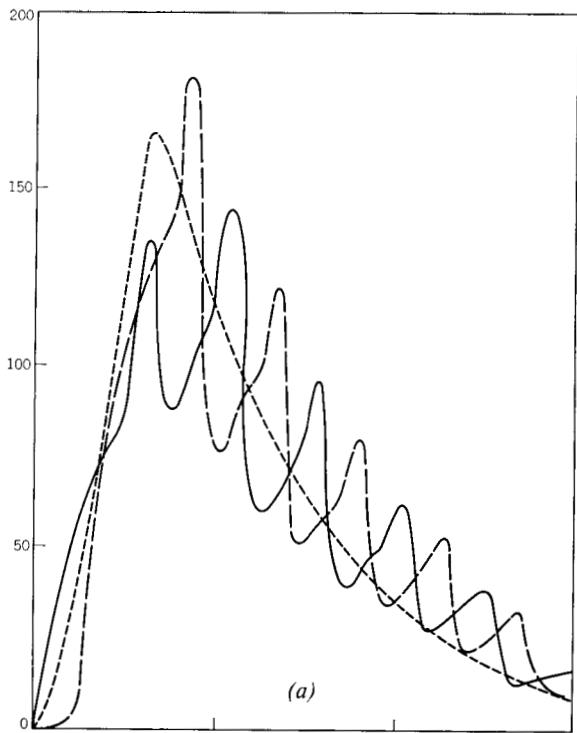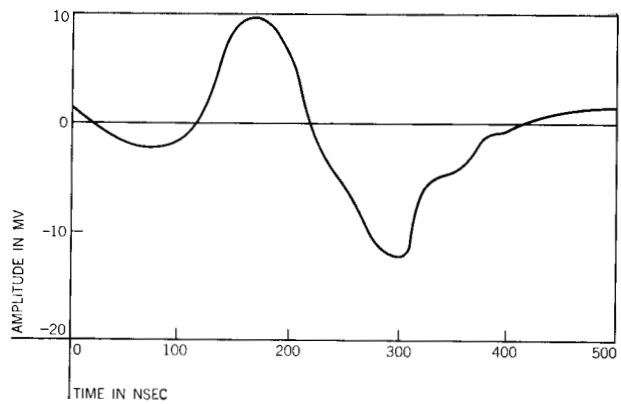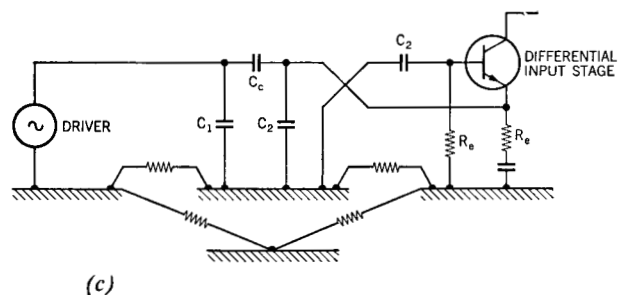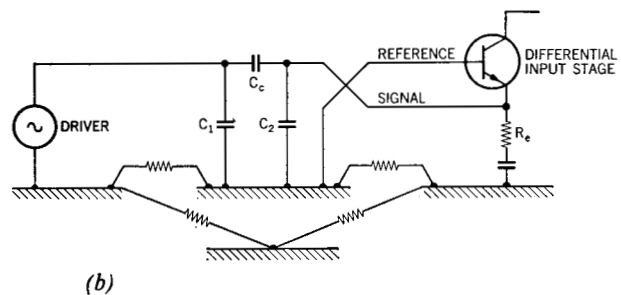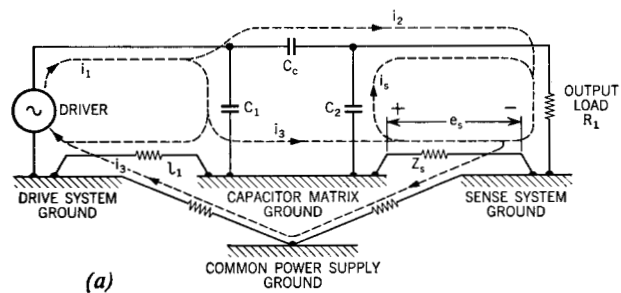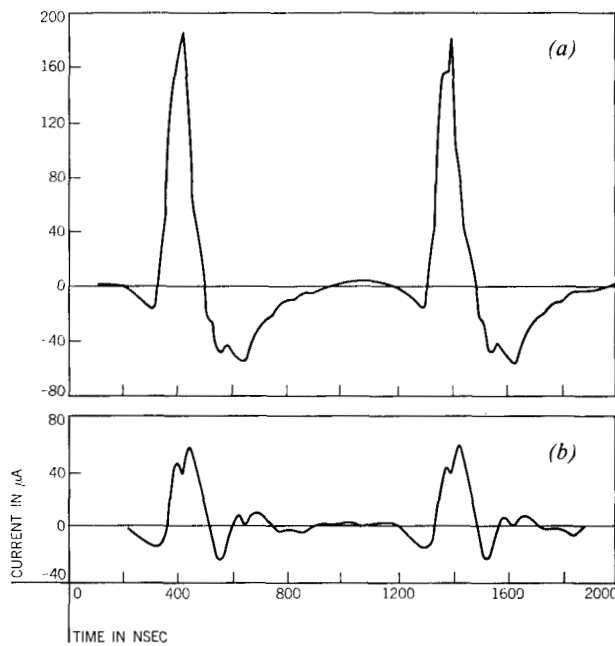

(a)

(b)

(c)

Figure 11 Computed matrix response to ramp input signal for lumped-parameter and distributed-parameter circuits. (a) rise time, 25 nsec, (b) rise time, 60 nsec.

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Figure 14 Typical observed matrix response of ROS. (a) ONE signal, (b) ZERO signal.

sense ground impedance, Z_s by this current can be large enough to overwhelm the legitimate signal current i_2.

To avoid this condition a pseudo four-terminal system is formed by using a differential input sense system connected as shown in Fig. 13b. Ground shifts between matrix and sense system now appear as common mode noise applied to the differential input.

A slight unbalance exists in the application of the common mode noise to the differential input. This occurs because the reference lead receives the ground shift directly while the signal lead receives the ground shift via the series capacitance C_2 and shunt resistance R_s. This unbalance is minimized by inserting an equivalent RC network in the reference lead, Fig. 13c.

Comparsion of computed and observed results

Figure 14 shows typical ONE and ZERO matrix outputs for a 4032-word ROS. Graphical analysis of the signals shows a charge content of about 14 and 5 pC for the ONE and ZERO, respectively. This is about 4 pC more than that contributed by the basic matrix action. The excess is attributed to the system background noise (half-select noise, ground shifts, etc.). Subtraction of 4 pC from both signals would result in a 10 to 1 charge ratio, agreeable with the theoretical value.

Three ONE signals (center input, end input, and an input point half-way between the center and end of the
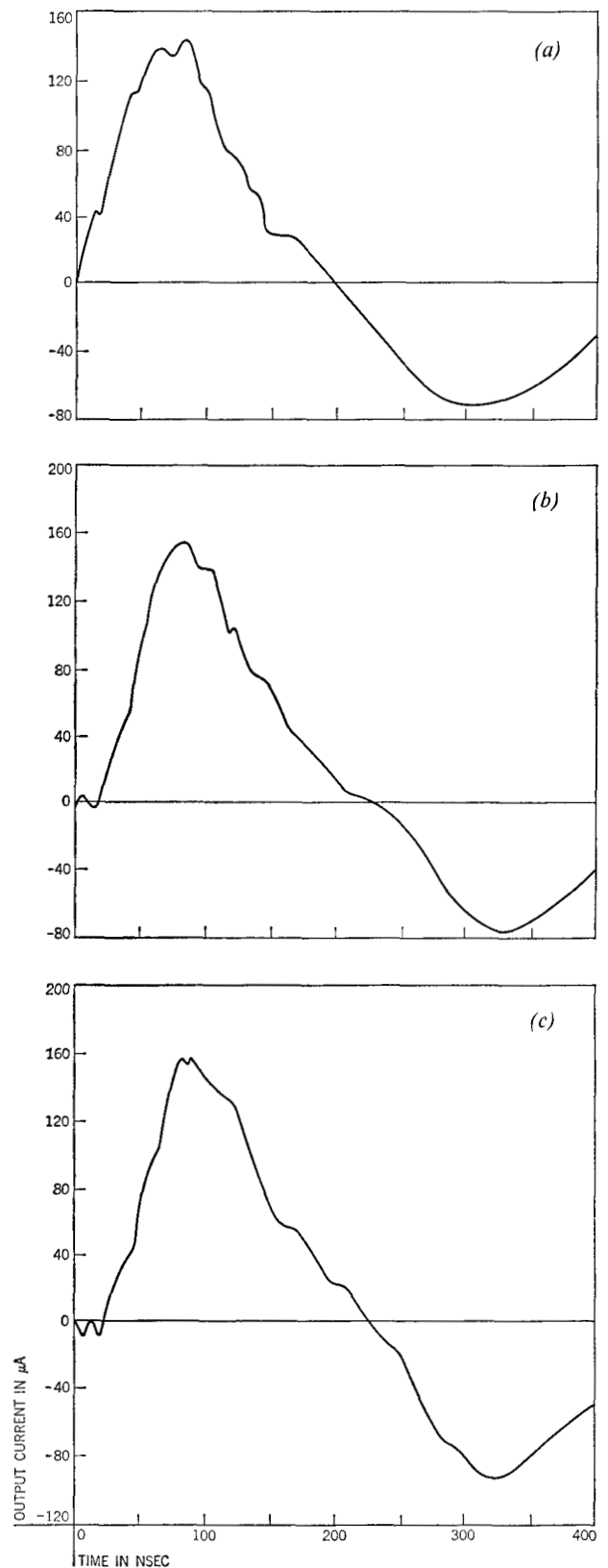

Figure 15 Observed matrix response for different locations of signal origin on sense bus. (a) center signal origin, (b) three-quarter signal origin, (c) end signal origin.
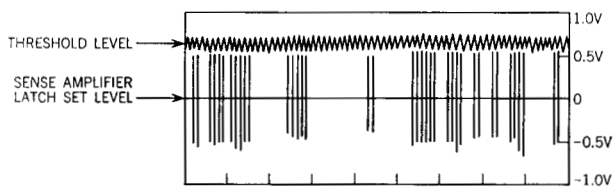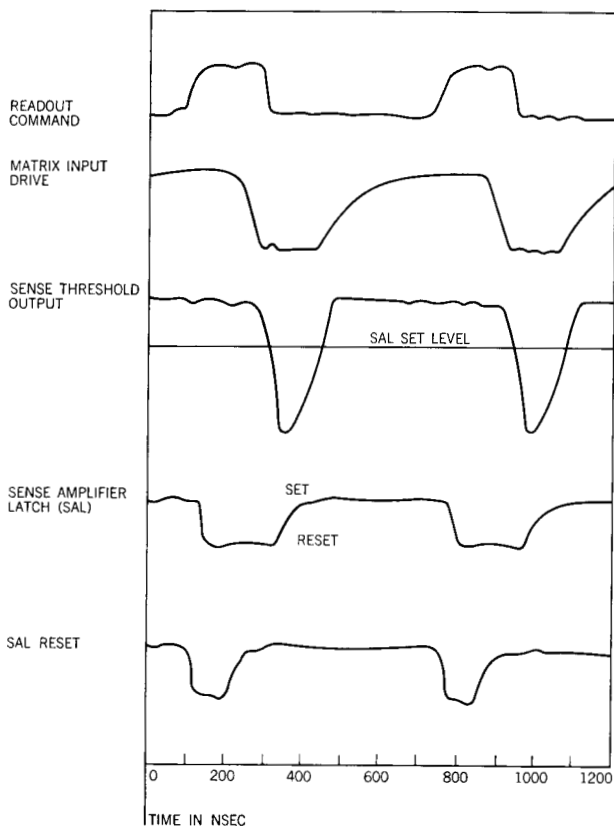
Figure 16 Sample of bit line response.

Figure 17 Time relations between ROS waveforms.

sense bus) are shown on an expanded time scale in Fig. 15. The drive inputs for the three word addresses involved are similar but not identical. The 40-Mc/sec superimposed oscillation is barely discernible because of the nominal drive rise times and frequency limitations in the measuring equipment. The outputs, however, are characteristically single-peaked for end input and double-peaked for center input.

A sampling of a typical bit line during normal ROS

operation is shown in Fig. 16. The pattern of randomly occurring ONE's and ZERO's is shown after amplification, partial integration, and thresholding to suppress the first 30% of the ONE signal. The threshold output is relatively clean with no disturbances of comparable amplitude to the ONE signals.

Because of varying definitions of access time none is given here; however, Fig. 17 shows the significant time relationships of a 4032-word ROS in a 0.65 μsec test cycle.

Acknowledgments

Appendix A—Matrix signal route equivalent circuits and transfer functions

The equivalent circuits and transfer functions for the different signal routes shown in Fig. 7 are given in Fig. A1. Simplifications of circuits and transfer functions were made wherever negligible error results.
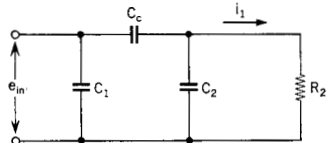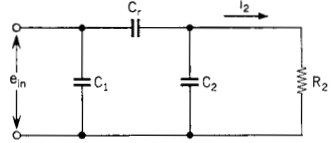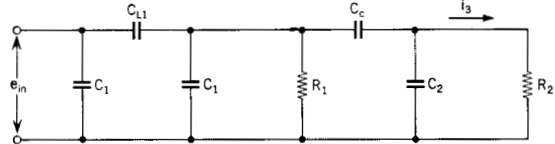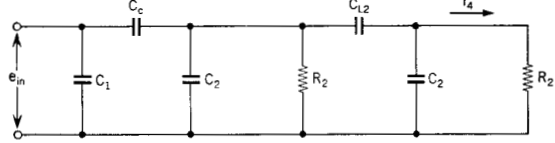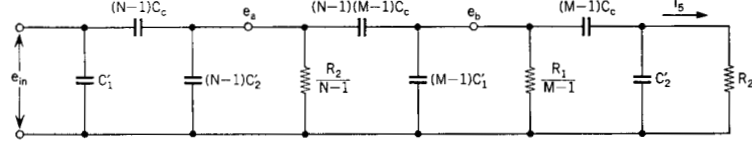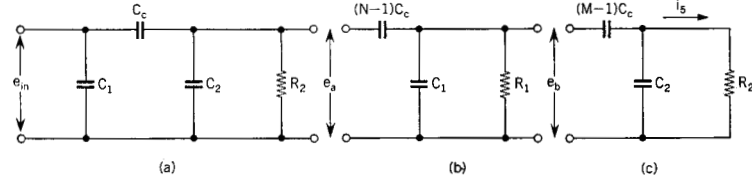
Note that in the circuit for Route 3 the input line-to-line capacitance, C_{L1} is the sum of coupling capacities between the energized input line and all neighboring unselected input lines referred to a single input line. Similarly, the output line-to-line capacitance, C_{L2}, is the sum of coupling capacities between the observed output line and all neighboring lines carrying ONE signals referred to a single output line.

The parameters of Circuit 1 for Route 5 (Fig. A1) refer to the worst-case pattern (Fig. 8c) where all normal line intersection couplings exist except at the intersection of the energized input line and the observed output line. The rationale for the circuit derivation is as follows:

1. The energized input line develops ONE signals, e_a, on (N — 1) output lines; that is, all output lines except the observed line.
2. With e_a as a signal source on (N — 1) output lines, a disturb signal, e_b is induced on all unselected, (M — 1) input lines.
3. With e_b as a signal source on (M — 1) input lines the sneak path signal, i_s, is induced into the observed output line.

While this equivalent circuit is solvable by standard methods, its solution leads to a complex expression that

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Figure A1 Signal route equivalent circuits and transfer functions.

SIGNAL ROUTE	EQUIVALENT CIRCUIT	TRANSFER FUNCTION
ROUTE 1 NORMAL LINE INTERSECTION COUPLING	C_c = LINE INTERSECTION CAPACITANCE C_1 = INPUT-LINE SHUNT LOAD CAPACITANCE R_2 = EXTERNAL OUTPUT LOAD RESISTANCE C_2 = OUTPUT LINE SHUNT LOAD CAPACITANCE	$\dfrac{I_1}{E_{in}}(S) \cong \beta C_c \left[\dfrac{S}{S+\beta}\right]$ WHERE $1/\beta = R_2 C_2, \quad C_2 \gg C_c$
ROUTE 2 RESIDUAL LINE INTERSECTION COUPLING	C_r = RESIDUAL LINE INTERSECTION CAPACITANCE	$\dfrac{I_2}{E_{in}}(S) \cong \beta C_r \left[\dfrac{S}{S+\beta}\right]$ WHERE $1/\beta = R_2 C_2, \quad C_2 \gg C_r$
ROUTE 3 INPUT LINE-TO-LINE COUPLING	C_{L1} = INPUT LINE-TO-LINE CAPACITANCE R_1 = EXTERNAL INPUT LOAD RESISTANCE	$\dfrac{I_3}{E_{in}}(S) \cong \beta \dfrac{C_{L1}C_c}{C_1}\left[\dfrac{S^2}{(S+\alpha)(S+\beta)}\right]$ WHERE $1/\alpha = R_1 C_1,\ 1/\beta = R_2 C_2$ $C_1 \gg C_{L1}$ and C_c
ROUTE 4 OUTPUT LINE-TO-LINE COUPLING	C_{L2} = OUTPUT LINE-TO-LINE CAPACITANCE.	$\dfrac{I_4}{E_{in}}(S) \cong \beta \dfrac{C_{L2}C_c}{C_2}\left[\dfrac{S^2}{(S+\beta)^2}\right]$ WHERE $1/\beta = R_2 C_2,$ $C_2 \gg C_{L2}$ and C_c
ROUTE 5 MATRIX OR SNEAK-PATH COUPLING	CIRCUIT 1 C_1' = INPUT LINE-TO-GROUND CAPACITANCE (EXCLUDING LINE INTERSECTION LOAD) C_2' = OUTPUT LINE-TO-GROUND CAPACITANCE (EXCLUDING LINE INTERSECTION LOAD) M = NUMBER OF INPUT LINES N = NUMBER OF OUTPUT LINES CIRCUIT 2 (a) (b) (c)	$\dfrac{E_a}{E_{in}}(S) \cong \dfrac{C_c}{C_2}\left[\dfrac{S}{S+\beta}\right]$ $\dfrac{E_b}{E_a}(S) \cong \dfrac{(N-1)C_c}{C_1}\left[\dfrac{S}{S+\alpha}\right]$ $\dfrac{I_5}{E_b}(S) \cong \beta(M-1)C_c\left[\dfrac{S}{S+\beta}\right]$ $\dfrac{I_5}{E_{in}}(S) \cong \beta\dfrac{(M-1)(N-1)C_c^3}{C_1 C_2}\left[\dfrac{S^3}{(S+\alpha)(S+\beta)^2}\right]$

is tedious to evaluate. For the range of parameters in the ROS, an alternate form can be substituted with negligible error and will lead to a more easily evaluated expression. This alternate form is given as Circuit 2 for Route 5 (Fig. A1).

The alternate form is based on the following reasoning:

1. The ONE signal, e_a, developed on a single output line is the output of Subcircuit a of the Figure.
2. The disturb signal, e_b, developed on a single input line due to the ONE signals on $(N - 1)$ output lines is the output of Subcircuit b.
3. The resultant sneak-path signal, i_s, developed on the observed output line due to the disturb signals on $(M - 1)$ input lines is the output of Subcircuit c.

Since the loading of each circuit is self-contained, the three subcircuits can be cascaded without interaction, leading to the overall transfer function given in the Figure.

Appendix B—Transmission line characteristics of the ROS Structure

❧ *Input lines*

Each input line consists of two parts:

1. an etched line over a ground plate connecting the driver to the information document and
2. the information document row line.

The etched line, which varies from 3 to 12 in. in length, is a strip transmission line with a characteristic impedance of 73 Ω and a time delay of 0.17 nsec/in. Total delay through the etched line varies from 0.5 to 2.0 nsec.

The information document row line, containing 60 enlargements spaced at 0.087-in. intervals, may be considered as either a lumped-parameter or a uniformly distributed-parameter transmission line. The configuration of the line sections has been shown in Fig. 2b, and the equivalent circuits corresponding to etched copper lines and printed silver ink lines are given in Figs. B1a and B1b, respectively.

In an etched copper line document the lines are predominantly inductive with a negligible resistive component. A 60-section lumped-parameter model most conveniently represents the row lines. The characteristic impedance, Z_0, is $(L/C)^{1/2} = 11.5$ Ω, and the total delay, T_d, is 60 $(LC)^{1/2} = 1.4$ nsec.

In a printed silver line document the lines are predominantly resistive at all frequencies of interest. These row lines present a more complex problem for analysis since the propagation constant, $\sqrt{ZY}$, is not frequency invariant. By defining the input function, however, a particular solution for time response can be obtained from which the time delay can be determined by the following procedure.

Let the row line be represented as a uniformly distributed unloaded RC line with a transfer function derived from the familiar transmission line equations as:

$$\frac{V_O}{V_I}(s) = \frac{1}{\cosh \sqrt{sRC}} \tag{1}$$

where

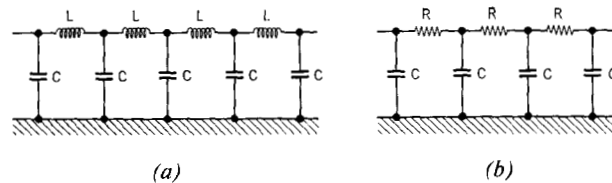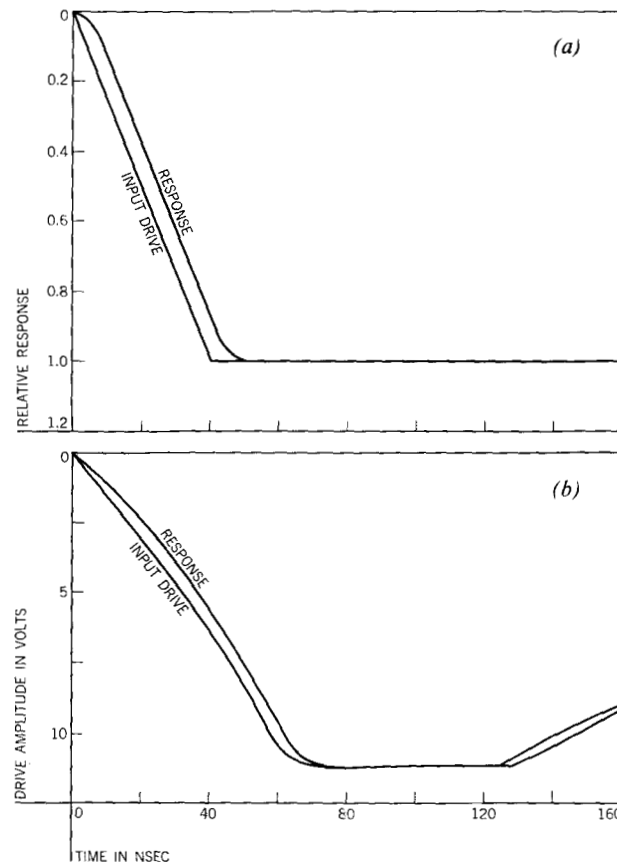$$R = 60\Omega$$

$$C = 130\text{pF}.$$

Figure B1 Equivalent circuits for information document row lines. (a) Etched-copper line document, (b) printed silver line document.

Figure B2 Response of printed silver line. (a) computed response to ideal ramp input, (b) measured response to typical drive input.

This function is adequately represented, for the parameters involved, by the first three terms of the hyperbolic cosine series expansion.

$$\frac{V_O}{V_I}(s) = \frac{1}{1 + \dfrac{sRC}{2!} + \dfrac{(sRC)^2}{4!} + \cdots} \tag{2}$$

$$\frac{V_O}{V_I}(s) = \frac{ab}{(s+a)(s+b)}, \tag{3}$$

where

$$a = \frac{6 + 2\sqrt{3}}{RC}$$

$$b = \frac{6 - 2\sqrt{3}}{RC}.$$

For an ideal ramp input function of rise time t_1 and amplitude V

$$V_O(s) = \frac{V}{t_1}(1 - \epsilon^{-t_1 s}) \frac{ab}{s^2(s+a)(s+b)}, \tag{4}$$

and the time response is

$$V_O(t) = \left[t - \frac{a+b}{ab} + \frac{a\epsilon^{-bt}}{b(a-b)} - \frac{b\epsilon^{-at}}{a(a-b)} \right]$$
$$- [u(t - t_1)]\left[(t - t_1) - \frac{a+b}{ab} \right.$$
$$\left. + \frac{a\epsilon^{-b(t-t_1)}}{b(a-b)} - \frac{b\epsilon^{-a(t-t_1)}}{a(a-b)} \right]. \tag{5}$$

Figure B2 shows the correlation between the computed and observed response. The time delay is taken as 5 nsec.

• Output lines

Each output line consists of two parts:

1. the sense line on the individual storage board and
2. the sense bus parallel-connecting the 43 corresponding sense lines on all storage boards.

The storage board sense line can be considered as a 48-section LC transmission line with per-section parameter values of 1.2 nH series inductance and 2.2 pF shunt capacitance for an unpunched set of information documents. The characteristic impedance and maximum time delay is then 23 Ω and 2.5 nsec, respectively. The time delay will be decreased by the presence of punched line intersections.

The sense bus can be considered as a 43-section LC transmission line where the 0.25 in. bus segment between adjacent boards contributes series inductance, and the individual storage board sense lines contribute a lumped shunt capacitive load. The series inductance is fixed by the geometry of the sense bus strip construction at 3 nH per segment; however, the shunt capacitance can vary
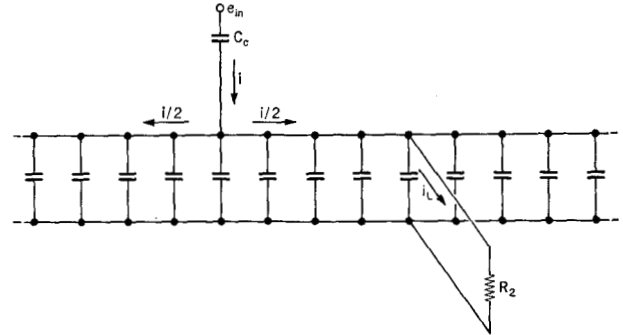

Figure C1 Injection of transferred charge onto the sense bus.

from 86 to 118 pF depending on the information document punched pattern. The line characteristic impedance can then vary from 5 to 6 Ω and the transit time from 22 to 26 nsec.

• Cable connecting sense bus to sense amplifier

The sense bus-to-sense amplifier connection is provided by an 18-in. shielded, twisted-pair cable. The cable load is nominally 7 Ω, the input impedance of a common-base transistor stage. Due to the dissimilarity of the cable characteristic impedance and the load, some impedance transformation occurs, which increases the impedance presented to the sense bus. The effective sense-bus load for nominal conditions is experimentally determined (by measurement of the decay characteristics of the matrix signal) to be approximately 12 Ω.

Appendix C—Matrix signal waveform

Consider the charge or current pulse transferred by the line intersection coupling capacity to be injected on the sense bus at some arbitrarily chosen point as in Fig. C1. For a uniform line, the charge will divide into two equal components (except for two special cases treated later) which travel in opposite directions on the bus, undergoing reflection at the open ends. As each component passes the center load point, part of it is absorbed by the load, and the remainder undergoes another reflection. If line losses and secondary reflection effects at the load point are ignored, the approximate waveform of the load current can be determined by a summation of the current diverted from each component in the course of these sense bus transits.

Injection of the transferred charge at the end or center of the bus represents the two extremes of matrix waveform; they are also special cases. For end injection, the transferred charge is not split and travels the sense bus as one double-amplitude component. For center injection

the transferred charge splits into three components; one is immediately absorbed by the load, and the remaining two equal components undergo reflection. The load current waveform for end injection is expressed by the summation

$$I_l = \sum_0^\infty i\left(\frac{Z_0}{Z_0 + R_2}\right)\left(\frac{R_2}{Z_0 + R_2}\right)^x, \qquad (6)$$

at time intervals $t_x = (x - 1/2) T_d$, and for center injection by the summation

$$I_l = i\left(\frac{Z_0}{Z_0 + 2R_2}\right) + \sum_1^\infty 2i\left(\frac{R_2}{Z_0 + 2R_2}\right)\left(\frac{R_2}{Z_0 + R_2}\right)^x \qquad 7)$$

at time intervals $t_x = xT_d$.

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