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Semiconductor Logic Technology in IBM

In the last twenty-five years the performance of integrated circuits has improved by more than three orders of magnitude and the unit cost has been reduced by approximately the same factor. This paper describes the evolution of semiconductor logic technology in IBM from its early replacement of vacuum tubes in the mid-1950s to the beginnings of VLSI. It highlights the major challenges and accomplishments in the development of bipolar and field-effect transistor technologies and their embodiment in components for a wide spectrum of IBM products.

Introduction

Ultimately, the purpose of all the creativity and toil applied to the development and manufacture of the electronics for data processing systems can be reduced to a few key objectives:

- to improve the performance—reduce signal handling and/or propagation time;
- to lower the cost—including packaging, power, and cooling costs;
- to enhance the reliability—decrease the failure rate and increase length of life;
- and to shorten the development/manufacturing cycle—marketing considerations often demand minimum lapse of time between product definition and its availability.

The quest for improved computer performance and reliability led to the replacement of relays by vacuum tubes and solid state germanium diodes in the early 1950s. The purpose of the vacuum tube was to provide signal amplification, to perform the logical INVERT function, and to drive the long cables between computer I/O (input/output) equipment and the main frame. AND or OR logic was performed with point-contact germanium diodes. Transition to all solid state circuits was completed by the mid-1950s, driven by the rapid development of the alloy junction bipolar transistor.

Even though the early transistors were hardly cost-competitive with vacuum tubes, they had several intrinsic advantages over vacuum tubes in digital circuit applications. Solid state devices have a much lower failure rate and a significantly longer life. The operating voltages are lower, and the absence of high-temperature cathodes results in lower power dissipation and in appreciably lower operating temperatures. Denser packaging is hence possible with the same or even reduced cooling requirements. Denser packaging permits shorter interconnections which reduce capacitive loading and/or signal propagation delays, thus contributing to improved performance.

Since the first use of transistors in the mid-1950s, IBM scientists and engineers have originated many revolutionary changes in structure, design techniques, packaging, manufacturing, and testing of solid state devices and integrated circuits; and they have invented several important device and circuit configurations. The performance (delay) has been improved by more than a thousand times, and the unit cost has been reduced by about the same factor.

During the late 1950s and early 1960s, when the performance limits of transistor logic circuits were still being explored, two other competing approaches were studied: tunnel (Esaki) diodes and parametric amplifiers. For amplification, both relied on a negative resistance phenomenon, inherent to the tunnel diode and induced in the parametric amplifier by a "pump" of double frequency.

Both suffered from the fundamental drawback of two-terminal devices of possessing no inherent isolation between their input and output terminals, and both were eventually abandoned for logic applications.

In this paper we describe the evolution in IBM of binary logic solid state circuit technology—its major challenges, accomplishments, and future trends—and highlight some of the technical contributions of people in IBM who helped make its rapid progress possible.

Overview

There are two periods in the evolution of solid state electronics: the period of discrete components and the period of integrated circuits. The discrete component period began in the early 1950s with the use of germanium transistors in adaptations of vacuum tube circuits, soon followed by growing understanding and utilization of properties peculiar to semiconductors. Silicon diodes and transistors were introduced toward the end of that decade and laid the foundation for monolithic (integrated) circuit technology, which made continued advances through the ensuing years to the present and totally altered the design and manufacture of electronic components. The potential of this technology has not yet been fully realized.

Discrete component technology at IBM progressed rapidly when, in the mid-1950s, project Stretch was initiated with the goal of increasing the operating speed on typical technical applications to at least a hundred times that of the fastest general-purpose computers then in use [1]. The goal of one MIP (million instructions per second) was achieved by advancing all factors that go into the design: the instruction set, the internal system organization, the data and instruction word length, and the supporting technology—the circuits, their components, and their packaging [2].

In 1961, IBM initiated development and manufacture of a broad range of solid state logic and storage products as a technology base for IBM System/360, then under development. Silicon bipolar technology was selected for logic and supporting circuits.

Silicon technology became pervasive (at IBM and throughout the industry) because of the availability of silicon material and because stable SiO_2 film layers could be grown on a silicon surface with ease. In addition, leakage currents in silicon junctions are much lower than in germanium junctions, and the base collector junction of a silicon device can be forward biased much more than a germanium device before saturation becomes significant. This simplifies the circuit design such that compatible input-output signal levels with a sufficient noise margin can be obtained more simply than with germanium devices. The thin layers of silicon oxide or silicon nitride, and also those of several metals and alloys, adhere well to silicon and to each other over a wide range of temperatures. They can be "machined" using photolithographic etching to control diffused regions in silicon in order to form devices, to interconnect devices and complete circuits, and to provide connections to and foundations for the external terminals. Ingenious utilization of these properties was and is the base for progress, as for example is described in more detail by W. E. Harding in a companion paper on manufacturing technology [3].

Silicon technology branched out into two very successful families: the bipolar devices, which were direct extensions of the germanium transistors and diodes, and the field-effect transistors (FETs). Bipolar devices dominate the high-performance applications, while FETs are more suitable for low-cost products. They, in fact, lead in the integration race and are almost exclusively used in computer main memories and microprocessors.

No fundamentally new bipolar switching circuits initially resulted from the change from germanium to silicon. However, in the early 1960s, IBM engineering teams embarked upon a radical departure from the discrete component technology. Small (one-half inch on a side) ceramic "modules" contained all components and interconnections of a circuit, until then assembled on a printed circuit card many times the size of this Solid Logic Technology (SLT) module [4]. SLT was pervasively used in the System/360 processors and stood well the test of time [5]. Packaging components which augmented SLT modules are described in [6]. Design automation systems provided many levels of support [7].

A major change in circuit design occurred with the advent of the monolithic (fully integrated in the body of silicon) logic products which appeared in the early 1960s, the result of developments due to R. N. Noyce [8], then of Fairchild Semiconductor, and J. S. Kilby [9] of Texas Instruments. (The September 1977 issue of *Scientific American*, Vol. 237, No. 3, presents a comprehensive review of the early development of microelectronics.) These products had up to six circuits per silicon chip. The high transistor cost consideration vanished. A new challenge was presented by the bulk manufacturing of all circuit components at once. Some circuit components would have all parameter values well within the desired tolerance limits while others would not.

Fortunately, some relief was provided by the "tracking" between important parameters; *e.g.*, resistor values or junction voltage drops would all shift in the same

direction by approximately the same amount on the same chip. For example, a current switch circuit relies for its operation on the ratio between the emitter and the collector resistors and on the difference between the input voltage and a reference voltage. Therefore, it was a natural choice for the early IBM high-speed integrated circuits [10]. At this modest level of integration most logic functions performed on chip were simple AND, OR, INVERT functions. Most circuits were required to drive off-chip signal networks. Therefore, to achieve a 5–10-ns packaged delay the power dissipation per circuit was quite high, in the 20-mW range.

L. F. Miller's improved solder joining technology [11, 12] became known as C-4, for controlled collapse chip connections. The initial increase in the chip terminals from 3–5 to 12–16 was an important modification of the SLT packaging technology [11, 13], as it laid the foundation for extensions of solderable and reworkable chip-module interfaces to well past one hundred terminals. The increased package density of Monolithic Systems Technology (MST) [14] contributed to the improved cost-performance of the System/370.

The MST packaging hierarchy followed the SLT pattern; namely, approximately 5 to 60 modules were soldered to a printed circuit card. Up to 20 cards were plugged into a board, which thus could offer up to approximately 6000 circuits. Various size (processor) frames contained the required number of boards. Figure 1 depicts the packaging granularity of the System/370 and its successor technologies, and extrapolates the trend.

Toward the end of the 1960s an industry-wide integration race began to offer technology users an ever-increasing function-to-price ratio. The race still continues, following two competing routes: custom design and masterslice (also called logic gate array) design. FETs permit higher levels of integration than their bipolar counterparts because they offer, for the same physical dimensions, lower delay-power products and higher densities while requiring a less complex manufacturing process.

Much of the impact and early acceptance of the FET technology came not so much from its fundamental technological capabilities—measured by cost, density, power, performance, etc.—as from the ease with which it was understood. FET circuit and chip design and fabrication could be quickly grasped as second skills by engineers and managers whose expertise was in design of end products. System designers could design their own handhoned custom designed integrated circuits to provide unique compact functions for their machines. System development laboratories could, because of the simplicity of the FET process, afford to set up their own FET prototype fabricators. IBM, in 1970, set up a semiconductor manufacturing and engineering facility dedicated to small systems and I/O applications which assisted in the release and manufacture of large-scale integrated circuits designed at IBM systems laboratories throughout the world. The era during which small low-budget machine projects had to settle for the technological fallout of large processor-oriented semiconductor developments, which they could not hope to influence, was over. They had an affordable leading-edge technology of their own.

The custom design approach evolved naturally from the initial thrust toward achieving the highest circuit density (actually circuit productivity) of each individual part number. Popular combinations of two or more part number functions were merged into a single chip as soon as advances in photolithography (smaller manufacturable dimensions and/or tolerances of devices and their interconnections) and general process cleanliness (lower defect density resulting in higher yield) would permit. The unique investment in such designs was thus reduced to an affordable level, one which could be economically prorated over the anticipated production volume. Two very important products emerged from this evolution: storage arrays and microprocessors.

Since the discrete component era, logic circuits have been supplemented by latches (flip-flops). Increased integration brought suitable drivers, decoders, and encoders onto the same chip with the storage cells producing random-access storage arrays (RAMs) proceeding from registers to caches. The bipolar RAMs now contain 2–8 kilobits per chip, with the best access times well under 10 ns, while FET RAMs offer ten times the capacity of bipolar RAMs but ten to thirty times longer access time. The evolution of RAMs for main memories is presented in another paper in this issue [15].

Read-only store (ROS) has been popular as an inexpensive medium for storing control instructions. The semiconductor ROS arrays use a single transistor or Schottky barrier diode per bit. Consequently, their densities are four to six times that of a RAM in the same technology and on the same size chip.

Significant enhancement of the logic power of ROS was described by J. C. Logue *et al.* [16] in 1975 as programmable logic arrays (PLAs), in which output of the first AND array drives the input of the second OR array. Addition of latches and signal feedback loops provided capability for a small sequential machine which can be programmed as quickly and easily as personalizing ROS. PLAs became very popular for applications which put a premium on short design time.

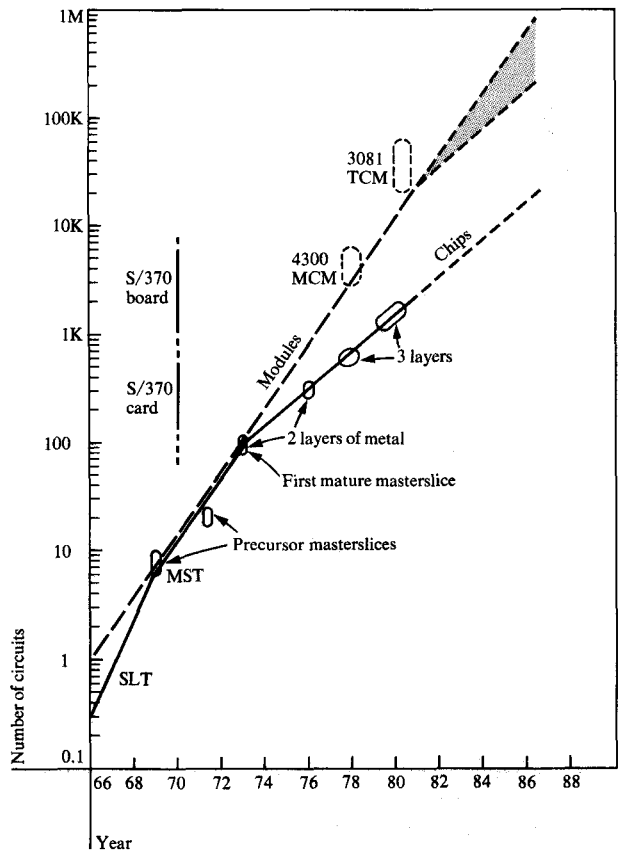

Figure 1 Logic technology evolution.

In a large randomly partitioned system the repeated use of parts (*e.g.*, cards) diminishes with increased circuit count per part [17], and the part number count increases. Therefore, there is a need to reduce time and expense involved in design, qualification, and production testing of each part number. As the level of integration progressed toward 100 circuits per chip, IBM opted for a masterslice (card-like) open part number approach to expedite the design, qualification, and release to manufacturing of bipolar logic chips.

A fixed pattern of circuit components in silicon and optimized provisions for interconnections [18] allowed automatic placement and wiring of many hundreds and even thousands [7, 19] of logic gates per chip for the quick design and release of many part numbers. Further reduction in manufacturing turnaround time resulted from elimination of optical masks by developing electron-beam pesonalization [20-22]. To keep the masterslice chip size comparable to optimized custom designs and yet provide required wiring channels, IBM designers developed two and later three levels of metal interconnections [23] (Fig. 1). The number of circuits on a chip masterslice rose from approximately 10 in 1970 to 1000-2000 by 1980. Thus, a single air-cooled multichip module of the IBM 4300 [24] has the same circuit count as a fully populated board of the early System/370.

Perhaps the most dramatic increase in circuits per module was achieved by the thermal conduction (cooled) module—TCM [25]—of the IBM 3081. It interconnects, powers, and cools about 100 masterslice chips with up to approximately 700 circuits each. Thus, it contains the equivalent of all logic gates of the IBM 370/145 processor. Much shorter interconnections contribute to enhanced performance. Only a few modules contain the entire processor. Its reliability is greatly improved by elimination of many connectors.

With interconnections placed above (instead of between) the circuit cells, their size again became the key factor determining the chip size. The invention of merged transistor logic (MTL), also known as integrated injection logic (I^2L) [26, 27], produced possibly the smallest achievable cell size for logic circuits, which is particularly useful for storage arrays [26(d)-(e)]. The performance of I^2L circuits in logic application falls slightly below that of other bipolar circuits. Schottky diodes were added to enhance their performance [28]. However, the exceedingly small cell sizes cannot always be fully utilized because of wireability considerations. Nevertheless, the chip designers have a wide range of circuits to choose from in this technology to fine-tune a specific design.

Since many signal nets were now contained within a single chip, the circuit cells became specialized for low-power on-chip and high-power off-chip (driver) applications. Yet another challenge arose from the needs to detect (exhaustively) any fault(s) which would impair chip functionality and to diagnose fast and unambiguously the causes of malfunctions.

A successful solution to this problem developed by E. Eichelberger [29] prescribes sequential logic whose correct operation is not dependent on signal transitions nor on circuit and wire delays; it requires transformation of the sequential logic into combinatorial logic by adhering to design ground rules and test generation techniques which call for internal storage elements to be operational as shift registers. This solution became known as level-sensitive scan design (LSSD). At present, further integration on a chip, especially merging of arrays with logic, or packaging of multiple logic and array chips on a module, still taxes practitioners of test generation to the limit.

Whether custom design, array, or masterslice, each increase in the level of integration provides additional

leverage for reducing the unit cost of packaged circuits and for improved reliability; and it may contribute to an improved performance. Each increase in integration is predicated upon further advances in techniques and practices to manufacture, to test, and to package (connect, supply power to, and cool) clusters of hundreds and now thousands and even tens of thousands of circuits and/or storage bits on a 5–15-mm chip. The producers and/or users of these chips have the growing challenge [30, 31] of deciding what to design. And they must design correctly and within affordable schedules and resources. The benefits and the challenges are greatly compounded by the elimination of some of the previously used packaging levels (Fig. 1) which were facilitating the tests, and, if required, such corrective actions as the debug, repair, and design upgrade of computer subassemblies.

Comprehensive studies of limits of integrated circuits [32, 33] and extrapolations of technology and systems evolution [34–36] indicate that by the year 2000 even the largest computers (with circuit count in excess of one million) will be implemented in a very small number of chips. The roles of the semiconductor (and packaging) technologists and the circuit/chip designer will be very tightly coupled with those of the system designer and the architect. This evolution also lays a sound foundation for technological eras to follow, such as that of the Josephson junction [37, 38].

Bipolar logic

The germanium transistor switching circuits of the early 1950s were adaptations of vacuum tube circuits, as exemplified by the diode transistor logic (DTL) circuit of Fig. 2. In it, the AND/OR logic function is performed by diodes and the transistor is used to invert and amplify. This was probably the most commonly used discrete-component transistor logic circuit in the early 1950s, and it is still used today.

During the early 1950s pioneering work led to an understanding of how to use bipolar transistors in switching circuits. Perhaps appreciation of the fact that the bipolar transistor is a current amplifier and such parameters as temperature and ON and OFF base current were important in design came first. However, dc design procedures were soon developed, and major effort was centered on obtaining a thorough understanding of how parameters like minority-carrier storage, base resistance, and junction depletion capacitances affect circuit performance. This work was in turn coupled with efforts to understand the relationship between these parameters and the physical device dimensions.

The growing understanding of device parameters revealed very nonlinear and complex relationships, most

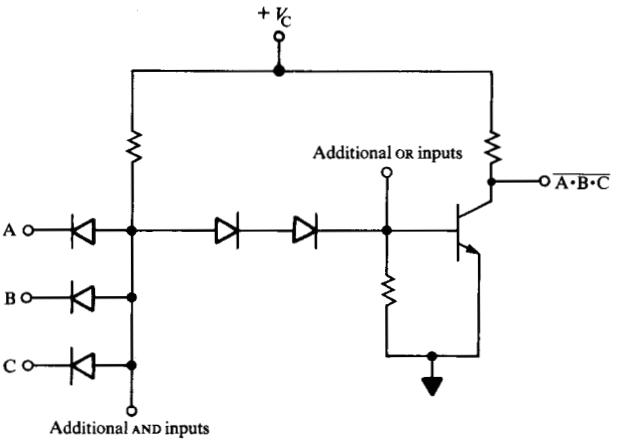

Figure 2 A DTL circuit.

unsuitable for the pencil and paper calculations of the average engineer. Hence, concurrent with the device and circuit development, computer programs attempted to model device parameters from their structures and to predict circuit performance [39–41]. With time, sophisticated computer-aided programs [42–48], culminating in ASTAP [49], have been developed which cope well with these complexities, address statistical parameter distributions, and shorten the product development cycle. A bonus provided by these programs is their ability to calculate signal waveforms which are no longer accessible via an oscilloscope.

The first bipolar switching circuits that were not derived from vacuum tube circuits, but instead utilized the inherent switching properties of the transistor, were the direct-coupled transistor logic circuits [50], DCTL, shown in Fig. 3. In DCTL circuits, current in the resistor load flows into the parallel base loads or into the driver circuit, depending on the state of the driver. Thus, no level-shifting devices were required between driver output and base inputs. Good logic capability was provided by the parallel connection of transistors resulting in a NOR logic function. DCTL circuits were characterized by small signals, good performance, and low power dissipation. However, the device parameter tolerances required to guarantee operation (in particular the emitter-base diode voltage drop at a fixed current) made the devices hard to fabricate. Consequently, DCTL circuits are no longer used.

H. Yourke's current switch [51, 52] was originally developed [53, 54] for the Stretch computer and subsequently used in the IBM 7090 and 7094 computers. It is

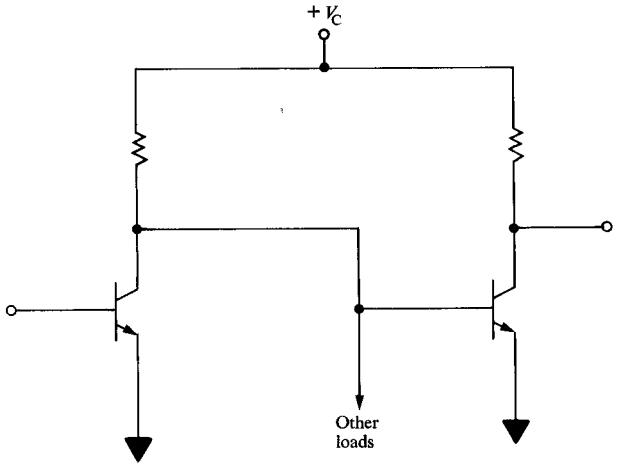

Figure 3 Basic DCTL circuit.

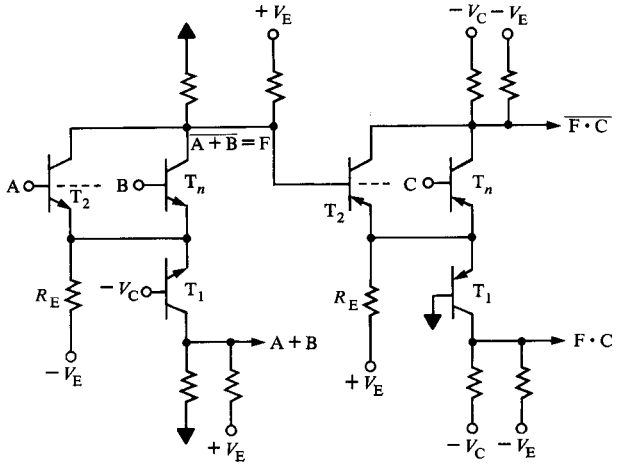

Figure 4 The first ECL circuits.

also known as emitter-coupled logic (ECL) and, adapted to integrated circuits, still dominates high-performance applications.

In this circuit, Fig. 4, current from a current source (R_E, V_E) is switched between a reference transistor T_1 and one or more input transistors $T_2 \cdots T_n$. Outputs are directly coupled to a complementary version of the circuit. This allows all transistors to operate well away from the saturation region—the key to the superior performance. The logic functionality is also enhanced because both a normal function and its complement are always available. The disadvantages are that more different power supply voltages are needed and both pnp and npn transistors are required.

The discrete circuit components, diodes and transistors in their protective hermetic packages, were assembled on planar printed circuit cards [2] forming from two to six circuits, depending on the card width. The cards were plugged into gates, two in a frame. The wire-wrap interconnections were supplemented by ground planes to contain electrical noise; coaxial cables for the long signal lines and power distribution buses were also employed. This particular packaging system was called SMS (Standard Modular System). A successful attempt was made to limit the proliferation of different logic circuit families, while providing means of adjusting the values of circuit elements to the particular application conditions.

Lower-cost diode-transistor circuits were used in other 7000 and 1400 series processors, also employing the SMS package. To further reduce cost, L. Hellerman initiated statistical design to replace worst-case design, thus permitting wider tolerances in the component parameters [55]. Multiple use of the same card reduced demands on the spare stock and also often enabled a problem to be fixed by interchanging two cards of the same part number. The electrical testing took advantage of many circuit nodes being accessible through the pins and more on the back of the card. Changes and/or corrections of the logic were expedited by the wire-wrap connections on the back of the gates, which were also available to the service personnel for scope probing. Newly developed design automation programs provided wiring data (see the companion papers [6, 7]).

Solid Logic Technology (SLT) eliminated the need for protective device encapsulation by covering silicon dual-diode and transistor chips with glass and connecting device terminals to the solder balls at the chip surface. The ceramic module had screened, fired, and tinned lands for direct solder-attachment of the chips and screened-on thick-film resistors which were mechanically trimmed to tight tolerances [4]. The ceramic module, in addition to electrical connections, provided mechanical support and protection, and acted as a heat sink—a role which all modules still play.

The initial single-circuit-module SLT offered four DTL families in the 7–700-ns performance range. Denser extensions, SLD (Solid Logic Dense), for numerous applications were soon added as well as denser and faster ASLT (Advanced Solid Logic Technology) for System/360 Models 91 and 95 in which CSEF (current switch emitter follower) circuits were used to reduce delays to 1.5–3.0 ns.

The established SLT base was combined with advantages of the emerging monolithic (fully integrated in the silicon chips) circuits into MST, which was a significant factor in the improved cost-performance of IBM System/370 [14].

The type of device used in MST circuits is shown in Fig. 5. In this structure an n epitaxial layer of approximately 6 μm was grown on a p^- substrate. The subcollector was arsenic, and isolation and contact to the substrate were provided by a p^+ boron diffusion. Resistors were made with the p base diffusion and all components on the masterslice were connected with a single layer of metal. Two base contacts to the p^- boron base were used to provide a low base resistance. The transient characteristics of such a device were usually determined first by the base-collector capacitance and second by the capacitance between subcollector and p^+ isolation. The base-collector capacitance could be reduced at the expense of increased base resistance by removing one base contact and reducing the base area, but this usually decreased performance speed because of the significant increase in base resistance. In these devices the horizontal dimensions were so large that the diffusion capacitance (minority carrier charge in both the base region and the emitter region) did not play a significant role in the transient response. This is not the case for devices used today.

There were a number of disadvantages with the device structure used in the first monolithic circuits of the type used in the first System/370 computers. To control the isolation-to-subcollector capacitance, a minimum separation had to be guaranteed between the subcollector and the isolation region and, since the subcollector was not self-aligned to the center of the isolation pocket, it was necessary to make the pocket, and therefore the base collector area and capacitance, larger to guarantee this minimum distance. Another degradation was caused by the shallow reach-through collector diffusion. Since the epitaxial layer was quite thick ($\approx$6 μm), the saturation characteristic and the subsequent circuit power dissipation suffered because of the large series resistance created by the epitaxial region between the reach-through and the subcollector. This could be reduced by making the isolation pocket larger to accommodate a deeper collector reach-through, but only at the expense of the increased collector capacitance. Despite their limitations, these devices constituted an improvement over their predecessors.

The first masterslices used in IBM MST technology were simply collections of components capable of providing only a limited part number set. The level of integration was low, approximately four circuits, and the advantage

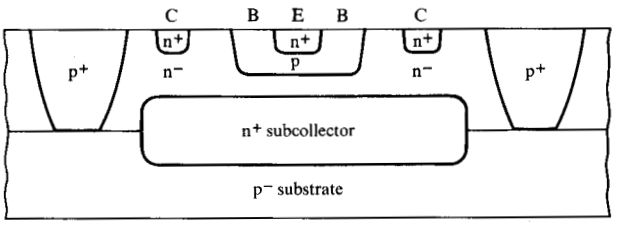

Figure 5 MST transistor cross section.

of the masterslice was quick turnaround time. In time, MST grew in integration level to over one hundred circuits. At this point the masterslice consisted of well-defined circuit cells (gate arrays) which were connected by two levels of metal.

The masterslice provides a base for automatic placement and wiring of many hundreds, and even thousands, of logic gates per chip. The masterslice ground rules permit only a limited number of different circuit configurations to facilitate optimization of design-limited yields, and to make it economically feasible to offer a comprehensive set of ground rules for interconnection networks and associated performance predictors, especially for signal delays. Once qualified for on-chip and off-chip applications, the ground rules are incorporated into automatic design and checking routines to facilitate direct release of newly designed and automatically qualified parts to manufacturing at considerable savings in time and effort.

Whether a custom design chip or a masterslice, the minimum chip size is determined by the total area of circuit cells plus a necessary and sufficient allowance for signal lines and power buses. Dominance of the early chip sizes by the circuit cell dimensions focused attention on circuit configurations which could combine a small cell area with the ability to function within the parameter tolerances of the devices.

The MST technology of the 370 series machines was superseded by a new logic technology which is used in the IBM System/38, 4300 series, and the 3081. The key features of this semiconductor technology are an increased level of integration ranging from 700 to well over 1000 circuits per chip. The devices are smaller and faster than their MST predecessors. A device cross section is shown in Fig. 6. Beyond the dimensional changes, the most significant change is in the use of oxide-filled trenches which reduce the collector perimeter capacitance and significantly reduce the wiring capacitance. The trench between the base and collector separates the

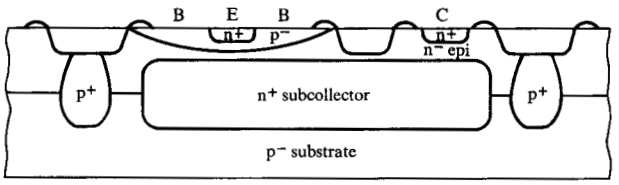

Figure 6 Cross section of transistor technology used in IBM System/38, 4300 series, and 3081.

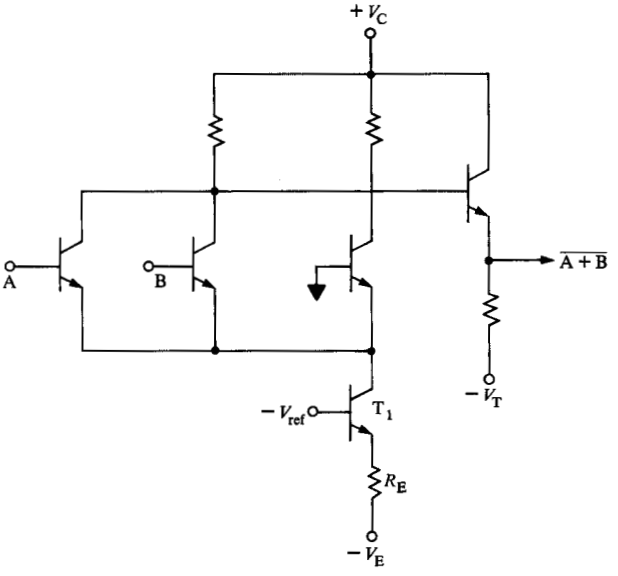

Figure 7 ECL circuit using device of Fig. 6.

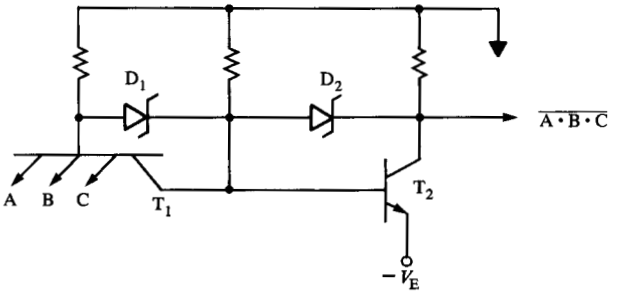

Figure 8 T^2L circuit using device of Fig. 6.

base diffusion from the collector reach-through diffusion, thus reducing the base collector capacitance. Platinum silicide Schottky barrier diodes [56] are used as base collector clamps and in array cells. Significant use is made of 2kΩ/□ ion-implanted resistors, particularly in array cells. However, the most significant improvement is that three levels of metal are used to reduce chip size and improve performance. Solder ball C-4 terminals, arranged in an 11 × 11 matrix, are used for input/output, ground and power.

This technology can be applied to both T^2L and ECL circuits. An ECL circuit is shown in Fig. 7. Transistor T_1 and R_E comprise a constant current source. The reference voltage, $-V_{ref}$, is generated on-chip. The use of the transistor current source makes the circuit current independent of the input level and results in an improved design. A T^2L circuit is shown in Fig. 8. This circuit is well-suited to monolithic technology. Circuit layout area is reduced by putting the emitter base diodes of the input transistor T_1 in a common collector bed. Diodes D_1 and D_2 are platinum silicide and improve performance by holding T_1 and T_2 out of saturation. Output collectors may be wired together to improve the logic capability.

Chips are mounted on multilayer ceramic modules [6, 24, 57]. For high-performance application, liquid cooling enhancement is employed [25]. Because the chip pitch on the ceramic modules is small, signal line length between chips is greatly reduced, thus improving system performance.

There is a bright future for bipolar technology. The use of E-beam lithography and plasma etching promises a further reduction in device size, which implies improved performance at lower power dissipation. These improvements in semiconductor technology will be matched by further improvements in multilayer ceramic packaging technology. But perhaps most significant will be the clever uses made of the base technology advances in terms of new device structures and circuits. One example is the integrated injection logic circuit (I^2L/MTL) proposed by S. K. Weidmann and H. H. Berger. A cross section of the MTL device is shown in Fig. 9(a), while the basic circuit is shown in Fig. 9(b). MTL is significant because of the small silicon area used and this fact has led to much work on the device structure and its use in logic and arrays [26, 27, 58–60].

However, one should recognize that many of the new base technology improvements mentioned above will also be used to significantly improve FET technology, which is discussed in the next section.

FET logic

A dramatic means of overcoming yield and power dissipation limitations was offered by the Field Effect Transistor (FET). The metal-oxide-silicon (MOS) technology requires fewer photolithographic operations than comparable bipolar processes and, therefore, collects fewer de-

fects. In addition, the FETs produced by the MOS processes rely for their operation on only one species of current carrier (holes or electrons) and are relatively immune to the recombination phenomena that occur at silicon faults and destroy the gain of bipolar transistors. Operation of FET circuits at substantially higher voltages and lower currents than bipolar circuits makes them less sensitive to the growing problem of resistive voltage drops that occur on long narrow metal or semiconductor interconnections within a monolithic chip. The FET's relatively simpler structure is contrasted with that of a bipolar device in Fig. 10.

The phenomenon of the insulated gate field effect transistor had actually been postulated [61] prior to Shockley's announcement of the bipolar transistor. The device was conceptually simple—a potential placed on an electrode (gate) separated from the semiconductor surface by a thin dielectric attracts carriers to the surface, creating a conductive channel between diffused electrodes in the semiconductor. Reducing the potential repels the carriers and switches off the conduction. Unfortunately, early silicon surfaces exhibited conductive states which obscured this phenomenon, and early dielectrics contained impurity ions which modulated conduction independently of applied gate voltage.

Since the predominant ionic impurity in the oxide was positively charged sodium, its presence shifted the voltage necessary to cause conduction (the threshold voltage) in the negative direction. This problem was most serious in those devices (n-channel) that conducted by means of electrons attracted to the surface, since the natural threshold of conduction for such devices was near-zero gate potential and the presence of ions in the gate generally made it impossible to turn the device off without applying to the gate a potential more negative than that of the transistor's other electrodes. Efficient logic circuits require that the transistors be switched in and out of conduction at a potential intermediate to those existing at its other electrodes. Because of this, most researchers concentrated on p-channel devices, which conducted via positive charges or holes.

An IBM device technology group recognized, however, that the mobility of electrons was three times that of holes and that the performance of n-channel devices would therefore be much better than that of a p-channel structure [62, 63]. It demonstrated that charge-free insulators could be grown and stabilized by doping them with phosphorus. It pointed out that FET threshold voltages could be varied by modifying substrate doping and/or applying a bias to the body of the semiconductor on which the FETs were fabricated. It also demonstrated

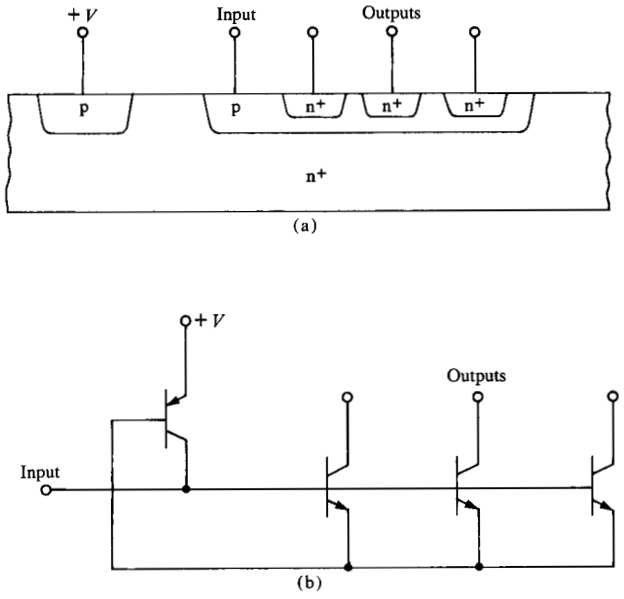

Figure 9 (a) MTL device cross section. (b) MTL circuit.

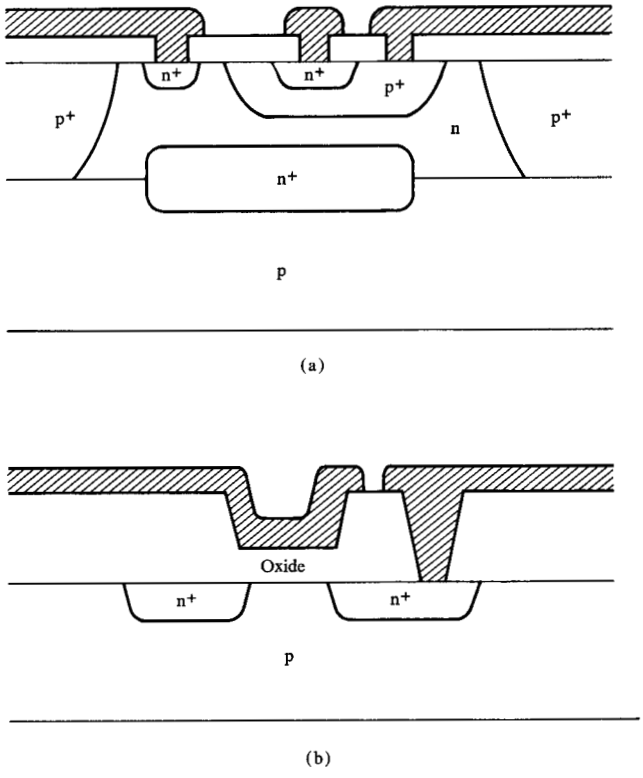

Figure 10 FET structural simplicity: The FET structure (b) requires only four photomask steps compared with the six steps commonly used in bipolar devices (a).

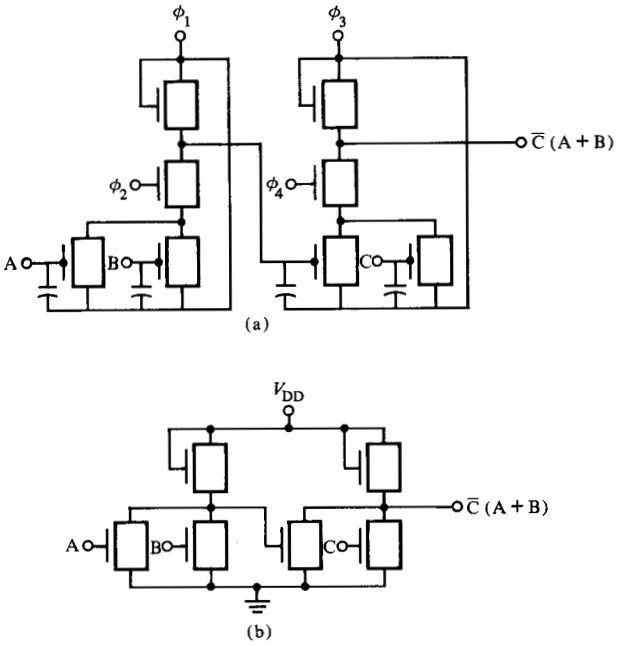

Figure 11 A contrast of the simplicity of the static circuit in (b) with its dynamic equivalent in (a).

that n-channel FETs could be passivated and packaged reliably in nonhermetic modules using IBM's C-4 technology [11].

Preparation of the accurate and detailed fine-line photolithographic masks used to define the shapes of the FET devices and their interconnection soon became a challenge as the number of desirable topological ensembles of devices grew with the achievable complexity of the technology. The traditional method of cutting detailed geometries in rubylith for each semiconductor layer could not meet the demand for numerous accurate complex masks. In 1967, Dr. H. Frietag described [64] a computer-controlled method of artwork generation that reduced the time necessary to generate typical integrated circuit masks from a labor-intensive and error-laden 200 hours to a computer-aided systematic three hours. Later that same year A. Weinberger reported [65] a highly automated procedure for laying out dense integrated circuits that was to allow IBM engineers to design hundreds of highly customized functional chips each year for products starting with the IBM 2740 key entry system [66].

Physical design was only one of the problems encountered by early integrated circuit designers. The complexity of the logical design process and that of the electrical design process were equally significant. The selection of an elementary circuit building block was a subject of controversy among designers. Most designers utilized variations of the "four-phase dynamic" [Fig. 11(a)] circuitry popularized by Dr. F. Wanlass [67] of American Microelectronics, Inc. In the dynamic logic circuit, charge is stored on the insulating gate of a field effect transistor, causing it to conduct. The charge is removed at a subsequent time period if and only if a conductive path to ground has been previously established by charge storage on the gates of other similar transistors attached to the storage node. Dynamic logic has several advantages:

- low power dissipation on the chip itself,
- small device size, and
- the ability to construct complex combinatorial logic functions in a single stage.

It also has several disadvantages:

- Clock signals are required to precharge and discharge the signal nodes. These require relatively complex external circuitry for their generation and consume valuable silicon area for their distribution to all circuits on a chip.
- Since charge leaks off signal nodes with time, the clocks must be operated continuously. Data must be sampled before they are destroyed in a subsequent clock cycle.
- The clock frequency must be slow enough to permit charging and discharging of the most heavily loaded circuit on the chip. Once the clock frequency is set, all circuits propagate signals as slowly as that slowest circuit.
- Dynamic circuits are sensitive to the minute leakage currents found in early n-channel devices. Consequently, early dynamic-circuit developers were reluctant to work in the n-channel process despite its superior performance potential.

IBM designers recognized that success in nondynamic circuit [Fig. 11(b)] designs depends upon the ability to use the larger, more dissipative devices only where they are necessary to improve the delay of a critical circuit path. Larger devices conduct more current and hence switch capacitive loads faster. However, they also present more capacitance to the circuits which drive them and dissipate additional power. IBM engineers developed a computerized chip design system that allowed heavily loaded networks to be driven by higher-powered circuits. This system evolved into an FET automated design system in which the size and placement of devices were algorithmically determined in a manner that minimized the power dissipated for any set of circuit delay requirements submitted by the logic designer. This system was coupled to physical placement and wiring algorithms similar to those described previously such that circuit power could be

varied to compensate for loading changes generated during physical placement and wiring of the circuits on the chip (see also the companion paper [7]).

Circuit designers produced circuit innovations which improved performance of the FET technology. The use of an FET biased in its linear operating region improved the power-performance of the logic technology [68]. Circuits were developed to sense device and application parameters and then to adjust the bias voltages applied to the logic circuits to compensate for variations in process and application parameters which would otherwise increase delay. Through the process of ion implantation [69] it became possible to alter the threshold voltage of those transistors used as current sources. The resulting "depletion load" circuitry was 30% faster than earlier versions.

The most significant gains in performance, density, and productivity came through shrinkage of the basic photolithographic feature size. IBM engineers pioneered the technique of maintaining a planar oxide surface so that the depth of field limitations of exposure equipment would not constrain device geometries. Projection printing techniques made it possible to expose a wafer without contacting it. The consequent reduction in defect density made larger chip sizes economically feasible.

Given the ability to integrate more than one thousand logic circuits in a single chip, designers worked to include complex functions within the boundaries of their chips. Triggers, latches, integraters, registers, and other special functions were soon integrated parts of logic chips. These increases in function, density, and performance put new pressure on the developers of test equipment to produce systems capable of driving and/or measuring precise currents or voltages on each of over 100 terminals located within a 5-6 mm square.

Such systems were required to handle thousands of patterns, to provide diagnostic measurements, and to support logistics for handling and sorting large quantities of chips of any of hundreds of part numbers. The software required to simulate and test increasingly complex integrated circuits presented no less formidable a development task than did the hardware. Many designers sought to simplify these problems by designing additional circuitry and/or test ports into their chips for the sole purpose of facilitating simulation and test. As the complexity of the design process grew with the capability of the technology, the need for simpler, faster design methodologies became more and more apparent.

In the System/360 era, capacitor read-only storage (ROS) devices provided an inexpensive alterable medium for storing instructions to control an electronic processor. The FET technology offered an array of transistors which could be personalized with a single automatically generated photo mask, much the same way control store changes were generated in the System/360 era. Designers were so excited about the ability to quickly integrate large amounts of function that the technology evolved from the 5000-bit ROS developed in the late 1960s through hundreds of part numbers to the 100 000-plus-bit ROS in production a decade later.

ROS devices are limited by the fact that they represent only one level of logic. In a PLA, latches, signal feedback lines, and circuits for creating combinatorial logic functions of inputs and feedback variables form the skeleton of a sequential machine which can be programmed by personalizing the AND and OR arrays [16]. PLAs became popular devices for implementing adaptors and other functions where the design times were more important than optimal silicon utilization [70]. Since ROSs and PLAs proved so effective for the rapid design of individual components, designers soon began to use them to design functional macros which were subsequently assembled to form larger multimacro chips such as those used in the IBM 3270 display system.

Significant derivatives and variations of the FET process have occurred and will continue to emerge. Developers interested in very high performance build FET circuits on insulating substrates such as sapphire to reduce capacitances. Other developers interested in applications requiring ultra-low standby power such as watches or hand-held devices have developed complementary (CMOS) circuits. These circuits replace the n-channel pull-up devices of conventional logic circuits with p-channel devices which can be turned off when not in use, reducing the power dissipated by the circuit.

Advances in FET logic have continued to shrink circuit size and improve performance through new processes such as vapor deposition of polysilicon [71], doped oxides, and dry etching; and through improved tools such as step and repeat and electron-beam lithography. More designers are finding that interconnections rather than active devices are becoming the dominant factor influencing chip size and performance. They are treating the electrical and physical design of interconnections as seriously as the design of the transistors themselves, replicating circuits when that results in more efficient wiring and using transfer devices to isolate portions of nets when they are not in use. They are using multiple layers of metals and/or low-resistance polysilicon to enhance the wireability of complex logic.

Today chips containing over 50 000 transistors are readily available in 2–3-micrometer technologies. FET technologies are theoretically extendible to densities 100 times greater than today's. However, the increased complexity of these technologies and their areas of application may drastically alter both the form and the rate of this progress [72].

Early FET chips consisted of a couple of hundred circuits comprising all or part of a small logic function whose detailed operation was within the logical grasp of one or two individuals. Systems were constructed as ensembles of these functional chips or chip sets. The fabrication process was simple, prototypes could be fabricated, tested, and redesigned in a few weeks' time. A system designer could try out several iterations of hardware in the course of developing his system.

Improvements in density, cost, and performance of FETs have come at the expense of the simplicity which was the technology's original attraction. Pilot facilities must now be ultra-clean and must contain expensive equipment such as ion implanters, CVD systems, and electron-beam exposure systems. The time and resource required to prototype a totally custom part is beyond the horizon and affordability of most system development projects. System designers are making increased use of general-purpose microprocessors and supporting microsystems components. These systems are customized by programming separate electrically alterable read-only memory components [73] or, increasingly, by programming electrically alterable arrays embedded in the microprocessor chips. The true custom system component designer is no longer the driving force behind FET VLSI progress.

Component developers are increasingly concerned about the granularity of their offerings—the need to keep the function on each chip small enough that it can be cost-effective in multiple applications. This trend is counter to the traditional LSI formula for progress, *i.e.*, to put a lot more function on a chip that is only a little more expensive than its predecessor. This is more difficult as chip densities approach the total traditional circuit count of many small systems. Such systems cannot afford the time or money to develop custom parts and are unlikely to find a single part that meets their functional requirements. VLSI will only impact such systems if component designers provide functions not previously performed electronically.

The future belongs to the architect/engineers who can conceive of general applications that are large enough by themselves or are part of a sufficient set of functional macros that can be quickly interconnected into a large enough function to effectively utilize the tens of thousands of circuits available on a VLSI chip of economical size. Component architects are viewing such applications as floating-point arithmetic, memory system management, and data sorting, once considered the province of the systems software specialist, as opportunities for hardware integration. As yet another interdisciplinary barrier falls to the vanguard of silicon integration, we should expect to see silicon subroutines continue the trend of performance and functionality improvement set by predecessor LSI and VLSI technologies. This evolution will fundamentally alter the classical (separate) roles of circuit, chip, and system designers.

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