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Chenming Calvin Hu, Microelectronics Visionary, to Receive 2009 IEEE Jun-Ichi Nishizawa Medal

Achievements Have Been Critical to Producing Smaller Yet More Reliable and Higher-Performance Integrated Circuits

PISCATAWAY, N.J. – 22 June 2009 – Chenming Calvin Hu, a researcher whose seminal work on metal–oxide semiconductor (MOS) reliability and device modeling has had enormous impact on the continued scaling of electronic devices, is being honored by IEEE with the 2009 IEEE Jun-Ichi Nishizawa Medal. IEEE is the world's largest technical professional association.

The medal, sponsored by The Federation of Electric Power Companies, Japan and the Semiconductor Research Foundation, recognizes Hu for technical contributions to MOS device reliability, scaling of CMOS and compact device modeling. The medal will be presented on 25 June 2009 at the IEEE Honors Ceremony in Los Angeles, Calif. For the first time, the IEEE Honors Ceremony will be broadcast live on the Web through IEEE.tv (www.ieee.tv).

Considered a pioneer in MOS reliability efforts, Hu's achievements have also impacted the scaling of MOS devices as well as models for efficient circuit simulation. As the need increases for smaller device sizes, resulting in more transistors being placed in smaller chip areas, difficulties in operation and reliability can arise that slow further scaling progress. Hu's work has addressed reliability and scaling issues with models and simulation tools that are critical to current predictive capabilities in the semiconductor industry.

During the 1980s, Hu developed models capable of predicting circuit failures caused by hot electron effects, oxide breakdown and wearout, metal line failures,; and the effects of external ionizing radiation. This award-winning work has led to the development of highly reliable integrated circuits.

One of Hu's more famous contributions is a promising MOS field-effect transistor (FET) called the "FinFET." As the team leader, and using conventional technology, Hu co-developed a multiple-gate transistor that will allow much smaller transistors to be built. The FinFET has already enabled several corporations and universities to set records for designing the smallest transistor. Hu also contributed to the creation of the "Berkley Short-Channel IGFET Model" (BSIM) series of compact models. Chosen by the industry as the first international transistor model standards, these models enable efficient circuit simulation for accurate integrated circuit design, and most major chip manufacturers have made these models their preferred choice for circuit simulation.

His research in MOS scaling led to innovations such as variable threshold transistors, low-power flash memory cells, ultra-thin-body devices, and multiple-gate structures. These scaling accomplishments are a result of Hu's innovations in new device designs. Hu is currently developing a replacement for MOSFET that would potentially reduce integrated circuit power consumption significantly.

An IEEE Fellow and member of the National Academy of Engineering and Academia Sinica, Hu has received many awards including "R&D" magazine's R&D 100 Award for BSIM3, Sigma Xi Moni Ferst Award for advancement of research, the IEEE Jack Morton Award in 1997 for physics and modeling of MOS device reliability, the IEEE Solid State Circuits Award in 2002 for MOSFET modeling as well as the Berkeley Distinguished Teaching Award—UC Berkeley's highest honor for teaching. He received his bachelor's degree from National Taiwan University, Taipei, and his master's and doctorate degrees from the University of California, Berkeley. Hu is currently the TSMC Distinguished Professor of Microelectronics at the University of California, Berkeley, where he has taught since 1976.

About IEEE

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