Flash Memory with Nanoparticle Floating Gates

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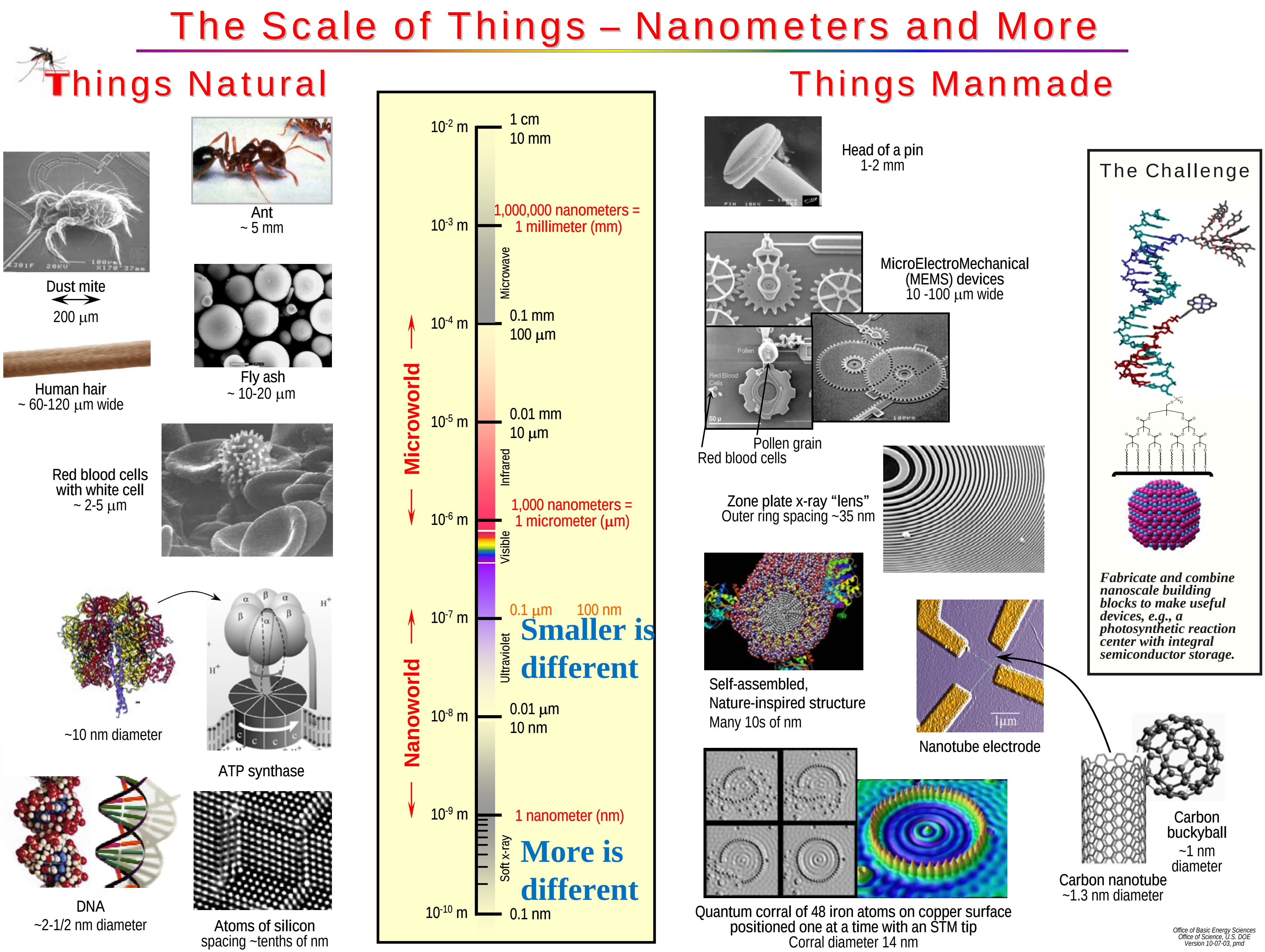
- Why Nanoparticles in Flash Memory
- Self-assembly schemes
- Device Performance

Acknowledgements: DARPA MARCO, NSF NIRT, Micron

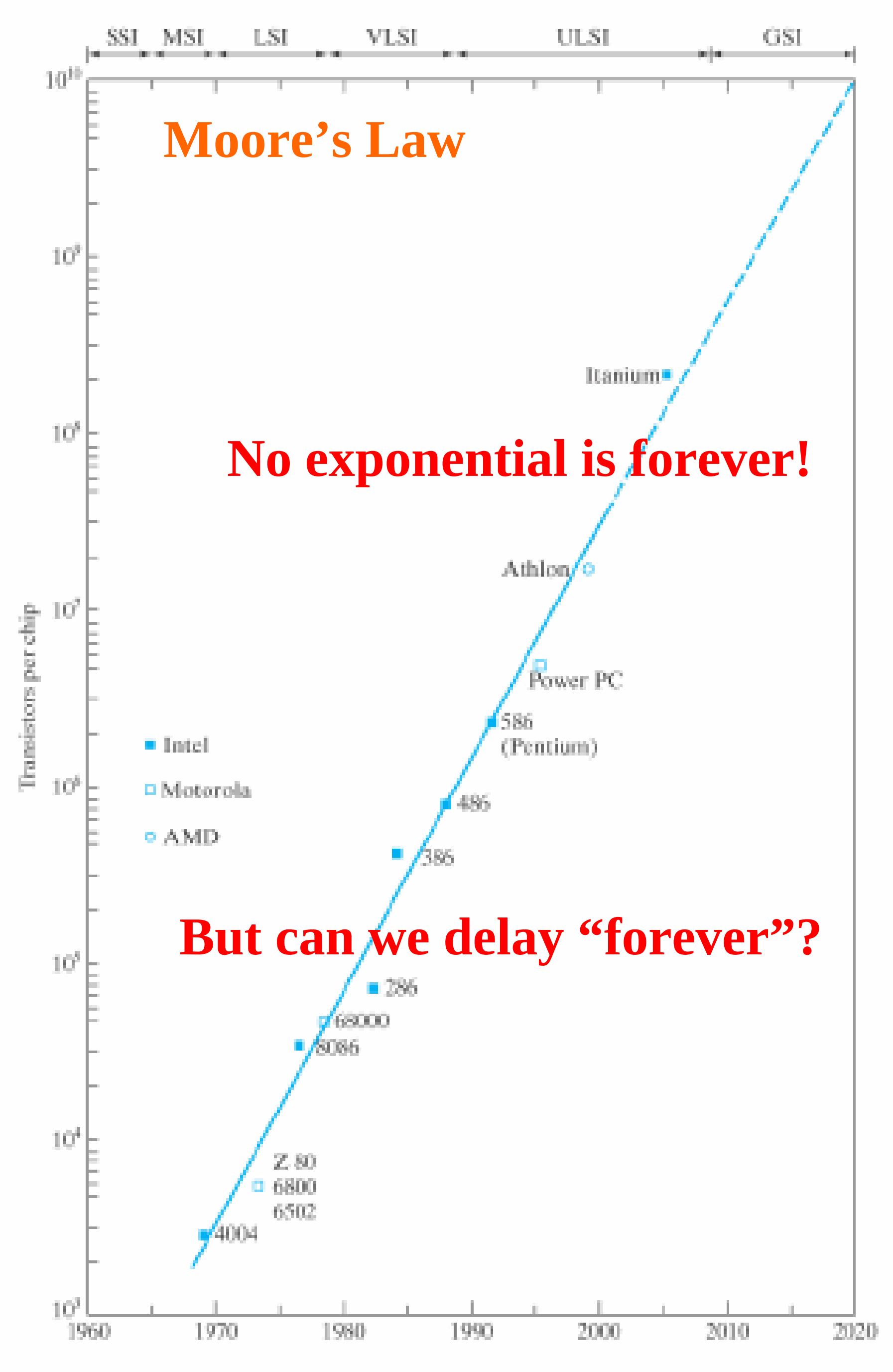


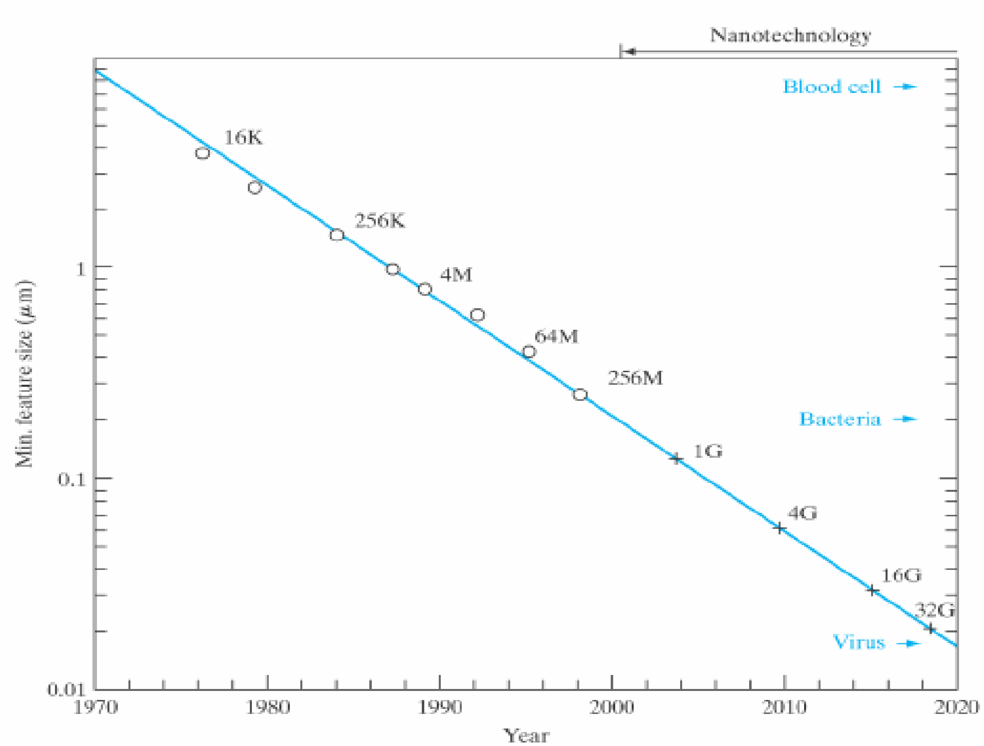
The Scale of Things – Nanometers and More
Things Natural
Dust mite
200 μm
Ant
~ 5 mm
Human hair
~ 60-120 μm wide
Fly ash
~ 10-20 μm
Red blood cells
with white cell
~ 2-5 μm
~10 nm diameter
ATP synthase
DNA
~2-1/2 nm diameter
Atoms of silicon
spacing ~tenths of nm
10^{-2} m
1 cm
10 mm
10^{-3} m
1,000,000 nanometers =
1 millimeter (mm)
Microwave
10^{-4} m
0.1 mm
100 μm
10^{-5} m
0.01 mm
10 μm
Infrared
Microworld
10^{-6} m
1,000 nanometers =
1 micrometer (μm)
Visible
10^{-7} m
0.1 μm
100 nm
Ultraviolet
Smaller is different
10^{-8} m
0.01 μm
10 nm
Nanoworld
10^{-9} m
1 nanometer (nm)
Soft x-ray
More is different
10^{-10} m
0.1 nm
Things Manmade
Head of a pin
1-2 mm
MicroElectroMechanical
(MEMS) devices
10 -100 μm wide
Pollen grain
Red blood cells
Zone plate x-ray "lens"
Outer ring spacing ~35 nm
Self-assembled,
Nature-inspired structure
Many 10s of nm
Nanotube electrode
Quantum corral of 48 iron atoms on copper surface
positioned one at a time with an STM tip
Corral diameter 14 nm
Carbon nanotube
~1.3 nm diameter
Carbon
buckyball
~1 nm
diameter
The Challenge
Fabricate and combine nanoscale building blocks to make useful devices, e.g., a photosynthetic reaction center with integral semiconductor storage.
Office of Basic Energy Sciences
Office of Science, U.S. DOE
Version 10-07-03, pmd

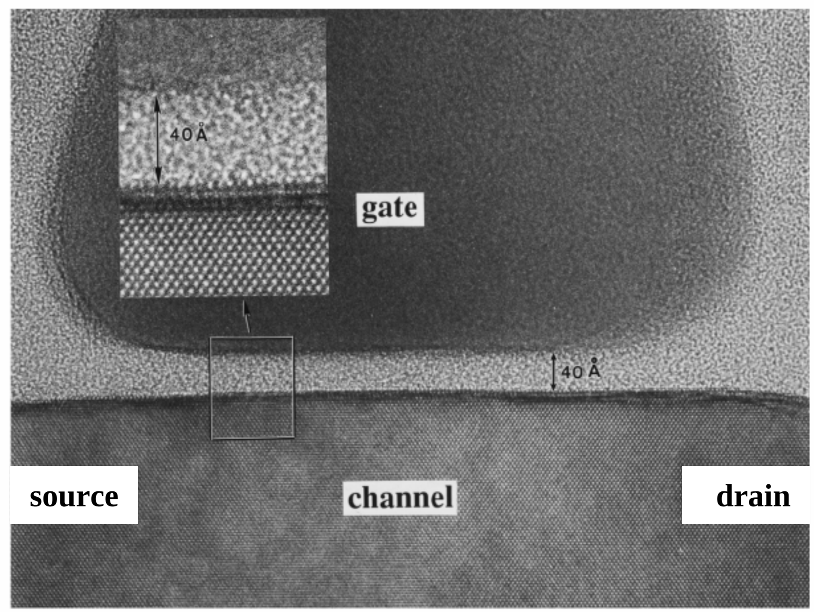
Moore's Law

No exponential is forever!

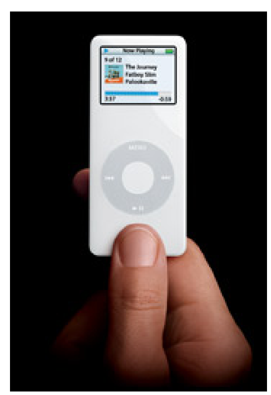
But can we delay "forever"?







Flash memory applications



Markets

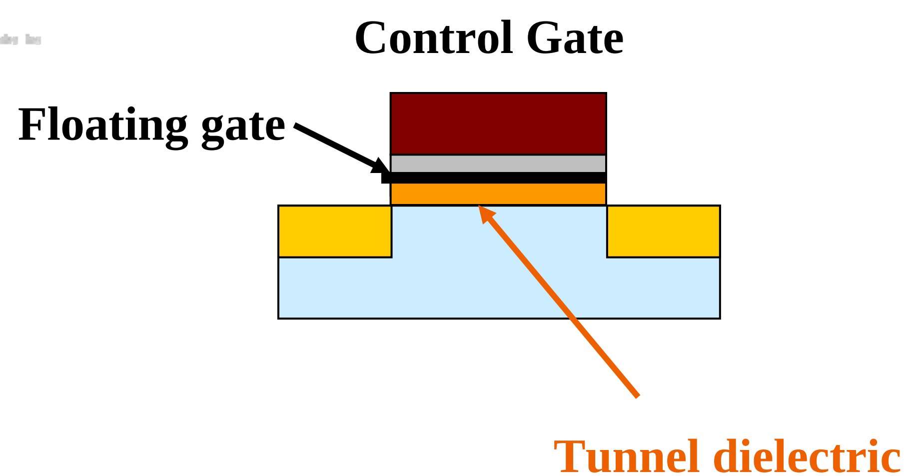
Consumer Electronics

Networking

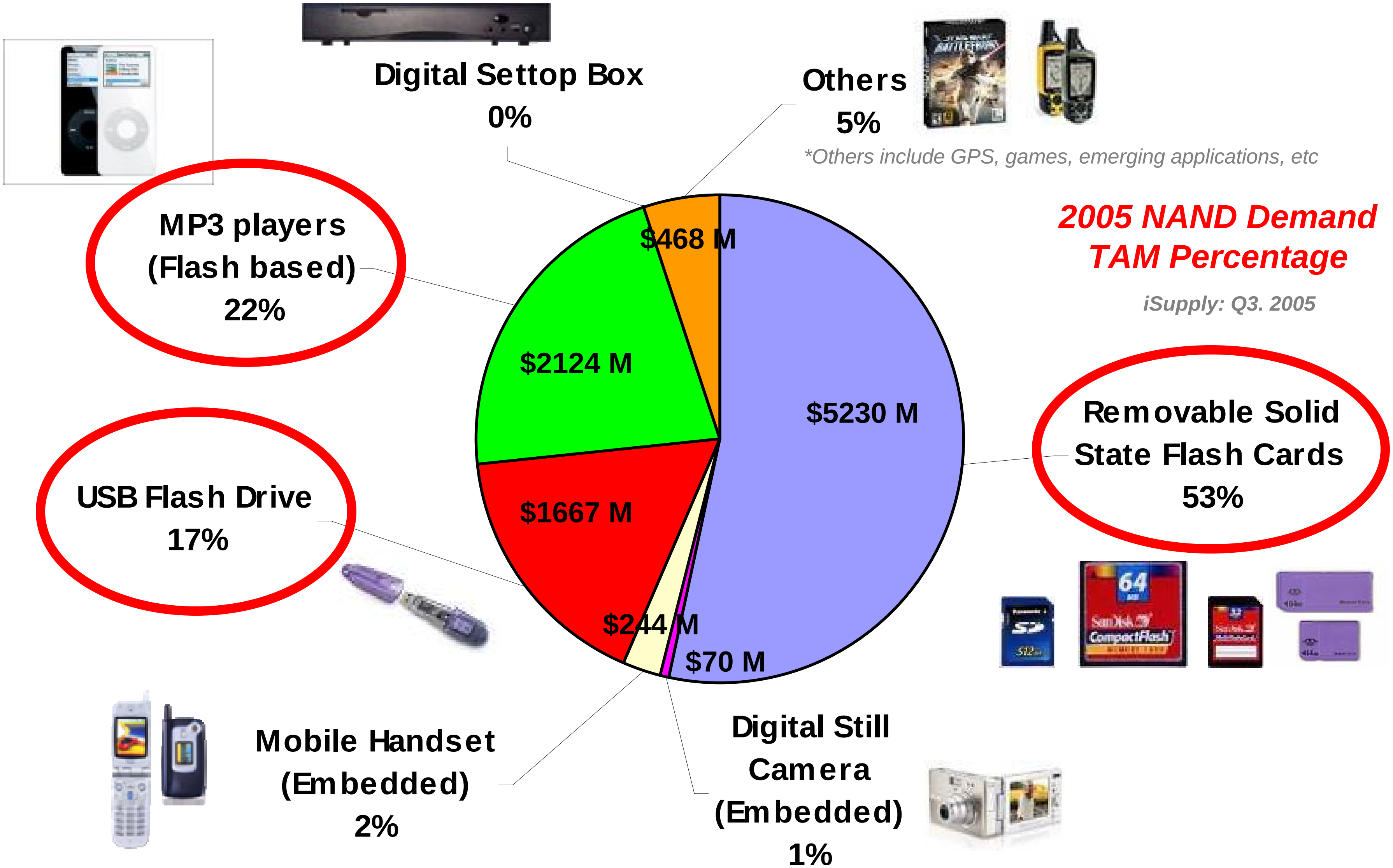
Wireless

Industrial Control

Automotive



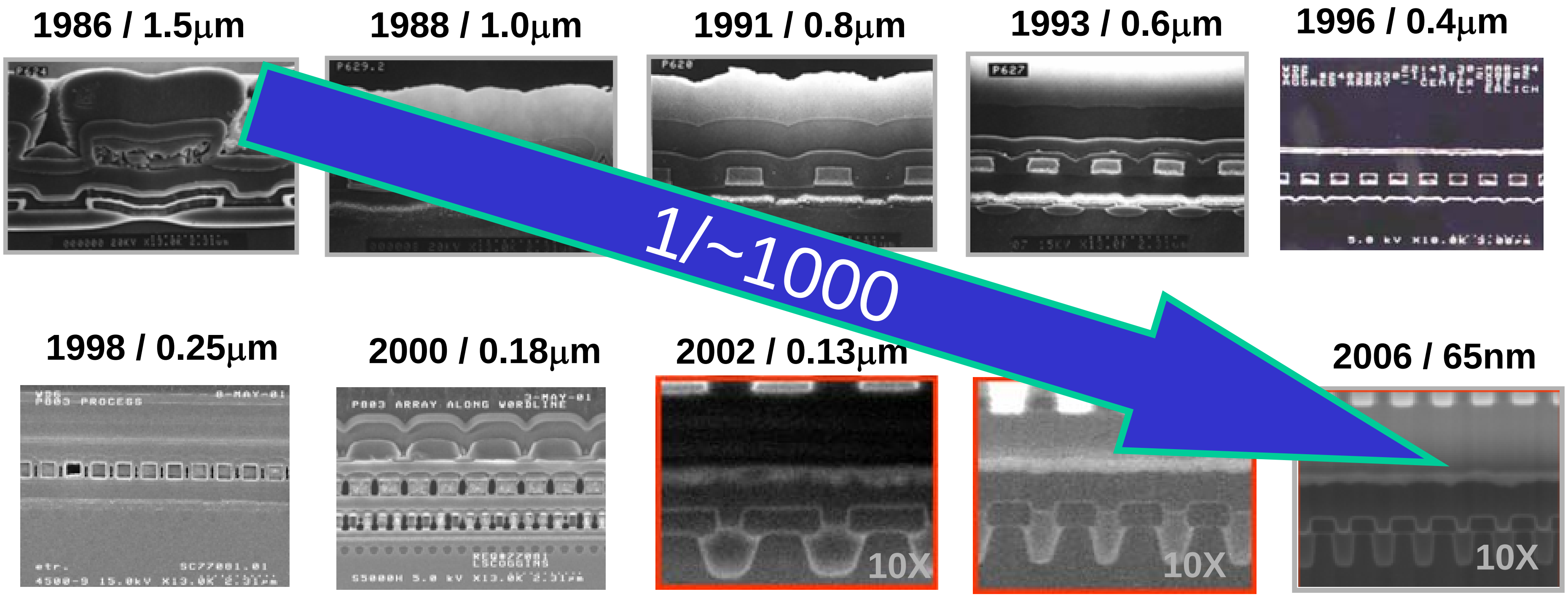
NAND Flash Market Segmentation



NOR Flash had TAM of 7B$, mostly in wireless cell phones.

Very high growth rates!!!

Flash Technology Scaling History



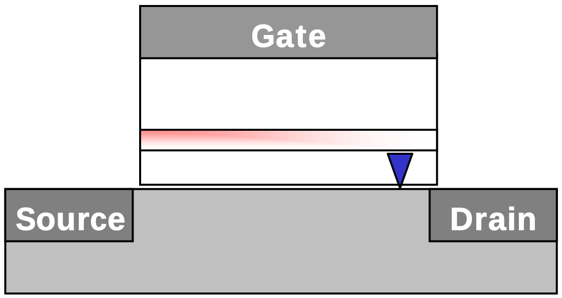
Volume Production Year / Technology Generation Source: Intel

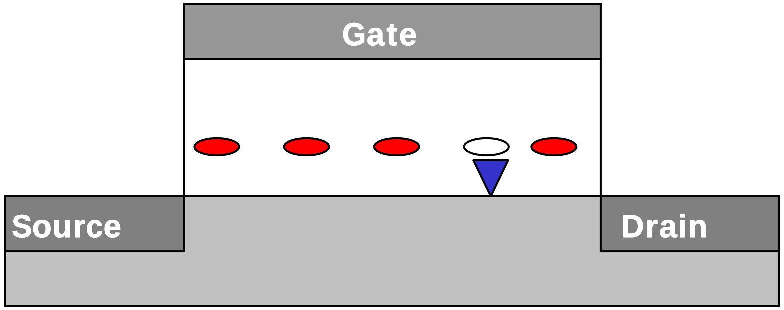
- **Flash Invented in mid 1980's**
  - **NOR flash evolved from EPROM**
  - **NAND started as poly-poly erase cell later evolving to present structure**
- **~20 years & 10 Generations of ETOX® (Intel NOR) High Volume Production**
- **8+ years & 5 Generations of MLC: 2bit / cell**

NVM- Long Term Requirements (ITRS 2006)

Year of Production	2014	2015	2016	2017	2018	2019	2020
DRAM ½ Pitch (nm) (contacted)	28	25	22	20	18	16	14
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	28	25	22	20	18	16	14
MPU Physical Gate Length (nm)	11	10	9	8	7	6	6
Flash technology NOR/NAND – F (nm) [1]	28/25	25/23	22/20	20/18	18/16	16/14	14/13
Flash NOR cell size – area factor a in multiples of F^2 [2], [3], [4], [5]	10–12	10–13	10–-13	11–14	11–14	12–14	12–14
Flash NAND cell size – area factor a in multiples of F^2 SLC/MLC [6]	4.0/1.0	4.0/1.0	4.0/1.0	4.0/1.0	4.0/1.0	4.0/1.0	4.0/1.0
Flash NOR typical cell size (μm^2) [7], [8]	0.0086	0.0073	0.0057	0.005	0.004	0.0034	0.0026
Flash NOR L_g-stack (physical – μm) [8], [9]	0.09	0.09	0.08	0.08	0.07	0.07	0.06
Flash NOR highest W/E voltage (V) [10], [11]	6–8	6–8	6–8	6–8	6–8	6–8	6–8
Flash NAND highest W/E voltage (V) [12]	15–17	15–17	15–17	15-17	15–17	15–17	15–17
Flash NOR I_{read} (μA) [13]	24–30	23–29	22–28	21–27	20–26	19–25	18–24
Flash coupling ratio [14]	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7	0.6-0.7	0.6-0.7
Flash NOR tunnel oxide thickness EOT (nm) [15]	7 – 8	7 – 8	7 – 8	7 – 8	7 – 8	7 – 8	7 – 8
Flash NAND tunnel oxide thickness EOT (nm) [16]	6–7	6–7	6–7	6–7	6–7	6–7	6–7
Flash NOR interpoly dielectric thickness EOT (nm) [17]	8–10	8–10	8–10	8–10	7–9	6–8	6–8
Flash NAND interpoly dielectric thickness (nm) [18]	9–10	9–10	9–10	9–10	9–10	9–10	9–10
Flash endurance (erase/write cycles) [19]	1.00E+06	1.00E+06	1.00E+07	1.00E+07	1.00E+07	1.00E+07	1.00E+07
Flash nonvolatile data retention (years) [20]	20	20	20	20	20	20	20
Flash maximum number of bits per cell (MLC) [21]	4	4	4	4	4	4	4

Nanoparticle Gate Flash Memory





Conventional Flash Memory

A defect totally discharges the floating gate

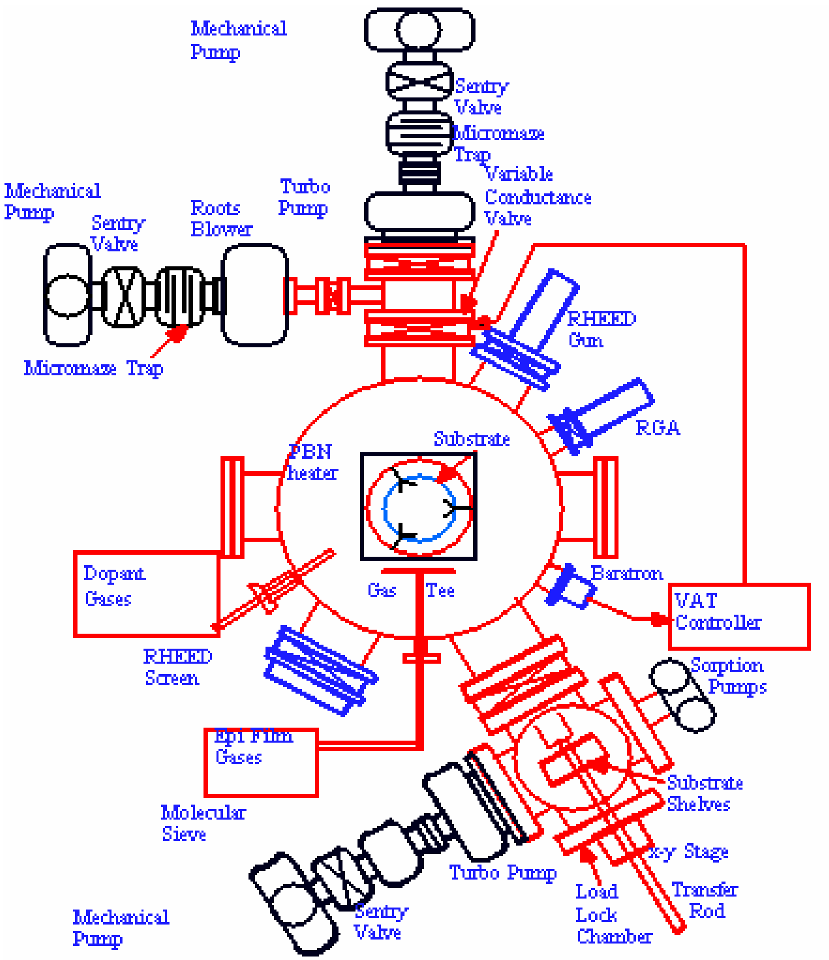
- Thick tunnel oxide
- High voltage/ power
- Low reliability/ speed

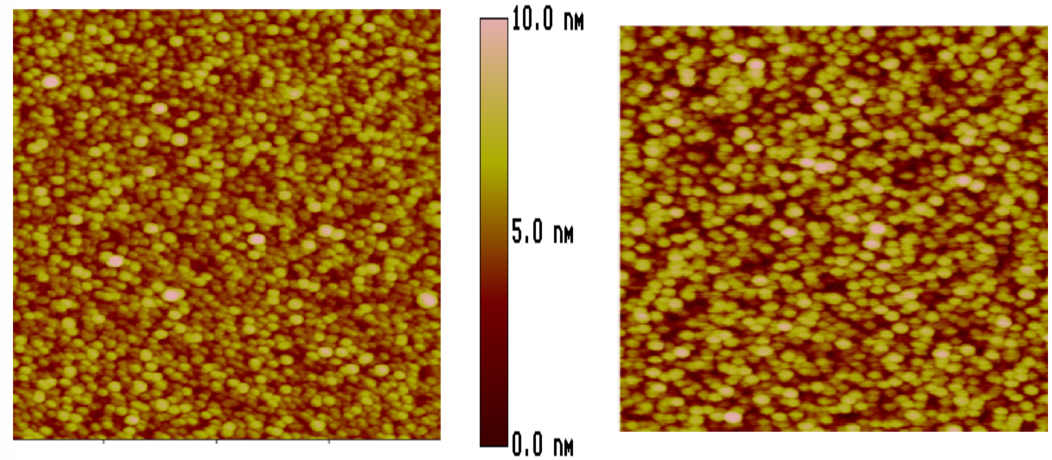
Nano-floating Gate Memory

A defect discharges only one dot

- High-k tunnel oxide
- Speed/ power/ density better
- Reliability improved
- *New phenomena*- self-assembly, Coulomb blockade, multi-level cells

SiGe Nanocrystals on High-K Dielectrics



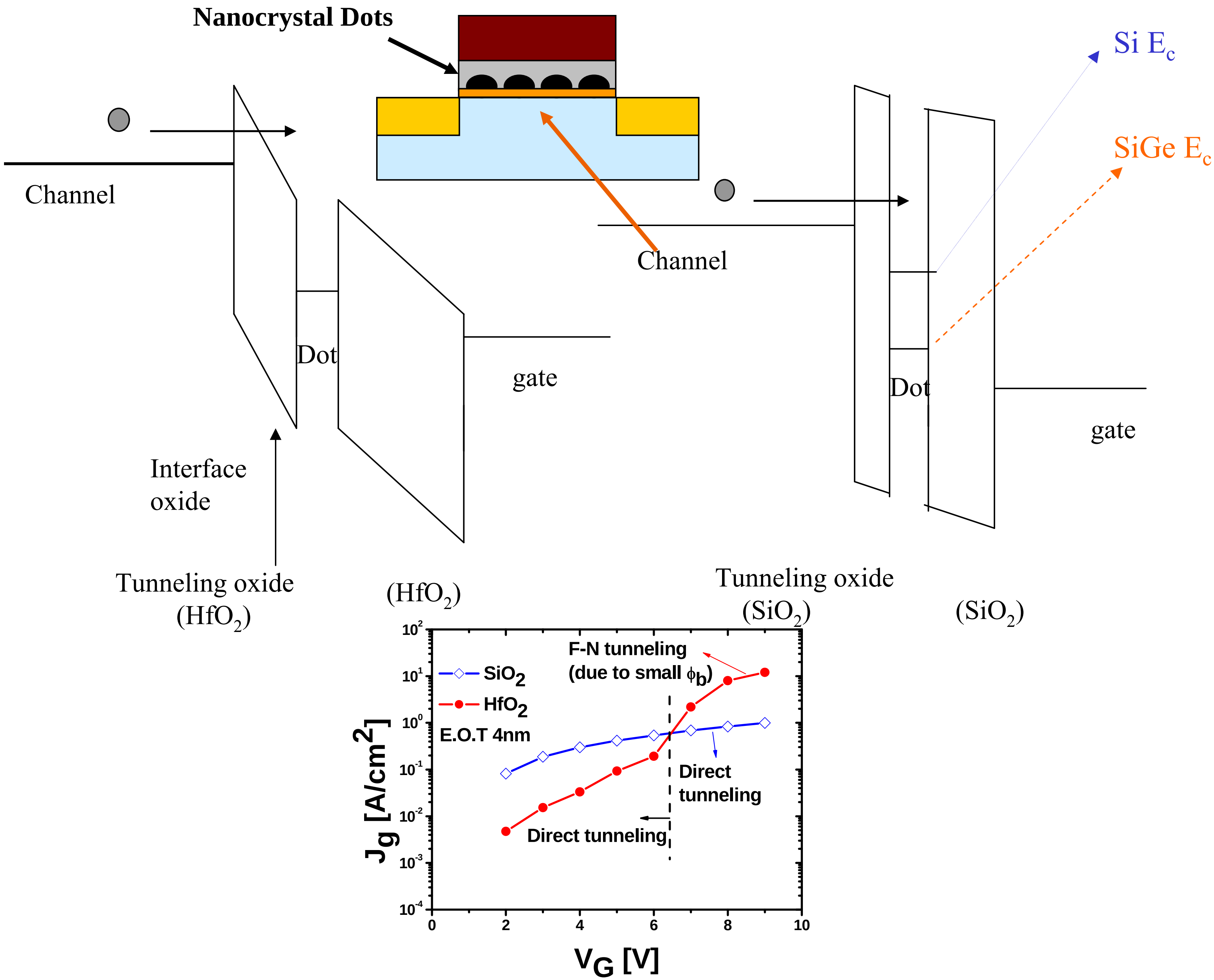


HfO_2 SiO_2

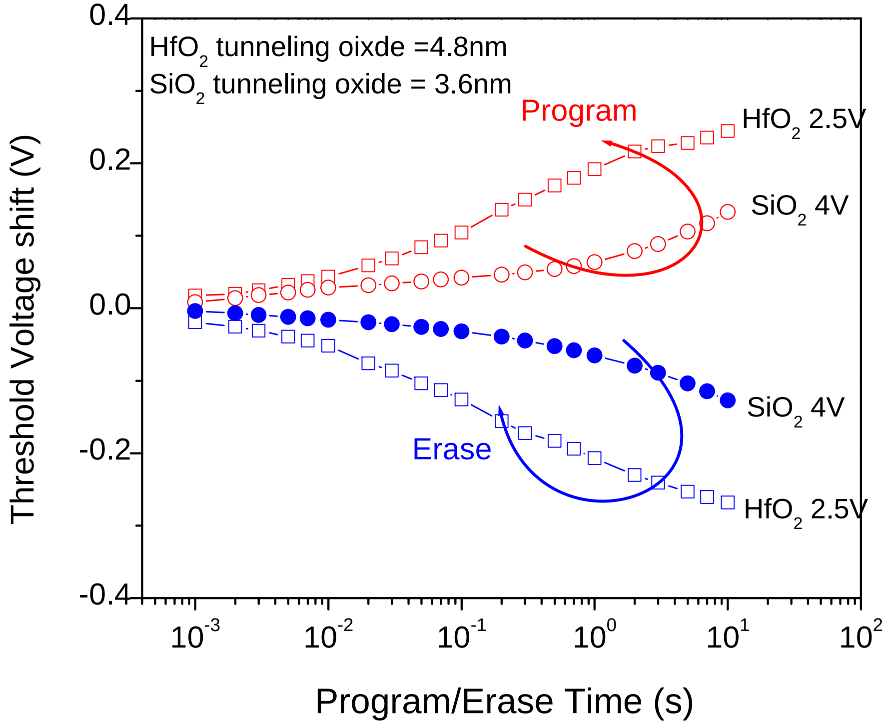
AFM scans (1 micron x 1micron) showing SiGe dots grown at ~ 500ºC for 90 s with 0.75 gas ratio of GeH_4 to Si_2H_6.

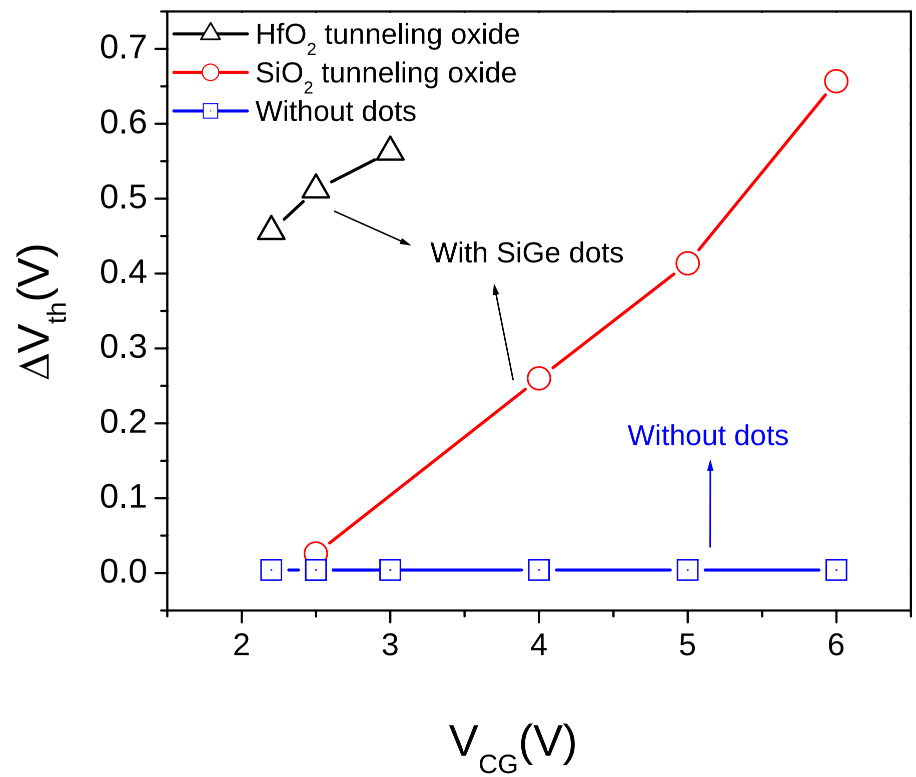
Kim., Banerjee, Growth of germanium quantum dots on different dielectric substrates by chemical-vapor deposition, J VAC SCI TECHNOL B 19 (4): 2001

Band diagram of HfO_2 and SiO_2 dielectric at low program voltage



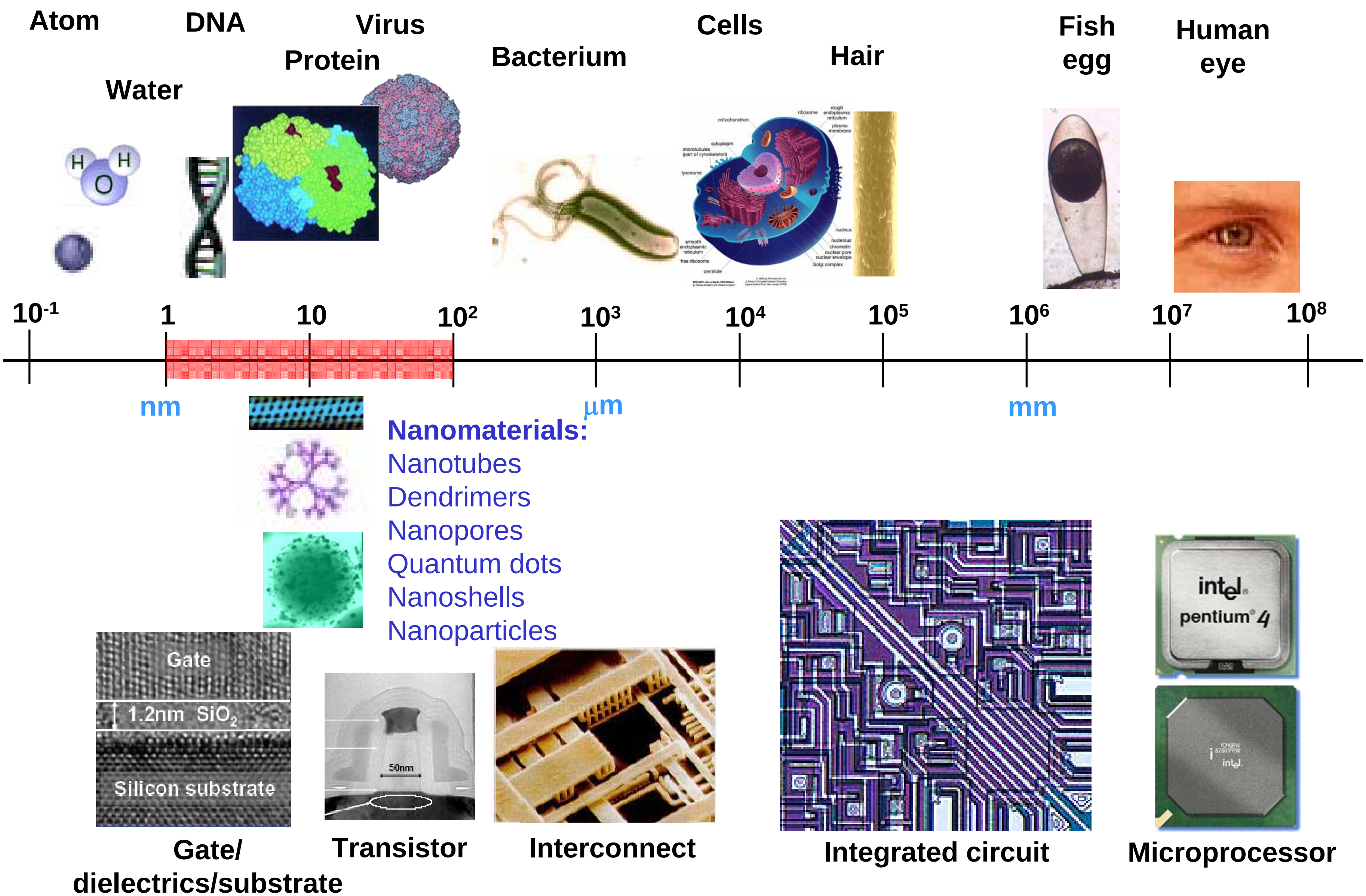
Program & Erase Transient Characteristics





Kim DW, Kim T, Banerjee SK, ELECTRON DEV 50 (9): 1823-1829 SEP 2003

The Bio-nanometer Perspective



Slide by C. Li

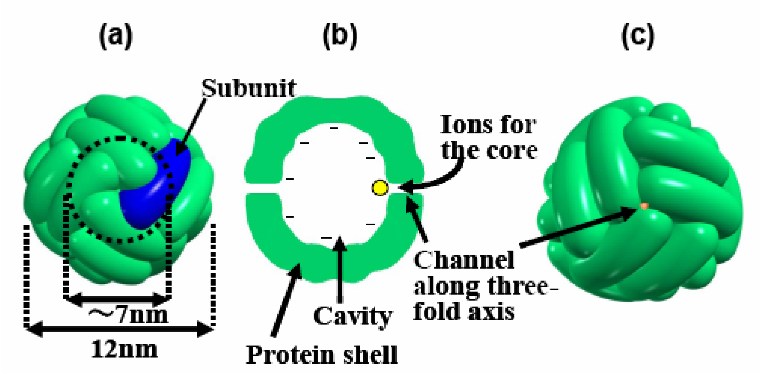
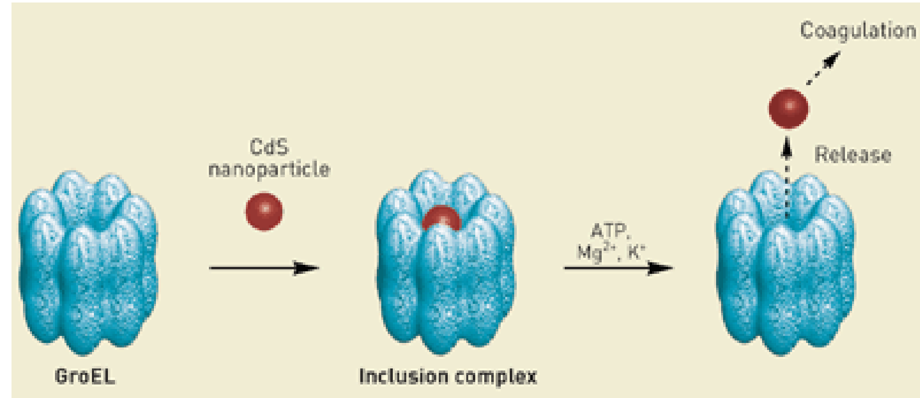


Fig. 1. Schematic drawings of apoferritin molecule, (a) looking down along four fold axis (b) cross-section of apoferritin (c) looking down along three fold axis.



Yamashita, IEDM 2006, p. 447 (Ferritin)

Ishii, Nature Vol. 423, 2003 (Chaperonin)

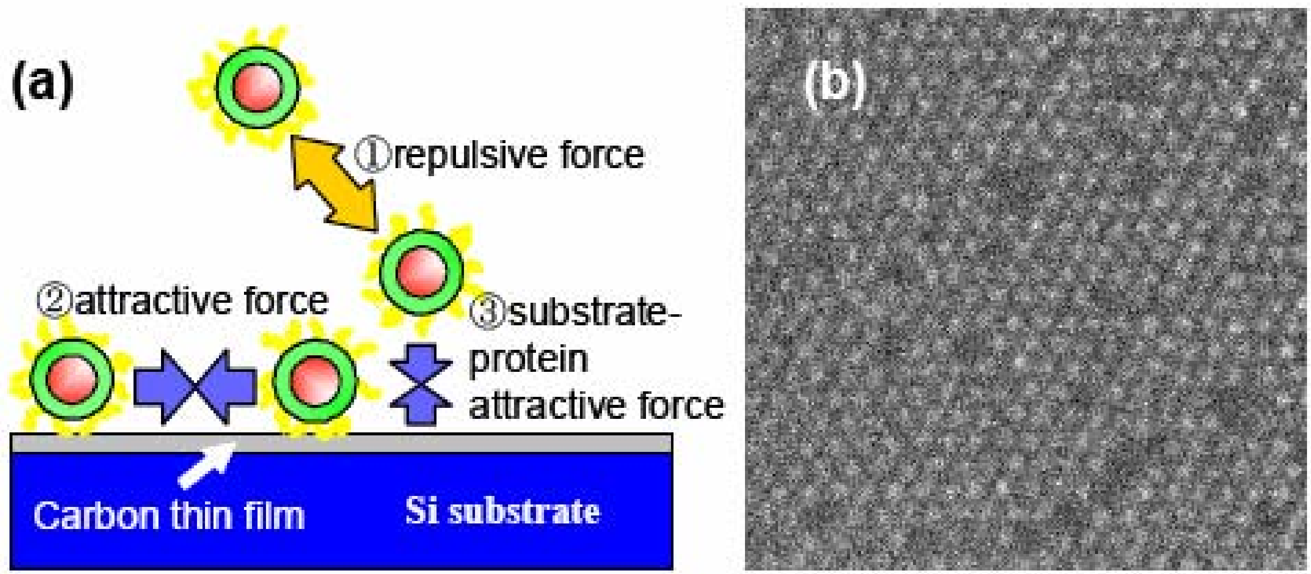
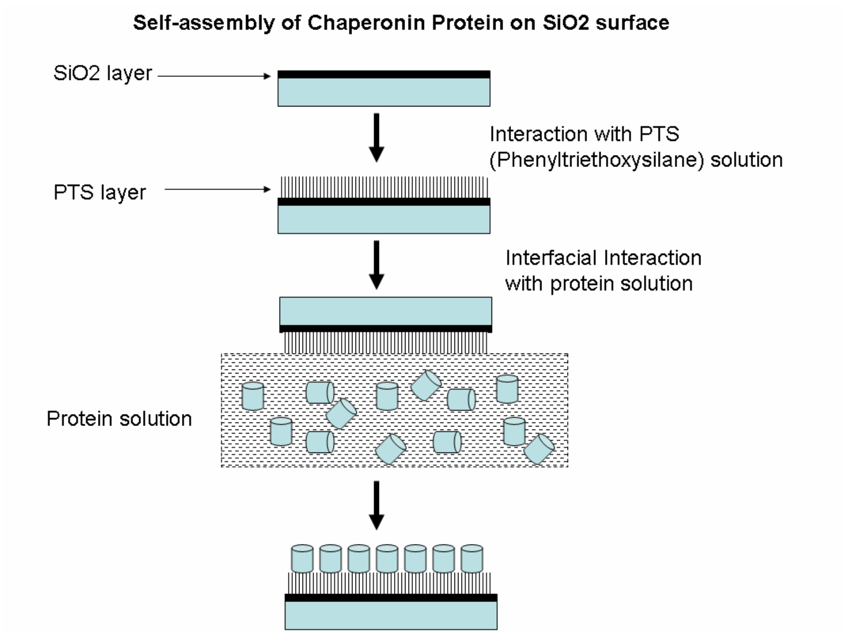
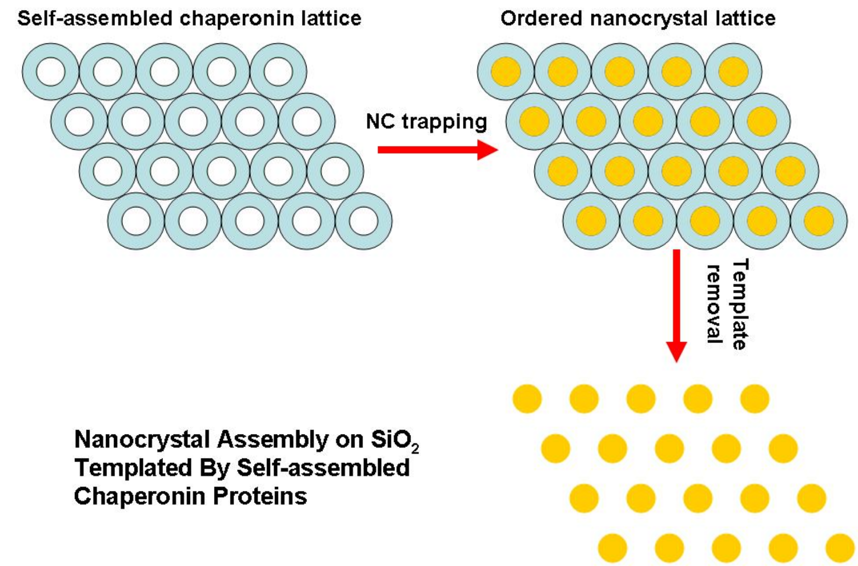
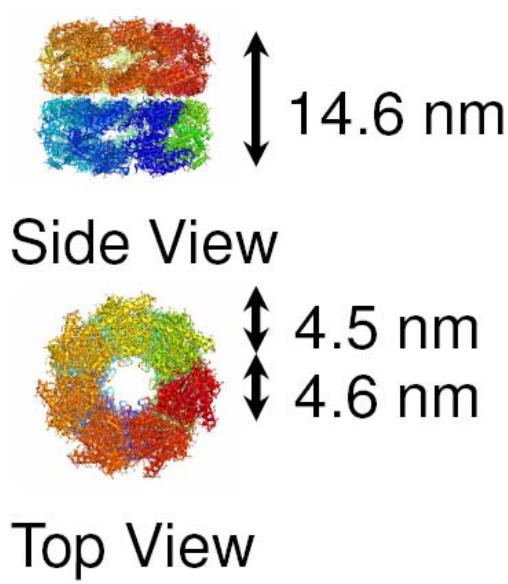


Fig. 3. (a) Interaction of protein-protein and substrate-protein bestowed by the target-specific affinity peptides. (b) Two-dimensional hexagonally close packed array directly formed on the Si substrate.

Protein assembly of Metal (Co, Au,..) and Semiconductor (PbSe, CdSe, Ge ..) NCs

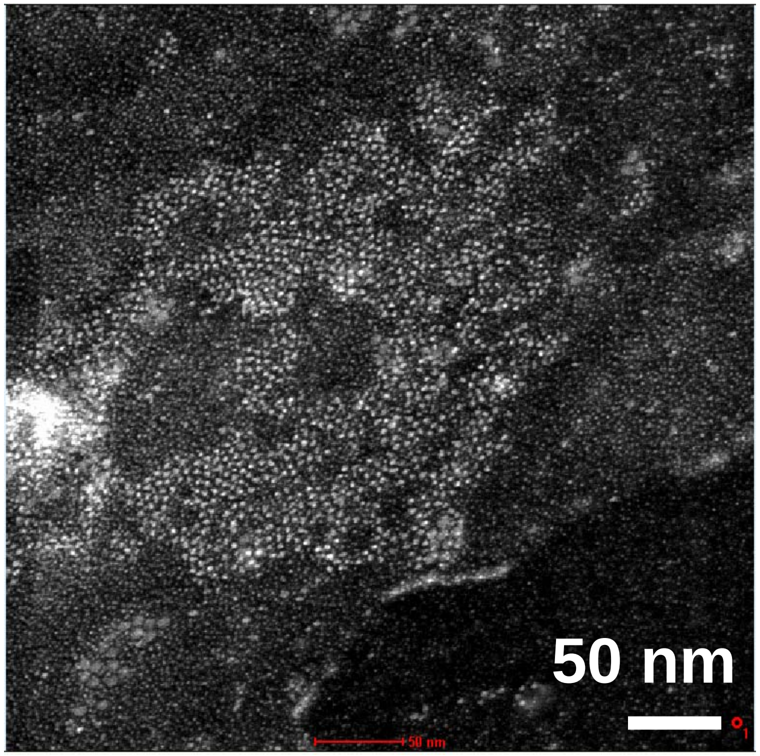




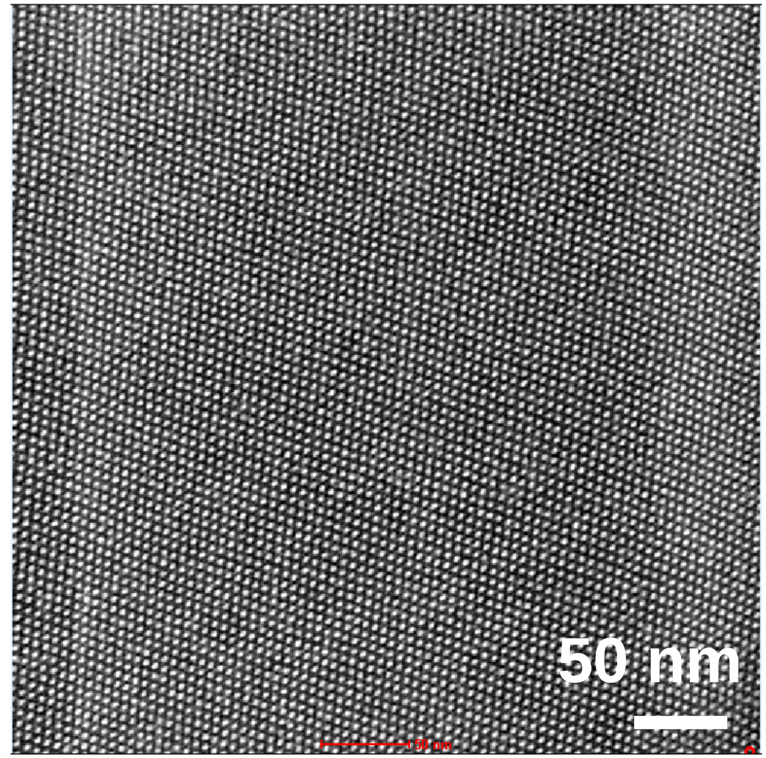


Schematic structure of Chaperonin 60 (GroEL)

STEM images of PbSe nanocrystals on SiO_2



Without chaperonin template

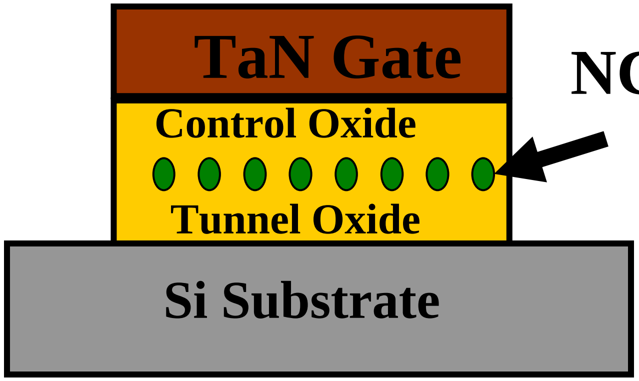


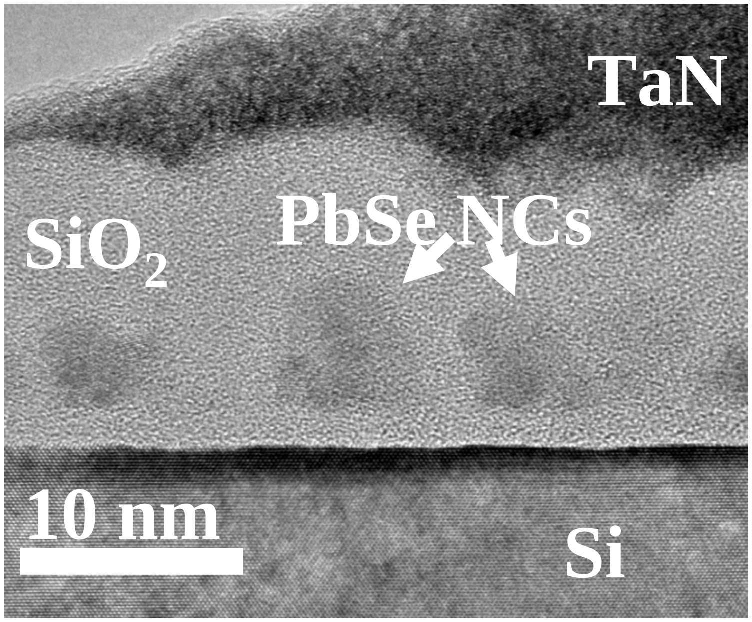
With chaperonin template

Various semiconductor and metal nanocrystals self-assembled, including Co

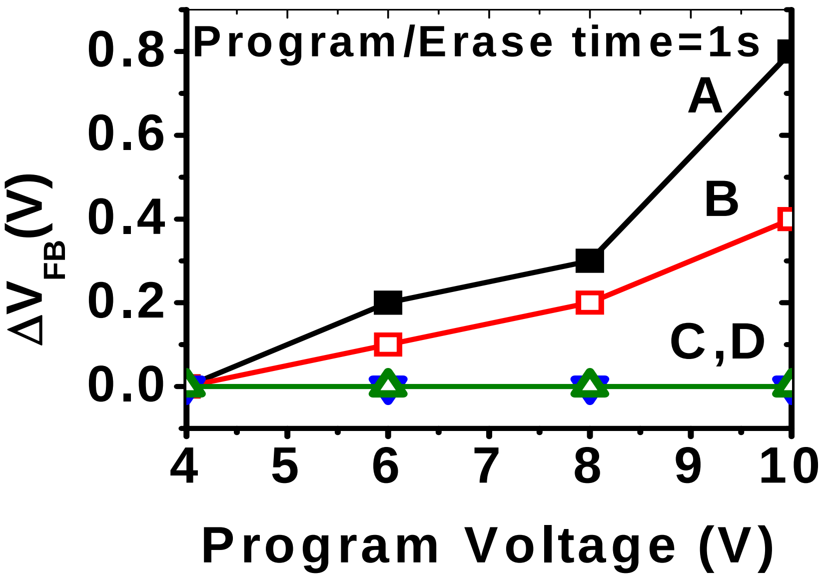
Density~ 10^{12} cm^{-2}

ΔV_{FB} comparison of protein-mediated PbSe NC MOS capacitor and control samples

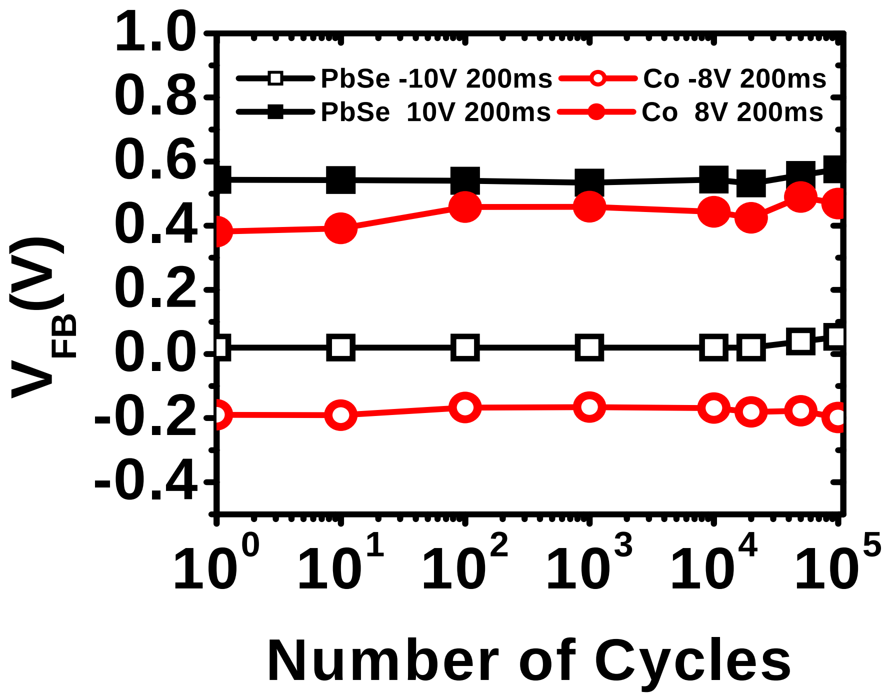


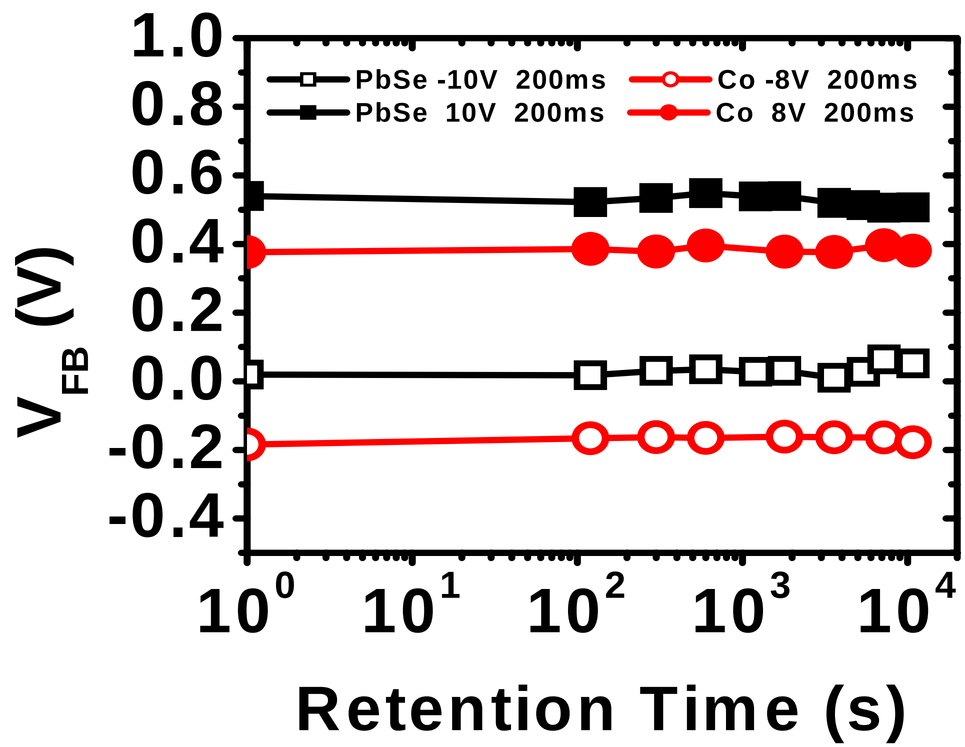


	PbSe NCs	Protein Template (Annealed)
A	✓	✓
B	✓	×
C	×	✓
D	×	×



Endurance and Retention Characteristics

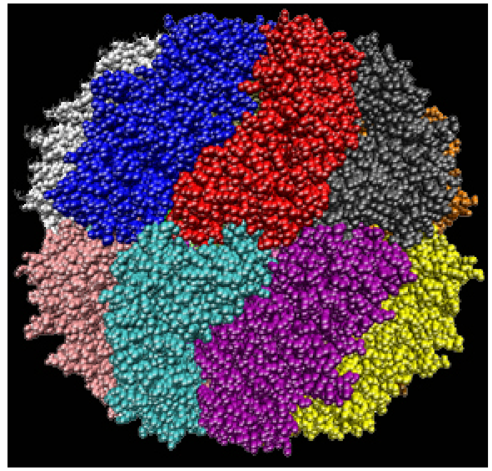


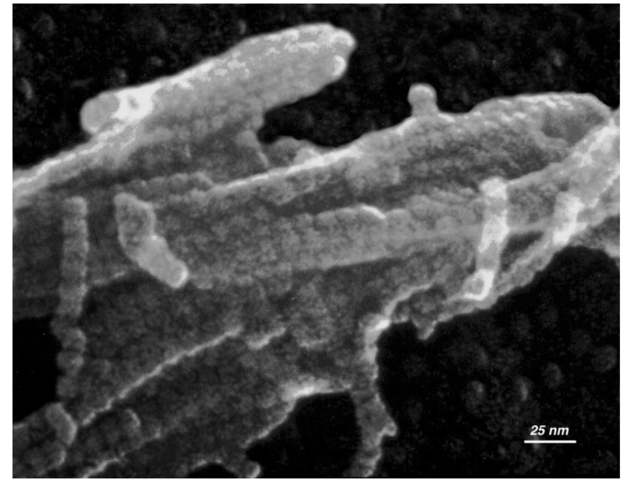


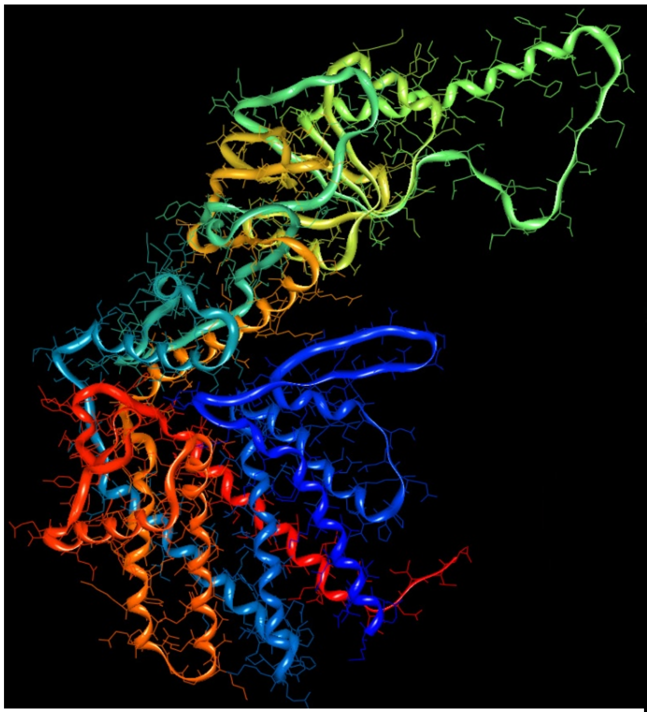
Devices survived 10^5 cycles of program/erase operation; no sign of window closure

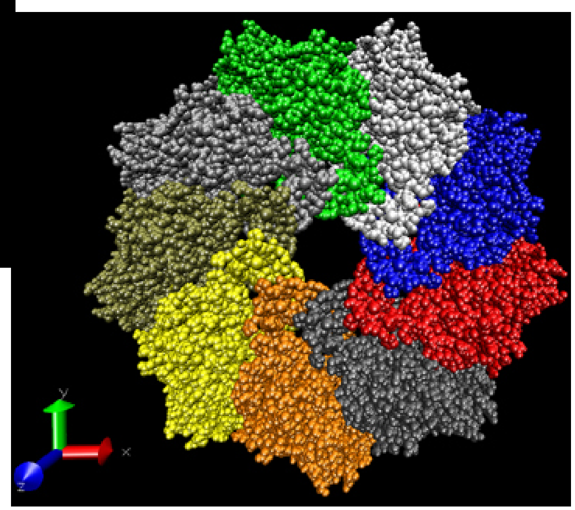
Devices have good retention.

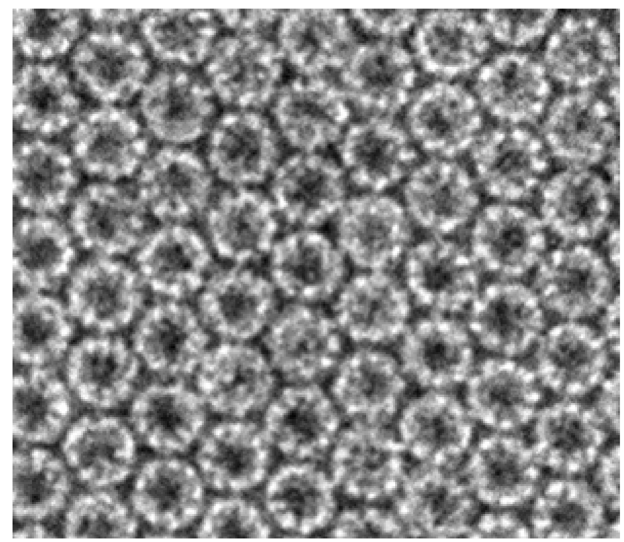
Heat Shock Proteins (Trent, NASA)



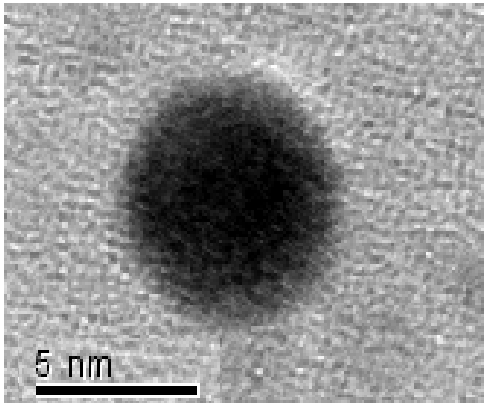




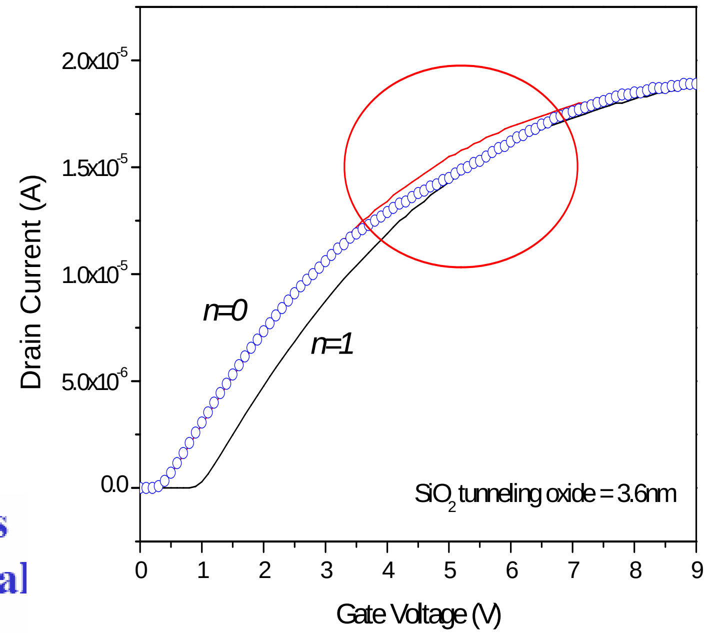




Coulomb Blockade in SiGe dot on SiO_2 and HfO_2

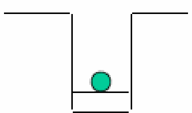


SiGe on SiO_2 @ 520 ºC

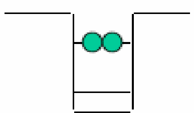


- **Limits programming by direct tunneling at low voltages**
- **Multiple electron storage reduces life-time in nanocrystal**

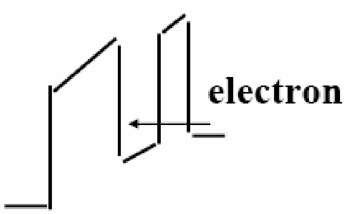
Putting an electron on nanocrystal raises other energy levels

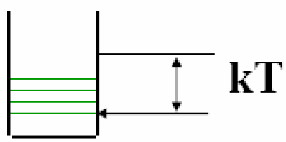


$dE \sim \frac{e^2}{C}$

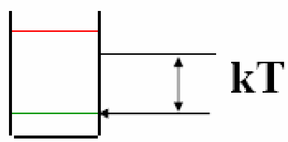


For small capcitor ($C \sim 10^{-18}$ F), dE can be > thermal energy, kT





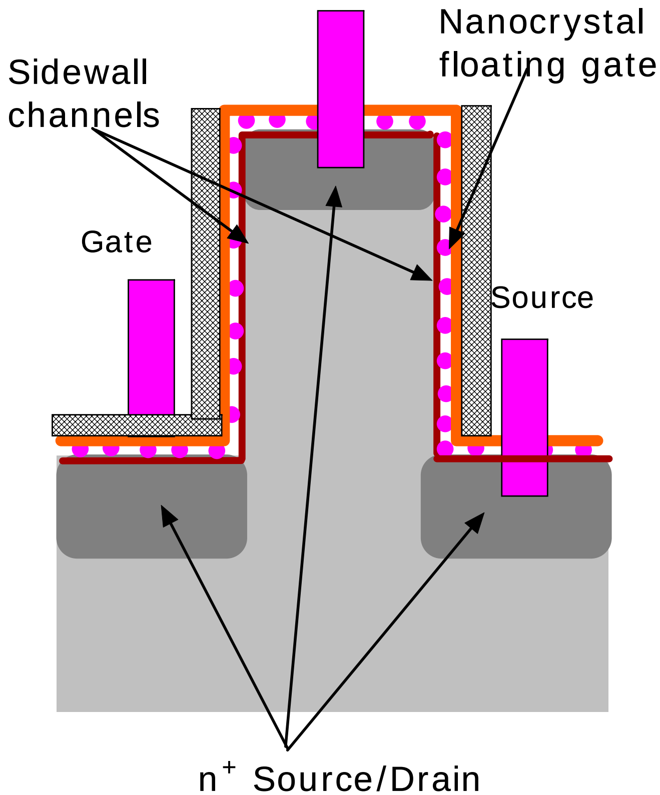
Large C, high T



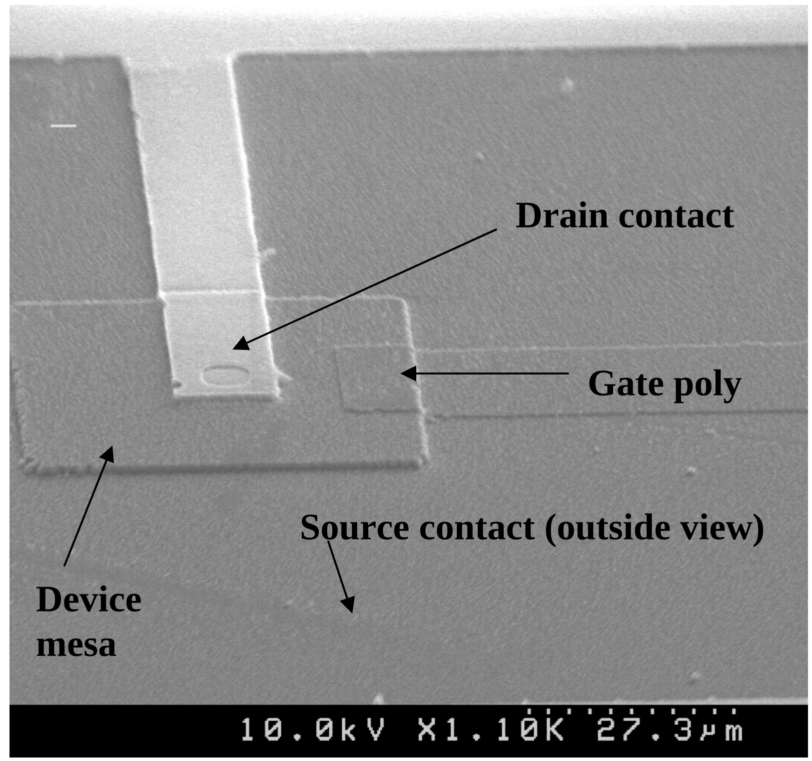
Small C, low T

- *Low T: Given a Write voltage, fixed no. of electrons in nanocrystal*
- *For nanocrystals < 5nm, this effect is significant at room temperature*

Vertical Flash Memory

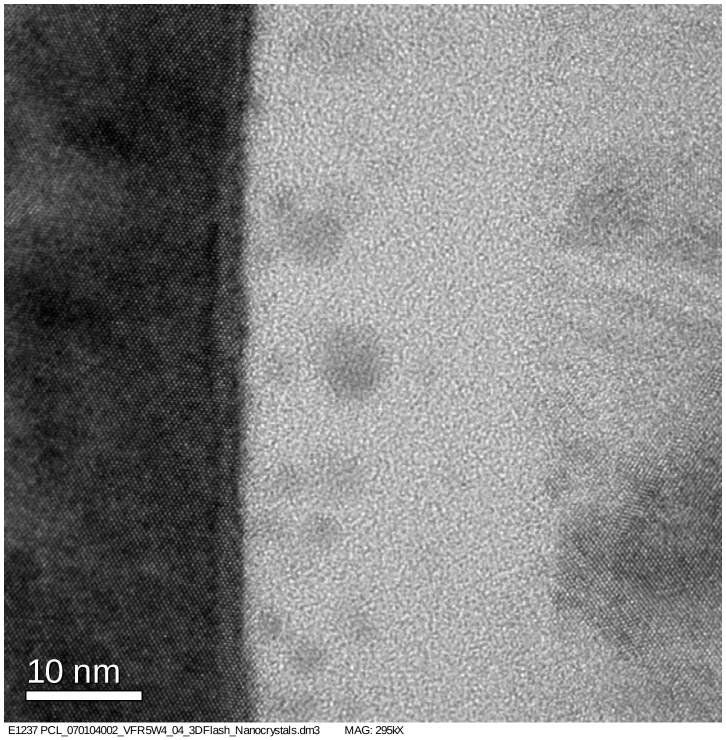


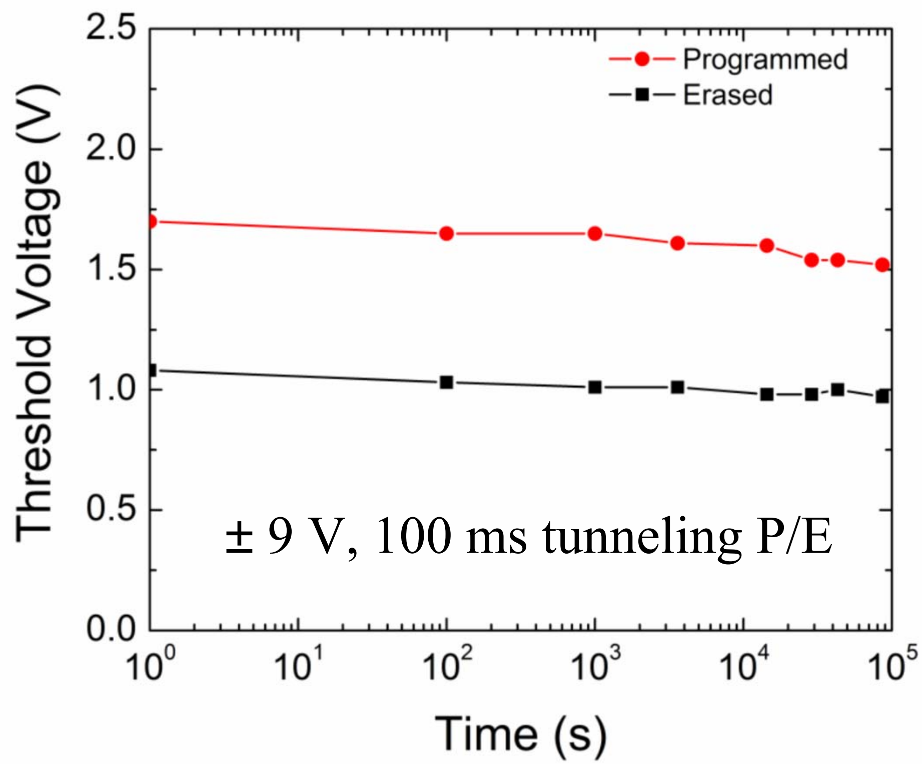
Schematic side view



Scanning Electron Micrograph

Vertical Flash Retention at 300K

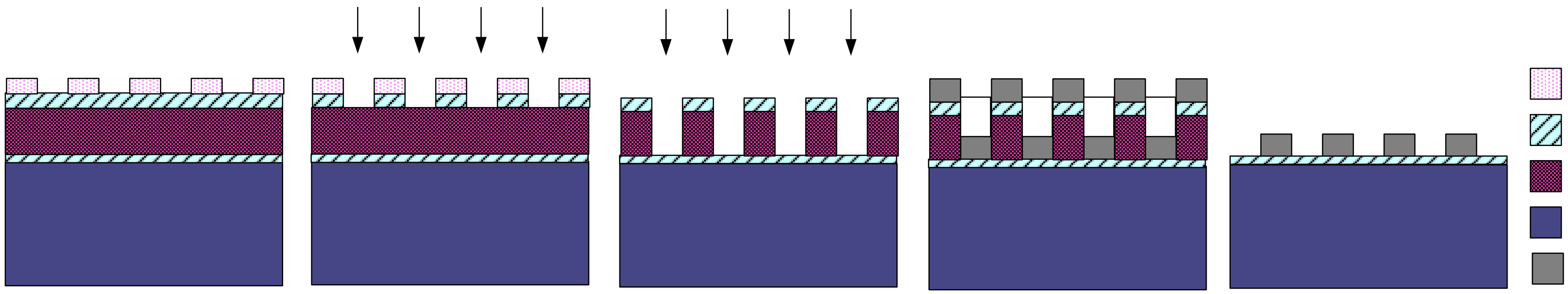




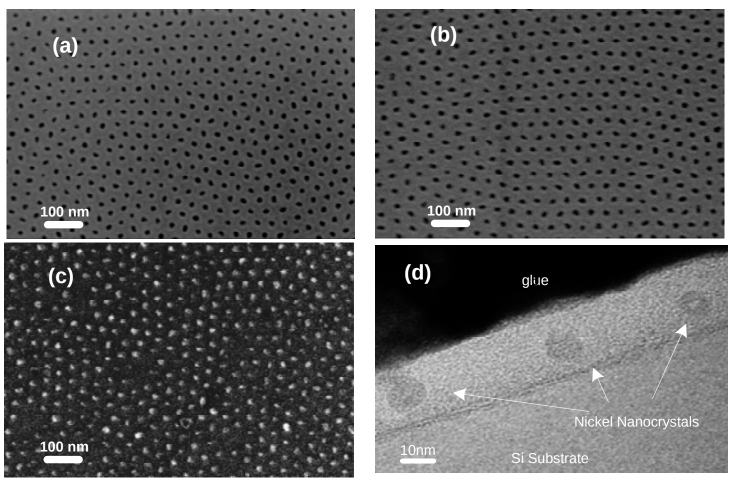
Nanoparticle Self-Assembly Using PS-*b*-PMMA Copolymer

Process Flow

Employing a sandwich of organic/ inorganic/ organic layers (Polyimide/ SiO_2/ PS-*b*-PMMA) to engineer the aspect ratio of the patterns



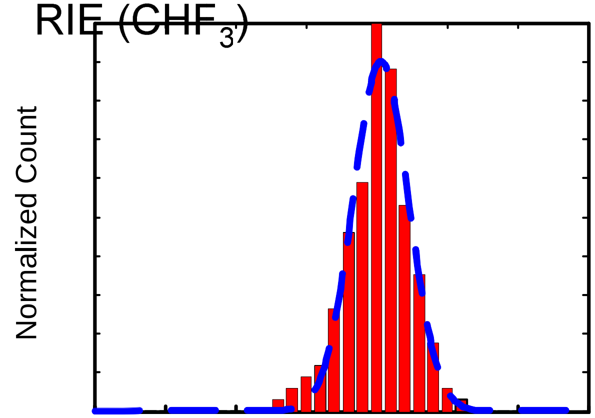
Material Characterization



SEM micrographs of (a) Copolymer template, (b) transferred polymer patterns into the underlying SiO2 layer, (c) ultimate array of Ni nanoparticles. (d) Cross-sectional image of the embedded nanoparticles within SiO_2.

RIE (CHF_3)

RIE (O_2)



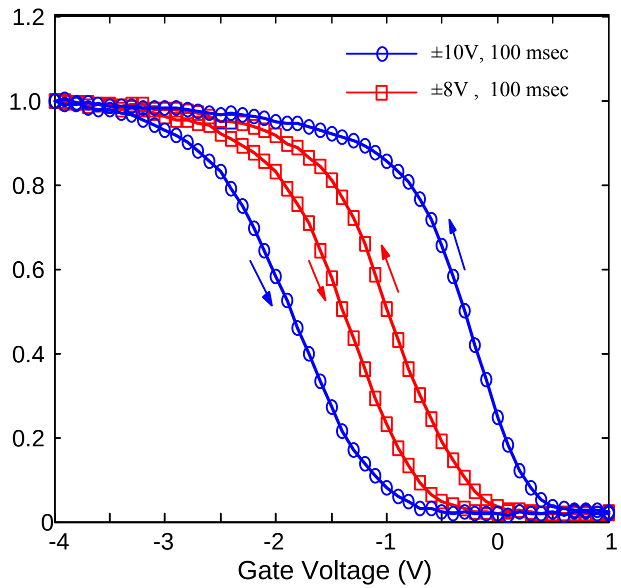
Histogram of the copolymer pore size distribution shown in Fig. (a)

(a)

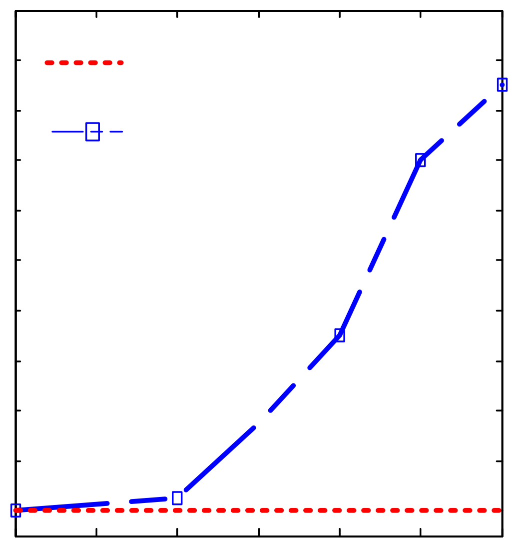
(b)

(c)

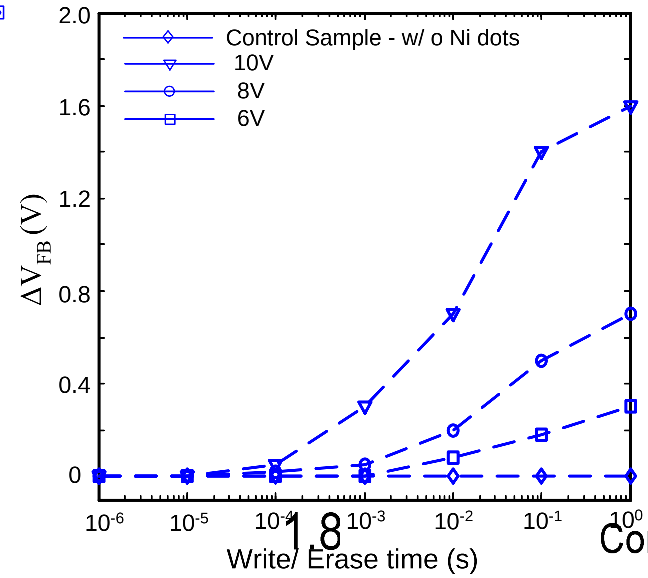
Characteristics of MOSCAP Memory Devices



High frequency C-V Characteristics @ 1MHz



Memory window for different program voltages



Transient characteristics of the memory device

Control sar

w/ Ni dots

1.4

1.0

ce (C/C_{ox})

V_{FB} (V)

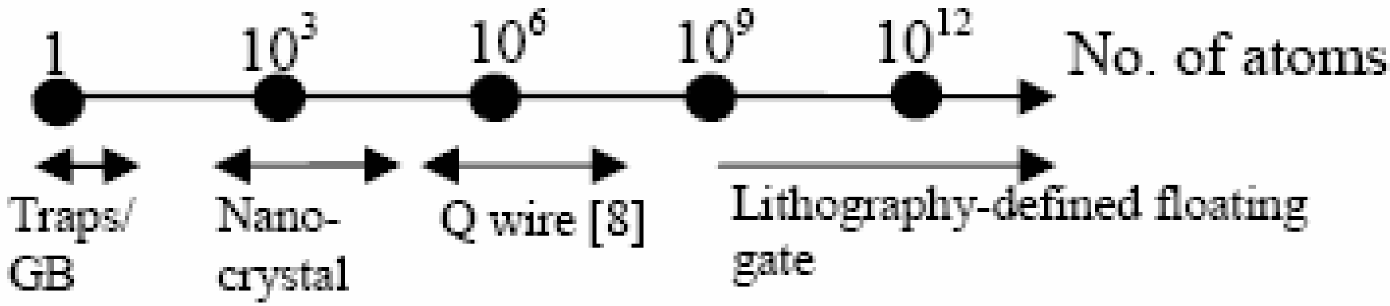


Fig. 1. Nonvolatile charge storage node comparisons.

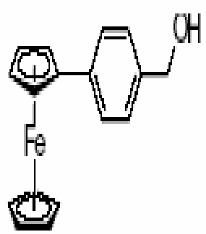
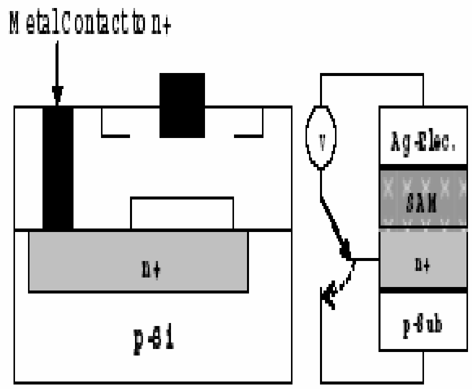
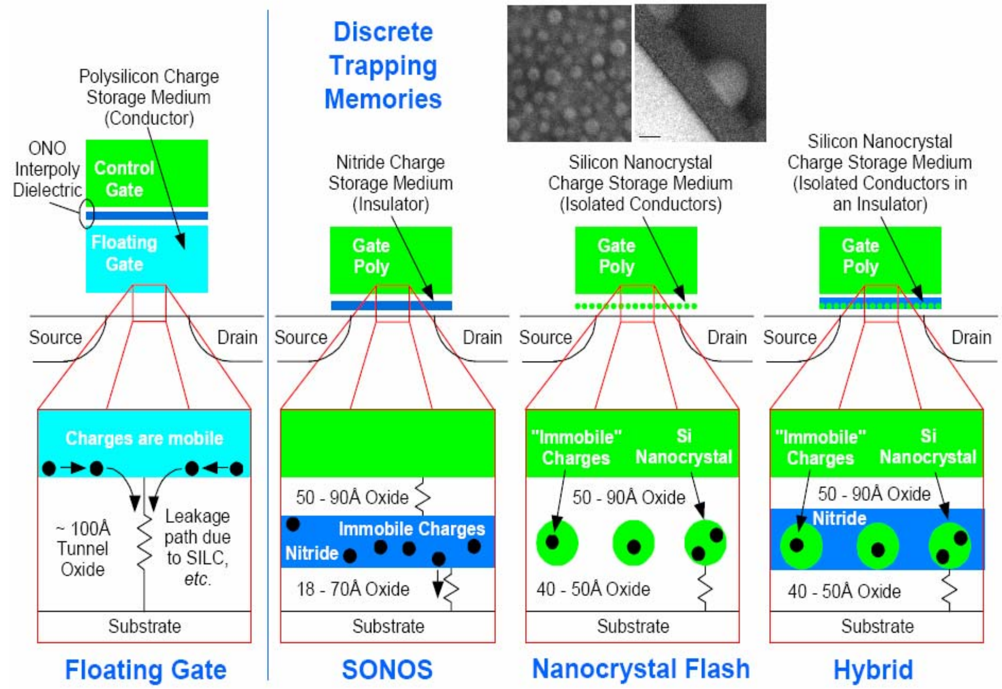


Figure 1b. Molecular structure of Fc-BzOH.





Molecular Memories, Misra,
IEDM p.537 2003; IEDM p. 707 2004.

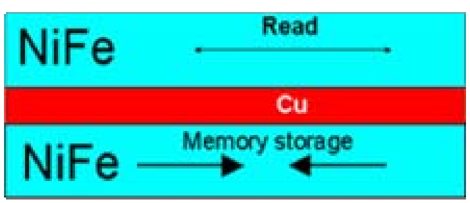
Variability, DOS ?

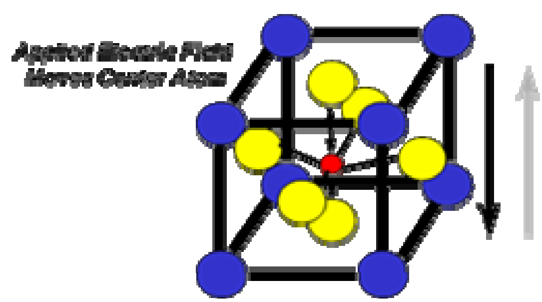
SONOS trap densities ~10^{19} cm^{-3} eV^{-1}
For ~3 nm layer, ~3X10^{12} cm^{-2} traps
spatially and energetically distributed

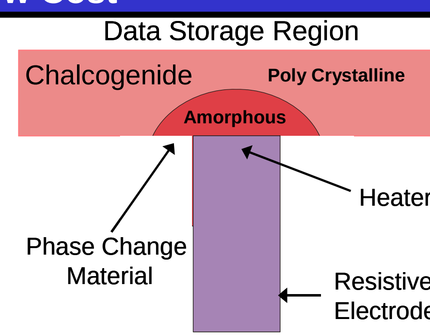
Non-MOS Memory Contenders (adapted from Fazio, Intel)

	MRAM	FeRAM	Phase Change
Cell Size λ^2	Large ~40 → 20	Large ~25	Small ~6.5
CMOS Integration	<200C Post Magnetic Tight MJT control	Fe reduces in hydrogen Etching difficult for Fe	Compatible with backend CMOS metal processing
Read	Non-Destructive, Fast, Low Power	Destructive: Endurance limited read	Non-Destructive, Moderate speed, Scales poorly
Write	Power constrained, Scales poorly; half select issue	Low power capacitive Theoretically good speed	Power constrained, large drivers, Improves with scaling
Cycling Endurance	Theoretically Infinite	1e-8 → 1e12; claims made, but limited data	~1e12; claims made, but limited data; Erratic failures
Scalability	Write current increases with scaling, materials engineering required at each scaling node; superparamagnetic limit?	3D cell required sub 90nm. Material engineering required at each scaling node	No material changes, No physical limits known down to ~5nm
Application	Embedded Working Memory Low Density	Embedded Low Power Low Density	Stand Alone or Embedded High Density Low Cost

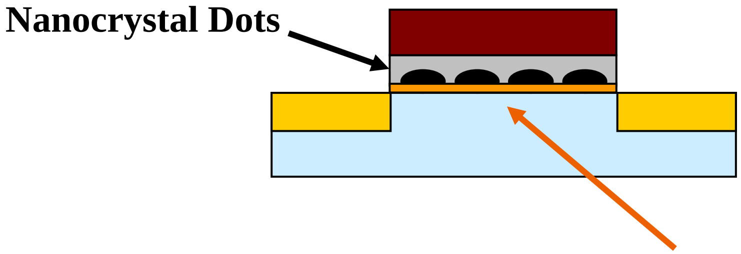
Color Code
Poor
OK
Good

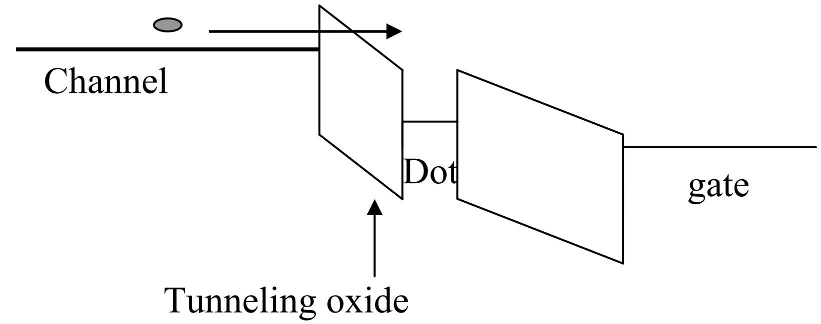






Memory Type		SRAM	DRAM	MRAM Industry	NOR	NAND	FeRAM	PCM
Cell Elements		6T	1T1C	1R 1T	1T		1T1C	1T1R
Feature Size F, nm	2007	90/65	65	180	65/57	65/57	130	90
	2018	*18*	*18*	*22*	*25*	*25*	*25*	*18*
Cell Area	2007	140 F^2	7.5 F^2	25 F^2	9-11 F^2	4 F^2	34 F^2	7.2 F^2
	2018	*140 F^2*	*5 F^2*	*16 F^2*	*9/4 F^2*	*4/1 F^2*	*16 F^2*	*4.7 F^2*
Read Time	2007	0.4 ns	<15 ns	<25 ns	14 ns	70 ns	80 ns	60 ns
	2018	*70 ps*	*<15 ns*	*<0.5 ns*	*2.5 ns*	*12 ns*	*<20 ns*	*<60 ns*
W/E Time	2007	0.4 ns	<15 ns	<25 ns	1 µs/10 ms	1ms/0.1 ms	15 ns	50/120 ns
	2018	*<0.1 ns*	*<15 ns*	*<0.5 ns*	*1 µs/10 ms*	*1ms/0.1 ms*	*1 ns*	*Not known*
Retention Time	2007	Voltatile	64 ms	> 10 y	> 10 y	> 10 y	> 10 y	> 10 y
	2018	*Voltatile*	*64 ms*	*> 10 y*	*> 10 y*	*> 10 y*	*> 10 y*	*> 10 y*
Write Cycles	2007	>3E16	>3E16	>1E16	>1E5	>1E5	1E13	1E12
	2018	*>3E16*	*>3E16*	*>1E16*	*>1E5*	*>1E5*	*>1E16*	*1E15*
Write operating voltage (V)	2007	1.2	2.5	1.8	7-9	15-17	0.9 - 3.3	3
	2018	*0.7*	*1.5*	*<1.8*	*6-8*	*15-17*	*0.7 - 1*	*<3*
Read operating voltage (V)	2007	1.2	2.5	1.8	2.5	2.5	09 - 3.3	3
	2018	*0.8*	*1.5*	*<1.8*	*1.2*	*1.2*	*0.7 - 1*	*<3*
Write energy (J/bit)	2007	7E-16	1E-16	1E-10	8E-15	8E-15	2E-14	1E-10
	2018	*2E-17*	*4E-17*	*2E-11*	*3E-15*	*3E-15*	*4E-15*	*Not known*
3D Potential		No	No	Yes	No	No	No	Yes
Cell Stacking		No	No	Yes	Yes	Yes	No	Not known
MLC Potential		No	No	Yes	Yes	Yes	No	Not known
Die Efficiency %		70	56-63	Not known	35-46	54-60	Not known	Not known





- End-of-roadmap (2020, L=6 nm) NAND F= 14 nm, Tox= 6 nm, Cell area ~ 1000 $nm^{2;}$ (3X for NOR)
- NC spacing ~ tunnel oxide thickness ~ 4 nm
- Spacing & NC size/DOS affects charge capture cross-section & Read
- Optimal spacing depends on dielectric & NC band diagram, retention (10^8 s), Erase/Write times (10^{-6} s)→ E_{barr}= 1eV
- For NC densities of ~ 10^{12} cm^{-2}, room for ~10 NC
- Variability is a challenge for NC & trap-based cells
- Self-assembly and non-planar structures?

There is plenty of room at the bottom! Feynman

The fundamental parameters of the human brain[132] are estimated to be:

- Number of neurons—2E10
- A single neuron can make 100 to 10,000 synaptic connections
- Mass—1.3 kg[133]
- Volume—600 cm^3
- Power consumption—15–30 Watts
- Information stored—1E12 (short term) bits
- Information processed—1E16 bits/second

- Will these devices make it? The answer is a very definite…..

Maybe!!