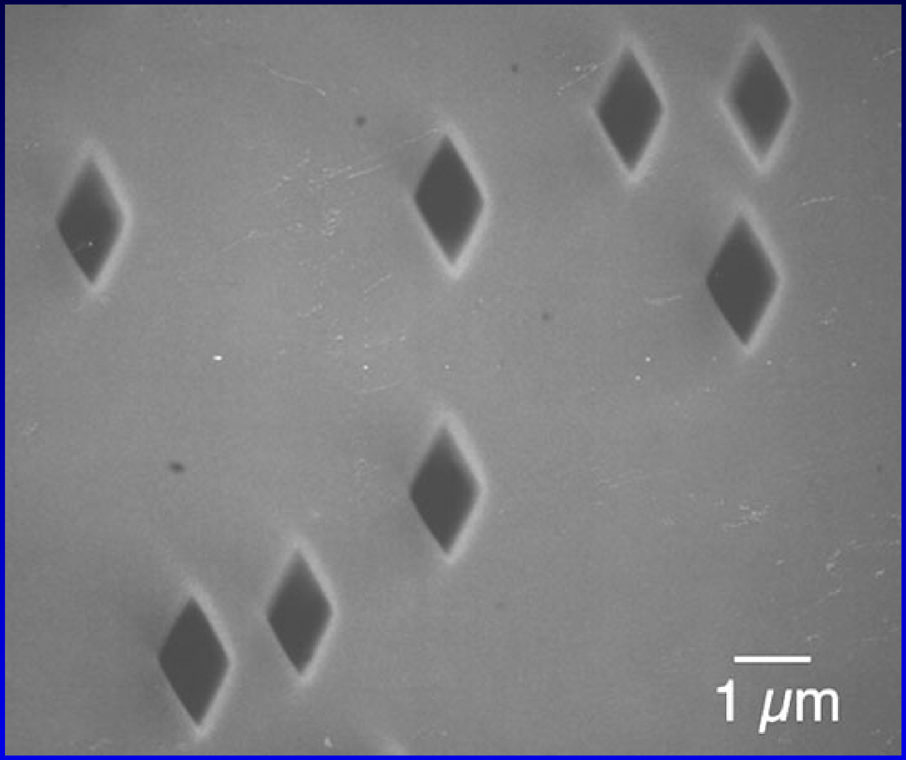
Debye Lecture 10

Nanoporus Templates for Nanofabrication

C.T. Black & C. B. Murray

Etched Ion Tracks in Mica



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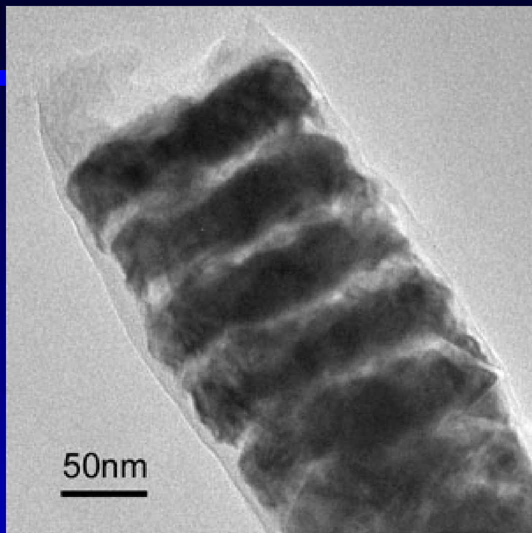
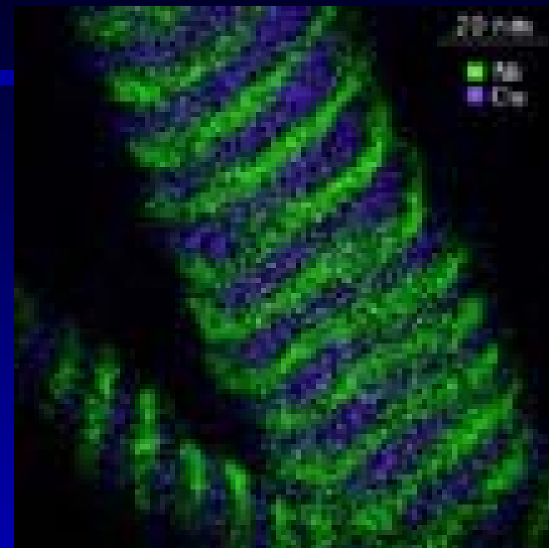
SEM image of etched particle tracks in single crystal mica. The pores are diamond in shape since the slowest etching planes are the oxygen terminated {110} planes



TEM image of a 120 nm diameter Cu/Ni multilayer nanowire with 20 nm Ni and 10 nm Cu layers



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EELS image of two 30 nm diameter Cu/Ni nanowires with 5 nm Ni and 5 nm Cu layers. <>

The pores are diamond shaped with a sharp size distribution, and are aligned with the in-plane crystalline axes of mica [*Appl. Phys. Lett.* **74**, 2803 (1999).]. [*J. Mater. Sci.***35**, 1097 (2000).].

APPLIED PHYSICS LETTERS VOLUME 72, NUMBER 10 9 MARCH 1998

Self-organized formation of hexagonal pore arrays in anodic alumina

O. Jessensky, F. Müller,[a)] and U. Gösele
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(Received 7 July 1997; accepted for publication 14 January 1998)

The conditions for the self-organized formation of ordered hexagonal structures in anodic alumina were investigated for both oxalic and sulfuric acid as an electrolyte. Highly ordered pore arrays were obtained for oxidation in both acids. The size of the ordered domains depends strongly on the anodizing voltage. This effect is correlated with a voltage dependence of the volume expansion of the aluminum during oxidation and the current efficiency for oxide formation. The resulting mechanical stress at the metal/oxide interface is proposed to cause repulsive forces between the neighboring pores which promote the formation of ordered hexagonal pore arrays. [S0003-6951(98)03510-4]

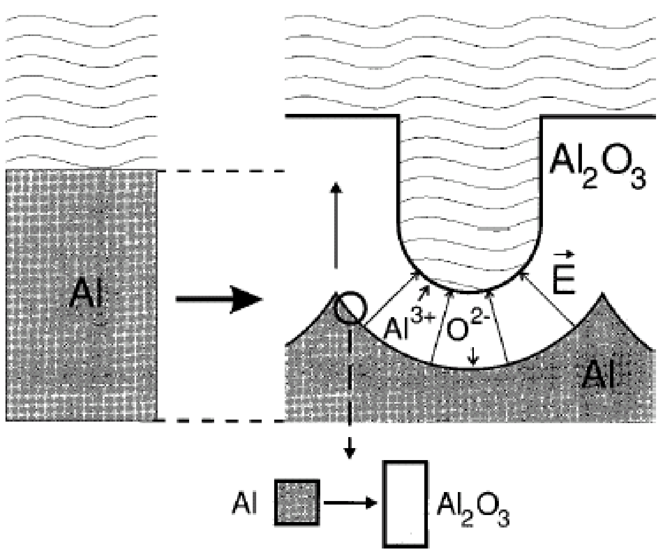


FIG. 1. Expansion of aluminum during anodic oxidation. On the left the level of the unoxidized metal surface is depicted.

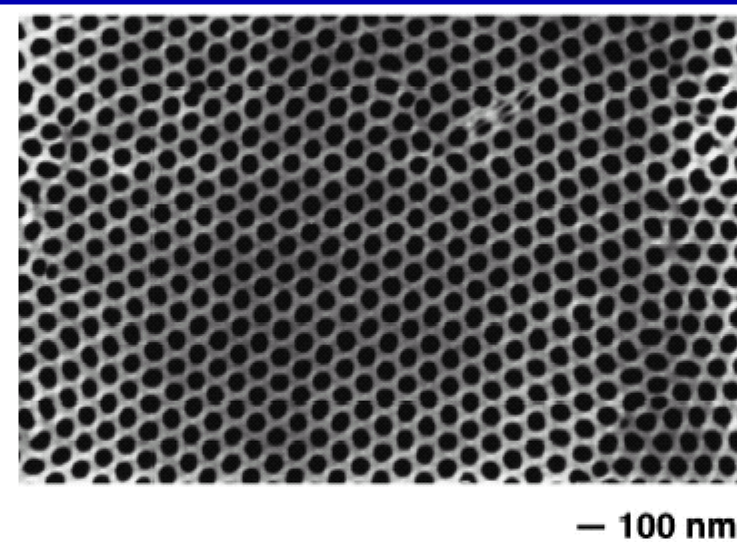
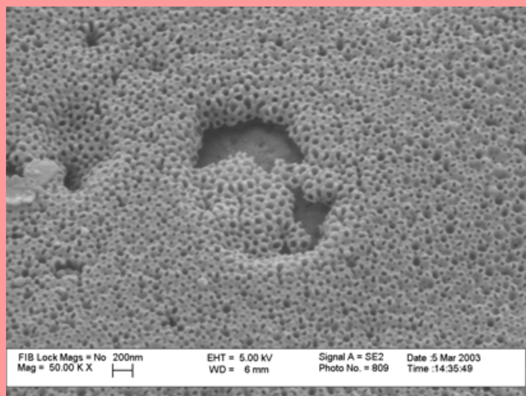
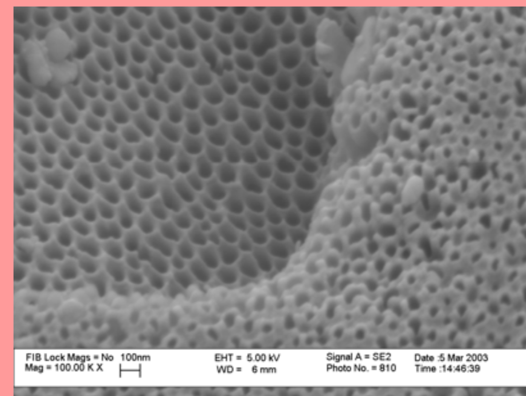
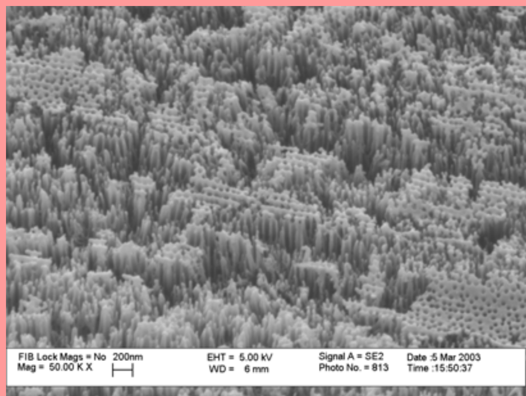


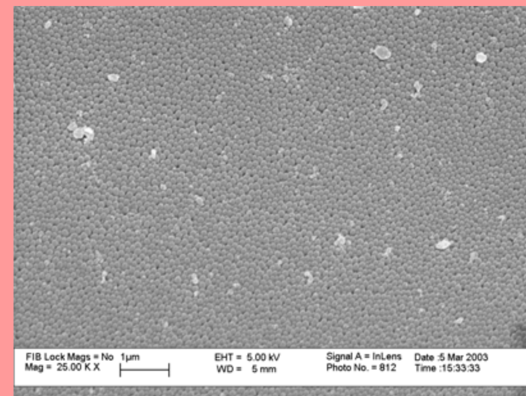
FIG. 2. SEM bottom view of a porous anodic Al_2O_3 layer with ordered hexagonal pore structure after opening the pore bottoms by chemical etching [40 V, 0.3 M $(COOH)_2$, 1 °C].

Anodic Porous Alumina Membranes









High-density ferromagnetic nanowire arrays obtained from ordered porous alumina templates

K. Nielsch, J. Barthel, F. Müller and R.B. Wehrspohn

in collaboration with

S.F. Fischer and H. Kronmüller, MPI für Metallforschung, Stuttgart

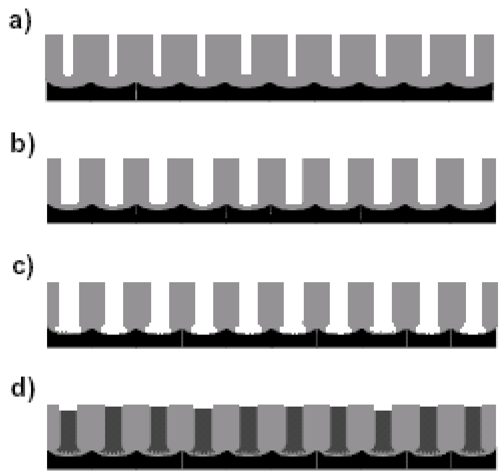


Fig. 1: Preparational steps for a highly ordered array of magnetic nanowires embedded in an alumina matrix.

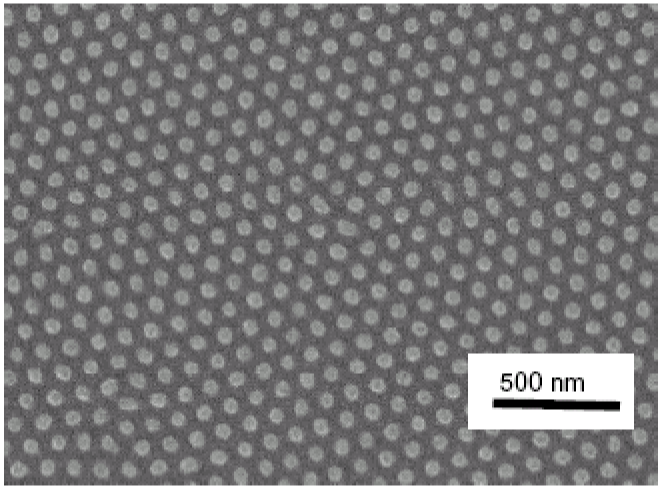


Fig. 2: SEM top-view image of a nickel filled alumina structure with a pitch of 100 nm. The diameter of the nickel columns is 35 nm.

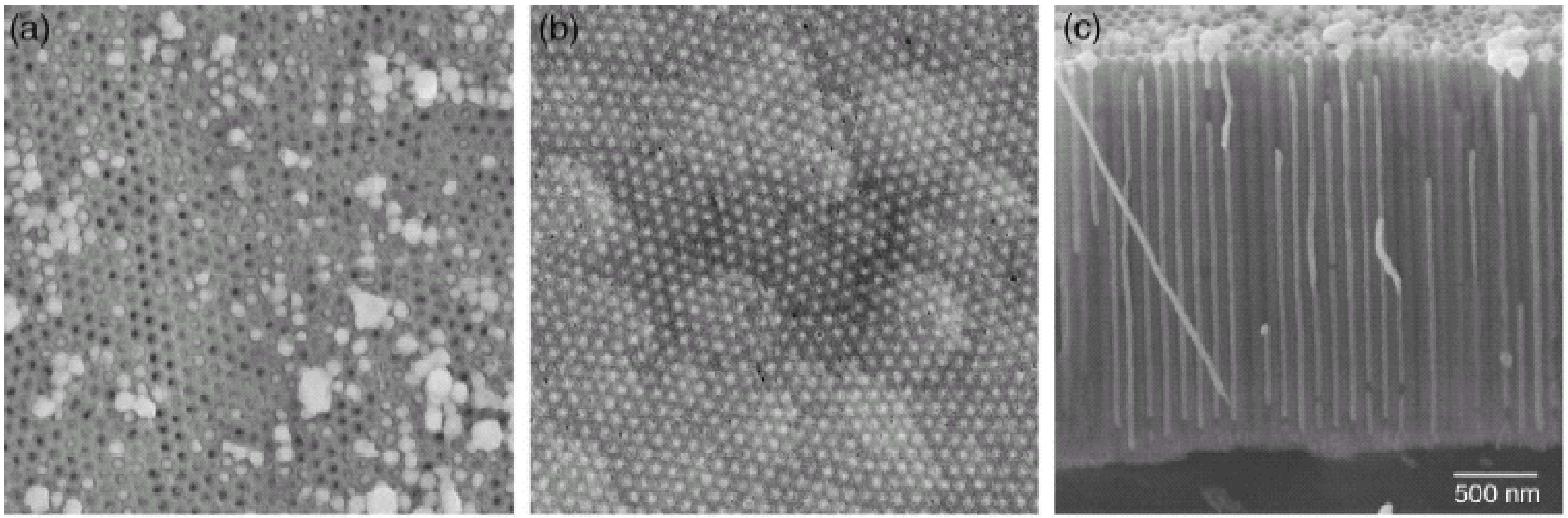


FIG. 4. SEM micrographs of a silver-filled alumina membrane. (a) Top view of an unthinned sample, (b) top view of the same sample approximately 200 nm underneath the initial surface, and (c) side view of a fracture.

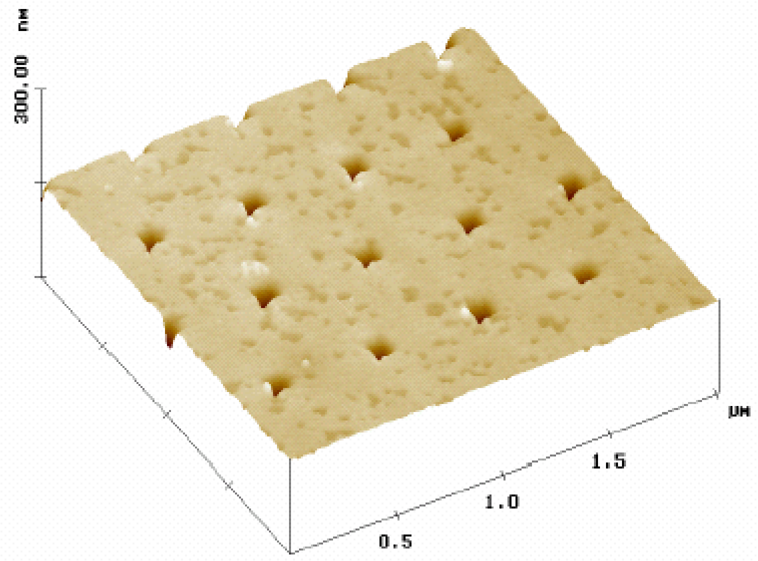


Figure 2 AFM image of inverse pyramidal holes in the surface of electropolished aluminum after imprint under 5 kN/cm^2.

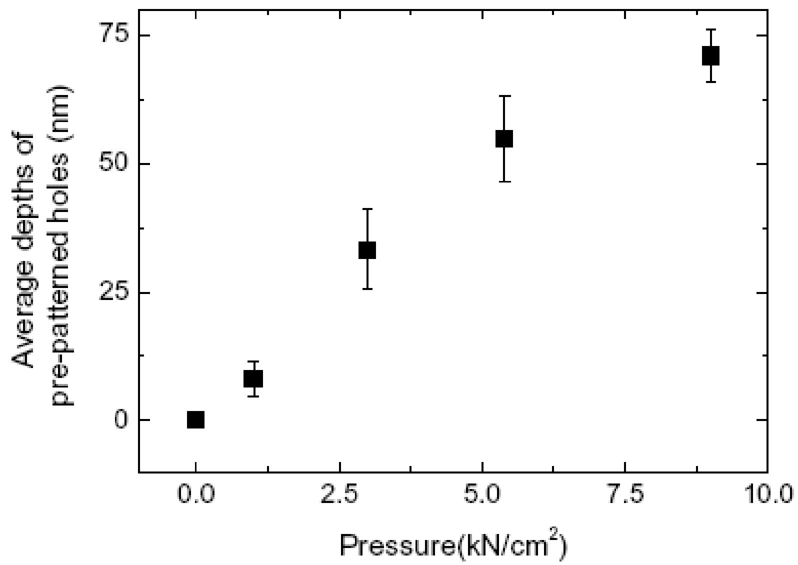


Figure 3 The relationship between imprint pressure and average depths of pre-patterned holes in the surface of aluminum.

Large-area porous alumina photonic crystals via imprint method

J. Choi, J. Schilling, K. Nielsch, R. Hillebrand, M. Reiche, R. B. Wehrspohn,

U. Gösele

Max–Planck–Institute of Microstructure Physics, Weinberg 2, 06120 Halle, Germany

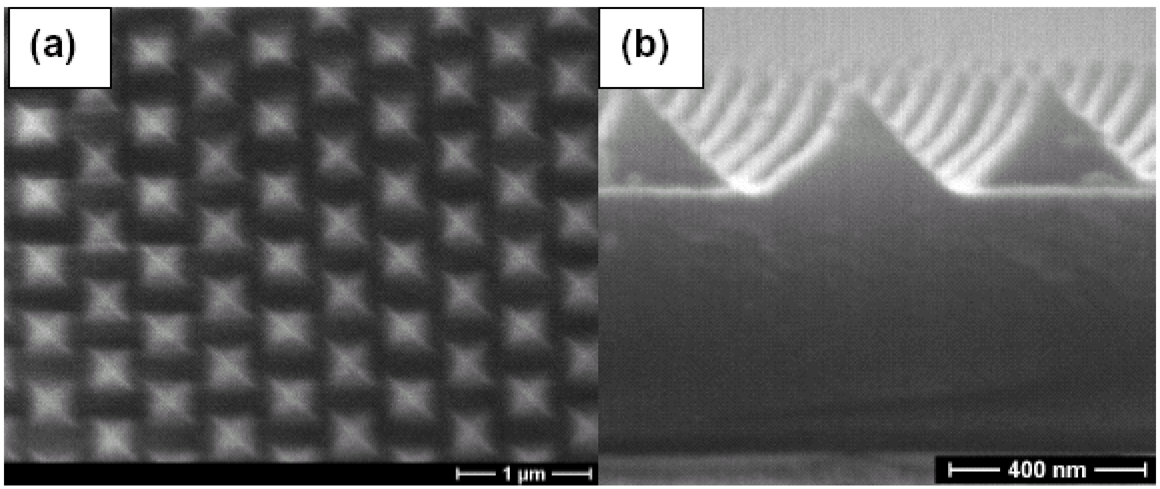


Figure 1 SEM images of a novel imprint stamp consisting of pyramids with 500 nm lattice constant and 260 nm height. (a) top view and (b) side view

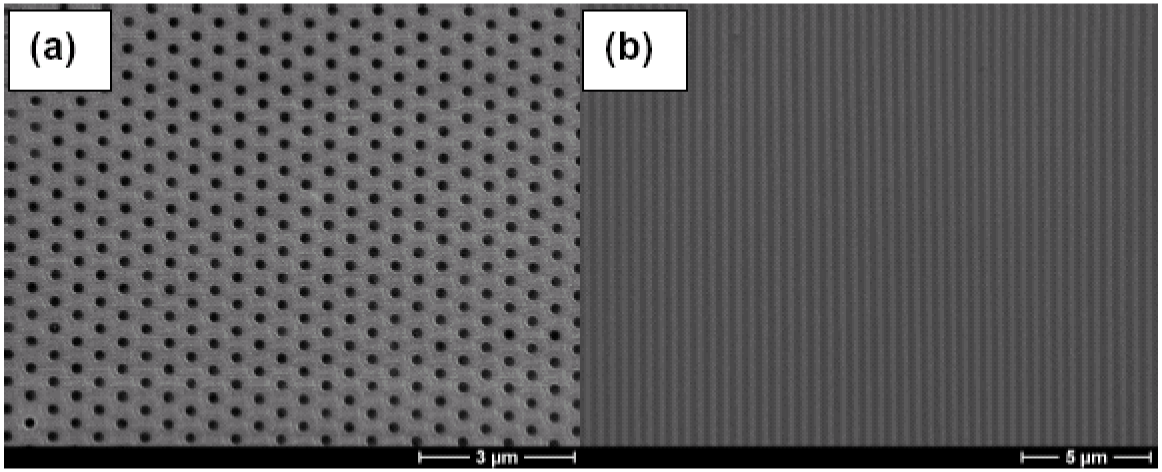


Figure 4 SEM images of a mono-domain porous alumina fabricated by anodization of pre-patterned aluminum. (a) top view and (b) side view

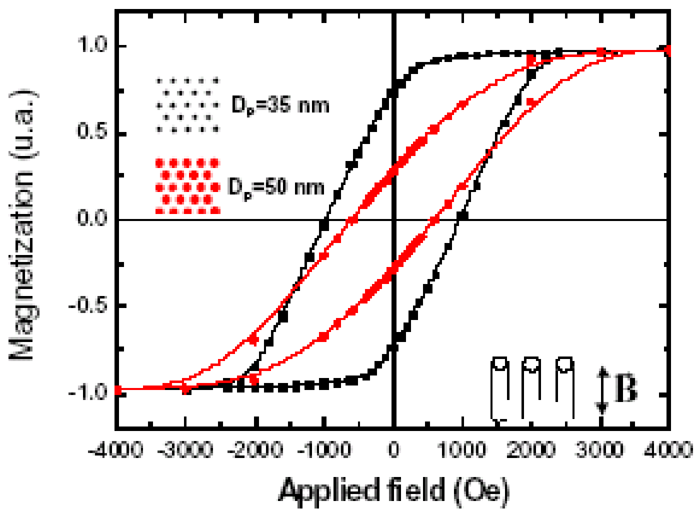


Fig. 3: SQUID hysteresis loops for two hexagonally ordered Ni nanowire arrays (100 nm pitch) with a pore diameter of 35 nm and 50 nm measured at 300 K.

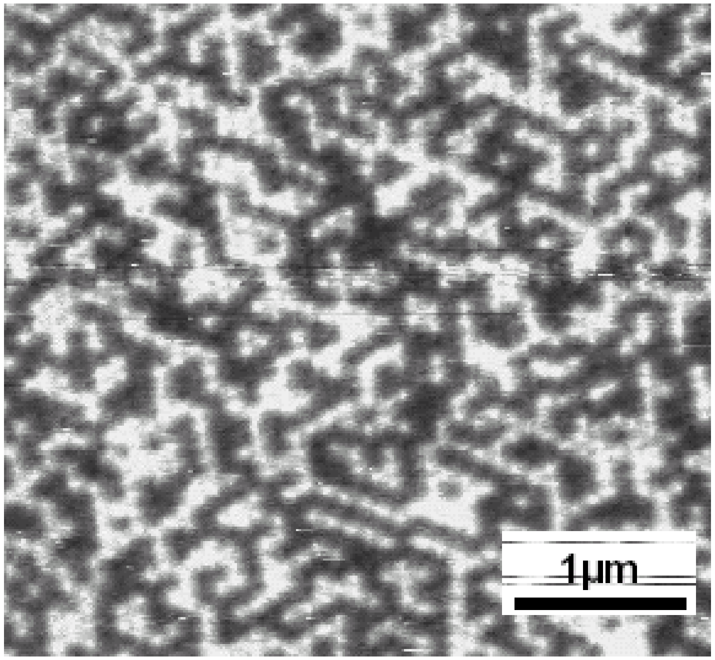


Fig. 4: MFM-image of an Nickel nanowire array with a pitch of 100 nm.

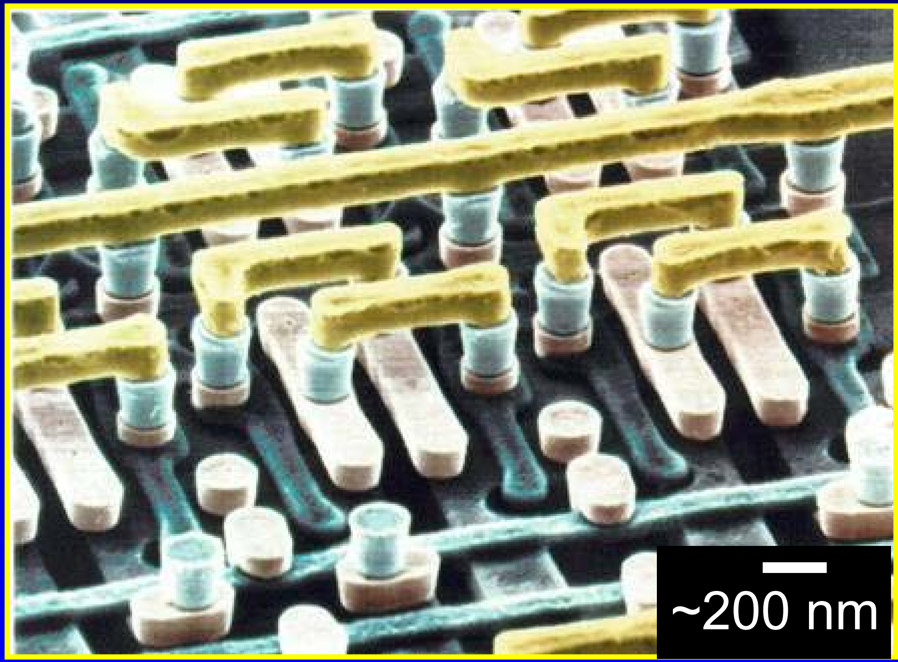
Chuck Black
IBM Research
Kathryn Guarini, Ying Zhang, Craig Hawker, Bob Sandstrom,
Odile Bezencenet, Julie Casperson

Application of diblock copolymer thin film self assembly to semiconductor electronics

:

motivation: integrated circuit fabrication

- complex patterning at lithographic resolution limits
- many (> 30) mask levels to define devices & interconnects
- iterative processing (deposition, lithography, RIE, anneal…, repeat….)



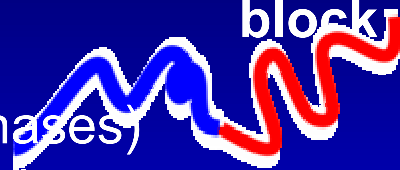
ideas: can self assembly reduce the difficulty of any IC fabrication steps?
can self assembly enable fabrication of increasingly-complex ICs?

diblock copolymer thin films

meet requirements for integration with semiconductor processing:
(material compatibility, batch wafer processing, cover large wafer areas)

we use cylindrical-phase PS:PMMA (70:30), M_n~64kg/mol

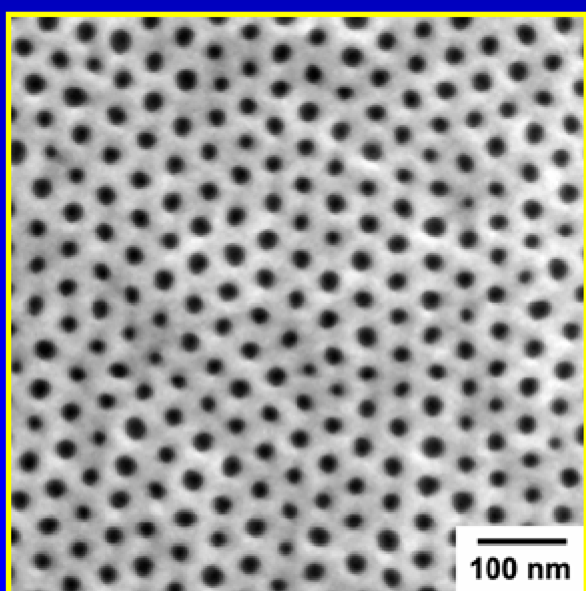
block A: polystyrene (PS)



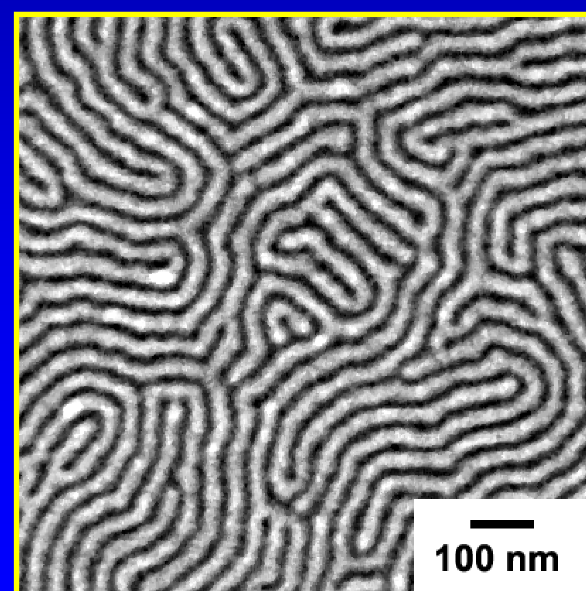
block B: PMMA

other possibilities (spherical, lamellar phases)
with lots of great research demonstrations

perpendicular cylinder domains



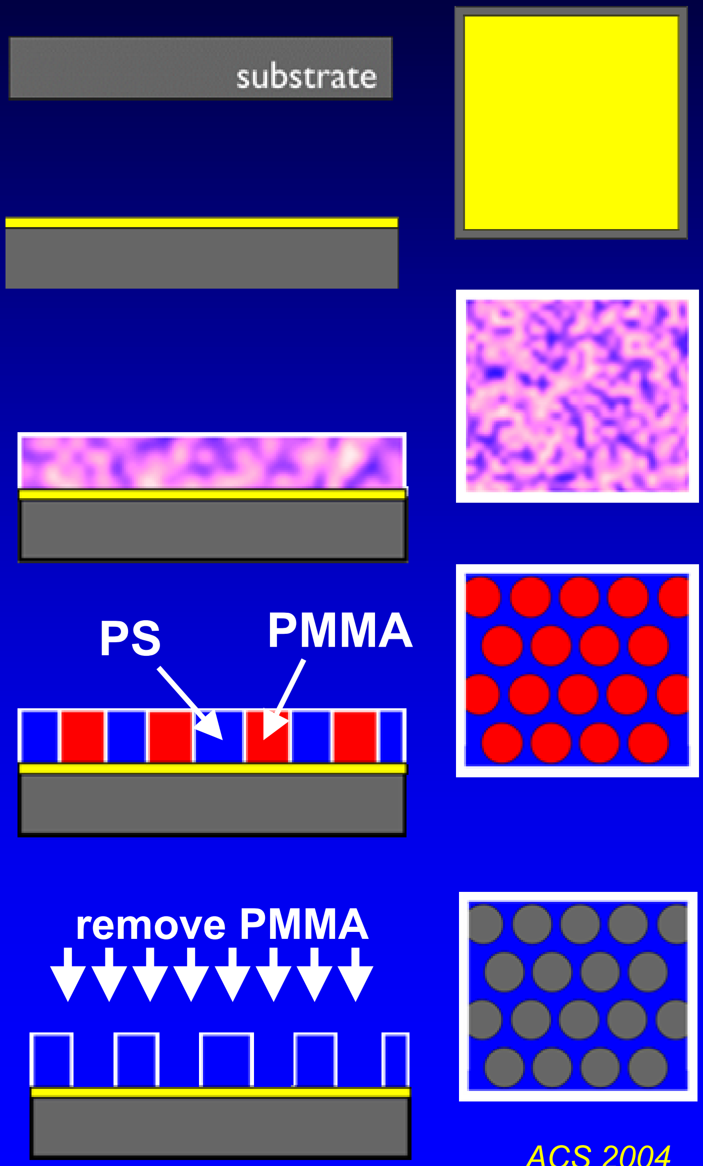
parallel cylinder domains



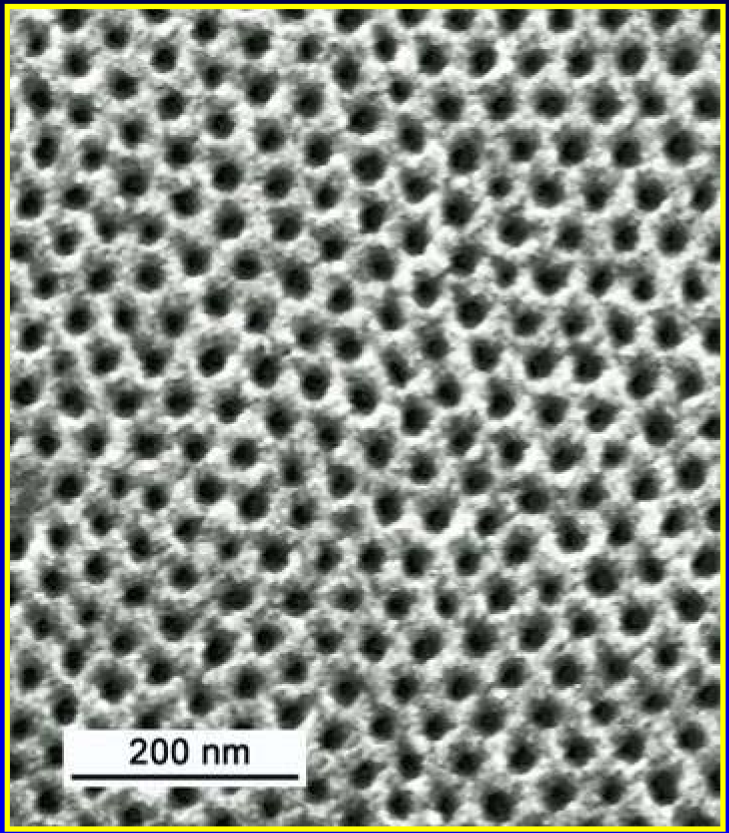
assembling the copolymer template

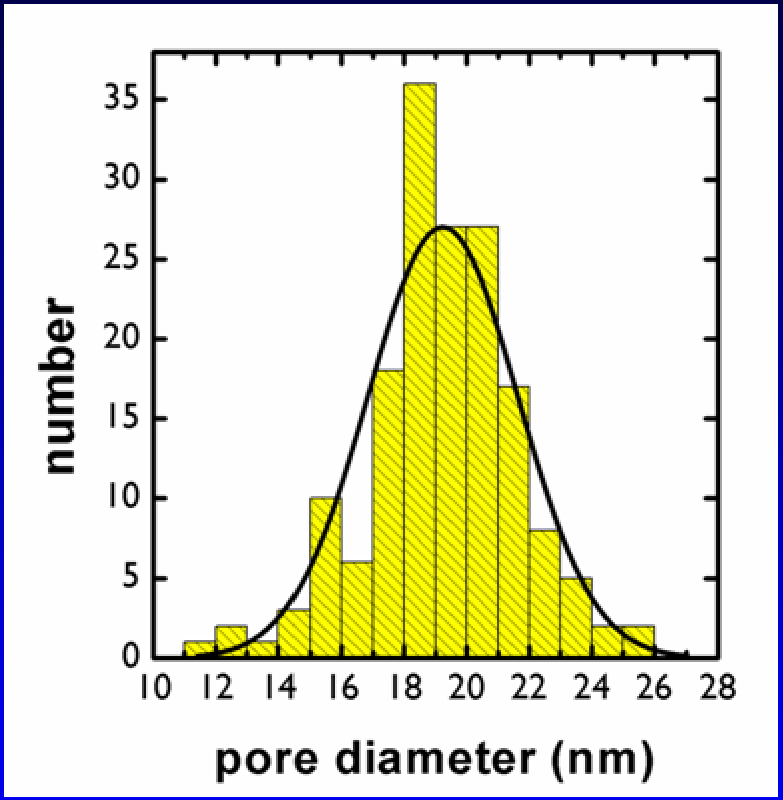
T.P. Russell (Umass Amherst), C.J. Hawker (IBM) *Adv. Mat.*, 12, 787 (2000).

1. apply random copolymer
   (spin casting + bake)
2. apply copolymer film
   (spin casting)
3. bake in oven (self assembly)
4. remove PMMA block with solvent



completed polymer template



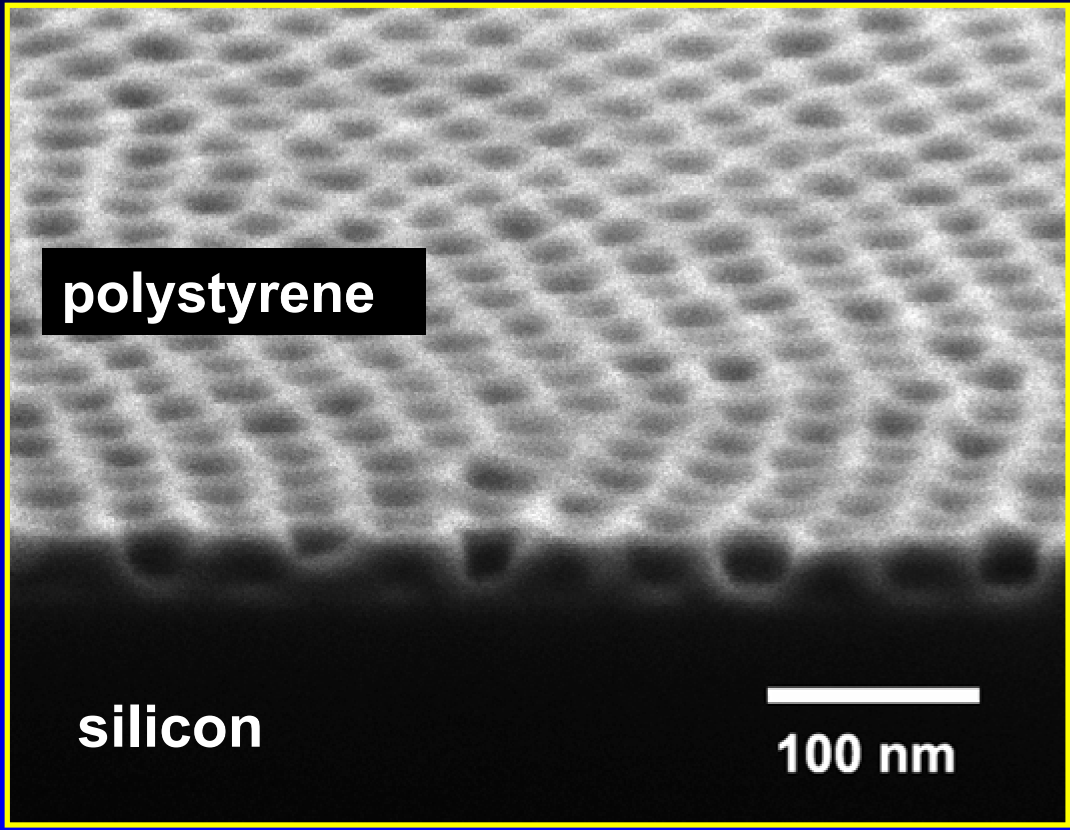


process generates dense arrays of hexagonally-packed **20-nm-diameter** cylindrical pores with **10% size uniformity** in a **40-nm-thick** film

ACS 2004

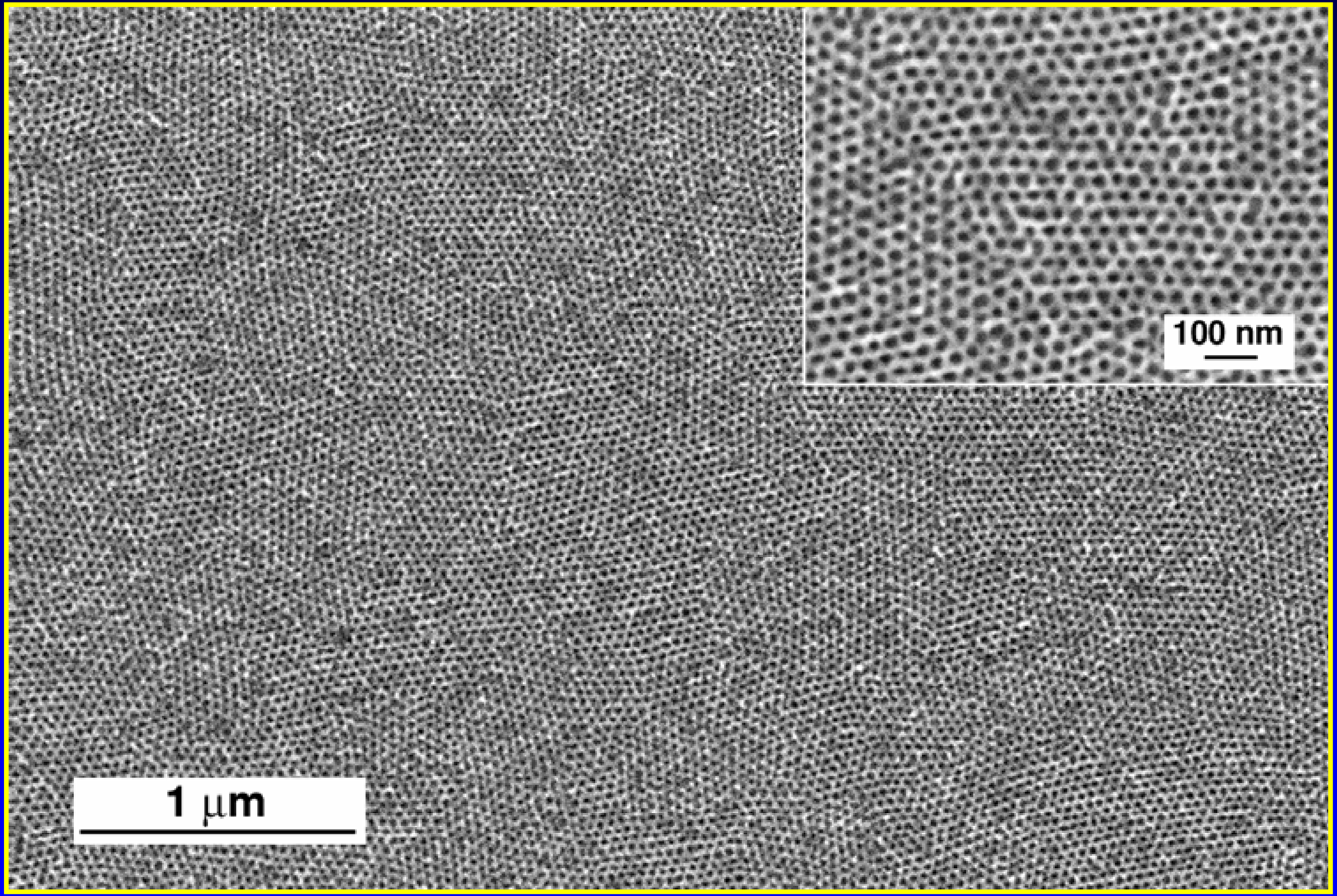
IBM

completed polymer template



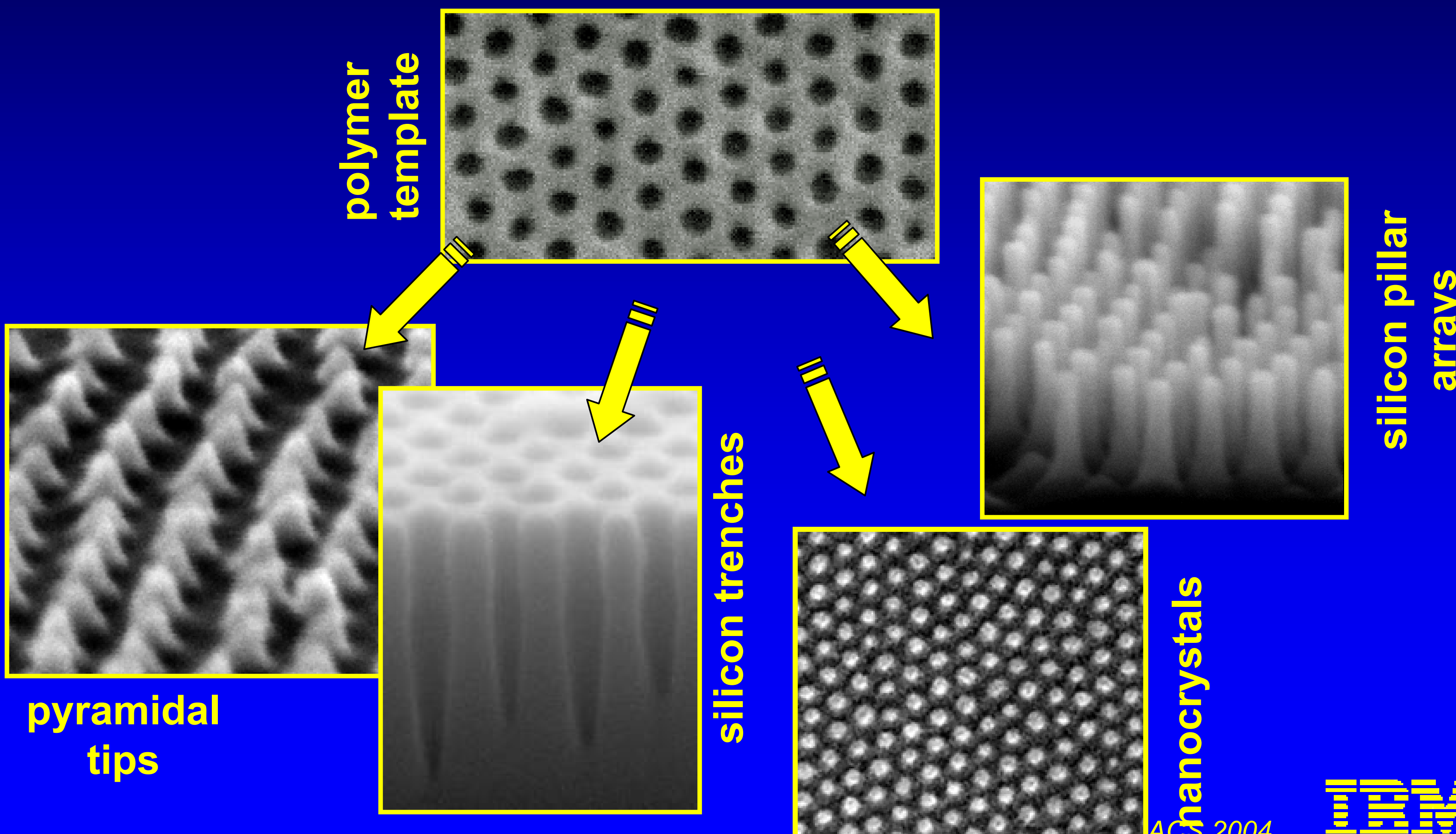
liquid develop removes PMMA, creating porous PS template

template formed over 200 mm silicon wafers



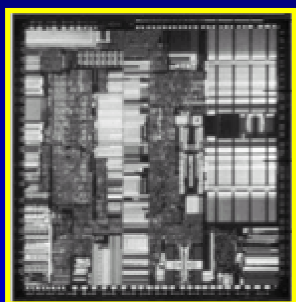
semiconductor processing for microelectronics

goal: integrate nanometer-scale self assembly with semiconductor processing for application to microelectronics



onchip decoupling capacitors

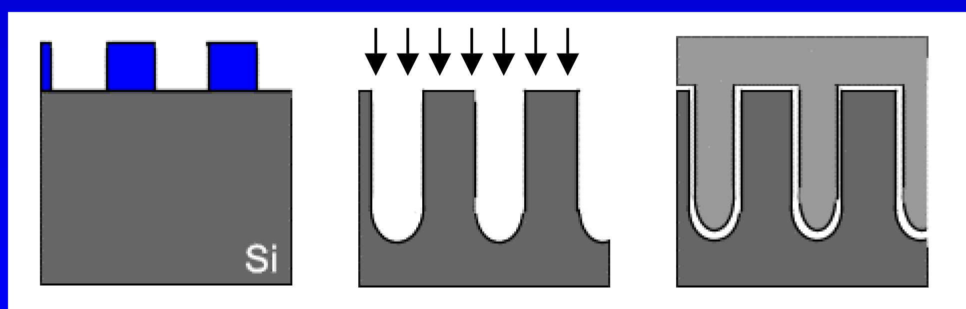
- **high-end microprocessors require on-chip power supply decoupling capacitors**
- **need C_{decap}~0.5 μF while occupying minimal on-chip area**



- **to fit in <5% chip area requires C_{decap} >2.5 μF/cm²**
- **for planar capacitors:**

  14 Å SiO_2 (ε~4)
  35 Å Al_2O_3 (ε~10)
  70 Å HfO_2 (ε~20)

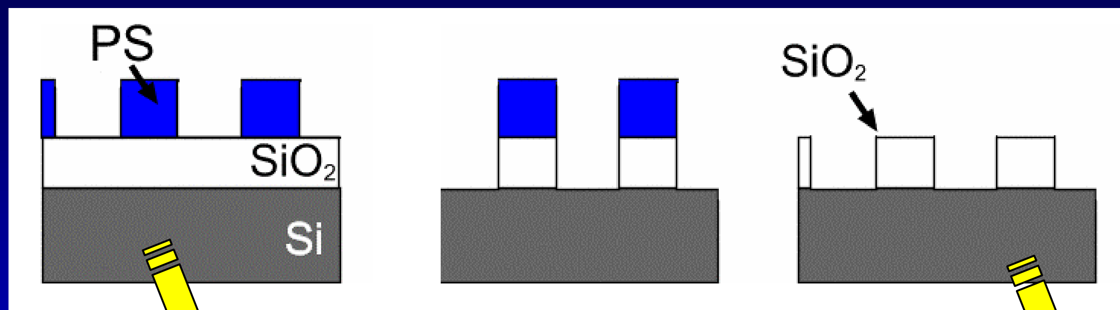
our approach: increase lateral capacitance density via *surface area*

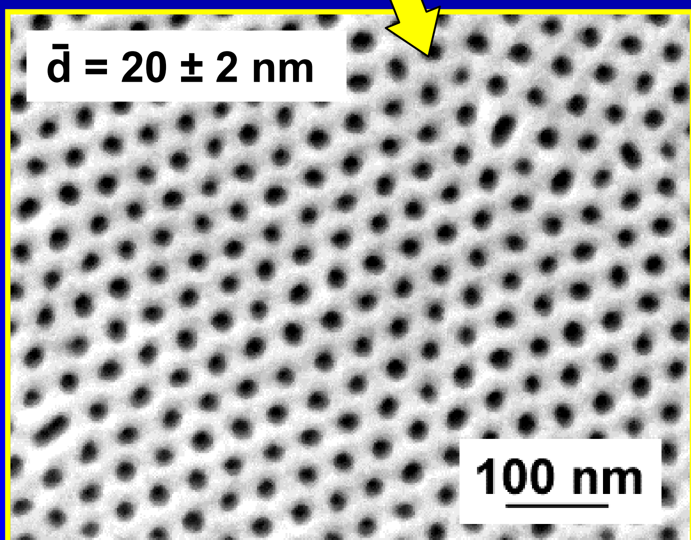


advantages: no new materials integration; compatible with thin SOI; minimal added complexity

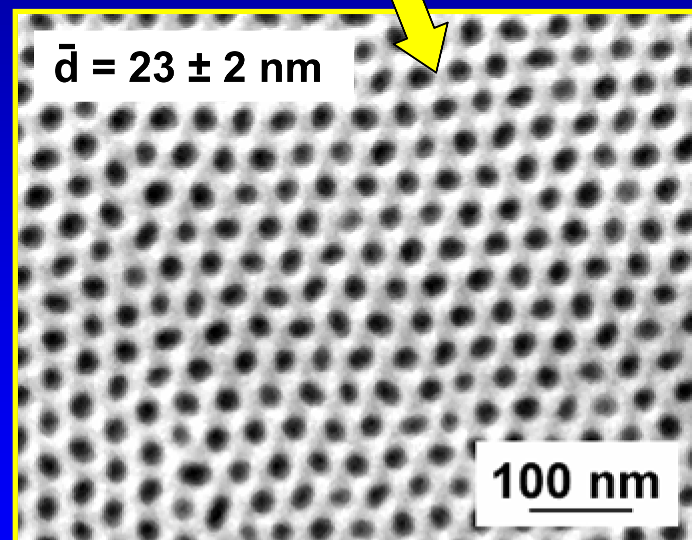
pattern transfer into dielectric films

goal: transfer polymer pattern into underlying oxide hardmask





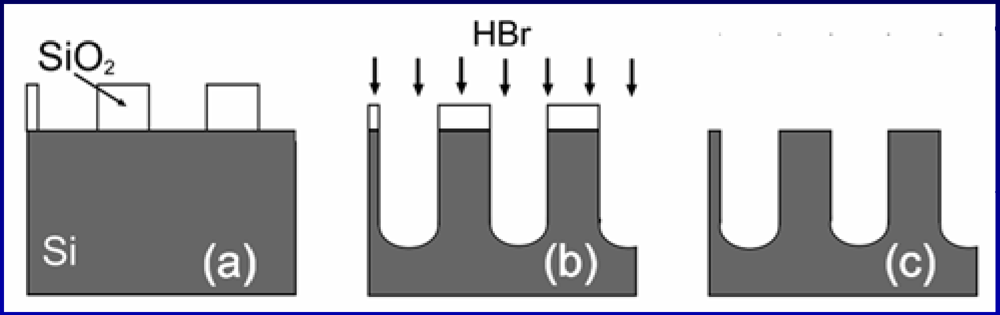
polymer pattern formed on 20 nm SiO_2 on Si

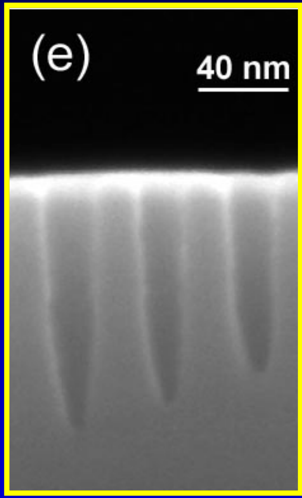


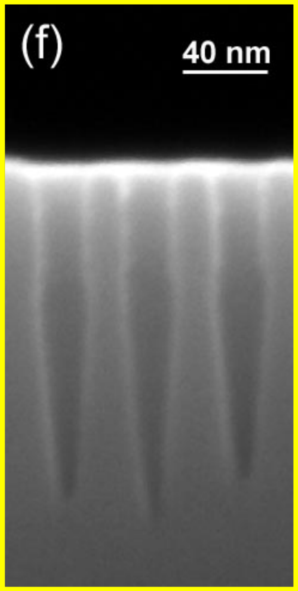
polymer pattern reproduced in SiO_2

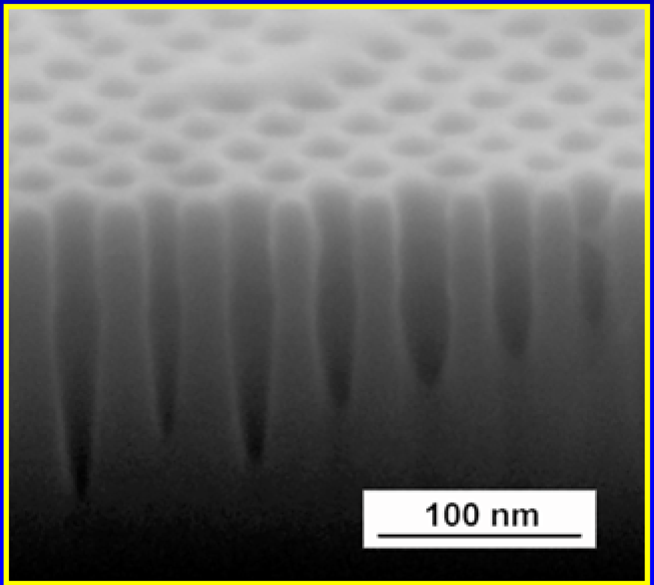
high-aspect-ratio silicon trenches

oxide hardmask facilitates high-aspect ratio etching





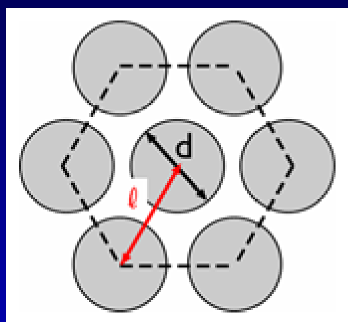




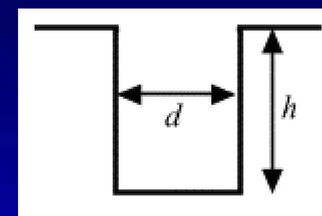
- trench depth (i.e. surface area increase) determined by etch time
- achieved up to 10:1 aspect ratio with 20 nm oxide hardmask

surface area enhancement

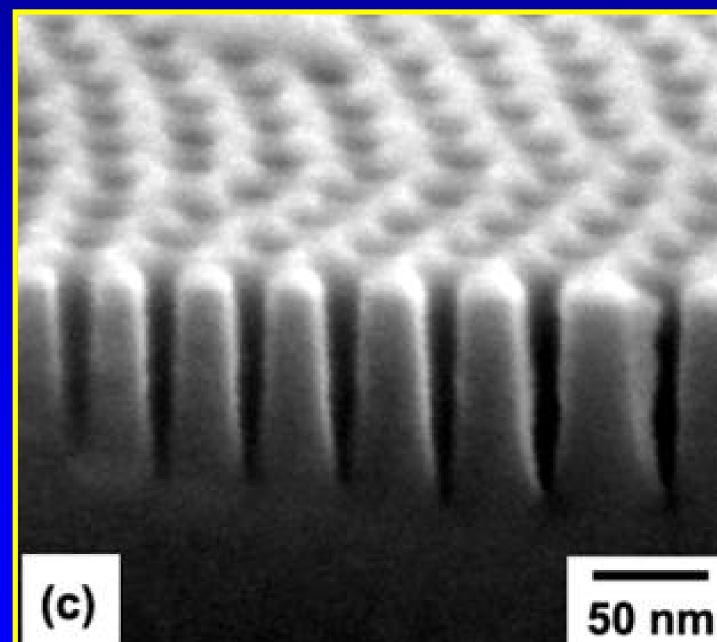
high aspect ratio pores result in significant surface area increases



$$A_{patterned} = A_{planar}\left[1 + \frac{\pi a}{\sin(60)}\left(\frac{d}{\bullet}\right)^2\right]$$

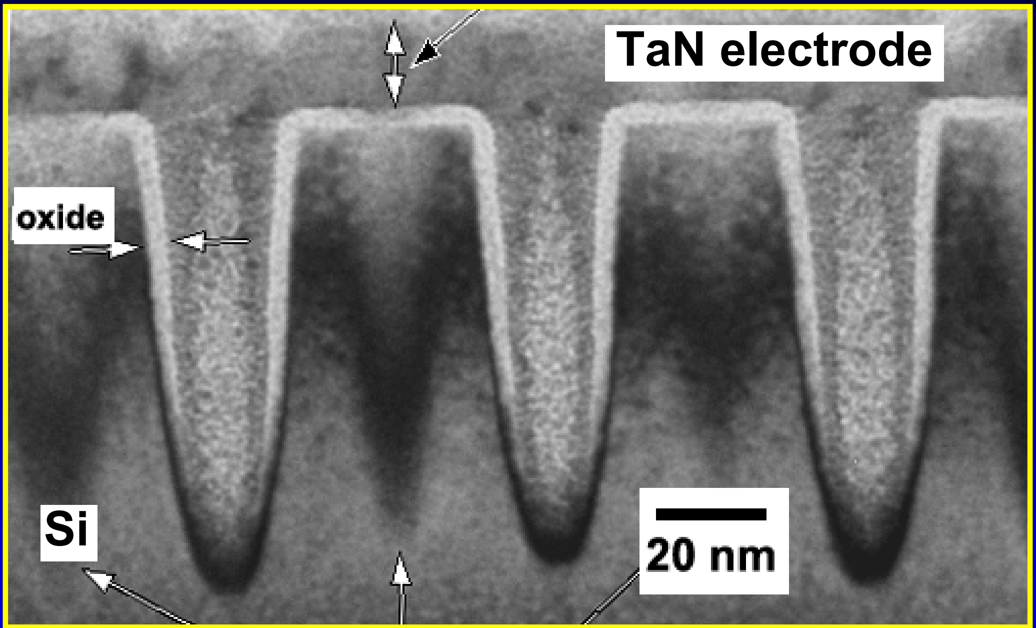


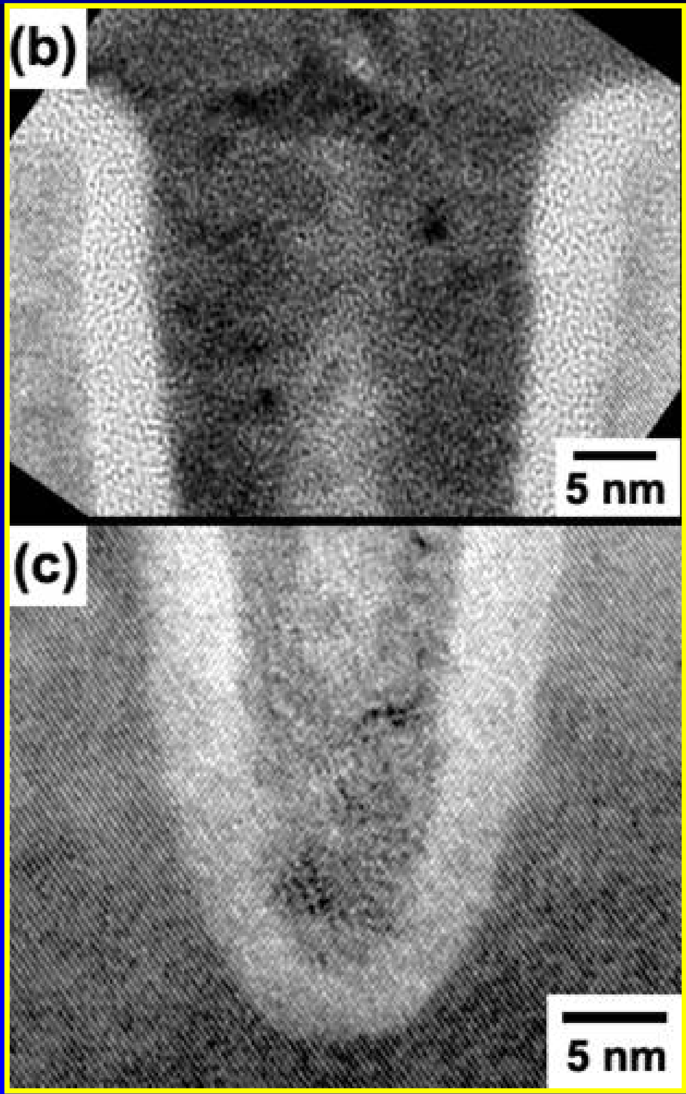
pore aspect ratio (a=h/d)	surface area enhancement
0.5:1	141%
1:1	182%
5:1	510%
10:1	920%



estimates for:
- 20 nm pores, 42 nm spacing
- 4 nm oxide thickness

on-chip MOS decoupling capacitors

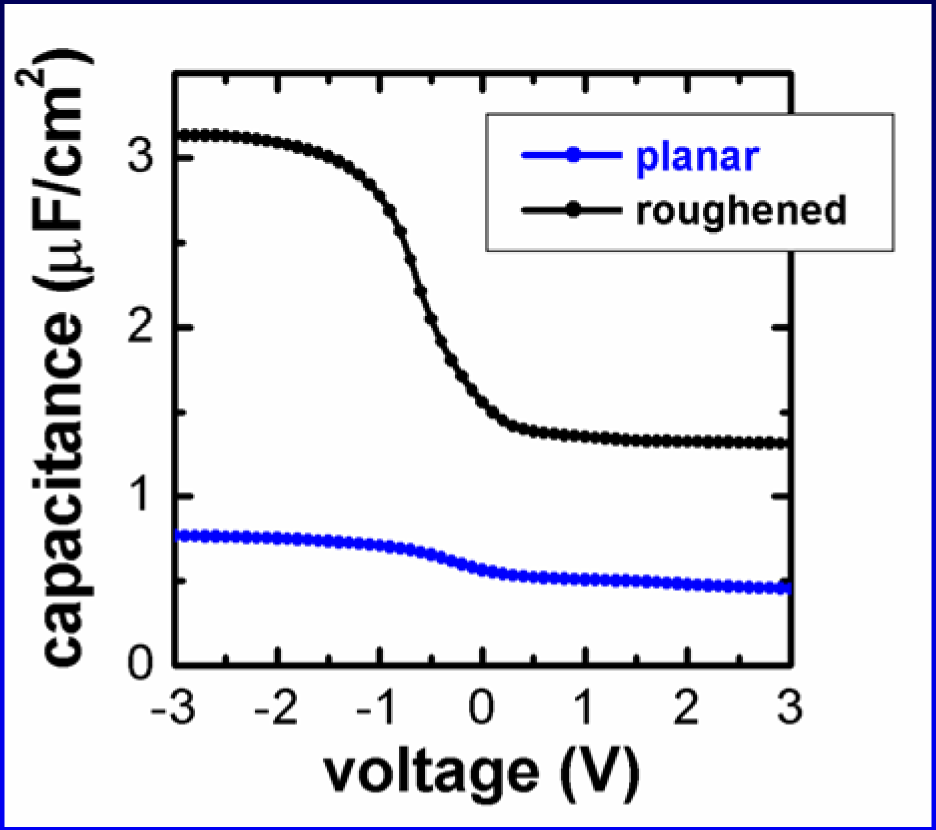




atomic-layer-deposition (ALD) conformally fills narrow trenches

C. T. Black, K. W. Guarini et al. *IEEE Elect. Dev. Lett*. (submitted).

on-chip MOS decoupling capacitors



in accumulation:

$$\frac{C_{patt}}{C_{planar}} = 4.1x$$

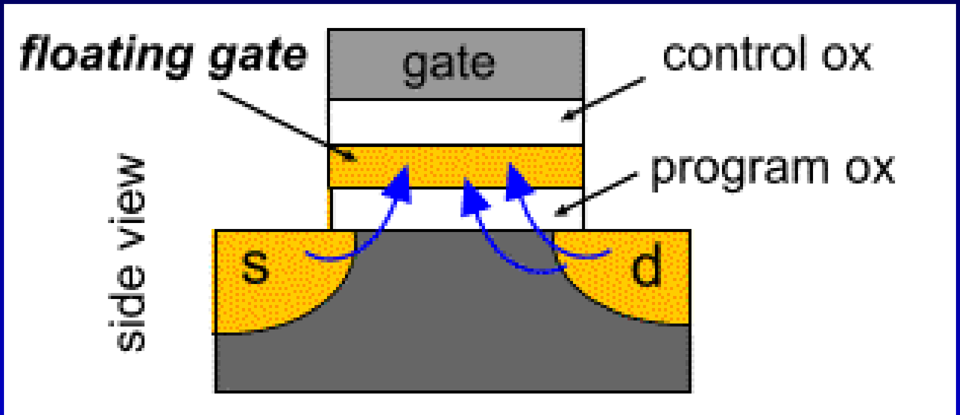
$$C_{patt} = 3.13\ \mu\text{F/cm}^2$$

equivalent to planar capacitor with ε~16 (HfO_2)

- capacitance enhancement correlates with device geometry
- no new dielectric integration required; minimal process complexity

nonvolatile FLASH memory

FLASH memory is compact (1 transistor per memory bit)

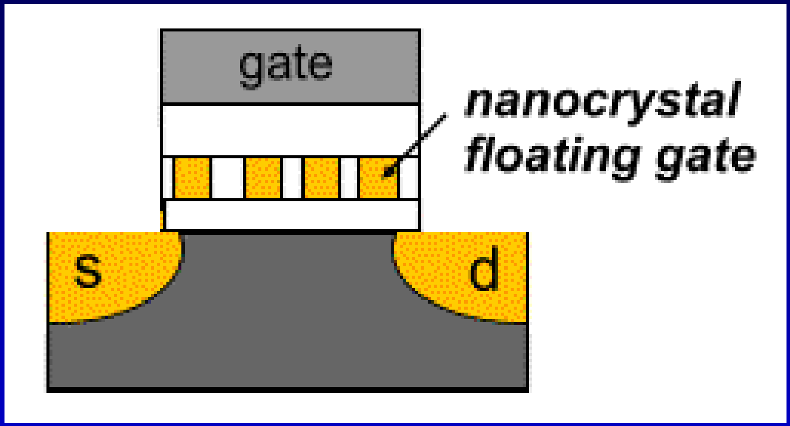


programming FG with charge shifts transistor V_T

- **FLASH has established itself in the nonvolatile memory market (used in cellular phones and digital cameras)**
- **drawbacks: high power (12-15V operation), slow, low-cyclability**
- **increasing difficulty in scaling device to smaller dimensions**

why nanocrystal FLASH?

replacing FG with layer of nanocrystals may help device scaling

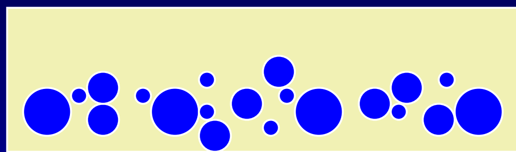


Potential advantages of nanocrystal memories compared to standard FLASH:

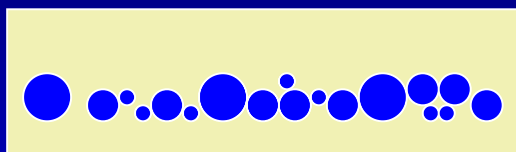
- improved scalability, retention, & cyclability
- lower voltage operation

methods of fabricating nanocrystals

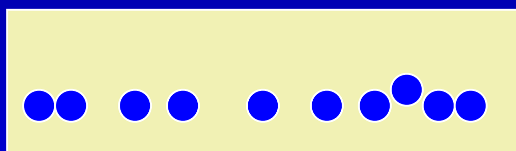
challenge: how to pattern FG at sub-lithographic dimensions?



ion implantation

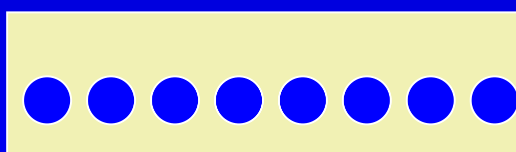


chemical vapor deposition (CVD)



aerosol deposition

our idea:

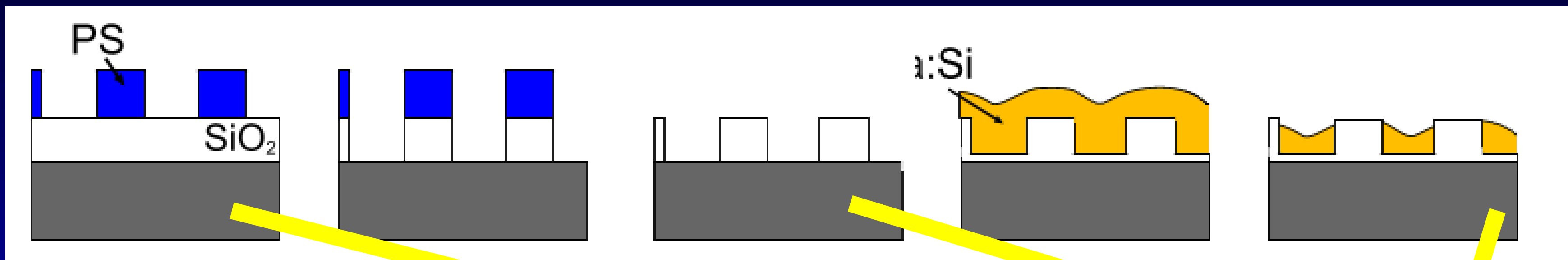


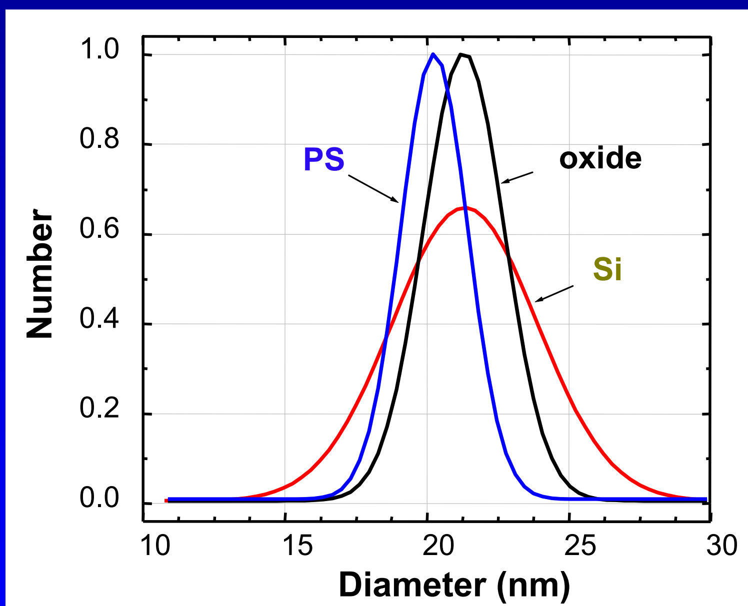
templated self assembly

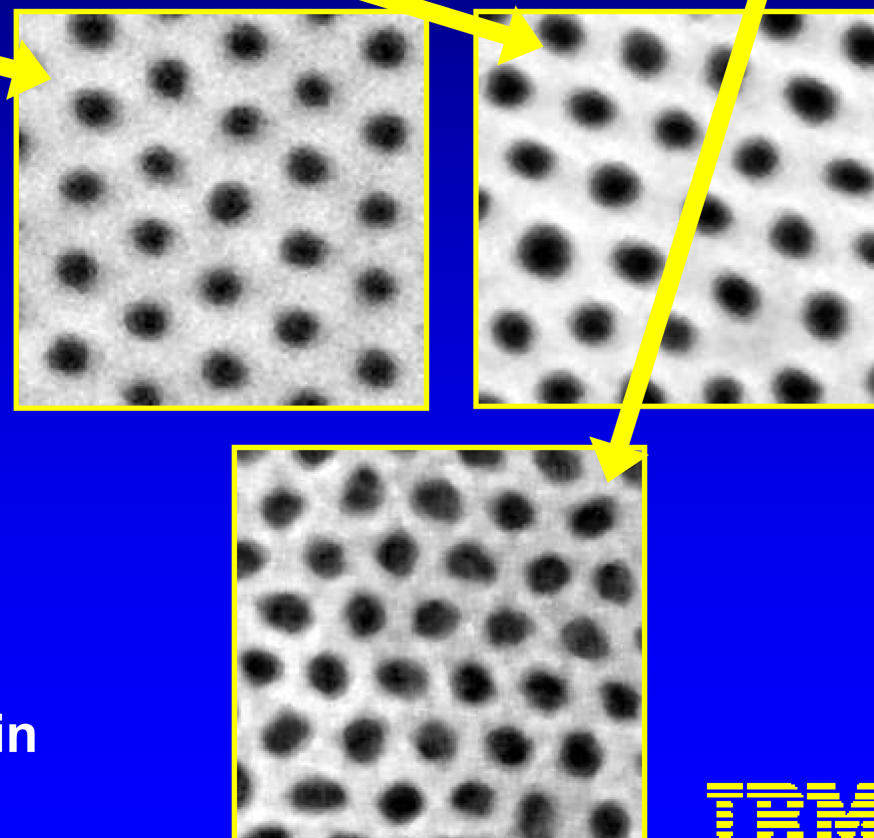
advantages:

- **precise definition of tunnel barrier**
- **well defined nanocrystal sizes**
- **constant nanocrystal density**

formation of embedded nanocrystal arrays

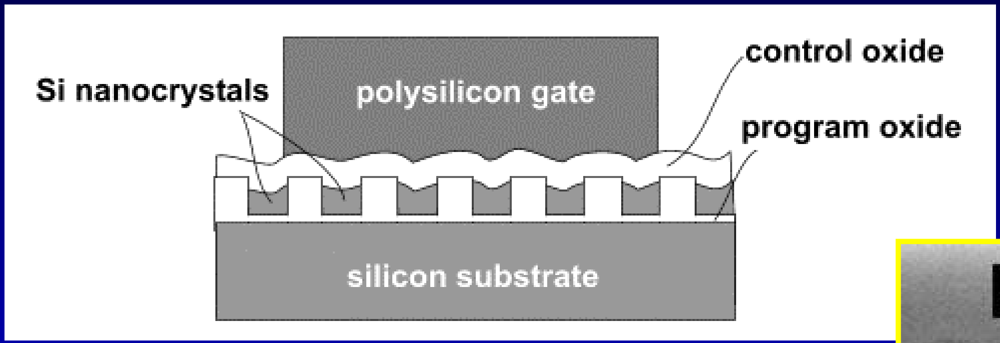


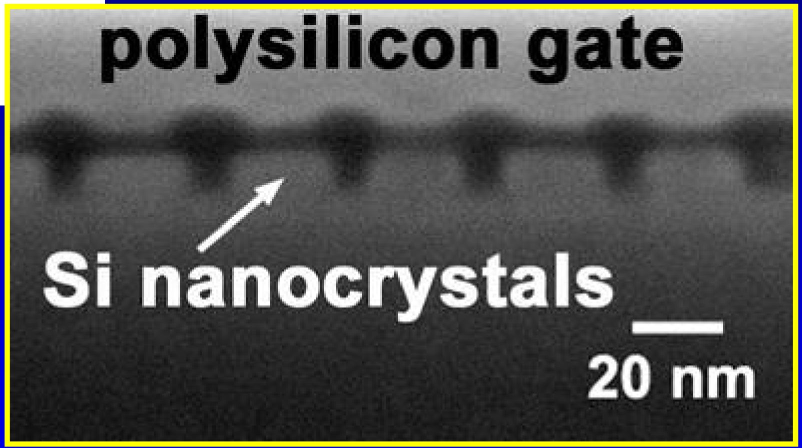




pattern transfer processes maintain
original template uniformity

nanocrystal FLASH capacitors





MOS capacitors fabricated with:

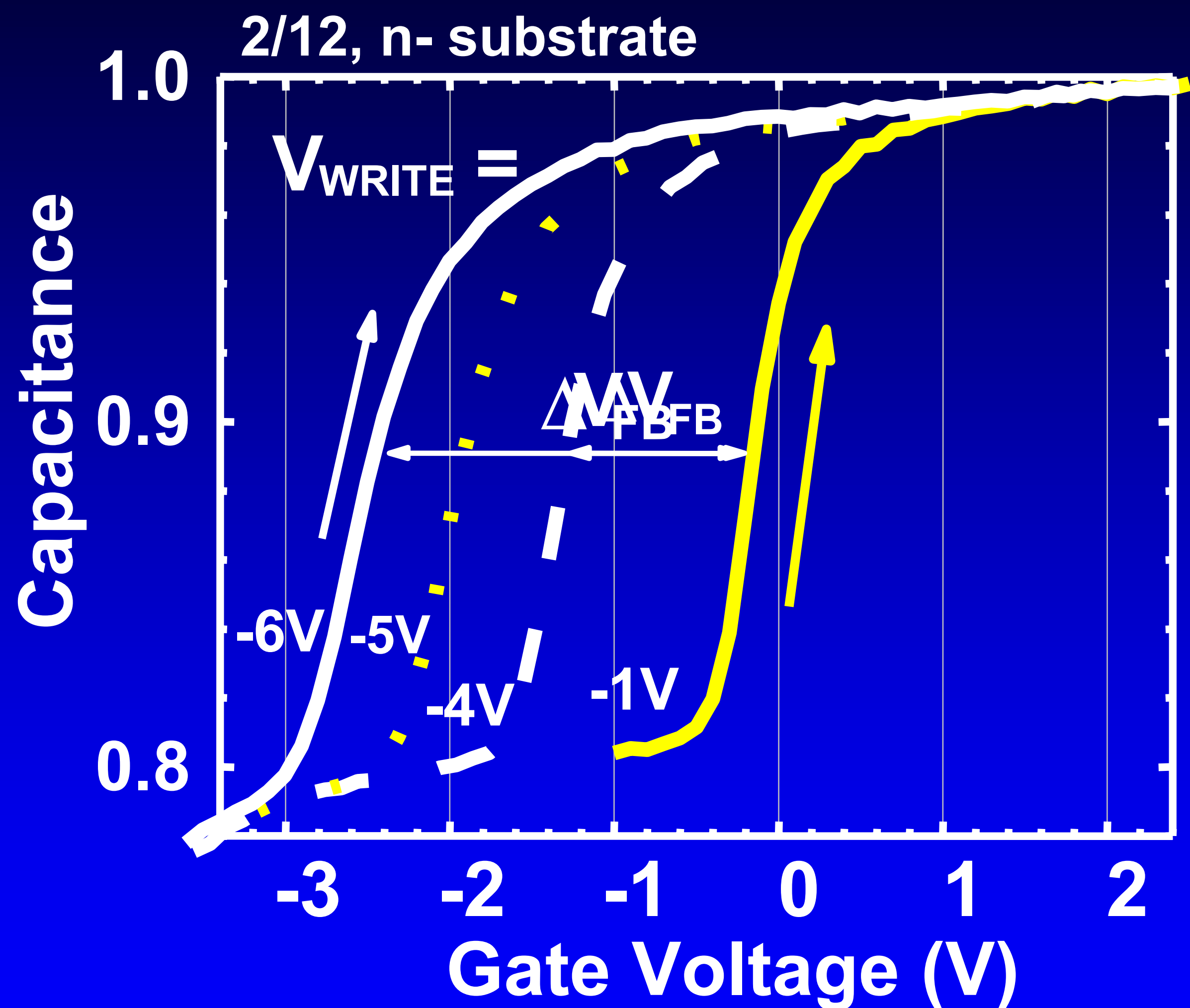
program oxide thickness: 2 and 3 nm

control oxide thickness: 7 and 12 nm

(Intel 64 MB flash: prog ox: 9nm, ctl ox: 15 nm (electrical thickness))

K. W. Guarini, C. T. Black et al. *IEDM Tech. Dig.* (2003).

nanocrystal FLASH capacitors

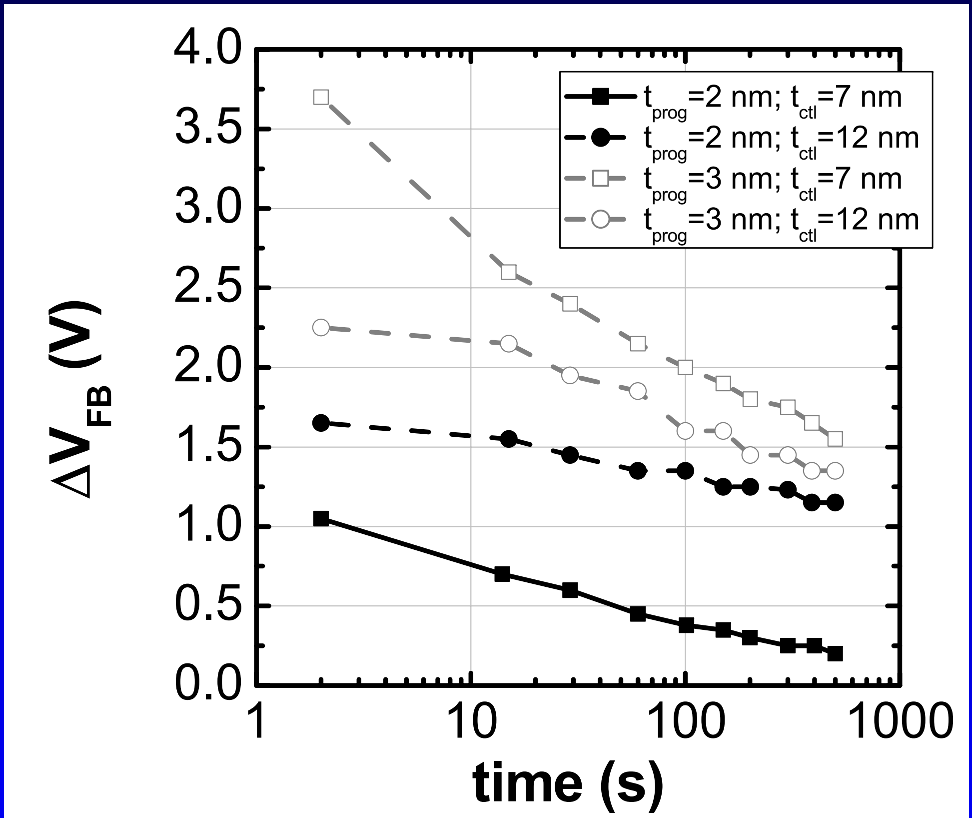


low-V operation due to thin prog & ctl oxides

-V sweep from inversion to accumulation

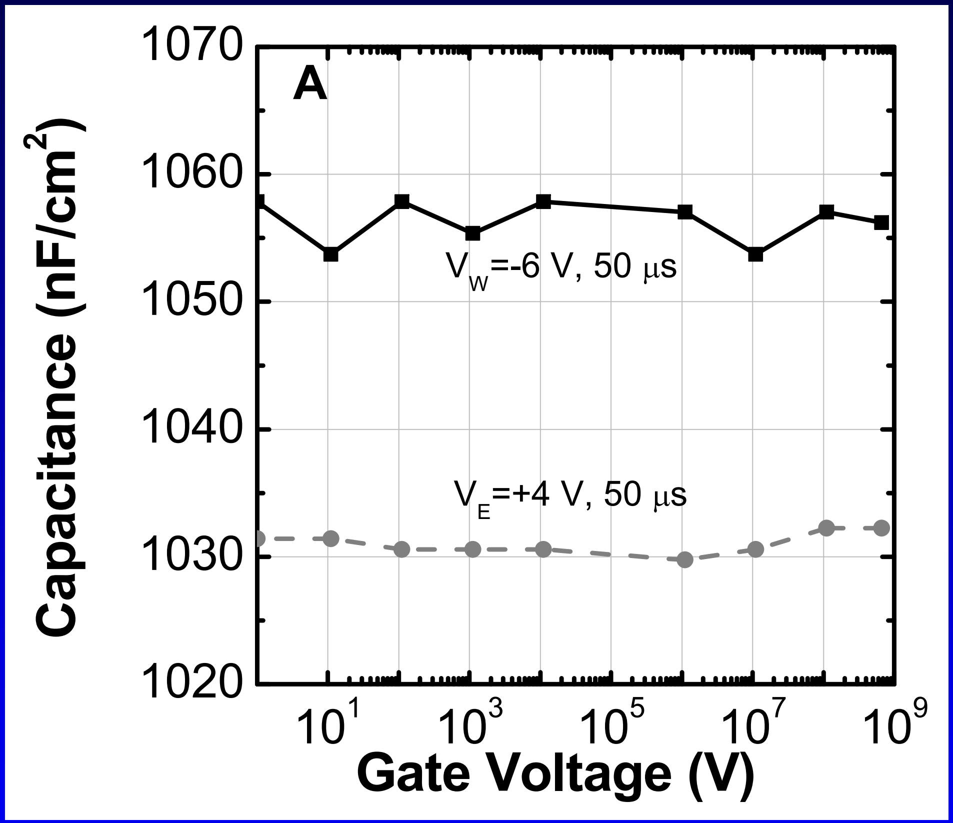
Charge injected into nanocrystals shifts device flat band voltage, ΔV_{FB}

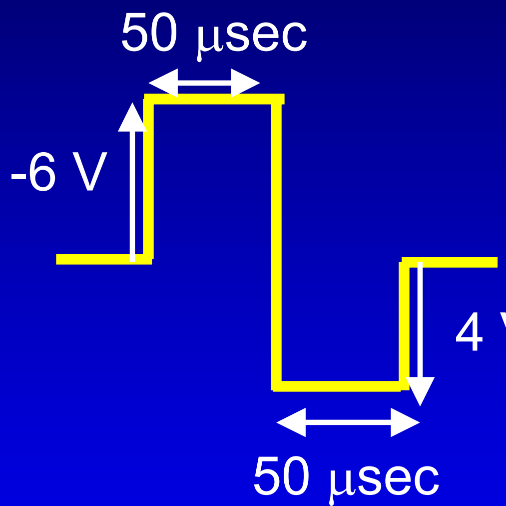
memory retention time



- all devices show:
  ΔV_{FB} ~ const. – k*ln(t)
- logarithmic fit projects retention time >10^6 s for t_{prog}=2 nm
- time constants do not obviously scale with t_{prog}

memory endurance





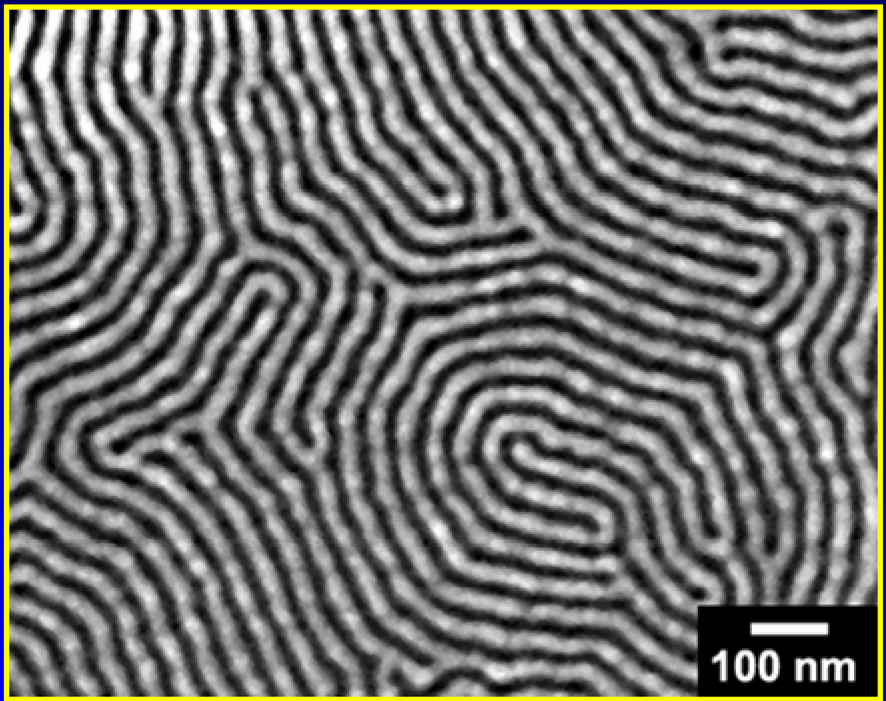
- commercial FLASH cycles 10^8 times before failing
- our nanocrystal FLASH is cyclable $>10^9$ times without degradation

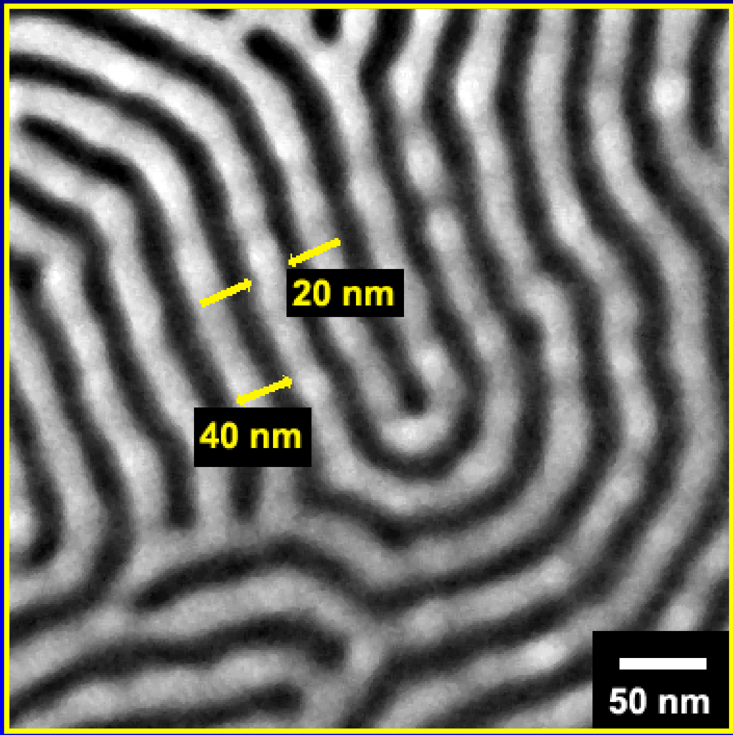
IC decoupling capacitor and nanocrystal FLASH memory rely on uniform *size* of polymer domains

What about applications which require control of polymer domain size and *position*?

directing polymer assembly

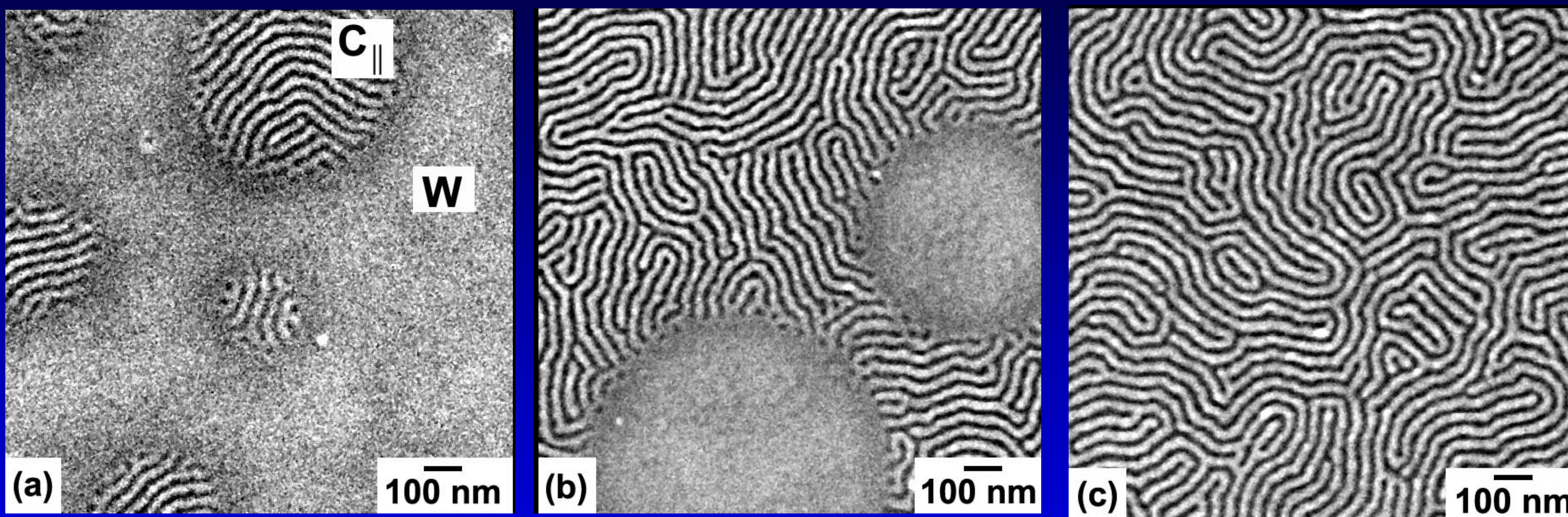
without random copolymer, cylindrical domains orient in-plane





line/space pattern dimensions defined by intrinsic polymer properties

thickness dependence



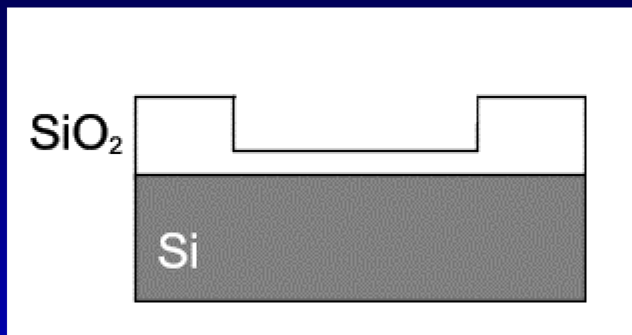
pre-bake thickness:

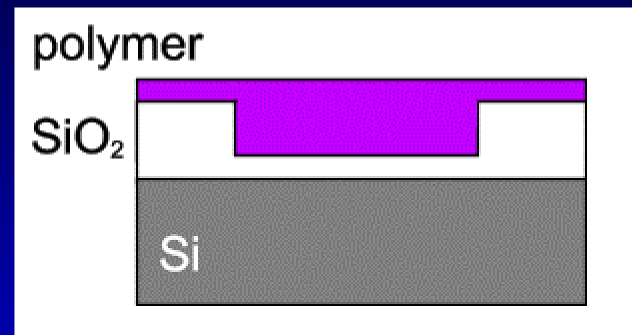
300 Ǻ | 320 Ǻ | 350 Ǻ

- **in-plane self assembly exhibits strong thickness dependence**
- **below a critical thickness, polymer favors formation of "islands" of cylinders**

directing polymer assembly

idea: use surface topography to position polymer "islands"





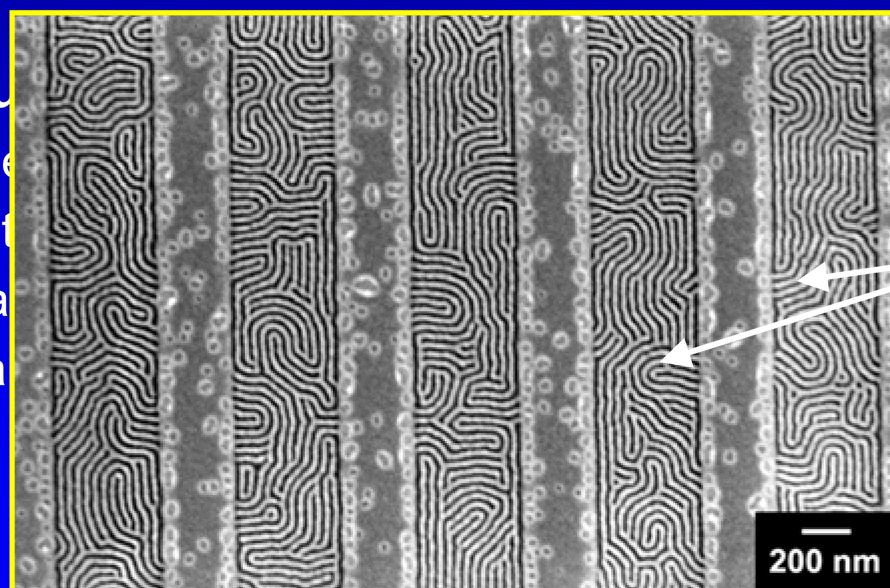
several beautifu **proach:**

R. Segalman e

J. Y. Cheng et

S. O. Kim et a

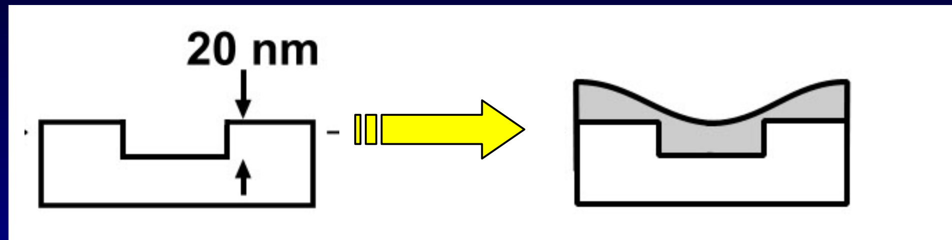
S. H. Kim et a



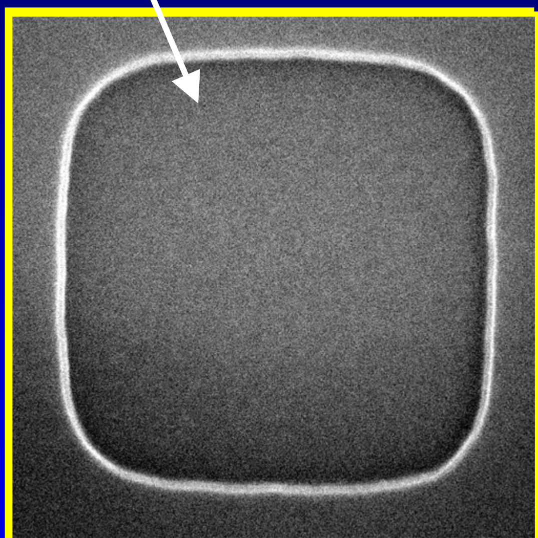
oxide recessed 20 nm

polymer islands preferentially form in recessed areas

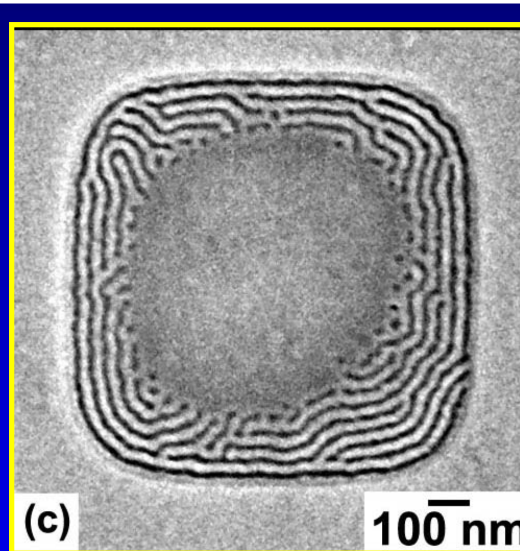
kinetics of directed polymer assembly



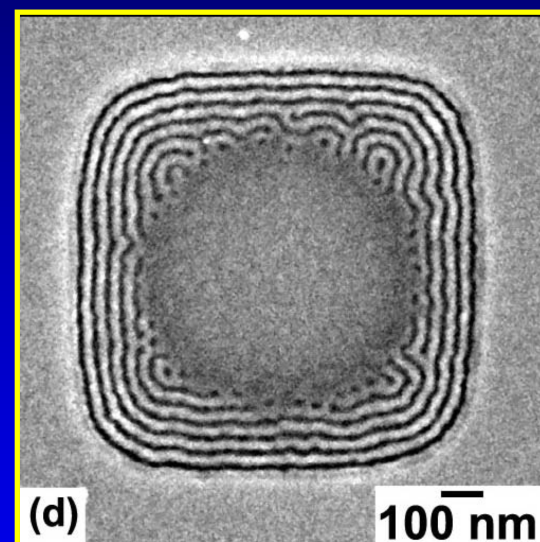
recessed
20 nm



10 min.



1 hr



12 hr

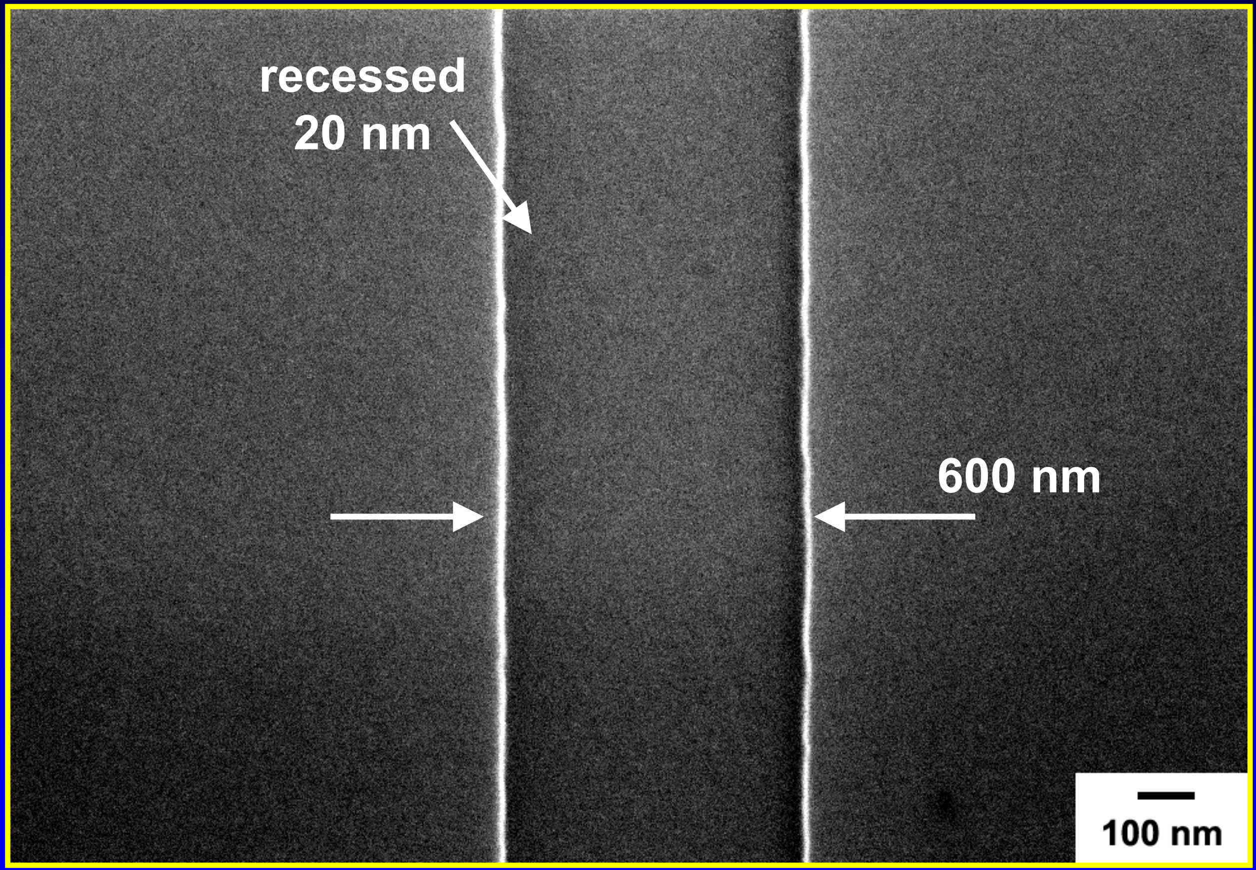
step edge nucleates polymer phase separation

parallel domains run ~4 μm (i.e. around the perimeter) without defects

C. T. Black and O. Bezencenet, *IEEE Transactions on Nanotechnology* (in press).

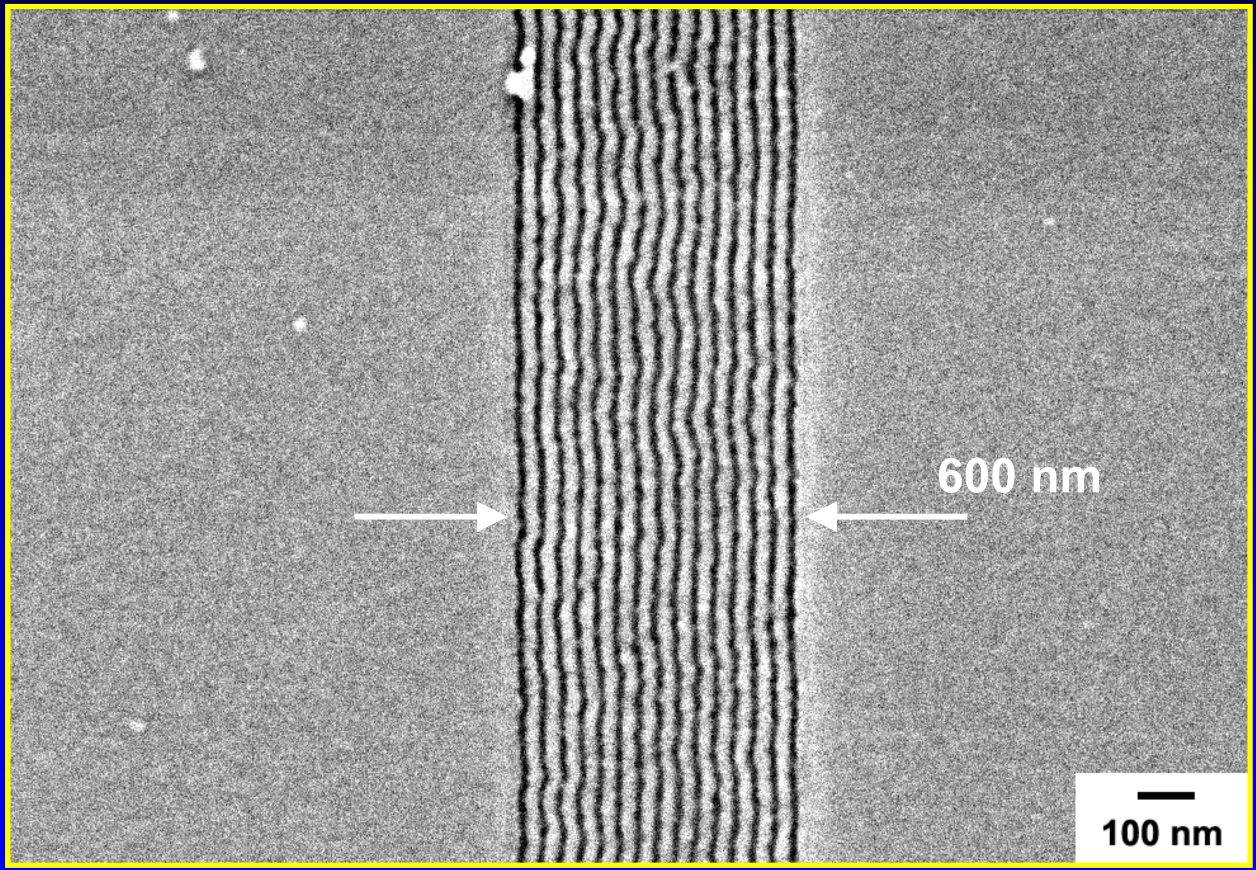
IBM

lithographic subdivision by self assembly



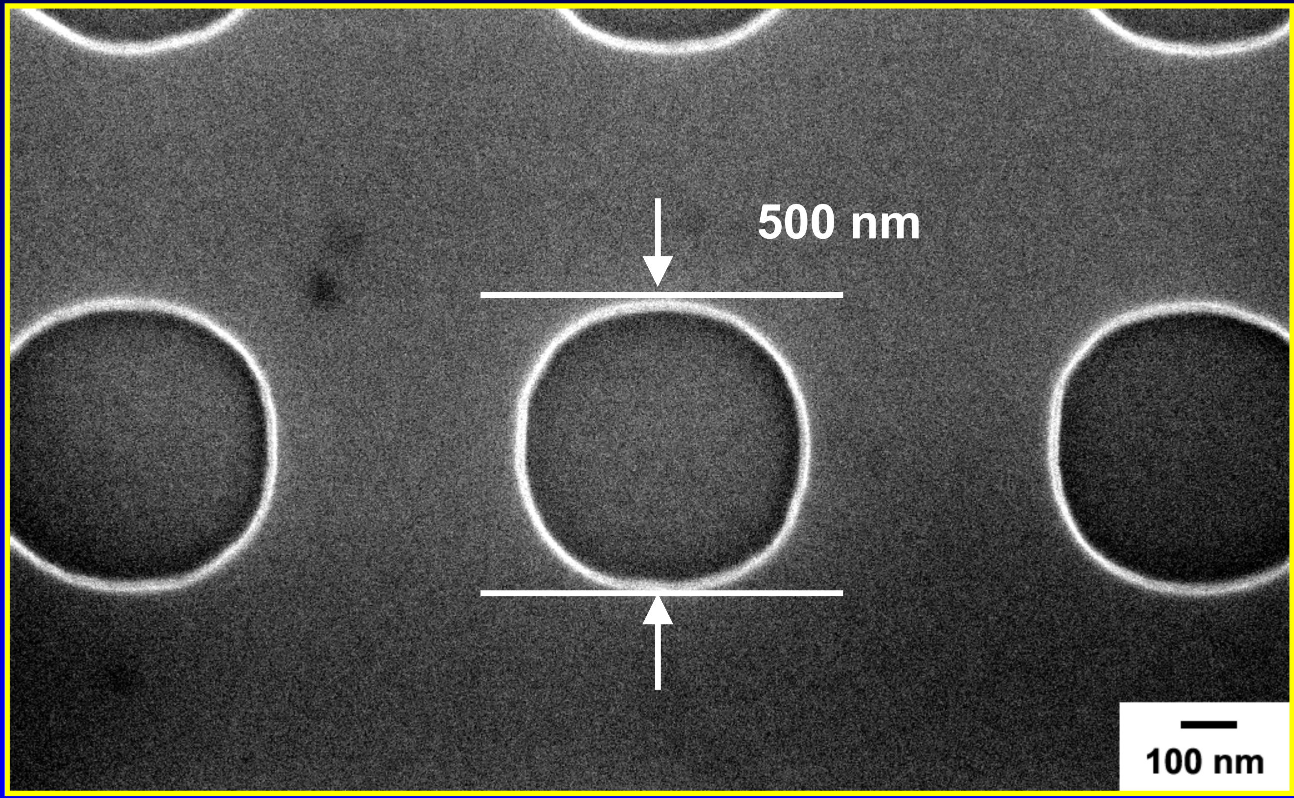
0.6 μm line patterned by conventional methods (optical lithography + reactive-ion etching)

lithographic subdivision by self assembly



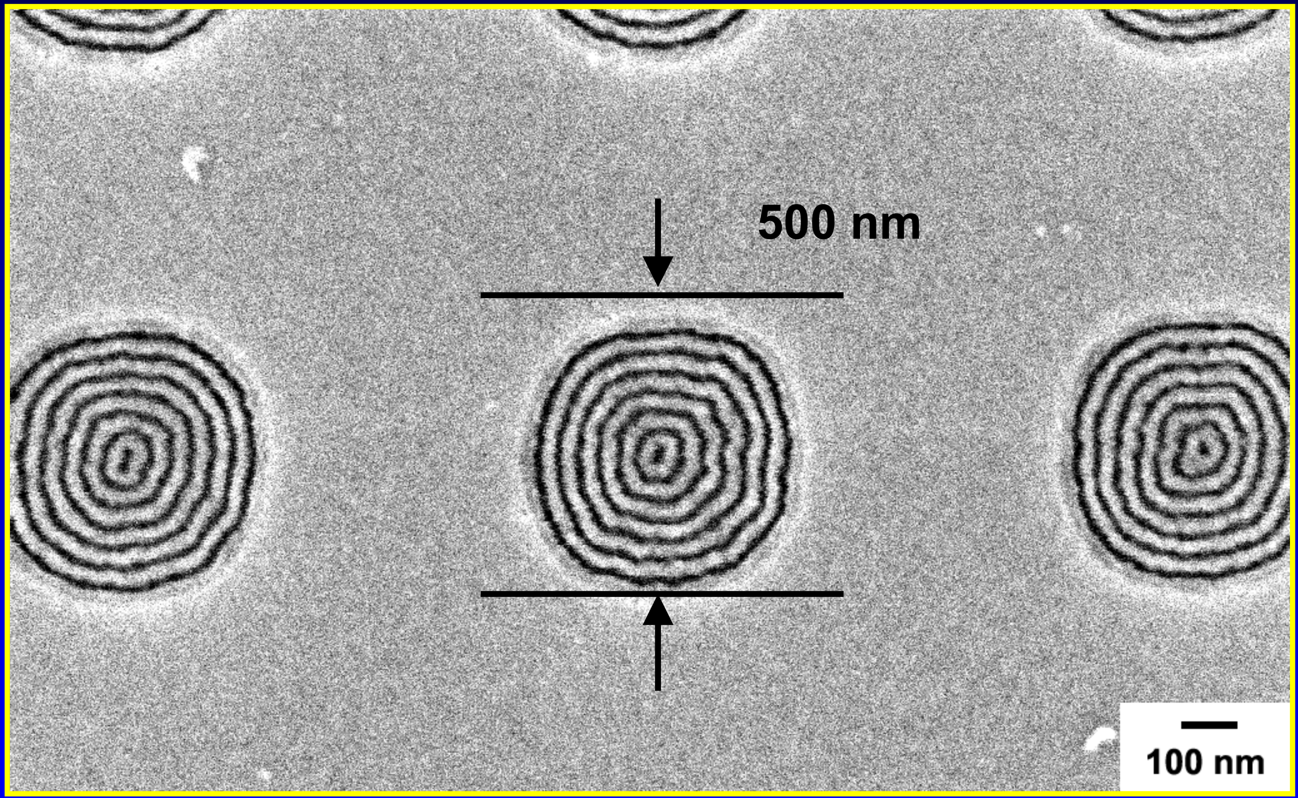
0.6 μm line completely subdivided by 14.5 polymer periods

lithographic subdivision by self assembly



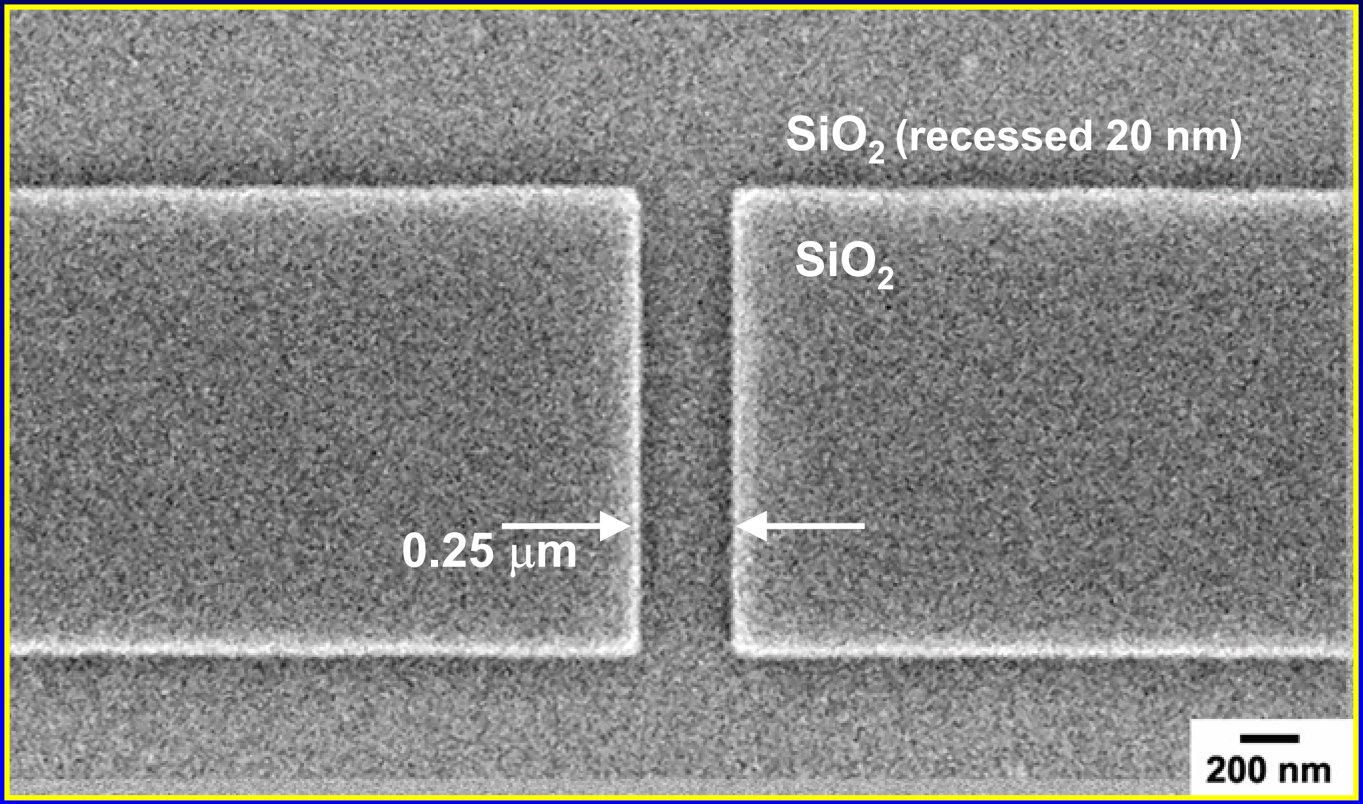
0.5 μm diameter circles patterned by conventional methods
(optical lithography + reactive-ion etching)

lithographic subdivision by self assembly



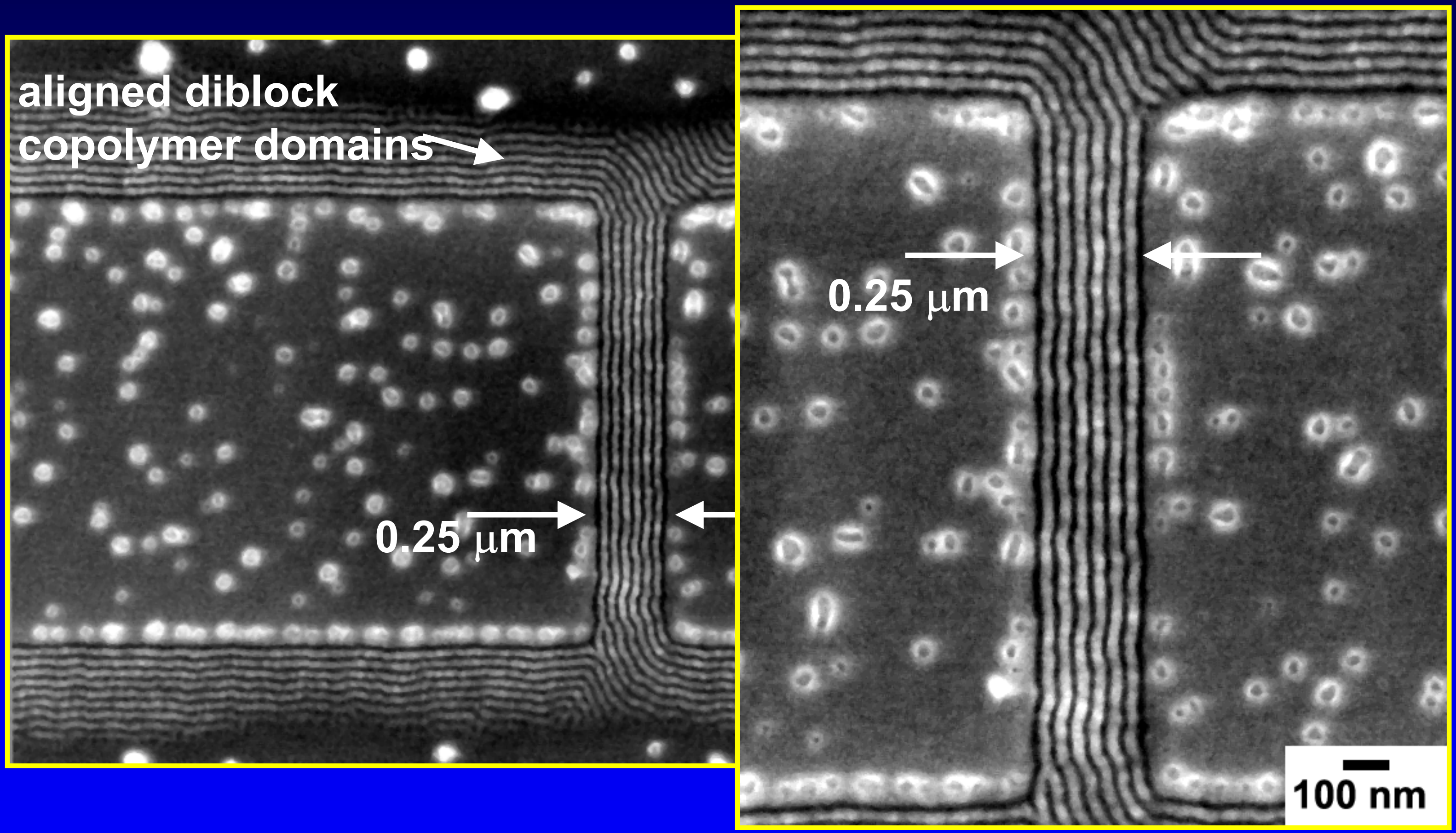
0.5 μm diameter circles subdivided by 7.5 concentric polymer periods

lithographic subdivision by self assembly



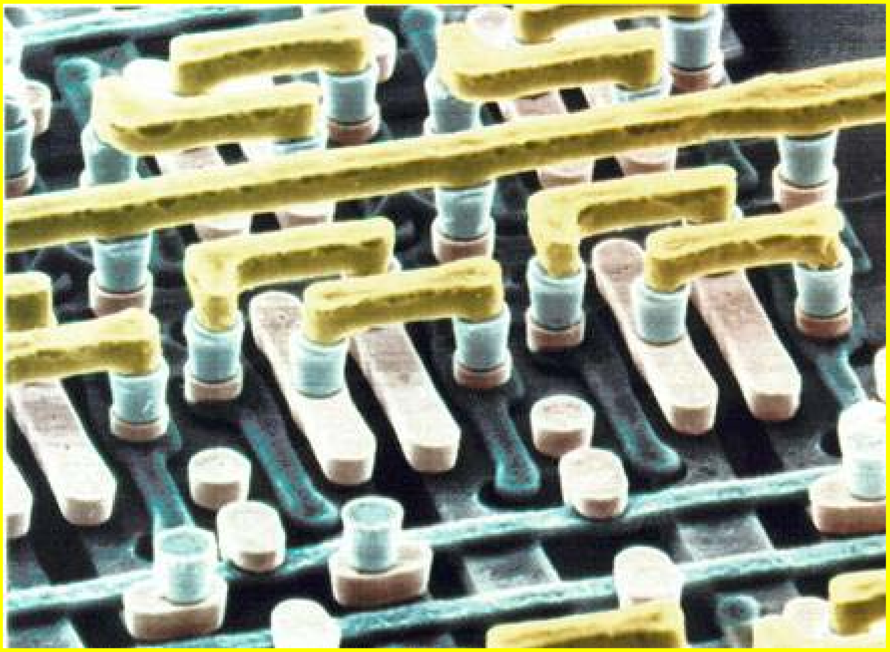
more complex shapes can be patterned in a similar manner

lithographic subdivision by self assembly

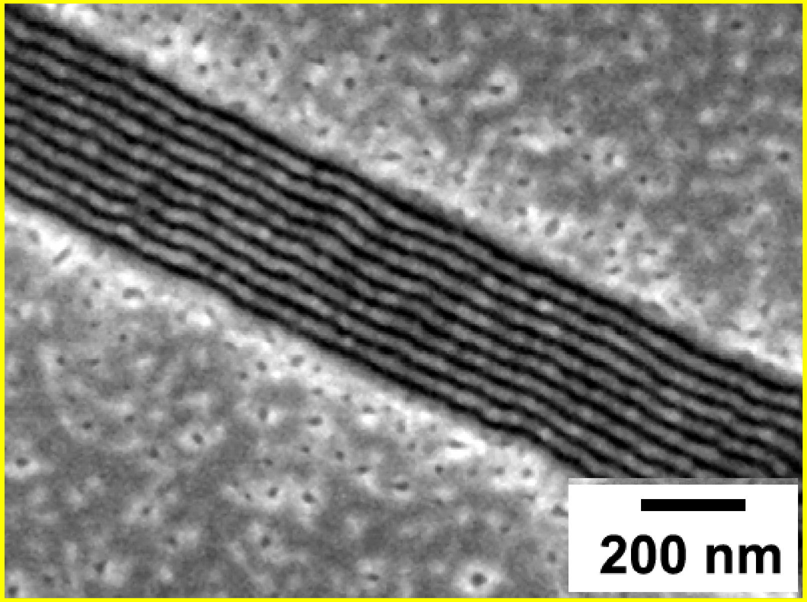


"open" lithographic shapes help assembly at boundaries

self assembling circuits?



conventional manufacturing:
- complex, precise, repeatable
- high cost, labor/tool intensive



self assembly:
smaller sizes? cheaper? easier?

not yet, but….

message

diblock copolymer thin films

- meet materials compatibility requirements for semiconductor processing
- allow access to nanometer length scales

combine advantages of self assembly and microfabrication to produce new routes to nanostructures

applications in microelectronics

- IC decoupling capacitor
- nanocrystal FLASH memory

directing polymer assembly with lithographic patterning

- lithographic subdivision
- applications requiring discrete self-assembled elements