CHECK IT POSTcard

POSTcard and PCI POSTcard

Diagnostic Cards

Version 2.0

User's Manual

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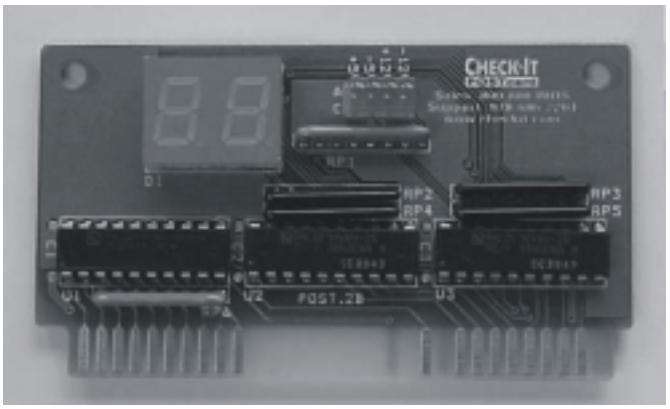

QUALITY TESTED

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Unicore Software, Inc

CheckIt POSTcard

POSTcard mini and
PCI POSTcard

Power On Self Test (POST) System

Diagnostic Board

Version 2.0

User's Manual

Unicore Software, Inc. does not make any claims as to the accuracy of the information contained in this manual and reserves the right to make changes to this information without prior notice.

Warranty

The Unicore Software, Inc. CheckIt POSTcards™ are warranted to be free from failures due to defects in material and workmanship for a period of 90 days following purchase. During this period, Unicore will, at its sole option, repair or replace at no charge a CheckIt POSTcard which in its opinion is defective.

This warranty applies only if the CheckIt POSTcard fails to function properly under normal use and within Unicore's specifications. If the failed CheckIt POSTcard has been modified without Unicore's consent or if the failure is a result of misuse, abuse, or misapplication, Unicore is under no obligation to repair or replace the failed CheckIt POSTcard.

You are responsible for properly packing the failed card for shipment and for the charges to ship the failed CheckIt POSTcard to Unicore and Unicore is responsible for charges to ship the repaired or replacement CheckIt POSTcard back to you.

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For information on obtaining service under this warranty, contact the Dealer from which the CheckIt POSTcard was purchased or contact Unicore directly.

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Overview

The Unicore Software, Inc. CheckIt POSTcard is an 8-bit card that fits into a PCI or ISA slot on your computer. The CheckIt PCI POSTcard and POSTcard Mini will work on any computer (XT all the way to Pentium class machines) that support BIOS POST codes.

The two CheckIt POSTcards are ideal tools for troubleshooting PCs down to the component level, saving you hundreds of dollars along the way. These POSTcards use hexadecimal LED displays to indicate possible error codes.

POST Sequence

The Power on System Test (POST) routines in the BIOS perform tests and initialize the circuitry on the motherboard peripheral adapter boards. The POST is reached by powering on the system or by using the Ctrl-Alt-Del reboot keystrokes.

The degree and path of the test/initialization will vary among different versions of the BIOS. The usual sequence is:

- CPU register checks.
- Setup the 8253/8254 timer for RAM refresh timing.
- Setup the DMA in RAM refresh on channel 0.
- Verify refresh is operating.
- Test low RAM 16-64k.
- Load interrupt vectors and assign a stack in the low RAM area.
- Initialize video and keyboard devices.
- Size and test remaining RAM.
- Initialize all COM, LPT and game ports.
- Initialize floppy disk system.
- Initialize hard disk system (AT class systems).
- Scan user ROM area.
- Call boot strap interrupt.
- Most ISA machines output their POST codes to port 80h with the exception of COMPAQ, which outputs all codes to I/O port 84h.

Installation

WARNING! The CheckIt POSTcard must always be installed with the arrow on the sticker on the back of the card facing the back of the computer. If you insert the card the wrong way, you will burn out its power cells and it will not function.

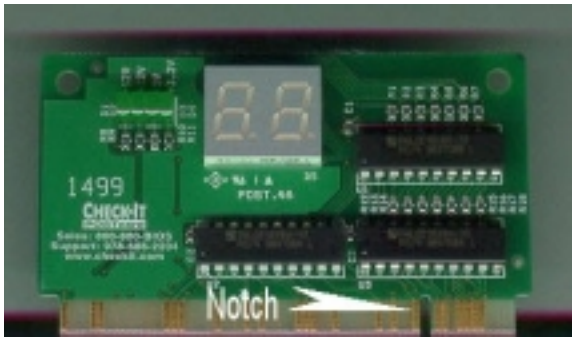
Note: The back of the computer is the end where all the cables for the monitor, keyboard, mouse, etc. are plugged in.

What slot to insert the cards into:

There are two different kinds of cards.

1. One is an ISA-style card that has an arrow. When you insert the card, make sure the arrow is pointing toward the back of the computer.

   This is the **CheckIt ISA POSTcard** goes into an ISA slot. ISA slots are usually black and about 5.5" long. Insert the card so that the arrow on the sticker on the card is pointing toward the back of the computer. Put the card into the slot so that it is as close to the back of the computer as possible. See the picture below of this card and its notch in the bottom.



2. The other card has a notch in the bottom. This card is the **CheckIt PCI POSTcard** and it goes in a PCI slot. PCI slots are usually white and about 3.25" long. A PCI card has a notch in it that allows it to go into a PCI slot in only one direction. If your card does not have a notch, it should go into an ISA slot. See below.

Note: Shut your computer's power OFF when installing the CheckIt POSTcard.

To install:

1. Turn off your CPU, monitor, printer, and all other peripherals attached to the computer.
2. Disconnect all cables and power cords from the rear of your computer.
3. Remove the cover of your computer very carefully.
4. Carefully take the CheckIt POSTcard mini from its protective wrapping, making sure to handle the card by its edges.

5. To determine which slot to insert the card into, see the two choices listed above.
6. Position the card so that the arrow on the sticker on it points to the back of your computer. The back of the computer is where all the cables are plugged in.

Note: If your card does not have an arrow with a sticker on it, insert the card with the CheckIt label on the same side as the back of the computer.

7. Press the card firmly into the slot.
8. To run the card, turn on your computer.

The card's displays your computer's ROM BIOS POST codes as the computer boots up.

If the LED display stops on a particular code, look this code up under the appropriate BIOS manufacturer's table in the appendix to determine what the problem is.

For example, if you have a Award BIOS, go to that table's codes and look up the one on the card. For instance, 09 for a Award BIOS means the keyboard is not working, perhaps because it is not plugged in.

Troubleshooting

If you are having problems installing the POSTcard, review this checklist:

- Is everything in your computer plugged in and turned on?
- Are all cables and cords connected properly?
- Are all necessary jumper or DIP switches set correctly?
- Is the proper diskette in the proper floppy drive?
- Is the electric wall socket the computer is plugged into working?
- Is the power on?
- Do any LED lights light up? If the LED lights are not on and your computer is plugged in and turned on, then the power supply may not work on your computer.
- Does the hard drive light come on? Do any of the floppy disk drive lights come on? Do any of the disk drives make noises? If the power light is on, but the disk drive lights do not come on or you do not hear the disk drives turning, the problem may be with the floppy disk drives or the hard disk drives.

Does the computer beep when you turn it on? One beep means your computer is okay. More than one beep means there is an error code. Write down the error code on the LED display and the number of beeps and whether they are long or short.

Lights on the Card

When you boot up your computer with a CheckIt POSTcard installed, there are a series of lights on the cards that give you information.

Reset: When lit, this means the computer was successfully reset or rebooted.

CLK: This tells you that the data and command lines were synchronized correctly.

+12V, -12V, +5V, +3.3V: These lights tell you what kind of voltage is going into your computer. If +3.3V is not lit, then that kind of voltage is not going to your computer. This is for informational purposes only.

Frequently Asked Questions

Q: Will the CheckIt POSTcard work in my XT computer?

A: Yes, the POSTcard works on any PC as long as that computer's ROM BIOS supports POST error codes.

Q: What are ROM BIOS POST error codes?

A: When your system is first turned on, the ROM BIOS initializes various components on your system and determines what is and is not working. While running this sequence of tests, the ROM BIOS outputs certain numerical codes to a particular I/O port on your computer. This code is called a POST code and signifies what particular test the BIOS is executing at that time.

Q: What do I do with the POST code?

A: If your computer fails one of the POST tests, that POST code will be displayed on the POSTcard's LED displays. You can then look up the POST code in the appendix of this manual to determine which test the ROM BIOS actually failed on.

Q: How do I determine which ROM BIOS is on my machine?

A: To determine which BIOS you have:

- When your computer first boots up, you may see a message indicating a particular brand of ROM BIOS and version number.
- When your system first boots up, you may see a message display with the particular brand of BIOS and its version number on your screen.
- If your system will not boot, look on the motherboard for the ROM BIOS chips. These chips are marked with the brand name on a sticker (see Figure 2).
- If you cannot find this information on the chips, look in the manual that came with your system for the brand name of the BIOS that came with your computer or call the computer manufacturer for this information.

Q: What are the most popular brand names for ROM BIOS?

A: The most popular are AMI, AWARD, IBM, MR BIOS, PHOENIX, and QUADTEL.

Q: What happens if my ROM BIOS does not support POST codes?

A: Most BIOS versions support POST codes, but if your system does not, you can always replace your existing ROM BIOS with a new BIOS which does support POST codes.

System Motherboard

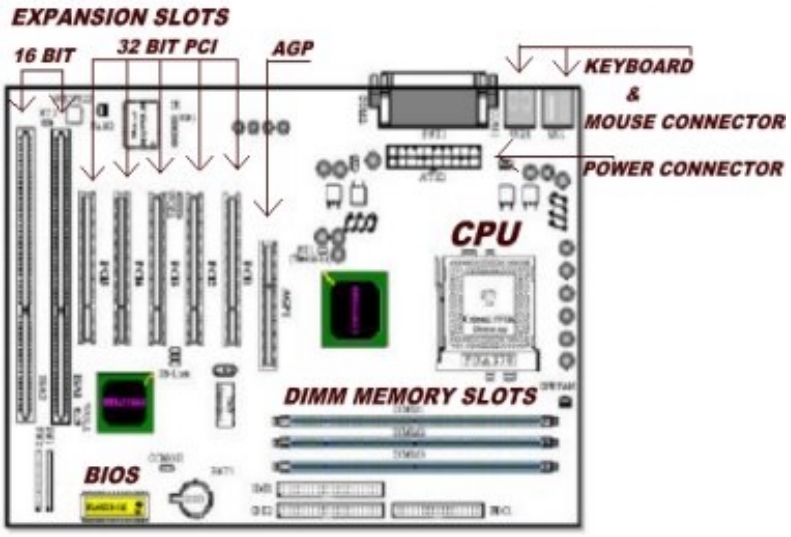


Figure 2. System Motherboard

Figure 2 is a diagram of a typical motherboard layout. Some computers have what is called a passive backplane. On these systems, most of the electronics would be on a plug-in card. The POSTcard will work the same as on a standard motherboard.

BIOS-Specific POST Codes

Note: These POST Codes are extracted from a book called The BIOS Companion. You can order this book from this website: http://www.electrocution.com. The BIOS Companion explains all those settings in your BIOS in plain English, as well as containing stacks of other technical information

The POST code that the CheckIt POSTcard displays points to the general area of a failure. The codes change with each test that is performed. If the code stays on at 00h or FFh, then the BIOS is not emitting POST codes. Check to make sure the BIOS that came with your computer supports BIOS POST codes and determine which I/O port it uses.

Note: Remember to always check the area indicated by the POST code. The failure indicated by the POST code should be fixed. If this does not solve the problem, you need to perform more testing. Test the chip or chips that the POST code indicated had failed.

During the POST on AT-compatibles and above, special signals are output to I/O port 80H at the beginning of each test (genuine PCs and XTs don't issue POST codes, although some machines with compatible BIOSes do). Some computers may use a different port, such as 84 for the Compaq or 378 (LPT1) for Olivetti. IBM PS/2s use 90, while some EISA machines send them to 300H as well. Those at 50h are chipset or custom platform specific.

Having obtained a POST code, identify the manufacturer of the chipset on the motherboard, then refer to the *Chipsets* section to find the chip(s) that control whatever is not working.

The POST checks three levels, *Early*, *Late* and *System Initialization*. Early POST failures are generally fatal and will produce a beep code, because the video will not be active; in fact, the last diagnostic during Early POST is usually on the video, so that Late failures can actually be seen. System Initialization involves loading configuration from the CMOS, and failures will generate a text message. Consistent failures indicate a bad battery backup system.

Shutdown or Reset Commands

The Reset command stops the current operation and begins fetching instructions from the BIOS, as if the power has just been switched on. The Shutdown command, on the other hand, just forces the CPU to leave protected mode for real mode, so the system behaves differently after each one. Before issuing the shutdown command, the BIOS sets a value into the *shutdown byte* in the CMOS, which is checked after a reset, so the BIOS can branch to the relevant code and continue where it left off.

One of the problems with shutdown handling is that the POST must do some handling before anything else, immediately after power-on or system reset. The path between the CPU and the BIOS ROM, as well as basic control signals, has to be working before the POST gets to its first diagnostic test (usually the CPU register test), so some of the

circuitry that the CPU test is supposed to check will be checked by the shutdown handling instead, and you will get no POST indication if a critical failure occurs.

Manufacturing Loop Jumper

The phrase *Check for Manufacturing Jumper* in the tables refers to one on the motherboard that makes the POST run in a continuous loop, so you can burn in a system, or use repetitive cycling to monitor a failing area with an oscilloscope or logic analyzer. It usually forces a reset, so the POST has to start from the beginning every time. Compaq used to have the shorted jumper cause the POST to jump to another ROM at E000 just after power-on, which could have diagnostic code in it. IBM and NCR used a germanium or silicon diode to short together the keyboard connector pins 1 (cathode, bar) and 2 (5-pin DIN) or 1 (anode, arrow) and 5 (6-pin mini-DIN), so the POST checks the keyboard controller to see whether the jumper is installed.

Note: To get the latest updates to the Post Codes, you may have to go to the manufacturer's specific web site and download their last post codes.

ACER

Based on Award BIOS 3.03, but not exactly the same.

Code	Meaning
04	Start
08	Shutdown
0C	Test BIOS ROM checksum
10	Test CMOS RAM shutdown byte
14	Test DMA controller
18	Initialize system timer
1C	Test memory refresh
1E	Determine memory type
20	Test 128K memory
24	Test 8042 keyboard controller
28	Test CPU descriptor instruction
2C	Set up and test 8259 interrupt controller
30	Set up memory interrupts
34	Set up BIOS interrupt vectors and routines
38	Test CMOS RAM
3C	Determine memory size
XX	Shut down 8 (system halt C0h + checkpoint)
40	Shutdown 1
44	Initialize Video BIOS ROM
45	Set up and test RAM BIOS
46	Test cache memory and controller
48	Test memory
4C	Shutdown 3
50	Shutdown 2
54	Shutdown 7
55	Shutdown 6
5C	Test keyboard and auxiliary I/O

Code	Meaning
60	Set up BIOS interrupt routines
64	Test real time clock
68	Test diskette
6C	Test hard disk
70	Test parallel port
74	Test serial port
78	Set time of day
7C	Scan for and invoke option ROMs
80	Determine presence of math coprocessor
84	initialize keyboard
88	Initialize system 1
8C	Initialize system 2
90	Invoke INT 19 to boot operating system
94	Shutdown 5
98	Shutdown A
9C	Shutdown B

ALR

See *Phoenix*.

Ambra

See *Phoenix*.

AMI

Not all tests are performed by all AMI BIOSes. Those below refer to the 2 Feb 91 BIOS.

POST Procedures

Procedure	Explanation
NMI Disable	NMI interrupt line to the CPU is disabled by setting bit 7 I/O port 70h (CMOS).
Power On Delay	Once the keyboard controller gets power, it sets the hard and soft reset bits. Check the keyboard controller or clock generator.
Initialize Chipsets	Check the BIOS, CLOCK or chipsets.
Reset Determination	The BIOS reads the bits in the keyboard controller to see if a hard or soft reset is required (a soft reset will not test memory above 64K). Failure could be the BIOS or keyboard controller.
ROM BIOS Checksum	The BIOS performs a checksum on itself and adds a preset factory value that should make it equal 00. Failure is due to the BIOS chips.
Keyboard Test	A command is sent to the 8042 (keyboard controller) which performs a test and sets a buffer space for commands. After the buffer is defined the BIOS sends a command byte, writes data to the buffer, checks the high order bits (Pin 23) of the internal keyboard controller and issues a No Operation (NOP) command.
CMOS	Shutdown byte in CMOS RAM offset 0F is tested, the BIOS

Procedure	Explanation
	checksum calculated and diagnostic byte (0E) updated before the CMOS RAM area is initialized and updated for date and time. Check RTC/CMOS chip or battery.
8237/8259 Disable	The DMA and Interrupt Controller are disabled before the POST proceeds any further. Check the 8237 or 8259 chips.
Video Disable	The video controller is disabled and Port B initialized. Check the video adapter if you get problems here.
Chipset Init/Memory Detect	Memory addressed in 64K blocks; failure would be in the chipset. If all memory is not seen, failure could be in a chip in the block after the last one seen.
PIT test	The timing functions of the 8254 interrupt timer are tested. The PIT or RTC chips normally cause problems here.
Memory Refresh	PIT's ability to refresh memory tested (if an XT, DMA controller #1 handles this). Failure is normally the PIT (8254) in ATs or the 8237 (DMA #1) in XTs.
Address Lines	Test the address lines to the first 64K of RAM. An address line failure.
Base 64K	Data patterns are written to the first 64K, unless there is a bad RAM chip in which case you will get a failure.
Chipset Initialization	The PIT, PIC and DMA controllers are enabled.
Set Interrupt Table	Interrupt vector table used by PIC is installed in low memory, the first 2K.
8042 check	The BIOS reads the buffer area of the keyboard controller I/O port 60. Failure here is normally the keyboard controller.
Video Tests	The type of video adapter is checked for then a series of tests is performed on the adapter and monitor.
BIOS Data Area	The vector table is checked for proper operation and video memory verified before protected mode tests are entered into. This is done so that any errors found are displayed on the monitor.
Protected Mode Tests	Perform reads and writes to all memory below 1 Mb. Failures at this point indicate a bad RAM chip, the 8042 chip or a data line.
DMA Chips	The DMA registers are tested using a data pattern.
Final Initialization	These differ with each version. Typically, the floppy and hard drives are tested and initialized, and a check made for serial and parallel devices. The information gathered is then compared against the contents of the CMOS, and you will see the results of any failures on the monitor.
Boot	The BIOS hands over control to the Int 19 bootloader; this is where you would see error messages such as non-system disk.

AMI BIOS 2.2x

Code	Meaning
00	Flag test
03	Register test
06	System hardware initialization
09	BIOS ROM checksum
0C	Page register test

Code	Meaning
0F	8254 timer test
12	Memory refresh initialization
15	8237 DMA controller test
18	8237 DMA initialization
1B	8259 interrupt controller initialization
1E	8259 interrupt controller test
21	Memory refresh test
24	Base 64K address test
27	Base 64K memory test
2A	8742 keyboard self test
2D	MC 146818 CMOS test
30	Start first protected mode test
33	Memory sizing test
36	First protected mode test
39	First protected mode test failed
3C	CPU speed calculation
3F	Read 8742 hardware switches
42	Initialize interrupt vector area
45	Verify CMOS configuration
48	Test and initialize video system
4B	Unexpected interrupt test
4E	Start second protected mode test
51	Verify LDT instruction
54	Verify TR instruction
57	Verify LSL instruction
5A	Verify LAR instruction
5D	Verify VERR instruction
60	Address line 20 test
63	Unexpected exception test
66	Start third protected mode test
69	Address line test
6C	System memory test
6F	Shadow memory test
72	Extended memory test
75	Verify memory configuration
78	Display configuration error messages
7B	Copy system BIOS to shadow memory
7E	8254 clock test
81	MC 146818 real time clock test
84	Keyboard test
87	Determine keyboard type
8A	Stuck key test
8D	Initialize hardware interrupt vector
90	Math coprocessor test
93	Determine COM ports available
96	Determine LPT ports available
99	Initialize BIOS data area
9C	Fixed/Floppy controller test
9F	Floppy disk test
A2	Fixed disk test
A5	External ROM scan

Code	Meaning
A8	System key lock test
AE	F1 error message test
AF	System boot initialization
B1	Interrupt 19 boot loader

AMI Old BIOS (AMI Plus BIOS); 08/15/88—04/08/90

Code	Meaning
01	NMI disabled & 286 reg. test about to start
02	286 register test over
03	ROM checksum OK
04	8259 initialization OK
05	CMOS pending interrupt disabled
06	Video disabled & system timer counting OK
07	CH-2 of 8253 test OK
08	CH-2 delta count test OK
09	CH-1 delta count test OK
0A	CH-0 delta count test OK
0B	Parity status cleared
0C	Refresh & system timer OK
0D	Refresh link toggling OK
0E	Refresh period ON/OFF 50% OK
10	Confirmed refresh ON & about to start 64K memory
11	Address line test OK
12	64K base memory test OK
13	Interrupt vectors initialized
14	8042 keyboard controller test OK
15	CMOS read/write test OK
16	CMOS checksum/battery check OK
17	Monochrome mode set OK
18	Color mode set OK
19	About to look for optional video ROM
1A	Optional video ROM control OK
1B	Display memory read/write test OK
1C	Display memory read/write test for alt display OK
1D	Video retrace check OK
1E	Global equipment byte set for video OK
1F	Mode set call for Mono/Color OK
20	Video test OK
21	Video display OK
22	Power on message display OK
30	Virtual mode memory test about to begin
31	Virtual mode memory test started
32	Processor in virtual mode
33	Memory address line test in progress
34	Memory address line test in progress
35	Memory below 1MB calculated
36	Memory size computation OK
37	Memory test in progress
38	Memory initialization over below 1MB

Code	Meaning
39	Memory initialization over above 1MB
3A	Display memory size
3B	About to start below 1MB memory test
3C	Memory test below 1MB OK
3D	Memory test above 1MB OK
3E	About to go to real mode (shutdown)
3F	Shutdown successful and entered in real mode
40	About to disable gate A-20 address line
41	Gate A-20 line disabled successfully
42	About to start DMA controller test
4E	Address line test OK
4F	Processor in real mode after shutdown
50	DMA page register test OK
51	DMA unit-1 base register test about to start
52	DMA unit-1 channel OK; about to begin CH-2
53	DMA CH-2 base register test OK
54	About to test f/f latch for unit-1
55	f/f latch test both unit OK
56	DMA unit 1 & 2 programmed OK
57	8259 initialization over
58	8259 mask register check OK
59	Master 8259 mask register OK; about to start slave
5A	About to check timer and keyboard interrupt level
5B	Timer interrupt OK
5C	About to test keyboard interrupt
5D	ERROR! timer/keyboard interrupt not in proper level
5E	8259 interrupt controller error
5F	8259 interrupt controller test OK
70	Start of keyboard test
71	Keyboard BAT test OK
72	Keyboard test OK
73	Keyboard global data initialization OK
74	Floppy setup about to start
75	Floppy setup OK
76	Hard disk setup about to start
77	Hard disk setup OK
79	About to initialize timer data area
7A	Verify CMOS battery power
7B	CMOS battery verification done
7D	About to analyze diagnostic test results for memory
7E	CMOS memory size update OK
7F	About to check optional ROM C000:0
80	Keyboard sensed to enable setup
81	Optional ROM control OK
82	Printer global data initialization OK
83	RS-232 global data initialization OK
84	80287 check/test OK
85	About to display soft error message
86	About to give control to system ROM E000:0
87	System ROM E000:0 check over
00	Control given to Int-19; boot loader

AMI BIOS 04/09/90-02/01/91

Code	Meaning
01	NMI disabled and 286 register test about to start.
02	286 register test passed.
03	ROM BIOS checksum (32K at F800:0) passed.
04	Keyboard controller test with and without mouse passed.
05	Chipset initialization over; DMA and Interrupt controller disabled.
06	Video disabled and system timer test begin.
07	CH-2 of 8254 initialization half way.
08	CH-2 of timer initialization over.
09	CH-1 of timer initialization over.
0A	CH-0 of timer initialization over.
0B	Refresh started.
0C	System timer started.
0D	Refresh link toggling passed.
10	Refresh on and about to start 64K base memory test.
11	Address line test passed.
12	64K base memory test passed.
15	Interrupt vectors initialized.
17	Monochrome mode set.
18	Color mode set.
19	About to look for optional video ROM at C000 and give control to ROM if present.
1A	Return from optional video ROM.
1B	Shadow RAM enable/disable completed.
1C	Display memory read/write test for main display type as set in the CMOS setup program over.
1D	Display memory read/write test for alternate display type complete if main display memory read/write test returns error.
1E	Global equipment byte set for proper display type.
1F	Video mode set call for mono/color begins.
20	Video mode set completed.
21	ROM type 27256 verified.
23	Power on message displayed.
30	Virtual mode memory test about to begin.
31	Virtual mode memory test started.
32	Processor executing in virtual mode.
33	Memory address line test in progress.
34	Memory address line test in progress.
35	Memory below 1MB calculated.
36	Memory above 1MB calculated.
37	Memory test about to start.
38	Memory below 1MB initialized.
39	Memory above 1MB initialized.
3A	Memory size display initiated. Will be updated when BIOS goes through memory test.
3B	About to start below 1MB memory test.
3C	Memory test below 1MB completed; about to start above 1MB test.
3D	Memory test above 1MB completed.
3E	About to go to real mode (shutdown).

Code	Meaning
3F	Shutdown successful and processor in real mode.
40	Cache memory on and about to disable A20 address line.
41	A20 address line disable successful.
42	486 internal cache turned on.
43	About to start DMA controller test.
50	DMA page register test complete.
51	DMA unit-1 base register test about to start.
52	DMA unit-1 base register test complete.
53	DMA unit-2 base register test complete.
54	About to check F/F latch for unit-1 and unit-2.
55	F/F latch for both units checked.
56	DMA unit 1 and 2 programming over; about to initialize 8259 interrupt controller.
57	8259 initialization over.
70	About to start keyboard test.
71	Keyboard controller BAT test over.
72	Keyboard interface test over; mouse interface test started.
73	Global data initialization for keyboard/mouse over.
74	Display 'SETUP' prompt and about to start floppy setup.
75	Floppy setup over.
76	Hard disk setup about to start.
77	Hard disk setup over.
79	About to initialize timer data area.
7A	Timer data initialized and about to verify CMOS battery power.
7B	CMOS battery verification over.
7D	About to analyze POST results.
7E	CMOS memory size updated.
7F	Look for <DEL> key and get into CMOS setup if found.
80	About to give control to optional ROM in segment C800 to DE00.
81	Optional ROM control over.
82	Check for printer ports and put the addresses in global data area.
83	Check for RS232 ports and put the addresses in global data area.
84	Coprocessor detection over.
85	About to display soft error messages.
86	About to give control to system ROM at segment E000.
00	System ROM control at E000 over now give control to Int 19h boot loader.

AMI New BIOS; 02/02/91—12/12/91

Code	Meaning
01	Processor register test about to start and NMI to be disabled.
02	NMI is Disabled. Power on delay starting.
03	Power on delay complete. Any initialization before keyboard BAT is in progress.
04	Init before keyboard BAT complete. Reading keyboard SYS bit to check soft reset/ power-on.
05	Soft reset/ power-on determined. Going to enable ROM. i. e. disable shadow RAM/Cache.
06	ROM enabled. Calculating ROM BIOS checksum, waiting for KB controller input buffer to be free.

Code	Meaning
07	ROM BIOS Checksum passed. KB controller I/B free. Going to issue BAT comd to kboard controller.
08	BAT command to keyboard controller issued. Going to verify BAT command.
09	Keyboard controller BAT result verified. Keyboard command byte to be written next.
0A	Keyboard command byte code issued. Going to write command byte data.
0B	Keyboard controller command byte written. Going to issue Pin-23 & 24 blocking/unblocking command
0C	Pin 23 & 24 of keyboard controller is blocked/unblocked. NOP command of keyboard controller to be issued next.
0D	NOP command processing done. CMOS shutdown register test to be done next.
0E	CMOS shutdown register R/W test passed. Going to calculate CMOS checksum, update DIAG byte.
0F	CMOS checksum calculation is done DIAG byte written. CMOS init. to begin (If INIT CMOS IN EVERY BOOT is set).
10	CMOS initialization done (if any). CMOS status register about to init for Date and Time.
11	CMOS Status register initialized. Going to disable DMA and Interrupt controllers.
12	DMA Controller #1 & #2, interrupt controller #1 & #2 disabled. About to disable Video display and init port-B.
13	Video display disabled and port-B initialized. Chipset init/auto mem detection about to begin.
14	Chipset initialization/auto memory detection over. 8254 timer test about to start.
15	CH-2 timer test halfway. 8254 CH-2 timer test to be complete.
16	Ch-2 timer test over. 8254 CH-1 timer test to be complete.
17	CH-1 timer test over. 8254 CH-0 timer test to be complete.
18	CH-0 timer test over. About to start memory refresh.
19	Memory Refresh started. Memory Refresh test to be done next.
1A	Memory Refresh line is toggling. Going to check 15 microsecond ON/OFF time.
1B	Memory Refresh period 30 microsec test complete. Base 64K memory test about to start.
20	Base 64k memory test started. Address line test to be done next.
21	Address line test passed. Going to do toggle parity.
22	Toggle parity over. Going for sequential data R/W test.
23	Base 64k sequential data R/W test passed. Setup before Interrupt vector init about to start.
24	Setup before vector initialization complete. Interrupt vector initialization about to begin.
25	Interrupt vector initialization done. Going to read I/O port of 8042 for turbo switch (if any).
26	I/O port of 8042 is read. Going to initialize global data for turbo switch.
27	Global data initialization is over. Any initialization after interrupt vector to be done next.
28	Initialization after interrupt vector is complete. Going for monochrome mode setting.
29	Monochrome mode setting is done. Going for Color mode setting.

Code	Meaning
2A	Color mode setting is done. About to go for toggle parity before optional ROM test.
2B	Toggle parity over. About to give control for any setup before optional video ROM check.
2C	Processing before video ROM control is done. About to look for optional video ROM and give control.
2D	Optional video ROM control done. About to give control to do any processing after video ROM returns control.
2E	Return from processing after the video ROM control. If EGA/VGA not found then do display memory R/W test.
2F	EGA/VGA not found. Display memory R/W test about to begin.
30	Display mem R/W test passed. About to look for retrace checking.
31	Display mem R/W test/ retrace check failed. About to do alternate Display memory R/W test.
32	Alternate Display memory R/W test passed. About to look for alternate display retrace checking.
33	Video display checking over. Verification of display with switch setting and card to begin.
34	Verification of display adapter done. Display mode to be set next.
35	Display mode set complete. BIOS ROM data area about to be checked.
36	BIOS ROM data area check over. Going to set cursor for power on message.
37	Cursor setting for power on message id complete. Going to display the power on message.
38	Power on message display complete. Going to read new cursor position.
39	New cursor position read and saved. Going to display the reference string.
3A	Reference string display is over. Going to display the Hit <Esc> message.
3B	Hit <Esc> message displayed. Virtual mode memory test about to start.
40	Preparation for virtual mode test started. Going to verify from video memory.
41	Returned after verifying from display memory. Going to prepare the descriptor tables.
42	Descriptor tables prepared. Going to enter in virtual mode for memory test.
43	Entered in the virtual mode. Going to enable interrupts for diagnostics mode.
44	Interrupts enabled (if diagnostics switch is on). Going to initialize data to check memory wrap around at 0:0.
45	Data initialized. Going to check for memory wrap around at 0:0and finding the total system memory size.
46	Memory wrap around test done. Memory size calculation over. About to go for writing patterns to test memory.
47	Pattern to be tested written in extended memory. Going to write patterns in base 640k.
48	Patterns written in base memory. Going to find out amount of memory below 1Mb.
49	Amount of memory below 1Mb found and verified. Going to find out amount of memory above 1M memory.

Code	Meaning
4A	Amount of memory above 1Mb found and verified. Going for BIOS ROM data area check.
4B	BIOS ROM data area check over. Going to check <Esc> and clear mem below 1Mb for soft reset.
4C	Memory below 1M cleared. (SOFT RESET). Going to clear memory above 1M.
4D	Memory above 1M cleared.(SOFT RESET). Going to save the memory size.
4E	Memory test started. (NO SOFT RESET). About to display the first 64k memory test.
4F	Memory size display started. This will be updated during memory test. Going for sequential and random memory test.
50	Memory test below 1Mb complete. Going to adjust memory size for relocation/ shadow.
51	Memory size adjusted due to relocation/shadow. Memory test above 1Mb to follow.
52	Memory test above 1Mb complete. Going to prepare to go back to real mode.
53	CPU registers are saved including memory size. Going to enter in real mode.
54	Shutdown successful. CPU in real mode. Going to restore registers saved during preparation for shutdown.
55	Registers restored. Going to disable gate A20 address line.
56	A20 address line disable successful. BIOS ROM data area about to be checked.
57	BIOS ROM data area check halfway. BIOS ROM data area check to be complete.
58	BIOS ROM data area check over. Going to clear Hit <Esc>message.
59	Hit <Esc> message cleared. WAIT. . . message displayed. About to start DMA and interrupt controller test.
60	DMA page register test passed. About to verify from display memory.
61	Display memory verification over. About to go for DMA #1 base register test.
62	DMA #1 base register test passed. About to go for DMA #2 base register test.
63	DMA #2 base register test passed. About to go for BIOS ROM data area check.
64	BIOS ROM data area check halfway. BIOS ROM data area check to be complete.
65	BIOS ROM data area check over. About to program DMA unit 1 and 2.
66	DMA unit 1 and 2 programming over. About to initialize 8259 interrupt controller
67	8259 initialization over. About to start keyboard test.
80	Keyboard test started. Clearing output buffer, checking for stuck key. About to issue keyboard reset
81	Keyboard reset error/stuck key found. About to issue keyboard controller i/f test command.
82	Keyboard controller interface test over. About to write command byte and init circular buffer.
83	Command byte written Global data init done. About to check for

Code	Meaning
	lock-key.
84	Lock-key checking over. About to check for memory size mismatch with CMOS.
85	Memory size check done. About to display soft error; check for password or bypass setup.
86	Password checked. About to do programming before setup.
87	Programming before setup complete. Going to CMOS setup program.
88	Returned from CMOS setup and screen cleared. About to do programming after setup.
89	Programming after setup complete. Going to display power on screen message.
8A	First screen message displayed. About to display WAIT. . . message.
8B	WAIT. . . message displayed. About to do Main and Video BIOS shadow.
8C	Main/Video BIOS shadow successful. Setup options programming after CMOS setup about to start.
8D	Setup options are programmed, mouse check and init to be done next
8E	Mouse check and initialization complete. Going for hard disk floppy reset.
8F	Floppy check returns that floppy is to be initialized. Floppy setup to follow.
90	Floppy setup is over. Test for hard disk presence to be done.
91	Hard disk presence test over. Hard disk setup to follow.
92	Hard disk setup complete. About to go for BIOS ROM data area check.
93	BIOS ROM data area check halfway. BIOS ROM data area check to be complete.
94	BIOS ROM data area check over. Going to set base and extended memory size.
95	Memory size adjusted due to mouse support hdisk type 47. Going to verify from display memory.
96	Returned after verifying from display memory. Going to do any init before C800 optional ROM control.
97	Any init before C800 optional ROM control is over. Optional ROM check and control next.
98	Optional ROM control is done. About to give control to do any required processing after optional ROM returns control.
99	Any initialization required after optional ROM test over. Going to setup timer data area and printer base address.
9A	Return after setting timer and printer base address. Going to set the RS-232 base address.
9B	Returned after RS-232 base address. Going to do any initialization before Copro test.
9C	Required initialization before coprocessor is over. Going to initialize the coprocessor next.
9D	Coprocessor initialized. Going to do any initialization after Coprocessor test.
9E	Initialization after co-pro test complete. Going to check extd keyboard; ID and num-lock.
9F	Extd keyboard check done ID flag set. num-lock on/off. Keyboard ID

Code	Meaning
	command to be issued.
A0	Keyboard ID command issued. Keyboard ID flag to be reset.
A1	Keyboard ID flag reset. Cache memory test to follow.
A2	Cache memory test over. Going to display any soft errors.
A3	Soft error display complete. Going to set the keyboard typematic rate.
A4	Keyboard typematic rate set. Going to program memory wait states.
A5	Memory wait states programming over. Screen to be cleared next.
A6	Screen cleared. Going to enable parity and NMI.
A7	NMI and parity enabled. Going to do any initialization required before giving control to optional ROM at E000.
A8	Initialization before E000 ROM control over. E000 ROM to get control next.
A9	Returned from E000 ROM control. Going to do any initialization required after E000 optional ROM control.
AA	Initialization after E000 optional ROM control is over. Going to display system configuration.
00	System configuration is displayed. Going to give control to INT 19h boot loader.

AMI New BIOS; 06/06/92-08/08/93

Code	Meaning
01	Processor register test about to start and NMI to be disabled.
02	NMI is Disabled. Power on delay starting.
03	Power on delay complete. Any initialization before keyboard BAT is in progress next.
04	Any init before keyboard BAT is complete. Reading keyboard SYS bit, to check soft reset/power on.
05	Soft reset/ power-on determined. Going to enable ROM; i.e. disable shadow RAM/Cache if any.
06	ROM is enabled. Calculating ROM BIOS checksum and waiting for 8042 keyboard controller input buffer to be free.
07	ROM BIOS checksum passed; KB controller input buffer free. Going to issue BAT command to the keyboard controller.
08	BAT command to keyboard controller is issued. Going to verify the BAT command.
09	Keyboard controller BAT result verified. Keyboard command byte to be written next.
0A	Keyboard command byte code is issued. Going to write command byte data.
0B	Keyboard controller command byte is written. Going to issue Pin-23 & 24 blocking/unblocking command.
0C	Pin-23 & 24 of keyboard controller is blocked/ unblocked. NOP command of keyboard controller to be issued next.
0D	NOP command processing is done. CMOS shutdown register test to be done next.
0E	CMOS shutdown register R/W test passed. Going to calculate CMOS checksum and update DIAG byte.
0F	CMOS checksum calculation is done; DIAG byte written. CMOS init to begin (If "INIT CMOS IN EVERY BOOT" is set).
10	CMOS initialization done (if any). CMOS status register about to init

Code	Meaning
	for Date and Time.
11	CMOS Status register initialized. Going to disable DMA and Interrupt controllers.
12	DMA controller #1 & #2, interrupt controller #1 & #2 disabled. About to disable Video display and init port-B.
13	Disable Video display and initialize port B. Chipset init/auto memory detection about to begin.
14	Chipset initialization/auto memory detection over. 8254 timer test about to start.
15	CH-2 timer test halfway. 8254 CH-2 timer test to be complete.
16	Ch-2 timer test over. 8254 CH-1 timer test to be complete.
17	CH-1 timer test over. 8254 CH-0 timer test to be complete.
18	CH-0 timer test over. About to start memory refresh.
19	Memory Refresh started. Memory Refresh test to be done next.
1A	Memory Refresh line is toggling. Going to check 15 microsecond ON/OFF time.
1B	Memory Refresh period 30 microsecond test complete. Base 64K memory test about to start.
20	Base 64k memory test started. Address line test to be done next.
21	Address line test passed. Going to do toggle parity.
22	Toggle parity over. Going for sequential data R/W test.
23	Base 64k sequential data R/W test passed. Any setup before Interrupt vector init about to start.
24	Setup required before vector initialization complete. Interrupt vector initialization about to begin.
25	Interrupt vector initialization done. Going to read I/O port of 8042 for turbo switch (if any).
26	I/O port of 8042 is read. Going to initialize global data for turbo switch.
27	Global data initialization is over. Any initialization after interrupt vector to be done next.
28	Initialization after interrupt vector is complete. Going for monochrome mode setting.
29	Monochrome mode setting is done. Going for Color mode setting.
2A	Color mode setting is done. About to go for toggle parity before optional ROM test.
2B	Toggle parity over. About to give control for any setup required before optional video ROM check.
2C	Processing before video ROM control is done. About to look for optional video ROM and give control.
2D	Optional video ROM control done. About to give control for processing after video ROM returns control.
2E	Return from processing after video ROM control. If EGA/VGA not found do display memory R/W test.
2F	EGA/VGA not found. Display memory R/W test about to begin.
30	Display memory R/W test passed. About to look for the retrace checking.
31	Display memory R/W test or retrace checking failed. About to do alternate Display memory R/W test.
32	Alternate Display memory R/W test passed. About to look for the alternate display retrace checking.
33	Video display checking over. Verification of display type with switch setting and actual card to begin.

Code	Meaning
34	Verification of display adapter done. Display mode to be set next.
35	Display mode set complete. BIOS ROM data area about to be checked.
36	BIOS ROM data area check over. Going to set cursor for power on message.
37	Cursor setting for power on message complete. Going to display power on message.
38	Power on message display complete. Going to read new cursor position.
39	New cursor position read and saved. Going to display the reference string.
3A	Reference string display over. Going to display the Hit <ESC> message.
3B	Hit <ESC> message displayed. Virtual mode memory test about to start.
40	Preparation for virtual mode test started. Going to verify from video memory.
41	Returned after verifying from display memory. Going to prepare descriptor tables.
42	Descriptor tables prepared. Going to enter in virtual mode for memory test.
43	Entered in virtual mode. Going to enable interrupts for diagnostics mode.
44	Interrupts enabled (if diags switch on). Going to initialize data to check mem wrap around at 0:0.
45	Data initialized. Going to check for memory wrap around at 0:0 and finding total memory size.
46	Mem wrap around test done. Size calculation over. About to go for writing patterns to test memory.
47	Pattern to be tested written in extended memory. Going to write patterns in base 640k memory.
48	Patterns written in base memory. Going to find out amount of memory below 1M b.
49	Amount of memory below 1Mb found and verified. Going to find amount of memory above 1Mb.
4A	Amount of memory above 1Mb found and verified. Going for BIOS ROM data area check.
4B	BIOS ROM data area check over. Going to check <ESC> and clear mem below 1 Mb for soft reset.
4C	Memory below 1Mb cleared. (SOFT RESET). Going to clear memory above 1 Mb.
4D	Memory above 1Mb cleared. (SOFT RESET). Going to save memory size.
4E	Memory test started. (NO SOFT RESET). About to display first 64K memory test.
4F	Memory size display started. This will be updated during memory test. Going for sequential and random memory test.
50	Memory test below 1Mb complete. Going to adjust memory size for relocation/shadow.
51	Memory size adjusted due to relocation/shadow. Memory test above 1Mb to follow.
52	Memory test above 1Mb complete. Preparing to go back to real mode.

Code	Meaning
53	CPU registers saved including memory size. Going to enter real mode.
54	Shutdown successful; CPU in real mode. Going to restore registers saved during prep for shutdown.
55	Registers restored. Going to disable gate A20 address line.
56	A20 address line disable successful. BIOS ROM data area about to be checked.
57	BIOS ROM data area check halfway. BIOS ROM data area check to be complete.
58	BIOS ROM data area check over. Going to clear Hit <ESC> message.
59	Hit <ESC> message cleared. <WAIT...> message displayed. About to start DMA and PIC test.
60	DMA page register test passed. About to verify from display memory.
61	Display memory verification over. About to go for DMA #1 base register test.
62	DMA #1 base register test passed. About to go for DMA #2 base register test.
63	DMA #2 base register test passed. About to go for BIOS ROM data area check.
64	BIOS ROM data area check halfway. BIOS ROM data area check to be complete.
65	BIOS ROM data area check over. About to program DMA unit 1 and 2.
66	DMA unit 1 and 2 programming over. About to initialize 8259 interrupt controller.
67	8259 initialization over. About to start keyboard test.
80	Keyboard test started. Clearing output buffer, checking for stuck key. About to issue keyboard reset.
81	Keyboard reset error/stuck key found. About to issue keyboard controller interface command.
82	Keyboard controller interface test over. About to write command byte and init circular buffer.
83	Command byte written, Global data init done. About to check for lock-key.
84	Lock-key checking over. About to check for memory size mismatch with CMOS.
85	Memory size check done. About to display soft error and check for password or bypass setup.
86	Password checked. About to do programming before setup.
87	Programming before setup complete. Going to CMOS setup program.
88	Returned from CMOS setup program, screen is cleared. About to do programming after setup.
89	Programming after setup complete. Going to display power on screen message.
8A	First screen message displayed. About to display <WAIT...> message.
8B	<WAIT...> message displayed. About to do Main and Video BIOS shadow.
8C	Main/Video BIOS shadow successful. Setup options programming after CMOS setup about to start.

Code	Meaning
8D	Setup options programmed; mouse check and initialization to be done next.
8E	Mouse check and initialization complete. Going for hard disk and floppy reset.
8F	Floppy check returns that floppy is to be initialized. Floppy setup to follow.
90	Floppy setup is over. Test for hard disk presence to be done.
91	Hard disk presence test over. Hard disk setup to follow.
92	Hard disk setup complete. About to go for BIOS ROM data area check.
93	BIOS ROM data area check halfway. BIOS ROM data area check to be complete.
94	BIOS ROM data area check over. Going to set base and extended memory size.
95	Mem size adjusted due to mouse support, hard disk type 47. Going to verify from display memory.
96	Returned after verifying from display memory. Going to do any init before C800 optional ROM control
97	Any init before C800 optional ROM control is over. Optional ROM check and control will be done next.
98	Optional ROM control is done. About to give control to do any required processing after optional ROM returns control.
99	Any init required after optional ROM test over. Going to setup timer data area and printer base address.
9A	Return after setting timer and printer base address. Going to set the RS-232 base address.
9B	Returned after RS-232 base address. Going to do any initialization before coprocessor test
9C	Required initialization before co-processor over. Going to initialize the coprocessor next.
9D	Coprocessor initialized. Going to do any initialization after coprocessor test.
9E	Initialization after coprocessor test complete. Going to check extd keyboard
	keyboard ID and num lock.
9F	Extd keyboard check is done, ID flag set. num lock on/off. Keyboard ID command to be issued.
A0	Keyboard ID command issued. Keyboard ID flag to be reset.
A1	Keyboard ID flag reset. Cache memory test to follow.
A2	Cache memory test over. Going to display soft errors.
A3	Soft error display complete. Going to set keyboard typematic rate.
A4	Keyboard typematic rate set. Going to program memory wait states.
A5	Memory wait states programming over. Screen to be cleared next.
A6	Screen cleared. Going to enable parity and NMI.
A7	NMI and parity enabled. Going to do any initi before giving control to optional ROM at E000.
A8	Initialization before E000 ROM control over. E000 ROM to get control next.
A9	Returned from E000 ROM control. Going to do any initialization after E000 optional ROM control.
AA	Initialization after E000 optional ROM control is over. Going to display the system configuration.
00	System configuration is displayed. Going to give control to INT 19h

Code	Meaning
	boot loader.

AMI WinBIOS; 12/15/93 Onwards

Code	Meaning
01	Processor register test about to start; disable NMI next.
02	NMI is Disabled. Power on delay starting.
03	Power on delay complete (to check soft reset/power-on).
05	Soft reset/power-on determined, going to enable ROM (i.e. disable shadow RAM cache, if any).
06	ROM is enabled. Calculating ROM BIOS checksum.
07	ROM BIOS checksum passed. CMOS shutdown register test to be done next.
08	CMOS shutdown register test done. CMOS checksum calculation next.
09	CMOS checksum calculation done; CMOS diag byte written; CMOS initialization to begin.
0A	CMOS initialization done (if any). CMOS status register about to init for Date and Time.
0B	CMOS status register init done. Any initialization before keyboard BAT to be done next.
0C	KB controller I/B free. Going to issue the BAT command to keyboard controller.
0D	BAT command to keyboard controller is issued. Going to verify the BAT command.
0E	Keyboard controller BAT result verified. Any initialization after KB controller BAT next.
0F	Initialization after KB controller BAT done. Keyboard command byte to be written next.
10	Keyboard controller command byte is written. Going to issue Pin-23 & 24 blocking/unblocking command.
11	Keyboard controller Pin-23 & 24 blocked/unblocked; check press of <INS> key during power-on .
12	Checking for pressing of <INS> key during power-on done. Going to disable DMA/Interrupt controllers.
13	DMA controller #1 and #2 and Interrupt controller #1 and #2 disabled; video display disabled and port B initialized; chipset init/auto memory detection next.
14	Chipset init/auto memory detection over. To uncompress the POST code if compressed BIOS.
15	POST code is uncompressed. 8254 timer test about to start.
19	8254 timer test over. About to start memory refresh test.
1A	Memory Refresh line is toggling. Going to check 15 micro second ON/OFF time.
20	Memory Refresh 30 microsecond test complete. Base 64K memory/address line test about to start.
21	Address line test passed. Going to do toggle parity.
22	Toggle parity over. Going for sequential data R/W test on base 64k memory.
23	Base 64k sequential data R/W test passed. Going to set BIOS stack and do any setup before Interrupt
24	Setup required before vector initialization complete. Interrupt vector

Code	Meaning
	initialization about to begin.
25	Interrupt vector initialization done. Going to read Input port of 9042 for turbo switch (if any) and clear password if POST diag switch is ON next.
26	Input port of 8042 is read. Going to initialize global data for turbo switch.
27	Global data initialization for turbo switch is over. Any initialization before setting video mode to be done next.
28	Initialization before setting video mode is complete. Going for mono mode and color mode setting.
2A	Monochrome and color mode setting is done. About to go for toggle parity before optional ROM test.
2B	Toggle parity over. About to give control for any setup required before optional video ROM check next.
2C	Processing before video ROM control is done. About to look for optional video ROM and give control.
2D	Optional video ROM control is done. About to give control to do any processing after video RON returns control.
2E	Return from processing after video ROM control. If EGA/VGA not found do display memory R/W test.
2F	EGA/VGA not found. Display memory R/W test about to begin.
30	Display memory R/W test passed. About to look for the retrace checking.
31	Display mem R/W test or retrace checking failed. About to do alternate Display memory R/W test.
32	Alternate Display memory R/W test passed. About to look for the alternate display retrace checking.
34	Video display checking over. Display mode to be set next.
37	Display mode set. Going to display the power on message.
39	New cursor position read and saved. Going to display the Hit <DEL> message.
3B	Hit <DEL> message displayed. Virtual mode memory test about to start.
40	Going to prepare the descriptor tables.
42	Descriptor tables prepared. Going to enter in virtual mode for memory test.
43	Entered in virtual mode. Going to enable interrupts for diagnostics mode.
44	Interrupts enabled (if diags switch is on). Going to initialize data to check memory wrap around at 0:0.
45	Data initialized. Going to check for memory wrap around at 0:0 and find total system memory size.
46	Memory wrap around test done. Memory size calculation over. About to go for writing patterns to test memory.
47	Pattern to be tested written in extended memory. Going to write patterns in base 640k memory.
48	Patterns written in base memory. Going to find amount of memory below 1Mb.
49	Amount of memory below 1Mb found and verified. Going to find out amount of memory above 1Mb memory.
4B	Amount of memory above 1Mb found and verified. Check for soft reset and going to clear memory below 1Mb for soft reset next (if power on go to POST # 4Eh).

Code	Meaning
4C	Memory below 1Mb cleared.(SOFT RESET)
4D	Memory above 1Mb cleared.(SOFT RESET); save memory size next (go to POST # 52h).
4E	Memory test started. (NOT SOFT RESET); display first 64K memory size next.
4F	Memory size display started. This will be updated during memory test; sequential and random memory test next.
50	Memory testing/initialization below 1Mb complete. Going to adjust displayed memory size for relocation/ shadow.
51	Memory size display adjusted due to relocation/ shadow. Memory test above 1Mb to follow.
52	Memory testing/initialization above 1Mb complete. Going to save memory size information.
53	Memory size information is saved. CPU registers are saved. Going to enter real mode.
54	Shutdown successful, CPU in real mode, disable gate A20 line next.
57	A20 address line disable successful. Going to adjust memory size depending on relocation/shadow.
58	Memory size adjusted for relocation/shadow. Going to clear Hit <DEL> message.
59	Hit <DEL> message cleared. <WAIT...> message displayed. About to start DMA and interrupt controller test.
60	DMA page register test passed. About to go for DMA #1 base register test.
62	DMA #1 base register test passed. About to go for DMA #2 base register test.
65	DMA #2 base register test passed. About to program DMA unit 1 and 2.
66	DMA unit 1 and 2 programming over. About to initialize 8259 interrupt controller.
67	8259 initialization over. About to start keyboard test.
F4	Extended NMI sources enabling is in progress (EISA).
80	Keyboard test started. Clear output buffer; check for stuck key; issue reset keyboard command next.
81	Keyboard reset error/stuck key found. About to issue keyboard controller interface test command.
82	Keyboard controller interface test over. About to write command byte and init circular buffer.
83	Command byte written; global data init done; check for lock-key next.
84	Lock-key checking over. About to check for memory size mismatch with CMOS.
85	Memory size check done. About to display soft error and check for password or bypass setup.
86	Password checked. About to do programming before setup.
87	Programming before setup complete. Uncompress SETUP code and execute CMOS setup.
88	Returned from CMOS setup and screen is cleared. About to do programming after setup.
89	Programming after setup complete. Going to display power on screen message.
8B	First screen msg displayed. <WAIT...> message displayed. About

Code	Meaning
	to do Main/Video BIOS shadow.
8C	Main and Video BIOS shadow successful. Setup options programming after CMOS setup about to start.
8D	Setup options are programmed; mouse check and init next.
8E	Mouse check and initialization complete. Going for hard disk controller reset.
8F	Hard disk controller reset done. Floppy setup to be done next.
91	Floppy setup complete. Hard disk setup to be done next.
94	Hard disk setup complete. Going to set base and extended memory size.
96	Memory size adjusted due to mouse support, hard disk type 47; any init before C800, optional ROM control next.
97	Init before C800 optional ROM control is over. Optional ROM check and control next.
98	Optional ROM control done. About to give control for any required processing after optional ROM returns control next.
99	Any initialization required after optional ROM test over. Going to setup timer data area and printer base address.
9A	Return after setting timer and printer base address. Going to set the RS-232 base address.
9B	Returned after RS-232 base address. Going to do any initialization before coprocessor test.
9C	Required initialization before co-processor is over. Going to initialize the coprocessor next.
9D	Coprocessor initialized. Going to do any initialization after coprocessor test.
9E	Init after coprocessor test complete. Going to check extd keyboard; keyboard ID and NumLock.
9F	Extd keyboard check is done; ID flag set; NumLock on/off, issue keyboard ID command next.
A0	Keyboard ID command issued. Keyboard ID flag to be reset.
A1	Keyboard ID flag reset. Cache memory test to follow.
A2	Cache memory test over. Going to display any soft errors.
A3	Soft error display complete. Going to set the keyboard typematic rate.
A4	Keyboard typematic rate set. Going to program memory wait states.
A5	Memory wait states programming over. Going to clear the screen and enable parity/NMI.
A7	NMI and parity enabled. Going to do any initialization required before giving control to optional ROM at E000 next.
A8	Initialization before E000 ROM control over. E000 ROM to get control next.
A9	Returned from E000 ROM control. Going to do init required.
AA	Init after E000 optional ROM control is over. Going to display the system configuration.
B0	System configuration is displayed. Going to uncompress SETUP code for hot-key setup.
B1	Uncompressing of SETUP code is complete. Going to copy any code to specific area.
00	Copying of code to specific area done. Going to give control to INT 19h boot loader.

EISA

Code	Meaning
F0	Initialization of I/O cards in slots is in progress (EISA).
F1	Extended NMI sources enabling is in progress (EISA).
F2	Extended NMI test is in progress (EISA).
F3	Display any slot initialization messages.
F4	Extended NMI sources enabling in progress.

Arche Technologies

Legacy BIOS

Derives from AMI (9 April 90), using port 80; certain codes come up if a copy is made without AMI's copyright notice. The major differences are at the end.

Code	Explanation
01	Disable NMI and test CPU registers
02	Verify ROM BIOS checksum (32K at F800:0)
03	Initial keyboard controller and CMOS RAM communication
04	Disable DMA and interrupt controllers; test CMOS RAM interrupt
05	Reset Video
06	Test 8254 timer
07	Test delta count for timer channel 2 (speaker)
08	Test delta count for timer channel 1 (memory refresh)
09	Test delta count for timer channel 0 (system timer)
0A	Test parity circuit and turn on refresh
0B	Enable parity check circuit and test system timer
0C	Test refresh trace link toggle
0D	Test refresh timing synchronization of high and low period
10	Disable cache and shadow BIOS; test 64K base memory address lines
11	Test base 64K memory for random addresses and data read/write
12	Initialize interrupt vectors in lower 1K of RAM
14	Test CMOS RAM shutdown register read/write; disable DMA and interrupt controllers
15	Test CMOS RAM battery and checksum, and different options such as diagnostic byte
16	Test floppy information in CMOS RAM; initialize monochrome video
17	Initialize color video
18	Clear parity status if any
19	Test for EGA/VGA video ROM BIOS at C000:0 and pass control to it if there
1A	Returned from video ROM. Clear parity status if any; update system parameters for any video ROM found; test display memory read/write
1B	Primary video adapter: check vertical and horizontal retrace; write/read test video memory
1C	Secondary video adapter: check vertical and horizontal retrace; write/read test video memory
1D	Compare and verify CMOS RAM video type with switches and actual

Code	Explanation
	video adapter; set equipment byte if correct
1E	Call BIOS to set mono/color video mode according to CMOS RAM
20	Display CMOS RAM write/read errors and halt if any
21	Set cursor to next line and call INT 10 to display
22	Display Power on "386 BIOS" message and check CPU speed is 25 or 33 MHz
23	Read new cursor position and call INT 10 to display
24	Skip 2 rows of text and display (C)AMI at bottom of screen
25	Refresh is off, so call shadow RAM test
F0	Failure inside shadow RAM test
30	Verify (C)AMI... and overwrite with blanks before entering protected mode
31	Enter protected mode and enable timer interrupt (IRQ0). Errors here indicate gate A20 circuit failed
32	Size memory above 1Mb
33	Size memory below 640K
34	Test memory above 1Mb
35	Test memory below 1Mb
36	Unknown AMI function
37	Clear memory below 1Mb
38	Clear memory above 1Mb
39	Set CMOS shutdown byte to 3 and go back to real mode
3A	Test sequential and random data write/read of base 64K RAM
3B	Test RAM below 1Mb and display area being tested
3C	Test RAM above 1Mb and display area being tested
3D	RAM test OK
3E	Shutdown for return to real mode
3F	Back in real mode; restore all variables
40	Disable gate A20 since now in real mode
41	Check for (C)AMI in ROM
42	Display (C)AMI message
43	Clear <Esc> message; test cache
4E	Process shutdown 1; go back to real mode
4F	Restore interrupt vectors and global data in BIOS RAM area
50	Test 8237 DMA controller and verify (c)AMI in ROM
51	Initialize DMA controller
52	Test various patterns to DMA controller
53	Verify (C)AMI in ROM
54	Test DMA control flip-flop
55	Initialize and enable DMA controllers 1 and 2
56	Initialize 8259 interrupt controllers—clear write request and mask registers
57	Test 8259 controllers and setup interrupt mask registers
61	Check DDNIL status bit and display message if clear
70	Perform keyboard BAT (Basic Assurance Test)
71	Program keyboard to AT type
72	Disable keyboard and initialize keyboard circular buffer
73	Display "DEL" message for setup prompt and initialize floppy controller/drive
74	Attempt to access floppy drive
75	If CMOS RAM is good, check and initialize hard disk type identified in CMOS RAM

Code	Explanation
76	Attempt to access hard disk and set up hard disk
77	Shuffle any internal error codes
78	Verify (C)AMI is in ROM
79	Check CMOS RAM battery and checksum; clear parity status
7A	Compare size of base/extended memory to CMOS RAM info
7B	Unknown AMI function
7C	Display (C)AMI
7D	Set/reset AT compatible memory expansion bit
7E	Verify (C)AMI is in ROM
7F	Clear <DEL> message from screen and check if DEL pressed
80	Find option ROM in C800 to DE00 and pass control to any found
81	Return from adapter ROM; initialize timer and data area
82	Setup parallel and serial port base info in global data area
83	Test for presence of 80387 numeric coprocessor and initialize
84	Check lock key for keyboard
85	Display soft error messages if any CMOS RAM data error was detected such as battery or checksum
86	Test for option ROM in E000:0 and pass control to any found
A0	Error in 256 Kbit or 1Mbit RAM chip in lower 640K memory
A1	Base 64K random address/data pattern test (only in 386APR and Presto 386SX BIOS)
A9	Initialize on-board VGA (Presto 386SX)
B0	Error in 256 Kbit RAM chip in lower 640K memory
B1	Base 64K random address/data pattern test (only in Presto 386SX BIOS)
E0	Returned to real mode; initialize base 64K RAM (Presto)
E1	initialize base 640K RAM (Presto)
EF	Configuration memory error in Presto -can't find memory
F0	Test shadow RAM from 0:4000 RAM area
00	Call INT 19 boot loader

AST

See also *Phoenix* or *Award*. AST introduced an enhanced BIOS in 1992 with 3 beeps before all early POST failure messages, for Field Replaceable Unit identification. Otherwise, the most significant (left) digit of the POST code indicates the number of long beeps, and the least significant (right) digit indicates the short beeps. 17 therefore means 1 long beep and 7 short. Doesn't work after 20.

Early POST Codes

These are usually fatal and accompanied by a beep code:

Code	Meaning
1	System Board
2	SIMM Memory; System Board
3	SIMM Memory; System Board
4	SIMM Memory; System Board
5	Processor; System Board
6	Keyboard Controller; System Board

Code	Meaning
7	Processor; System Board
8	Video Adapter; Video RAM; System Board
9	BIOS; System Board
10	System Board
11	External cache; System Board

Code	Meaning
00	Reserved
	Beep and Halt if Error occurs
01	Test CPU registers and functionality
02	Test empty 8042 keyboard controller buffer
03	Test 8042 keyboard controller reset
04	Verify keyboard ID and low-level keyboard communication
05	Read keyboard input port (WS386SX16 only)
06	Initialize system board support chipset
09	Test BIOS ROM checksum; flush external cache
0D	Test 8254 timer registers (13 short beeps)
0E	Test ASIC registers (CLEM only, 14 short beeps)
0F	Test CMOS RAM shutdown byte (15 short beeps)
10	Test DMA controller 0 registers
11	Test DMA controller 1 registers
12	Test DMA page registers (see code 17)
13	see code 17
14	Test memory refresh toggle (see code l7)
15	Test base 64K memory
16	Set interrupt vectors in base memory
17	Initialize video; if EGA/VGA, issue code 12-13 if error, but only use this POST code beep pattern
12	EGA/VGA vertical retrace failed (different from normal beep)
13	EGA/VGA RAM test failed (different than normal beep tone)
14	EGA/VGA CRT registers failed (different than normal beep)
18	Test display memory
	Don't beep and don't halt if error occurs
20	EISA bus board power up (EISA Systems only)
30	Test interrupt controller #1 mask register
31	Test interrupt controller #2 mask register
32	Test interrupt controllers for stuck interrupt
33	Test for stuck NMI (P386 25/33, P486, CLEM and EISA)
34	Test for stuck DDNIL status bit (CLEM only)
40	Test CMOS RAM backup battery
41	Calculate and verify CMOS RAM checksum
42	Setup CMOS RAM options (except WS386SX16)
50	Test protected mode
51	Test protected mode exceptions
60	Calculate RAM size
61	Test RAM
62	Test shadow RAM (WS386SXI6, P386 25/33, P486, CLEM, EISA), or test cache (P386/I6)
63	Test cache (P38625/33, P486, CLEM, EISA), or copy system BIOS to shadow RAM (P386C, P386/I6, WS386SX16)

Code	Meaning
64	Copy system BIOS to shadow RAM (P386 25/33, P486, CLEM, EISA), or copy video BIOS to shadow RAM (P38616, SW386SX16)
65	Copy video BIOS to shadow RAM (P386 25/33, P486, CLEM, EISA), or test cache (WS386SX16)
66	Test 8254 timer channel 2 (P386 25/33, P486, EISA)
67	Initialize memory (Eagle only)

AT&T

Either Phoenix or Olivetti BIOS. See Olivetti M24 for early 6300 series motherboards., and Phoenix for later ones with Intel motherboards. After 1991 see NCR.

Award

The general procedures below are valid for greater than XT v3.0 and AT v3.02-4.2.The sequence may vary slightly between versions.

Award Test Sequence—up to v4.2

Procedure	Meaning
CPU	BIOS sets verifies and resets the error flags in the CPU (i.e. carry; sign; zero; stack overflow). Failure here is normally due to the CPU or system clock.
POST Determination	BIOS determines whether motherboard is set for normal operation or a continuous loop of POST (for testing). If the POST test is cycled 1-5 times over and over either the jumper for this function is set to burn-in or the circuitry involved has failed.
Keyboard Controller	BIOS tests the internal operations of the keyboard controller chip (8042). Failure here is normally due to the keyboard chip.
Burn In Status	1-5 will repeat if the motherboard is set to burn in (you will see the reset light on all the time). If you haven't set the board for burn-in mode, there is a short in the circuitry.
Initialize Chipset	BIOS clears all DMA registers and CMOS status bytes 0E & 0F. BIOS then initializes 8254 (timer). Failure of this test is probably due to the timer chip.
CPU	A bit-pattern is used to verify the functioning of the CPU registers. Failure here is normally down to the CPU or clock chip.
RTC	BIOS verifies that that the real time clock is updating CMOS at normal intervals. Failure is normally the CMOS/RTC or the battery.
ROM BIOS Checksum	BIOS performs a checksum of itself against a predetermined value that will equal 00. Failure is down to the ROM BIOS.
Initialize Video	BIOS tests and initializes the video controller. Failure is normally the video controller (6845) or an improper setting of the motherboard or CMOS.

Procedure	Meaning
PIT	BIOS tests the functionality of channels 0 1 2 in sequence. Failure is normally the PIT chip (8254/53).
CMOS Status	Walking-bit pattern tests CMOS shutdown status byte 0F. Failure normally in CMOS.
Extended CMOS	BIOS checks for any extended information of the chipset and stores it in the extended RAM area. Failure is normally due to invalid information and can be corrected by setting CMOS defaults. Further failure indicates either the chipset or the CMOS RAM.
DMA	Channels 0 and 1 are tested together with the page registers of the DMA controller chip(s)—8237. Failure is normally due to the DMA chips.
Keyboard	The 8042 keyboard controller is tested for functionality and for proper interfacing functions. Failure is normally due to the 8042 chip.
Refresh	Memory refresh is tested; the standard refresh period is 120-140 ns. Failure is normally the PIT chip in ATs or the DMA chip in XTs.
Memory	The first 64K of memory is tested with walking-bit patterns. Failure is normally due to the first bank of RAM or a data line.
Interrupt Vectors	The BIOS interrupt vector table is loaded to the first bank of RAM. Failure here is not likely since memory in this area has been tested. If a failure does occur suspect the BIOS or the PIC.
Video ROM	Video ROM is initialized which performs an internal diagnostic before returning control to the System BIOS. Failure is normally the video adapter or the BIOS.
Video Memory	This is tested with a bit-pattern. This is bypassed if there is a ROM on the video adapter. Failure is normally down to the memory on the adapter.
PIC	The functionality of the interrupt controller chip(s) is tested (8259). Failure is normally down to the 8259 chips but may be the clock.
CMOS Battery	BIOS verifies that CMOS byte 0D is set which indicates the CMOS battery power. Suspect the battery first and the CMOS second.
CMOS Checksum	A checksum is performed on the CMOS. Failure is either incorrect setup or CMOS chip or battery. If the test is passed the information is used to configure the system.
Determine System Memory	Memory up to 640K is addressed in 64K blocks. Failure is normally due to an address line or DMA chip. If all of the memory is not found there is a bad RAM chip or address line in the 64K block above the amount found.
Memory Test	Tests are performed on any memory found and there will normally be a message with the hex address of any failing bit displayed at the end of boot.
PIC	Further testing is done on the 8259 chips.
CPU protected mode	Processor is placed into protected mode and back into real mode; the 8042 is used for this. In case of failure suspect the 8042; CPU; CMOS; or BIOS in that order.
Determine Extended Memory	Memory above 1 Mb is addressed in 64K blocks. The entire block will be inactive if there is a bad RAM chip on a block.

Procedure	Meaning
Test Extended Memory	Extended memory is tested with a series of patterns. Failure is normally down to a RAM chip, and the hex address of the failed bit should be displayed.
Unexpected Exceptions	BIOS checks for unexpected exceptions in protected mode. Failure is likely to be a TSR or intermittent RAM failure.
Shadow/Cache	Shadow RAM and cache is activated; failure may be due to the cache controller or chips. Check the CMOS first for invalid information.
8242 Detection	BIOS checks for an Intel 8242 keyboard controller and initializes it if found. Failure may be due to an improper jumper setting or the 8242.
Initialize Keyboard	Failure could be the keyboard or the controller.
Initialize Floppy	All those set in the CMOS. Failure could be incorrect CMOS setup or floppy controller or the drive.
Detect Serial Ports	BIOS searches for and initializes up to four serial ports at 3F8/2F8/3E8 and 2E8. Detection failure is normally due to an incorrect jumper setting somewhere or an adapter failure.
Detect Parallel Ports	BIOS searches for and initializes up to four parallel ports at 378/3BC and 278. Detection failure is normally due to an incorrect jumper setting somewhere or an adapter failure.
Initialize Hard Drive	BIOS initializes any hard drive set in CMOS. Failure could be due to invalid CMOS setup, hard drive or controller.
Detect NPU Coprocessor	Initialization of any NPU Coprocessor found. Failure is due to either an invalid CMOS setup or the NPU is failing.
Initialize Adapter ROM	Any adapter ROMs between C800 and EFFF are initialized. The ROM will do an internal test before giving back control to the System ROM. Failure is normally due to the adapter ROM or the attached hardware.
Initialize External Cache	Any cache external to the 486 is enabled. Failure would indicate invalid CMOS setup, cache controller or chips.
NMI Unexpected Exceptions	A final check for unexpected exceptions before giving control to the Int 19 boot loader. Failure is normally due to a memory parity error or an adapter.
Boot Errors	Failure when the BIOS attempts to boot off the default drive set in CMOS is normally due to an invalid CMOS drive setup or as given by an error message. If the system hangs there is an error in the Master Boot Record or the Volume Boot Record.

Award Test Sequence—after v4.2 (386/486)

Procedure	Meaning
CPU	BIOS sets verifies and resets the error flags in the CPU then performs a register test by writing and reading bit patterns. Failure is normally due to the CPU or clock chip.
Initialize Support Chips	Video is disabled as is parity/DMA and NMI. Then the PIT/PIC and DMA chips are initialized. Failure is normally down to the PIT or DMA chips.
Init Keyboard	Keyboard and Controller are initialized.
ROM BIOS Test	A checksum is performed by the ROM BIOS on the data

Procedure	Meaning
	within itself and is compared to a preset value of 00. Failure is normally due to the ROM BIOS.
CMOS Test	A test of the CMOS chip which should also detect a bad battery. Failure is due to either the CMOS chip or the battery.
Memory Test	First 356K of memory tested with any routines in the chipsets. Failure normally due to defective memory.
Cache Initialization	Any cache external to the chipset is activated. Failure is normally due to the cache controller or chips.
Initialize Vector Table	Interrupt vectors are initialized and the interrupt table is installed into low memory. Failure is normally down to the BIOS or low memory.
CMOS RAM	CMOS RAM checksum tested, BIOS defaults loaded if invalid. Check CMOS RAM.
Keyboard Init	Keyboard initialized and Num Lock set On. Check the keyboard or controller.
Video Test	Video adapter tested and initialized.
Video Memory	Tested on Mono and CGA adapters. Check the adapter card.
DMA Test	DMA controllers and page registers are tested. Check the DMA chips.
PIC Tests	8259 PIC chips are tested.
EISA Mode Test	A checksum is performed on the extended data area of CMOS where EISA information is stored. If passed the EISA adapter is initialized.
Enable Slots	Slots 0-15 for EISA adapters are enabled if the above test is passed.
Memory Size	Memory addresses above 265K written to in 64K blocks and addresses found are initialized. If a bit is bad, entire block containing it and those above will not be seen
Memory Test	Read/Write tests performed to memory over 256K; failure due to bad bit in RAM.
EISA Memory	Memory tests on any adapters initialized previously. Check the memory chips.
Mouse Initialization	Checks for a mouse and installs the appropriate interrupt vectors if one is found. Check the mouse adapter if you get a problem.
Cache Init	The cache controller is initialized if present.
Shadow RAM Setup	Any Shadow RAM present according to the CMOS Setup is enabled.
Floppy Test	Test and initialize floppy controller and drive.
Hard Drive Test	Test and initialize hard disk controller and drive. You may have an improper setup or a bad controller or hard drive.
Serial/Parallel	Any serial/parallel ports found at the proper locations are initialized.
Maths Copro	Initialized if found. Check the CMOS Setup or the chip.
Boot Speed	Set the default speed at which the computer boots.
POST Loop	Reboot occurs if the loop pin is set; for manufacturing purposes.
Security	Ask for password if one has been installed. If not check the CMOS data or the chip.
Write CMOS	The BIOS is waiting to write the CMOS values from Setup to CMOS RAM. Failure is normally due to an invalid

Procedure	Meaning
	CMOS configuration.
Pre-Boot	BIOS is waiting to write the CMOS values from Setup to CMOS RAM.
Adapter ROM Initialize	Adapter ROMs between C800 and EFFF are initialized. The ROM will do an internal test before giving back control to the System ROM. Failure is normally due to the adapter ROM or the attached hardware.
Set Up Time	Set CMOS time to the value located at 40h of the BIOS data area.
Boot System	Control is given to the Int 19 boot loader.

3.Ox

Uses IBM beep patterns. Version 3.xx sends codes 1-24 to port 80 and 300 and the system hangs up. Afterwards, codes are sent to the POST port and screen without hanging up.

Code	Meaning
01	CPU test 1: verify CPU status bits
02	Powerup check—Wait for chips to come up; initialize motherboard and chipset (if present) with defaults. Read 8042 status and fail if its input buffer contains data but output buffer does not.
03	Clear 8042 Keyboard interface—send self-test command AA, fail if status not 2 output buffer full.
04	Reset 8042 Keyboard controller—fail if no data input (status not equal 1) within a million tries, or if input data is not 55 in response to POST 03.
05	Get 8042 manufacturing status—read video type and POST type bits from 8042 discrete input port; test for POST type = manufacturing test or normal; fail if no response from 8042.
06	Initialize on-board chips—disable color & mono video, parity, and 8237 DMA; reset 80x87 math chip, initialize 8255 timer 1, clear DMA chip and page registers and CMOS RAM shutdown byte: initialize motherboard chipset if present.
07	CPU test 2: read/write/verify registers except SS, SP, BP with FF and 00 data
08	Initialize CMOS RAM/RTC chip—update timer cycle normally; disable PIE, AIE, UIE and square wave. Set BCD date and 24-hour mode.
09	Checksum 32K of BIOS ROM; fail if not 0
0A	Initialize video interface—read video type from 8042 discrete input port. Fail if can't read it. Initialize 6845 controller register at either color or mono adapter port to 80 columns, 25 rows, 8/14 scan lines per row, cursor lines at 6/11 (first) & 7/12 (last), offset to 0.
0B	Test 8254 timer channel 0- this test is skipped; already initialized for mode 3.
0C	Test 8254 timer channel 1—this test is skipped; already initialized for mode 0.
0D	Test 8254 timer channel 2—write/read/verify FF, then 00 to timer registers; initialize with 500h for normal operation.
0E	Test CMOS RAM shutdown byte (3.03: CMOS date and timer—this test is skipped and its functions performed
0F	Test extended CMOS RAM if present (3.03: test CMOS shutdown

Code	Meaning
	byte—write/read/verify a walk-to-left I pattern at CMOS RAM address 8F)
10	Test 8237 DMA controller ch 0—write/read/verify pattern AA, 55, FF and 00.
11	Test 8237 DMA controller ch 1—write/read/verify pattern AA, 55, FF and 00.
12	Test 8237 DMA controller page registers—write/read/verify pattern AA, 55, FF and 00: use port addresses to check out address circuitry to select page registers. At this point, POST enables user reboot.
13	Test 8741 keyboard controller interface—read 8042 status, verify buffers are empty, send AA self-test command, verify 55 response, send 8741 write command to 8042, wait for 8042 acknowledgement, send 44 data for 8741 (keyboard enabled, system flag, AT interface), wait for ack, send keyboard disable command, wait for ack. Fail if no ack or improper responses.
14	Test memory refresh toggle circuits—fail if not toggling high and low.
15	Test first 64K of base system memory—disable parity checking, zero all of memory, 64K at a time, to clear parity errors, enable parity checking, write/read/verify 00, 5A, FF and A5 at each address.
16	Set up interrupt vector tables in low memory.
17	Set up video I/O operations—read 8042 (motherboard switch or jumper) to find whether color or mono adapter installed; validate by writing a pattern to mono memory B0000 and select mono I/O port if OK or color if not, and initialize it via setting up the hardware byte and issuing INT 10. Then search for special video adapter BIOS ROM at C0000 (EGA/VGA), and call it to initialize if found. Fail if no 8042 response.
18, 1 beep	Test MDA/CGA video memory unless EGA/VGA adapter is found—disable video, detect mono video RAM at B0000 or color at B8000, write/read/verify test it with pattern A5A5, fill it with normal attribute, enable the video card. No error halt unless enabled by CMOS. Beep once to let user know first phase of testing is complete. From now on, POST will display test and error messages on the screen.
19	Test 8259 PIC mask bits, channel 1—write/read/verify 00 to mask register.
1A	Test 8259 PIC mask bits, channel 2—write/read/verify 00 to mask register.
1B	Test CMOS RAM battery level—poll CMOS RTC/RAM chip for battery level status. Display error if level is low, but do not halt.
1C	Test CMOS RAM checksum—check CMOS RAM battery level again, calculate checksum of normal and extended CMOS RAM. Halt if low battery or checksum not 0; otherwise reinitialize motherboard chipset if necessary.
1D	Set system memory size parameters from CMOS RAM data, Cannot fail.
1E	Size base memory 64K at a time, and save in CMOS RAM. Cannot fail, but saves diagnostic byte in CMOS RAM if different from size in CMOS.
1F	Test base memory found from 64K to 640K—write/read/verify FFAA and 5500 patterns by byte. Display shows failing address and data.
20	Test stuck bits in 8259 PICs
21	Test for stuck NMI bits (parity /I0 check)
22	Test 8259 PIC interrupt functionality—set up counter timer 0 to count down and issue an interrupt on IRQ8. Fail if interrupt does not occur.

Code	Meaning
23	Test protected mode, A20 gate. and (386 only) virtual 86 & 8086 page mode.
24	Size extended memory above 1Mb; save size into CMOS RAM. Cannot fail, but saves diagnostic byte in CMOS RAM if different from size in CMOS.
25	Test all base and extended memory found (except the first 64K) up to 16 Mb. Disable parity check but monitor for parity errors. Write/read/verify AA55 then 55AA pattern 64K at a time. On 386 systems use virtual 8086 mode paging system. Displays actual and expected data and failing address.
26	Test protected mode exceptions—creates the circumstances to cause exceptions and verifies they happen; out-of-bounds instruction, invalid opcode, invalid TSS (JMP, CALL, IRET, INT), segment not present on segment register instruction, generate memory reference fault by writing to a read-only segment.
27	Initialize shadow RAM and move system BIOS and/or video BIOS into it if enabled by CMOS RAM setup. Also (386 only) initialize the cache controller if present in system. This is not implemented in some versions of 3.03
28	Detect and initialize Intel 8242/8248 chip (not implemented in 3.03)
29	Reserved
2A	Initialize keyboard
2B	Detect and initialize floppy drive
2C	Detect and initialize serial ports
2D	Detect and initialize parallel ports
2E	Detect and initialize hard drive
2F	Detect and initialize math coprocessor
30	Reserved
31	Detect and initialize adapter ROMs
BD	Initialize Orvonton cache controller if present
CA	Initialize 386 Micronics cache if present
CC	Shutdown NMI handler
EE	Test for unexpected processor exception
FF	INT 19 boot

3.00—3.03 8/26/87

Code	Meaning
01	Processor test part 1; Processor status verification. Tests following CPU status flags: set/clear carry zero sign and overflow (fatal). Output: infinite loop if failed; continue test if OK. Registers: AX/BP.
02	Determine type of POST test. Manufacturing (e.g. 01-05 in loop) or normal (boot when POST finished). Fails if keyboard interface buffer filled with data. Output: infinite loop if failed; continue test if OK. Registers: AX/BX/BP.
03	Clear 8042 keyboard interface. Send verify TEST_KBRD command (AAh). Output: infinite loop if failed; continue test if OK. Registers: AX/BX/BP.
04	Reset 8042 keyboard controller. Verify AAh return from 03. Infinite loop if test fails. Registers: AX/BX/BP.
05	Get 8042 keyboard controller manufacturing status. Read input port via keyboard controller to determine manufacturing or normal mode

Code	Meaning
	operation. Reset system if manufacturing status from 02. Output: infinite loop if failed; continue test if OK. Registers: AX/BX/BP.
06	Init chips on board LSI chips. Disable color/mono video; parity and DMA (8237A). Reset coprocessor; initialize (8254) timer 1; clear DMA page registers and CMOS shutdown byte.
07	Processor test #2. read/write verify SS/SP/BP registers with FFh and 00h data pattern.
08	Initialize CMOS chip
09	EPROM checksum for 32 Kbytes
0A	Initialize video interface
0B	Test 8254 channel 0
0C	Test 8254 channel 1
0D	Test 8254 channel 2
0E	Test CMOS date and timer
0F	Test CMOS shutdown byte
10	Test DMA channel 0
11	Test DMA channel 1
12	Test DMA page registers
13	Test 8741 keyboard controller
14	Test memory refresh toggle circuits
15	Test 1st 64k bytes of system memory
16	Setup interrupt vector table
17	Setup video I/O operations
18	Test video memory
19	Test 8259 channel 1 mask bits
1A	Test 8259 channel 2 mask bits
1B	Test CMOS battery level
1C	Test CMOS checksum
1D	Setup configuration byte from CMOS
1E	Sizing system memory & compare w/CMOS
1F	Test found system memory
20	Test stuck 8259'S interrupt bits
21	Test stuck NMI (parity/IO chk) bits
22	Test 8259 interrupt functionality
23	Test protected mode and A20 gate
24	Sizing extended memory above 1MB
25	Test found system/extended memory
26	Test exceptions in protected mode
27	Reserved

286 N3.03 Extensions

Code	Meaning
2A	POST_KEYBOARD present during reset keyboard before boot has no relationship to POST 19.
2B	POST_FLOPPY present during init of floppy controller and drive(s)
2C	POST_COMM present during init of serial cards.
2D	POST_PRN present during init of parallel cards
2E	POST_DISK present during init of hard disk controller and drive(s)
2F	POST_MATH present during init of math coprocessor. Result remains after DOS boot; left on the port 80 display

Code	Meaning
30	POST_EXCEPTION present during protected mode access or when processor exceptions occur. A failure indicates that protected mode return was not possible
CC	POST_NMI present when selecting the F2 system halt option

XT 8088/86 BIOS v3.1

Code	Meaning
01	Processor test 1; processor status verification
02	Determine type of POST test. Failed if keyboard interface buffer filled with data.
06	Init 8259 PIC and 8237 DMA controller chips. Disable color and mono video, parity circuits and DMA chips. Reset math coprocessor. Initialize 8253 Timer channel 1. Clear DMA chip and page registers.
07	Processor test #2. Write, read and verify all registers except SS, SP and BP with data patterns 00 and FF.
09	EPROM checksum for 32 Kbytes
0A	Initialize video controller 6845 registers as follows: 25 lines x 80 columns, first cursor scan line at 6/11 and last at 7/12, reset display offset to 0.
15	Test 1st 64K of system memory
16	Setup interrupt vector table in 1st 64K
17	Setup video I/O operations
18	Test video memory
19	Test 8259 channel 1 mask bits
1A	Test 8259 channel 2 mask bits
1D	Setup configuration byte from CMOS
1E	Sizing system memory & compare w/CMOS
1F	Test found system memory
20	Test stuck 8259's interrupt bits
21	Test stuck NMI (parity/IO chk) bits
22	Test 8259 interrupt functionality
2A	Initialize keyboard
2B	Initialize floppy controller and drive
2C	Initialize COM ports
2D	Initialized LPT ports
2F	Initialize maths coprocessor
31	Initialize option ROMs
FF	Int 19 Boot attempt

Modular (386) BIOS v3.1

Also for PC/XT v3.0+ and AT v3.02+. Tests do not necessarily execute in numerical order.

Code	Meaning
01	Processor test part 1. Processor status verification. Tests the following processor-status flags: set/clear carry; zero; sign and overflow (fatal). BIOS sets each flag; verifies they are set and turns each flag off verifying its state. Failure of a flag means a fatal error. Output: infinite loop if failed; continue test if OK. Registers: AX/BP.

Code	Meaning
02	Determine POST type; whether normal (boot when POST finished) or manufacturing (run 01-05 in loop) which is often set by a jumper on some motherboards. Fails if keyboard interface buffer filled with data. Output: infinite loop if failed; continue test if OK. Registers: AX/BX/BP.
03	Clear 8042 keyboard interface. Send verify TEST_KBRD command (AAh). Output: infinite loop if failed; continue test if OK. Registers: AX/BX/BP.
04	Reset 8042 keyboard controller. Verify AAh return from 03. Infinite loop if test fails. Registers: AX/BX/BP.
05	Get 8042 keyboard controller manufacturing status; read input port via keyboard controller to determine manufacturing or normal mode operation. Reset system if manufacturing; i.e. if 02 found the status to be Manufacturing triggers a reset and 01-05 are repeated continuously. Output: infinite loop if failed; continue test if OK. Registers: AX/BX/BP.
06	Initialize chips on board LSI chips. Disables color and mono video/parity circuits/DMA (8237) chips; resets maths coprocessor; initializes timer 1 (8255); clears DMA chip and all page registers and the CMOS shutdown byte.
07	Processor Test 2. Reads writes and verifies all CPU registers except SS/SP/BP with data pattern FF and 00.
08	Initializes CMOS timer/RTC and updates timer cycle; normally CMOS (8254) timer; (8237A) DMA; (8259) interrupt and EPROM.
09	EPROM Checksum; test fails if not equal to 0. Also checksums sign-on message.
0A	Initialize Video Interface; specifically register 6845 to 80 characters per row and 25 rows per screen and 8/14 scan lines per row for mono/color; first scan line of cursor 6/11; last scan line of cursor 7/12; reset display offset to 0.
0B	Test Timer (8254) Channel 0. See also below.
0C	Test Timer (8254) Channel 1.
0D	Test Timer (8254) Channel 2.
0E	Test CMOS Shutdown Byte using a walking-bit algorithm.
0F	Test Extended CMOS. On motherboards supporting extended CMOS configuration such as C & T the BIOS tables of CMOS information configure the chipset which has an extended storage facility enabling you to keep the configuration with the power off. A checksum is used for verification.
10	Test DMA Channel 0. This and the next two tests initialize the DMA chip and test it with an AA/55/FF/00 pattern. Port addresses are used to check the address circuit to DMA page circuit registers.
11	DMA Channel 1
12	DMA Page Registers
13	Test keyboard controller interface.
14	Test memory refresh toggle circuits.
15	First 64K of system memory which is used by the BIOS; an extensive parity test.
16	Interrupt Vector Table. Sets up and loads interrupt vector tables in memory for the 8259 PIC.
17	Video I/O operations. Initializes the video; EGA and VGA ROMs are used if present.
18	Video memory test for CGA and mono cards (EGA and VGA have their own procedures).

Code	Meaning
19	Test 8259 mask bits—Channel 1.Interrupt lines turned alternately off and on. Failure is fatal.
1A	8259 Mask Bits—Channel 2
1B	CMOS battery level; verifies battery status bit set to 1. 0 could indicate bad battery at CMOS.
1C	Tests the CMOS checksum data at 2E and 2Fh and extended CMOS checksum if present.
1D	Configuration of the system from CMOS values if the checksum is good.
1E	System memory size is determined by writing to addresses from 0-640K continuing till there is no response. The size is then compared to the CMOS and a flag set if they do not compare. An error message will then be displayed.
1F	Tests memory from the top of 64K to the top of memory found by writing patterns FFAA and 5500 and reading them back byte by byte for verification
20	Stuck 8259 Interrupt Bits.
21	Stuck NMI bits (parity or I/O channel check).
22	8259 function.
23	Verifies protected mode; 8086 virtual and page mode.
24	As for 1E but for extended memory from 1-16Mb on 286/386SX systems and 64 Mb on 386s and above. The value found is compared to the CMOS settings.
25	Tests extended memory found above using virtual 8086 paging mode and writing an FFFF/AA55/0000 pattern.
26	Protected Mode Exceptions; tests other aspects of protected mode operations.
27	Tests cache control (386/486) or Shadow RAM. Systems with CGA and MDA indicate that video shadow RAM is enabled even though there is no BIOS ROM to shadow.
28	Set up cache controller or 8242 keyboard controller. Optional Intel 8242/8248 keyboard controller detection and support.
29	Reserved.
2A	Initialize keyboard and controller.
2B	Initialize floppy drive(s) and controller.
2C	Detect and initialize serial ports.
2D	Detect and initialize parallel ports.
2E	Initialize hard drive and controller.
2F	Detect and initialize math coprocessor.
30	Reserved.
31	Detect and initialize option ROMs. Initializes any between C800-EFFF.
3B	Initialize secondary cache with OPTi chipset (486 only).
CC	NMI Handler Shutdown. Detects untrapped NMIs during boot.
EE	Unexpected Processor Exception.
FF	Boot Attempt; if POST is complete and all components are initialized with no errors.

ISA/EISA BIOS v4.0

EISA codes may be sent to 300h.

Code	Meaning
01	Processor test 1: Verify CPU status flags—set, test, clear, and test the carry, zero, sign, overflow flags (fatal)
02	Processor test 2: Write/read/verify all CPU registers, except SS, SP and BP with data patterns FF and 00.
03	Calculate BIOS EPROM and sign-on message checksum; fail if not 0
04	Test CMOS RAM interface and verify battery power Is available.
05	Initialize chips: Disable NMI, PIE, AIE, UEI, SQWV; disable video, parity checking, and DMA: reset math coprocessor, clear all page registers and CMOS RAM shutdown byte: Initialize timers 0, 1 and 2, and set EISA timer to a known state: initialize DMA controllers 0 and 1: initialize interrupt controllers 0 and 1; initialize EISA extended registers.
06	Test memory refresh toggle to ensure memory chips can retain data.
07	Set up low memory; Initialize chipset early; test presence of memory; run OEM chipset initialization routines, clear lower 256K of memory; enable parity checking and test parity in lower 256K; test lower 256K memory.
08	Setup interrupt vector table; initialize first 120 interrupt vectors with SPURlOUS_INT_HDLR and initialize INT 00-1F according to INT_TBL.
09	Test CMOS RAM checksum and load default; if checksum is bad.
0A	Initialize keyboard; detect type of keyboard controller (optional); set NUMLOCK status.
0B	Initialize video interface; read CMOS RAM location 14 to find out type of video in use; detect and initialize the video adapter.
0C	Test video memory; write signon message to screen.
0D	OEM specific—initialize motherboard special chips as required by OEM; initialize cache controller early, when cache is separate from chipset.
0E	Reserved.
0F	Test DMA controller 0 with AA, 55, FF, 00 pattern.
10	Test DMA controller 1 with AA, 55, FF, 00 pattern.
11	DMA page registers—use 1/O ports to test address circuits.
12-13	Reserved
14	Test 3254 timer 0 counter 2.
15	Verify 8259 interrupt controller channel 1 by toggling interrupt lines off/on.
16	Verify 8259 interrupt controller channel 2 by toggling interrupt lines off/on.
17	Test stuck 8259 interrupt bits: turn interrupt bits off and verify no interrupt mask register is on.
18	Test 8259 functionality: force an interrupt and verify the interrupt occurred.
19	Test stuck NMI bits (parity I/O check): verify NMI can be cleared.
1A-1E	Reserved.
1F	Set EISA mode: If EISA non-volatile memory checksum is good, execute EISA init. If not, execute ISA tests and clear EISA mode flat. Test EISA config mem checksum and communication ability.
20	Initialize and enable EISA slot 0 (system board).
21-2F	Initialize and enable EISA slots 1-15.
30	Size base memory from 256-640K and test with various patterns.

Code	Meaning
31	Test extended memory above 1Mb using various patterns. Press Esc to skip.
32	If EISA mode flag set, test EISA memory found during slot initialization. Skip this by pressing Esc.
33-3B	Reserved.
3C	Verify CPU can switch in/out of protected, virtual 86 and 8086 page modes.
3D	Detect if mouse is present, initialize it, and install interrupt vectors.
3E	Initialize cache controller according to CMOS RAM setup
3F	Enable shadow RAM according to CMOS RAM setup or if MEM TYPE is SYS in the EISA configuration information.
40	Reserved
41	Initialize floppy disk drive controller and any drives.
42	Initialize hard disk drive controller and any drives.
43	Detect and initialize serial ports.
44	Detect and initialize parallel ports.
45	Detect and initialize math coprocessor
46	Print Setup message (press Ctrl-Alt-Esc to enter Setup at bottom of the screen, and enable setup.
47	Set speed for boot.
48-4D	Reserved.
4E	Reboot if manufacturing POST loop pin is set. Otherwise, display any messages for non-fatal POST errors; enter setup if user pressed Ctrl-Alt-Esc.
4F	Security check (optional): Ask for password.
50	Write all CMOS RAM values back to CMOS RAM, and clear the screen.
51	Preboot enable: Enable parity, NMI, cache before boot.
52	Initialize ROMs between C80000-EFFFF. When FSCAN enabled, init from C80000 to F7FFF.
53	Initialize time value at address 40 of BIOS RAM area.
55	Initialize DDNIL counter to NULLs.
63	Boot attempt: Set low stack and boot by calling INT 19.
B0	Spurious interrupt occurred in protected mode.
B1	Unclaimed NMI. If unmasked NMI occurs, display "Press F1 to disable NMI, F2 to boot".
BF	Program chipset: Called by POST 7 to program chipset from CT table.
C0	OEM specific—Turn on/off cache.
C1	OEM specific—Test for memory presence and size on-board memory.
C2	OEM specific—Initialize board and turn on shadow and cache for fast boot.
C3	OEM specific—Turn on extended memory DRAM select and initialize RAM.
C4	OEM specific—Handle display/video switch to prevent display switch errors.
C5	OEM specific—Fast Gate A20 handling.
C6	OEM specific—Cache routine for setting regions that are cacheable.
C7	OEM specific—Shadow video/system BIOS after memory proven good.

Code	Meaning
C8	OEM specific—Handle special speed switching.
C9	OEM specific—Handle normal shadow RAM operations.
D0-DF	Debug: available POST codes for use during development.
EO	Reserved.
E1-EF	Setup pages: E1 = page 1, E2 = page 2, etc.
FF	If no error flags such as memory size are set, boot via INT 19—load system from drive A, then C; display error message if boot device not found.

EISA BIOS

Code	Meanings
1	CPU flags
2	CPU registers
3	Initialize DMA
4	Memory refresh
5	Keyboard initialization
06	ROM checksum
07	CMOS
08	256K memory
09	Cache
0A	Set interrupt table
0B	CMOS checksum
0C	Keyboard initialization
0D	Video adapter
0E	Video memory
0F	DMA channel 0
10	DMA channel 1
11	DMA page register
14	Timer chip
15	PIC controller 1
16	PIC controller 2
17	PIC stuck bits
18	PIC maskable IRQs
19	NMI bit check
1F	CMOS XRAM
20	Slot 0
21	Slot 1
22	Slot 2
23	Slot 3
24	Slot 4
25	Slot 5
26	Slot 6
27	Slot 7
28	Slot 8
29	Slot 9
2A	Slot 10
2B	Slot 11

Code	Meanings
2C	Slot 12
2D	Slot 13
2E	Slot 14
2F	Slot 15
30	Memory size 256K
31	Memory test over 256K
32	EISA memory
3C	CMOS setup on
3D	Mouse
3E	Cache RAM
3F	Shadow RAM
40	N/A
41	Floppy drive
42	Hard drive
43	RS232/parallel
45	NPU
47	Speed
4E	Manufacturing loop
4F	Security
50	CMOS update
51	Enable NMI
52	Adapter ROMs
53	Set time
63	Boot
B0	NMI in protected
B1	Disable NMI
BF	Chipset program
C0	Cache on/off
C1	Memory size
C2	Base 256K test
C3	DRAM page select
C4	Video switch
C5	Shadow RAM
C6	Cache program
C8	Speed switch
C9	Shadow RAM
CA	OEM chipset
FF	Boot

Late Award BIOS (4.5x-non PnP)

Code	Meaning
C0	Turn Off Chipset Cache; OEM specific cache control
01	Processor Test 1; Processor Status (1Flags) Verification. Tests carry/zero/sign/overflow processor status flags.
02	Processor Test 2; Read/Write/Verify all CPU registers except SS/SP and BP with data pattern FF and 00.
03	Initialize Chips; Disable NMI/PIE/UEL/SQWV; video; parity checking; DMA; reset maths coprocessor. Clear all page registers and CMOS

Code	Meaning
	shutdown byte. Initialize timer 0 1 and 2 including set EISA timer to a known state. Initialize DMA controllers 0 and 1; interrupt controllers 0 and 1 and EISA extended registers.
04	Test Memory Refresh Toggle
05	Blank video; initialize keyboard
06	Reserved
07	Test CMOS Interface and battery status. Detects bad battery. BE and Chipset Default Initialization. Program chipset registers with power-on BIOS defaults.
C1	Memory Presence Test; OEM specific test to size on-board memory
C5	Early Shadow; OEM specific—enable for fast boot
C6	Cache Presence Test; External cache size detection
08	Setup Low Memory; Early chipset initialization. Memory presence test. OEM chipset routines. Clear low 64K of memory. Test first 64K memory
09	Early Cache Initialization. Cyrix CPU Initialization. Cache Initialization
0A	Setup Interrupt Vector Table; Initialize first 120 interrupt vectors with SPURIOUS_INT_HDLR and initialize INT 00-FF according to INT_TBL.
0B	Test CMOS RAM Checksum if bad or Insert key depressed; load defaults.
0C	Initialize keyboard; Set NUM LOCK status.
0D	Initialize video interface; Detect CPU Clock. Read CMOS location 14h to find out type of video. Detect and initialize video adapter.
0E	Test Video Memory. Write signon message to screen. Set up Shadow RAM and enable according to Setup.
0F	Test DMA Controller 0. BIOS Checksum Test. keyboard detect and initialization.
10	Test DMA Controller 1
11	Test DMA Page Registers
12-13	Reserved
14	Test Timer Counter 2. Test 8254 Timer 0 Counter 2
15	Test 8259-1 Mask Bits. Alternately turns on and off interrupt lines.
16	Test 8259-2 Mask Bits. Alternately turns on and off interrupt lines.
17	Test Stuck 8259 interrupt bits. Turn off interrupts then verify no interrupt mask register is on.
18	Test 8259 Interrupt Functionality. Force an interrupt and verify that it occurred.
19	Test Stuck NMI Bits (Parity/I/O check). Verify NMI can be cleared.
1A	Display CPU Clock
1B-1E	Reserved
1F	Set EISA Mode. If EISA NVR checksum is good execute EISA initialization. If not execute ISA tests and clear EISA mode flag. Test EISA configuration memory integrity (checksum and communication interface).
20	Enable Slot 0. Motherboard
21-2F	Enable Slots 1-15
30	Size Base and Extended Memory. From 256-640K and that above 1 Mb.
31	Test Base and Extended Memory. Various patterns are used on that described above. This will be skipped in EISA mode and can be skipped in ISA mode with Esc.

Code	Meaning
32	Test EISA Extended Memory. If EISA Mode flag is set then test EISA memory found in slots initialization. This will be skipped in ISA mode and can be skipped in EISA mode with Esc.
33-3B	Reserved
3C	Setup Enabled
3D	Initialize and Install Mouse
3E	Setup Cache Controller
3F	Reserved
BF	Chipset Initialization. Program registers with Setup values.
40	Display virus protect enable or disable.
41	Initialize floppy drive(s) and controller
42	Initialize hard drive(s) and controller
43	Detect and initialize Serial/Parallel Ports and game port.
44	Reserved
45	Detect and Initialize Maths Coprocessor
46	Reserved
47	Reserved
48-4D	Reserved
4E	Manufacturing POST Loop or Display Messages. Reboot if manufacturing POST Loop Pin is set. Otherwise display any messages (i.e. non-fatal errors detected during POST) and enter Setup.
4F	Security Check. Ask password (optional)
50	Write CMOS. Write all CMOS values back to RAM and clear screen.
51	Pre-boot Enable. Enable Parity Checker; NMI and cache before boot.
52	Initialize Option ROMs. Between C800-EFFF. When FSCAN option is enabled will initialize between C800-F7FF
53	Initialize Time Value In 40h BIOS area.
60	Setup Virus Protect. According to Setup
61	Set Boot Speed
62	Setup NumLock. According to Setup
63	Boot attempt. Set Low Stack. Boot via INT 19
B0	Spurious. If interrupt occurs in protected mode
B1	Unclaimed NMI. If unmasked NMI occurs display "Press F1 to disable NMI; F2 reboot"
E1-EF	Setup Pages. E1=Page 1; E2=Page 2 etc
FF	Boot

Late Award BIOS (4-5x PnP)

Code	Meaning
C0	1.Turn off OEM specific cache, shadow 2.Initialize standard devices with default values: DMA controller (8237) Programmable Interrupt Controller (8259) Programmable Interval Timer (8254) RTC chip
C1	Auto detection of onboard DRAM & Cache
C3	1. Test the first 256K DRAM 2. Expand the compressed codes into temporary DRAM area including the compressed system BIOS & Option ROMs

Code	Meaning
C5	Copy the BIOS from ROM into E000FFFF shadow RAM so that POST will go faster
01-02	Reserved
03	Initialize EISA registers (EISA BIOS only)
04	Reserved
05	1. Keyboard Controller Self Test 2. Enable Keyboard Interface
06	Reserved
07	Verifies CMOS's basic R/W functionality
BE	Program defaults values into chipset according to the MODBINable Chipset Default Table
09	1.Program configuration register of Cyrix CPU according to the MODBINable Cyrix Register Table 2.OEM specific cache initialization
0A	1.Initialize the first 32 interrupt vectors with corresponding interrupt handlers Initialize INT No from 33120 with Dummy (Spurious) interrupt handler 2.Issue CPUID instruction to identify CPU type 3.Early Power Management initialization (OEM specific)
0B	1.Verify the RTC time is valid or not 2.Detect bad battery 3.Read CMOS data into BIOS stack area 4.PnP initializations including (PnP BIOS only) Assign CSN to PnP ISA card Create resource map from ESCD 5.Assign IO & Memory for PCI devices (PCI BIOS only)
0C	Initialization of the BIOS data area (40:040:FF)
0D	1.Program some of the chipset's value according to setup.(Early setup value program) 2.Measure CPU speed for display & decide the system clock speed 3.Video initialization including Monochrome, CGA, EGA/VGA If no display device found, the speaker will beep.
0E	1.Initialize the APIC (MultiProcessor BIOS only) 2.Test video RAM (If Monochrome display device found) 3.Show message including: Award logo Copyright string BIOS date code & Part No OEM specific sign on messages Energy Star logo (Green BIOS only) CPU brand, type & speed
0F	DMA channel 0 test
10	DMA channel 1 test
11	DMA page registers test
12-13	Reserved
14	Test 8254 timer 0 counter 2
15	Test 8259 interrupt mask bits for channel 1
16	Test 8259 interrupt mask bits for channel 2
17	Reserved
19	Test 8259 functionality
1A-1D	Reserved
1E	If EISA NVM checksum is good, execute EISA initialization (EISA BIOS only)

Code	Meaning
1F-29	Reserved
30	Get base memory & extended memory size
31	1.Test base memory from 256K to 640K 2.Test extended memory from 1M to the top of memory
32	1.Display the Award Plug & Play BIOS extension message(PnP BIOS only) 2.Program all onboard super I/O chips(if any) including COM ports, LPT ports, FDD port according to setup value
33-3B	Reserved
3C	Set flag to allow users to enter CMOS setup utility
3D	1.Initialize keyboard 2.Install PS2 mouse
3E	Try to turn on level 2 cache Note: Some chipset may need to turn on the L2 cache in this stage. But usually, the cache is turn on later in Post 61h
3F-40	Reserved
BF	1.Program the rest of the chipset's value according to setup (later setup value program) 2.If auto configuration is enabled, programmed the chipset with predefined values in the MODBINable AutoTable
41	Initialize floppy disk drive controller
42	Initialize hard drive controller
43	If it is a PnP BIOS, initialize serial & parallel ports
44	Reserved
45	Initialize math coprocessor
46-4D	Reserved
4E	If there is any error detected (such as video, KB....), show all the error messages on the screen & wait for user to press <F1> key
4F	1.If password is needed, ask for password 2.Clear the Energy Star logo (Green BIOS only)
50	Write all the CMOS values currently in the BIOS stack are back into the CMOS
51	Reserved
52	1.Initialize all ISA ROMs 2.Later PCI initializations(PCI BIOS only) assign IRQ to PCI devices initialize all PCI ROMs 3.PnP initializations (PnP BIOS only) assign IO, Memory, IRQ & DMA to PnP ISA devices initialize all PnP ISA ROMs 4.Program shadow RAM according to setup settings 5.Program parity according to setup setting 6.Power Management initialization Enable/Disable global PM APM interface initialization
53	1.If it is not a PnP BIOS, initialize serial & parallel ports 2.Initialize time value in BIOS data area by translate the RTC time value into a timer tick value
54-5F	Reserved
60	Setup virus protection (boot sector protection) functionality according to setup setting
61	1.Try to turn on level 2 cache (if L2 cache already turned on in post 3D, this part will be skipped)

Code	Meaning
	2.Set the boot up speed according to setup setting 3.Last chance for chipset initialization 4.Last chance for Power Management initialization (Green BIOS only) 5.Show the system configuration table
62	1.Setup daylight saving according to setup values 2.Program the NUM lock, typematic rate & typematic speed according to setup setting
63	1.If there is any changes in the hardware configuration, update the ESCD information (PnP BIOS only) 2.Clear memory that have been used 3.Boot system via INT 19h
FF	Boot

Unexpected Errors

Code	Meaning
B0	If interrupt occurs in protected mode
B1	Unclaimed NMI occurs

v3.3

Code	Meaning
1-5	Keyboard controller
06	On board LSI
07	CPU
8-0E	CMOS; 8254; 8237; 8259; EPROM
0F	Extended CMOS
10-14	Refresh
15	First 64K RAM
16	Interrupt vector tables
17	Video initialization
18	Video memory
19-1A	Interrupt line mask
1B	Battery good
1C	CMOS checksum
1D	CMOS chip
1E	Memory size
1F	Memory verifier
20-23	CPU support chips
24	Extended memory size
25	Extended memory size
26	Protected mode
27-28	Shadow RAM
29	Reserved
2A	Initialize keyboard
2B	Floppy drive initialization
2C	Serial port initialization
2D	Parallel port initialization
2E	Hard disk initialization

Code	Meaning
2F	Math coprocessor
30	Reserved
31	Optional ROMs
FF	Boot

Chips and Technologies

Some are sent to the display in decimal as well as port 80 in hex. Micro Channel BIOSes use ports 680 and 3BC.

POST Procedures

Procedure	Meaning
Power On Tests	CPU synchronizes with clock. Check the CPU or clock.
System ROM Check	The BIOS runs a checksum on itself. Check the BIOS chips.
DMA Controller Fail	DMA Controllers are initialized and tested. Check the DMA chips.
System Timer Failed	Channels 0/1/2 are tested in sequence. Check the PIT chips.
Base 64K Memory Testing	Walking-bit test performed on 1st 64K of RAM which is critical for the BIOS vector area to be initialized. Check for bad RAM chips or a data or address line.
Interrupt Contr Failed	Test the 8259 chip.
CPU Still In Protected Mode	Attempts are made to read the configuration of the system through the 8042 keyboard controller.
Refresh Not Occurring	Memory refresh is tested; standard refresh is 120-140 ns. Check the PIT chip.
Keyboard Controller Not Responding	Tests are run on the keyboard controller. Check the 8042 chip.
Could Not Enter Protected Mode	BIOS attempts to enter protected mode to test extended memory. Check the 8042 chip or the A20 address line.
Initialize Timer	Attempts are made to initialize the PIT.
Initi DMA Controller	Attempts are made to initialize the DMA Controller.
Entering/Exiting Protected Mode	The transition is handled by the keyboard controller and the A20 line. Check the 8042 or the A20.
Relocate Shadow RAM	BIOS attempts to shadow itself into extended memory. Check for memory problems.
Test For EMS	Check the EMS adapter or an improper CMOS/Jumper setting.
Test Video Capabilities	Normally includes a memory test on the adapter memory up to 256K.
Test Memory	Extensive testing of Base, Extended, Expanded memory. Check for defective memory modules; 8042 chip; A20 line or an improper CMOS/Jumper setting.
Check System Options	The hardware in the system is compared with the values stored in CMOS. The PIT/PIC/8042/RTC and other system board chips are tested again.

Procedure	Meaning
Peripheral Check/Test	Checks are made for peripherals at standard I/O ports including serial and parallel ports keyboards and maths coprocessors. You should see an error message on screen at this point.
Floppy Test	Floppy devices set in CMOS are checked and initialized. If a bootable floppy is found the fixed disks are tested and the BIOS will boot to the floppy disk. Check for defective controllers or an improper CMOS Setup.
Fixed Disk Test	Checks for fixed disks in CMOS. If no bootable floppy in the A: drive the BIOS loads the first sector off the first fixed disk and jumps to the area of memory where the sector was loaded. You may just see a flashing cursor or an error message from the potential operating system. Check for improper CMOS setup/defective controller/fixed disk or corruption of bootloader software on the fixed disk.
Advanced Options	These include mouse/cache etc. You should see an error message on the screen at this point, except that a defective cache may hang the system; in most cases, the cache will be disabled by the BIOS.

POST Codes

NEAT, PEAK/DM, OC8291, ELEAT BIOS

Hex	Dec	Code
00h	00	Error in POS register.
01h	01	Flag register failed.
02h	02	CPU register failed.
03h	03	System ROM did not checksum
04h	04	DMA controller failed
05h	05	System timer failed
06h	06	Base 64K RAM failed address test: not installed, misconfigured, or bad addressing
07h	07	Base 64K RAM failed data test
08h	08	Interrupt controller failed
09h	09	Hot (unexpected) interrupt occurred
0Ah	10	System timer does not interrupt
0Bh	11	CPU still in protected mode
0Ch	12	DMA page registers failed
0Dh	13	Refresh not occurring
0Eh	14	Keyboard controller not responding
0Fh	15	Could not enter protected mode
10h	16	GDT or IDT failed
11h	17	LDT register failed
12h	18	Task register failed
13h	19	LSL instruction failed
14h	20	LAR instruction failed
15h	21	VERR/VERW failed
16h	22	Keyboard controller gate A20 failed
17h	23	Exception failed/unexpected exception

Hex	Dec	Code
18h	24	Shutdown during memory test
19h	25	Last used error code
1Ah	26	Copyright checksum error
1Bh	27	Shutdown during memory sizing
1Ch	28	CHIPSet initialization
50h	80	Initialize hardware
51h	81	Initialize timer
52h	82	Initialize DMA controller
53h	83	Initialize interrupt controller
54h	84	Initialize CHIPSet
55h	85	Setup EMS configuration
56h	86	Entering protected mode for first time
57h	87	Size memory chips
58h	88	Configure memory chip interleave
59h	89	Exiting protected mode for first time
5Ah	90	Determine system board memory size
5Bh	91	Relocate shadow RAM
5Ch	92	Configure EMS
5Dh	93	Set up wait state configuration
5Eh	94	Re-test 64K RAM
5Fh	95	Test shadow RAM
60h	96	Test CMOS RAM
61h	97	Test video
62h	98	Test and initialize DDNIL bits
63h	99	Test protected mode interrupt
64h	100	Test address line A20
65h	101	Test memory address lines
66h	102	Test memory
67h	103	Test extended memory
68h	104	Test timer interrupt
69h	105	Test real time clock (RTC)
6Ah	106	Test keyboard
6Bh	107	Test 80x87 math chip
6Ch	108	Test RS232 serial ports
6Dh	109	Test parallel ports
6Eh	110	Test dual card
6Fh	111	Test floppy drive controller
70h	112	Test hard drive controller
71h	113	Test keylock
72h	114	Test pointing device
90h	144	Setup RAM
91h	145	Calculate CPU speed
92h	146	Check configuration
93h	147	Initialize BIOS
94h	148	POST Bootstrap
95h	149	Reset ICs
96h	150	PEAK: System board POS. NEAT/OC8291 ELEAT: Test/initialize cache RAM and controller.
97h	151	VGA Power on Diagnostics and setup
98h	152	Adapter POS
99h	153	Re-initialize DDNIL bits

Hex	Dec	Code
A0h	160	Exception 0
A1h	161	Exception 1
A2h	162	Exception 2
A3h	163	Exception 3
A4h	164	Exception 4
A5h	165	Exception 5
A6h	166	Exception 6
A7h	167	Exception 7
A8h	168	Exception 8
A9h	169	Exception 9
AAh	170	Exception A
ABh	171	Exception B
ACh	172	Exception C
ADh	173	Exception D
C0h	224	System board memory failure
C1h	225	I/O Channel Check activated
C2h	226	Watchdog timer timeout
C3h	227	Bus timer timeout

Compaq

Port 84 codes indicate errors while port 85 codes show the category:

00 System BIOS

01 Error after boot

05 Video POST

General

Code	Meaning
00	Initialize flags
01	Read manufacturing jumper
02	8042 Received Read command
03	No response from 8042
04	Look for ROM at E000
05	Look for ROM at C800
06	Normal CMOS reset code
08	Initialize 8259
09	Reset code in CMOS byte
0A	Vector Via 40:67 reset function
0B	Vector Via 40:67 with E01 function
0C	Boot reset function
0D	Test #2 8254 Counter 0
0E	Test #2 8254 Counter 2
0F	Warm Boot

Overall Power Up Sequence

Code	Meaning
10	PPI disabled
11	Initialize (blast) VDU controller
12	Clear Screen; turn on video
13	Test time 0
14	Disable RTC interrupts
15	Check battery power
16	Battery has lost power
17	Clear CMOS diags
18	Test base memory (first 128K)
19	Initialize base memory
1A	Initialize VDU adapters
1B	The system ROM
1C	CMOS checksum
1D	DMA controller/page registers
1E	Test keyboard controller
1F	Test 286 protected mode
20	Test real and extended memory
21	Initialize time-of-day
22	Initialize 287 coprocessor
23	Test the keyboard and 8042
24	Reset A20
25	Test diskette subsystem
26	Test fixed disk subsystem
27	Initialize parallel printer
28	Perform search for optional ROMs
29	Test valid system configuration
2A	Clear screen
2B	Check for invalid time and date
2C	Optional ROM search
2D	Test timer 2
2F	Write to diagnostic byte

Base RAM Initialization

Code	Meaning
30	Clear first 128K bytes of RAM
31	Load interrupt vectors 70-77
32	Load interrupt vectors 00-1F
33	Initialize MEMSIZE and RESETWD
34	Verify CMOS checksum
35	CMOS checksum not valid
36	Check battery power
37	Check for game adapters
38	Check for serial ports
39	Check for parallel printer ports
3A	Initialize port and comm timeouts
3B	Flush keyboard buffer

Base RAM Test

Code	Meaning
40	Save RESETWD value
41	Check RAM refresh
42	Start write of 128K RAM test
43	Rest parity checks
44	Start verify of 128K RAM test
45	Check for parity errors
46	No RAM errors
47	RAM error detected

VDU Initialization and Test

Code	Meaning
50	Check for dual frequency in CMOS
51	Check CMOS VDU configuration
52	Start VDU ROM search
53	Vector to VDU option ROMs
54	Initialize first display adapter
55	Initialize second display adapter
56	No display adapters installed
57	Initialize primary VDU mode
58	Start of VDU test (each adapter)
59	Check existence of adapter
5A	Check VDU registers
5B	Start screen memory test
5C	End test of adapter
5D	Error detected on an adapter
5E	Test the next adapter
5F	All adapters successfully tested

Memory Test

Code	Meaning
60	Start of memory tests
61	Enter protected mode
62	Start memory sizing
63	Get CMOS size
64	Start test of real memory
65	Start test of extended memory
66	Save size memory (base
67	128K option installed CMOS bit
68	Prepare to return to Real Mode
69	Back in Real Mode—successful
6A	Protected mode error during test
6B	Display error message
6C	End of memory test
6D	Initialize KB OK string

Code	Meaning
6E	Determine size to test
6F	Start MEMTEST
70	Display XXXXXKB OK
71	Test each RAM segment
72	High order address test
73	Exit MEMTEST
74	Parity error on bus

80286 Protected Mode

Code	Meaning
75	Start protected mode test
76	Prepare to enter protected mode
77	Test software exceptions
78	Prepare to return to Real Mode
79	Back in Real Mode—successful
7A	Back in Real Mode—error occurred
7B	Exit protected test
7C	High order address test failure
7D	Entered cache controller test
7E	Programming memory cache
7F	Copy system ROM to high RAM

8042 and Keyboard

Code	Meaning
80	Start of 8042 test
81	Do 8042 self test
82	Check result received
83	Error result
84	OK 8042
86	Start test
87	Got acknowledge
88	Got result
89	Test for stuck keys
8A	Key seems to be stuck
8B	Test keyboard interface
8C	Got result
8D	End of Test

System Board Test

Code	Meaning
90	Start of CMOS test
92	CMOS seems to be OK
92	Error on CMOS read/write test
93	Start of DMA controller test
94	Page registers seem OK
95	DMA controller is OK

Code	Meaning
96	8237 initialization is complete
97	Start of NCA RAM test

Diskette Test

Code	Meaning
A0	Start of diskette tests
A1	FDC reset active (3F2h bit 2)
A2	FDC reset inactive (3F2h bit 2)
A3	FDC motor on
A4	FDC timeout error
A5	FDC failed reset
A6	FDC passed reset
A8	Start to determine drive type
A9	Seek operation initiated
AA	Waiting for FDC seek status
AF	Diskette tests completed
B0	Start of fixed disk drive tests
B1	Combo board not found—exit
B2	Combo controller failed—exit
B3	Testing drive 1
B4	Testing drive 2
B5	Drive error (error condition)
B6	Drive failed (failed to respond)
B7	No fixed drives—exit
B8	Fixed drive tests complete
B9	Attempt to boot diskette
BA	Attempt to boot fixed drive
BB	Boot attempt failed FD/HD
BC	Boot record read, jump to boot record
BD	Drive error, retry booting
BE	Weitek coprocessor test (386, 386/xxe, 386&486/33L, P486c)

EISA TESTS

Deskpro/M, /LT, /33L, P486c

Code	Meaning
C0	EISA non-volatile memory checksum
C1	EISA DDF map initialization
C2	EISA IRQ initialization
C3	EISA DMA initialization
C4	EISA slot initialization
C5	EISA display configuration error messages
C6	EISA PZ initialization begun
C7	EISA PZ initialization done
C8	System manager board self-test

Code	Meaning
C0	Disable NMI
C1	Turn off hard disk subsystem
C2	Turn off video subsystem
C3	Turn off floppy disk subsystem
C4	Turn off hard disk/modem subsystems
C5	Go to standby
C6	Update BIOS time of day
C7	Turn on hard disk/modem subsystems
C8	Turn on floppy disk subsystem
C9	Turn on video subsystem
CB	Flush keyboard input buffer
CC	Reenable MNI

Standard POST Functions

Code	Meanings
D0	Entry to clear memory routine
D1	Ready to go to protected mode
D2	Ready to clear extended memory
D3	Ready to reset back to real mode
D4	Back in real mode, ready to clear
D5	Clear base memory, CLIM register init failure (SLT/286)
D7	Scan and clear DDNIL bits
D9	Orvonton 4-way cache detect
DD	Built-in self-test failed

Option ROM Replacement

Code	Meaning
E0	Ready to replace E000 ROM
E1	Completed E000 ROM replacement
E2	Ready to replace EGA ROM
E3	Completed EGA ROM replacement
E8	Looking for serial external boot ID str (Deskpro 2/386N, 386s/20)
E9	Receiving for serial external boot sector (2/386N, 386s/20)
EA	Looking for parallel external boot ID str (2/386N, 386s/20)
EB	Receiving parallel external boot sector (2/386N, 386s/2O)
EC	Boot record read, jump to boot record (2/386N, 386s/20)

Port 85=05 (Video POST)

Code	Meaning
00	Entry into video option ROM
01	Alternate adapter tests
02	Vertical sync tests
03	Horizontal sync tests
04	Static tests
05	Bus tests
06	Configuration tests
07	Alternate ROM tests
08	Color gun off tests
09	Color gun on tests
0A	Video memory tests
0B	Board present tests
10	Illegal configuration error
20	No vertical sync present
21	Vertical sync out of range
30	No horizontal sync present

Code	Meaning
40	Color register failure
50	Slot type conflict error
51	Video memory conflict error
52	ROM conflict error
60	Red DAC stuck low error
61	Green DAC stuck low error
62	Blue DAC stuck low error
63	DAC stuck high error
64	Red DAC fault error
65	Green DAC fault error
66	Blue DAC fault error
70	Bad alternate ROM version
80	Color gun stuck ON base code
90	Color gun stuck OFF base code
A0	Video memory failure base code
F0	Equipment failure base code
00	Video POST over (also send 00 to 85)

After the POST, the BIOS boots the operating system. If it detects a run-time error, it sends category code 01 to port 85, and the error code to port 84 in the same way it sends POST codes before booting. These are the run-time codes:

Code	Meaning
10	Entered dummy end-of-interrupt routine
11	Entered "int 2" module (parity error)
12	Emulating "lock" instruction
13	Emulating "loadall' instruction
14	Illegal opcode instruction encountered
15	Entered "dum iret" module
16	Entered "irg9" module
17	Entered "287err" module

286 DeskPro

Code	Meaning
01	CPU
02	Coprocessor
03	DMA
04	Interrupt Controller
05	Port 61
06	Keyboard Controller
07	CMOS
08	CMOS
09	CMOS
10	Programmable Timer
11	Refresh Detect Test
12	Speed Test
14	Speaker Test
21	Memory Read/Write

Code	Meaning
24	Memory Address
25	Walking I/O
31	Keyboard Short Test
32	Keyboard Long Test
33	Keyboard LED Test
35	Security Lock Test
41	Printer Failed
42	Printer Date
43	Printer Pattern Test
48	Printer Failed
51	VDU Controller Test
52	VDU Controller Test
53	VDU Attribute Test
54	VDU Character Set Test
55	VDU 80x25 Mode
56	VDU 80x25 Mode
57	VDU 40x25 Mode
60	Diskette Drive ID Test
61	Format
62	Read Test
63	Write/Read Compare Test
64	Random Seek
65	ID Media Test
66	Speed Test
67	Wrap Test
68	Write Protect Test
69	Reset Controller Test

386 DeskPro

Code	Meaning
01	I/O ROM Error
02	System Memory Board Failure
12	System Option Error
13	Time and Date not set
14	Memory Size Error
21	Memory Error
23	Memory Address Error
25	Memory Error
26	Keyboard Error
33	Keyboard Controller Error
34	Keyboard or System Unit Error
41	Printer Error
42	Mono Adapter Failure
51	Display Adapter Failure
61	Diskette Controller Error
62	Diskette Boot Recorder Error
65	Diskette Drive Error
67	Ext FDC Failed—Go To Internal F
6A	Floppy Port Address Conflict

Code	Meaning
6B	Floppy Port Address Conflict
72	Coprocessor Detection

486 DeskPro

Code	Meaning
01	CPU Test Failed
02	Coprocessor or Weitek Error
03	DMA Page Registers
04	Interrupt Controller Master
05	Port 61 Error
06	Keyboard Controller Self Test
07	CMOS RAM Test Failed
08	CMOS Interrupt Test Failed
09	CMOS Clock Load Data Test
10	Programmable Timer
11	Refresh Detect Test Failed
12	Speed Test Slow Mode out of range
13	Protected Mode Test Failed
14	Speaker Test Failed
16	Cache Memory Configuration
19	Installed Devices Test
21	Memory Machine ID Test Failed
22	Memory System ROM Checksum
23	Memory Write/Read Test Failed
24	Memory Address Test Failed
25	Walking I/O Test Failed
26	Increment Pattern Test Failed
31	Keyboard Short Test, 8042
32	Keyboard Long Test Failed
33	Keyboard LED Test, 8042
34	Keyboard Typematic Test Failed
41	Printer Failed or Not Connected
42	Printer Data Register Failed
43	Printer Pattern Test
48	Printer Not Connected
51	Video Controller Test Failed
52	Video Memory Test Failed
53	Video Attribute Test Failed
54	Video Character Set Test Failed
55	Video 80x25 Mode
56	Video 80x25 Mode
57	Video 40x25 Mode Test Failed
58	Video 320x200 Mode Color Set 1
59	Video 320x200 Mode Color Set 1
60	Diskette ID Drive Types Test
61	Diskette Format Failed
62	Diskette Read Test Failed
63	Diskette Write
65	Diskette ID Media Failed

Code	Meaning
66	Diskette Speed Test Failed
67	Diskette Wrap Test Failed
68	Diskette Write Protect Test
69	Diskette Reset Controller Test
82	Video Memory Test Failed
84	Video Adapter Test Failed

Dell

OEM version of Phoenix, sent to Port 80. Also uses Smartvu display on front of machine.

Code	Beeps	SmartVu	Meaning
01	1-1-2	Regs xREG xCPU(2)	CPU register test in progress
02	1-1-3	CMOS xCMS	CMOS write/read test failed
03	1-1-4	BIOS xROM	ROM BIOS checksum bad
04	1-2-1	Timr xTMR	Programmable interval timer failed
05	1-2-2	DMA xDMA	DMA initialization failed
06	1-2-3	Dpge xDPG	DMA page register write/read bad
08	1-3-1	Rfsh xRFH	RAM refresh verification failed
09	1-3-2	Ramp RAM?	First 64K RAM test in progress
0A	1-3-3	xRAM	First 64K RAM chip or data line bad, multi-bit
0B	1-3-4	xRAM	First 64K RAM odd/even logic bad
0C	1-4-1	xRAM	Address line bad first 64K RAM
0D	1-4-2	64K? x64K	Parity error detected in first 64K RAM
10	2-1-1		Bit 0 first 64K RAM bad
11	2-1-2		Bit 1 first 64K RAM bad
12	2-1-3		Bit 2 first 64K RAM bad
13	2-1-4		Bit 3 first 64K RAM bad
14	2-2-1		Bit 4 first 64K RAM bad
15	2-2-2		Bit 5 first 64K RAM bad
16	2-2-3		Bit 6 first 64K RAM bad
17	2-2-4		Bit 7 first 64K RAM bad
18	2-3-1		Bit 8 first 64K RAM bad
19	2-3-2		Bit 9 first 64K RAM bad
1A	2-3-3		Bit 10 first 64K RAM bad
1B	2-3-4		Bit 11 first 64K RAM bad
1C	2-4-I		Bit 12 first 64K RAM bad
1D	2-4-2		Bit 13 first 64K RAM bad
1E	2-4-3		Bit 14 first 64K RAM bad
1F	2-4-4		Bit 15 first 64K RAM bad
20	3-1-1	SDMA xDMS	Slave DMA register bad
21	3-1-2	MDMA xDMM	Master DMA register bad
22	3-1-3	PICO xICO	Master interrupt mask register bad
23	3-1-4	PIC1 xIC1	Slave interrupt mask register bad
25	3-2-2	Intv	Interrupt vector loading in progress
27	3-2-4	Kybd xKYB	Keyboard controller test failed

Code	Beeps	SmartVu	Meaning
28	3-3-1	CmCk	CMOS RAM power bad; calculating checksum
29	3-3-2	Cnfg	CMOS configuration validation in progress
2B	3-3-4		Video memory test failed
2C	3-4-1	CRTI	Video initialization failed
2D	3-4-2		Video retrace failure
2E	3-4-3	CRT?	Search for video ROM in progress
30	none		Screen operable, running with video ROM
31	none		Monochrome monitor operable
32	none		Color monitor (40 column) operable
33	none		Color monitor (80 column) operable

Non-Fatal Error Meanings for ATs

Only if Manufacturing Jumper is on POST

Code	Beeps	Smartvu	Meaning
34	4-2-1	Tick	Timer tick interrupt test in progress or bad
35	4-2-2	Shut	Shutdown test in progress or bad
36	4-2-3	A20	Gate A20 bad
37	4-2-4		Unexpected interrupt in protected mode
38	4-3-1	Emem	RAM test in progress or high address line bad > FFFF
3A	4-3-3	Tmr2	Interval timer channel 2 test or bad
3B	4-3-4	Time	Time-of-Day clock test or bad
3C	4-4-1	Asyn	Serial port test or bad
3D	4-4-2	Prnt	Parallel port test or bad
3E	4-4-3		Math coprocessor test or bad
3F	4-4-4	XCsh	Cache test failure

DTK

Evolved from ERSO (Taiwan).

Post Procedures—Symphony 486 BIOS

Procedure	Meaning
Initialize Interrupt Controller	Check the PIC chips.
Initialize Video Card	
Initialize DMA Controller	
Initialize Page Register	Check the 74612 chips.
Test Keyboard Controller	Internal operations of the keyboard controller are tested (8042).
Initialize DMA Contr/Timer	All DMA registers and CMOS status bytes 0E/0F are cleared. The BIOS then initializes the 8254 chip. Check the DMS or PIT chips.

Procedure	Meaning
DRAM Refresh Testing	
Base 64K Memory Testing	A walking-bit test of the first 64K of RAM address which is critical for the BIOS vector area to be initialized. Check for bad RAM chips or a data or address line.
Set System Stack	An area of memory is set aside by BIOS as a stack. Check bad DMA/memory.
Read System Configuration via 8042	e.g. the keyboard controller. Check for incorrect setup or bad keyboard controller or CMOS chip.
Test Keyboard Clock and Data Line	The keyboard's ability to handle the A20 line is tested as well as its internal clock. Check the keyboard controller or a bad address line.
Determine Video Type	
Check RS232/Printer	Test serial/parallel ports. Check I/O cards.
FDC Check	Test floppy controller. Check the drive as well.
Count Shadow RAM	Run a series of memory tests on the system. Check for bad memory chips address lines or data lines.
Display Total Mem/Return to Real Mode	Total memory detected is displayed and the machine is returned to real mode. Check the keyboard controller or A20 line.
Back to Real Mode	Transition is attempted through the A20 line and the keyboard controller.
Check HDC	The hard drive controller is tested.
Check FDD	Attempts are made to initialize the floppy drives.
Turn off Gate A20 and Test CoProcessor	Attempts are made to transition back to real mode by disabling the A20 line then the coprocessor is tested if present. Check the keyboard controller coprocessor or improper setup in CMOS.
Set Time and Date	Time and date will be read from the RTC.

POST Codes

Code	Meaning
01	Power on start
03	Initialize interrupt controller—8259
05	Initialize video card—MCA and CGA
0D	Initialize DMA controller—8237
0E	Initialize page register—74612
12	Test keyboard controller—8042
16	Initialize DMA controller and timer
22	DRAM refresh testing
25	Base 64K memory testing
30	Set system stack
33	Read system configuration through 8042
37	Test keyboard clock and data line
40	Determine video type
44	Testing MGA and CGA if existing
48	Video 80 x 25 mode initialization
4D	Display DTK BIOS title
4F	Check RS232 and printer
50	FDC check

Code	Meaning
55	Count shadow RAM
58	Display total memory and return to real mode
5A	Back to real mode
60	Check HDC
62	Check FDD
65	Check HDC
67	Initialize FDC and HDC
6A	Turn off gate A20 and test coprocessor
70	Set time and date according to RTC
77	Boot

Eurosoft

See *Mylex/Eurosoft*.

Faraday A-Tease

Owned by Western Digital.

Code	Meaning
01	CPU test failed
02	BIOS ROM checksum test
03	Shutdown
04	DMA page register test
05	8254 timer test
06	Start refresh
07	8042 keyboard controller test
08	Test lower 128K RAM
09	Setup video
0A	Test 128K-640K
0B	Test DMA controller #1
0C	Test DMA controller #2
0D	Test interrupt controller #1
0E	Test interrupt controller #2
0F	Test control port
10	Test parity
11	Test CMOS RAM
12	Test for manufacturing mode
13	Set up interrupt vectors
14	Test keyboard
15	Configure parallel port
16	Configure serial ports
17	Configure lower 640K RAM
18	Configure RAM above 1 Mb
19	Configure keyboard
1A	Configure floppy drive
1B	Configure hard drive

Code	Meaning
1C	Configure game card
1D	Configure 80287 math chip
1E	Check CMOS real time clock
1F	Generate and verify CMOS RAM checksum
21	Initialize PROM drivers
22	Test parallel port loopback
23	Test serial port loopback
24	Test CMOS real time clock
25	Test shutdown
26	Test memory over 1mb; output codes for errors 80-FF
80	Divide overflow
81	Single step
82	NMI
83	Breakpoint
84	Int 0 detect
85	Bound error
86	Invalid opcode
87	Processor extension not available
88	Double exception
89	Processor extended segment error
8A	Invalid task state segment
8B	Segment not present
8C	Stack segment not present
8D	General protection error
8E	General protection error
8F	General protection error
90	Processor extension error
91-FF	Spurious interrupts (except F3 and F0)
F3	CPU virtual (protected mode) test error
F0	Virtual block move error

Headstart

See *Philips*.

HP

Derived from Phoenix, all POST information is sent to the screen.

Vectra

A failure during POST will emit four beeps, and a 4-digit hex code to the monitor. Failures that occur before EGA/VGA monitors are initialized will not be displayed, so use a mono instead. BIOSes prior to March 1989 initialized the video before getting on with the POST.

POST Procedures

Code	Meaning
CPU	Registers in CPU tested with data patterns; error flags are set, verified and reset.
ROM BIOS Checksum	Checksums are performed on High and low BIOS Chips.
PIC Test	Test Timer Channels 0-2 then the memory refresh signal. Initialize timer if tests are passed. Check the 8254 chip.
64K Test	Walking-bit and address collision tests are performed on the first 64K of memory. Check for a bad memory chip or address line.
Cache Controller	Test the CPU cache controller and memory.
Video Adapter	Initialize the video adapter. If EGA/VGA is present wait for adapter to finish internal diagnostics. check the adapter or for improper setup.
DMA Test	Bit-patterns written to all DMA controller registers (inc page registers) and verifies the patterns written. If the tests pass the registers are reset and the controller initialized.
PIC Test	Test mask register of master and slave interrupt controllers. Generate interrupt and monitor CPU to test success. Failure is normally down to the PIC but the interrupt test uses the BIOS clock (interrupt) and the RTC so check those.
Keyboard Controller	Perform several tests on the 8042 keyboard controller then send a series of interrupt request commands via the 8259 PIC.
HP-HIL Test	Test the HP-HIL (Hardware Interrupt Level) controller with data patterns and verify it.
CMOS Test	Perform a checksum on the standard and extended CMOS RAM areas; perform a register test and check Byte 0D to determine power status. Check the CMOS extended CMOS RAM or battery respectively.
Manufacturing Test	Search for diagnostic tool used in manufacturing and run predetermined tests if found. Otherwise continue POST.
Base Memory Test	Test RAM between 64-640K with several pattern tests; the bit failure and bank can be determined by the displayed hex code.
Ext Memory Test	Test extended memory found. Bank and failing bit displayed by the hex code.
RTC Test	Test the RTC portion of the CMOS chip.
Keyboard Controller	Test keyboard controller; initialize k/b if no errors.
Floppy Disk	Test and initialize floppy controllers and drives found; check specific errors with the displayed hex code. Check for correct setup or defective CMOS chip or battery.
Maths Copro	Test NPU registers and interrupt request functions.
CPU Clock Test	Test interface between CPU and system at different speeds. Check for incorrect clock setting for system peripherals or a bad CPU or clock generator chip.
Serial/Parallel Test	Test and initialize serial/parallel ports. Failure here will not halt the POST. The Vectra RS BIOS does not test the parallel port.
Boot	Initialize the BIOS vector table; standard and extended CMOS data areas and any adapter ROMs present. Then

Code	Meaning
	call Int 19 and give control to the boot loader. Failures past this point are usually down to the hard drive or corrupt OS code.

POST Codes

Code	Meaning
01	LED test
02	Processor test
03	System (BIOS) ROM test
04	RAM refresh timer test
05	Interrupt RAM test
06	Shadow the System ROM BIOS
07	CMOS RAM test
08	Internal cache memory test
09	Initialize the Video Card
10	Test external cache
11	Shadow option ROMs
12	Memory Subsystem test
13	Initialize EISA/ISA hardware
14	8042 self-test
15	Timer 0/Timer 2 test
16	DMA Subsystem test
17	Interrupt controller test
18	RAM address line independence test
19	Size extended memory
20	Real-Mode memory test (first 640K)
21	Shadow RAM test
22	Protect Mode RAM test (extended RAM)
23	Real Time clock test
24	Keyboard test
25	Mouse test
26	Hard disk test
27	LAN test
28	Flexible disk controller subsystem test
29	Internal numeric coprocessor test
30	Weitek coprocessor test
31	Clock speed switching test
32	Serial Port test
33	Parallel Port test

IBM

Tests are performed by PC/XT/AT and PS/2 machines. There will be POST Codes (below), beep codes and screen displays if possible, but the XT does not give POST codes. ATs emit codes to 80h, while PS/2 models 25 and 30 emit to 90h, and 35 and above to 680. The BIOS will test main system components first, then non-critical

ones. If there is an error, the BIOS will look for a reference diskette in drive A: so diagnostics can be performed.

IBM POST I/O Ports

Architecture	Typical Computer	Port
PC	PC	none
ISA	XT	60
	AT	80
	PS/2 25,30	90, 190
MCA	PS/2 50 up	680, 3BC
EISA	none	none

POST Procedures

Procedure	Meaning
CPU	Perform register test on the CPU by writing data patterns to the registers and reading the results of the write.
ROM BIOS Checksum	The value of the bits inside the BIOS chip(s) is added to a preset value that should create a total of 00.
CMOS RAM	RAM within the CMOS chip is tested by writing data patterns to the area and verifying that the data was stored correctly.
DMA	Test DMA chips by forcing control inputs to the CPU to an active state and verifying that the proper reactions occur.
8042/8742 Keyboard Controller	Test including Gate A20 and the reset command. The buffer space is prepared and data is sent to the determined area via the keyboard controller to see if commands are received and executed correctly.
Base 64K System RAM.	Perform a walking-bit test of the first 64K of RAM so the BIOS vector area can be initialized. Check for bad RAM chips or a data/address line.
8259A PIC	Determine if commands to interrupt CPU processes are carried out correctly. Check the PIC/PIT/RTC/CMOS or Clock chip(s).
8254 PIT	Check that proper setup and hold times are given to the PIC for interrupts of the CPU processes. Check the PIT or Clock chip.
82385 Cache Controller	This is normally responsible for cache and shadow memory.
CMOS RAM Configuration Data	Check information in CMOS RAM before further testing so any failures after this could also be down to the CMOS chip.
CRT controllers	Test any video adapters listed in the CMOS.
RAM above 64K	Perform a walking-bit test on memory above 64K listed in the CMOS.
Keyboard	Test interface to the keyboard including scan code stuck keys etc.
Pointing Device (mouse etc)	Test and initialize vector for any pointing devices found. Failure to see a device may be down to the device itself but there may be a problem with the CMOS or 8042/8742.

Procedure	Meaning
Diskette Drive A:	Test and initialize the A: drive.
Serial Interface Circuitry	Test any RS232 devices found at the proper I/O address.
Diskette Controllers	If an A: drive has been found further testing is performed before proceeding to the bootloader. This test includes reading the first sector of any diskette in the drive to see if a valid boot code is there.
Fixed Disk Controllers	Test and initialize any hard drives set in the CMOS including reading the first sector of the hard drive to see if a valid boot code exists.

XT (Port 60)

The PC uses an irregular way of sending codes to ports 10 and 11, which makes it impractical to monitor them on a POST card. The XT, on the other hand, uses three methods; before initializing the display, it issues a few codes to port 60 (the 8255 controller for the keyboard) for critical system board errors. It beeps to indicate successful or unsuccessful POST, and displays error messages.

After initializing the display, it writes error codes to memory address 15, which are sent to the screen to make up part of other error messages.

Code	Meaning
00 or FF	CPU register test failed
01	BIOS ROM (ROS) checksum failed
02	Timer I failed
03	8237 DMA register write/read failed or unexpected timer 1 request for DMA ch 1
04	After enabling port 213 expansion box, base 32K memory write/read of AA, 55, FF, 01 and 00 test failed; POST output alternates between POST code and failing bit pattern.
	Size memory, initialize the 8259 PIC, setup BIOS interrupt vectors in RAM, read the configuration switches, poll the manufacturing jumper. If installed, load the manufacturing test via the keyboard port and run it. If not, initialize the rest of the system.

AT POST Codes

Code	Meaning
00	Main board damaged
01	80286 test in real mode; verify read/write registers, flags and conditional jumps.
02	ROM checksum test—test 32K ROMs; POST BASIC and BIOS.
03	Test CMOS shutdown byte—rolling bit pattern and verified at shutdown address.
04	8254 timer 1; all bits on; set timer count; check all bits on.
05	8254 timer 1; all bits off; set timer count; check all bits off.
06	8237 DMA 0 initialization channel register test. Disable DMA controller; r/w current address to all channels
07	8237 DMA 1 initialization channel register test. Disable DMA controller; r/w current address to all channels

Code	Meaning
08	DMA page register test—r/w all page registers. Check 74LS612.
09	Storage refresh test—verify refresh occurring. 8042 i/face test I/O issue self test; check 55H received
0A	Keyboard controller test 1; Soft reset
0B	Keyboard controller test 2; Reset 8042
0C	Keyboard controller test 3; Test switch settings
0D	Keyboard controller test 4: Write byte 0 of 8042 mem; issue comd to 8042, await response.
0E	Base 64K r/w memory test—r/w data patterns AAh, 55h.
0F	Get I/P buffer switch setting. Also Base 64K r/w memory test #2—r/w data patterns AAh, 55h.
10	Roll error code to MFG Port
11	Initialize display row count. Verify 286 LGDT.SGDT LIDT/SIDT instruction
12	Protected mode register test failure
13	Initialize 8259
14	Setup interrupt vector to temp interrupt
15	Establish BIOS interrupt call subroutine vectors. Verify CMOS checksum/battery OK
16	Set data segment or Check CMOS battery condition.
17	Set defective battery flag or CMOS checksum error.
18	Ensure CMOS dividers set or enable protected mode.
19	Set return address byte in CMOS.
1A	Set temporary stack or protected mode test. Determine memory size; verify parity.
1B	Segment address 01-0000 (second 64K memory test)
1C	Set or reset; check 512—640 memory installed
1E	Set (expanded?) memory size determined in CMOS; or determine memory size above 1024K.
1F	Test address lines 19-23
20	Fatal addressing error; Shutdown.
21	Return 1 from shutdown. Initialize and start CRT controller (6845); test video r/w; test video enable; select alpha mode; w/r patterns; or check CMOS config data.
22	Enable video signal and set mode; CRT interface test; verify video enable and horizontal sync. Video card initialization failure or invalid switch setting.
23	Check for advanced video card; Video card initialization failure or invalid switch setting.
24	8259 PIC test -r/w interrupt mask register with 1s and 0s; mask device interrupts off.
25	Check for hot interrupts; test interrupt mask registers.
26	Display 101 error; Check for unexpected interrupts.
27	Check the converting logic (106 error)
28	Check hot NMI interrupts (error 107)
29	Test data bus to timer 2 (error 108). 8253 timer register failure.
2A	8253 Timer speed failure (error 102)
2B	Too fast; or 8253 Timer interrupt initialization.
2C	Too slow; or Timer 0 interrupt failure (error 103)
2D	Check 8042 (k/b controller) for last command excepted (error 105)
2F	Check for warm boot
30	Set shutdown return 2; Protected mode r/w memory test step 1.

Code	Meaning
31	Enable protected mode; Protected mode r/w memory test step 2.
32	Address lines 0-15
33	Next block of 64K; Protected mode r/w memory test step 3.
34	Restore checkpoint; Protected mode r/w memory test step 4.
35	Keyboard test; Check for manufacturing burn in test.
36	Check <AA> scan code; keyboard clock error.
38	Error—check 8042 working; also 37 and 39
3A	Initialize 8042; keyboard locked
3B	Check for ROM in 2K blocks
3C	Check for floppy diskette drive
3D	Initialize floppy for drive type
3E	Initialize hard drive
3F	Initialize printer; non-fatal error; press F1 to continue.

Additional Protected Mode Tests

Code	Meaning
40	Enable hardware interrupt if 80287; initialization
41	System code @ segment code E000.0
42	Exit to system code
43	Go to boot loader diskette attachment test
44	Boot from fixed disk
45	Unable to boot; go to BASIC
81	Build descriptor table
82	Switch to virtual mode
90-B6	EXEC_00 to EXEC_31 & SYS_32 to SYS_38 tests; memory test; boot loader.
DD	Transmit error code to MFG_PORT
F0	Set data segment
F1	Interrupt test (programming interrupt 32)
F2	Exception interrupt test
F3	Verify 286 LDT/SDT and LTR/STR instructions.
F4	Verify 286 bound instruction
F5	Verify push and pop all instruction; stack/register test.
F6	Verify access rights function correctly.
F7	Verify Adjust RPL field of selector instructions (ARPL) functions
F8	Verify LAR function
F9	Verify LSL i(Load Segment Limits) instruction
FA	Low meg chip select test

PS/2 (Micro Channel) POST Codes

Code	Meaning
00	CPU test; FFAA0055 pattern
01	32 bit CPU register test; setup system timer
02	System ROM checksum
03	Test system enable/system port 94 enable/check
04	Test system POS register; port 102 enable/check
05	Test adapter setup port; POS port 96 enable/check
06	Test RTC/CMOS shutdown byte; Byte 0F CMOS (NMI disable)

Code	Meaning
07	Test extended CMOS location; ports 74-76 test
08	Test DMA & page register 8 channels; ports 2
09	Initialize DMA command & mode registers
0A	Test refresh (port 61)
0B	Test keyboard controller buffers (8042—port 61
0C	Keyboard controller self test (8042—port 60)
0D	Keyboard controller test continuation (8042)
0E	Keyboard self test error indicated (port 64)
0F	Setup system memory configuration
10	Test first 512K RAM in real mode
11	Half system if memory test error
12	Verify LGDT/SGDR LIDT/SIDT (keyboard commands)
13	Initialize PIC #1 (Master)
14	Initialize PIC #2 (Slave)
15	Initialize A20 interrupt vectors
16	Setup extended vector table
17	Check power RTC/CMOS power good signal (byte 0D)
18	Check RTC/CMOS checksum
19	RTC/CMOS lost power (0D 80h)
1A	Skip memory test in protected mode if warm reset
1B	Prepare for shutdown; protected mode initialization
1C	Setup stack pointer point to the end of first 64K
1D	Decide low memory size in protected mode; Size base memory
1E	Save memory size detected
1F	Setup system memory split address
20	Check for extended memory beyond 64 Mb
21	Test memory address bus lines
22	Clear parity error and channel check; Disable NMI
23	Initialize interrupt 00; system timer
24	Determine CMOS validity
25	Write keyboard controller (8042) command byte
40	Check valid CMOS and video
41	Display error code 160. Check CMOS, AC ripple.
42	Test PIC #1 & PIC #2 registers; Master/Slave test
43	Test PIC #1 & PIC #2 registers with another pattern
44	Check for interrupt with interrupt masked; check for NMI when disabled.
45	Test NMI
46	NMI error detected
47	Test system timer 0
48	Check stuck speaker clock; speaker bitstuck test
49	Test timer 0 count
4A	Test timer 2 output
4B	Check if timer interrupt occurred
4C	Test timer 0 for count too fast or slow
4D	Verify timer 0 interrupt
4E	Check 8042 ready for command; buffer free
4F	Check for soft reset
50	Prepare for shutdown/protected mode
51	Start protected mode test
52	Test memory in 64K increments

Code	Meaning
53	Check if memory test done
54	Shutdown system and return to real mode
55	Test for manufacture or regular test; test for loop. Check jumper.
56	Disable keyboard
57	Check for keyboard self test
58	Keyboard test passed; check for errors
59	Test keyboard interface
5A	Initialize mouse
5B	Disable mouse
5C	Initialize interrupt vectors
5D	Initialize interrupt vectors
5E	Initialize interrupt vectors
5F	BIOS data area
60	Determine diskette rate
61	Reset floppy controller/drive
62	Floppy drive test
63	Turn floppy motor off
64	Serial port setup
65	Enable/test RTC interrupt
66	Configure floppy drives
67	Configure hard drive
68	Enable system CPU arbitration; wait states
69	Scan for optional ROMs
6A	Verify serial and parallel ports
6B	Setup equipment byte
6C	Setup configuration errors reported
6D	Set keyboard typematic rate
6E	Reset page register; boot up system (Int 19 bootloader)
70	Reset disk
71	Read bootcode for E6/E9
72	Control to bootcode
73	Bootcode/ROM Basic

Landmark

BIOS came with POST card and replaced that in motherboard being tested; same as BIOSYS BIOS. Beeps as for IBM AT. Codes sent to ports 280 and 80.

XT Jumpstart

Code	Meaning
01	Jump to reset area in ROM BIOS
02	Initialize DMA page register
03	Initialize DMA refresh register
04	Clear all RAM
05	Perform RAM test on 1st 64k
06	Clear 1st 64k
07	Initialize BIOS stack to 0:FC0
08	Set the equipment flag based on switches
09	Initialize default interrupt vectors

Code	Meaning
0A	Initialize 8255 if it exists and enable parity
0B	Initialize 8259 and enable interrupts
0C	Setup adapters and peripherals
0D	Setup video
0E	Initialize video
0F	Initialize equipment
10	Initialize memory configuration in RAM (currently = 64K)
11	Setup timer function
12	Initialize timer function
13	Setup time of day function
14	Initialize time of day function
15	Setup and init print screen function
16	Setup and init cassette function
17	Setup and init bootstrap function
18	Setup and init keyboard function
19	Enable speaker
1A	Setup timer 0 for the real time clock
1B	Enable RTC
1C	Setup timer 2 for the beeper
1D	Size memory: write 55AA/AA55 to 1st/last word in segment
1E	Read 1st and last word of segment
1F	Compare 1st and last words
20	Report determined memory size to screen
21	Perform checksum on ROM BIOS
22	If cold boot perform complete RAM testing
23	Move system stack to bottom of memory and save pointer at 40:0E
24	Reset parity after RAM sizing
25	Enable timer and keyboard interrupts
26	Setup the serial and parallel ports
27	Setup the game port
28	Setup the floppy disk controller
29	Scan for optional ROM in 2K chunk from C8000 to start of BIOS
2A	Boot System

AT Jumpstart

Code	Meaning
03	1 short beep when first awake
04	Initialize bell tone
05	Enable CMOS RAM
06	Reset video controller
07	Disable I/O parity
08	Start memory refresh
09	Clear reset flag in RAM
0A	Test DMA page registers
10	Use CMOS to determine if soft reset
11	Perform ROM checksum
12	Test timer A
13	Test DMA channel A
14	Test DMA channel B

Code	Meaning
15	Test refresh
16	Flush 8042 input buffer
17	Reset 8042
18	Get keyboard switch
19	Initialize keyboard
1A	Clear any existing parity
1B	Enable on-board parity
1C	Test base 64K memory
1D	Test base 64k parity
1E	Initialize POST stack
20	Put keyboard # in RAM
65	Set video speed
21	Test protected mode registers
22	Initialize 8259 interrupts
23	Zero all 256 interrupts
24	Initialize interrupts 0-1fh
25	Perform DRAM checksum
26	Adjust configuration based on hardware found
27	Check manufacturing switch (may exit POST)
28	Initialize video controller
2A	Test video memory
2B	Test video sync
2C	Look for external video
2D	Change video configuration if external video
2E	Unused
2F	Initialize video controller
30	Change video interrupt
31	Print any POST messages
32	Size memory by testing it
33	Adjust memory configuration
33	Verify CMOS RAM size
34	Enable I/O parity
35	Test 8259
36	Bytes swap test
37	Test NMI
38	Timer test
39	Initialize timer A
3A	Protected mode memory test
3B	Test keyboard
3C	Test keyboard interrupt
3D	Enable A20
3E	Reset hard disk controller
3F	Setup floppy controller
40	Test floppies
41	Setup keyboard (NUMLOCK)
42	Enable timer interrupt
43	Check for dual floppy/hard disk controller
44	Find floppy drive A type
45	Find floppy drive B type
46	Reset hard disk
47	Enable slave DMA

Code	Meaning
63	Set video interrupt vector
48	Call any external ROMs
49	Initialize printer
4A	Initialize serial
4B	Initialize 80287
4C	Read CMOS RAM status
4D	Check CMOS configuration against hardware found
70	Check CMOS configuration against memory found
4E	Initialize timer ticks
4F	Enable IRQ9
50	Enable on-board parity
51	Call add-on card ROM
52	Enable keyboard interrupt
53	Reset printer
60	Check for any errors
61	One short beep
62	Print sign-on message
64	Perform boot

Magnavox

See *Philips*.

MR BIOS

The last code emitted is the one that failed. There may also be a message on screen. Beep codes are in a binary format and are preceded by a high and low tone (described elsewhere). Check also *Nasty Noises* for more codes.

POST Procedures

Procedure	Meaning
Reset	See if a warm boot (Ctrl+Alt+Del) or a cold boot (Reset) is needed.
Chipset Initialization	Reset the support chips (8259) DMAs and timers to defaults before proceeding.
Disable Chips	Disable NMI/DMA and Video (6845) to get accurate results later. Failure here is normally a NMI generated by one of the disabled chips.
ROM BIOS Checksum	Perform checksum test, add a preset value stored in BIOS to create value of 00.
DMA Test	Perform a test of the page registers in the DMA controller.
Keyboard Controller Test	Send a command to the 8042 keyboard controller to perform a selftest. The keyboard controller will return a buffer and error buffer address.
Chipset Initialization	Initialize the DMA (8237)/PIC (8259)/PIT (8254) and RTC chips.

Procedure	Meaning
DMA Test	Test the registers of the master 16-bit and slave 8-bit DMA controllers by writing bit patterns and reading the results.
Cache/Shadow Disable	Disable cache and shadow RAM before processing with POST.
Refresh	Test interval in which PIT (8254) chip sends a refresh signal to the DMA chips.
Base 64K Memory Test	Test the first 64K of system memory with a walking-bit pattern.
PIC Test	Test the mask registers of the master and slave interrupt controllers by setting the mask-bit in the registers and generating an interrupt to see if the interrupt is trapped. Then test the additional registers in the PICs with a walking-bit pattern.
PIT Test	Test the interrupt timer channels 0-2 and initialize if no failures occur.
RTC	Perform read/write test of RTC portion of CMOS and initialize if no failures occur.
Video	Test and initialize the video adapter, which will perform an internal diagnostic and sign on before returning an OK status.
CMOS Checksum	Perform a checksum on the system RAM.
Keybd Initialization	Initialize the keyboard and read the buffer address for errors.

OEM Specific

Procedure	Meaning
Base Memory Test	Test memory addresses between 64-640K with a walking-bit pattern. There may be a hex display of the failing it.
Keyboard 2nd Init	Tries again if the first failed.
Protected Mode Test	Test the ability of the keyboard controller address line 20 to respond to commands that switch the CPU in and out of protected mode.
Extended Memory Test	Test addresses above 1 Mb in 64K blocks and perform pattern tests.
OEM Memory	Normally test the cache controller and shadow RAM.
RTC Time Test	Test the write active line of the RTC/CMOS chip. Check bad CMOS/battery
Serial Port	Generate an interrupt of the CPU through I/O ports reserved for RS232 devices. Failure to see a device could be the device itself or more than one set to the same port. Checks are only made for two devices.
Parallel	Check for parallel devices. Failure to see a device could be the device itself or more than one using the same port. Checks are only made for three.
NPU Test	Perform a register test on the NPU then initialize if passed.
Floppy Test	Test floppy controller and drive.
Fixed Disk	Test fixed disk controller and drive and compare the results against the CMOS setting. This is skipped if no

Procedure	Meaning
	drive is installed.
CMOS Update	Update information in CMOS RAM based on the previous results.

Non-Fatal Errors

Procedure	Meaning
Lock Check	Check if a system lock-byte is set and wait for user response if an error is generated. Check the panel lock or circuitry.
NumLock/Pwd/Setup	Set NumLock on (if set) and ask for password (if set) and display setup message.
Typematic Rate	Set the typematic rate.
Floppy Disk	Perform any further initialization needed.
Hard Disk	Perform any further initialization needed.
Video Mode	Set primary video mode and display any errors found during initialization routines.
Shadow/Cache Enable	
Adapter ROM	Initialize adapters with a ROM signature of 55AA. Self tests will be performed by the equipment concerned before handing back control to the POST.
Video Monitor Mode	Set the video mode based on the information in the CMOS and update the time variables from the RTC.
Parity/NMI Enable	Enable NMI by setting bit 7 of CMOS address 41 and enable parity. There should be no failures during this.
Set Stack	Set the last significant byte of the stack pointer and install the shadow RAM at E000 if set by CMOS.
Acknowledge	Acknowledge errors and set primary video mode before calling Int 19 boot loader. Errors reported will await a keyboard response before proceeding. Errors beyond this point are normally software related.

POST Codes (inc 3.4x)

Code	Meaning
00	Cold-Boot commences (Not seen with warm-boot). Output EDX register to I/O ports 85h, 86h, 8Dh, 8Eh for later use
01	HOOK 00 OEM specific typically resets chipset to default. Initialize any Custom KBD controller, disable CPU cache, cold initialize onboard I/O chipset, size & test RAM, size cache
02	Disable critical I/O: 6845s CRT; 8237s DMA; 7675 floppy and parity latches (monitor, DMA, FDC, I/O ports, Speaker, NMI).
03	BIOS checksum test
04	DMA Page register test (Ports 81-8F)
05	8042 (Keyboard Controller) Self test. Enable A20 Gate.
06	Init ISA I/O: Game Port: 8237 master/slave; 8254 ch2/1; RTC Reg3 F/A; 8259 master/slave
07	HOOK 01. OEM specific; typically disables cache/shadow/ or memory refresh circuit test, or warm initialize custom KBD controller, warm initialize onboard I/O chipset.

Code	Meaning
08 (09?)	Refresh toggle test (PORTB)
09 (08?)	Pattern test master/slave 8237s; eight 16-bit regs each
0A	Base 64K memory test—check beep code.
0B	Pattern test master/slave 8259 mask regs
0C	8259/IRQ tests purge powerup ints—check beep code. Test 8259 Slave, test 8259 slave's interrupt range, initialize interrupt vectors 00-77h, init KBD buffer variables.
0D	8254 channel-0 test and initialization
0E	8254 channel-2 toggle test speaker circuitry
0F	RTC tests/inits: Init REG-B; write/readback NVRAM. PIE test
10	Video Initialization; display cold boot sign-on message or possible error messages.
11	CMOS Checksum test
12	Sign-on msg. Accept KB BAT; perform 1st try KB unit; cold boot delay
13	HOOK 02. OEM specific; select 8MHz bus
14	Size/Test base memory (low 64K already done)
15	Perform 2nd try KB init if necessary
16	HOOK 03. OEM specific. Size/Test cache
17	Test A20 gate off; then on; stuck in asserted state.
18	Size/Test extended memory
19	HOOK 04 and Size/Test system memory ("special" OEM memory)
1A	Test RTC Update-In-Progress and validate time; RTC settings invalid.
1B	Serial port determination off-board/on-board
1C	Parallel port determination off-board/on-board
1D	Copro determination/initialization
1E	Floppy controller test/determination CMOS validation
1F	Fixed Disk controller test/determination CMOS validation
20	Rigorous CMOS parameter validation display other config changes
21	Front-Panel lock check; wait for user to acknowledge errors
22	Set NumLock; Password-Security Trap; despatch to setup utility
23	HOOK 05. OEM specific. Final determination of onboard Serial/Parallel ports.
24	Set typematic rate
25	Floppy subsystem initialization
26	Fixed subsystem initialization
27	ACK errors; set primary adapter video mode
28	HOOK 06. OEM specific; typically enables shadow, cache, turbo. Cyrix WB-CPU support, Green PC: purge 8259 slave, relieve any trapped IRRs before enabling PwrMgmt, set 8042 pins, Ctrl-Alt-Del possible now, Enable CPU Features.
29	Disable A20-gate; set low stack, install C800, E000 ROMs.
2A	ACK errors; set video mode, set DOS time variables from RTC.
2B	Enable parity checking and NMI
2C	Set low stack, Install E000 ROM
2D	ACK errors, set primary video mode.
2E	HOOK 07. OEM specific. Log-in EMS (if built-in). Fast A20: Fix A20.
2F	Purge 8259 slave; relieve any trapped IRRs before enabling Green-PC. Pass control to INT 19.
32	Test CPU Burst
33	Reserved

Code	Meaning
34	Determine 8042, Set 8042 Warm-Boot flag STS.2
35	Test HMA Wrap, Verify A20 enabled via F000:10 HMA
36	Reserved
37	Validate CPU: CPU Step NZ, CPUID Check. Disable CPU features
38	Set 8042 pins (Hi-Speed, Cache-off)
39	PCI Bus: Load PCI; Processor Vector init'd, BIOS Vector init'd, OEM Vector init'd
3A	Scan PCI Bus
3B	Initialize PCI Bus with intermediate defaults
3C	Initialize PCI OEM with intermediate defaults, OEM bridge
3D	PCI Bus or PLUGnPLAY: Initialize AT Slotmap from AT-Bus CDE usage
3E	Find phantom CDE ROM PCI-cards
3F	PCI Bus: final Fast-Back-to-Back state
40	OEM POST Initialization, Hook Audio
41	Allocate I/O on PCI-Bus, logs-in PCI-IDE
42	Hook PCI-ATA chips
43	Allocate IRQs on the PCI Bus
44	Allocate/enable PCI Memory/ROM space
45	Determine PS/2 Mouse
46	Map IRQs to PCI Bus per user CMOS, Enable ATA IRQs.
47	PCI-ROM install, note user CMOS
48	If Setup conditions: execute setup utility
49	Test F000 Shadow integrity, Transfer EPROM to Shadow-RAM
4A	Hook VL ATA Chip
4B	Identify and spin-up all drives
4C	Detect Secondary IRQ, if VL/AT-Bus IDE exists but its IRQ not known yet, then autodetect it
4D	Detect/log 32-bit I/O ATA devices
4E	ATAPI drive M/S bitmap to Shadow-RAM, Set INT13 Vector
4F	Finalize Shadow-RAM variables
50	Chain INT 13
51	Load PnP, Processor Vector init'd, BIOS Vector init'd, OEM Vector init'd
52	Scan PLUGnPLAY, update PnP Device Count
53	Supplement IRQ usage—AT IRQs
54	Conditionally assign everything PnP wants
58	Perform OEM Custom boot sequence just prior to INT 19 boot
59	Return from OEM custom boot sequence. Pass control to 1NT 19 boot
5A	Display MR BIOS logo
88	Dead motherboard and/or CPU and/or BIOS ROM.
FF	BIOS POST Finished.

Msg	Low-High	Problem
03	LH-LLL	ROM-BIOS Checksum Failure
04	LH-HLL	DMA Page Register Failure

Msg	Low-High	Problem
05	LH-LHL	Keyboard Controller Selftest Failure
08	LH-HHL	Memory Refresh Circuitry Failure
09	LH-LLH	Master (16 bit) DMA Controller Failure
09	LH-HLH	Slave (8 bit) DMA Controller Failure
0A	LH-LLLL	Base 64K Pattern Test Failure
0A	LH-HLLL	Base 64K Parity Circuitry Failure
0A	LH-LHLL	Base 64K Parity Error
0A	LH-HHLL	Base 64K Data Bus Failure
0A	LH-LLHL	Base 64K Address Bus Failure
0A	LH-HLHL	Base 64K Block Access Read Failure
0A	LH-LHHL	Base 64K Block Access Read/Write Failure
0B	LH-HHHL	Master 8259 (Port 21) Failure
0B	LH-LLLH	Slave 8259 (Port A1) Failure
0C	LH-HLLH	Master 8259 (Port 20) Interrupt Address Error
0C	LH-LHLH	Slave 8259 (Port A0) Interrupt Address Error
0C	LH-HHLH	8259 (Port 20/A0) Interrupt Address Error
0C	LH-LLHH	Master 8259 (Port 20) Stuck Interrupt Error
0C	LH-HLHH	Slave 8259 (Port A0) Stuck Interrupt Error
0C	LH-LHHH	System Timer 8254 CH0 / IRQ0 Interrupt Failure
0D	LH-HHHH	8254 Channel 0 (System Timer) Failure
0E	LH-LLLLH	8254 Channel 2 (Speaker) Failure
0E	LH-HLLLH	8254 OUT2 (Speaker Detect) Failure
0F	LH-LHLLH	CMOS RAM Read/Write Test Failure
0F	LH-HHLLH	RTC Periodic Interrupt / IRQ8 Failure
10	LH-LLHLH	Video ROM Checksum Failure at Address XXXX Mono Card Memory Error at Address XXXX Mono Card Memory Address Line Error at XXXX CGA Card Memory Error at Address XXXX CGA Card Address Line Error at Address XXXX
11	(None)	Real Time Clock (RTC) Battery is Discharged
11	(None)	Battery Backed Memory (CMOS) is Corrupt
12	LH-HLHLH	Keyboard Controller Failure
14/18/19	LH-LHHLH	Memory Parity Error
14/18/19	LH-HHHLH	I/O Channel Error
14		
18		
19	(None)	RAM Pattern Test Failed at XXXX Parity Circuit Failure in Bank XXXX Data Bus Test Failed: Address XXXX Address Line Test Failed at XXXX Block Access Read Failure at Address XXXX Block Access Read/Write Failure: Address XXXX Banks Decode to Same Location: XXXX and YYYY
15	(None)	Keyboard Error—Stuck Key Keyboard Failure or no Keyboard Present
17	LH-LLLHH	A20 Test Failure Due to 8042 Timeout

Msg	Low-High	Problem
17	LH-HLLHH	A20 Gate Stuck in Disabled State (A20=0)
17	(None)	A20 Gate Stuck in Asserted State (A20 Follows CPU)
1A	LH-LHLHH	Real Time Clock (RTC) is Not Updating
1A	(None)	Real Time Clock (RTC) Settings are Invalid
1E	(None)	Diskette CMOS Configuration is Invalid Diskette Controller Failure Diskette Drive A: Failure Diskette Drive B: Failure
1F	(None)	Fixed Disk CMOS Configuration is Invalid Fixed Disk C: (80) Failure Fixed Disk D: (81) Failure Please Wait for Fixed Disk to Spin Up
20	(None)	Fixed Disk Configuration Change Diskette Configuration Change Serial Port Configuration Change Parallel Port Configuration Change Video Configuration Change Memory Configuration Change Numeric Coprocessor Configuration Change
21	(None)	System Key is in Locked Position—Turn Key to Unlocked Position
29	(None)	Adapter ROM Checksum Failure at Address XXXX

Mylex/Eurosoft

Derived from Eurosoft BIOS.

4.71

Pass	Fail	Meaning
03	04	DMA page registers test
05	06	Keyboard reply test
07	08	Keyboard self-test
09	0A	8042 keyboard controller able to read links
0B		RATMOD/DIAG link
0C	0D	Keyboard acceptance of 60H
0E	0F	Keyboard acceptance of parameter
10	11	Read keyboard command byte
12	13	Keyboard command byte came back
14	15	RAM refresh toggle test
16	17	RAM bit test
18	19	RAM parity test
1A	1B	CMOS RAM test
1C	1D	CMOS RAM battery test
1E	1F	CMOS RAM checksum test
	20	CMOS RAM battery fault bit set
21	22	Master DMA controller test
21	23	Slave DMA controller 2 test
24		Protected mode entered safely

Pass	Fail	Meaning
25		RAM test completed
26	27	BIOS ROM checksum test
28		Protected mode exit
29	2A	Keyboard power-up reply received test
2B	2C	Keyboard disable command acceptance test
	2D	Video display presence check
	2E	POST Errors were reported
	2F	About to halt
30		Protected mode entered safely (2)
31		RAM test complete
33		Master interrupt controller test
34	35	Slave interrupt controller test
36	37	Chipset initialization
38	39	System BIOS shadowed
3A	3B	Video BIOS shadowed

EISA/ISA

Code	Meaning
1	Always present—indicates start of beep coding
2	Video adapter bad or not detected
3	Keyboard controller error
4	Keyboard error
5	8259 Programmable Interrupt Controller (PIC) 1 error
6	8259 PIC 2 error
7	DMA page register failure
8	RAM refresh error
9	RAM data test failed
10	RAM parity error occurred
11	8237 DMA controller 1 failed
12	CMOS RAM failure
13	8237 DMA controller 2 failed
14	CMOS RAM battery failure
15	CMOS RAM checksum error
16	BIOS ROM checksum error

Code	Meaning
01	Processor test
02	DMA Page Register
03	8042 keyboard controller
04	BIOS ROM Checksum error
05	Send keyboard command test bad
06	CMOS RAM Test
07	RAM Refresh Test
08	1st 64K memory test
09	8237 DMA controller test
0A	Initialize DMA controller
0B	Interrupt Test
0C	Determine RAM size

Code	Meaning
0D	Initialize video
0E	EGA/VGA ROM checksum test failed
10	Search for monochrome card
11	Search for color card
12	Word splitter and byte shifter test failed
13	Keyboard Test
14	RAM Test failed
15	Timer test error
16	Initialize output port of keyboard controller
17	Keyboard interrupt test
18	Initialize keyboard
19	RTC clock test failure
1A	Maths copro test failure
1B	Reset hard/floppy controller
1C	Initialize floppy drive
1D	Initialize hard drive
1E	Initialize ROMs in C000-DFFF
1F	Initialize serial and parallel ports
20	Initialize time of day in RTC
21	Initialize ROMs in E000-EFFF
22	Look for boot device
23	Boot from floppy disk
24	Boot from hard disk
25	Gate A20 enable/disable failure
26	Parity error occurred
30	DDNIL bit scan failure
FF	Fatal error occurred and system halted

NCR

Purchased in 1991 by AT&T. 3 main types of motherboards: OEM from AMI, AT and Micro channel clones. See AMI pre-0490 for PC386, and below for others. All NCR-designed systems send POST codes to LPT1, but see table.

Architecture	Typical PC	BIOS	POST Code Port
XT	PC6	NCR	378 or 3BC (LPT 1)
AT (ISA)	3728, 3204, PC 916	NCR	80 and 378 or 3BC (LPT 1)
	PC386	AMI Pre-0490	80
Micro Channel	3421	Phoenix	680 and 3BC

PC6

Code	Meanings
AA	8088 CPU failure
B1	2764 EPROM checksum failure
B2	8237 DMA controller failure
B3	8253 timer failure
B4	RAM failure. Halts if error in first 64K, otherwise displays MEMORY ERROR.
B5	8259 interrupt controller failure. Displays INTERRUPT FAILURE
B6	RAM Parity error. Displays ERROR IN BASE MEMORY or ERROR ON EXPANSION CARD.
BB	All tests passed

3302/3304/3728/PC916SX

Code	Meaning
01	Test CPU registers
02	Test system I/0 port—write and read port 61 to confirm it will handle RAM refresh.
03	Test ROM BIOS checksum
04	Test DMA page registers
05	Test timer channel 1 (refresh)
06	Test timer channel 2 (speaker)
07	Test RAM refresh logic. Also verifies timer is working.
08	Test base 64K RAM
09	Test 8/16 bit bus conversion
0A	Test interrupt controller 1
0B	Test interrupt controller 2
0C	Test I/O controller
0D	Test CMOS RAM read/write
0E	Test for battery power low or interrupted since last test
0F	Test CMOS RAM checksum
10	Test CPU protected mode
11	Test video configuration in CMOS RAM or display switch
12	Test primary video controller
13	Test secondary video controller
20	Display results of tests to this point
21	Test DMA controller 1
22	Test DMA controller 2
23	Test Timer channel 0 (system timer tick)
24	Initialize interrupt controllers
25	Test interrupts
26	Test interrupts
30	Check base 640K memory size
31	Check extended memory size
32	Test higher 8 address lines
33	Test base memory
34	Test extended memory
40	Test keyboard—enable/disable
41	Test keyboard—reset
42	Test keyboard—clock low

Code	Meaning
43	Test keyboard—for interrupt, enable keyboard, init pointers, write out subcommand
44	Test 8086 address overrun compatibility (gate A20)
50	Set up hardware interrupt vectors
51	Enable interrupt from timer channel 0
52	Security ROM
60	Test floppy disk controller and drive
61	Test hard disk controller
62	Initialize floppy drives
63	Initialize hard drives
70	Test real time clock
71	Set time of day in real time clock
72	Check parallel interfaces
73	Check serial interfaces
74	Check for and execute adapter option ROMs
75	Check if math coprocessor is installed and enable interrupt
76	Enable keyboard and real time clock interrupts
F0	System not configured correctly, or hardware defect
F1	Scan for and execute motherboard option ROMs
F2	INT 19 to boot operating system—No POST errors.

PC916 5/6

*halt on error if loop jumper installed in keyboard connector

Code	Meaning
01	Test CPU registers, reset video cards, display diagnostic messages
02	Verify port 61, disable non-maskable interrupt, start speaker timer channel 2
03	Test ROM BIOS checksum
04	Test DMA page registers
05	Test timer channel 1 (refresh)
06	Test timer channel 2 (speaker)
07	Test refresh logic by reading port 61 bit 4 every 15 microseconds
08	Test base 64K RAM
09	Test 8/16-bit bus converting logic, initialize both interrupt controllers
0A	Test interrupt mask register A
0B	Test interrupt mask register B, write temporary interrupt vector table for INT 00-77
0C	Test 8042/8742 keyboard controller
0D	Test CMOS RAM shutdown byte
0E*	Test CMOS RAM battery power low or interrupted since last test
0F*	Test CMOS RAM checksum; initialize periodic rate
10	Test CPU protected mode
11	Test video configuration in CMOS RAM or display switch, look for advanced video card ROM in segment C000, initialize interrupt vectors.
12	Initialize and test primary video controller
13	Primary video error, test secondary video controller
14	Test disabling Speed stretch enable/disable port 69 bit 0=1
15	Start refresh timer 1 counter 1, disable speed switch timer 2, counter 2

Code	Meaning
16	Enable then disable speed stretch enable/disable port 69 bit 0
17	Clear write protect bit
18	Write/verify global/local/interrupt descriptor table registers; copy ROM BIOS to shadow RAM F000
19	Verify RAM to ROM BIOS copy OK; reinitialize restart vector, check and execute for burn-in ROM D000. Disable real time clock in CMOS status reg B, reset and initialize video cards.
IA	Command 8042 to execute self-test and verify result
1B	Test 64K Shadow RAM in segment F000
20	Display results of tests to this point
21	Test DMA controller 1
22	Test DMA controller 2 and initialize all 8 channels
23	Test timer 1 counter 0 840 ns clock timer for IRQ0 (INT8)
24	Initialize both interrupt controllers
25	Check for unexpected (hot) interrupts
26	Wait for interrupt
27*	Test timer 2 counter 0 for NMI (INT02), failsafe
28*	Test timer 2 counter 1 (INT72-74)
30	Check base 640K memory size
31	Check extended memory size (max 256M RAM on 5.2, 6 BIOS)
32	Test higher 8 address lines for mirror addresses (5.x BIOS)
33*	Test base memory
34*	Test extended memory (up to 256M)
35*	Test RAM in E000 (v6 BIOS—also test keyboard shutdown command FE—shutdown path 0B)
40	Test keyboard—enable/disable
41	Test keyboard—reset command FF (halt on error if loop jumper not installed)
42	Test keyboard—clock low (halt on err if loop jumper not installed)
43	Test keyboard—check for interrupt, enable keyboard, initialize buffer pointers, verify keyboard unlocked, disable external interrupts mask A=F, turn on write protect for RAM E000-FFFF, write out subcommand (halt on error if loop jumper not installed).
44	Test address overrun compatibility (turn off gate A20, 8042 P2 bit 1 = 0)
45	v6 BIOS—Init mouse, en IRQ1 (INT09)keyboard (15 IRQs, 1 disabled), disp "Press F1 for Setup".
50	Set up hardware interrupt vectors 0-15, 70-77
51	Enable IRQ0 interval interrupt 08 from timer channel 0; enable external interrupts (STI)
60	Test for floppy/hard disk controller and drive
61	Test cylinder register for disk controller
62	Initialize floppy drives
63	Initialize hard drives
70*	Test real time clock
71	Set interval timer RAM counts
72	Configure and test parallel interfaces
73	Configure and test serial interfaces
74	Check for and execute adapter option ROMs C8000-DFFFF
75*	Test math coprocessor if installed, and enable interrupt
76	Enable keyboard and real time clock IRQ8 (INT 70) interrupts; enable slave interrupt controller 2 via PIC 1 mask bit 2=0.

Code	Meaning
F0	Display logged errors. Halt if locked; loop if loop jumper installed
F1	Test system code at segment E000 (v5.x BIOS only); v6 BIOS—copy video ROM BIOS (if present) to shadow RAM if system ROM is absent and switch pack switch 1 is on
F2	INT 19 to boot operating system—No POST errors
F3	Go to setup if F1 key pressed. v6 BIOS: execute floppy diagnostic if Ctrl-D pressed, enable failsafe NMI port 61 bit 2=0, enable parity error port 61 bit 3=0, enable NMI.
F4	v5.x BIOS only—Display speed setting
F4	v6 BIOS—Display speed setting Auto, high, fixed
F5	v5.x BIOS only—initialize counter 2 for speed requested
F6	v5.x BIOS only—Test base memory (long test in 5.2 BIOS)
F6	v6 BIOS only—Test base memory (long test) if F2 pressed
F7	v5.x BIOS only—Test extended memory (long test in 5.2 BIOS)
F7	v6 BIOS only—Long test extended memory if F2 pressed

Olivetti

For EISA and PS/2, the code is issued after the test has passed, so a stuck code indicates the next test failed. Codes are sent to printer ports 3BC (the mono adapter's parallel port), 278, or 378; they will not be printed because no strobe data is sent. AT&Ts using the Olivetti motherboard and BIOS (e.g. the AT&T 6300) do the same.

1076/AT&T 6312/WGS 80286

The first checkpoint, 40, resets and initializes a test monitoring device on the parallel port. When an error occurs, the most recent checkpoint code sent to port 378 is exclusive-ored with 3F to complement the lower 6 bits, and then sent to 378, so if the refresh test fails (45), the POST card will show 7B because the most recent code sent before the failure was 44.

If an error occurs, the POST tries to run through a sequence of activities that display a message on the monitor, showing "tttt Error: xx", where *tttt* is the name of the failing routine, and *xx* is a suberror number. If the error is fatal, the display will show "Unrecoverable power-up error", wait for you to press F1, and return to the failing test. If video has failed, the POST will output beep codes.

Pass	Fail	Meaning
40		Dummy check—reset black box
41	7F	80286 CPU flags and register test
42	7E	Check and verify shutdown code—read keyboard status from port 64. if shutdown bit is set, read the shutdown byte from CMOS RAM (and clear the location there), check it for an illegal shutdown condition, initialize the 8259s unless shutdown is 9 or A, and jump to the correct routine to handle the shutdown: 0= warm boot (go to next test), 1= return to advanced protected mode test, 2= return to memory test above 1 Mb, 3=return to protected mode test 2, 4=INT19, 5=send EOI to 8259 and return to user routine, 9=int15 block move, and A=return to user routine.

Pass	Fail	Meaning
43	7D	Checksum test the BIOS ROMs—verify contents add up to 0.
44	7C	Test the 8253 timer—check all 3 timers for not counting, counting too slowly, or counting too fast. Suberror display is the bad timer number 0, 1, or 2.
45	7B	Start memory refresh and verify it occurs every 15.1 microseconds. Init the manufacturing test byte in RAM.
46	7A	Command the 8041 keyboard controller to do a self-test. Suberror display is 1 if error return, 2 if self-test times out.
47	79	Test the first 8K of RAM in 4 passes: 1) write into each word a data value corresponding to the address; 2) invert all bits written; 3) write an odd parity pattern; 4) write zeros. Only pass 4 is done on a warm boot. Beep once when this test passes. Install dummy interrupt vectors, set up the stack and other memory areas. display power-on banner on screen.
48	78	Test 80286 in protected mode 1—pattern test all IDT and GDT registers, verify LIDT, SIDT, LGDT, and SGDT instructions.
49	77	Test CMOS RAM shutdown byte with a pattern, then clear it.
4A	76	Test 80286 in protected mode 2—put CPU into protected mode, check it's there, then return to real mode
4B	75	Test RAM from 8K to 640K (cold boot only)—display progress for each 128K block; write, read, and compare the address and inverted address into each word.
4C	74	Test all RAM above IM—same as below 1 Mb test. Also verify CPU runs properly in protected mode.
4D	73	Test for NMI—installs NMI vector in interrupt table and small service routine. Disables I/O and memory parity errors, then checks for hot NMI.
4E	72	Test for RAM parity—turn NMI parity checking back on, and run a pattern test on the parity checking circuit, monitoring for a parity error.
50	71	Test 8259 interrupt controller 1—pattern test the mask register, install interrupt vectors for IRQs, mask them all off. look for hot interrupt coming through mask, set timer 0 to issue an interrupt, unmask it, count down, and expect the interrupt. Suberror display is l=no in, 2=timer doesn't count, 3=int occurred when masked, 4=bad mask register.
51	6F	Test 8259 interrupt controller 2—same as # 1, but no timer test is done. Suberror display is 5=int occurs wen masked, 6=bad mask register. When the test passes, install the interrupt service routine pointer in the vector table, mask off all interrupts. and display PASS message.
52	6E	Test DMA page register—marching bit test on all page registers.
53	6D	Test 8237 DMA controller 1—pattern test all read/write registers. Initialize each channel into the correct mode for BIOS. Suberror 1 display if failure.
54	6C	Test 8237 DMA controller 2—pattern test all read/write registers. Initialize each channel into the correct mode for BIOS. Suberror 3 display if failure.
55	6B	Test PIC port—write/read pattern test speaker port 61.
56	6A	Test keyboard controller—reset the keyboard and initiate self-test Suberror display is l=bad keyboard self-test completion code. 2=stuck key. 3=no keyboard interrupt Otherwise, display pass message, and set up keyboard id flags and buffer in

Pass	Fail	Meaning
		BIOS RAM area.
57	69	Test CMOS clock/calendar chip—verify accurate time keeping and display pass message.
59	68	Test 80286 advanced protected mode—tests LDT, SDT, LTR, STR, VERR, VERW, LAR, SLR, ARPL instructions; forces exception ints 13 and 5. Suberror display is 3=instruction error, 4=no exception or protection violation. Otherwise display protected mode pass message.
5A	66	Test CMOS RAM battery and display message if low.
5B	65	Test CMOS RAM non-destructively—copy contents to base memory, write/read pattern test CMOS RAM, restore contents. Suberror 2 if failure.
5C	64	Verify CMOS RAM checksum.
5D	63	Test parallel port by writing AA to 3BC, 278 and 378, and set config info in BIOS RAM area.
5E	62	Test serial port configuration—read 3FA and 3FA and assume a UART is present if values not FF. Set up port addresses and timeout values in BIOS RAM area.
5F	61	Test configuration of memory below 640K—compare memory size stored in CMOS RAM with result of earlier test. Display message to run setup if different.
60	60	Test configuration of memory above 1M—compare memory size stored in CMOS RAM with result of earlier test. Display message to run setup if different.
61	5F	Test configuration of 80287 math coprocessor chip -verify math chip same as in CMOS RAM info. Display pass or run setup message.
62	5E	Test configuration of game port at 201 and set equipment bit in BIOS RAM data area.
62	5D	Test keylock switch and wait till unlocked.
63	5D	Test hard drive configuration—initialize controller and drive. Display whether drives are present, and message to run setup if not same as CMOS RAM info.
64	5C	Configure floppy drives A and B—initialize controller and drive. Display whether drives are present, and message to run setup if not same as CMOS RAM info.
66	5B	Test option ROMs—look for signature AA5 each 2K beginning at C8000, run checksum and display error if it occurs. Otherwise pass control to the ROM so it can initialize, and display pass message when done.
		INT 19—boot the system.

M20

Not a true IBM clone, as it had a Zilog Z8001 CPU. Also, a typical POST card will not fit in a slot, so you can only monitor codes from the parallel port. The POST shows a triangle, diamond, or 4 lines on the screen to indicate early POST failure, as shown in the table.

Code	Meaning
	Program video controller using load, output, and jump relative instructions (need video).

100

Code	Meaning
Triangle	Test Z8001 CPU registers and instructions; infinite loop if failure.
Triangle	Test RAM module; infinite loop if failure; also send message to printer: E Mc bb ssss wwww. c = RAM configuration # (3 = 1 32K memory card); bb = hex 16K bank # (0,4,5,6,9,A=motherboard; 1,7,B=expansion board 1; 2=expansion board 2; 3,11,12=cxpansion board 3); ssss = what data should be; wwww = what data was (hex).
4 vertical lines	Test CPU call and trap instructions; infinite loop if failure.
Diamond	Initialize screen and printer drivers.
	Program USARTs (serial chips) and 8253 baud rate generator for keyboard at 1200 baud and RS232 at 9600. Now test remaining circuits and send codes to display and printer.
EC0	8255 parallel interface chip test failed
EC1	6845 CRT controller chip test failed
EC2	1797 floppy disk controller chip test failed
EC3	8253 timer chip test failed
EC4	8251 keyboard serial interface chip test failed
EC5	8251 RS232 serial interface chip test failed
EC6	8259 interrupt controller chip test failed
EK0	Keyboard did not respond
EK1	Keyboard responded, but self-test failed
ED1	Disk drive 1 test failed
ED0	Disk drive 0 test failed
E10	Non-vectored interrupt error
E11	Vectored interrupt error

M21/M24 (AT&T 6300)

The M24 went to the US as the AT&T 6300. It had an 8086, so was faster than the PC, albeit difficult to work on.

POST codes are sent to 378 (LPT1). If a fatal error occurs, it performs more initialization of DMA and interrupt controller circuits, tries to display an error message, complements the lower 6 bits of the POST code, sends the result to port 378, and halts the CPU, so numbers will flicker on the POST display with bit 6 on and the lower bits running from 0 upward. The codes start at 40 because a black box was used to monitor POST status at the parallel port. Bit 6 was set true (to a 1) to alert the box that the POST was starting.

Code	Meaning
40	CPU flags and register test failed (fatal)
41	BIOS ROM checksum test failed (fatal)
42	Disable pdma controller command and test 8253 timer channel 1, mode 2, refresh counter (fatal); display sub-error code of 1 if interval is below window, 2 if above, and 3 if timer does not respond.
43	8237 DMA controller test failed (fatal)—master clear the controller, set the mask register, read the control registers, test all 8 read/writeable channel registers. Test registers 0-3 DMA address and count with FFFF then 0000.Set up channel 0 for 64K RAM address refresh. Set up

Code	Meaning
	memory-to-I/O transfer, unmask the RAM refresh, and let refresh begin for the first time. Set up the 8253 for proper refresh count. Test for unexpected DMA request (suberror 3), and init DMA channel 1 (not used), 2 (floppy), 3 (display), and init nibble latches. Check for proper DMA transfer into lowest 64K bank of RAM (suberror 4 if parity error).
44	8259 PIC test failed (halt)—initialize stack to lower 64K RAM area just tested, init and disable 8259A, set up interrupt vectors in RAM, set up software then hardware diagnostic interrupt vectors, test software interrupts, then hardware interrupts. Disable interrupts via 8259 mask register, check for hot interrupts, convert hot mask to IRQ number, save any error code, install interrupt vectors, initialize video, and display any error messages (H:#, where # is the hot IRQ#).
45	Install real interrupt vectors, determine system configuration from switches, and initialize video mono and color. Set video mode 3, clear the screen, and display any passing error messages for CPU, ROM, DMA, or interrupt controller. Size and clear RAM at every 64K bank past the lowest 64K, displaying the tested RAM as test progresses. Display any error in form cc:y000:zzz:wwww:rrrr, where cc is the config number, y the failing segment, z the offset, w the written data and r the read data. Test the MM58174 clock calendar, and display message if fails Test 8253 real time clock count capability, and tone generator. Display any error, and halt if failure.
48	Send beep to display and initialize all basic hardware. Init 8041 keyboard controller, determine parallel port configurations and test their registers, determine serial 8250 and Z8530 configurations, check for game card, set up interrupt controller, set all 4 Z8530 serial controllers to 9600 baud, no parity, 1 stop and 8 data. Set up interrupt vectors, initialize RAM variables, clear the screen, initialize the hard disk controller, test for and initialize option ROMs, verify ROM checksums okay, initialize floppy disk controller, allow user to select alternate Z8000 processor if installed and perform INT 19 cold boot.

EISA 2.01

Port 278, 378, Or 3BC (i.e. printer ports)

Code	Meaning
01	Test CPU flags, registers. Initialize interrupt controller
02	Test memory refresh
03	Test CMOS RTC periodic interrupt
04	Test gate A20 line
05	Test mapping memory SRAM
06	Test first 128K RAM. Stack has now been established
07	Test for console presence and initialize
08	Verify system BIOS ROM checksum
09	Test 8042 keyboard controller Normal burn-in/manufacturing mode established
0A	Test timer ratio
0B	Test CMOS RAM battery
0C	Verify CMOS RAM checksum
0D	Test for unexpected NMI
0E	Test interrupt controller #1
0F	Test interrupt controller #2

Code	Meaning
10	Test timer 1 counter 0
11	Test system control port B
12	Test system control port A
13	Verify checksum of NVRAM configuration memory
14	Initialize system board
15	Initialize adapter
16	Initialize ESC SCSI adapter
17	Initialize system video
18	Test and copy shadow RAM. Video is initialized—display banner and non-fatal errors
19	Test DMA page registers
1A	Test DMA address registers
1B	Test DMA count registers
1C	Test DMA mask registers
1D	Test DMA stop registers. Initialize DMA controllers
1E	Test IDTR and GDTR
1F	Test CMOS shutdown byte
20	Test real/protected mode
21	Check system memory configuration
22	Size memory
23	Test 640K base memory
24	Verify base memory configuration
25	Test extended memory (above 1 Mb)
26	Verify extended memory configuration
27	Check for contiguous extended memory
28	Test cache memory. Extended BIOS data area created and POST errors logged
29	Test protected mode instructions
2A	Test CMOS RAM
2B	Test real time clock
2C	Check calendar values
2D	Test keyboard/AUX device fuse
2E	Test keyboard
2F	Initialize keyboard typematic rate and delay
30	Test auxiliary device
31	Test 80x87 math coprocessor
32	Test and initialize Weitek math coprocessor
33	Run 1860 CPU basic and advanced diagnostics
34	Test and configure serial ports
35	Test and configure parallel ports
36	Detect game port
37	Test and initialize hard drives
38	Test and initialize floppy drives
39	Scan for and pass control to adapter ROMs
3A	INT 19 boot—load operating system

PS/2 Compatible

Code	Meaning
01	Processor test
02	Shutdown
03	Interrupt controller initialization
04	Refresh test
05	CMOS periodic interrupt test
06	Timer ratio
07	Test first 64k RAM
08	Test the KBC (8742)
09	NMI test
0A	8254 test
0B	Port 94h test
0C	Port 103h test
0D	Port 102h test
0E	Port 96h test
0F	Port 107h test
10	Blank the screen
11	KB/Aux device fuse check
12	CMOS battery test
13	CMOS RAM checksum test
14	Extended CMOS checksum 0-8K
15	System board and adapter initialization
16	RAM test and initialization
17	Protected mode register test
18	CMOS RAM shutdown byte test
19	80286 protected mode test
1A	Video option ROM scan
1B	EPROM checksum test
1C	Interrupt controller #1 test
1D	Interrupt controller #2 test
1E	Interrupt vector initialization
1F	CMOS RAM test
20	Extended CMOS r/w test
21	CMOS clock test
22	Clock calendar test
23	Dummy checkpoint
24	Watchdog timer test
25	Test RAM from 64K to 640K
26	Configure memory 640K
27	Text expansion memory
28	Initialize extended BIOS data segment and log POST errors
29	Configure memory above 1 Mb
2A	Dummy checkpoint
2B	Test RAM parity
2C	Test DMA page registers
2D	Test DMA controller base/current address registers
2E	Test DMA transfer count register
2F	Initialize DMA controller
30	Test PIO 61
31	Test keyboard

104

Code	Meaning
32	Initialize keyboard typematic rate and delay
33	Test AUX device
34	Test advanced protected mode
35	Configure parallel ports
36	Configure 8250 serial ports
37	Configure coprocessor
38	Configure game card
39	Configure and initialize hard disk
3A	Floppy disk configuration
3B	Initialize ROM drivers
3C	Display total memory and hard drives
3D	Final initialization, Checkpoints complete
3E	Detect and initialize parallel ports
3F	Initialize hard drive and controller
40	Detect and initialize math coprocessor
41	Reserved
42	Initiate adapter ROM scan
CC	Unexpected processor exception occurred
DD	Save DDNIL status
EE	NMI handler shutdown
FF	INT 19 boot

Packard Bell

See *Phoenix*.

Philips/Magnavox/Headstart

Philips, Magnavox, and HeadStart use motherboards designed by Philips Home Electronics in Montreal. Most use a Philips-designed BIOS, although at least one of their portables uses one from Award Software. The beep pattern consists of a series of long and short beeps that correspond to the binary representation of the POST code where leading zeroes are omitted; a zero means a short and a one means a long beep. The various Philips platforms do not all execute the same POST tests.

Philips Platform Cross Reference

Platfom	CPU	System Model/Name
Avenger	80286	Magnavox MaxStation 286, Magnum GL; Headstart Series 300
P3212	80286	Magnavox MaxStation 480, Headstart System 380
P 3239	80286 80386SX	Magnavox Headstart/Maxstation/Magnum/Professional 1200, 48CD, 1600, 64CD, P160, SR16CD
P 3349	80386SX-20	Magnavox Headstart/Maxstation/Magnum/Professional

Platfom	CPU	System Model/Name
		SX20, 80CD
P3345	80386SX	Magnavox Maxstation 386SX, Magnum SX; Headstart Series 500
P33711	80386DX	Headstart/Maxstation/Magnum/Professional 3300

Code	Beeps 0=sh 1=lg	Meanings (Port 80)
0A	1010	DMA page register write/read bad
10	1 0000	CMOS RAM read/write error (only after hard reset)
11	1 0001	System ROM BIOS checksum error
12	1 0010	Timer A error
13	1 0011	DMA controller A error
14	1 0100	DMA controller B error
15	1 0101	Memory refresh error
16	1 0110	Keyboard controller error
17	1 0111	Keyboard controller error
19	1 1001	Keyboard controller error
1C	1 1100	Base 64K RAM error
1D	1 1101	Base 64K RAM parity error
1F	1 1111	Orvonton LSI sync missing
21	10 0001	PVAM register error
25	10 0101	System options error
2B	10 1011	Video sync error (incorrect switch setting or CMOS RAM—run SETUP)
2C	10 1100	Video BIOS ROM error
2D	10 1101	Monochrome/color configuration error
2E	10 1110	No video memory
35	11 0101	Interrupt controller error
36	11 0110	Byte swapper error
37	11 0111	NMI error
38	11 1000	Timer interrupt
39	11 1001	LSI timer halted
3A	11 1010	Main memory test error
3B	11 1011	Keyboard error
3C	11 1100	Keyboard interrupt error (only after hard reset)
3D	11 1101	DDNIL scan halted, cache disabled
40	100 0000	Diskette error
48	100 1000	Adapter card error
4c	100 1100	CMOS battery/checksum error (run SETUP)
4D	100 1101	System options error (run Setup)
52	101 0010	Keyboard controller error
6A	110 1010	Failure shadowing BIOS ROM
70	111 0000	Memory size configuration error (run SETUP)

Phoenix

Created the first clone of IBM's BIOS. POST Codes and beeps used. On 4.3 and above, the system will attempt to generate a beep code consisting of four groups of beeps, with one to four beeps per group. The micro channel version sends codes to port 680, with an execution sequence of: 01, 03, 41, 02, 42, 05, 06, 08, 04, 09—22, 23, 25, 27, 28, 29, 2E, 2B, 2C, 2D, 30, 31, 32, 61, 62, 34, 35, 3A, 38, 3B.

Architecture	Typical Computer	POST Port
ISA	XT	60
	AT	80
	PS/2 25/30	90
EISA	Intel chipset	80
MCA	PS/2 50 up	68O

POST Procedures

Procedure	Meaning
CPU	Check internal operations e.g. ALE/IRQ status; Request; ALU and Memory Read/Write.
CMOS RAM	Test with walking-bit pattern.
ROM BIOS	Perform checksum on ROM BIOS where all bits are added and compared to a factory-set total.
PIT	Check to ensure interrupt requests are properly executed.
DMA	Check DMA from CPU to memory without BIOS. Also check page registers.
Base 64K	Check first 64K block.
Serial and Parallel	I/O data areas for any devices found are assigned; they are not tested.
PIC	Check that proper interrupt request levels are addressed.
Keyboard Controller	Check 8240 for proper operation, including scan code response and Gate A20 which allows CPU operation in protected mode.
CMOS	Check data within CMOS and compare to BIOS information. Failure of the extended area is often due to wrong data setup. Constant failure after resetting CMOS is either battery CMOS chip or RTC.
Video Controller	Test and initialize controller and ROM on the video adapter.
RTC	Check to ensure proper frequencies are on proper lines for the Video Color CPU and DMA Frequency. Check RTC/PIT or system crystal.
CPU	Return From Protected Mode. CPU is put into protected mode and returns to the POST at the point indicated by the CMOS ROM data area byte 0F. Failure here is normally due to the CPU/keyboard controller/CMOS chip or an address line.
PIC	Test Counter 2.
NMI	Check the Non-Maskable Interrupt request vector for active status. Failure is normally due to the CMOS but could also be the BIOS IRQ or CPU chips.
Keyboard	Check for NumLock/Caps and Shift Keys.
Mouse	Initialize through the keyboard controller; this is only done

Procedure	Meaning
	if a mouse is present and it is initialized in this way.
RAM above 64K	Test in 64K blocks with a walking-bit pattern and parity enabled.
Fixed/Floppy Controllers	Test for proper response to BIOS calls.
Shadow RAM Areas	Look in CMOS for settings on which adapter or system ROMs are to be shadowed.
Option ROM	Look for ROM signatures of 55AA in extended memory then initialize the ROM and halt testing while internal checks are carried out.
External Cache	Check controller chip for external cache.
CPU Internal Cache	
Hardware Adapters	Initialize and test video/floppy/hard I/O adapters/serial and parallel.
Cassette	Test internal or external cassette drives.
Boot Code Errors	Errors occurring after this point are normally a corrupt boot record.

2.52 BNP XT

Code	Meaning
01	Test 8253 timer
02	First 64K RAM failed
03	First 1K parity check failed
04	Initialize 8259 interrupt controller
05	Second 1K RAM test (BIOS data area) failed

BIOS Plus or v1.0 POST/Beep Codes

Only for BIOS PLUS or A286/A386/A486 Version 1.xx on an AT-class (80286 or higher) systems. Codes in the 50h range or beyond are chipset or custom platform specific, and will vary from system to system.

Code	Beeps	Meaning
01	none	CPU register test in progress.
02	1-1-3	CMOS write/read failure.
03	1-1-4	ROM BIOS Checksum Failure.
04	1-2-1	Programmable interval timer failure.
05	1-2-2	DMA Initialization failure.
06	1-2-3	DMA page register write/read failure.
08	1-3-1	RAM refresh verification failure.
09	none	1st 64K RAM test in progress.
0A	1-3-3	1st 64K RAM chip or data line failure multi-bit.
0B	1-3-4	1st RAM odd/even logic failure.
0C	1-4-1	Address line failure 1st 64K RAM.
0D	1-4-2	Parity failure 1st 64K RAM.
10	2-1-1	Bit 0 1st 64K RAM failure.
11	2-1-2	Bit 1 1st 64K RAM failure.
12	2-1-3	Bit 2 1st 64K RAM failure.

Code	Beeps	Meaning
13	2-1-4	Bit 3 1st 64K RAM failure.
14	2-2-1	Bit 4 1st 64K RAM failure.
15	2-2-2	Bit 5 1st 64K RAM failure.
16	2-2-3	Bit 6 1st 64K RAM failure.
17	2-2-4	Bit 7 1st 64K RAM failure.
18	2-3-1	Bit 8 1st 64K RAM failure.
19	2-3-2	Bit 9 1st 64K RAM failure.
1A	2-3-3	Bit A(10) 1st 64K RAM failure.
1B	2-3-2	Bit B(11) 1st 64K RAM failure.
1C	2-4-2	Bit C(12) 1st 64K RAM failure.
1D	2-4-2	Bit D(13) 1st 64K RAM failure.
1E	2-4-3	Bit E(14) 1st 64K RAM failure.
1F	2-4-4	Bit F(15) 1st 64K RAM failure.
20	3-1-1	Slave DMA register failure.
21	3-1-2	Master DMA register failure.
22	3-1-3	Master interrupt mask register failure.
23	3-1-4	Slave interrupt mask register failure.
25	none	Interrupt vector loading in progress.
27	3-2-4	8042 keyboard controller test failure.
28	none	CMOS power failure/checksum calculation in progress.
29	none	CMOS configuration validation in progress.
2B	3-3-4	Screen memory test failure.
2C	3-4-1	Screen initialization failure.
2D	3-4-2	Screen retrace test failure.
2E	none	Search for video ROM in progress.
30	none	Screen believed running with video ROM.
31	none	Mono monitor believed operable.
32	none	Color monitor (40 col) believed operable.
33	none	Color monitor (80 col) believed operable.
34	4-2-1	Timer tick interrupt test in progress or failed (non-fatal).
35	4-2-2	Shutdown failure (non-fatal).
36	4-2-3	Gate A20 failure (non-fatal).
37	4-2-4	Unexpected interrupt in protected mode (non-fatal).
38	4-3-1	Mem high address line fail at 01000-0A000 (non-fatal).
39	4-3-2	Mem high addr line fail at 100000-FFFFFF (non-fatal).
3A	4-3-3	Timer chip counter 2 failed (non-fatal).
3B	4-3-4	Time-of-day clock stopped
3C	4-4-1	Serial port test
3D	4-4-2	Parallel port test
3E	4-4-3	Maths coprocessor test
41	low 1-1-2	System board select bad
42	low 1-1-3	Extended CMOS RAM bad

UMC Chipset PCI

Code	Meaning
02	Verify Real Mode
04	Get CPU type
06	Initialize system hardware
08	Initialize chipset registers with initial POST values
09	Set in POST flag
0A	Initialize CPU registers
0C	Initialize cache to initial POST values
0E	Initialize I/O
10	Initialize power management
11	load alternate registers with initial POST values
12	Jump to User Patch 0
14	Initialize keyboard controller
16	BIOS ROM checksum
18	8254 timer initialization
1A	8237 DMA controller initialization
1C	Reset PIC
20	Test DRAM refresh
22	Test 8742 keyboard controller
24	Set ES segment register to 4 Gb
26	Enable Address Line A20
28	Autosize DRAM
2A	Clear 512K base RAM
2C	Test 512K base address lines
2E	Test 512K base memory
30	Test base address memory
32	Test CPU bus clock frequency
34	Test CMOS RAM
35	Test chipset register initialize
36	Test check resume
37	Reinitialize the chipset
38	Shadow System BIOS ROM
39	Reinitialize the cache
3A	Autosize the cache
3C	Configure advanced chipset registers
3D	Load alternate registers with CMOS values
3E	Read hardware configuration from keyboard controller
40	Set initial CPU speed
42	Initialize interrupt vectors
44	Initialize BIOS interrupts
46	Check ROM copyright notice
47	Initialize manager for PCI option ROMs
48	Check video configuration against CMOS
49	Initialize PCI bus and devices
4A	Initialize all video adapters
4C	Shadow video BIOS ROM
4E	Display copyright notice
50	Display CPU type and speed
52	Test keyboard
54	Set key click if enabled

Code	Meaning
56	Enable keyboard
58	Test for unexpected interrupts
5A	Display prompt "Press F2 to Enter Setup"
5C	Test RAM between 512 and 640K
5E	Test base memory
60	Test expanded memory
62	Test extended memory address lines
64	Jump to User Patch 1
66	Configure advanced cache registers
68	Enable external and CPU caches
69	Set up power management
6A	Display external cache size
6C	Display shadow message
6E	Display non-disposable segments
70	Display error messages
72	Check for configuration errors
74	Test RTC
76	Check for keyboard errors
7A	Enable keylock
7C	Set up hardware interrupt vectors
7E	Test coprocessor if present
80	Disable onboard I/O ports
82	Detect and install external RS232 ports
84	Detect and install external parallel ports
86	Reinitialize onboard I/O ports
88	Initialize BIOS data area
8A	Initialize extended BIOS data area
8C	Initialize floppy controller
8E	Hard disk autotype configuration
90	Initialize hard disk controller
91	Initialize local bus hard disk controller
92	Jump to User Patch 2
94	Disable A20 address line
96	Clear huge ES segment register
98	Search for option ROMs
9A	Shadow option ROMs
9C	Set up Power Management
9E	Enable hardware interrupts
A0	Set time of day
A2	Check key lock
A4	Initialize typematic rate
A8	Erase F2 prompt
AA	Scan for F2 key stroke
AC	Enter Setup
AE	Clear in-POST flag
B0	Check for errors
B2	POST done
B4	One beep
B6	Check password (optional)
B8	Clear global descriptor table
BC	Clear parity checkers

Code	Meaning
BE	Clear screen (optional)
BF	Check virus and backup reminders
C0	Try to boot with INT 19
D0	Interrupt handler error
D2	Unknown interrupt error
D4	Pending interrupt error
D6	Initialize option ROM error
D8	Shutdown error
DA	Extended Block Move
DC	Shutdown 10 error

These are for boot block in Flash ROM:

Code	Meaning
Flash BIOS Integrity Test	
E2	Initialize the chipset
E3	Check for Forced Flash
E5	Check HW status of ROM
E6	BIOS ROM is OK
E7	Do a complete RAM test
Flash Recovery	
E8	Do OEM initialization
E9	Initialize interrupt controller
EA	Read in the bootstrap code
EB	Initialize all vectors
EC	Boot the flash program
ED	Initialize the boot device
EE	Boot code was read OK.

PCI

Code	Meaning
02	If the CPU is in protected mode turn on A20 and pulse the reset line; forcing a shutdown 0.
04	On a cold boot save the CPU type information value in the CMOS.
06	Reset DMA controllers. Disable videos. Clear pending interrupts from RTC. Setup port B register.
08	Initialize chipset control registers to power on defaults.
0A	Set a bit in the CMOS that indicates POST; used to determine if the current configuration causes the BIOS to hang. If so default values will be used on next POST.
0C	Initialize I/O module control registers.
0E	External CPU caches are initialized. Cache registers are set to default.
10/12/14	Verify response of 8742.
16	Verify BIOS ROM checksums to zero.
18	Initialize all three of 8254 timers.
1A	Initialize DMA command register. Initialize 8 DMA channels.
1C	Initialize 8259 interrupt controller to :ICW4 needed; Cascade

Code	Meaning
	and edge-triggered mode.
20	Test DRAM refresh by polling refresh bit in PORTB.
22	Test 8742 keyboard controller. Send self test command to 8742 and await results. Also read the switch inputs from the 8742 and write the keyboard controller command byte.
24	Set ES segment register to 4 Gb
26	Enable Address Line A20
28	Autosize DRAM
2A	Clear first 64K of RAM
2C	Test RAM address lines
2E	Test first 64K bank of memory consisting of a chip address line test and a RAM test.
30/32	Find true MHz value
34	Clear CMOS diagnostic byte (register E). Check RTC and verify battery has not lost power. Checksum the CMOS and verify it has not been corrupted.
36/38/3A	External cache is autosized and its configuration saved for enabling later in POST.
3C	Configure advanced cache features. Configure external cache's configurable parameters.
3E	Read hardware configuration from keyboard controller
40	Set system power-on speed to the rate determined by the CMOS. If the CMOS is invalid use a conservative speed.
42	Initialize interrupt vectors 0-77h to the BIOS general interrupt handler.
44	Initialize interrupt vectors 0-20h to proper values from the BIOS interrupt table.
46	Check copyright message checksum.
48	Check video configuration.
4A	Initialize both monochrome and color graphics video adapters.
4C/4E	Display Copyright message.
50	Display CPU type and speed
52	Test for the self-test code if a cold start. When powered the keyboard performs a self-test and sends an AA if successful.
54	Initialize keystroke clicker during POST.
56	Enable keyboard
58	Test for unexpected interrupts. First do an STI for hot interrupts; secondly test NMI for unexpected interrupt. Thirdly enable parity checkers and read from memory checking for unexpected interrupt.
5A	Display prompt "Press F2 to Enter Setup"
5C	Determine and test the amount of memory available. Save the total memory size in the BIOS variable called bdaMemorySize.
5E	Perform address test on base memory. The following address lines are tested based on the memory size.
60	Determine and test the amount of extended memory available. Save the total extended memory size in the CMOS at CMOSExtended.
62	Perform an address line test on A0 to the amount of memory available. This test is dependent on the processor since the test will vary depending on the width of memory (16 or 32 bits). This test will also use A20 as the skew address to prevent corruption of the system memory.

Code	Meaning
68	External and CPU caches if present are enabled. Non-cacheable regions are configured if necessary.
6A	Display cache size on screen if non-zero.
6C	Display BIOS shadow status.
6E	Display the starting offset of the non-disposable section of the BIOS.
70	Check flags in CMOS and in the BIOS data area to see if any errors have been detected during POST. If so, display error messages on the screen.
72	Check status bits for configuration errors. If so display error messages on the screen.
74	Test RTC if the battery has not lost power. If the RTC is not running or the battery has lost powerset the incorrect time bit in register E of the CMOS.
76	Check status bits for keyboard errors. If so display error messages on the screen.
78	Check for stuck keys on the keyboard. If so display error messages on the screen.
7A	Enable keylock
7C	Set up hardware interrupt vectors
7E	Test coprocessor if present
80-82	Detect and install RS232 ports
84	Detect and install parallel ports
86-88	Initialize timeouts/key buffer/soft reset flag.
8A	Initialize extended BIOS data area and initialize the mouse.
8C	Initialize both floppy disks and display an error message if failure was detected. Both drives are checked so the appropriate diskette types are established in the BIOS data area.
8E	Hard disk autotype configuration
90	If the CMOS RAM is valid and intact and fixed disks are defined call the fixed disk init routine to initialize the fixed disk system and take over the appropriate interrupt vectors.
92-94	Disable A20 address line
96-98-	Scan for ROM BIOS extensions.
9E	Enable hardware interrupts
A0	Set time of day
A2	Set up NumLock indicator. Display a message if key switch is locked.
A4	Initialize typematic rate.
A6	Initialize hard disk autoparking.
A8	Erase F2 prompt.
AA	Scan for F2 key strokes.
AC	Check to see if SETUP should be executed.
AE	Clear ConfigFailedBit and InPostBit in CMOS.
B0	Check for POST errors
B2	Set/clear status bits to reflect POST complete.
B4	One beep.
B6	Check for password before boot.
B8	Clear global descriptor table (GDT).
BA	Initialize the screen saver.
BC	Clear parity error latch.

Code	Meaning
BE	Clear screen.
C0	Try to boot with INT 19
D0-D2	If an interrupt occurs before interrupt vectors have been initialized this interrupt handler will try to see if the interrupt caused was an 8259 interrupt and which one. If the interrupt is unknown, InterruptFlag will be FF. Otherwise it will contain the IRQ number that occurred
D4	Clear pending timer and keyboard interrupts, and transfer control to the double word address located at RomCheck.
D6-D8-DA	Return from extended block move.

Phoenix v3.07

See Quadtel.

ISA/EISA/MCA BIOS POST/Beep Codes (fatal)

Msg	Beeps	Meaning
01	none	CPU register test in progress.
02	1-1-3	CMOS write/read failure.
03	1-1-4	ROM BIOS Checksum Failure.
04	1-2-1	Programmable interval timer failure.
05	1-2-2	DMA Initialization failure.
06	1-2-3	DMA page register write/read failure.
08	1-3-1	RAM refresh verification failure.
09	none	1st 64K RAM test in progress.
0A	1-3-3	1st 64K RAM chip or data line failure multi-bit.
0B	1-3-4	1st RAM odd/even logic failure.
0C	1-4-1	Address line failure 1st 64K RAM.
0D	1-4-2	Parity failure 1st 64K RAM.
0E	1-4-3	Fail-safe timer failure.
0F	1-4-4	Software NMI port failure.
10	2-1-1	Bit 0 1st 64K RAM failure.
11	2-1-2	Bit 1 1st 64K RAM failure.
12	2-1-3	Bit 2 1st 64K RAM failure.
13	2-1-4	Bit 3 1st 64K RAM failure.
14	2-2-1	Bit 4 1st 64K RAM failure.
15	2-2-2	Bit 5 1st 64K RAM failure.
16	2-2-3	Bit 6 1st 64K RAM failure.
17	2-2-4	Bit 7 1st 64K RAM failure.
18	2-3-1	Bit 8 1st 64K RAM failure.
19	2-3-2	Bit 9 1st 64K RAM failure.
1A	2-3-3	Bit A 1st 64K RAM failure.
1B	2-3-2	Bit B 1st 64K RAM failure.
1C	2-4-2	Bit C 1st 64K RAM failure.
1D	2-4-2	Bit D 1st 64K RAM failure.
1E	2-4-3	Bit E 1st 64K RAM failure.
1F	2-4-4	Bit F 1st 64K RAM failure.
20	3-1-1	Slave DMA register failure.
21	3-1-2	Master DMA register failure.

Msg	Beeps	Meaning
22	3-1-3	Master interrupt mask register failure.
23	3-1-4	Slave interrupt mask register failure.
25	none	Interrupt vector loading in progress.
27	3-2-4	Keyboard controller test failure.
28	none	CMOS pwr failure; checksum calculation in progress.
29	none	CMOS RAM configuration validation in progress.
2B	3-3-4	Screen memory test failure.
2C	3-4-1	Screen initialization failure.
2D	3-4-2	Screen retrace test failure.
2E	none	Search for video ROM in progress.
30	none	Screen believed running with video ROM.
31	none	Mono monitor believed operable.
32	none	Color monitor (40 col) believed operable.
33	none	Color monitor (80 col) believed operable.

ISA/EISA/MCA BIOS POST/Beep Codes (non-fatal)

Non-fatal if manufacturing jumper is on.

Msg	Beeps	Meaning
34	4-2-1	No time tick.
35	4-2-2	Shutdown test in progress or failure.
36	4-2-3	Gate A20 failure.
37	4-2-4	Unexpected interrupt in protected mode.
38	4-3-1	Memory high address line failure at 01000-0A000. Also RAM test in progress or address failure >FFFH.
39	4-3-2	Memory high address line failure at 100000-FFFFFF.
3A	4-3-3	Interval Timer channel 2 test or failure.
3B	4-3-4	Time-of-day clock test or failure.
3C	4-4-1	Serial port test or failure.
3D	4-4-2	Parallel port test or failure.
3E	4-4-3	Maths coprocessor test
3F		Cache test (Dell)
41	low 1-1-2	System board select bad (Micro Channel only)
42	low 1-1-3	Extended CMOS RAM bad (Micro Channel only)

Phoenix v4.0

Beeps	Code	Meaning
1-1-1-3	02	Verify Real Mode
1-1-2-1	04	Get CPU type
1-1-2-3	06	Initialize system hardware
1-1-3-1	08	Initialize chipset registers with initial POST values
1-1-3-2	09	Set in POST flag
1-1-3-3	0A	Initialize CPU registers
1-1-4-1	0C	Initialize cache to initial POST values
1-1-4-3	0E	Initialize I/O
1-2-1-1	10	Initialize Power Management
1-2-1-2	11	Load alternate registers with initial POST

Beeps	Code	Meaning
		values
1-2-1-3	12	Jump to UserPatch0
1-2-2-1	14	Initialize keyboard controller
1-2-2-3	16	BIOS ROM checksum
1-2-3-1	18	8254 timer initialization
1-2-3-3	1A	8237 DMA controller initialization
1-2-4-1	1C	Reset Programmable Interrupt Controller
1-3-1-1	20	Test DRAM refresh
1-3-1-3	22	Test 8742 Keyboard Controller
1-3-2-1	24	Set ES segment to register to 4 GB
1-3-3-1	28	Autosize DRAM
1-3-3-3	2A	Clear 512K base RAM
1-3-4-1	2C	Test 512 base address lines
1-3-4-3	2E	Test 512K base memory
1-4-1-3	32	Test CPU bus-clock frequency
1-4-2-4	37	Reinitialize the chipset
1-4-3-1	38	Shadow system BIOS ROM
1-4-3-2	39	Reinitialize the cache
1-4-3-3	3A	Autosize cache
1-4-4-1	3C	Configure advanced chipset registers
1-4-4-2	3D	Load alternate registers with CMOS values
2-1-1-1	40	Set Initial CPU speed
2-1-1-3	42	Initialize interrupt vectors
2-1-2-1	44	Initialize BIOS interrrupts
2-1-2-3	46	Check ROM copyright notice
2-1-2-4	47	Initialize manager for PCI Options ROMs
2-1-3-1	48	Check video configuration against CMOS
2-1-3-2	49	Initialize PCI bus and devices
2-1-3-3	4A	Initialize all video adapters in system
2-1-4-1	4C	Shadow video BIOS ROM
2-1-4-3	4E	Display copyright notice
2-2-1-1	50	Display CPU type and speed
2-2-1-3	52	Test keyboard
2-2-2-1	54	Set key click if enabled
2-2-2-3	56	Enable keyboard
2-2-3-1	58	Test for unexpected interrupts
2-2-3-3	5A	Display prompt "Press F2 to enter SETUP"
2-2-4-1	5C	Test RAM between 512 and 640k
2-3-1-1	60	Test expanded memory
2-3-1-3	62	Test extended memory address lines
2-3-2-1	64	Jump to UserPatch1
2-3-2-3	66	Configure advanced cache registers
2-3-3-1	68	Enable external and CPU caches
2-3-3-3	6A	Display external cache size
2-3-4-1	6C	Display shadow message
2-3-4-3	6E	Display non-disposable segments
2-4-1-1	70	Display error messages
2-4-1-3	72	Check for configuration errors
2-4-2-1	74	Test real-time clock
2-4-2-3	76	Check for keyboard errors
2-4-4-1	7C	Set up hardware interrupts vectors

Beeps	Code	Meaning
2-4-4-3	7E	Test coprocessor if present
3-1-1-1	80	Disable onboard I/O ports
3-1-1-3	82	Detect and install external RS232 ports
3-1-2-1	84	Detect and install external parallel ports
3-1-2-3	86	Re-initialize onboard I/O ports
3-1-3-1	88	Initialize BIOS Data Area
3-1-3-3	8A	Initialize Extended BIOS Data Area
3-1-4-1	8C	Initialize floppy controller
3-2-1-1	90	Initialize hard-disk controller
3-2-1-2	91	Initialize local-bus hard-disk controller
3-2-1-3	92	Jump to UserPatch2
3-2-2-1	94	Disable A20 address line
3-2-2-3	96	Clear huge ES segment
3-2-3-1	98	Search for option ROMs
3-2-3-3	9A	Shadow option ROMs
3-2-4-1	9C	Set up Power Management
3-2-4-3	9E	Enable hardware interrupts
3-3-1-1	A0	Set time of day
3-3-1-3	A2	Check key lock
3-3-3-1	A8	Erase F2 prompt
3-3-3-3	AA	Scan for F2 key stroke
3-3-4-1	AC	Enter SETUP
3-3-4-3	AE	Clear in-POST flag
3-4-1-1	B0	Check for errors
3-4-1-3	B2	POST done--prepare to boot operating system
3-4-2-1	B4	One beep
3-4-2-3	B6	Check password (optional)
3-4-3-1	B8	Clear global descriptor table
3-4-4-1	BC	Clear parity checkers
3-4-4-3	BE	Clear screen (optional)
3-4-4-4	BF	Check virus and backup reminders
4-1-1-1	C0	Try to boot with INT 19
4-2-1-1	D0	Interrupt handler error
4-2-1-3	D2	Unknown interrupt error
4-2-2-1	D4	Pending interrupt error
4-2-2-3	D6	Initialize option ROM error
4-2-3-1	D8	Shutdown error
4-2-3-3	DA	Extended Block Move
4-2-4-1	DC	Shutdown 10 error
Flash BIOS Integrity Test		
4-3-1-3	E2	Initialize the chipset
4-3-1-4	E3	Initialize refresh counter
4-3-2-1	E4	Check for Forced Flash
4-3-2-2	E5	Check HW status of ROM
4-3-2-3	E6	BIOS ROM is OK
4-3-2-4	E7	Do a complete RAM test
Flash recovery		
4-3-3-1	E8	Do OEM initialization
4-3-3-2	E9	Initialize interrupt controller
4-3-3-3	EA	Read in bootstrap code

Beeps	Code	Meaning
4-3-3-4	EB	Initialize all vectors
4-3-4-1	EC	Boot the Flash program
4-3-4-2	ED	Initialize the boot device
4-3-4-3	EE	Boot code was read OK

Quadtel

v3.07 AT BIOS (Phoenix 3.07)

Code	Meaning
02	Flag test
04	Register test
06	System hardware initialization
08	Initialize chipset registers
0A	BIOS ROM checksum
0C	DMA page register test
0E	8254 timer test
10	8254 timer initialization
12	8237 DMA controller test
14	8237 DMA initialization
16	Initialize 8259/reset coprocessor
18	8259 interrupt controller test
1A	Memory refresh test
1C	Base 64K address test
1E	Base 64K memory test
20	Base 64K test (upper 16 bits) for 386 systems
22	8742 keyboard self test
24	MC 146818 CMOS test
26	Start first protected mode test
28	Memory sizing test
2A	Autosize memory chips
2C	Chip interleave enable test
2E	First protected mode test exit
30	Unexpected shutdown
31	DDNIL bit scan failure
32	System board memory size
34	Relocate shadow RAM if configured
36	Configure EMS system
38	Configure wait states
3A	Retest 64K base RAM
3C	CPU speed calculation
3E	Get switches from 8042
40	Configure CPU speed
42	Initialize interrupt vectors
44	Verify video configuration
46	Initialize video system
48	Test unexpected interrupts
4A	Start second protected mode test
4C	Verify LDT instruction
4E	Verify TR instruction

Code	Meaning
50	Verify LSL instruction
52	Verify LAR instruction
54	Verify VERR instruction
56	Unexpected exception
58	Address line 20 test
5A	Keyboard ready test
5C	Determine AT or XT keyboard
5E	Start third protected mode test
60	Base memory test
62	Base memory address test
64	Shadow memory test
66	Extended memory test
68	Extended address test
6A	Determine memory size
6C	Display error messages
6E	Copy BIOS to shadow memory
70	8254 clock test
72	MC 146818 RTC test
74	Keyboard stuck key test
76	Initialize hardware interrupt vectors
78	Maths coprocessor test
7A	Determine COM ports available
7C	Determine LPT ports available
7E	Initialize BIOS data area
80	Determine floppy/fixed disk controller
82	Floppy disk test
84	Fixed disk test
86	External ROM scan
88	System key lock test
8A	Wait for <F1> key pressed
8C	Final system initialization
8E	Interrupt 19 boot loader
B0	Unexpected interrupt before or after boot up.

16K XT

Code	Meaning
03	Test flag register
06	Test CPU Register
09	Initialize system hardware
0C	Test BIOS ROM checksum
0F	Initialize 8237 DMA page register
12	Test 8237 address and count registers
15	Initialize 8237 DMA
18	Test 8253 timer
1B	Initialize 8253 timer
1E	Start memory refresh test
21	Test base 64K RAM, Cycling POST display shows

Code	Meaning
	POST code, the upper then lower bytes of the failing address, separated by delays
24	Set up common INT temp stack
27	Initialize 8259 interrupt controller
2A	Test interrupt mask register
2D	Test for hot (unexpected) interrupt
30	Test V40 DMA if present
31	Test for DDNIL bits present
33	Verify system clock interrupt
36	Test keyboard
39	Set up interrupt table
3C	Read system configuration switches
3F	Test video
42	Determine COM ports available
45	Determine LPT ports available
48	Determine if game port available
4B	Display copyright message
4E	Calculate CPU speed
54	Test system memory
55	Test floppy drive
57	Initialize system before boot
5A	Call Interrupt 19 boot loader

SuperSoft

PC/XT/AT

	XT	AT
11	CPU register or logic error	CPU register or logic
12	ROM POST checksum error	ROMPOST A checksum error
13	8253 timer channel 0 error	ROMPOST B checksum error
14	8253 timer channel 1 error	8254 timer channel 0 error
15	8253 timer channel 2 error	8254 timer channel 1 error
16	8237A DMA controller error	8254 timer channel 2 error
17	8255 parity error detected	8237A DMA controller 1 err
18	16K critical RAM region error	8237A DMA controller 2 err
19	Memory refresh error	DMA page registers error
1A	-	8042 parity error detected
21	8259 Interrupt controller error	16K critical RAM region
22	Unexpected interrupt detected	Memory refresh error
23	Interrupt 0 (timer) error	CPU protected mode error
24	Nonmaskable interrupt error	8259 Interrupt controller 1 err
25	MDA video memory error	8259 Interrupt controller 2 err
26	CGA video memory error	Unexpected interrupt detected

	XT	AT
27	EGA/VGA memory error	Interrupt 0 (timer) error
28	8087 math chip error	CMOS real time clock error
29	Keyboard controller error	Nonmaskable interrupt error
2A	-	8Ox87 math chip error
31	Keyboard scan lines/stuck key	Keyboard controller error
32	Floppy controller error	Stuck key or CMOS RAM err
33	Floppy disk read error	Floppy controller error
34	Memory error at address x	Floppy disk read error
35	Slow refresh, address x	MDA video memory error
36, 37	-	CGA, EGA/VGA RAM error
38	-	BIOS checksum error
41	BIOS checksum error	Memory error at address x
42	BASIC ROM 1 checksum	Slow refresh, address x
43-45	BASIC ROM 2, 3, 4	Display pass count
59	No monitor	No monitor

Tandon

Slimline 286, 386SX and 486; 486 EISA

Type A AT 29 Feb 1988

Code	Meaning
01	Test 80286 CPU flags and registers
02	Test BIOS ROM checksum
03	Test MC146818 CMOS RAM battery (RTC)
04	Test 8254 timer
05	8254 timer test failed
06	Initialize RAM refresh
07	Test first 16K RAM
08	Initialize cold boot interrupt vectors
09	Test 8259 interrupt controller and interrupt vectors
0A	Fill in temporary interrupt vectors
0B	Initialize interrupt vector table 1
0C	Initialize interrupt vector table 2
0D	Initialize fixed disk vector
0E	Interrupt vector test failed
0F	Clear keyboard controller input buffer
10	Keyboard controller input buffer clearing failed
11	Run keyboard controller self-test
12	Initialize equipment check data area
13	Determine presence of and install 80287 math coprocessor
14	Test MC146818 CMOS RAM disk value range
15	Test for and install parallel port
16	Test for and install serial port
17	Invoke INT 19 to boot operating system

Type B AT—1992

Code	Meaning
01	Cold boot started
06	Initialize chipset if any
07	Warm boot entry. About to start 8042 keyboard controller self-test
08	Part of cold boot keyboard initialization passed
09	Keyboard self-test finished. Test ROM BIOS checksum.
0A	Test CMOS RAM battery level
0B	Save CMOS RAM battery condition in CMOS diagnostic/status register
0C	Finished saving CMOS RAM battery condition
0D	Test 8254 PIT. Disable RAM parity, I/O parity, DMA controllers, and speaker; enable timer channel 2.
0E, AA, xx	8245 test failed. xx is the failing channel number.
0F	Initialize 8254 timer channels (0 to mode 3 for 55 ms square wave, 1 to mode 2 as rate generator for refresh) and conduct memory refresh test.
10	Refresh test failed
11	Test base 64K RAM and fill with zeros
12	64K RAM test failed. 3 long beeps and halt.
13	RAM test passed
14	Set up stack, disable mappers for systems that support EMS drivers (for warm boot), initialize battery beep flag parameters for notebook, perform read/write test of CMOS RAM, enable error message if failed.
15	CMOS RAM read/write test complete
16	Calculating CPU speed; may set to low if CMOS RAM failed
18	Test and initialize both 8259 interrupt controllers
1A	8259 initialization complete
1B	Install interrupt handler and vector for INT 0F to check for unexpected (spurious) interrupts. Halt if spurious interrupt occurs.
1C	Spurious interrupt did not occur (test pass). Test 8254 timer channel 0, IRQ0, and software INT8 tests.
1D	Error. Timer 0 interrupt did not occur when expected. Halt system.
1E	Both 8259 interrupt controllers passed the tests
20	Set up interrupt vectors 02-1F
21	Set up interrupt vectors 70-77
22	Clear interrupt vectors for 41 and 46 (disk parameter pointers).
23	Read 8042 self-test result, DMA page reg ch 2 (port 81).
24	Test for proper 8042 self-test result (55).
25	Error: Keyboard controller self-test failed, display message and halt.
26	Keyboard controller self-test passed
27	Confirm DMA working; prepare DMA channel 2 for floppy data transfer
28	Reinitialize video (cold boot)
29	Reinitialize video with cursor off (warm boot)
2A	Video parameters are initialized

Code	Meaning
2B	Enable NMI and I/O channel check, disable 8254 timer channel 2 and speaker
2C	Run RAM test to determine size of RAM
2D	RAM sizing complete
2E	Send reset command to keyboard controller to initiate a keyboard scan cycle
2F	Keyboard has been initialized. Initialize the CMOS RTC
30	CMOS RTC has been initialized. Initialize on-board floppy if any
31	Install the hard disk controller
32	Disk controller has been installed; prepare DMA channel 2 for floppy transfers
33	Perform equipment check and initialize numeric data processor (math chip)
34	Install the serial/parallel ports
35	Test CMOS RAM battery level
36	Check for keypress—Esc=Setup, Spacebar=menu; do speed beeps 2=high, l=low
37	Enable 8254 timer channel 0 for system tick, enable keyboard and slave interrupt controller 8259 #2
38	Timer tick, keyboard and 8259 #2 have been enabled; enable/disable cache per CMOS RAM
39	Enable keyboard interface and interrupts. Go to built-in Setup program as necessary; shadow ROMs as appropriate.
3A	Setup finished, so clear the screen and display Please Wait message
3B	Test the fixed and floppy drives
3C	Scan for and invoke the adapter ROMs in C800-E000
3D	Turn off Gate A20; restore vectors 3bh-3fh with temporary interrupt service routines.
3E	Gate A20 is turned off
3F	Invoke INT19 to boot operating system.

These accompanied by 5 long beeps:

Code	Meaning
BF	486-based, 386SX/20c or 386SX/25c processor module boards are used in a system where the WD76C10 chipset is not revision F or above.
CF	CPU on a 486-based processor module has failed its internal self-test.
DF	386SX/20c or 386SX/25c processor module board failed correctly to initialize its on-board cache (bad cache RAM. illegal configuration, etc., or unknown module ID).
EF	Extended CMOS RAM within the WD76C10 chipset failed its self-test

486 EISA—10 Oct 1989

Code	Meaning
	Power on or system reset: enable 8042, RTC; disable 82C601 chip serial, parallel, floppy, hard drive, NMI; check 8042 status.

Code	Meaning
AA, 01, xx	Show 80486 BIST (built-in self-test) result: xx=00 if OK, FF if not.
01	Disable cache, enable ROM, high speed on, turn off caches, disable EISA NMIs, set master and slave IRQs to edge-triggered, disable reset chaining. disable 82C601 chip but set it valid.
05	Initialize address decoder, 640K RAM; set BIOS as cacheable, enable extended memory.
06	Clear Shutdown Flag.
07	8042 and keyboard test: wait till 8042 buffer empty, disable 8042 command, read 8042 output buffer, set response OK to DMA page reg channel 2.
08	Send 8042 NOP command, self-test command; get 8042 self-test result, send to DMA page reg channel 2.
AA, 01, xx	Show 8042 self-test result: xx=55 if OK
09	Test BIOS ROM checksum; 3 short beeps and halt if bad
0A	Read CMOS registers 3 times to clear pending CMOS RTC interrupts, and disable RTC interrupts. Check battery.
0B	Bad CMOS RAM battery.
0C	Send command to port 61 to disable parity and speaker, enable timer; disable DMA.
0D	Test 8254 counter timer: set all 3 counters to mode 3 (square wave), start them and read the counts.
0E	A counter timer is bad (at least one is 0 and not counting).
AA, 01, xx	Show the failing counter address (xx = 40, 41, or 42), then beep long-short-long-short and halt.
0F	Enable and check memory refresh (set timer 1 to mode 2 for 15 microsecond refresh, and turn on DMA to perform it); delay 1 millisecond and check bit 4 of port 61 for 0-to-1 toggle.
10	Memory refresh failed (no toggle); beep short-long-short, and halt.
11	Check and clear the first 64K of RAM in real mode: disable NMI, clear parity latches, fill 64K with 5555 and check it, then AAAA and check it, then 0000.
AA, 06, mmnn, oopp, qqrr	First 64K memory test failed. mmnn=location lsb, msb; oopp= value read lsb, msb; qqrr=value expected lsb, msb.
AA, 01, xx	Test port 61 for parity error (bits 7, 6=1) and display error xx=value read from port 61 if parity error occurred.
12	First 64K memory test failed. Clear parity latches, give 3 long beeps, and halt.
13	First 64K memory test passed.
14	Reset the warm boot flag (40:72) and test CMOS RAM. Turn off caches, shadow the BIOS, set speed high, calculate high speed and initialize GP flag, set speed low and turn off cache if CMOS not good or CMOS speed not high, otherwise turn on cache and set speed high.
16	Check Shutdown Flag 123x.
17	Reset was cold boot. Set 40:e9 bit 7 (disk_status).
18	Prepare 8259 interrupt controllers; send FF to mask register and check it.
19	Interrupt controller initialization failed; initialize video, display the error message, and halt.

Code	Meaning
1A	Test interrupt controller: set all 256 ints to slipped interrupt vector. If warm boot (40:e9 bit 7), skip to POST 1E.
1B	Set int 0F to spurious interrupt vector, check for spurious interrupts.
1C	Set int 08 (timer 0) to timer 0 int vector, enable timer and int, wait for int from timer.
1D	Timer interrupt did not occur. Initialize video, display error message and halt.
1E	Initialize interrupt vectors.
1F	Initialize interrupt vectors 00-6F to temporary interrupt service routine.
20	Set vectors for interrupt 02-1F.
21	Set interrupt vectors for 70-77, clear vectors 60-67 and 78-FF.
22	Clear interrupt vectors for 41 and 46 (disk parameter pointers).
23	Read 8042 self-test result from DMA page reg ch 2 (port 81).
24	Test for proper 8042 self-test result (55).
25	8042 self-test failed. Get keyboard controller status, initialize video, display error message, and halt.
26	Initialize 8042 keyboard controller, transfer 128K mem. exp. bit from 8042 to CMOS RAM (IBM compatible, but not used), read state of security switch and initialize RAM variable.
27	Check Shutdown Flag = 123x. No= cold boot.
28	If cold boot or CMOS RAM is bad, install video ROM and establish video, initialize equipment flags according to primary video adapter and CMOS RAM content, initialize POST status, initialize video.
29	If not cold boot and CMOS RAM is OK, install Video ROM and establish video for mono/CGA, initialize equipment flags according to primary video adapter and CMOS RAM contents, initialize video warm boot, initialize video.
2A	Check for bad CMOS RAM and queue the message if so; command port 61 to clear parity latches, disable the speaker and disable timer channel 2; enable NMI.
2B	Check Shutdown Flag = 123x. if warm boot, use memory sizes from CMOS RAM.
2C	If cold boot, turn caches off, test memory for appropriate size, and restore cache status.
2D	Turn off "POST Fail" CMOS RAM bit and display any queued error messages; initialize keyboard RAM (40:17-30) + (40:E0-E7).
2E	Initialize 8042 keyboard controller and test keyboard.
2F	Initialize time of day in the real time clock chip.
30	Test for and install floppy controller.
31	Enable C&T 82C601 chip IDE interface, test for and install hard drive.
32	Test 8259 DMA registers with 55 then AA, and initialize them to 0 (ports D2 and D4).
33	Test for and initialize math coprocessor chip
34	Test for and initialize parallel and serial ports, on and off board.
35	Initialize RAM variables for bad CMOS time, date, checksum,

Code	Meaning
	and battery condition.
36	Wait for user to press Esc, space. Check the keyboard lock, clear the keyboard lock override, beep to indicate speed, display any queued messages. Esc=setup, space=boot menu.
37	Enable system clock tick (IRQ0), keyboard (IRQ1), and slave interrupt controller (IRQ2)
38	Initialize RAM variables for Ctrl-Alt-Esc, Ctrl-Alt-Ins
39	Enter setup if user pressed Ctrl-Alt-Esc. If EISA, revert to ISA if tab key pressed.
3A	Clear screen and update equipment flags according to CMOS RAM contents (may have changed during setup). Shadow any ROMs per setup. Enable/disable cache per CMOS RAM.
3B	Initialize floppy and fixed disk drives.
3C	Set POST Fail bit in CMOS RAM, then scan for and invoke adapter option ROMs.
3D	Clear the Shutdown Flag to 0, turn off gate A20 to enable memory wrap in real mode.
3E	Set vectors for interrupts 3B-3F, clear Post Fail bit in CMOS RAM, home the cursor, display any error messages, clear MSW of 32-bit registers (ISC Unix).
3F	Invoke INT 19 to boot operating system.

Tandy

Uses OEM version of Phoenix BIOS.

Wyse

Uses OEM version of Phoenix BIOS.

Zenith

LEDs on system board to indicate the status of various stages of boot-up. All will light up first of all, then go out in sequence when the test concerned is completed. Zenith computers may also use an AMI (Plus, normally) or a Phoenix BIOS.

Post Procedures

Procedure	Meaning
CPU	Perform a read/write test on the internal register. Check for defective CPU or clock generator.
ROM BIOS	Check the CRC value stored in ROM against the computed value of this test. Check the BIOS or I/O circuitry.
RAM	Check first 64K of memory to see that data can be stored in

Procedure	Meaning
	it so the BIOS can use it later.
DMA	Test the register functions of the DMA chips.
PIT/PIC	Perform tests on the main support chips and enable the appropriate interrupts when completed. Check also for AC ripple.
RTC/CMOS	Check the validity of the CMOS RAM and compare value in CMOS with appropriate devices. The BIOS will use the values from the CMOS to set up appropriate IRQ routines for disk and other I/O access. Check for defective CMOS/battery/adapter or CMOS setting.
Video Display	Attempts will be made to initialize video to a mono screen very early on so error messages can be displayed. This test is for initializing upper video modes available with EGA/VGA.
Test/Boot to Diskette	Check the floppy subsystem and prepare the drive for boot if there is a bootable floppy in the A: drive.
Boot to Fixed Disk	Initialize any fixed disks in the CMOS and give control to the first one if a bootable floppy has not been detected previously. Check for corrupt boot code if not a hardware error.

POST Codes

Code	Meaning
01	VGA check
02	MDA initialize
03	Initialize video
05	Set hard reset
07	Check ROM at E000
08	Check ROM shadow at F000
09	Remap video to E000
0B	Keyboard controller test
0C	CMOS/8042 test
0D	DMA test
0E	DMA page register
0F	Test 64K memory
10	Test base memory
11	Second VGA unit
12	Mono initialization
13	RTC/CMOS test
15	CPU register test
16	CPU add test
17	RTC/8042 test
18	Enter protected mode
19	Testing memory
1A	Testing extended memory
1B	Leaving protected mode
1C	Testing system board
1D	Testing system board
1E	Testing system board
1F	Bus sizing
20	Set BIOS data area

Code	Meaning
21	Testing DMA
22	Checking C800 for ROM
24	Testing base memory
25	8042 test
26	8042 test
27	8042 test
28	Memory parity test
29	PIT test
2A	Testing floppy disk
2B	Testing FDC/drives
2C	Testing HDC/drives
2D	Checking CMOS settings
2E	Soft configuration
30	Checking adapter ROM
31	Checking CMOS settings
32	Enabling interrupts
33	Soft configuration
34	Soft configuration
35	Jump to boot code
00	Boot to OS

Orion 4.1E—1992

Checkpoints 00h-1Fh and F0h-FFh are displayed after the indicated function is completed.

Code	Meaning
02	Cold Boot, Enter Protected Mode
03	Do Machine Specific Initialization
F0	Start of Basic HW Initialization for Boot
F1	Clear CMOS Pre-Slush Status Location
F2	Starting CLIO Initialization
F3	Initialize SYSCFG Register
F4	DXPI Initialization for Boot Block
F5	Turning OFF Cache
F6	Configure CPU Socket Pins
F7	Checking for 387SX
F8	82C206 DEFAULT Initialization
F9	Superior Default Initialization
FF	End of Machine-specific Boot Block
04	Check Flash Checksum
05	Flash OK, jump into Flash (FFFD Flash Code
06	Reset or Power-Up
07	CLIO Default init command
08	SYSCFG REG initialized
09	CMOS Pre-slush error words initialization
10	SCP initialized
11	DRAM autosizing complete
12	Parity check enabled. Enable Memory Parity (EMP) LED turned off
13	Start of slushware test
14	Slushware at 000F0000h OK

Code	Meaning
15	BIOS ROM copied to slushware
16	Back in Real Mode
17	ROM BIOS Slushing is finished. CPU LED Turned off
18	Video ROM (C0000 Slushware Test
19	Internal Video ROM Slushed
1A	Back in Real Mode
1B	Internal video hardware enabled.
1C	CPU clock frequency determined
1E	BIOS RAM cleared

20-EF are displayed before the indicated function has been attempted. 20-2A indicate restart after system shutdown, usually to return to real mode from protected mode. The CMOS RAM shutdown byte (0F) will contain a value indicating the reason for the shutdown.

Code	Meaning
20	RESET (CMOS 0)
21	Continue after Setting Memory Size (CMOS 0F=1)
22	Continue after Memory Test (CMOS 0F=2)
23	Continue after Memory Error (CMOS 0F=3)
24	Continue with Boot Loader Request (CMOS 0F=4)
25	Jump to execute User Code (flush) (CMOS 0F=5)
26	Continue after Protected Mode Test Passed (CMOS 0F=6)
27	Continue after Protected Mode Test Failed (CMOS 0F=7)
28	Continue after Extended Protected Mode Test (CMOS 0F=8)
29	Continue after Block Move (CMOS 0F=9)
2A	Jump to execute User Code (CMOS 0F=A)
2B	Reserved
2C	Reserved
2D	Reserved
2E	Reserved
2F	Reserved
30	Exit from Protected Mode
31	TEST-RESET passed (80386). Warm Boot
32	Check the ROM Checksum. ROM LED Turned Off
33	Clear the Video Screen On
34	Check System DRAM Config Update CMOS-TOTAL-MEM-SIZE Value
35	Pro-load CMOS if CMOS is
36	Turn Off the UMB RAM
37	Turn Parity Generation
38	Initialize System Variable
39	Check for errors in POWER
3A	Initialize SCP MODE
3B	Test CMOS Diag. Power Reset
3C	Test CPU Reset 80386 & Determine State Number
3D	Save CPU ID & Processor-T
3E	Init the Video & Timers
3F	Init DMA Ports, Clear Page
40	Set Speed too Fast for Now

Code	Meaning
41	Test EEPROM Checksum
42	Enable/Disable Superior's Parallel, FDC & HDC Per CMOS
43	Slush External Video BIOS if on CMOS
44	Turn Cache off for Memory
45	Test Extended RAM (1-16Mb)
46	Test BASE RAM (0-64 OK). RAM LED turned off by Base RAM Test
47	Determine Amount of System
48	Set WARM-BOOT Flag if RES Indicates Cold Boot
49	Clear 16K of Base RAM
4A	Install BIOS Interrupt Vector
4B	Test System Timer. INT LED turned off if CLOCK Test passes
4C	(Re)Initialize Interrupt
4D	Enable Default Hardware Initialization
4E	Determine Global I/O Configuration
4F	Initialize Video
50	Init WD90C30 Scratchpad
51	Check for Errors before Boot
52	Reserved
53	Test (Ext Only) and Initialize
54	Reserved
55	Initialize the Keyboard Processor
56	Initialize the PS/2 Mouse
57	Configure CLIO for Mouse
58	Configure CLIO for LAN
59	Configure CLIO for SCSI
5A	Configure CLIO for WAM
5B	Wait for User to Enter Code
5C	Init System Clock TOD, Enable
5D	Test, Init Floppy Drive Sensor. Disk LED Turned off
5E	Check for Z150 Style Disk
5F	Init Winchester Subsystem
60	Set Default I/O Device Parameters
61	Get LAN ID Info from LAN
62	*Install ROMs at 0C8000h
63	*Install ROMs at 0E000h
64	Initialize SCSI Interface
65	Run with A2O off in PC Mode
66	Really turn off the SCP
67	Set Machine Speed using CMOS
68	Turn on Cache
69	Calibrate 1ms Constants
6A	*Enable Non-Maskable Interpreter
6B	Reserved
6C	Clear the warm-boot flag
6D	Check for Errors before Boot
6E	Boot

191 BIOS -1992

Code	Meaning

Code	Meaning
0	Start of Slush Test
1	Processor Test
2	CACHE and CLIO
3	ISP Defaults Set
4	Into Protected Mode
5	Memory SIMMs Count
6	Memory Controller

Code	Meaning
7	Preped to Test Block
8	First 1Mb of Ram

Code	Meaning
9	Checksum OEM ROM
10	Low Flash ROM Checks
11	F000 ROM Checks
12	Aurora VIDEO ROM
13	F000 ROM Slushed
14	Sep Initialized
15	Language Slushed
16	Do VIDEO Specific tests
17	Done Slushing
32	Point Interrupt Vectors
33	Turn on Parity Generation
34	Initialize System Variables
35	Init Interrupt Controllers
36	Check Error that Occurred
37	Reinitialize SCP Warm Boot
38	Test CMOS Diag, Power, Reset
39	Reserved, or DDNIL status flag check

Code	Meaning
3A	Test CPU Reset (80386)
3B	Save the CPU ID in GS
3C	Slush Video ROM to C0000
3D	Init the Video and Timers
3E	Init CMA Ports, Clear Page
3F	Set Speed too Fast for now
40	Checksum the Nonvolatile RAM
41	Initialize Configuration
42	Init Expansion Boards from VRAM
43	Turn Cache off for Memory Test
44	Init Memory Ctrlr, test Extd Memory
45	Test Base RAM
46	Determine amount of System RAM
47	Test and Init Cache if installed
48	Test System Timer Tick
49	Initialize the Write queues

Code	Meaning
4A	Initialize Monitor RAM
4B	Clear 16K of Base RAM
4C	Install BIOS Interrupt Vectors
4D	Enable Default Hardware Initialization
4E	Determine Global I/O configuration
4F	Reserved
50	Initialize Video
51	Init WD90C30 Scratchpad register
52	Initialize the keyboard processor
53	Turn off IRQ 12 if mouse is off
54	Wait for user to enter correct password
55	Init System Clock Time of Day
56	Test, Init Floppy System, Track Seeks
57	Init Winchester subsystem, Messages
58	Install ROMs starting at C80000H
59	Install ROM starting at E0000H
5A	Initialize SCSI interface
5B	Set default I/O Device Parameters
5C	Init the cache speed and clock
5D	Always tell System ROM 'Cold
5E	Run with A20 off in PC Mode
5F	Really turn off the SCP
60	Set machine speed using CFG
61	Turn on cache if machine halt
62	Calibrate 1ms constants
63	Enable NMI
64	Test for errors before boot
65	Boot