

32-bit FR Family

- **Wide performance range covered by single architecture**
- **External bus I/F supports 4GB memory space**
- **Up to 4 Mbytes embedded Flash**
- **Highly integrated on-chip peripherals**
- **Ethernet MAC and hardware IPSEC support**

FR Family Roadmap

FR family offers high performance RISC MCUs with 5 stage pipeline and Harvard architecture.

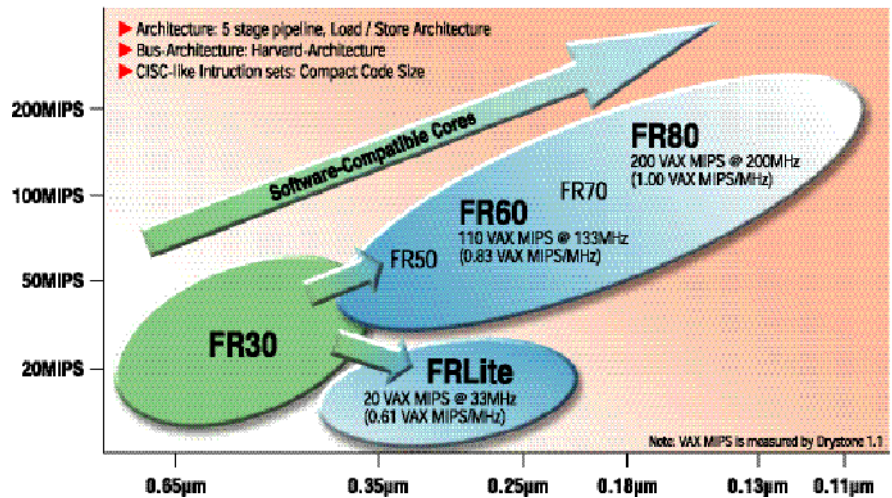
The family offers:

- High-speed, one-cycle instruction execution processing
- High code efficiency with a 16-bit fixed instrument set
- Wide range of highly integrated peripherals
- Single chip, new technology FR60lite
 - Deliver high performance MCU to 16-bit level applications
- New technology for high-end MCU - FR80
 - 256 MIPS CPU
 - Development plan for 400 MIPS performance

Fujitsu's 32-bit RISC FR microcontrollers feature the company's proprietary architecture core, which is dedicated to meeting the twin demands of high performance coupled with low cost, which are needed by today's high-end automotive, consumer and telecom applications.

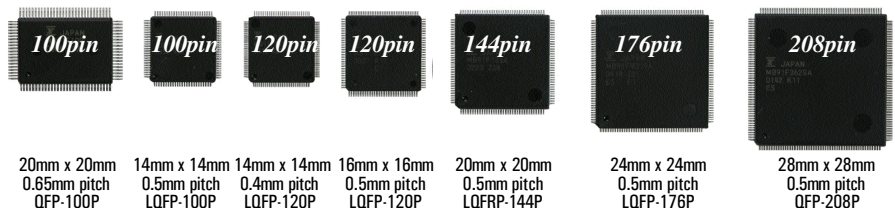
The FR family features a bus architecture that allows the integration of resources available to the Fujitsu F²MC-16 family of 16-bit microcontrollers and uses the 16-bit fixed-length commands required for such integration. Furthermore, added commands address bit operation, peripheral control, direct memory-to-memory transfer, and stack generation/release, to ensure optimum overall operation. As easy to use as any 8-bit or 16-bit microcontroller, the FR family also offers high code efficiency and the high performance of RISC.

FR Family Roadmap



Wide Range of Package Lineup

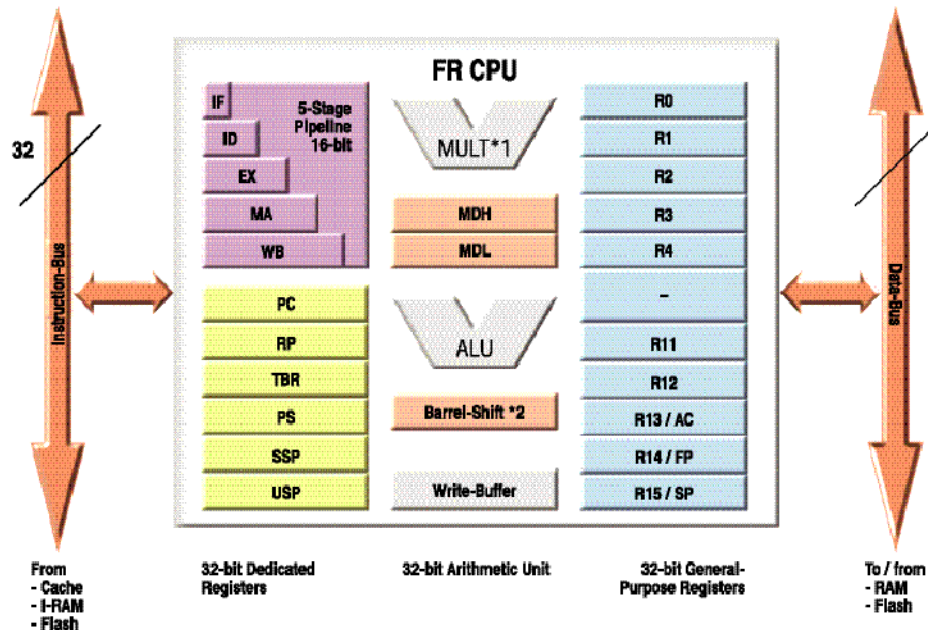
Fujitsu pioneered packaging technology which provides flexible packages ranging from 100 pins to 208 pins.



32-bit FR Family

Designed from the outset to be optimized for embedded applications, the CPU has a 16-bit instruction operation code, enabling maximum performance from low-cost, half-word external memory or else allowing double instruction fetches for each bus cycle. The CPU employs a five-stage pipeline, a 32 x 32 multiplier, a barrel shifter and a bit search unit that finds the first '1', '0' or change in a data word in a single cycle. The instruction set contains bit-manipulation instructions and data-moving instructions, which are very helpful in supporting the on-chip peripheral blocks and embedded application.

FR CPU-CORE Architecture

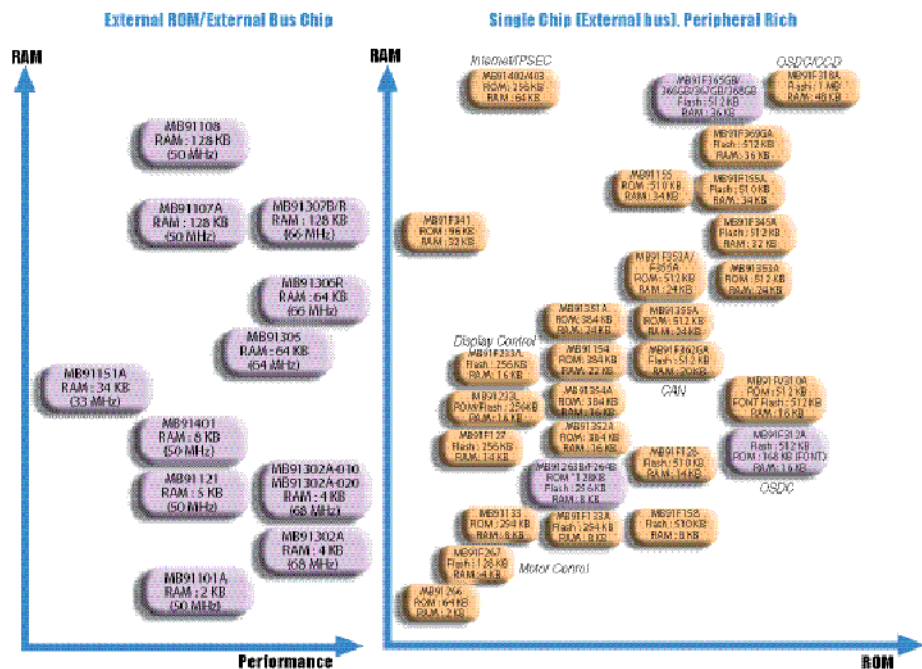


*1:32 bit x 32 bit: 5 clock cycles, 16 bit x 16 bit: 3 clock cycles. *2: 1 cycle. IF: Instruction Fetch ID: Instruction Decode EX: Execution MA: Memory Access WB: Write Back PC: Program Counter RP: Return Pointer TBR: Table Base Register PS: Program Status SSP: System Stack Pointer USP: User Stack Pointer AC: Accumulator FP: Frame Pointer SP: Stack Pointer

FR Family Application Coverage

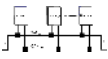





- Automotive:** Body-control networks, dashboards, power-train networks
- White Goods:** Washing machines, dish washers refrigerators
- Consumer:** Digital cameras, handheld electronic products
- Security:** Embedded network solution for banking, government, secure digital storage.

32-bit FR Family Lineup



32-bit FR Family

Peripheral Features

	<ul style="list-style-type: none"> • Up to 6ch of CAN • Up to 128 message buffers • Suitable for low- and high-speed CAN applications make the devices flexible. 	<p>Individually programmable TX and RX buffers, CAN wake-up & multilevel message buffer features</p>
<p>Motor Control</p> 	<ul style="list-style-type: none"> • Single-chip MCU with 6ch SMC • Devices with AC/DC brush-less, sensor-less motor control • High speed 8/10/12-bit ADC up to 24ch simplifies development for motor-control applications. 	<p>Integrated stepper-motor driver I/O enables designer to reduce BOM cost. Integrated multifunction timer for dead time creation</p>
<p>Display Control</p> 	<ul style="list-style-type: none"> • Embedded VFDC & LCDC of up to 896 segments. MCUs with LCDC support up to 152-pixels LCD display. These features make this family attractive for A/V display applications. 	<p>MCUs support large VFD</p>
<p>USB</p> 	<ul style="list-style-type: none"> • Full-speed USB mini-host & Device Function direct communication without a host PC. 	<p>12Mbps USB interface, with simple host features, enables</p>
<p>OSDC/ CCD</p> 	<ul style="list-style-type: none"> • Embedded On-screen display controller and closed-caption decoder 	<p>Suitable for TV applications featuring 1792 different characters and graphics</p>
<p>Ethernet/ IPSEC Engine</p> 	<ul style="list-style-type: none"> • IEEE802.3 10/100M MAC • MAC address filtering • DES/3DES, AES Support • HMAC-MD5 / HMAC-SHA1 • IKE / RSA 	<p>Supports low-cost implementation by embedded devices with IPV6 for virtually unlimited IP address space and network manageability</p>



32-bit FR Family

32-bit FR Family

Series	Pin Count	Vcc Volts	ROM KB	ROM Type	RAM KB	Cache KB	Clock MHz (kHz)	DMA Chns	Ext Bus I/F	Input Capture	Output Compare	ADC 10bit ch	Timer 16bit	PPG 16bit ch	I ² C ch	UART ch	CAN 2.0B	SMC ch	LCDC pixels	Special Features
MB91101	100	3 or 5		ROMless, Ext ROM	2	1	50	8	Yes			4	3			3				DRAM I/F
MB91107	120	3		ROMless, Ext ROM	128	1	50	8	Yes			4	3			3				DRAM I/F
MB91121	120	3		ROMless, Ext ROM	160	1	50	8	Yes			8	3			3				DRAM I/F, DSP
MB91129	100	3	256 to 510	Flash	14		25	8	Yes	4	4	8	3	4		3				Flash
MB91130	144	3 or 5	254	Mask, Flash	8		33 (32)	8	Yes	4	8	8	5	6		5				
MB91150	144	3	384 to 510	Mask, Flash	8 to 34	1	36	8	Yes	4	8	8	4	6	1	4				
MB91230A	120	3	256	Mask, Flash	16		33.6 (32)			2	4	8	4	6		4			128	
MB91245	144	5	256	Mask, Flash	16		32 (32)	5	Yes	4	2	32	3	4		4	2	6	128	C CAN-32 message buffer, LIN, SMC, LCDC motor control
MB91260B	100	5	128 to 256	Mask, Flash	8		33		Yes	4	6	12	3	8		3				
MB91265	100	5	64 to 128	Mask, Flash	2 to 4		33			4	6	11	3	4		2				
MB91270	100	5	256	Flash	10		32	5	Yes	8	8	24	3	8	3	7	1			CAN-32 message buffer, LIN
MB91301	144	3	4	Mask	4	4	68 (2)	5	Yes	3		4	3	4	2	3				SDRAM I/F, RTOS, program loader
MB91305	176	3		ROMless, Ext ROM	64	4	64	5	Yes	3		10	3	4	2	5				Multi communication I/Fs
MB91307	120	1.8 or 3		ROMless, Ext ROM	128	1	66	5	Yes			4	3		1	3				large RAM
MB91310	144	3	512	Mask, Flash	16	1	40 (32)	5		4	4	10	3	4	4	5				OSDC, USB Host, USB function
MB91319	176	3	1024	Mask, Flash	48		40 (2)	5		4	4	10	3	4	4	5				OSDC, CCD, USB function
MB91345B	100	3	512 to 1024	Mask, Flash	32		50 (2)	5	Yes	4	4	16	3	8	11	11				up to 1MB embedded Flash + external memory I/F, multiple communication interfaces
MB91350A	120/176	3	256 to 512	Mask, Flash	16 to 24		50 (2)	5	Yes	4	2 to 8	8 to 12	4	3 to 6		3 to 5				High-performance Flash device with multiple communication interfaces and timers
MB91360G	120/160/208	5	512	Flash	20 to 36		64 (2)	5		4	2	8 to 10	6	4	1	3 to 4	2 to 3	4		CAN, SMC, sound generator, Flash
MB91401	240/144	3	0 to 256	ROMless, Ext ROM, Mask	8 to 72	4	33 to 50	5	Yes				3		1	2				10/100 base T Ethernet MAC, IP-SEC
MB91460	176	5 or 3	0 to 1024	ROMless, Ext ROM, Mask, Flash	64 to 128	4	80	5	Yes	8	8	13 to 32	8	16	3	7 to 16	6	6	40x4	Multiple CAN each with 128 message buffers, LIN-UART with FIFO, up to 6ch SMC, SDRAM, FCRAM I/F option
MB91475/480/485	100/120/144/176	5	128 to 512	Mask, Flash	8 to 40		80/50	5	Yes	4 to 8	6 to 12	12	3	4	3					UART with I2C mode support, 12bit ADC, up to 12ch of waveform generators for inverter motor control

32-bit FR CAN and Stepper Motor Control Device Series

Series	Pin Count	Vcc Volts	ROM KB	ROM Type	RAM KB	Cache KB	Clock MHz (kHz)	DMA Chnls	Ext Bus I/F	Input Capture	Output Compare	ADC 10bit ch	Timer 16bit	PPG 16bit ch	I ² C ch	UART ch	CAN 2.0B	SMC ch	LCDC pixels	Special Features
MB91245	144	5	256	Mask, Flash	16		32 (32)	5	Yes	4	2	32	3	4		4	2	6	128	C CAN-32 message buffer, LIN, SMC, LCDC
MB91270	100	5	256	Flash	10		32	5	Yes	8	8	24	3	8	3	7	1			CAN-32 message buffer, LIN
MB91360G	120/160/208	5	512	Flash	20 to 36		64 (2)	5		4	2	8 to 10	6	4	1	3 to 4	2 to 3	4		CAN, SMC, Sound Generator, Flash
MB91460	176	5 or 3	0 to 1024	ROMless, Ext ROM, Mask, Flash	64 to 128	4	80	5	Yes	8	8	13 to 32	8	16	3	7 to 16	6	6	40x4	Multiple CAN each with 128 message buffers, LIN-UART with FIFO, up to 6ch SMC, SDRAM, FCRAM I/F Option

32-bit FRAC/DC Motor Control Device Series

Series	Pin Count	Vcc Volts	ROM KB	ROM Type	RAM KB	Clock MHz (kHz)	DMA Channels	Ext Bus I/F	Input Capture	Output Compare	ADC 10bit and 12bit	Timer 16bit	PPG 16bit ch	I ² C ch	UART ch	AC/DC Motor	Special Features
MB91260B	100	5	128 to 256	Mask, Flash	8	33		Yes	4	6	12	3	8		3	Yes	Inverter Motor Control
MB91265	100	5	64 to 128	Mask, Flash	2 to 4	33			4	6	11	3	4		2	Yes	Inverter Motor Control
MB91475/480/485	100/120/144/176	5	128 to 512	Mask, Flash	8 to 40	80/50	5	Yes	4 to 8	6 to 12	12 and 4	3	4	3	3 to 6	Yes	UART with I2C mode support, 12bit ADC, up to 12ch of Waveform Generators for Multiple Inverter Motor Control

32-bit FR Ethernet Device Series

Part	Pin Count	Vcc Volts	ROM KB	ROM Type	RAM KB	Cache KB	Clock MHz	DMA Chnls	Ext Bus I/F	EXT IRQ	I ² C	Timer 16bit	UART ch	LAN/LAN FIFO	Security	Special Features
MB91401	240	Dual-Int. 1.8V, I/O 3.3V	NA	ROMless, Ext ROM, Mask	Data RAM-8B	4	50	5	32/16/8-bit Async	3-ch+NMI	1-ch(100Kbps)	3	2	10/100 x1ch, TX 1.5KB, Rx 9.2KB	DES, 3DES, IP sec Manager	Authentication: MD5, SHA-1, HMAC, 8 GPIO, CF Card I/F, USB 2.0 FS
MB91402	144	Single 3.3V	256	ROMless, Ext ROM, Mask	RAM-64KB, Data RAM-8KB	4	33	5	16/8-bit Async, SDRAM, FCRAM I/F	2-ch+4-ch(GPIO pin)	1-ch(400Kbps)	3	2	10/100 x1ch, TX 1.5KB, Rx 3KB	NA	26 GPIO, Slave Bus I/F
MB91403	144	Single 3.3V	256	ROMless, Ext ROM, Mask	RAM-64KB, Data RAM-8KB	4	33	5	16/8-bit Async, SDRAM, FCRAM I/F	2-ch+4-ch(GPIO pin)	1-ch(400Kbps)	3	2	10/100 x1ch, TX 1.5KB, Rx 3KB	DES, 3DES, AES, (128/192/256bit) ECB/CBC	Authentication: MD5, SHA-1, HMAC, 26 GPIO, Slave Bus I/F

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