Development of a Custom Microprocessor for Automotive Control

Richard C. Breitzman

ABSTRACT: This paper describes the development of a high-performance microprocessor-based system for control of automotive emissions and fuel economy. The result is a two-chip system consisting of a VLSI single-chip 16-bit microprocessor with an integral analog-to-digital (A/D) converter and precision timing circuits, and a companion memory chip with a combination of read only memory (ROM) and random access memory (RAM).

Introduction

Requirements for minimum automotive emissions and maximum fuel economy create the need for a high-speed, accurate control system that can operate under harsh environmental conditions. Because of large production volumes (millions of vehicles per year) and long product life, customized microprocessor technology can be developed to meet this need using very large scale integrated (VLSI) circuit techniques. This paper outlines the joint Ford/Intel development of a VLSI single-chip microprocessor with its companion memory chip currently being used in the production of automobiles and light trucks.

The planning for this customized microprocessor for electronic engine control (named EEC-IV) began in 1978. Ford was already in production with a microprocessor-based interactive spark timing and exhaust gas recirculation (EGR) control system. For 1979, the addition of feedback controlled carburetion was developed and ready for production. Electronic fuel injection with EEC-III was well along its development for the 1980 model year introduction.

The two main motivations for the development of EEC-IV were: (1) the anticipated federal and California emission control legislation ultimately requiring all automobile manufacturers to meet a 0.4 g/mi oxides of nitrogen for vehicles undergoing the Federal Cold/Hot Metro emission test cycle, and (2) the improvements in fuel economy associated with tighter control limits for engine parameters.

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Ford engineers decided quite early in the design phase that EEC-IV was to provide a significant alternative to the already designed, mass-produced (or ready-to-be introduced) microprocessor-based control units, and that, specifically, it must have superior functional capabilities in several key areas: input/output type and capacity, memory size and computational/program execution speed. This allows an increased design life and the opportunity to take advantage of memory density improvements and reduced costs that continue to typify the semiconductor industry.

A global objective was set, according to which EEC-IV was required to (1) sense all critical engine operating parameters, (2) calculate all required engineering command values, and (3) output the required real-time commands for spark timing, exhaust gas recirculation valve positioning and for sequentially firing fuel injectors on or off, in a total time of 2.5 ms or less. This performance target meant that the total engine control cycle would be accomplished in a four-cylinder engine in 90 degrees of crankshaft rotation at an engine speed of 6000 r/min, as shown in Fig. 1.

Since for a four-cylinder engine, the crankshaft position reference signal occurs every 180 degrees of crankshaft rotation — during which time critical engine commands. like spark timing, have to be calculated once — an equal amount of sense-calculate-actuate time would be allowed for nonengine related control features: to be used for transmission, vehicle speed, idle speed, and similar control tasks in the future. Of course, the ability to handle the memory size normally associated with such a collection of tasks was also well planned for. This objective was evaluated by a benchmark engine control test program: a V-8 interactive spark timing, exhaust gas recirculation, and sequentially firing manifold fuel injection control program, which executed in a shorter-than-targeted time using a breadboard design model.

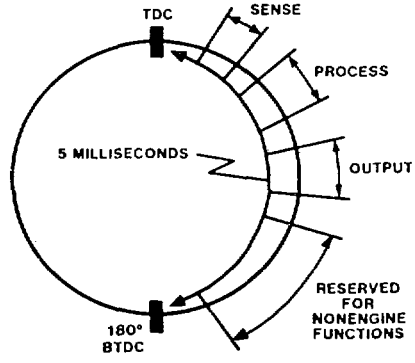

Fig. 1. Pictorial representation of computer time usage between critical engine events.

With the anticipated federal and California 0.4 g/mi oxides of nitrogen legislation remaining an uncertainty, Ford began to focus on how to use the new powers of EEC-IV optimally. It was decided that although EEC-IV has the power to handle complex interactive engine and transmission control strategies, utilization of its power will be phased in gradually, refining current control philosophies first, then expanding it to new strategy applications.

Engine Control Requirements

Automotive engine emission and fuel economy requirements necessitate control of a wide range of factors with varying degrees of accuracy. These items include air-fuel ratio, spark timing, and exhaust gas recirculation, which must all be accurately controlled to provide the best fuel economy for most operation conditions. Spark timing must be accurately controlled to meet engine emission constraints under various speed and torque outputs. Under transient driving conditions, the control strategy for spark becomes even more complex. It would be extremely difficult to accomplish these complex algorithms with a mechanical ignition system, and virtually impossible to provide the adaptive response of electronic controls. Electronic modules, however, are only part of the engine control system. Several sensors are used to measure characteristics of temperature, pressure, air flow, throttle position, crankshaft position, and knock. Actuators to control air, fuel, exhaust gas recirculation complete the control system [1].

Fuel control, either feedback carburetor or fuel injection, provides the means for maintaining the air-fuel ratio at stoichiometry for maximum catalyst efficiency. The wide dynamic range of air intake and the potential for rapid and frequent changes in this variable

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make high speed and high accuracy a necessary part of the control computer. An 8-bit structure is insufficient to handle these accuracies without using double precision algorithms where response speed is penalized. The EEC-IV computer is based on a 16-bit architecture with the flexibility to handle multiple data lengths. Higher computer arithmetic resolution also provides for simplification of software generation since most variable data do not require scaling to avoid round-off errors.

Ignition timing is also critical to engine performance by allowing the greatest spark advance without engine knock. The ability of a control system to accurately measure engine RPM and predict the next cylinder firing prior to top dead center is dependent on its ability to accurately measure time with regard to crankshaft position. The EEC-IV computer has been designed to resolve timed events to the nearest 2.4 μs. This translates to less than 0.1 degree of crankshaft rotation for a V-8 at 6000 r/min. While the mechanical parts of measuring engine speed cannot achieve this accuracy (at least with today's technology), the computer introduces truly negligible error in the ignition timing system. Adjustment of the percentage of EGR in the intake mixture is necessary for maintaining the temperature of combustion and thereby controlling the NO_x emission.

As control loops become more complex through better engine characterization and as additional features are added into the control task, the system speed and the number of input and output channels become more important. The ability to establish priorities among the various tasks and the ability to program output events accurately in real time through a self-sorting output stack of EEC-IV allows events to occur at their optimum time, based on the current engine environment.

High-speed operation optimizes the ability of the control system to detect and respond to changes in the engine operating conditions, thereby maximizing vehicle performance. As previously stated, the EEC-IV control system can monitor key sensors, complete execution of the associated control algorithms, and update output events as required, for each cylinder firing under most engine speeds. This provides the system with the ability to match, as closely as possible, the myriad of dynamic changes within the engine and its environment.

As many of the engine parameters are analog in nature (e.g., temperatures, pressures, or positions), a key element is the ability to convert the analog signals to digital format. The EEC-IV has integrated an analog-to-digital (A/D) converter with the microprocessor chip to monitor these parameters cost-effectively.

Custom Versus Standard LSI Approaches

The control microprocessor can be provided by assembling several standard, off-the-shelf integrated circuits for a particular application. The approach of using standard ICs provides flexibility by adding or taking away circuits to match the application but requires several devices for even minimal applications. Standard microprocessors also include support of features, such as BCD number systems, which are not required for control applications.

The custom design approach offers benefits in minimum chip count, minimum board/module size, and increased reliability. System speed can also be optimized in the custom approach by minimizing the bus structures and drive requirements between circuits to limit capacitance loading. Custom design offers the opportunity to tailor the device to the application without carrying unnecessary capability as overhead.

The EEC-IV approach has been a joint Ford/Intel custom VLSI development of a two-chip system where all the computing and I/O have been integrated into the 8061 microprocessor with the application software instructions contained in the companion 8361 memory circuit. Flexibility is provided by two-package options for the microprocessor to match the number of inputs/outputs (I/O) needed for various engine applications. In the 68 lead version, 41 pins are dedicated to I/O. A 40 lead version provides 18 pins for I/O.

Microprocessor Configuration

Figure 2 shows the microprocessor block diagram. Except for instruction memory, the complete microprocessor resides on a single die. A central processing unit (CPU), RAM register file, analog/digital converter, I/O controller, interrupt controller, watchdog timer, digital output ports, and clock generator are all integrated on the 8061. Instruction memory and additional read/write data memory in the form of a 128 × 8 RAM is on the 8361. A 15 MHz quartz crystal furnishes the time base for the 8061 clock generator. The 15 MHz oscillator is divided by three to generate the internal 5 MHz clock signals.

The following I/O is available on the two-package options:

	40 Pin	68 Pin
High-speed timed digital inputs	3	8
High-speed timed digital outputs	5	10
Low-speed digital outputs	2	8
Analog inputs	6	13
Bidirectional I/O	2	2

Eight high-speed timed digital inputs can detect input transitions with a time resolution of +/− 1.2 μs. Similarly, the ten high-speed timed digital outputs can generate output transitions to the same +/− 1.2 μs resolution.

One byte of low-speed digital output is provided. Also, a 2-bit bidirectional port can be used as either input or output. The 8061 can accept as many as 13 analog inputs. An analog multiplexer selects which input channel is converted.

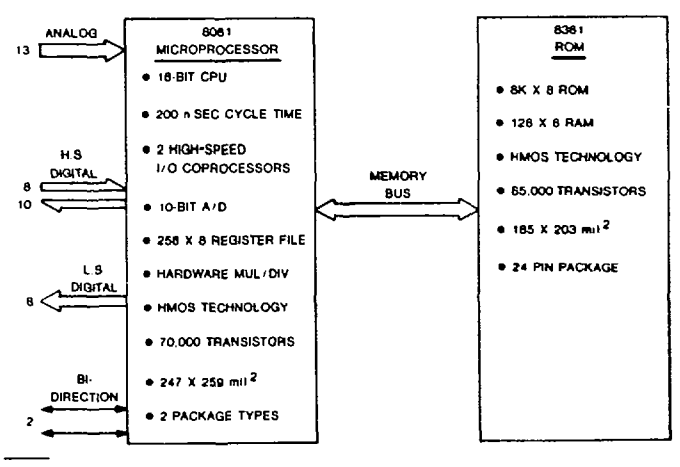

Fig. 2. EEC-IV microcomputer block diagram.

An 11-line (8 data, 3 control) custom memory bus (M Bus) provides the interface between the CPU and external memory; 8361 chip select inputs are internally generated and also programmable such that each 8361 ROM pattern can be programmed to reside in any one of the 8K segments of the 64K memory space. Additional memory mapped I/O could also be added via the M Bus.

Figure 3 shows a photograph of the 8061 with the major blocks identified. Die size is 247 mils (6.27 mm) by 259 mils (6.58 mm). A key point of the layout is the register and arithmetic/logic unit (RALU). This is the unit whose size is most directly affected by the decision to design a 16-bit or 8-bit machine. Implementing an 8-bit machine would have saved only about 4K mil^2 of silicon area so that the resultant chip size would be a 245^2 rather than the 253^2 as actually implemented. It is, therefore, interesting to note that all the advantages of the 16-bit architecture were purchased at a relatively minor cost in chip area.

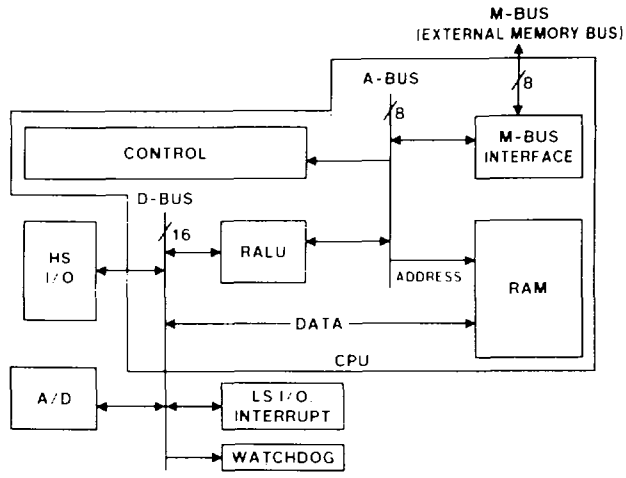

Fig. 4. Data path block diagram.

Figure 4 is a data-path block diagram, which defines the microprocessor. Major microprocessor components are the Address Bus (A Bus), Data Bus (D Bus), Control Logic, RALU, RAM, and M Bus Interface. The 8-bit M Bus transmits both address and data information between the 8061 and external memory. A data-path width of 8 bits was chosen to maximize the number of pins available for I/O. In order to optimize bus performance, the architecture was designed to include a slave program counter in all external memory devices. In the instruction stream, each byte fetch (as indicated by a Strobe pulse) causes the external slave program counter to increment and thus point to the next byte to be fetched. As a result, the 8061 does not need to generate instruction addresses in the normal instruction stream. However, on RESET, jumps, reading or writing external memory, and servicing interrupts, the 8061 will generate addresses to update the slave program counters.

Instruction execution is enhanced by the 16-bit width of the D Bus, which connects to the RALU, RAM, and on-chip I/O. All on-chip I/O registers in the high-speed I/O, low-speed I/O, interrupt, watchdog, and A/D converter are mapped into the first 16 bytes of memory space and communicate directly with the RALU by means of the D Bus using simple read/write instructions.

A key machine feature is the 120 words (16 bits) of static RAM in the microprocessor. This memory can be directly accessed by any memory instruction and can be used as scratch pad memory or general purpose registers. All 120 words can be considered as accumulators. This feature allows arithmetic and logical operations to be performed without moving data through a single accumulator register and results in significant performance improvements in program size and speed.

For controller applications, particularly automotive engine control, hardware multiply and divide are necessary to achieve the necessary system response time. A 16 × 16 multiply giving a 32-bit result can be exe-

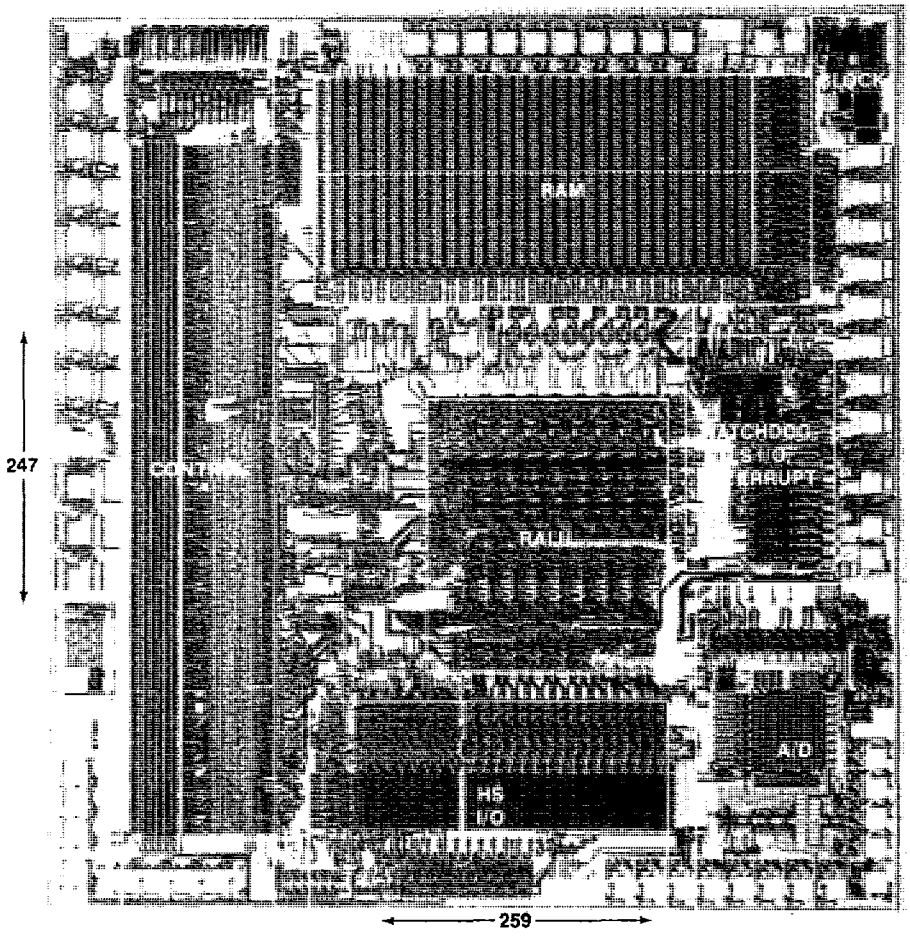

Fig. 3. 8061 layout—key points: 16-bit performance only requires 7% of die; divide requires <1% of die; large RAM, saves program size and execution time.

cuted in 5.2 μs. Division of a 32-bit dividend by a 16-bit divisor is accomplished in 5.2 μs as well.

The low-speed output is provided by a memory mapped register, which drives an 8-bit port. Outputs switch without delay when software writes to this register. Output states can also be read by the RALU, and bit masking is used to change individual bits. A 2-bit quasi-bidirectional port is also provided.

Two unique high-speed I/O coprocessors were implemented on the 8061 to reduce signal processing overhead on the CPU—an 11 deep first-in-first-out (FIFO) register stack for the high-speed input (HSI) signals and a 12-slot content addressable memory (CAM) file for the high-speed output (HSO) signals. Operation of both units, HSI and HSO, are synchronized with an internal master I/O timer, which is clocked every 2.4 μs (using a 15 MHz full-speed crystal clock).

The HSI unit (Fig. 5) looks for transitions on any of its input lines, and when one occurs, it records two things in one of its registers: the time, from the master I/O timer, and the transition. (In reality, all high-speed inputs are sampled.) The unit can be programmed to look at selected inputs for positive and negative transitions and can be programmed to generate an interrupt to the CPU when the first entry is made into the FIFO or when the next entry would cause the FIFO to overflow.

The HSO unit (Fig. 6) can be programmed to generate transitions on any of its output lines at specified times. HSO commands are stored in one of 12 CAM registers. Each register is 24 bits wide—16 bits specify the time at which the action is to occur and 8 bits specify the action(s). The CAM file rotates one position per state time. Thus, it takes 12 state times for the holding buffer to access all 12 registers. This defines the time resolution of the HSO unit as 12 state times (2.4 μs if a 15 MHz crystal frequency is used).

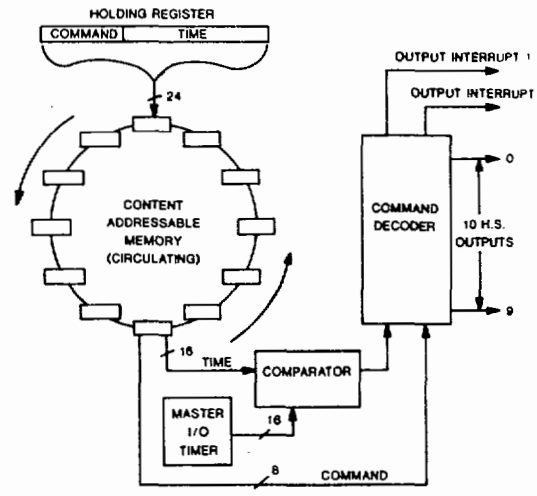

Fig. 6. High-speed output (HSO) unit.

We believe these high-speed I/O innovations are invaluable for real-time engine control applications since the coprocessors operate independently from the CPU, except for those periods when they have been programmed specifically to generate interrupts.

The on-board A/D converter is a linear, successive approximation, ratiometric type with 0.1 percent resolution (1 LSB = 5 mV). An 8-bit diffusion resistor ladder with 2 bits of capacitive interpolation is used to optimize silicon area. Process and design rules are standard HMOS technology. Conversion time is 36 μs.

The final key element of this unit is the interrupt structure. A two-level sequential priority interrupt hierarchy determines the order in which the unit services interrupt requests.

A register mapped Pending Register detects the rising edge of an interrupt input and retains it. Pending Register output drives the Mask Register, which determines if the interrupt is enabled.

A priority Select Register determines if the interrupt is high or low level and the Priority Encoder determines the order in which interrupts within a priority level are to be serviced. A higher level interrupt will interrupt the service routine of a lower level interrupt. A higher priority interrupt, however, will not interrupt the service routine of a lower priority interrupt on the same level. A list of the 8061 interrupts, along with their priorities and levels, is shown in Fig. 7.

8361 ROM/RAM

The instruction memory device for the EEC-IV system is the 8361. Each 8361 provides 64K bits of program memory internally arrayed as 4096 × 16. Each 16-bit access requires two CPU state times (0.4 μs). The RAM output buffer drives the 8-bit M Bus at the rate of 1 byte per processor state time, so

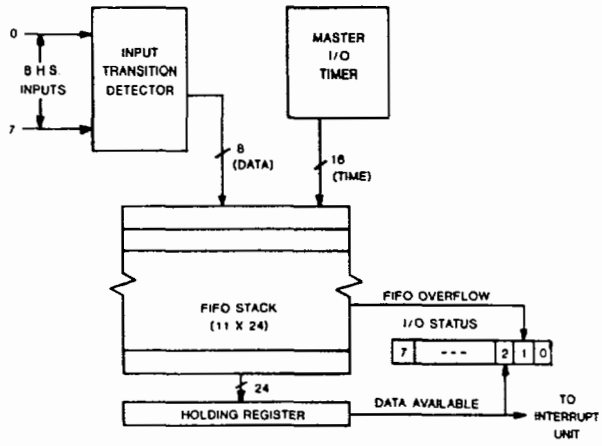

Fig. 5. High-speed input (HSI) unit.

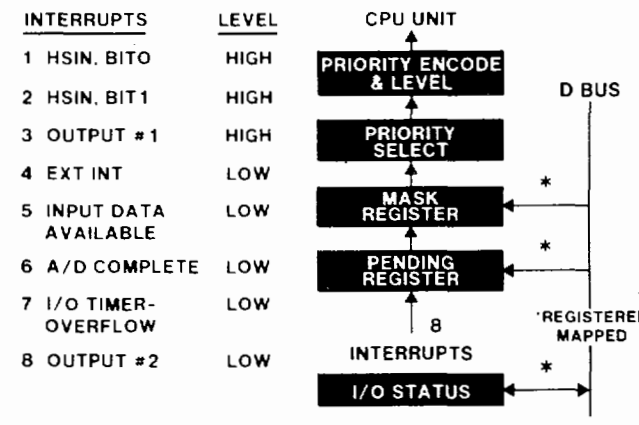

Fig. 7. Interrupt block diagram.

the processor views the ROM as 8.192K bytes of memory.

Three programmable decoder bits allow an 8361 to reside in any one of eight, 8K blocks of the 64K of system memory space. 1024 bits of RAM, organized as 128 bytes, are also located on the 8361. Nine mask programmable bits in the RAM decoder allow it to reside in any 128-byte block of the 64K address space.

Software Architecture

Every effort was made, in the design of the EEC-IV chip set, to provide the largest possible instruction set and addressing mode repertoire for future flexibility in use of structured high-level languages, like PASCAL. The 8061 supports bit, byte, word, and double-word data types with six addressing modes and eleven instruction categories defined. However, the overall instruction set/address mode mix was planned to produce a compact format. That is, frequently used instructions have the shortest instruction length with no wasted bits in the op-code. This structure uses less memory for a given set of program statements, and the program will execute faster. For assembly language programming, the user can create very compact programs by extensive use of the direct addressing mode and judicious movement of data between external memory and the register file.

A very powerful conditional jump instruction was added to the instruction set to complement the high-speed I/O units. This instruction, the "jump on bit equals zero," is used to test any one of the eight bits of a given byte and jump if the bit value equals zero. Other conditional jumps were added to avoid extensive data shifts. For typical applications based on a normal instruction mix, instruction execution times average 1 to 2 μs.

Instructions may have 0, 1, 2, or 3 operands. In three-operand instuctions—the two data operands and the destination, or results—operands are preserved in memory after execution. In the two-operand instruction, the results of the instruction replace one of the data operands in memory after execution. 8061 instruction types are summarized in Fig. 8. One operand of the two- and three-operand instructions can be addressed in any one of six modes. Fig. 9 lists the six addressing modes available in the 8061.

Diagnostics

On-board electronic engine control diagnostics were refined and expanded to exploit the powerful capabilities of EEC-IV. Generally, two types of diagnostics are performed: on-demand and continuous. *On-demand* is conducted during key-on/engine-off and during engine running modes to permit the microprocessor to test itself. *Continuous,* as the name implies, is ongoing whenever the system is in operation. Starting in 1983-1/2, EEC-IV has been used to remember conditions found during continuous testing, even after the key is turned off, with a special custom memory chip called *keep alive memory* (KAM). The KAM chip, which contains 128 bytes of read/write memory, is powered by a separate power supply so that its memory contents are retained when the EEC-IV system power is removed, i.e., during key-off. Memory retention is accomplished via a low current drain connection to the vehicle battery. This concept of continuous diagnostics of certain subsystems is interwoven with the normal engine control strategy. Faults, even intermittent ones, are recognized and stored away for recall during dealer service.

- 3-OPERAND INSTRUCTIONS
  - A = B + C
  - A & B ARE A REGISTER OR REGISTER PAIR
  - C CAN BE A REGISTER OR DATA -- ALL ADDRESS MODES SUPPORTED
  - ADD, SUBTRACT, AND MULTIPLY
- 2-OPERAND INSTRUCTIONS
  - A = A + B
  - A IS A REGISTER OR REGISTER PAIR
  - B CAN BE ANY ADDRESS MODE
  - ADD, SUBTRACT, MULTIPLY, DIVIDE, LOAD AND STORE, COMPARE, ZERO EXTEND, LOGICAL INSTRUCTIONS, SIGN EXTEND, WITH BORROW, ADD WITH CARRY
- 1-OPERAND INSTRUCTIONS
  - PUSH, CLEAR, COMPLEMENT, NEGATE, INCREMENT, DECREMENT, SIGN EXTEND, POP, JUMP, CONDITIONAL JUMPS, CALLS, JUMP ON BIT
- NO-OPERAND INSTRUCTIONS
  - PUSH AND POP PSW, ENABLE AND DISABLE INTERRUPTS, SET AND CLEAR CARRY, NOP

Fig. 8. 8061 instruction summary.

MODE	DESCRIPTION
DIRECT	THE OPERAND SPECIFIES THE REGISTER OR REGISTER PAIR CONTAINING THE DATA.
IMMEDIATE	THE OPERAND IS THE DATA, EITHER A BYTE OR A WORD.
INDIRECT	THE OPERAND SPECIFIES A REGISTER, WHICH CONTAINS THE ADDRESS OF THE REGISTER OR REGISTER PAIR CONTAINING THE DATA.
INDIRECT WITH AUTO-INCREMENT	SAME AS INDIRECT EXCEPT THAT ADDRESS REGISTER CONTENTS ARE INCREMENTED AFTER EACH ACCESS (ALLOWS EFFICIENT LIST PROCESSING).
SHORT INDEXED	BOTH A REGISTER PAIR AND A 1-BYTE CONSTANT ARE SPECIFIED. THE REGISTER PAIR CONTENTS ARE ADDED TO THE CONSTANT TO COMPUTE THE ADDRESS OF THE DATA.
LONG INDEXED	SAME AS SHORT INDEXED, EXCEPT THAT A 16-BIT CONSTANT IS SPECIFIED.

Fig. 9. 8061 Address modes.

Conclusion

The use of electronics in automobiles will continue to increase, providing improved vehicle fuel economy and performance without a deterioration in exhaust emissions and increased safety and comfort [2]. Future power train electronics will see the engine control system expanded to include the transmission. New transmissions will be electronically controlled to provide smooth, indiscernible shifts from one gear to another. The electronic control module will continuously monitor the requirements for maximum fuel economy, performance, and exhaust emission control and will select the optimum combination of engine and transmission parameters, thus becoming an integrated power train control system. The computer described herein has that capability by simply expanding the available memory size.

Control of engine accessories can produce improvements in fuel economy. Electronic control of the alternator, engine cooling fan, power steering pump, air-conditioning com-

pressor, and other accessories will optimize their performance with minimum engine loading.

Adaptive control strategies, vehicle diagnostics, and instrumentation memory requirements, such as electronic odometers, are but a few of the possibilities. Other electronic and semiconductor technologies of importance to future automotive systems include low cost "smart" power devices, voice recognition technology, electronic component packaging, low-cost sensors, and thick-film circuit technology. For additional information on the future of the EEC-IV system, please refer to the *Convergence '84 Proceedings* [3].

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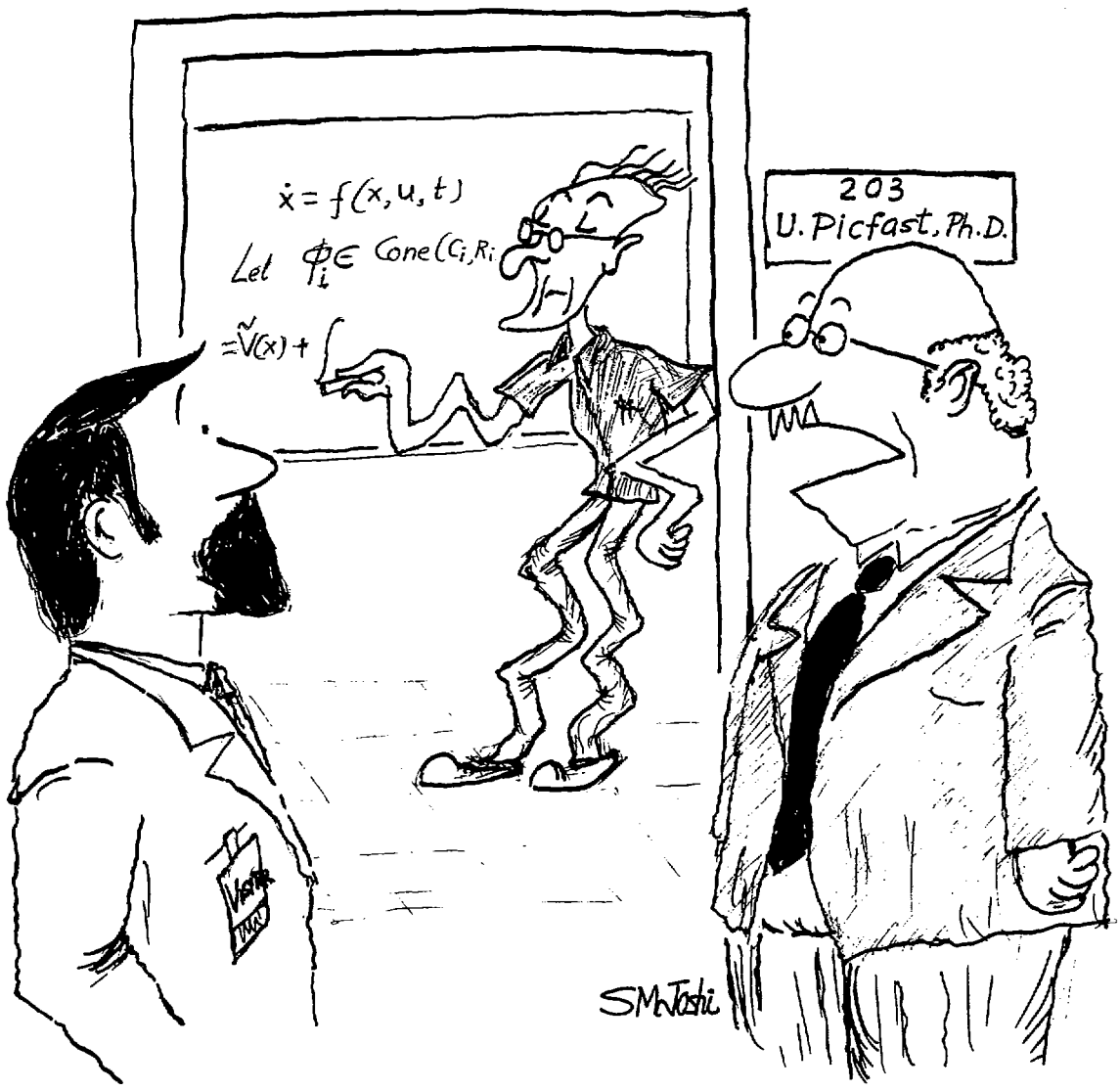
Out of Control



"He may not look impressive—but he's a world authority on nonlinear phenomena."