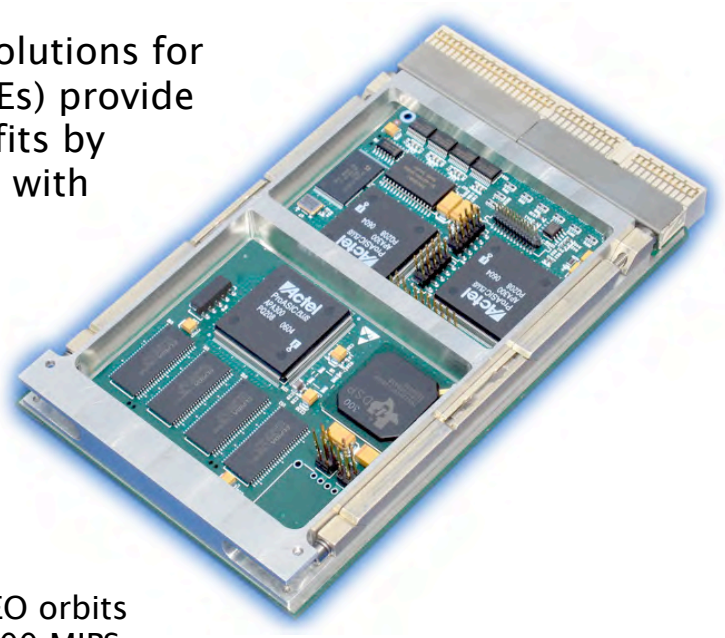
Proton200k™ DSP Processor Board

DSP for Space Applications

Space Micro's state-of-the-art solutions for single event radiation effects (SEEs) provide extraordinary performance benefits by removing the barriers associated with commercial DSPs.



The result is the first high-speed, SEE-hardened DSP available for space and satellite applications.

Features:

- Radiation Hardened for LEO and GEO orbits
- Optimized Processing Speed of 4,000 MIPS or 900 MFLOPS
- Industry Standard, upwardly compatible DSP Processor
- cPCI bus and form factors to support most configurations

- Payload Applications
  - On-board Digital Signal Processing (DSP) of sensor data for speedy and efficient transfer to ground.
  - Fixed Point (1 GHz) and Floating Point (300 MHz) versions operate at 5 Watts per board (typical).
- C & DH Applications
  - Capacity, speed and power requirements suitable to be sole computer for micro- and nano-satellites handling both housekeeping and payloads.

Space Micro Inc.

Proton200k-Fl (Floating-Point DSP)
Proton200k-Fx (Fixed-Point DSP)

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SPACE MICRO INC.

v 2.9.2

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Technical Specifications

Radiation Tolerance

- **SEL** > 70 LET (MeV-cm2/mg)
- **SEU** < 1 per 1,000 days (1.0 E-4, 90% W.C. GEO, Orbit dependent)
- **TID** > 100krad (Si), Orbit dependent
- **SEFI** 100% recoverable

Processor

- **TI 320C6XXX Series DSP** processor using:
  - TTMR™ technology for SEU detection/mitigation.
  - H-Core™ technology for SEFI detection/mitigation.
- **Fixed Point Version:**
  320C6415, 1GHz 8,000 MIPS native
  - 4,000 MIPS at 1E-4 unrecoverable errors /day
  - L1 32KB (16/16KB) Program/data Cache
  - L2 1MB (Cache/Mapped RAM, flexible allocation)
  - Timers 3, 32-bit
- **Floating Point Version:**
  320C6713, 300 MHz, 1,800 GFLOPS native
  - 900 MFLOPS/ 1,200 MIPS at 1E-4 unrecoverable errors/day
  - L1 8 KB (4/4KB) Program/Data Cache
  - L2 256KB (64KB Cache/Mapped +192KB Mapped RAM)
  - Timers: 32-bit (two)

Memory

- **128 Mbyte SDRAM w/EDAC**
  1 Mbyte EEPROM to 8 Mbyte (option)
- 512 Mbyte RH Flash (option)

Power

- 5-7 Watts (standard board), full speed

Interfaces

- **cPCI** 32bit, 33 MHz I/O bus
- **3.3V** I/O Voltage
- **UART** 4-channel buffered asynchronous w/ RS422
- **16 GPIO** Prog. General-purpose I/O
- Options LVDS; 1553; SpaceWire; CAN, Ethernet; USB; I2C

Mechanical

- **3U**, 100x160 mm [3.74 x 6.3”]
- 6U, 233x160mm [9.2 x 6”] (option)
- PCI-104 stretch [3.6 x 5"] (option)
- Other custom sizes (option)

Operating System and Software Support

- TI DSP/BIOS RTOS (option)
- TI Code Composer Studio (option)
- **JTAG** debugging support

Screening

- **Commercial**
- Class S / B (options)
- -20 to +85˚C Temp. Range
- MIL Temp range and beyond (options, Contact Factory)

Models (Proto/EDM/EM/FM)

- Prototype (off-the-shelf), for software development
- Engineering Development, same form factor and I/O as Flight
- Engineering (flight PCB w/ non-flight parts; Convection cooled)
- Flight (Conduction cooled)

Services Available

- DSP Software Optimization

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Space Micro Innovations & Enabling Technologies

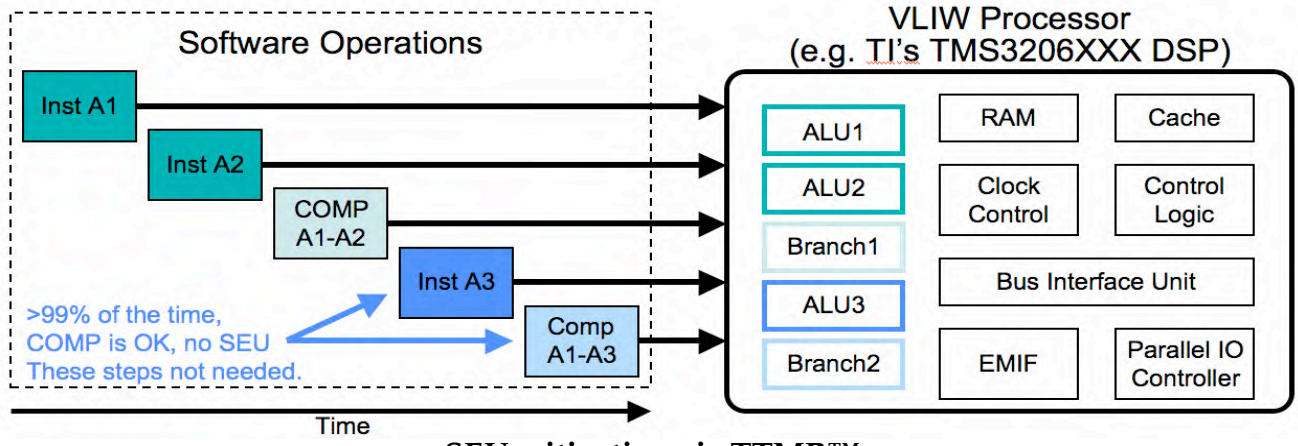
For Space Operations, State-of-the-Art Commercial Processors are prone to:

- Upsets (SEU), Single Event Upsets
- Functional Interrupts (SEFI) which could lock up processors

Space Micro uses its patent-protected technologies to mitigate, detect, and correct these problems.

SEU mitigation via TTMR™

- Detects & corrects SEUs
- TTMR™ enables use of State-Of-Art commercial Processors
- TTMR™ Combines Time with TMR (Triple-Modular-Redundancy)
  - Time: Takes advantage of the features of Very Long Instruction Word (VLIW) processors for parallel processing of instructions.
  - Spatial: Triple Modular Redundancy (TMR) operations on separate ALU units within a single DSP. Comparisons will only invoke Instruction set A3 if A1 ≠ A2.
- SEU error rate equals to TMR rate
- Proton radiation tested at 51 MeV
- TTMR implementation is transparent to DSP user, hardware or software-wise.



SEU mitigation via TTMR™

SEFI Mitigation via HCORE™

HCORE™ monitors processor functionality in real-time, provides fats detection and correction of any SEFIs that may occur.

- Hardware
  - Rad-Hard external watchdog circuit sends interrupts and reset as required
- Software
  - CPU - Generates health/status signals, run interrupt routines
  - H-Core IC - Monitors signals, initiate post-SEFI recovery using Interrupts, and full reset as required

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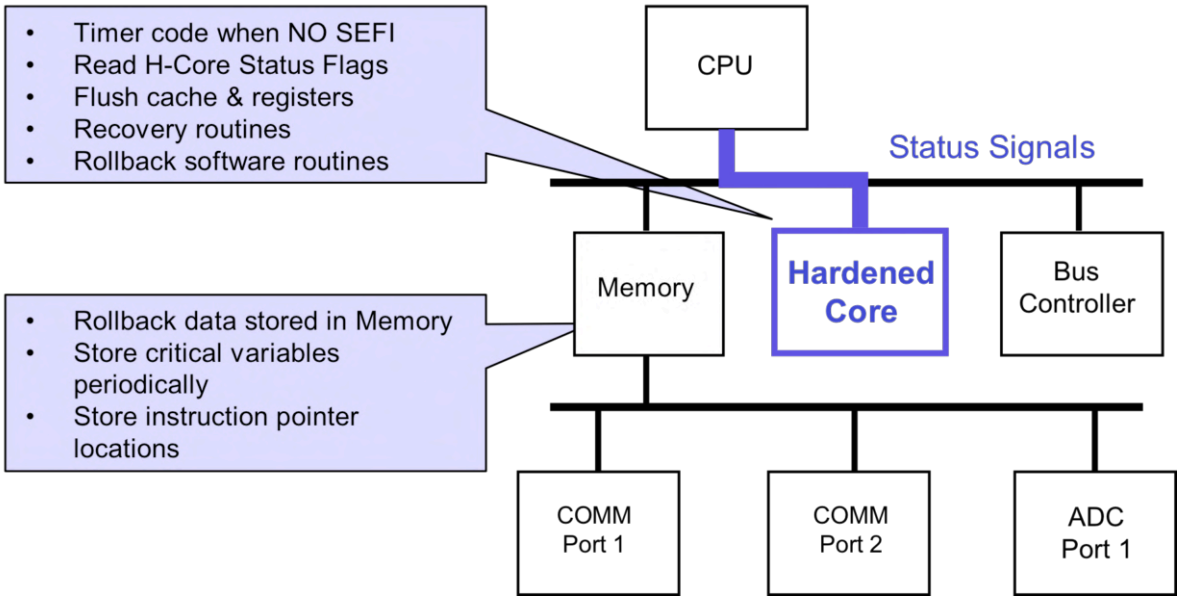
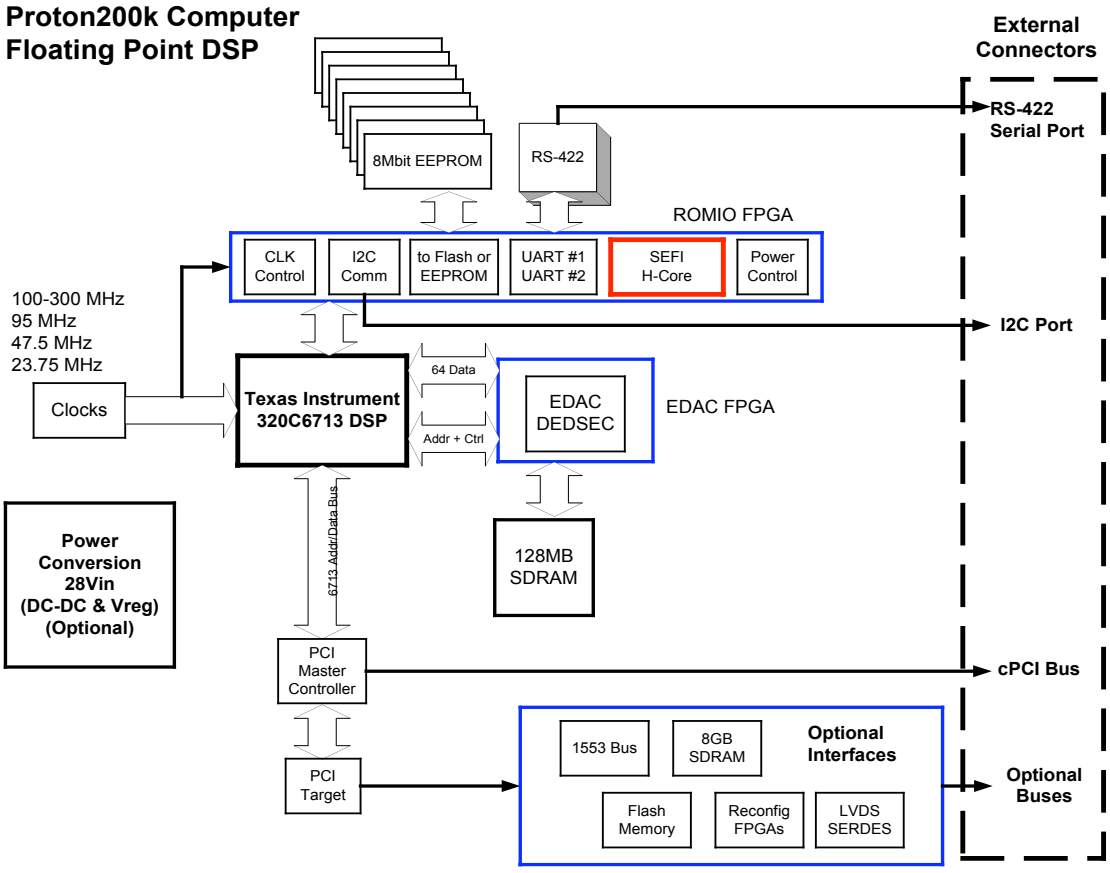


SEFI Mitigation via HCORE™



Proton200k Block Diagram

Please contact Space Micro for application specific configurations or further details.

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