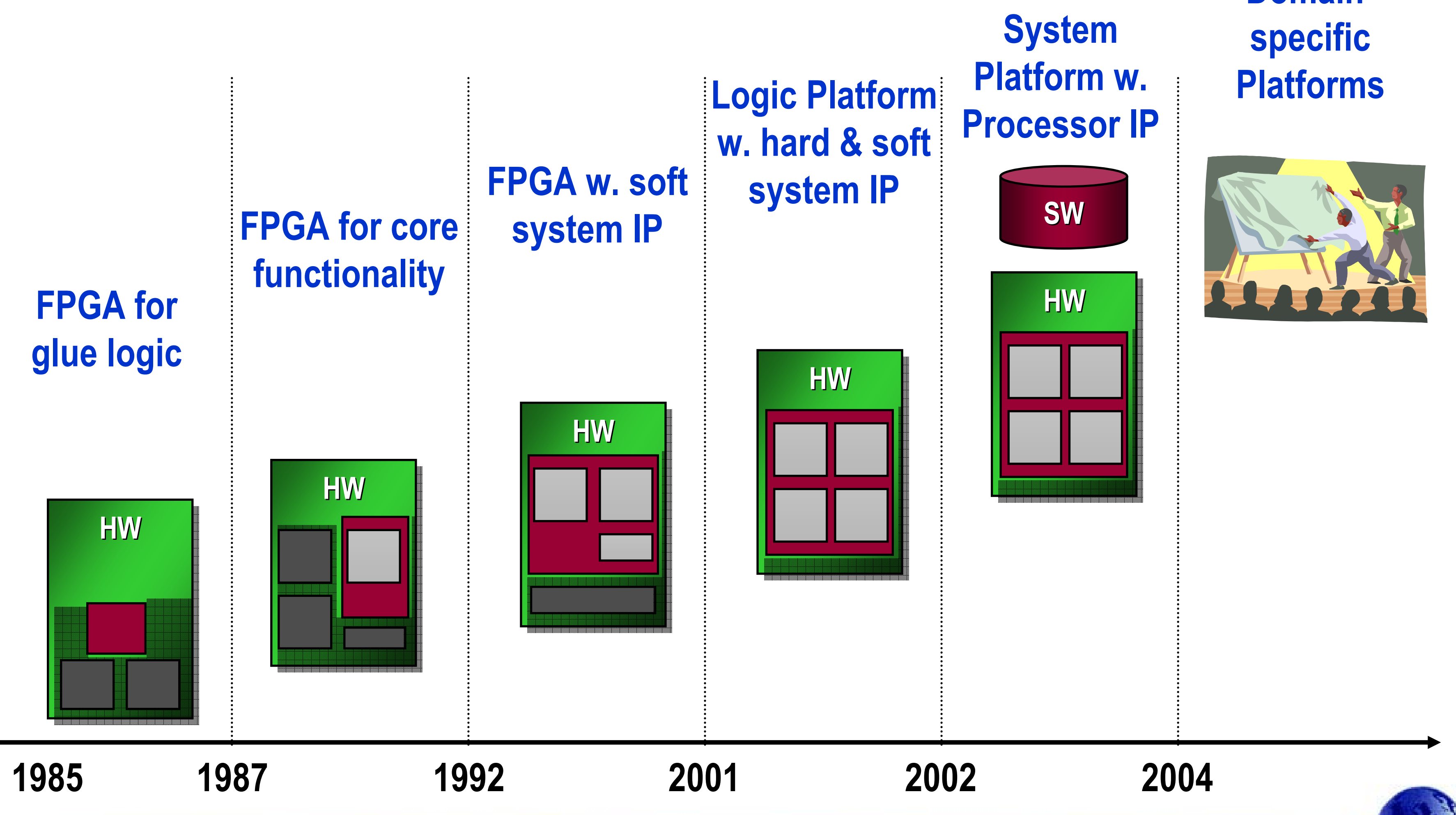
Revolutionary Architecture for the Next Generation Platform FPGAs

Embargoed News:

December 8, 2003

The Evolution of FPGA Architectures



FPGA Solution

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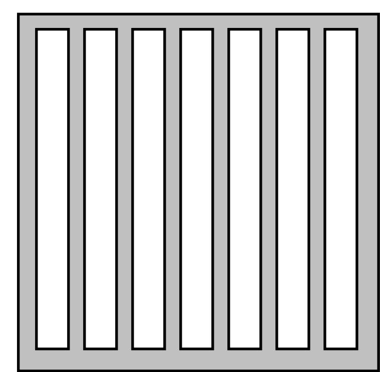
The ASMBL(TM) Architecture

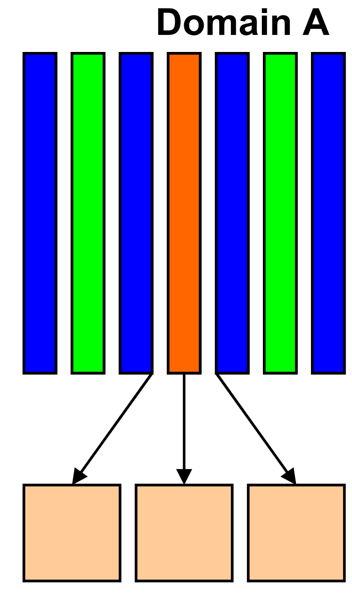
Application Specific Modular Block Architecture

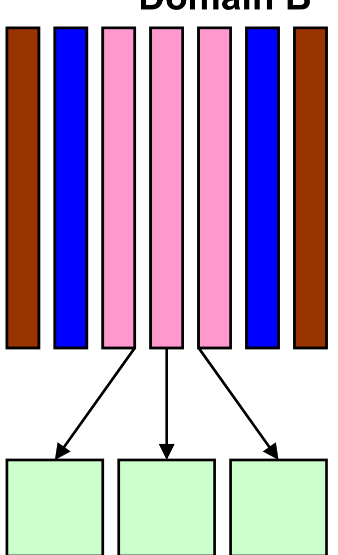
Column Based ASMBL Architecture

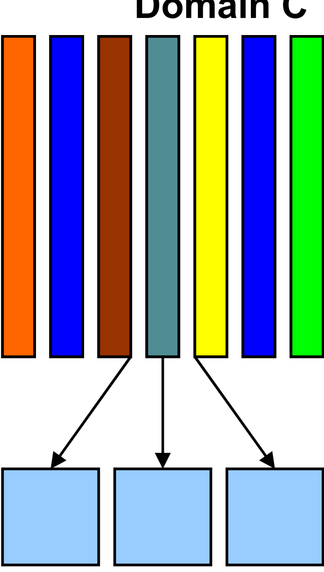


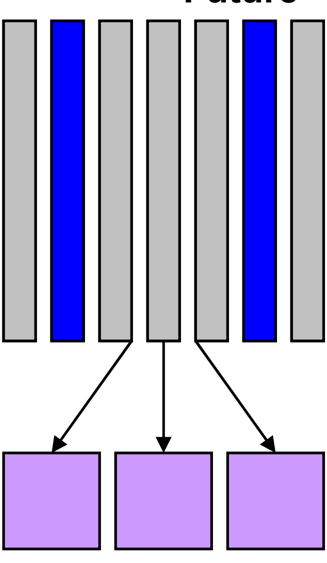
Feature Options

- Logic
- DSP
- Memory
- Processing
- High-speed I/O
- Hard IP
- Mixed Signal
- Future...









Applications

Addressing Geometric Constraints

- I/O and array dependency
- Power & ground distribution
- Hard IP scaling

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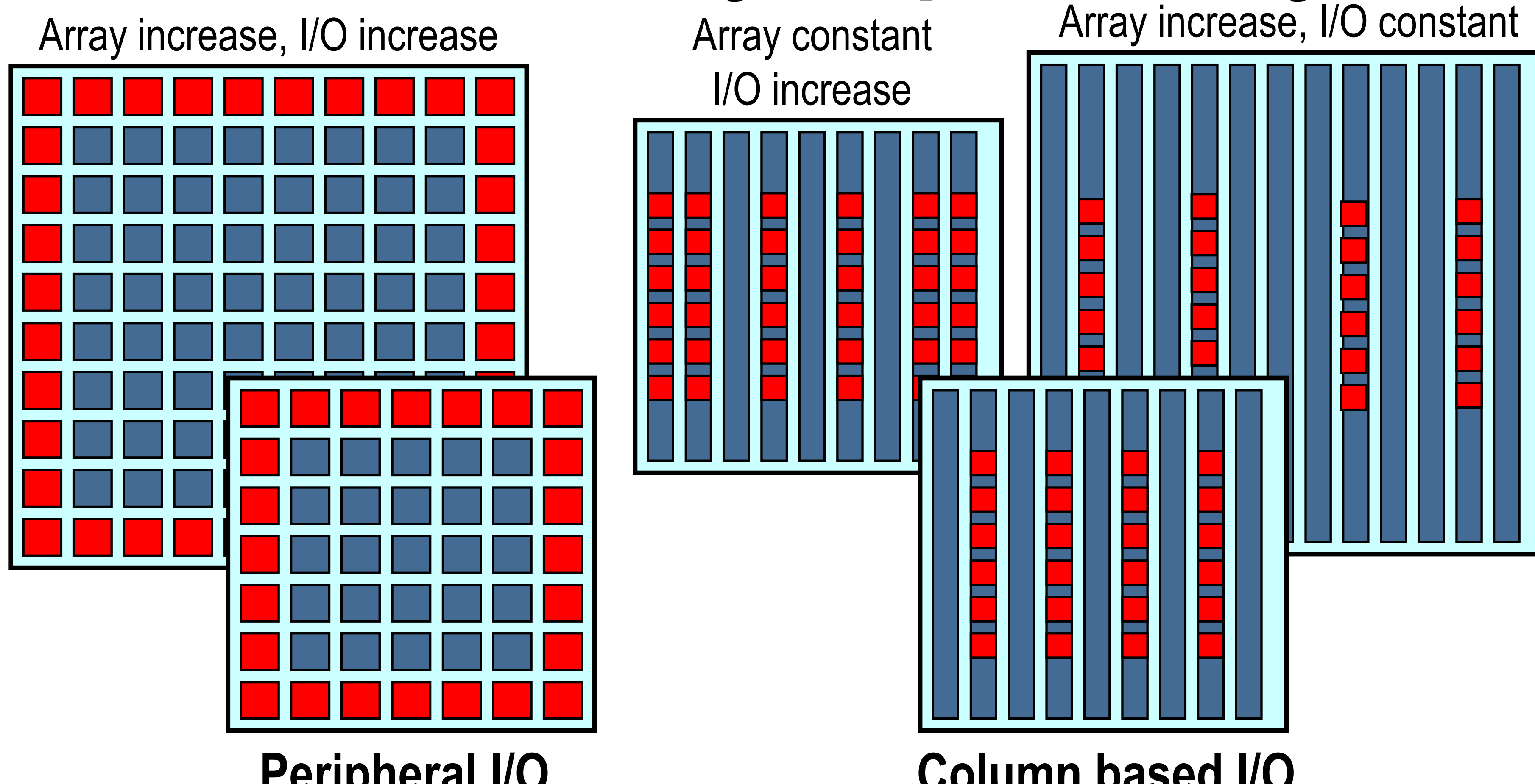
ASBML Addresses I/O and Array Dependency



Peripheral I/O dependent on array size

Column based I/O independent of array size

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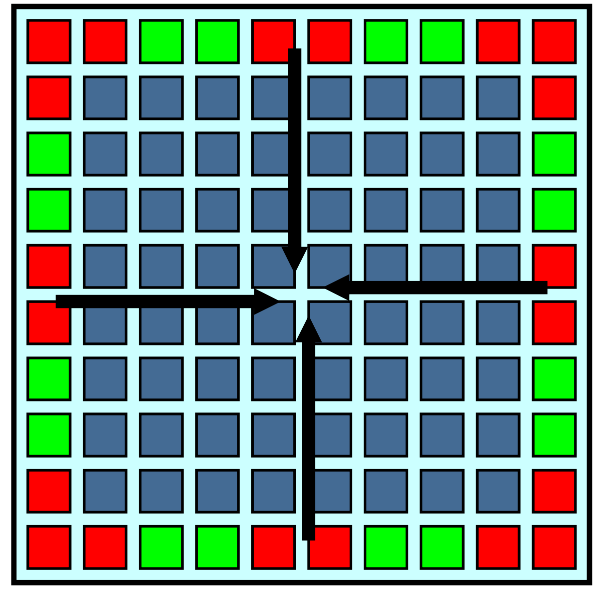
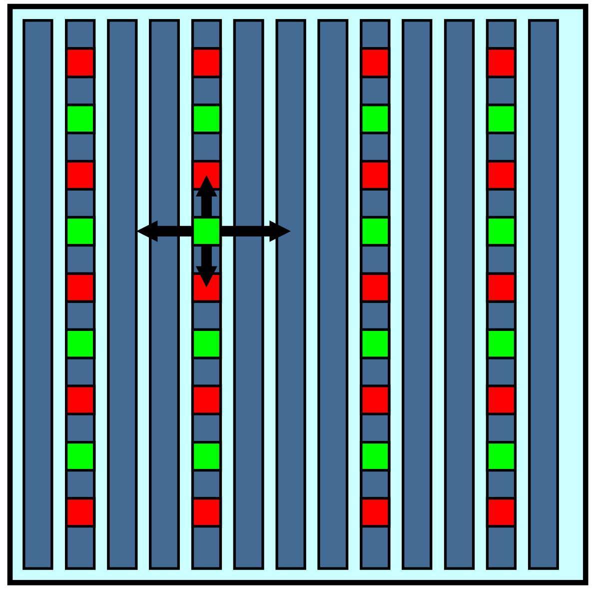
ASMBL Addresses PWR & GND Distribution

- New Pwr & Gnd distribution reduces voltage drop
- Switching reliability increase via higher thresholds



Traditional Architecture



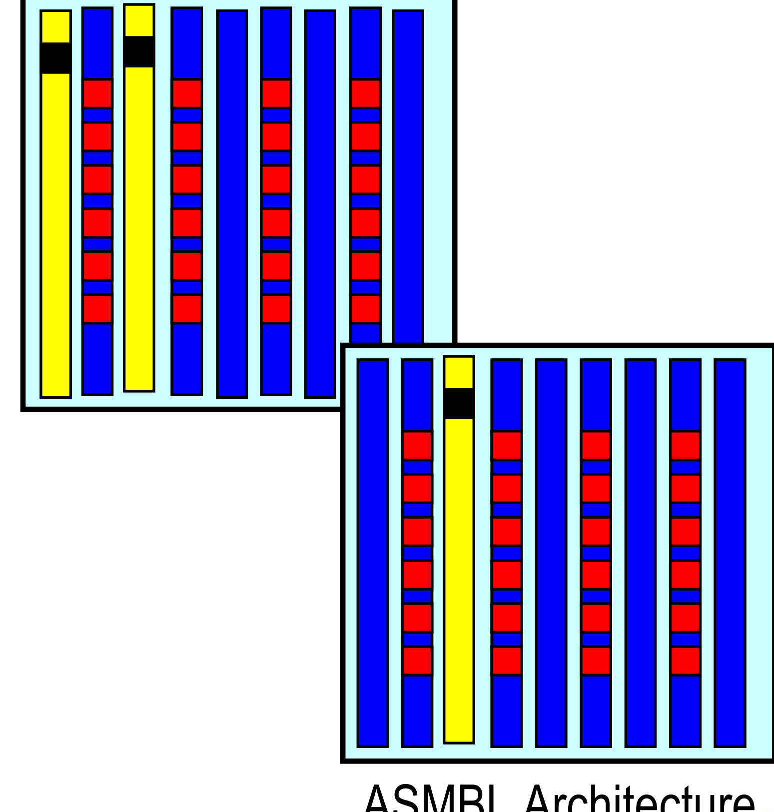
ASMBL Architecture

ASMBL Addresses Hard IP Scaling

Array size increase to accommodate feature scaling

Traditional Architecture

Array size constant as features scale independently



ASMBL Architecture

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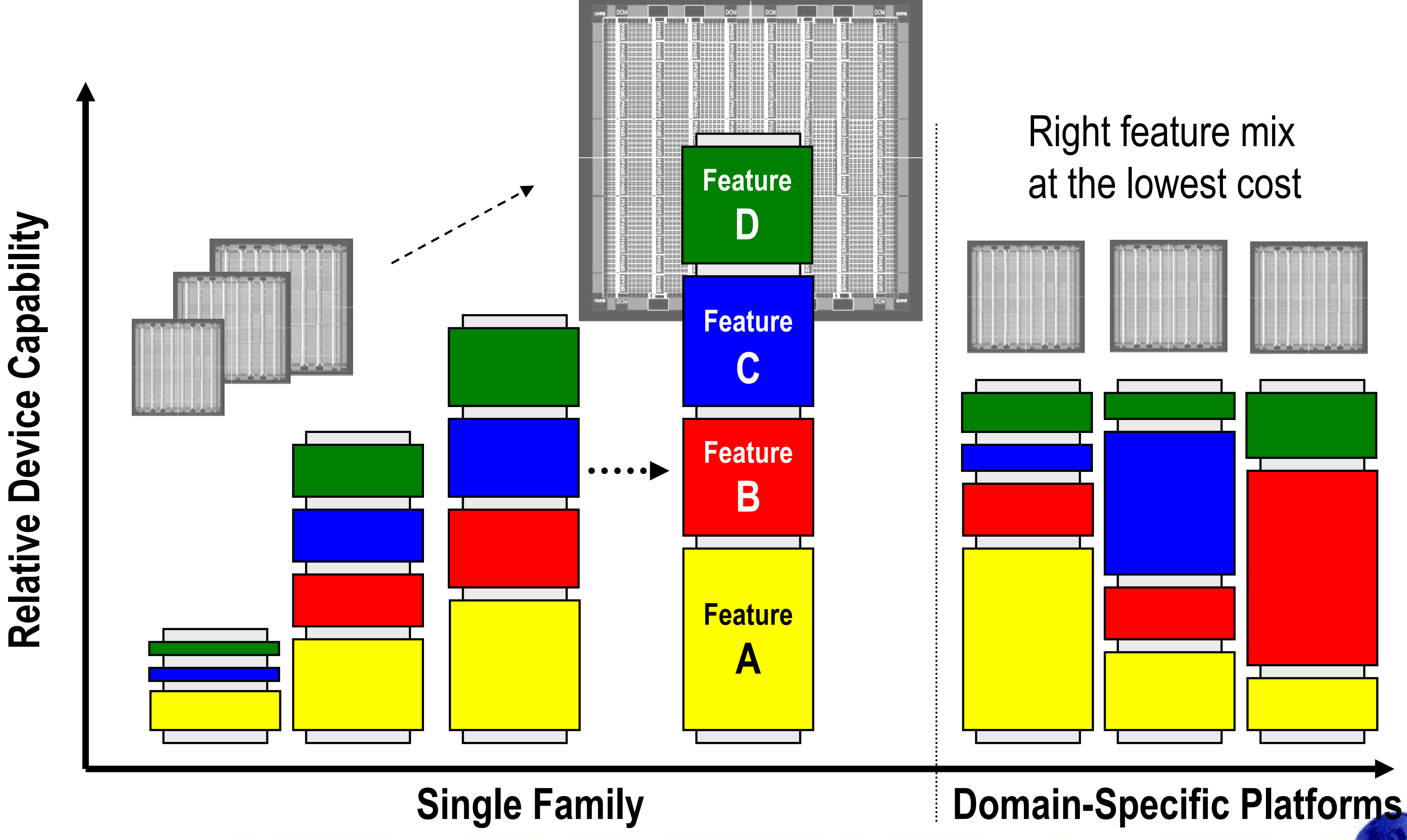
ASMBL Advantages

- Xilinx Benefits
  - Reduces time & risk for FPGA platform development
  - Enables cost-effective assembly of multiple platforms
  - Allows rapid response to new market demands
- Customer Benefits
  - Highest value solution at a given price point
  - Right feature mix for a given domain

ASMBL Enables Domain-Specific Platforms



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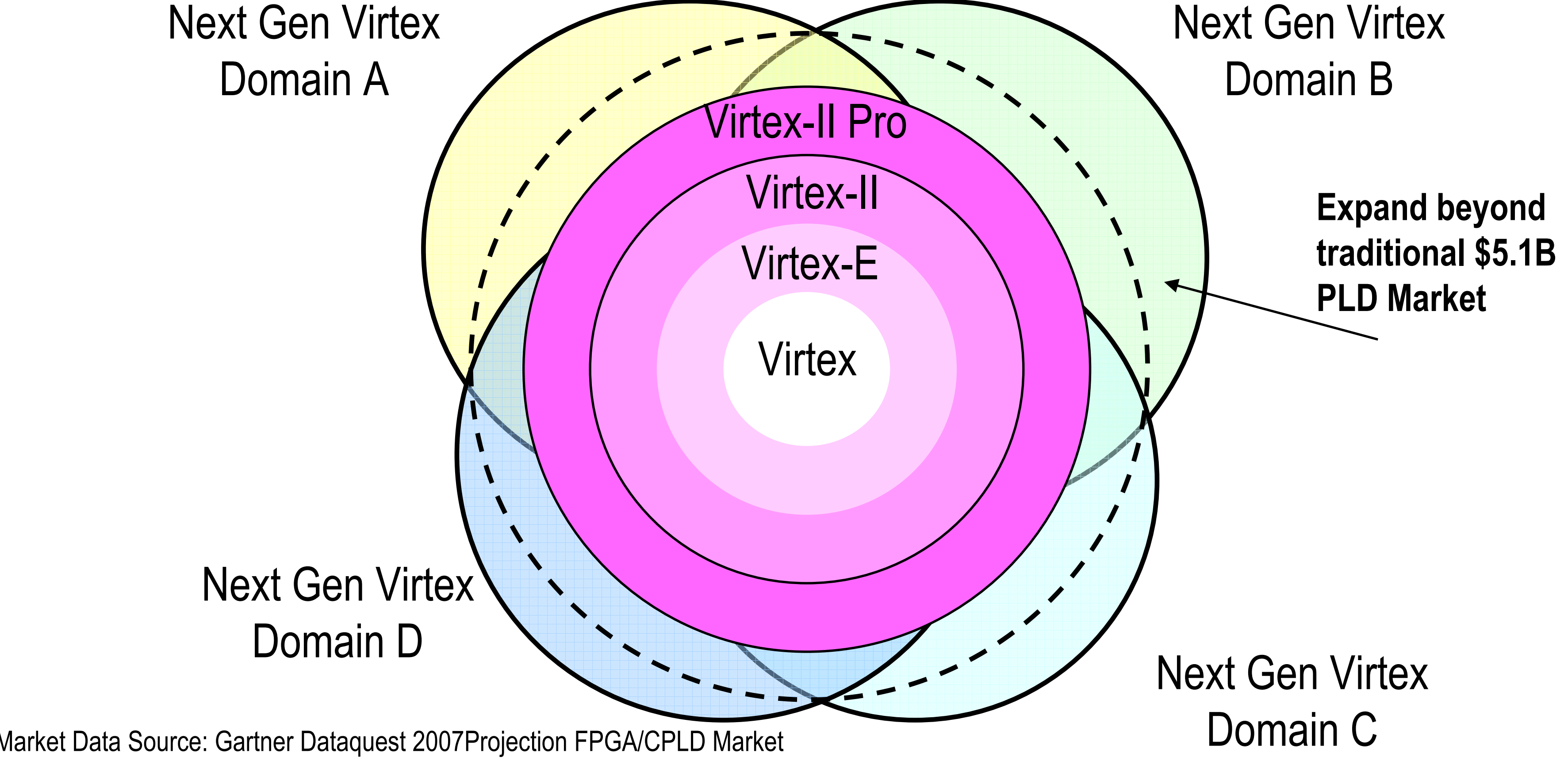
Cost Effectively Expanding Xilinx FPGA Application Domains



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Taking Advantage of Moore's Law

Millions of Transistors

1000
900
800
700
600
500
400
300
200
100

1996 1997 1998 1999 2000 2001 2002 2003 2004 2005

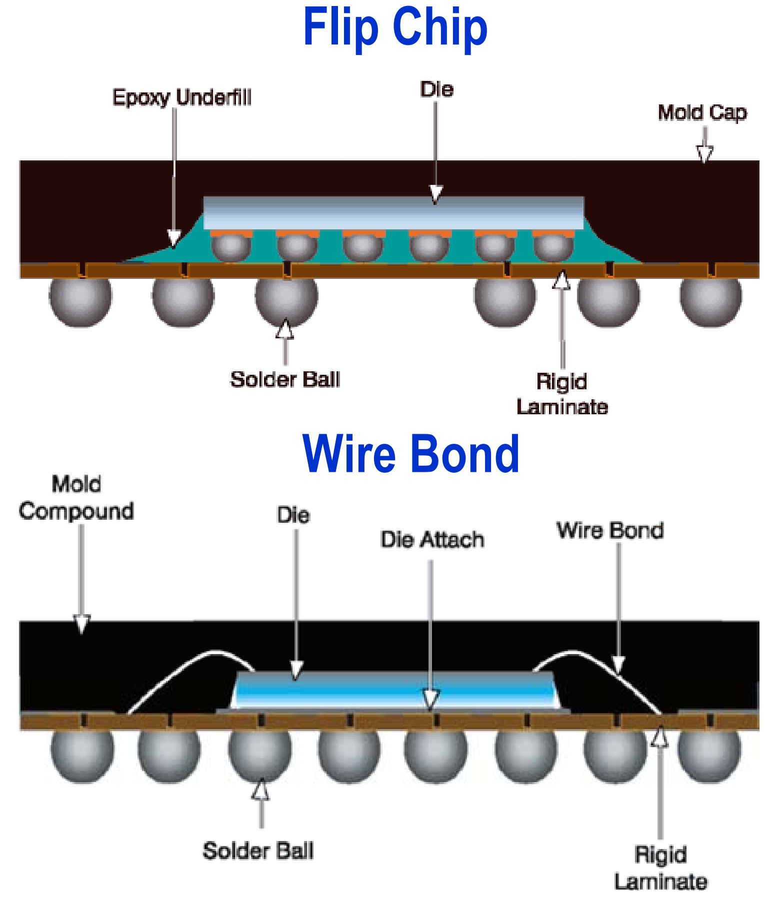
Virtex
Virtex-E
Virtex-II
Virtex-II Pro
Next Gen Virtex

Transistor count increases, cost decreases

Taking Advantage of 10+ Layers of Metal

Taking Advantage of Advanced Packaging

- Flip Chip enables column based architecture
- Allows connecting to I/Os anywhere on the die
- Enhanced thermal dissipation



Package source: Amkor Technology

Next Generation Cost Metrics

Cost per Function

220 nm

180 nm

150 nm

130 nm

Sub-90 nm

Next Gen Virtex

1998 1999 2000 2001 2002 2003 2004 2005

Old density based metrics

$/LC and $/Gate

New capability based metrics

$/MAC/s or $/BOPS

$/Mbit of storage

$/Gbps bandwidth

$/Gbyte/s bandwidth

$/DMIPS

$/system functionality

$/mixed signal

Conclusion

- ASMBL enables domain-specific Platform FPGAs
- Addresses traditional architectural limitations
- Highest value solution at a given price point