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Backplane Channels and Correlation Between Their Frequency and Time Domain Performance

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Abstract

Emerging standards that address serial 10 gigabit speeds across a backplane have been building upon 4-port S-parameter measurements of backplane channels. Transmission and return loss magnitude data has been a building block for the channel model for many specifications, such as XAUI and 10GBASE-CX4. Channel compliance methodologies for backplanes considered have been focusing more on time domain analysis of the channel, as the shape and magnitude of the channel pulse response provides critical information to the designer of what is required to equalize the channel. In addition, such analyses have shown that the interaction of the channel with the associated device package and terminations is critical in ultimately determining if a given system can be made to run at a given speed with acceptable performance.

The focus of this paper is the correlation of various physical aspects of the backplane channel to features observed in the frequency-domain transmission response and the time-domain pulse response. Using S-parameter measurements from a controlled backplane environment, a complete analysis is performed to understand how the different variables in a system environment (daughtercard trace length, backplane trace length, layer connection, and overall stackup design) can impact the time and frequency domain responses of the various channels considered.

Author's Biography

John D'Ambrosia is the Manager of Semiconductor Relations for Tyco Electronics in Harrisburg, PA. John works with semiconductor vendors to explore the interaction between semiconductor devices and Tyco Electronics interconnect solutions. This has led to his involvement in standards bodies defining solutions for backplane environments. He was an active participant in the development of XAUI, and served as the chair of the 10 Gigabit Ethernet Alliance XAUI Interoperability Group, which drove interoperability testing for XAUI solutions for the industry. He helped organize the High Speed Backplane Initiative (HSBI), as well as served as its secretary. John served as the chair of the Optical Internetworking Forum's (OIF) Market Awareness & Education Committee, and is participating in the development of the OIF Common Electrical I/O (CEI) project. Currently, John is the secretary for the IEEE 802.3ap Backplane Ethernet Task Force. John received a B.S. in Electrical Engineering Technology from the Pennsylvania State University in 1989 and a Master's Degree in Engineering Management from the National Technology University in 1999.

Adam Healey is a Distinguished Member of Technical Staff at Agere Systems and is responsible for the definition of subsystems and components required for access and enterprise networks. Adam joined Lucent Microelectronics / Agere Systems in 2000. Prior to joining Agere Systems, Adam worked for 7 years at University of New Hampshire's InterOperability Lab where he developed many of the test procedures and systems used to verify interoperability, performance, and compliance to standards of 10, 100, and 1000 Mb/s electrical and optical links. Adam is a member of IEEE and contributes to the development of international standards as a member of IEEE 802.3 working group. He currently serves as chair of the IEEE P802.3ap Backplane Ethernet Task Force. Adam received a BS and MS in Electrical Engineering from the University of New Hampshire.

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Introduction

In the development of a standard for a multi-gigabit serial I/O, there are three aspects to be addressed – the transmitter, the channel, and the receiver (refer to
Figure 1). A complete system specificaiton must completely define at least two of these three aspects. Typically, the channel is the most difficult to specify. While it is often argued that the channel can be tailored to fit the solution space, the reality is that the application and its associated economics will define the channel. Therefore, the difficulty in specifying the channel results from the sometimes contradictory requirements from multiple application spaces represented by a diverse set of users and suppliers.

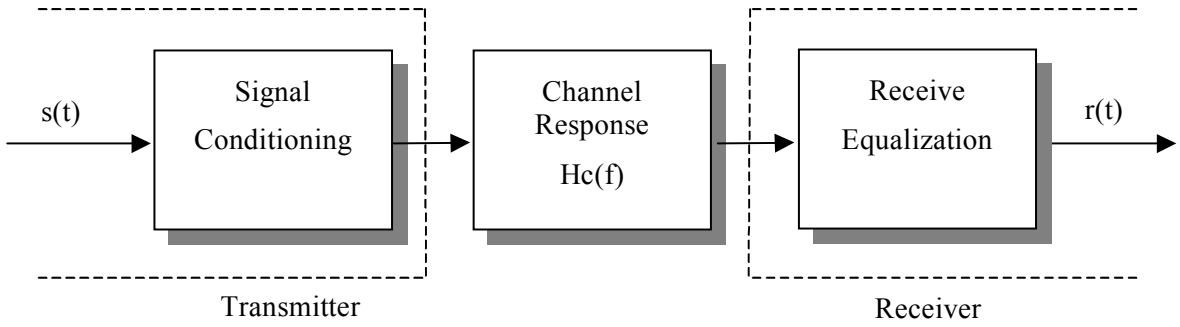


Figure 1 - Aspects to the System Interconnect

Scattering parameters (S-parameters) have played a crucial role in defining the channel, as they have been used in a normative and informative manner to describe transmission, return loss, and crosstalk performance. Unfortunately, making a real system work is not as simple as drawing a limit line for any one of these parameters. In truth it is a balanced equation where these factors interact with each other. This simple fact was the impetus for the development of a new tool for channel compliancy, referred to as StatEye.[1] Tools like StatEye derive statistics from the channel pulse response which may then be used to estimate the link bit error ratio (BER).

The problem with either approach, frequency-domain limit lines or StatEye, is bridging from the result to a basic understanding of the channel. S-parameter characterization is a fundamental building block that can be used as part of subsequent time domain simulation and analysis to predict performance. A simple magnitude plot of any one aspect, however, does not give an answer to system performance. The output of StatEye, on the other hand, provides a total picture, which may blur understanding the impact of any individual aspect of the channel.

This paper is written to serve the industry as a basis for understanding the impact of various aspects of the channel transmission response on 10.3125 Gb/s serial I/O. S-parameter measurements of different systems are used to generate pulse responses. The channels are then examined from both frequency- and time-domain perspectives to achieve a better understanding of the task facing the designer of a receiver for 10.3125 Gb/s application.

Channel Characterization Via S-Parametersii

The electrical performance of a differential channel can be measured using a four port vector network analyzer (VNA) as shown in Figure 3. The VNA measures the single ended S parameters in the frequency domain. Figure 2 shows a port labeling scheme for a differential channel that is measured as two single-ended channels.

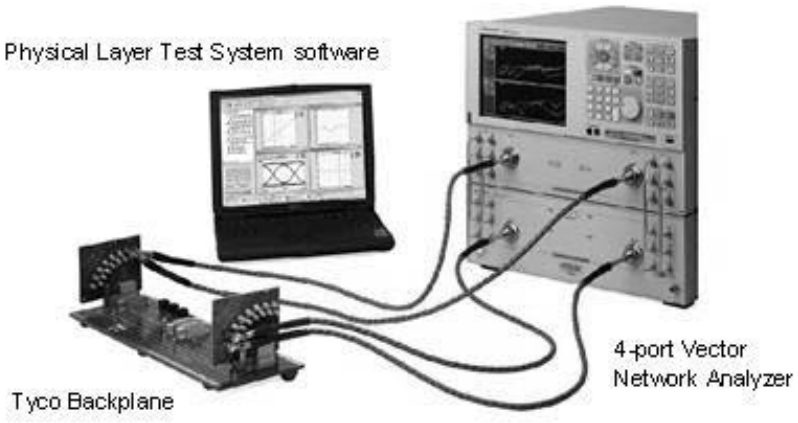


Figure 2 – Vector Network Analyzer Setup

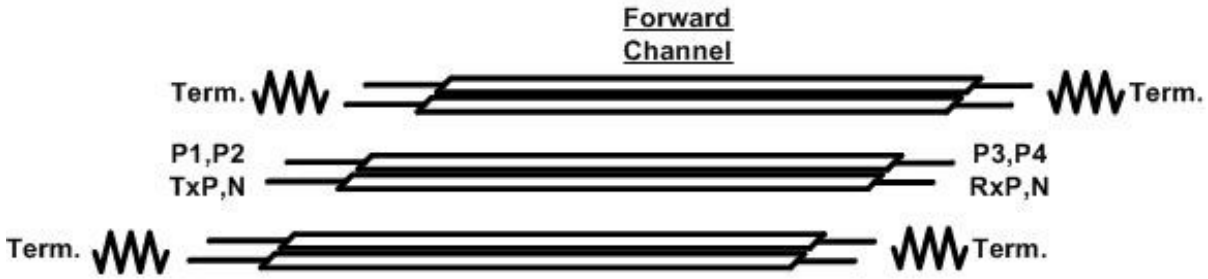


Figure 3 - VNA 4 Port Labeling Scheme

The single-ended S-parameters are then mathematically transformed into mixed-mode S parameters (refer to Figure 4). The mixed-mode parameters provide information about the differential return and insertion loss.

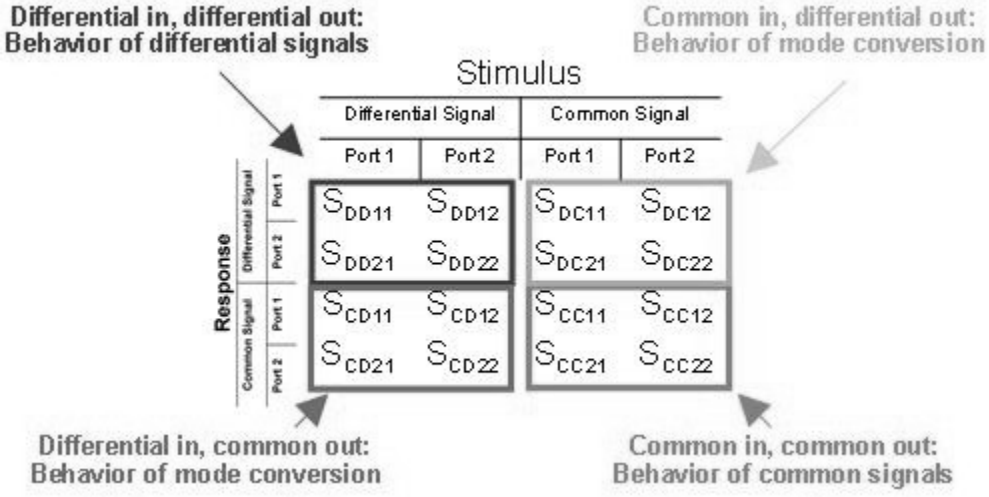


Figure 4 - S Parameter Quadrants

In order to interpret the large amount of data in the differential parameter matrix, it is helpful to analyze one quadrant at a time. The first quadrant is defined as the upper left 4 parameters describing the differential stimulus and differential response characteristics of the device under test. This is the actual mode of operation for most high-speed differential interconnects and is the quadrant that receives the most attention. It includes input differential return loss (S_{DD11}), input differential insertion loss (S_{DD21}), output differential return loss (S_{DD22}) and output differential insertion loss (S_{DD12}). Note the format of the parameter notation S_{XYab}, where "S" stands for scatttering parameter or S-parameter, "X" is the response mode (differential or common), "Y" is the stimulus mode (differential or common), "a" is the output port and b is the input port. This is the typical nomenclature for scattering parameters.

The second and third quadrants are the upper right and lower left 4 parameters, respectively. These are also referred to as the mixed mode quadrants. This is because they fully characterize any mode conversion occurring in the device under test, whether it is common-to-differential conversion (EMI susceptibility) or differential-to-common conversion (EMI radiation). Understanding mode conversion is very helpful when trying to optimize the design of interconnects for gigabit data throughput.

The fourth quadrant is the lower right 4 parameters and describes the performance characteristics of the common-mode signal propagating through the device under test. For a properly designed device there should be minimal common-mode output and the fourth quadrant data is often of little concern.

Backplane Channels

As described above, S-parameters are being used to characterize a channel's performance in the frequency domain. S_{DD21}, which is the differential response at the output of the channel based on a differential input, has been used as the main way of characterizing the capability of a channel. Figure 5 illustrates the well-documented impact of signal layer connection on the S_{DD21} performance of 34-inch channels from Tyco Electronics HM-Zd XAUI Backplane Platform, which is based on Nelco 4000-2 and has a nominal thickness of 200 mils.

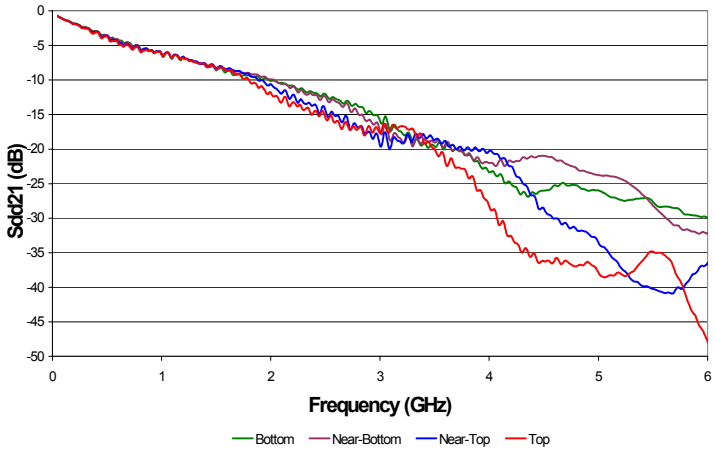


Figure 5 - Impact of Layer Connection on S_{DD21}

While Figure 5 demonstrates the layer connection effect, it does not address the ramifications of the full system interconnect. The complete backplane system interconnect is shown in Figure 6. The channel designer must balance the needs of the architecture to be implemented with the requirements of the various interconnects used to connect the components. Thus, the trace conditions from the transmitter on one card, on the backplane, and to the receiver on the other card must all be considered. Differential

trace geometries, trace length, board materials, and layer connection will all have an impact on the total channel performance.

Another aspect of the channel performance is that the receiver is typically specified as being AC coupled in most high speed I/O standards. First of all, AC coupling may be integrated into the device or may be discrete components on the line card. Figure 6 demonstrates an implementation using a discrete AC coupling scheme. While there are constraints related to integrations of coupling capacitors into a device, the implementation shown in Figure 6 has a direct impact on channel performance. With a discrete component implementation, it is a reasonable assumption that either one or two vias will exist. Thus, there will be the potential for additional impedance discontinuities and coupling structures inducing additional crosstalk.

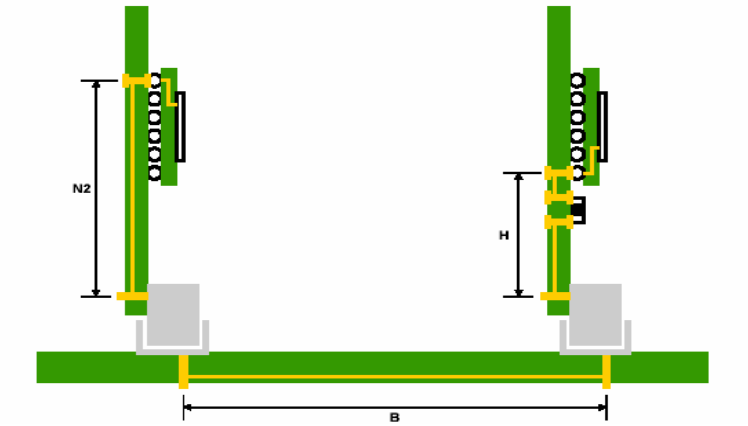


Figure 6 – The Backplane System Interconnect

To limit the scope of this study, the backplane channel model defined by the IEEE 802.3ap Backplane Ethernet Task Force will be used. In this model, TP1 is defined at the edge of the transmitter, while TP4 is defined at connector side of the AC-coupling capacitor. Thus, the impact of everything beyond TP4 is not included.

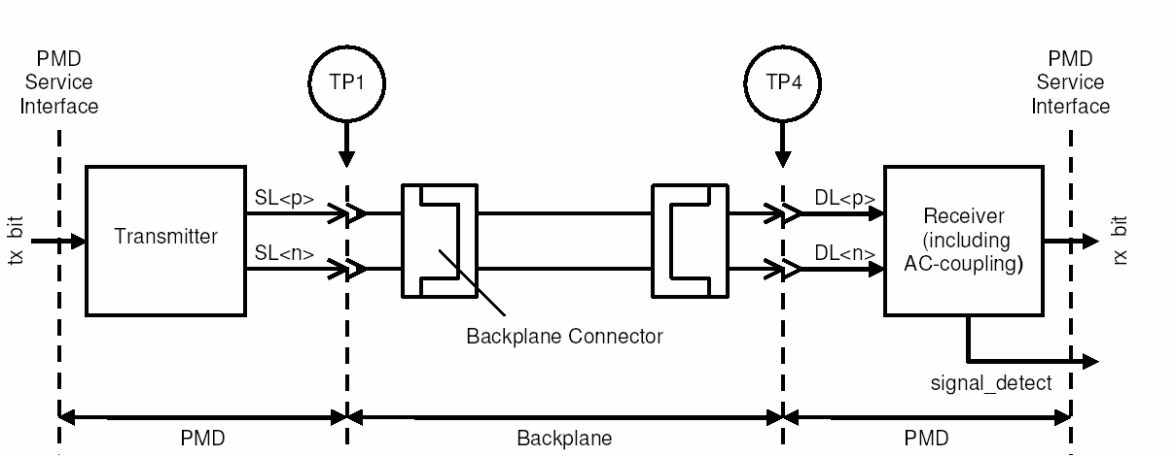


Figure 7 - IEEE 802.3ap Backplane Channel Model[iii]

Test Fixturing and Characterization

To examine the interrelations between channel components, various backplanes and line card designs were considered.

To explore the limitations of current backplane practices, the Tyco Electronics Z-PACK HM-Zd Legacy Backplane was used. This backplane is based on Nelco 4000-6 and has a nominal backplane thickness of 200 mils. The nominal trace width of the design is 6 mils, but the board used in this testing had a trace width of 5.5 mils. Traces are routed in a stripline configuration, and are distributed throughout the entire stackup of the backplane. No counterboring on the backplane vias has been done. The stackup is shown in Figure 8.

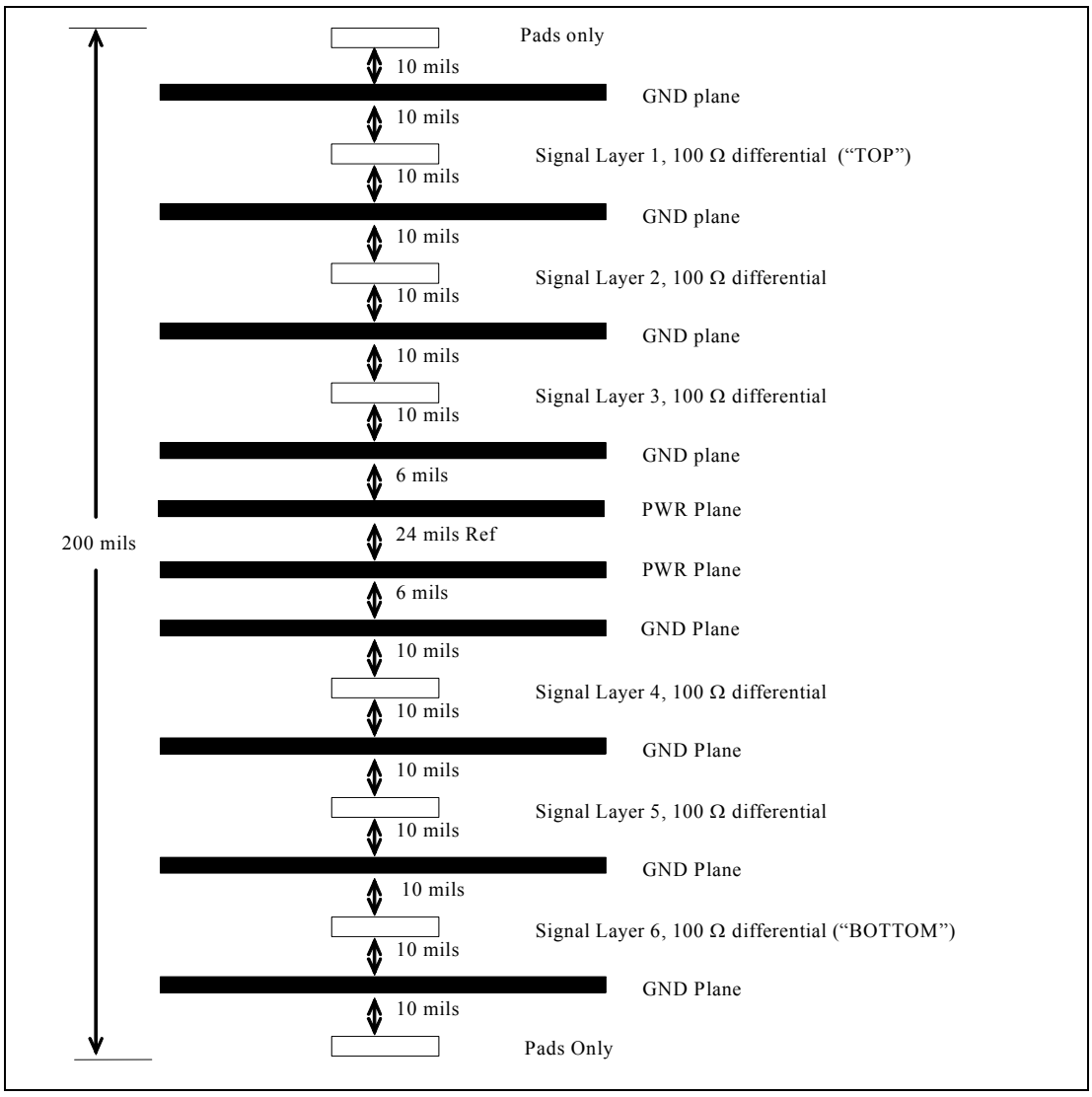


Figure 8 – Legacy HM-Zd Backplane Stackup

Backplanes based on the QuadRoute technique, introduced by Tyco Electronics three years ago, were also included. This technique increases signal routing efficiency per signal layer by permitting two differential pairs (4 traces) to be routed in between the signal columns of the Z-PACK HM-Zd connector. The trace widths used were based on a 4.75 mil nominal trace width. The increased routing density helps to reduce the number of signal layers needed. For example, using this technique a full mesh PICMG 3.0 ATCA backplane can be routed in 8 signal layers or a total of 20 layers.[iv] The reduction in layer count can then offset the cost of higher performing materials, and still provide an overall lower cost solution. Since the nominal overall thickness of the board has been reduced to 125 mils (3.175mm), the stub effects demonstrated in Figure 5 have been shifted to a higher frequency. To

explore the potential performance of this technique, the QuadRoute backplane design was fabricated in various materials, such as Nelco 4000-13, 4000-13SI, and 9000. No counterboring on the backplane vias has been done. The stackup is shown in Figure 9.

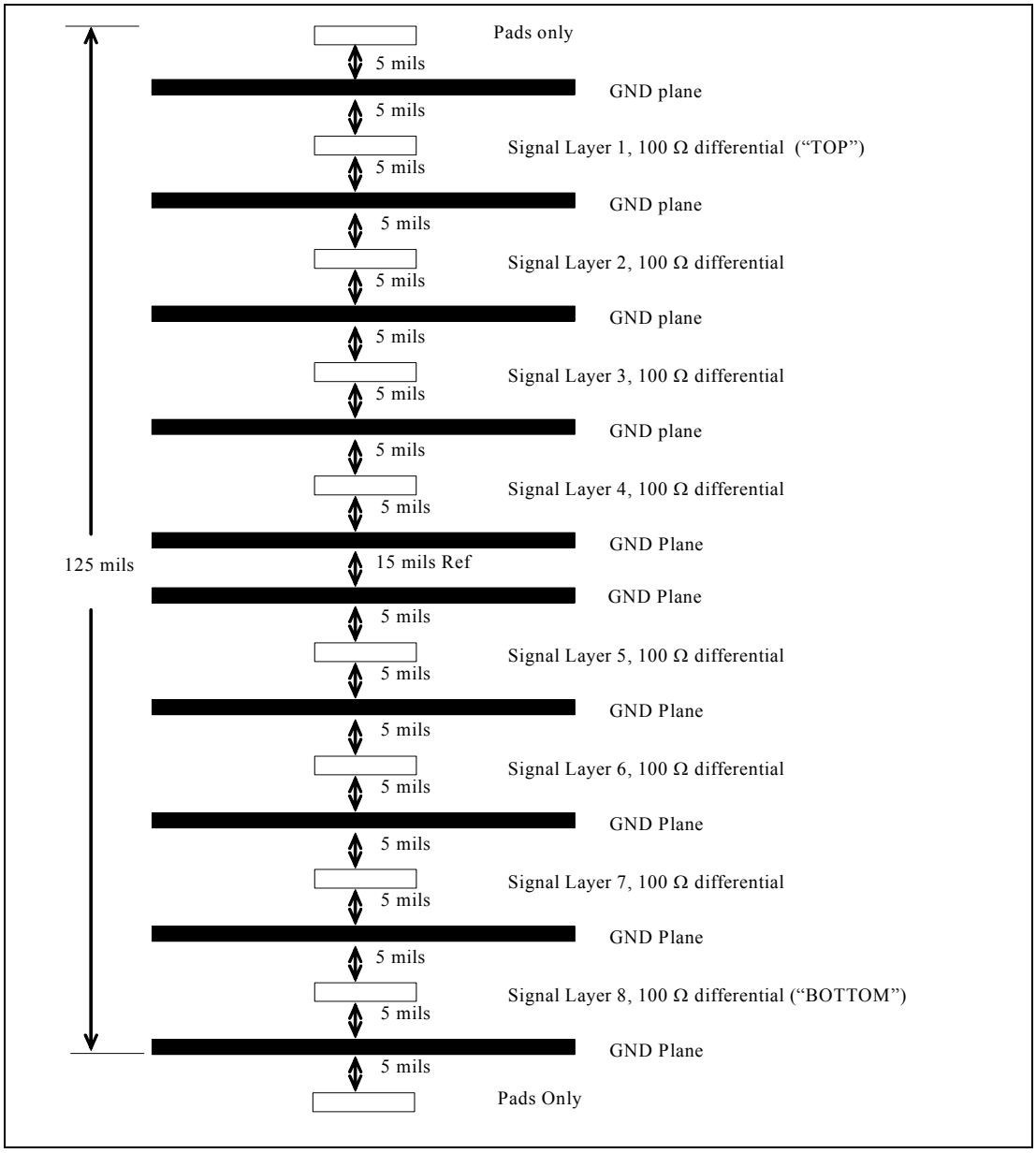


Figure 9 – QuadRoute HM-Zd Backplane Stackup

In addition to these backplanes, three identical sets of line cards, fabricated in Nelco 4000-6, 4000-13, and 4000-13SI were used. Within each set of cards trace lengths of 2.5" (63.5mm), 6" (152.4mm), and 10" (254mm) were included. All line cards were a nominal thickness of 92 mils (2.34mm). Stripline traces, based on 6 mil geometry, are routed throughout the entire line card. Counterboring was only used at the SMA connectors to improve the quality of the launch into the test fixture. In an attempt to minimize material variation, each set of line cards was fabricated on the same PCB panel.

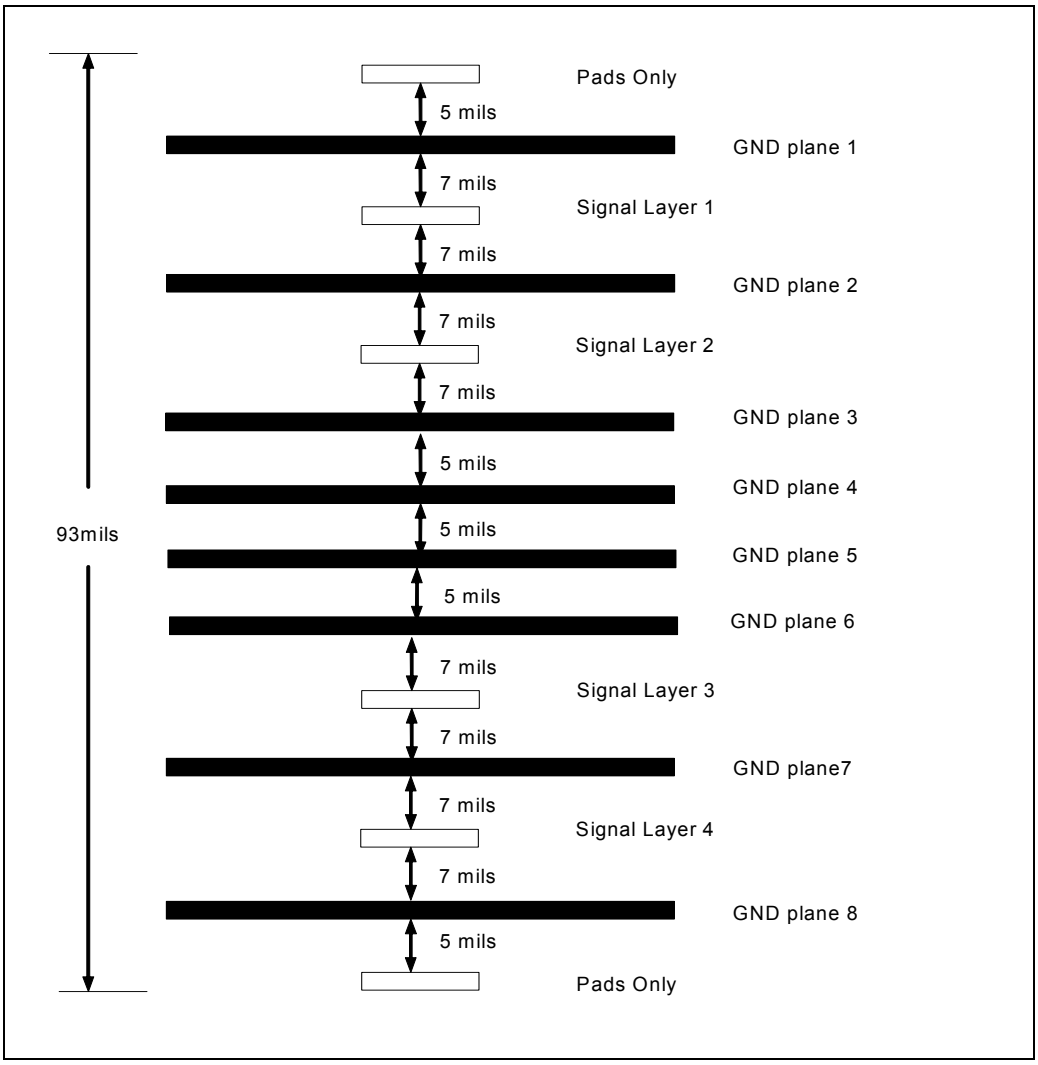


Figure 10 – Z-PACK HM-Zd Line Card Stackup

S-parameter characterization by an independent facility, the University of New Hampshire InterOperability Laboratory, was performed using the Agilent 8720ES with N4418A test set. Tyco Electronics would like to acknowledge and thank UNH-IOL for their support in assembling the test environment and completing the testing.

Pulse Response

The pulse response is a convenient way to observe the time-domain properties of the channel. It is a representation of the signal present at TP4 given that an isolated"1" symbol is input at TP1. Clearly, the signal at TP4 is a function of the signal input at TP1 and the channel between TP1 and TP4.

Therefore, it is important to describe the properties of the signal at TP1. A single pulse with unit amplitude and width equal to 1 symbol at the signaling rate of interest (e.g. approximately 97 ps at 10.3125 Gb/s) serves as the stimulus, s(t), for this study. The pulse exhibits a 10-90% rise time of 30 ps. For the first portion of the study, no transmitter waveshaping (such as pre-emphasis) is used, but this feature is introduced in later sections.

The pulse response of the channel can be derived directly from the measured SDD21 magnitude and phase. This process involves some pre-processing followed by the application of the inverse Fast Fourier Transform (IFFT). The exact process is left as an exercise to the reader.

The pulse response is typically sampled at the signaling rate and then decomposed into the cursor, which represents the amplitude of the pulse at the instant the receiver samples it, and inter-symbol interference (ISI). ISI represents the influence of preceding and following symbols on the amplitude observed at the sampling instant. It is further broken down into two categories – post-cursor ISI represents the influence of the previously detected symbols and pre-cursor ISI represents the influence of symbols yet to arrive. Note that the system is still causal, and notion of pre-cursor and post-cursor is a function of the placement of the sample point.

To this end, it is important to note the algorithm that is employed to determine the receiver sampling instant. While multiple possibilities exist, each representing actual timing recovery algorithms to various accuracy, this paper takes the simple approach of defining the sampling instant as the midpoint between the times that the pulse response crosses the 50% amplitude points.

This paper denotes the time-domain pulse response as t(n) where n = 0 represents the cursor or sampling instant. Value of n less than zero represent pre-cursor ISI and values greater than zero represent post-cursor ISI. At various points in the document, n may also be referred to as the sample index.

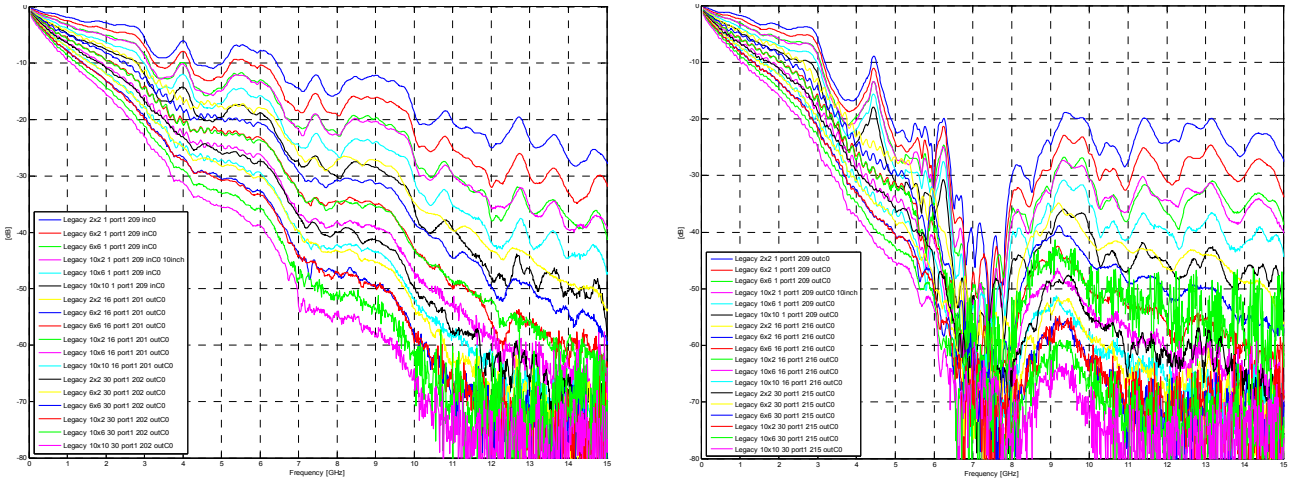
It should be noted that an ideal pulse response would have t(n) be zero for all n not equal to zero (i.e. no inter-symbol interference). In fact, the objective of equalization is to achieve this response, but the ability to do so is a function of the complexity of the equalizer and the nature of the channel itself. The extent to which this ideal result is approximated limits the BER performance of the interconnect. Therefore, the distribution of ISI in the pulse response provides very useful information about the channel.

The Legacy Backplane Environment

The first phase of this study was to look at a legacy environment in an attempt to understand the full extent of the impact of the stub effect on the backplane. Thus, the data selection was controlled by using a bottom layer connection on the daughtercard to the same signal pins (A/B) of the Z-PACK HM-Zd connector, and then looking at cases where the backplane connection was varied from top to bottom. While layer connections were held constant, daughtercard and backplane lengths were varied.

Figure 11 demonstrates the forward channel (SDD21) characterization of channels ranging from 6 inches to 50 inches. The figure on the left demonstrates all channels with a bottom layer connection on

the backplane, while the figure on the right demonstrates all of the channels with a top backplane layer connection.

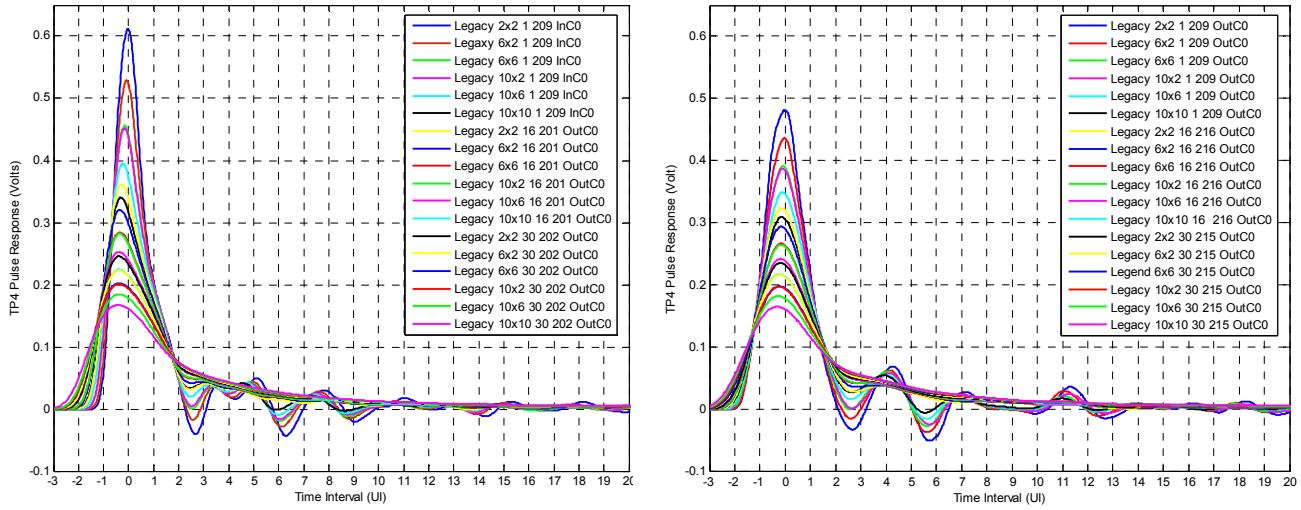


Bottom Layer Backplane Connection Top Layer Backplane Connection

Figure 11 - Legacy Backplane SDD21 Characterization

The general trends of these two graphs are probably not much of a surprise. Top layer connections exhibit deep nulls and in general more overall channel ripple. Also, shorter channels tend to exhibit more channel ripple than longer channels. From these simple magnitude-only plots, it is difficult to assess anything more than a general qualitative assessment. Without subsequent analysis it is also very difficult, if not impossible, to understand the task facing the receiver.

Figure 12 shows the same channels as Figure 11, except the channels are characterized via pulse responses. The figure on the left demonstrates all channels that had a bottom layer connection on the backplane, while the figure on the right demonstrates all of the channels with a top backplane layer connection.



Bottom Layer Top Layer

Figure 12 - Legacy Backplane 10.3 Gb/s Pulse Response

Several key observations can now be made regarding the impact of the backplane layer connection –

- The greater in magnitude the SDD21, the greater the t(0).
- Channels with stubs exhibit higher pre-cursor magnitude.
- There is greater variation in the pulse responses between top and bottom backplane layer connections for shorter channels than longer channels.
- Short backplane channels exhibit more "ripple" in the tail than longer backplane channels
- Longer channels have similar "tails" on the falling end, but the reduced amplitude of t(0) increases the impact of post-cursors.
- Channels of equivalent length can exhibit different behavior based on the spacing between line cards on the backplane.

Figure 13 focuses on the pre-cursors of the pulses shown in Figure 12. There is a noticeable difference in pre-cursor amplitude given the backplane layer connection. For the top layer on the Legacy Backplane the minimum pre-cursor at t(-1) is 0.142. It is important to notice, however, that this minimum value occurred for the longest channel (Legacy 10x10 30 215 OutC0), which subsequently had the highest pre-cursors at t(-3) and t(-2), 0.005 and 0.055 respectively. Note that the largest value of t(-1) in terms of absolute magnitude is actually the smallest value of t(-1) as a percentage of t(0). This is illustrated for top layer backplane connections in Figure 14.

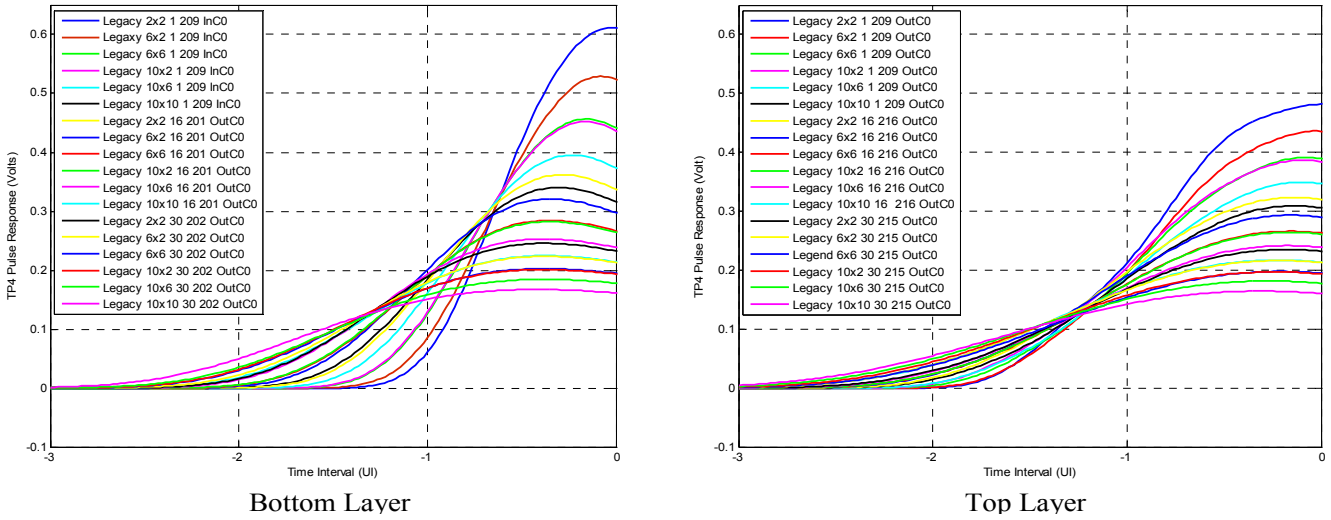


Figure 13 - Legacy Backplane 10.3 Gb/s Pre-Cursor Comparison

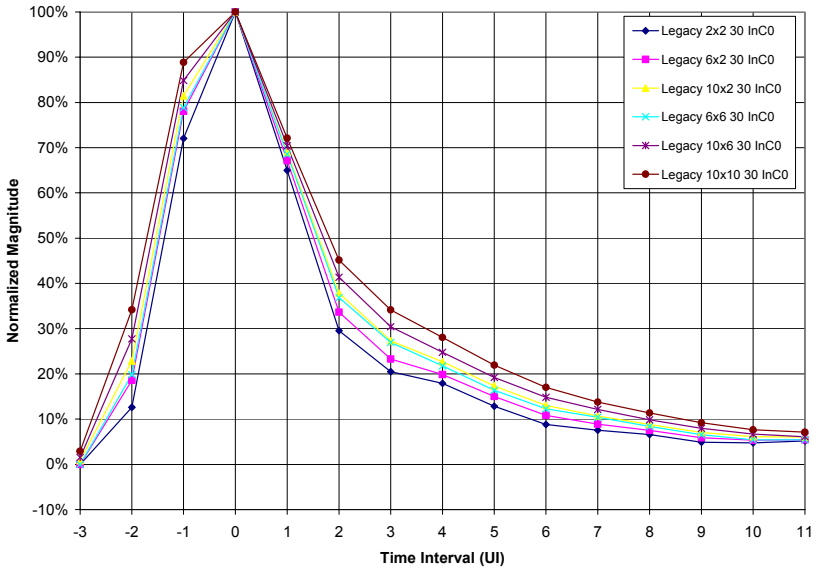
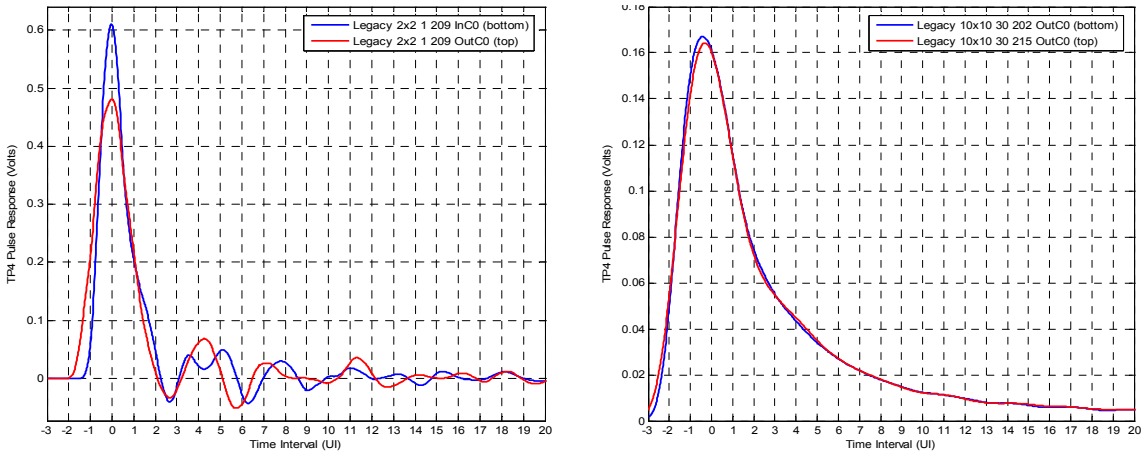


Figure 14 - Legacy Backplane 10.3 Gb/s, Top Layer Connections, Cursors Normalized to t(0)

Figure 15 illustrates the pulse responses for the shortest (5") and longest (50") channels. As already noted, the largest amount of variation caused by layer connection was observed for the 1" pitch (connector-to-connector trace length) backplane channels. With the subsequent increase in trace length, attenuation increased until the pulse responses were very similar regardless of layer connection effect. This is further explored in Figure 16, which shows the percent difference in normalized cursor value caused by layer connection effect. It is clear that as backplane length increases, the impact of stub effect on the pulse response lessens. Furthermore, the impact of stub effect is more readily seen in the pre-cursors, particularly t(-1), rather than the post-cursors.

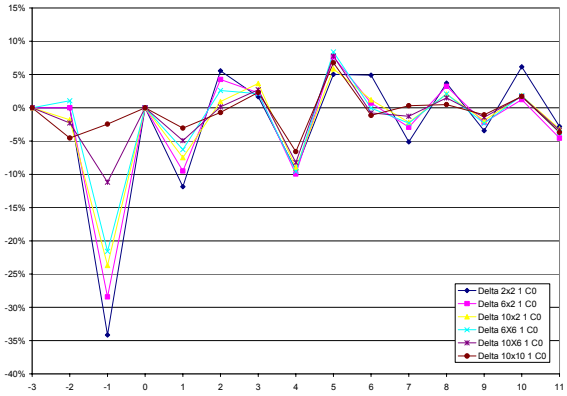


Short Channel (5" total) Long Channel (50" total)

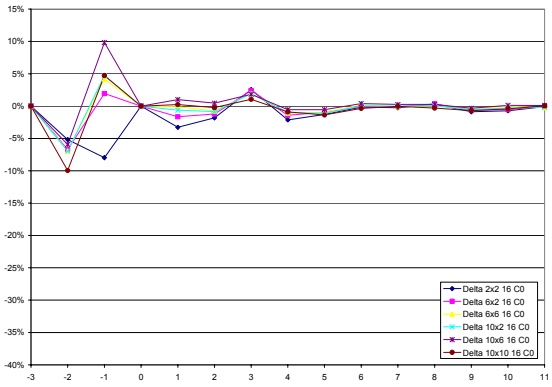
Figure 15 - Legacy Backplane 10.3 Gb/s Length Comparison

Figure 17 further highlights the impact of backplane length. Both channels have a total length of 21" and are based on backplane top layer connections. For "Legacy 10x10 1 Port1 209 OutC0" the line cards were 10" in length using a 1" backplane pitch, while for "Legacy 2x2 16 Port1 21 OutC0", the line cards were 2.5" in length using a 16" backplane pitch. Notice the general similarity in the SDD21 profile of the two channels with more "ripple" on the 1" backplane pitch channel. Conversely this

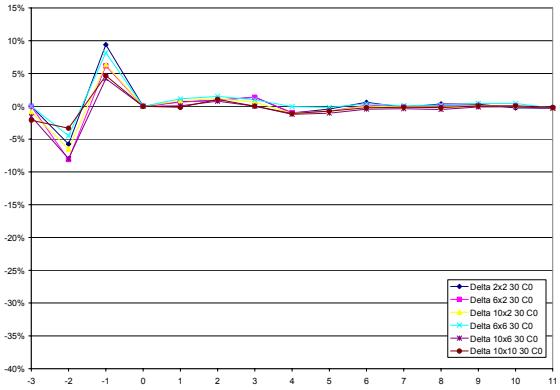
translates to the pulse responses shown in the same figure. There is a similarity between the pulse responses, but it can be seen that for the 1" backplane pitch there is a general rippling of the signal from t(3) to t(15) around the 16" backplane pitch channel pulse response.



1" Backplane Pitch



16" Backplane Pitch



30"Backplane Pitch

Figure 16 - Legacy Backplane 10.3 Gb/s Length Comparison

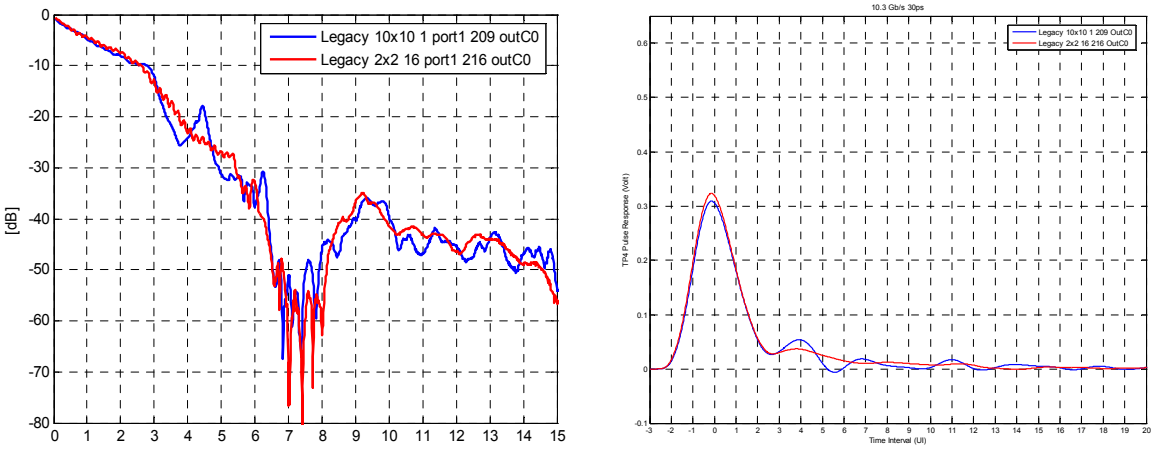
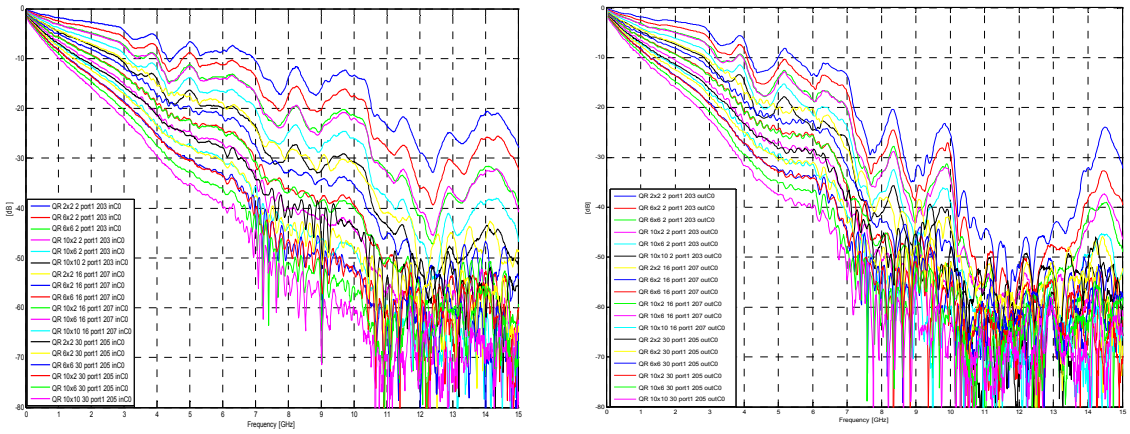


Figure 17 - Legacy Backplane 10.3 Gb/s, Comparison Between 21" Channels, Top Layer Backplane Connection

The QuadRoute Backplane Environment

The QuadRoute technique, introduced by Tyco Electronics three years ago, increases the signal routing efficiency per signal layer, which helps to reduce the overall thickness of the board. Channels based on ATCA backplanes that implemented this technique have been under the scrutiny of the IEEE P802.3ap Backplane Ethernet Task Force[v], and have been shown via comprehensive simulations to support operation at 10.3125 Gb/s. To better understand the impact that this technique has on backplane channel performance, the analysis employed in the previous section has been repeated.

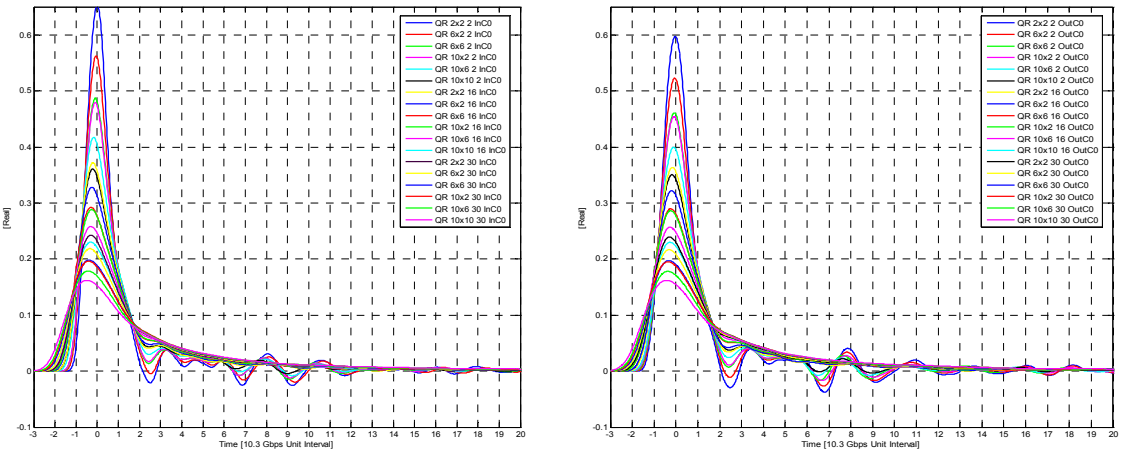


Bottom Layer Top Layer

Figure 18 - QuadRoute Backplane SDD21 Characterization

The general trends of these two graphs are similar to what was shown previously with the Legacy Backplane. Top layer connections exhibit deep nulls and in general more overall channel ripple. However, in comparison to the Legacy backplane, the nulls have been pushed upward to higher frequencies. Furthermore, it is clear that there is less channel ripple in all of the channels presented, as well as a more predictable loss.

Figure 19 features the same channels shown in Figure 18, except the channels are represented using pulse responses. The figure on the left shows all channels that had a bottom layer connection on the backplane, while the figure on the right shows all of the channels with a top backplane layer connection.

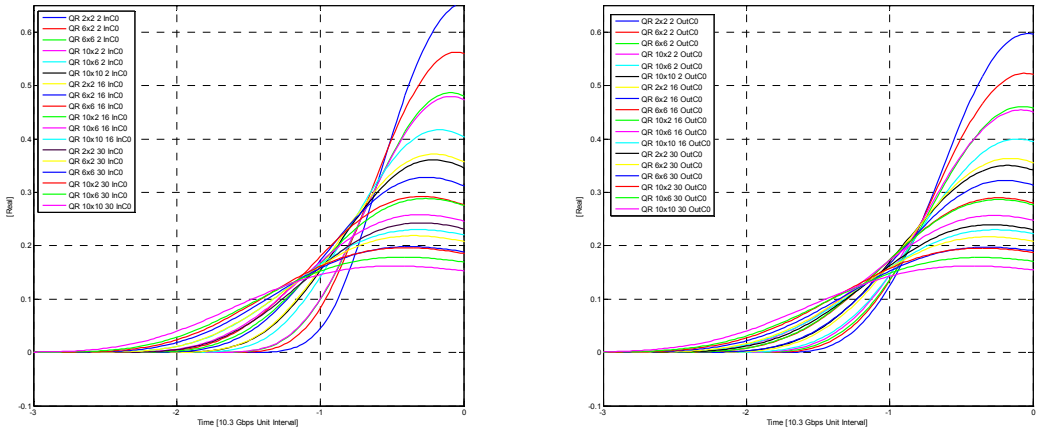


Bottom Layer Top Layer

Figure 19 - QuadRoute Backplane 10.3 Gb/s Pulse Response

There are some very significant differences between the pulse response characterizations of the two backplanes. There is minimal difference in the pulse responses due to layer connection. Therefore, for the shorter channels, the t(0) value for the top layer connections has increased. Furthermore, the shorter channels on the QuadRoute backplane do not have as much ripple in the tail that the Legacy Backplane exhibited.

Figure 20 focuses on the pre-cursors of the pulses shown in Figure 19. It is clear that the stub for the QuadRoute backplane is not having the same amount of impact as the stub of the Legacy Backplane. For the QuadRoute Backplane the amount of pre-cursor contribution at t(-1) has not been increased for the shorter channels as it was for the Legacy Backplane. If Figure 13 and Figure 20 are compared, it is clear that the stub on the Legacy Backplane contributed to a greater broadening of the pulse, resulting in energy shifting to earlier bits and impacting the pulse response magnitude at t(-1) and t(-2).

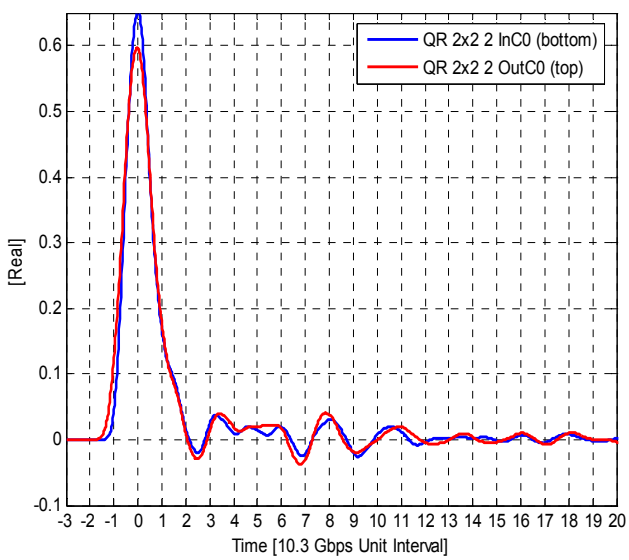


Bottom Layer Top Layer

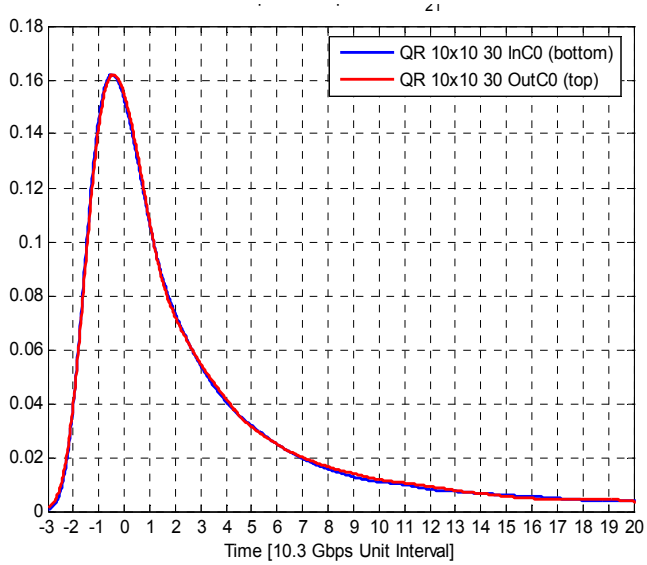
Figure 20 - QuadRoute Backplane 10.3 Gb/s Pre-Cursor Comparison

Figure 2121 illustrates the pulse responses for the shortest (6") and longest (50") channels. Notice that there is minimal difference due to layer connection for either plot, which is quite different than what was observed with the Legacy Backplane.

While the largest amount of variation caused by layer connection was observed for the 2" pitch backplane channels, there was significantly less deviation than what was observed with the Legacy backplane. With the subsequent increase in trace length, attenuation increased until the pulse responses were very similar regardless of layer connection effect. This is further explored in Figure 22, which shows the percent difference in the normalized pulse response amplitude caused by layer connection effect. It is clear that as backplane length increases, the impact of stub effect on the pulse response lessens. It should be pointed out that this assumes ideal terminations, and no subsequent multi-path reflections. Furthermore, the impact of stub effect is more readily seen in the pre-cursor amplitude, particularly t(-1), rather than the post-cursor amplitude.

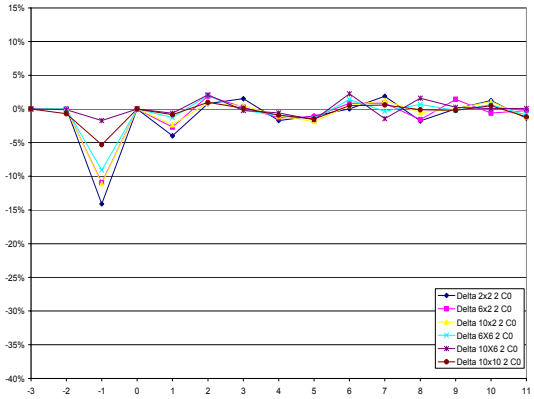


Short Channel (6 Inches Total)

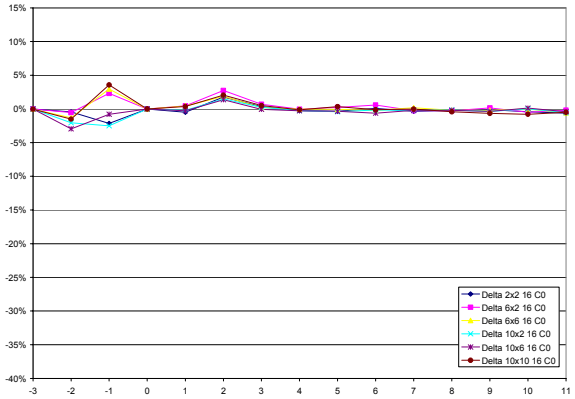


Long Channel (50 Inches Total)

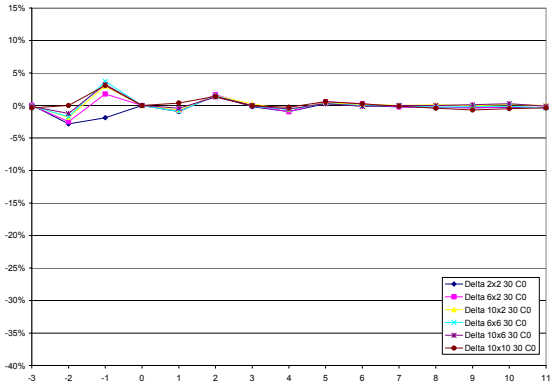
Figure 21 - QuadRoute Backplane 10.3 Gb/s Length Comparison



2” Backplane Pitch



16” Backplane Pitch



30” Backplane Pitch

Figure 22 - QuadRoute Backplane 10.3 Gb/s Length Comparison

Figure 2323 revisits the impact of the backplane topology. Both channels are based on backplane top layer connections. For "QR 10x10 2 Port1 203 OutC0" the line cards were 10" in length using a 2" backplane pitch, while for "QR 2x2 16 Port1 207 OutC0", the line cards were 2.5" in length using a 16" backplane pitch. Notice the general similarity in the SDD21 profile of the two channels with more "ripple" on the 2" backplane pitch channel. Conversely this translates to the pulse responses shown in the same figure. Once again note the general similarity of the pulse responses, but also notice that for the 2" backplane pitch, the overall ripple from t(3) to t(15) around the 16" backplane pitch channel pulse response. It should be noted that this difference is not as significant as the Legacy Backplane comparison demonstrated in Figure 17.

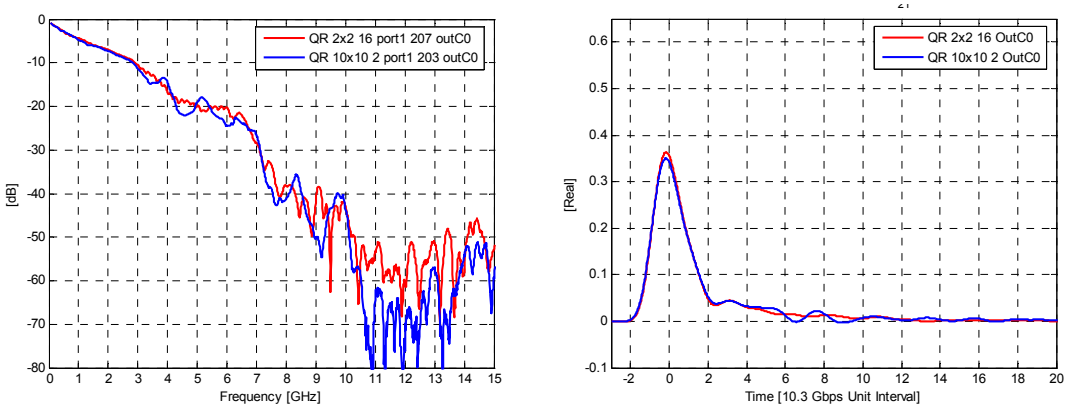


Figure 23 - QuadRoute Backplane 10.3 Gb/s Length Topology Comparison, Top Layer Backplane Connection

The Challenges the Channel Presents

The focus of the paper is on understanding the challenges that a pulse delivered through a channel presents to the receiver. Figure 24 has been discussed as the system interconnect, but it should also be realized that this figure represents the solution space. The road to serial 10 Gb/s across a backplane is one where there is a shared burden between the transmitter, channel, and receiver. Understanding this and the interaction between these aspects will provide the system designer with the knowledge to design the best overall system.

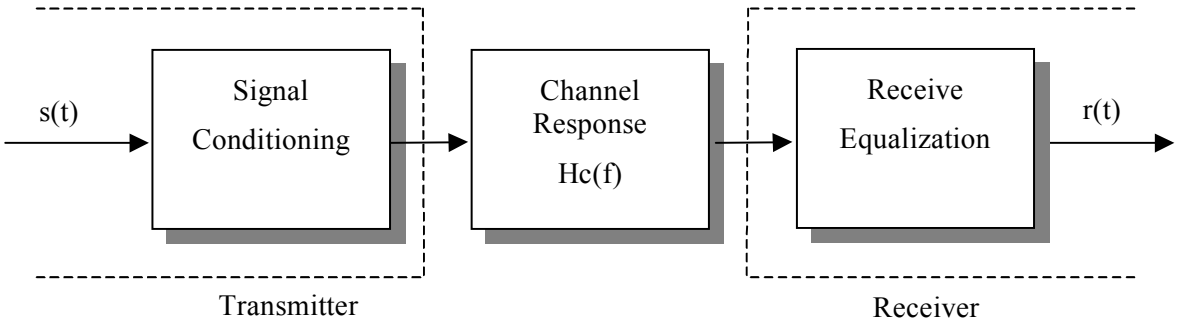


Figure 24 – The Solution Space

At this point two backplane systems with 6 different combinations of line cards have had various forward channels characterized in frequency domain via S-parameters and in the time domain via pulse responses. It is important that both time and frequency domain be used to analyze the available data in order to understand the phenomenon that is being addressed.

The frequency domain results provided here are similar to what has been presented over the past few years in the industry -

- Short total system lengths tend to have some ripple in them, which can then be magnified by stub effects.
- Channels similar in length but different in their overall topology design can exhibit similar loss characteristics, but with different ripple behavior.
- As system lengths increase, there is an increased loss, resulting in a lower SDD21.
- A 200 mil thick backplane based system will exhibit variation in transmission response between the layer connection extremes with top layer backplane connection channels exhibiting deep notches. The 125 mil thick backplane based system also exhibited this variation, but starting at much higher frequencies.

From the time domain pulse responses, additional observations above can be made -

- The 1" and 2" pitch backplane connections, which exhibited a lot of ripple in frequency domain, also exhibited a lot of ripple in their pulse responses. Stub effects exasperated the amount of ripple (both in magnitude and duration). The ripple existed even for very long line cards with these backplane channels, though the ripples were partially attenuated in magnitude due to the additional loss.
- Channels with similar frequency domain loss characteristics but different ripple characteristics exhibited pulse responses that were similar in general shape and magnitude, but with different ripple profiles in the tail.

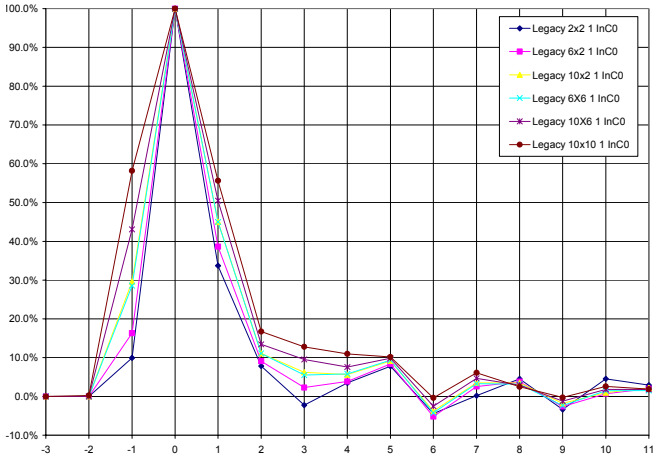
In channels with a bottom layer connection on the backplane, there are some general trends (see Figure 25) -

- As length increases, t(0) decreases.
- It was noted that the difference in the frequency-domain ripple for the short Legacy and QuadRoute channels corresponded to a higher t(0) value and less post-cursor ripple for the QuadRoute backplane.
- As attenuation grew the pulse width broadened, spreading into t(-2) and t(-1). As t(-2) grew in value, t(-1) began to decrease.
- For the longer backplane channels, which did not suffer from the multi-path reflections that were present in the 1" and 2" pitch backplane connections, the falling tails were in general very similar in terms of magnitude.
- When normalizing the magnitudes against t(0), which decreased in value with length, the influence of the pre and post cursors grew as system length increased.
- Comparing the Legacy Backplane against the QuadRoute backplane –
    - In general there was less dispersion on the rising edge of the pulse for the QuadRoute backplane than for the Legacy Backplane.
    - In general for the longer backplane channels, the falling tails all were very similar. The increase in length, however, decreased the amplitude of t(0), thus increasing the impact of the post-cursor inter-symbol interference on a percent basis.

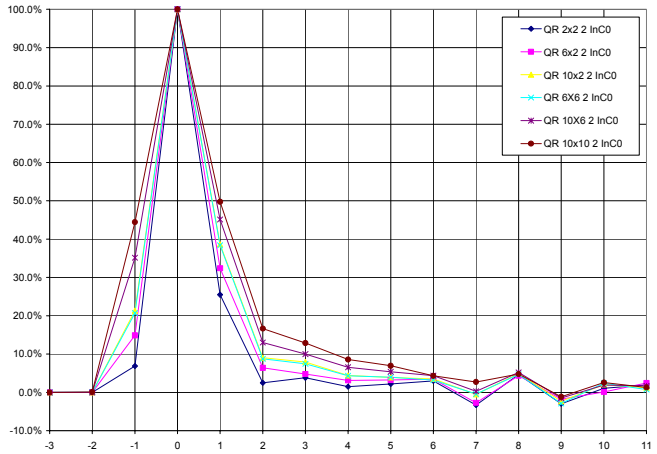
In channels with a top layer connection on the backplane, there are some general trends (see Figure 26) -

- As length increases, t(0) decreases.
- Pre-cursor amplitude was much higher for top layer connections. The longer stub associated with the Legacy Backplane created the highest pre-cursor amplitude. For the Legacy Backplane, the minimum pre-cursor amplitude at t(-1) was 44%, and this was for a 6" channel.

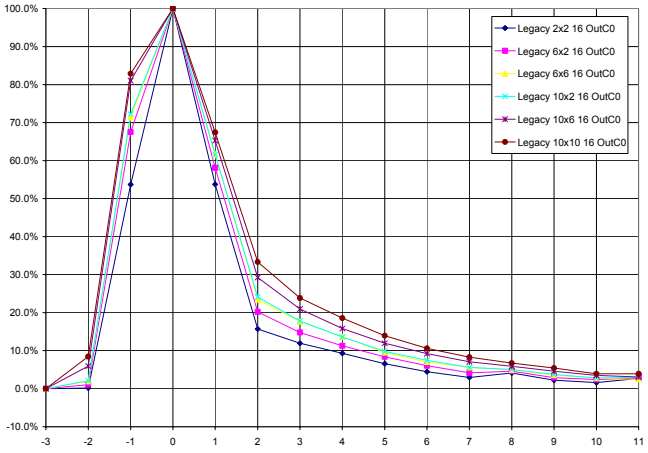
- The QuadRoute inter-symbol interference, both pre-cursor and post-cursor, was less than the Legacy inter-symbol interference to a varying degree. In general the greatest differences were seen at t(-2), t(-1), and t(1). Beyond t(1) the inter-symbol interference from the QuadRoute channels were slightly less than the Legacy channels.
- In looking at the longest channels, it can be observed that the QuadRoute Backplane has higher t(-1) values than the Legacy Backplane. While this is true, it must be realized that the Legacy Backplane channels experienced more pulse broadening, and had energy spread into t(-2) that was less than what was seen for the QuadRoute backplane.
- The ripple in the tail for the QuadRoute 2" backplane pitch was significantly less than what was observed for the Legacy 1" backplane pitch.



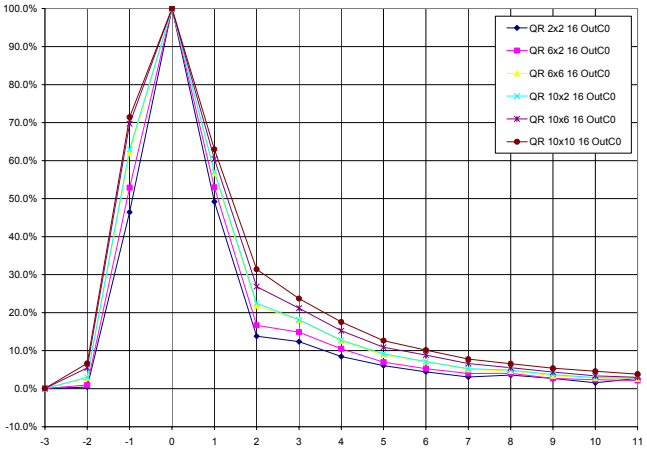
Legacy 1” Backplane, Bottom Layer



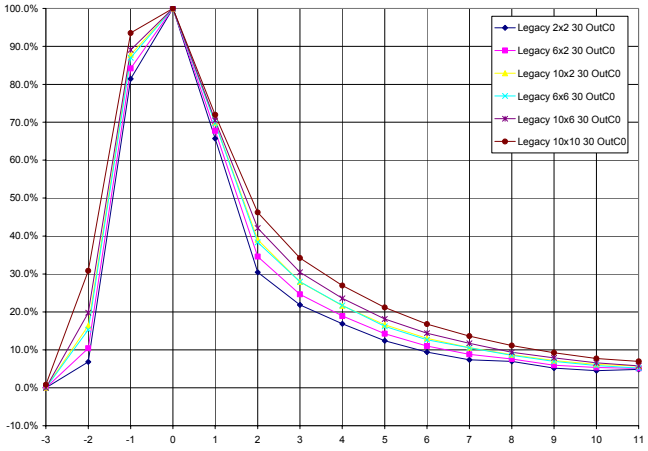
QuadRoute 2” Backplane, Bottom Layer



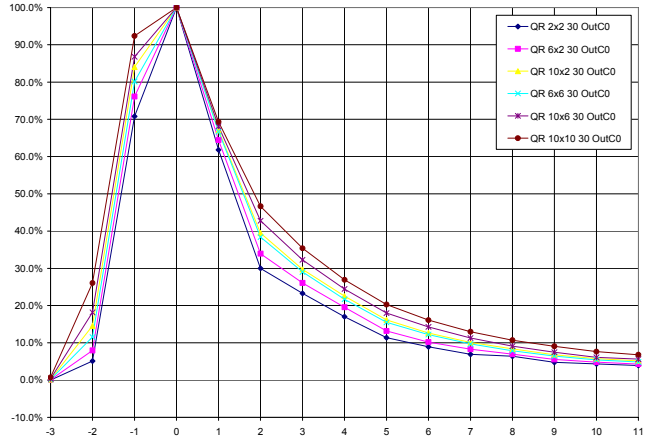
Legacy 16” Backplane, Bottom Layer



QuadRoute 16” Backplane, Bottom Layer

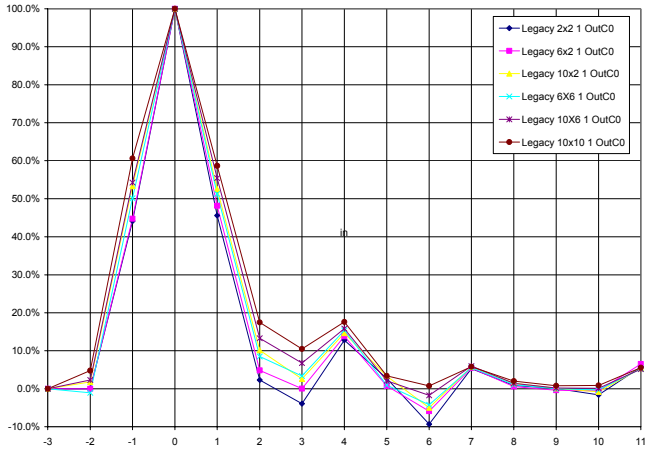


Legacy 30” Backplane, Bottom Layer

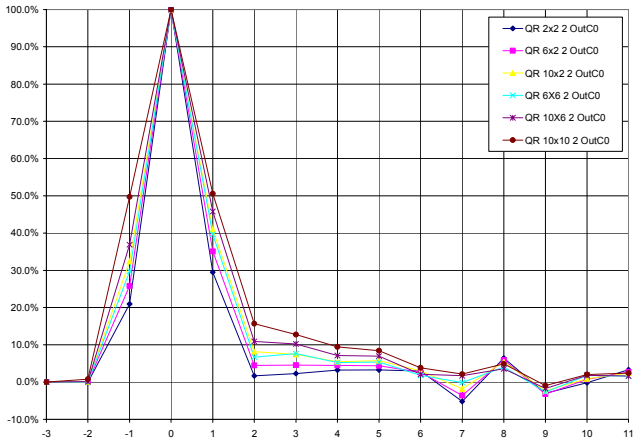


QuadRoute 30” Backplane, Bottom Layer

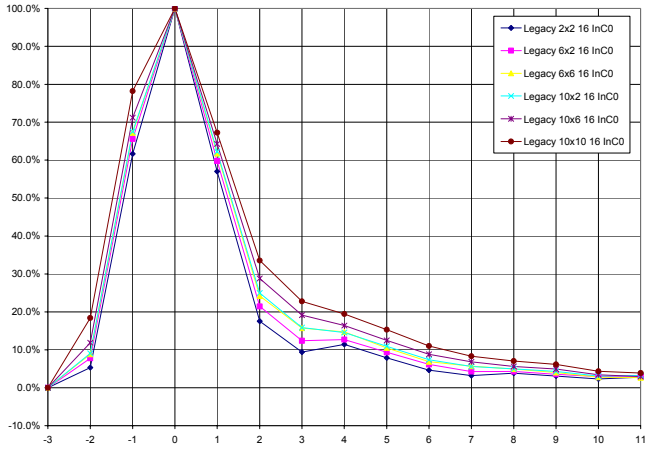
Figure 25 - Pulse Response Summary, Bottom Layer Connection



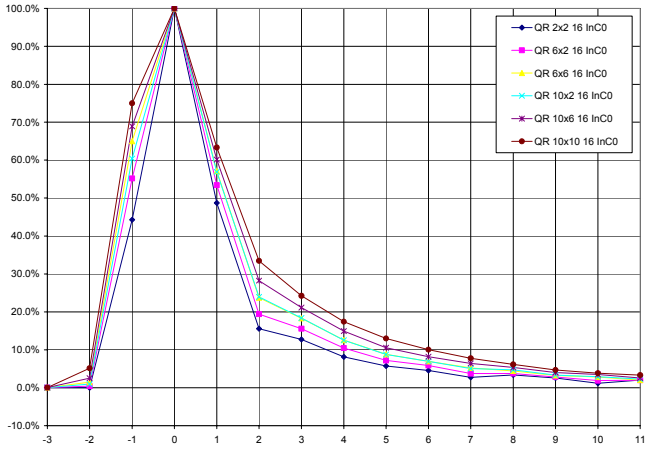
Legacy 1” Backplane, Top Layer



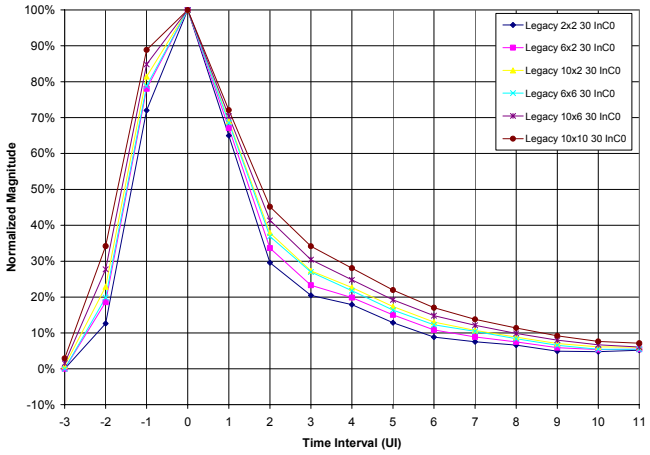
QuadRoute 2” Backplane, Top Layer



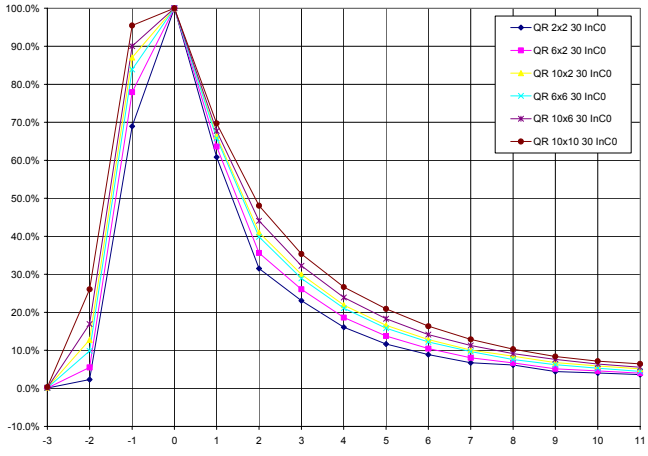
Legacy 16” Backplane, Top Layer



QuadRoute 16” Backplane, Top Layer



Legacy 30” Backplane, Top Layer



QuadRoute 30” Backplane, Top Layer

Figure 26 - Pulse Response Summary, Top Layer Connection

Sharing the Burden

The road to 10 Gb/s serial transmission across a backplane is one where there is a shared burden between the transmitter, channel, and receiver. Decision feedback equalization (DFE) in the receiver is currently getting a great deal of attention from the industry. A DFE estimates the post-cursor ISI contribution from previously detected symbols and then removes their contributions from the current symbol prior to detection. In general, there can be ”N” taps in a DFE which would effectively remove the contributions of the first N post-cursors. A 5 tap DFE receiver is typically assumed for 10 Gb/s serial applications. Inter-symbol interference outside of the 5 symbol window will continue to contribute to performance degradation. Therefore, additional improvements in what is delivered to the receiver must be pursued.

As discussed earlier, what is presented to the receiver is the product of the input into the channel and the channel itself. When the transmitter includes equalization (e.g. pre-emphasis), the shape of the channel will influence the spectral distribution of the signal launched into it. For the Legacy Backplane channels discussed, there is a significant difference in the transmission response between the top and bottom layer connections. Furthermore, the top layer connections examined experienced nulls that start at approximately 3 GHz, which is well below the Nyquist frequency of 5 GHz for 10 Gb/s non-return to zero (NRZ) signal. It will be shown that, in these extreme cases, the channel shape can limits the effectiveness of transmitter waveshaping.

To examine this phenomenon, three channels were chosen from the Legacy Backplane. All channels were 21” in total length. Two of the channels consisted of 2.5” line cards with a 16” backplane, and had either a top or bottom layer connection on the backplane. The third test channel was based on 10” line cards with a 1” backplane length, and a top layer connection on the backplane was chosen. The SDD21 profiles of the three channels are shown in Figure 27.

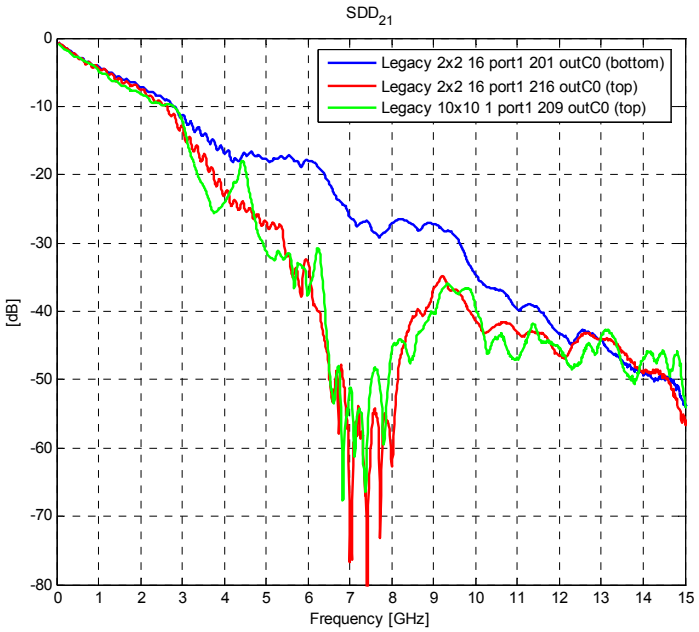


Figure 27 - Test Channels From Legacy Backplane

It was decided to test these three channels with simple pre-emphasis as a way to evaluate the impact of the channel on the efficiency of signal conditioning. Six pre-emphasis levels were chosen (8%, 18%,

29%, 43%, 60%, and 82%) and applied to the three channels. Figure 28 provides summary graphs of the results for the three channels.

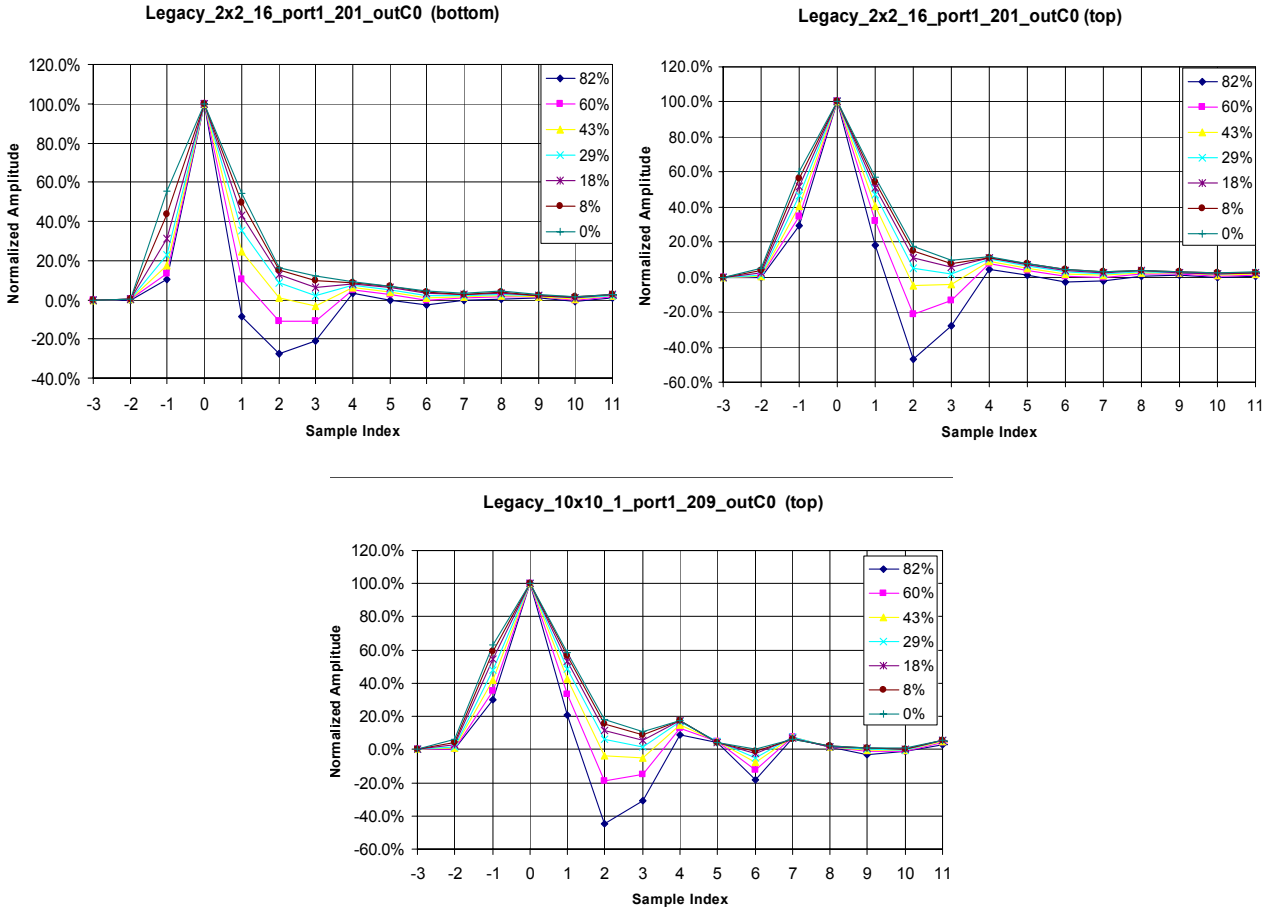


Figure 28 - Summary of Pulse Responses Employing Pre-Emphasis

It is obvious from these charts that pre-emphasis is having an effect, but not necessarily the desired effect. First, let's observe what impact pre-emphasis has had on the pulse responses. It can be seen that the use of pre-emphasis was able to reduce the first pre-cursor (t-1) on all three graphs. However, note that the greatest reduction in pre-cursor contribution was for the channel that had a bottom layer connection, lending credibility to the thought that the channel does influence the effectiveness of the transmit wave shaping. Furthermore, for the bottom layer connection incremental changes in pre-emphasis levels led to incremental changes in t(-1) amplitude. For the top layer connection, 43% pre-emphasis levels and greater caused the greatest impact on t(-1), but for the two top layer connections examined, there is still a fair amount of ISI (approximately 30%) at t(-1). It must also be pointed out that at these pre-emphasis levels, ripple in the tail began to increase. For the 1 inch backplane pitch with 10 inch line cards, the ripple in the channel needs consideration. Applying maximum pre-emphasis has increased the rippling from t(6) and beyond. For a channel response with ripple like this, it is easy to understand why the eye would be closed.

Conclusions

The ultimate goal of this paper was to quantify signal integrity issues that must be overcome in order to successfully run 10 Gb/s over a backplane. This has been accomplished by looking at various channels, in particular legacy style channels which are typically assumed to not support 10 Gb/s, not only in the frequency domain but also in the time domain. This should not be seen as an endorsement of the use of time domain over frequency domain analysis techniques. This paper has actually showed the opposite, that the use of both viewpoints can help the designer with qualitative and quantitative data that can be used to solve the overall system interconnect problem in a more timely fashion. There are things that can be easily seen in one domain that are not obvious in the other.

Today, a large portion of the industry is still hesitant to employ stub-removal techniques. This paper, based on the assumptions made, has demonstrated some of the issues with stub-limited channels for 10 Gb/s operation. In the frequency domain it is easy to see the difference in channel transmission responses, and hence, understand that ability of the transmitter to compensate for channel behavior will be dependent on the channel itself. The stubs introduce complex channel responses that can make it difficult to synthesize inverse filters that completely cancel the impairments. It was shown that while a reduction in pre-cursor magnitude may be realized, it may come at the cost of significantly enhancing post-cursor ISI.

Channel design can help alleviate this issue. The Tyco Electronics QuadRoute Backplane has demonstrated superior frequency and pulse response behavior in comparison to legacy environments without resorting to counterboring. While it is easy to understand how reducing the board thickness helped, it must be realized that this is a superficial explanation of what is actually happening. The technique is based on the use of narrow traces, which is counter to the current thinking of industry. The focus on transmission magnitude without concern for the overall quality of the transmission response is a one-dimensional approach to the problem being addressed.

It must also be pointed out that this paper has focused on one aspect of the overall system interconnect in order to understand its role in system performance. Looking beyond the IEEE P802.3ap TP1 – TP4 test points is crucial to the overall success of the system design. DC blocking caps and their associated vias, device packaging, ESD structures, and device terminations all play a role in altering quality of the signal delivered to the receiver. In addition, crosstalk will play a key role, and the reader should realize that at these speeds both near-end crosstalk (NEXT) and far-end crosstalk (FEXT) can be significant performance impairments. FEXT may become more problematic with improvements to the transmission response. This also implies that FEXT changes from channel to channel depending on that channel's overall length. The reader is encouraged to look at the problem from a system level perspective. As pointed out earlier, Figure 24 may be viewed as the system interconnect, but it also represents the solution space.

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[i] "Channel Compliance Testing Utilizing Novel Statistical Eye Methodology," Sanders, Resso, D'Ambrosia, DesignCon 2004 Proceedings.

[ii] "Investigating Microvia Technology for 10 Gb/s and Higher Telecommunication Systems," Resso, Modinger, Roe, and Gneiting, DesignCon 2005 Proceedings.

[iii] IEEE 802.3ap Backplane Ethernet Specification, Draft 1.0

[iv] "Channel Comparisons to Proposed Channel Model," D'Ambrosia, http://grouper.ieee.org/groups/802/3/ap/public/may04/dambrosia_02_0504.pdf

[v] "Channels for Consideration by the Signaling Ad Hoc," D'Ambrosia, Healey, http://grouper.ieee.org/groups/802/3/ap/public/sep04/dambrosia_01_0904.pdf