

# CMOS 18-Stage Static Shift Register

High-Voltage Types (20-Volt Rating)

■ CD4006B types are composed of 4 separate shift register sections: two sections of four stages and two sections of five stages with an output tap at the fourth stage. Each section has an independent single-rail data path.

A common clock signal is used for all stages. Data are shifted to the next stage on negative-going transitions of the clock. Through appropriate connections of inputs and outputs, multiple register sections of 4, 5, 8, and 9 stages or single register sections of 10, 12, 13, 14, 16, 17 and 18 stages can be implemented using one CD4006B package. Longer shift register sections can be assembled by using more than one CD4006B.

To facilitate cascading stages when clock rise and fall times are slow, an optional output ( $D_1+4'$ ) that is delayed one-half clock-cycle, is provided (see Truth Table for Output from Term. 2).

The CD4006B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

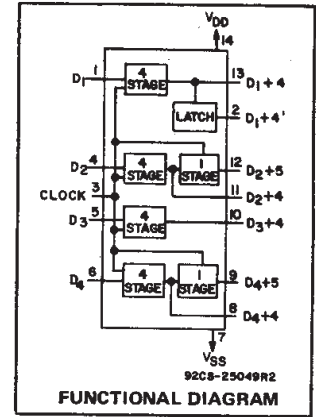
# CD4006B Types

### Features:

- Fully static operation
- Shifting rates up to 12 MHz @ 10 V (typ.)
- Permanent register storage with clock line high or low — no information recirculation required
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1  $\mu$ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) =
  - 1 V at  $V_{DD} = 5$  V
  - 2 V at  $V_{DD} = 10$  V
  - 2.5 V at  $V_{DD} = 15$  V
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

### Applications:

- Serial shift registers
- Frequency division
- Time delay circuits



TRUTH TABLE FOR SHIFT REGISTER STAGE

| D | CL <sup>▲</sup> | D + 1 |
|---|-----------------|-------|
| 0 |                 | 0     |
| 1 |                 | 1     |
| X |                 | NC    |

TRUTH TABLE FOR OUTPUT FROM TERM.2

| $D_1+4$ | CL <sup>▲</sup> | $D_1+4'$ |
|---------|-----------------|----------|
| 0       |                 | 0        |
| 1       |                 | 1        |
| X       |                 | NC       |

1 = HIGH      X = DON'T CARE  
 0 = LOW      ▲ = LEVEL CHANGE  
 NC = NO CHANGE

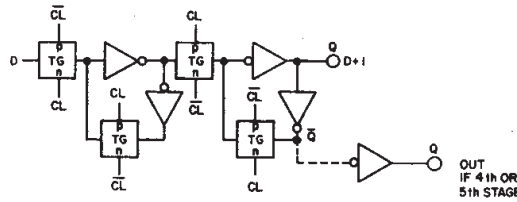
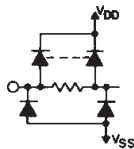
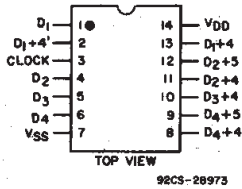


Fig. 1 - Logic diagram and truth table (one register stage).

### TERMINAL ASSIGNMENT



ALL INPUTS (TERMINALS 1,3,4,5,6)  
PROTECTED BY CMOS PROTECTION NETWORK

92CS-28974

RECOMMENDED OPERATING CONDITIONS at  $T_A = 25^\circ\text{C}$ , Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC  | $V_{DD}$<br>(V) | LIMITS |      | UNITS   |
|---|-----------------|--------|------|---------|
|   |                 | Min.   | Max. |         |
| Supply-Voltage Range (For $T_A =$ Full Package Temperature Range) | —               | 3      | 18   | V       |
| Clock Pulse Width, $t_{W}$  | 5               | 180    | —    | ns      |
|   | 10              | 80     | —    |         |
|   | 15              | 50     | —    |         |
| Data Setup Time, $t_S$  | 5               | 100    | —    | ns      |
|   | 10              | 50     | —    |         |
|   | 15              | 40     | —    |         |
| Data Hold Time, $t_H$   | 5               | 60     | —    | ns      |
|   | 10              | 40     | —    |         |
|   | 15              | 30     | —    |         |
| Clock Rise or Fall Time: $t_r, t_f$                               | 5, 10, 15       | —      | 15   | $\mu$ S |
| Clock Input Frequency, $f_{CL}$                                   | 5               | —      | 2.5  | MHz     |
|   | 10              | —      | 5    |         |
|   | 15              | —      | 7    |         |

# CD4006B Types

## MAXIMUM RATINGS, Absolute-Maximum Values:

|   |                                     |
|---|-------------------------------------|
| DC SUPPLY-VOLTAGE RANGE, (V <sub>DD</sub> )                             | -0.5V to +20V                       |
| Voltages referenced to V <sub>SS</sub> Terminal                         |                                     |
| INPUT VOLTAGE RANGE, ALL INPUTS   | -0.5V to V <sub>DD</sub> +0.5V      |
| DC INPUT CURRENT, ANY ONE INPUT   | ±10mA                               |
| POWER DISSIPATION PER PACKAGE (P <sub>D</sub> ):                        |                                     |
| For T <sub>A</sub> = -55°C to +100°C                                    | 500mW                               |
| For T <sub>A</sub> = +100°C to +125°C                                   | Derate Linearly at 12mW/°C to 200mW |
| DEVICE DISSIPATION PER OUTPUT TRANSISTOR                                |                                     |
| FOR T <sub>A</sub> = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) | 100mW                               |
| OPERATING-TEMPERATURE RANGE (T <sub>A</sub> )                           | -55°C to +125°C                     |
| STORAGE TEMPERATURE RANGE (T <sub>stg</sub> )                           | -65°C to +150°C                     |
| LEAD TEMPERATURE (DURING SOLDERING):                                    |                                     |
| At distance 1/16 ± 1/32 Inch (1.59 ± 0.79mm) from case for 10s max      | +265°C                              |

## STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC                                     | CONDITIONS         |                     |                     | LIMITS AT INDICATED TEMPERATURES (°C) |       |       |       |       |                   |      | UNITS |
|--|--------------------|---------------------|---------------------|---------------------------------------|-------|-------|-------|-------|-------------------|------|-------|
|  | V <sub>O</sub> (V) | V <sub>IN</sub> (V) | V <sub>DD</sub> (V) | -55                                   | -40   | +85   | +125  | +25   |                   |      |       |
|  |                    |                     |                     |                                       |       |       |       | Min.  | Typ.              | Max. |       |
| Quiescent Device Current, I <sub>DD</sub> Max.     | -                  | 0.5                 | 5                   | 5                                     | 5     | 150   | 150   | -     | 0.04              | 5    | μA    |
|  | -                  | 0.10                | 10                  | 10                                    | 10    | 300   | 300   | -     | 0.04              | 10   |       |
|  | -                  | 0.15                | 15                  | 20                                    | 20    | 600   | 600   | -     | 0.04              | 20   |       |
|  | -                  | 0.20                | 20                  | 100                                   | 100   | 3000  | 3000  | -     | 0.08              | 100  |       |
| Output Low (Sink) Current I <sub>OL</sub> Min.     | 0.4                | 0.5                 | 5                   | 0.64                                  | 0.61  | 0.42  | 0.36  | 0.51  | 1                 | -    | mA    |
|  | 0.5                | 0.10                | 10                  | 1.6                                   | 1.5   | 1.1   | 0.9   | 1.3   | 2.6               | -    |       |
|  | 1.5                | 0.15                | 15                  | 4.2                                   | 4     | 2.8   | 2.4   | 3.4   | 6.8               | -    |       |
| Output High (Source) Current, I <sub>OH</sub> Min. | 4.6                | 0.5                 | 5                   | -0.64                                 | -0.61 | -0.42 | -0.36 | -0.51 | -1                | -    | mA    |
|  | 2.5                | 0.5                 | 5                   | -2                                    | -1.8  | -1.3  | -1.15 | -1.6  | -3.2              | -    |       |
|  | 9.5                | 0.10                | 10                  | -1.6                                  | -1.5  | -1.1  | -0.9  | -1.3  | -2.6              | -    |       |
|  | 13.5               | 0.15                | 15                  | -4.2                                  | -4    | -2.8  | -2.4  | -3.4  | -6.8              | -    |       |
| Output Voltage: Low-Level, V <sub>OL</sub> Max.    | -                  | 0.5                 | 5                   | 0.05                                  |       |       | -     | 0     | 0.05              | -    | V     |
|  | -                  | 0.10                | 10                  | 0.05                                  |       |       | -     | 0     | 0.05              | -    |       |
|  | -                  | 0.15                | 15                  | 0.05                                  |       |       | -     | 0     | 0.05              | -    |       |
| Output Voltage: High-Level, V <sub>OH</sub> Min.   | -                  | 0.5                 | 5                   | 4.95                                  |       |       | 4.95  | 5     | -                 | -    | V     |
|  | -                  | 0.10                | 10                  | 9.95                                  |       |       | 9.95  | 10    | -                 | -    |       |
|  | -                  | 0.15                | 15                  | 14.95                                 |       |       | 14.95 | 15    | -                 | -    |       |
| Input Low Voltage, V <sub>IL</sub> Max.            | 0.5, 4.5           | -                   | 5                   | 1.5                                   |       |       | -     | -     | 1.5               | -    | V     |
|  | 1, 9               | -                   | 10                  | 3                                     |       |       | -     | -     | 3                 | -    |       |
|  | 1.5, 13.5          | -                   | 15                  | 4                                     |       |       | -     | -     | 4                 | -    |       |
| Input High Voltage, V <sub>IH</sub> Min.           | 0.5, 4.5           | -                   | 5                   | 3.5                                   |       |       | 3.5   | -     | -                 | -    | V     |
|  | 1, 9               | -                   | 10                  | 7                                     |       |       | 7     | -     | -                 | -    |       |
|  | 1.5, 13.5          | -                   | 15                  | 11                                    |       |       | 11    | -     | -                 | -    |       |
| Input Current I <sub>IN</sub> Max.                 | -                  | 0.18                | 18                  | ±0.1                                  | ±0.1  | ±1    | ±1    | -     | ±10 <sup>-5</sup> | ±0.1 | μA    |

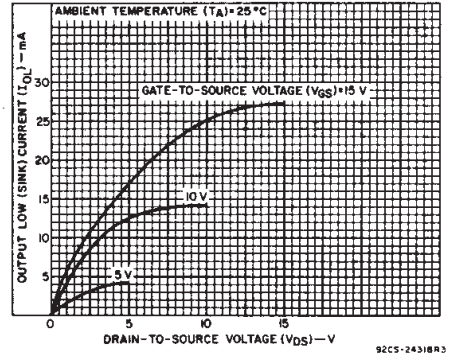


Fig. 2 - Typical output low (sink) current characteristics.

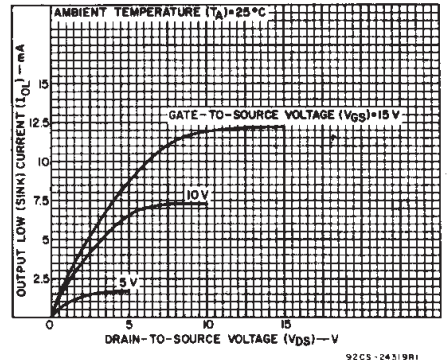


Fig. 3 - Minimum output low (sink) current characteristics.

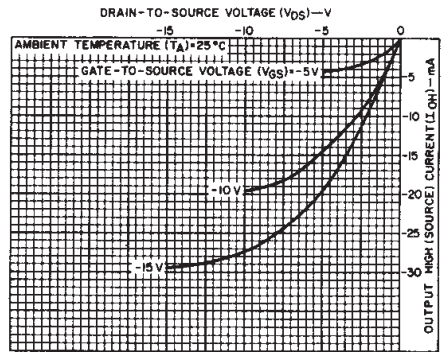


Fig. 4 - Typical output high (source) current characteristics.

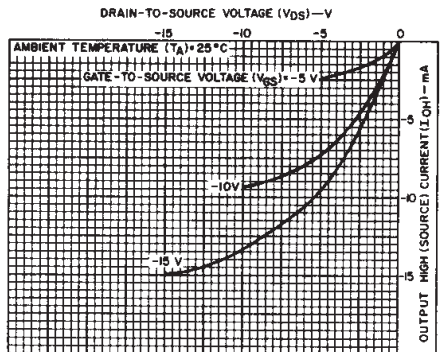


Fig. 5 - Minimum output high (source) current characteristics.

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# CD4006B Types

**DYNAMIC ELECTRICAL CHARACTERISTICS** at  $T_A = 25^\circ\text{C}$ ; Input  $t_{r_i}, t_{f_i} = 20\text{ ns}$ ,  
 $C_L = 50\text{ pF}$ ,  $R_L = 200\text{ k}\Omega$

| CHARACTERISTIC   | TEST CONDITIONS<br>$V_{DD}$ (V) | LIMITS |      |      | UNITS         |
|--|---------------------------------|--------|------|------|---------------|
|  |                                 | MIN.   | TYP. | MAX. |               |
| Propagation Delay Time,<br>$t_{PHL}, t_{PLH}$                  | 5                               | —      | 200  | 400  | ns            |
|  | 10                              | —      | 100  | 200  |               |
|  | 15                              | —      | 80   | 160  |               |
| Transition Time,<br>$t_{THL}, t_{TLH}$                         | 5                               | —      | 100  | 200  | ns            |
|  | 10                              | —      | 50   | 100  |               |
|  | 15                              | —      | 40   | 80   |               |
| Minimum Data Setup Time,<br>$t_s$                              | 5                               | —      | 50   | 100  | ns            |
|  | 10                              | —      | 25   | 50   |               |
|  | 15                              | —      | 20   | 40   |               |
| Minimum Clock Pulse Width,<br>$t_w$                            | 5                               | —      | 100  | 200  | ns            |
|  | 10                              | —      | 45   | 90   |               |
|  | 15                              | —      | 30   | 60   |               |
| Maximum Clock Input<br>Frequency, $f_{CL}$                     | 5                               | 2.5    | 5    | —    | MHz           |
|  | 10                              | 5      | 10   | —    |               |
|  | 15                              | 7      | 14   | —    |               |
| Maximum Clock Input Rise or<br>Fall Time, $t_{rCL}, t_{fCL}^*$ | 5                               | —      | —    | 15   | $\mu\text{s}$ |
|  | 10                              | —      | —    | 15   |               |
|  | 15                              | —      | —    | 15   |               |
| Input Capacitance, $C_{IN}$                                    | Any Input                       | —      | 5    | 7.5  | pF            |

\*If more than one unit is cascaded  $t_{rCL}$  should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

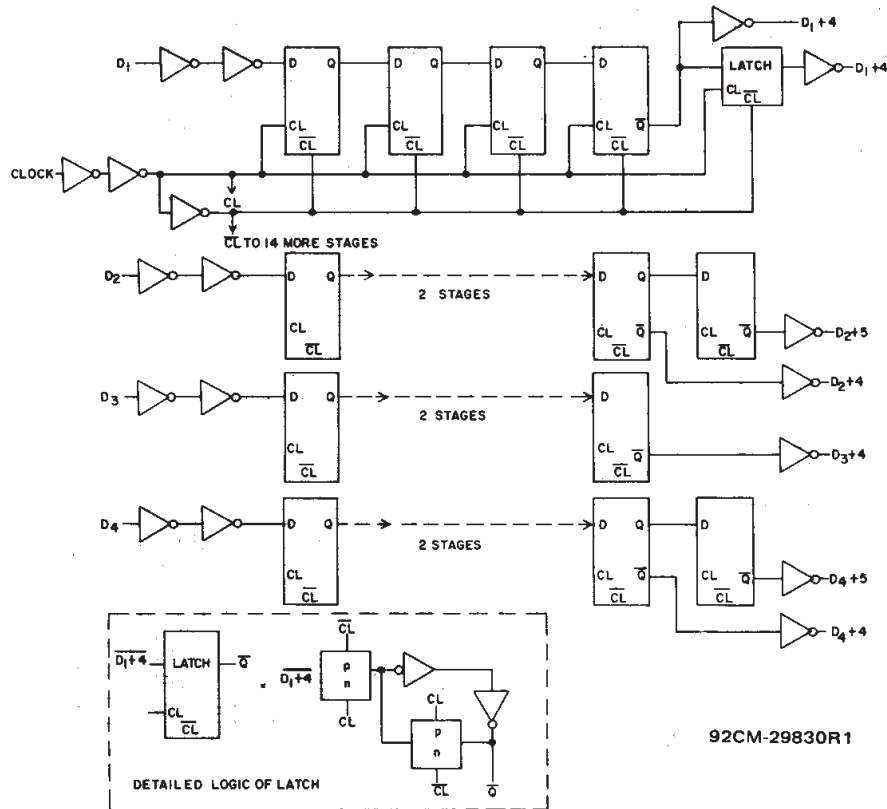


Fig. 6 - Logic diagram with detail of latch.

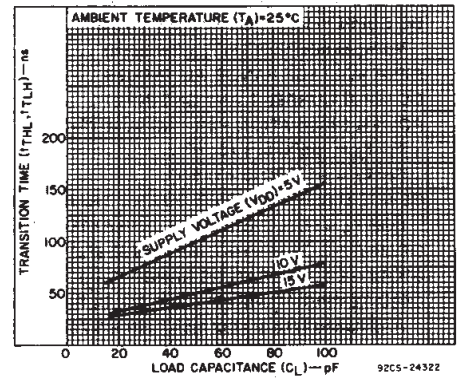


Fig. 7 - Typical transition time as a function of load capacitance.

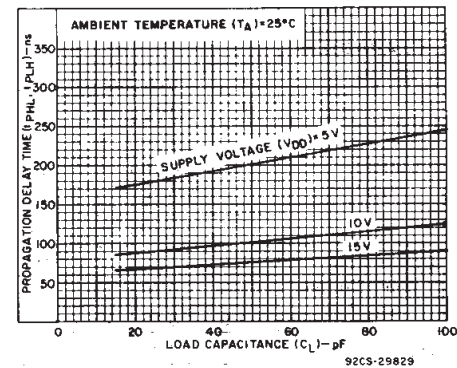


Fig. 8 - Typical propagation delay time as a function of load capacitance.

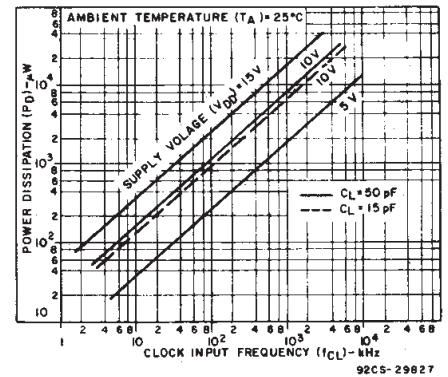


Fig. 9 - Typical dynamic power dissipation as a function of clock frequency.

# CD4006B Types

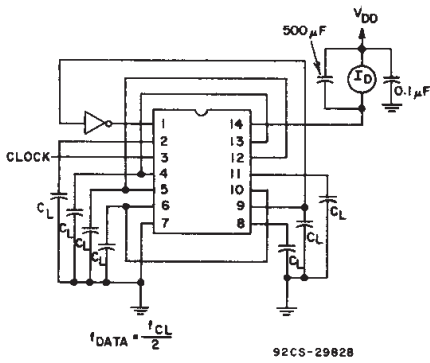


Fig. 10 - Dynamic power dissipation test circuit.

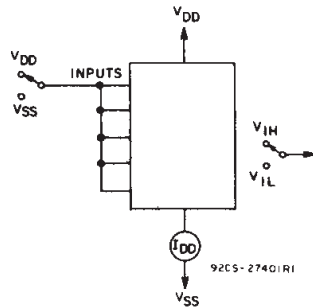


Fig. 11 - Quiescent device current test circuit.

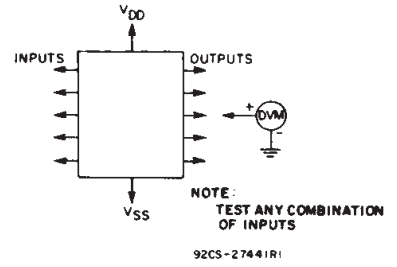


Fig. 12 - Input voltage test circuit.

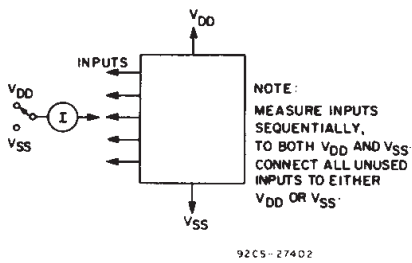
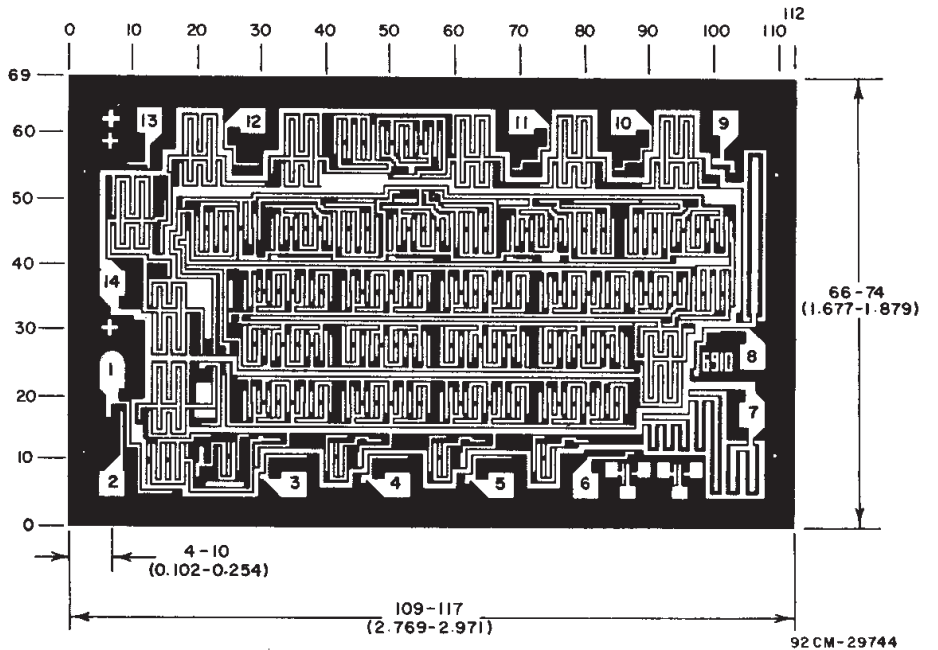


Fig. 13 - Input current test circuit.



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Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

Dimensions and pad layout for CD4006BH.

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| CD4006BE         | OBSOLETE              | PDIP         | N               | 14   |             | None                    | Call TI          | Call TI                      |
| CD4006BF3A       | ACTIVE                | CDIP         | J               | 14   | 1           | None                    | Call TI          | Level-NC-NC-NC               |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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