
Magic Packet Adapter Card Implementation



Application Note

ABSTRACT

This application note discusses the various aspects of Magic Packet adapter card design. It is recommended that this application note be used in conjunction with the Magic Packet Technology Application in Hardware and Software, Application Note, PID #20381A.

INTRODUCTION

To take full advantage of the Magic Packet technology, one needs to implement the complete system solution, i.e., motherboard (MBD), Network Interface Card (NIC), BIOS, standby power supply, and desktop management software.

This application note focuses on the hardware side of the system implementation. For modifications needed in the BIOS software, refer to the Magic Packet Technology Application in Hardware and Software, Application Note, PID#20381A. On the desktop management software side, the Magic Packet generation utility (MPWAKE), available from AMD, will run in conjunction with any existing desktop management software package. IBM Infinity and HP OpenView have already integrated this support in their current offerings, and several popular vendors' software packages (e.g., Unicenter™ TNG from Computer Associate and LANDesk from Intel) are soon to follow.

The motherboard accepts the wake-up signal from the Magic Packet capable NIC and performs the power management protocol. The wake-up signal will wake the motherboard either from standby or suspend mode. In standby mode, the computer is alive, with power to the entire motherboard. The low power consumption in this mode is accomplished by slowing down the processor clock, spinning down the hard drives, and putting the monitor in a low power consumption state.

In suspend mode, the computer is usually brought to a complete halt. The CPU is stopped and the main power supply is turned off, leaving the standby power supply to support the components. The entire system is powered down, except the power management circuit, (Super I/O or a keyboard controller chip) and the Ethernet components which receive the Magic Packet frame that wakes up the system.

ADAPTER DESIGN

The Magic Packet adapter card design has a single RJ45 connector for both 10BASE-T and 100BASE-T signals that are interfaced to a common magnetic.

The PHY component is responsible for Auto-Negotiation, sublayer coding, media transceivers, and timing. Because of its low I_{DD} requirements as compared to other 10/100 Physical Layer (PHY) solutions, the ICS 1890 is being used as an example for the PHY component in this application note. Other comparable PHY solutions are also available in the market and can be used as a PHY alternative for Magic Packet applications.

AMD recommends using the 10/100 PHY component with the lowest I_{DD} specification, which will minimize the overall I_{DD} requirement for the standby power supply. This in turn will allow one to use a lower cost standby power supply, thus lowering the overall Magic Packet implementation cost.

The Media Access Controller (MAC) block is the Am79C971 PCnet™-FAST controller, which is responsible for Ethernet protocol framing. For optimized performance, the two 32K x 8 SRAMs are used to extend the required FIFO depth externally to buffer the data in 100BASE-T mode.

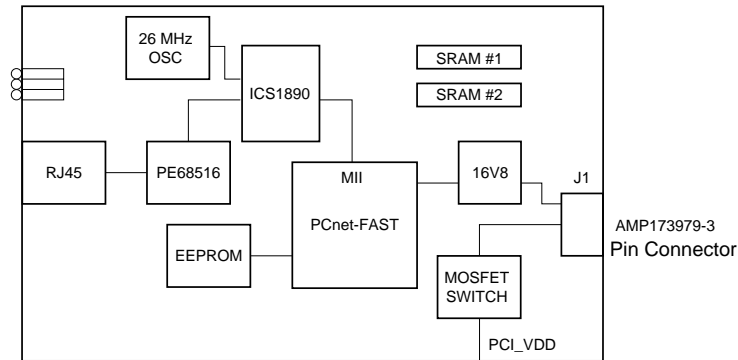
The PALCE16V8 device provides two main functions: (1) the necessary conditioning of the RESET line to the MAC and (2) the correct polarity of the LED3 pin to the LAN WAKE-UP signal input and to the power management circuit. The PCI RESET signal needs to be blocked during power-down because it prevents the MAC from staying in Magic Packet mode. A detailed explanation of the PAL equations is provided in a later section.

There are two methods of powering the networking components. One method is to power the Ethernet components (shown in Figure 1) with a +5 V standby supply at all times (normal and Magic Packet operations). The I_{DD} (max) requirement for the NIC design in Figure 1 is 430 mA. Therefore, in order to also support

the motherboard's power management circuitry, the current requirement for the +5-V standby power supply source should be at least 500 mA.

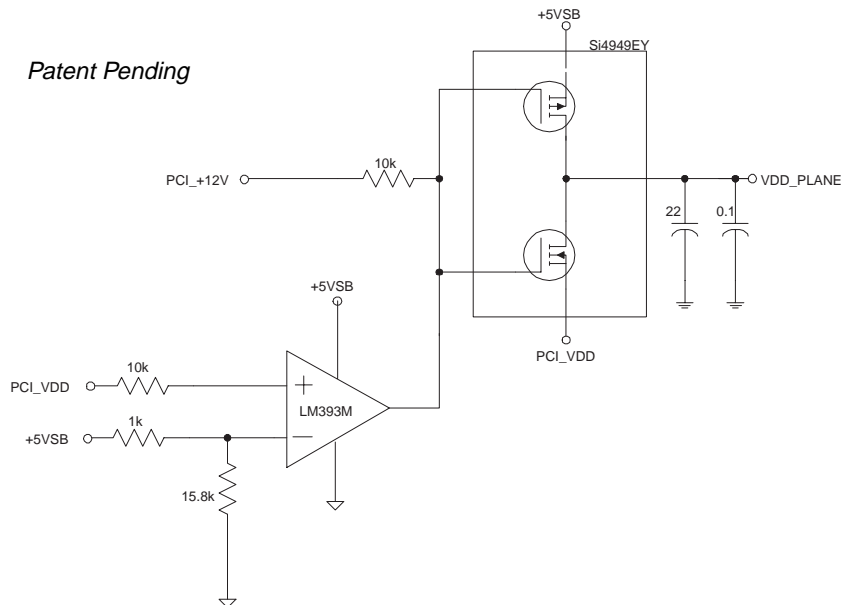
The other method of powering the networking components is to use the main power supply during normal operation and switch over to the +5 V standby power

supply during Magic Packet operation. The I_{DD} (max) requirement during Magic Packet mode with no PCI clock is 250 mA. This method can be achieved by dynamically switching the PCI +5 V main power over to the +5 V standby supply. Refer to Figure 2 for the dynamic power plane switching scheme.



21385A-1

Figure 1. Magic Packet Adapter Card



21385A-2

Figure 2. Power Plane Switching Scheme

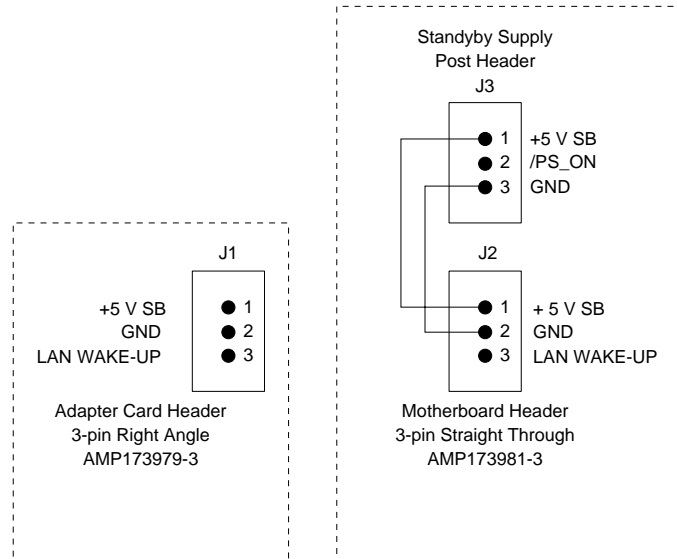
The trade-offs between the two methods described are the cost of the standby power supply versus the complexity of the NIC design. The first method greatly reduces the complexity of the NIC design, but increases the cost of the standby power supply. The second method increases the complexity of the NIC design, thereby, increasing the cost to the Bill of Materials

(BOM) by adding extra logic (enhanced P-MOSFET and N-MOSFET with a high-speed voltage comparator). However, the second method allows the use of a cheaper standby power supply (lower I_{DD} requirement). The designer will need to decide which method is more viable for the desired implementation.

In order for all NICs and MBDs to interoperate, the 3-pin header was defined as the standard component (as shown in J1) for connectivity between the NIC and the MBD for Magic Packet system implementation.

The J1 connector of Figure 3 is provided for routing the required +5 V standby power supply and the LAN

WAKE-UP signal. J1 is a standard AMP 173979-3 3-pin connector. The pinouts are pin 1 for +5 V standby supply, pin 2 for +5 V End Return, and pin 3 for LAN WAKE-UP signal. Figure 3 shows the relationship of the J1 adapter card header to the J2 motherboard header. Appendix A provides specifications for the connectors.



21385A-3

Figure 3. Adapter J1 3-Pin Header Definition

Signal Cable

To interconnect the MBD and the NIC, refer to Figure 4, which shows the required ribbon cable connecting J1 to J2. The cable length should be 12.0 ± 0.5 inches, and the wire gauge should be 26 AWG. No shielding is necessary.

PAL[®] EQUATION DISCUSSION

An external PALCE16V8 is used in this application to provide the necessary interface to the system bus RESET and to provide the proper polarity for the LED3 pin to interface to the power management circuit. Appendix B contains the PALASM[®] equations for the PALCE16V8 used. The PAL's function is to block the RESET during power down in order to preserve the state of the MAC controller in Magic Packet mode. Its other function is to interface the LED3 pin to the LAN WAKE-UP input pin of the motherboard's power management circuit.

CONCLUSION

Magic Packet technology provides MIS managers the benefit of remotely managing client PCs during off hours, while maintaining energy savings and, thereby, increasing overall productivity and lowering overall costs. Magic Packet technology can be easily implemented in 10/100BASE-T NICs by utilizing the Am79C971 MAC controller. To take *full* advantage of the Magic Packet technology, it is necessary that the entire system, including all components described in this application note, be implemented.

REFERENCE NOTES

- *Magic Packet Technology White Paper*, PID #20213A
- *Magic Packet Technology Specification*, PID #20212C
- *Magic Packet Technology Application in Hardware and Software*, Application Note, PID #20381A

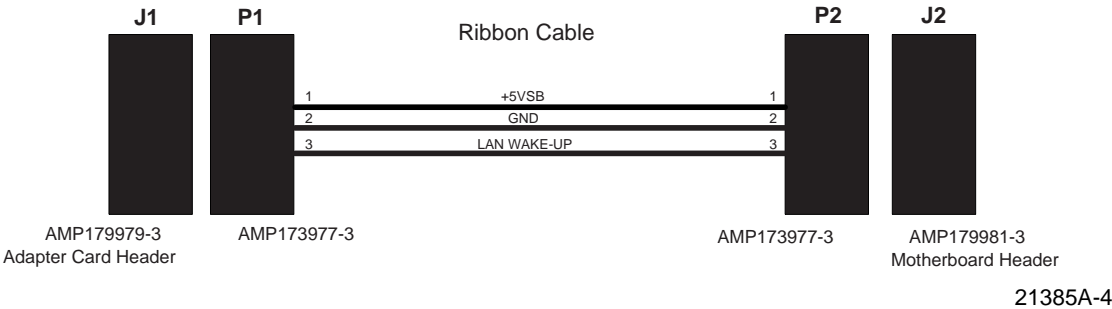


Figure 4. Ribbon Cable Definition and Recommended Connectors

AMP Connectors

WIRE-TO-BOARD CONNECTORS

AMP CT (Common Termination) Connector System

Post Header Assemblies (for MT and Crimp Type)

Standard Type

Post Header Assemblies (PC Board Application Side)

Horizontal Mount Type

Materials and Finishes:

Housing - UL 94V-0 rated, 6/6 Nylon, natural color

Post Contact - Tin plated brass

Drilled Hole Diameter: 0.85-0 -0.05

Punched Hole Diameter: 0.8-0 -0.3

2.0 Pitch (tolerance not to accumulate)

PC Board Layout:

(Acceptable board thickness 0.8 - 1.6 mm)

Vertical Mount Type:

Materials and Finishes:

Housing - UL 94V-0 rated, 6/6 Nylon, natural color

Post Contact - Tin plated brass

Drilled Hole Diameter: 0.85-0 -0.05

Punched Hole Diameter: 0.08-0 -0.3

2.0 Pitch (tolerance not to accumulate)

PC Board Layout:

(Acceptable board thickness 0.8 -1.6 mm)

No. of Positions	Dimensions		Part No. of Post Header Assembly	
	A	B	Horizontal Mount	Vertical Mount
3	4.0	7.8	173979-3	173981-3

FEATURES

Product Type	Connector
Connector Type	Crimp, MT (Mass Termination)
Mating Type	Header
No. of Positions	3
No. of Rows	1
Terminate To	PCB (Header)
Header Body Style	Standard
PCB Mount Style	Through Hole
PCB Mount Angle	Right Angle/Vertical
PCB Polarization	No
Special PCB Retention	Yes
Special PCB Retention Method	Self-Retaining Solder Post
Panel Attachment	No
Housing Material	6/6 Nylon
Housing Color	Natural

OTHER PROPERTIES

Dimension A	.157 [4.00] in. [mm]
Dimension B	.307 [7.80] in. [mm]
Housing Flammability Rating	UL 94V-0
Contact Material	Brass
Contact Mating Area Plating	Tin
Solder Tail Plating	Tin

WIRE-TO-BOARD CONNECTORS

AMP CT (Common Termination) Connector System

MT Connectors (2mm Pitch)

Receptacle Assemblies (Wire Application Side)

Materials and Finishes:

Housing - UL 94V-0 rated

glass filled PBT (color white, but other colors available; contact AMP Sales Dept. for details)

Contact - Pre-tin, phosphor bronze

Wire Size:

AWG = 28-26 (0.08 - 0.15²) [mm]

Insulation Diameter: 0.85 -1.05 mm

No. of Positions	Dimensions			Part No. of Receptacle Assembly White
	A	B	C	
3	4.0	6.8	8.0	173977-3

FEATURES

Product Type	Connector
Connector Type	Crimp, MT (Mass Termination)
Mating Type	Receptacle
No. of Positions	3
No. of Rows	1
Terminate To	Wire
Panel Attachment	No
Housing Material	Glass-Filled PBT
Housing Color	White

OTHER PROPERTIES

Dimension A	.158 [4.0] in. [mm]
Dimension B	.268 [6.8] in. [mm]
Dimension C	.315 [8.00] in. [mm]
Wire Range	28-26 [0.08-0.15 ²] AWG [mm]
Wire Insulation Diameter	.034-.041 [0.85-1.05] in. [mm]
Wire Termination Type	IDC Mass Termination
Housing Flammability Rating	UL 94V-0
Contact Material	Phosphor Bronze
Contact Mating Area Plating	Pre-Tin
Packaging Quantity	1000
Pistol Grip Handle Assembly	58074-1'
Pistol Grip Modular Assembly	58372-1
Pistol Grip Tool Assembly	911790-1

PALASM Design Description

;PALASM Design Description

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;-----Declaration Segment-----
-
TITLE      Magic Packet Convertor
PATTERN    MAG_PCI.PDS
REVISION   A
AUTHOR     David Stoenner
COMPANY    AMD
DATE       08/28/95
CHIP       _mag_pkt    PALCE16V8
;-----PIN Declarations-----
PIN 1      EEPROM_CLK
PIN 2      /RESET_IN
PIN 3      /VCC_GONE
PIN 4      /LED3
PIN 10     GND
PIN11      /OE
PIN12      /RESET_TO_CHIP
PIN 13     /FIRST_TIME
PIN 15     LED3_OUT
PIN 19     /SLEEP
PIN 20     VCC

;-----Boolean Equation Segment -----
EQUATIONS
LED3_OUT = LED3 * VCC_GONE * FIRST_TIME
          + LED3_OUT * VCC_GONE
FIRST_TIME: = VCC
RESET_TO_CHIP = /FIRST_TIME * RESET_IN
               + FIRST_TIME * LED3_OUT
               * VCC_GONE
SLEEP = VCC_GONE
;-----Simulation Segment-----
-

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