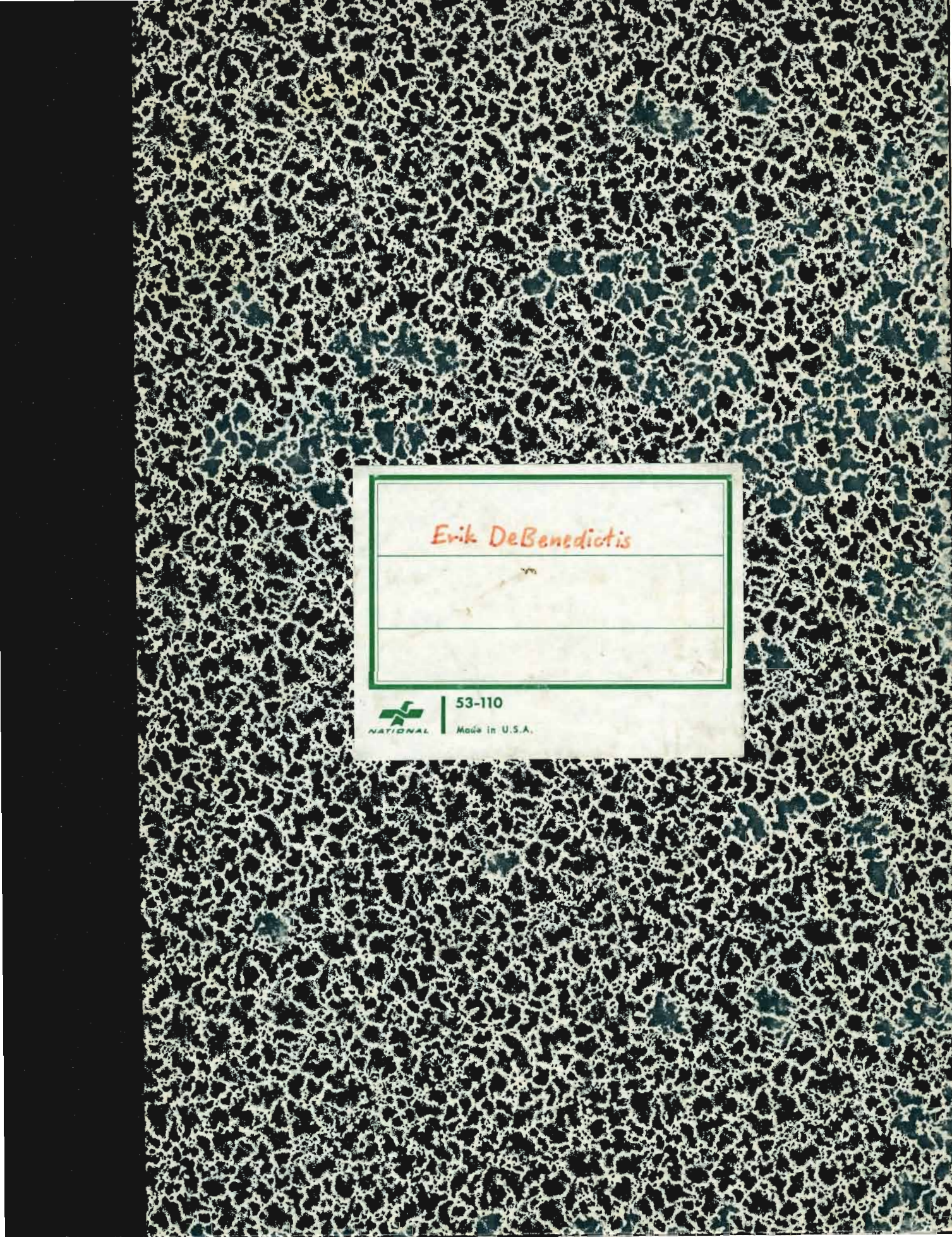
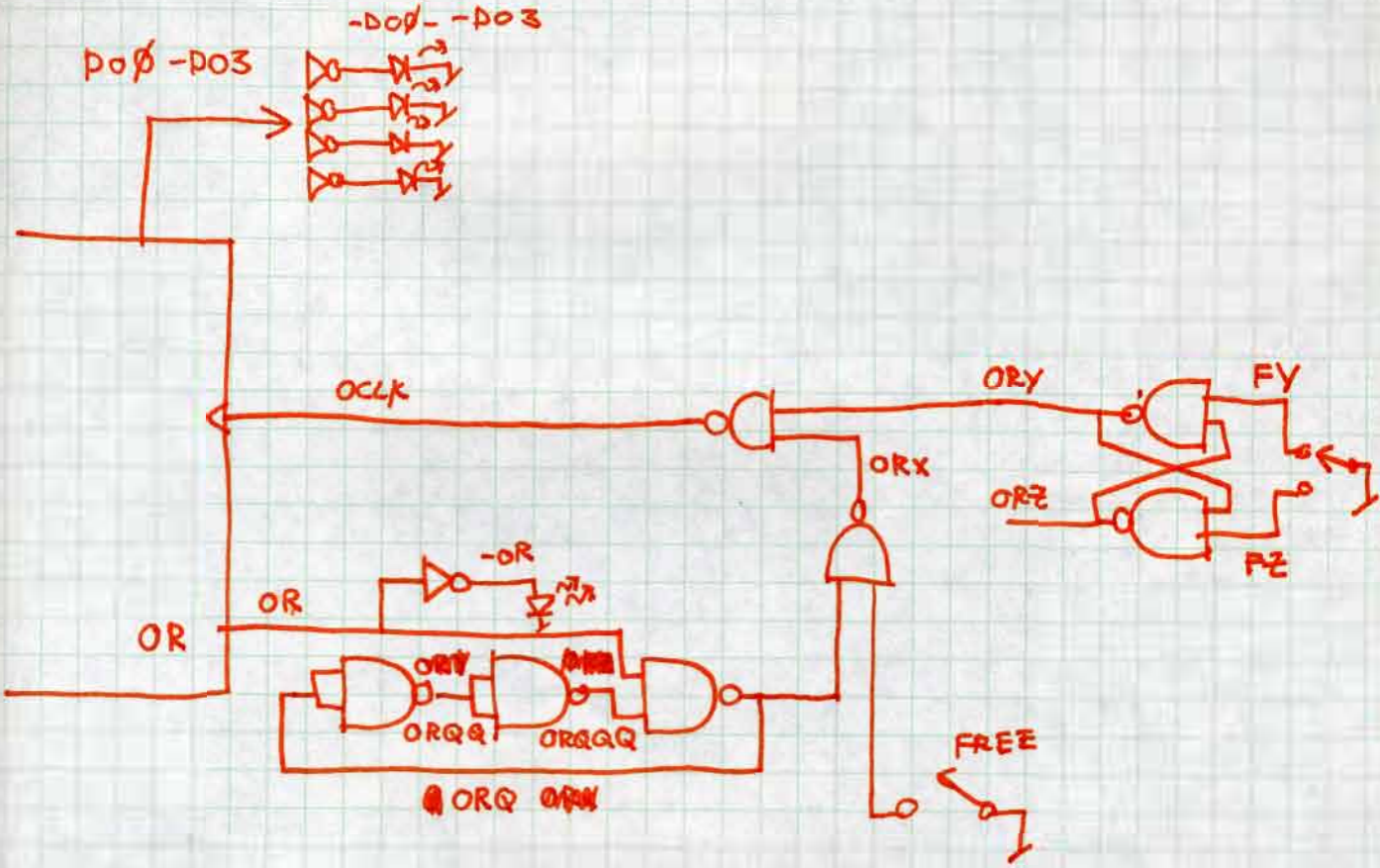
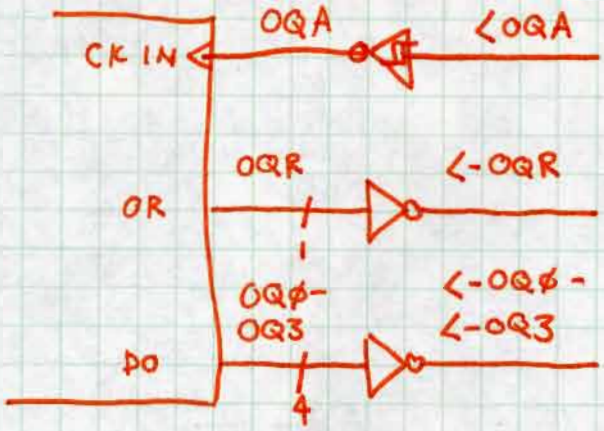
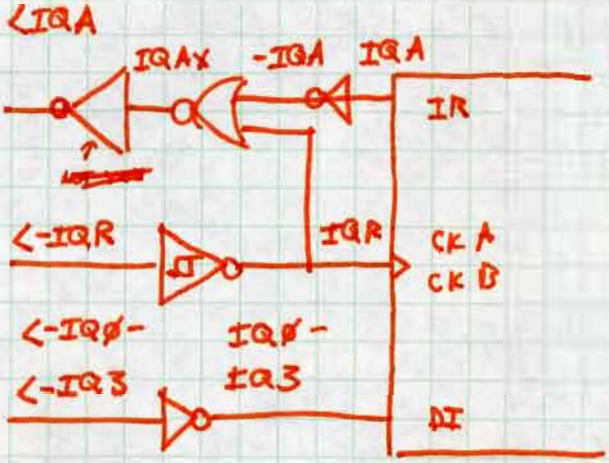

Evik DeBenedictis
NATIONAL
53-110
Made in U.S.A.

Erik DeBenedictis

UNLOAD CIRCUITRY







Internal Transfer Rate

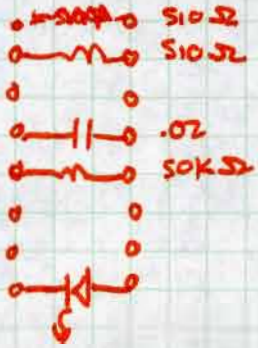
3' Ribbon Cable 900 ns / cycle

300" = 25' Ribbon Cable 2000ns / cycle

DHZ80 Board

03M01	!X1
03M02	!X2
⋮	
03M15	GND
03M16	GND

03M CC



3-Nov-81

PROM8

Does checksum of its prom (800-FFF) and prints on terminal. Repeats.

Should print 954B

PROMØ

Does checksum of PROMØ (0-800) and prints on terminal. Repeats.

Check with PROM burner for verification.

RAM4

Does ramcheck of ram at 4000-7FFF. Writes incrementing 16 bit patterns and compares back. Starting 16 bit value is printed each iteration.

If fail is found program checks S1 to continue

S1 up ⇒ continue

S1 down ⇒ wait

RAM8

Same as RAM4 but for RAM 8000-BFFF

RAMX

Same as RAM4 but for RAM 4000-BFFF

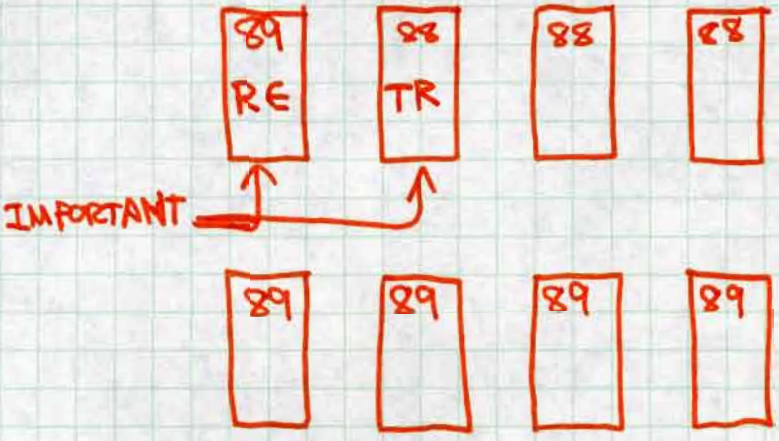
3-NOV-81

ECHO

Outputs message. Then inputs from terminal and echos character plus one.

I/O check: S10/0

Ch A	RxDA	12
	TxDA	15
Ch B	RxDB	28
	TxDB	26



RAMALL

Checks all RAM (4000-BFFF). If an error is detected the syndrome is printed. S1 up ⇒ continue on error, S1 down ⇒ stop on error.

ZMON for DHZ80

NMICNT 42FF

OUTBYT 4301

-IO78 <=> Reset fifos

4-NOV-81

TIMING

(Forget it)

13-NOV-81

MAIN BOARD

8288 -AEN should be GND, not 5V

-RAS should come from -A17

-PROM should come from A17

RAM ~~address~~ Power Supplies Backward

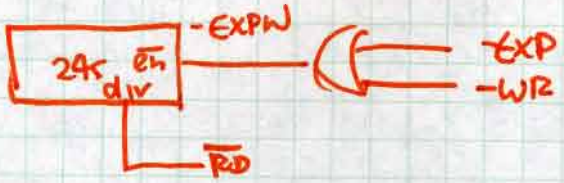
IO word addressed - change decoders to A4, A2, A3 from A0-A1-A2

21 Jan 82

BASE7 board/wirelist

Discovered logic error on 245, prevented reading external I/o space.

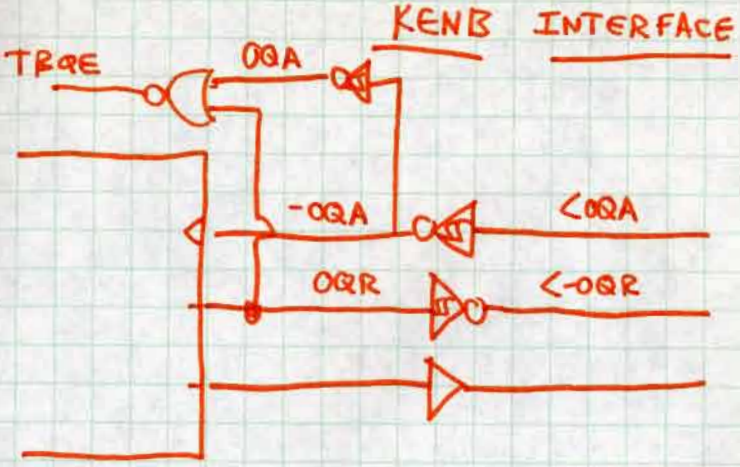
WAS

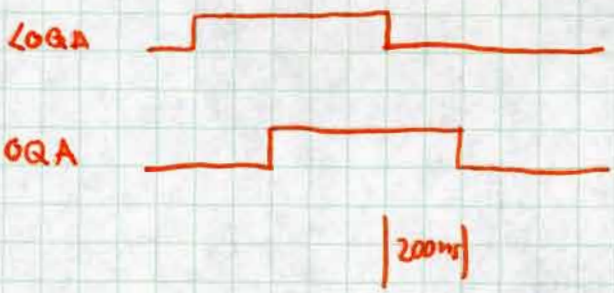


IS

Base7 is recommended for future designs.

KENB INTERFACE

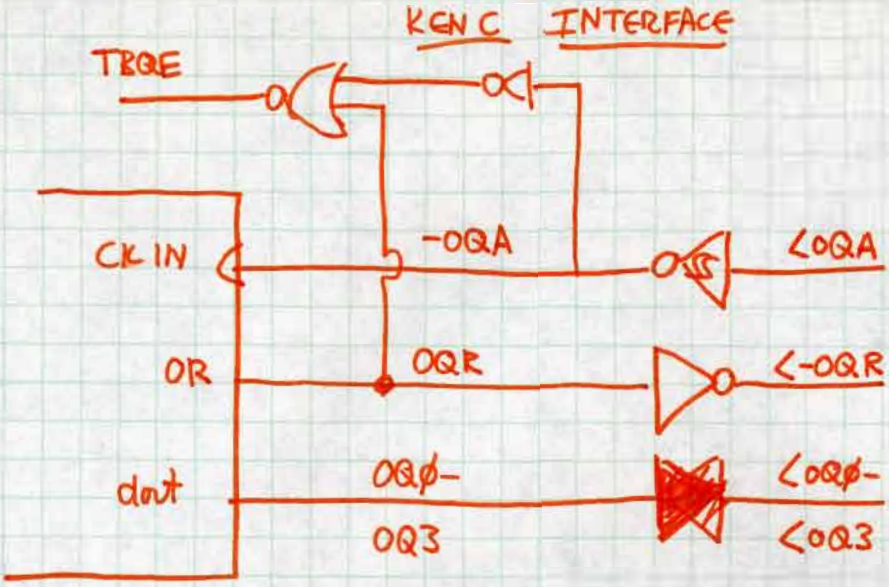




74C14s

Node OQR needs pullup.

Delay -OQA - OQA is too large.

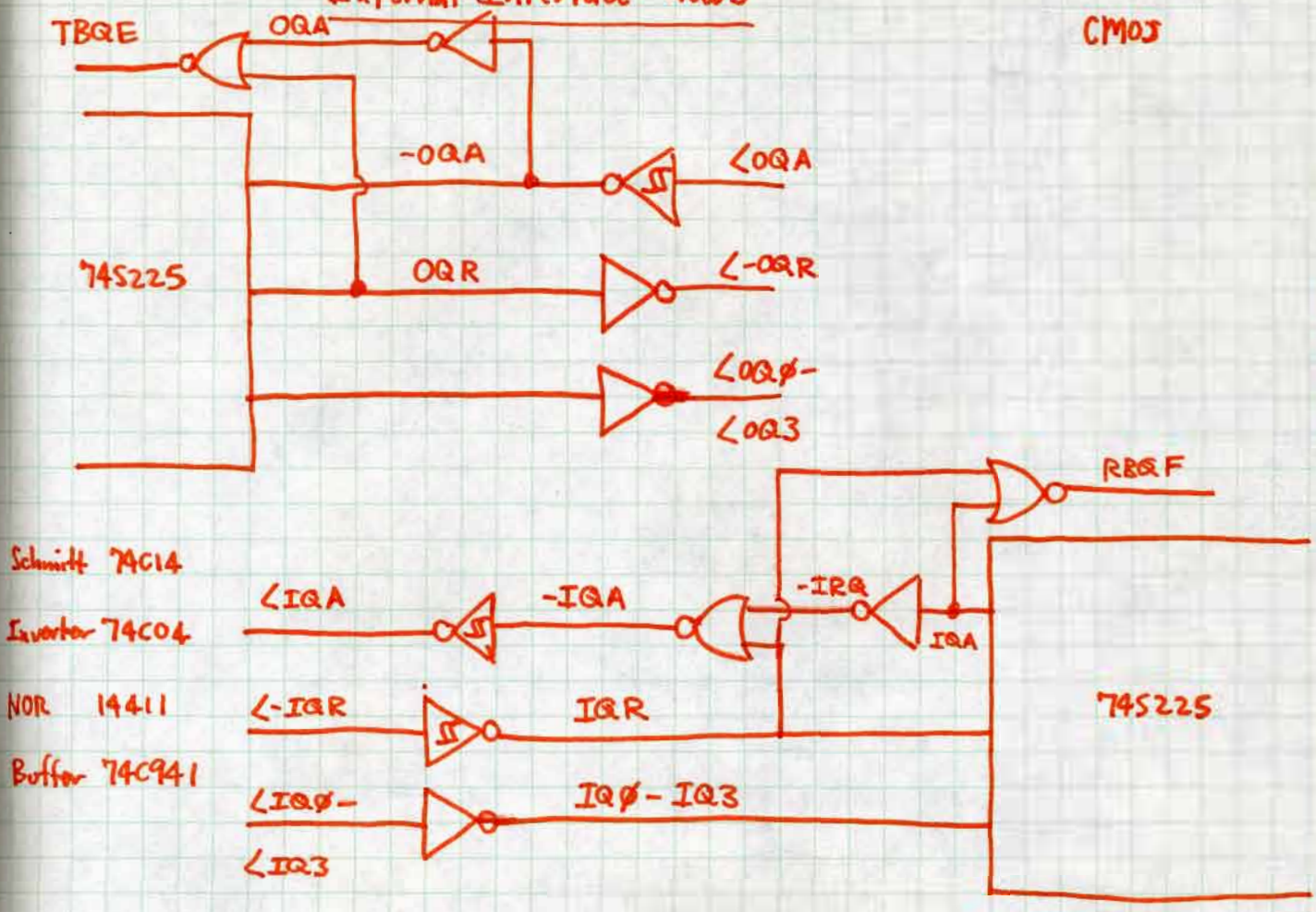


Delay CK IN ↓ to OR ↓ 25 ns

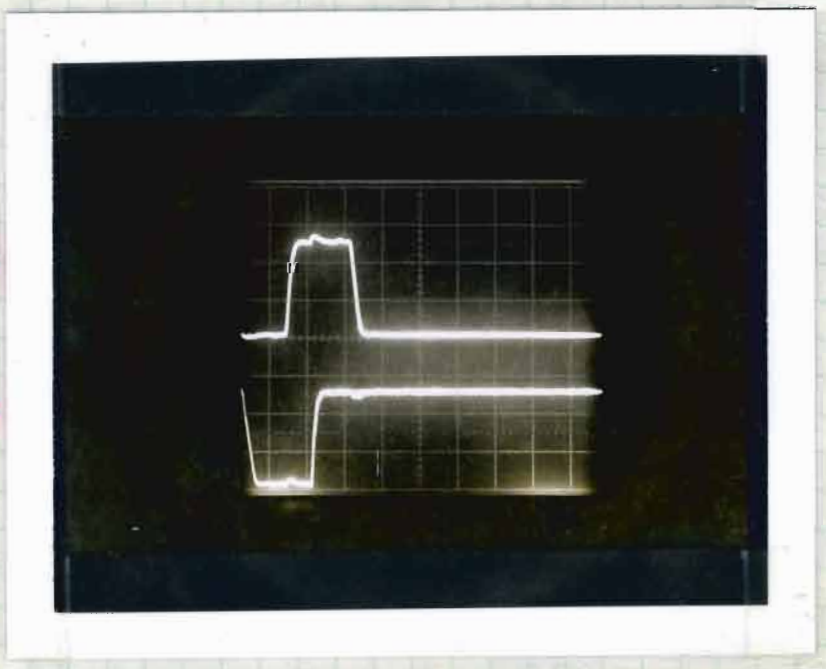
23 Jan 82

CMOJ

External Interface New5



Handshake



1 foot cable
(multi-colored
from stockroom)

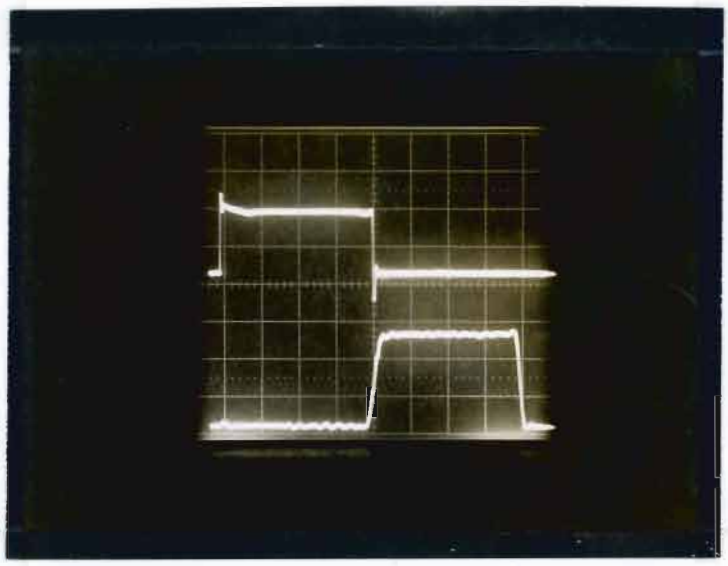
2v/div vert

500ns/div horiz

1.5μs cycle
(5 of 4 phases)

TBQE Generation

23 Jan 82
Chas

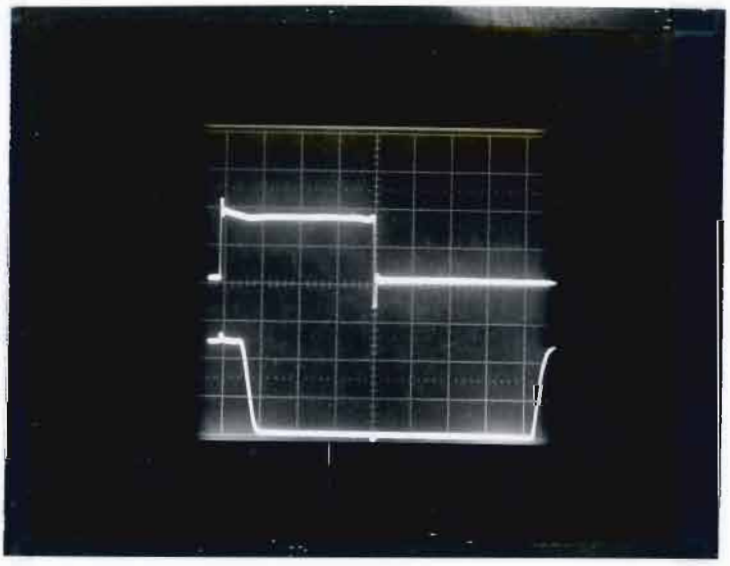


OQR → 01E02

OQA → 01E01

2V/div vert

200ns/div horiz



OQR → 01E02

TBQE → 01E03

2V/div vert

200ns/div horiz

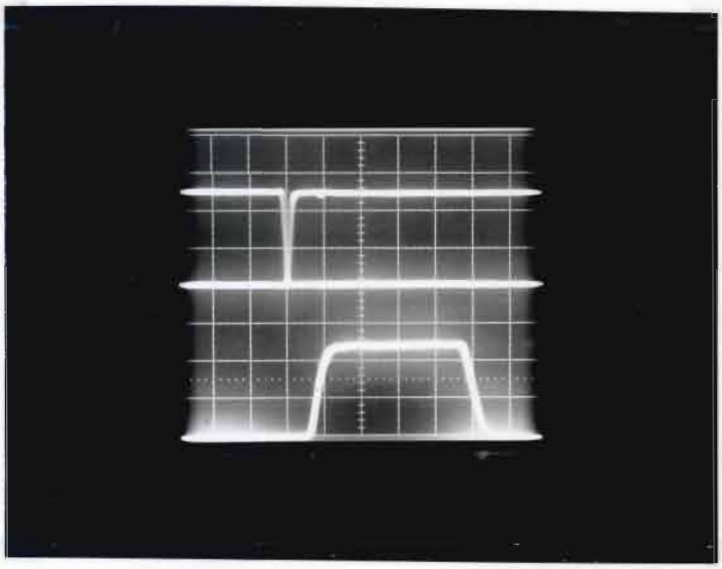
Traces are zeroed at center and bottom.

Zero overlap.

TB No glitch, but signal wiggles a bit.

23 Jan 82
CMOS

Data Setup



IQ Ø DMA
02F01 →

IQR →
02F04

2 v/div vert
200ns/div horiz
(Multicolored cable, 1' long)

150 ns setup time

23 Jan 82

MIXED

LS TTL implementation

Schmitt 7414 (LS)

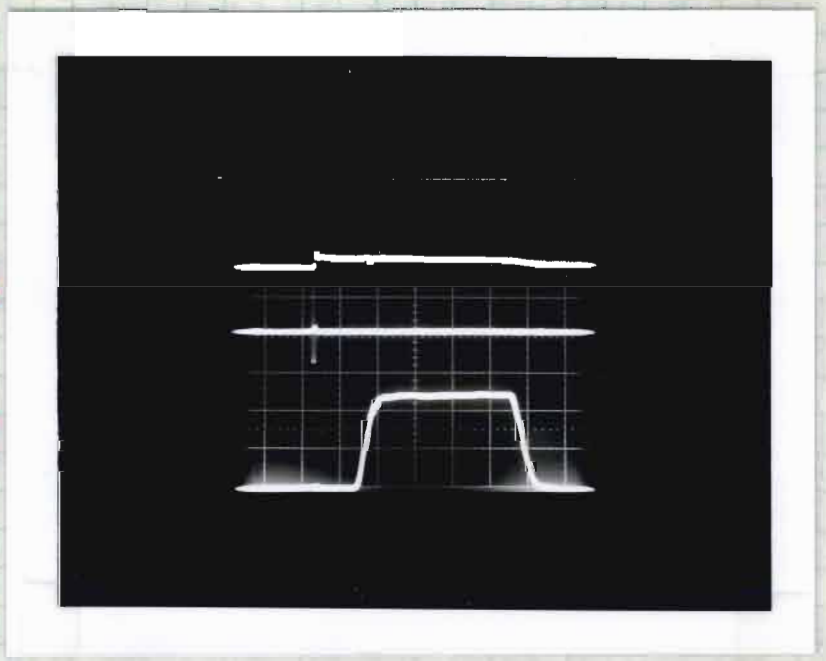
Inverter 7404 (LS)

Nor 14411

Buffer 74244 (LS)

Buffer Effect

Only change 74C941 for 74LS244!



IQØ →

IQR →

2 v/div vert

200 ns/div horiz

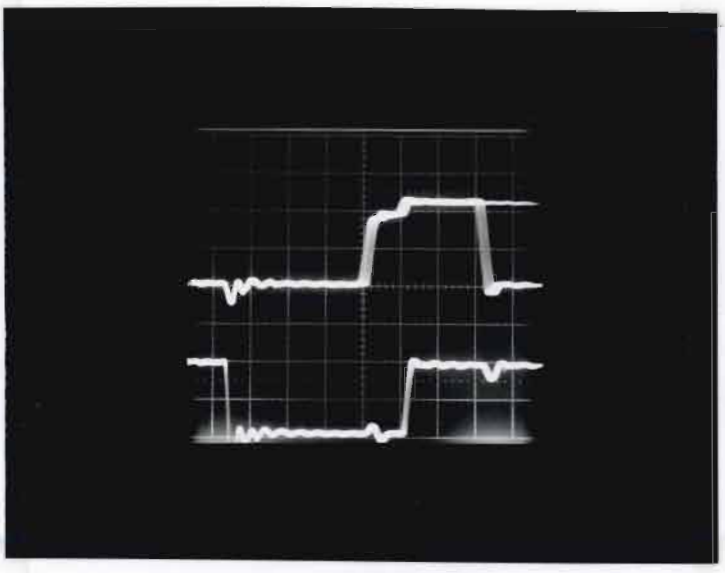
150-225 ns setup time change.

CMOS takes 75 ns longer than LSTTL.

23 Jan 82

LSTTL

Handshake



∠IQA
01A10 →

∠-IQR
01A13 →

2v/div vert

traces zeroed center & bottom

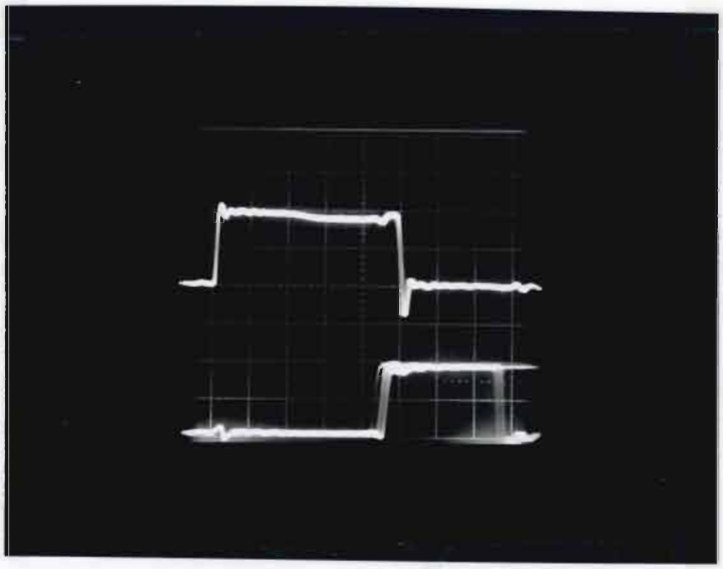
50ns/div horiz

350ns cycle (3 of 4 phases)

23 Jan 82

TBQE Generation

LSTTL

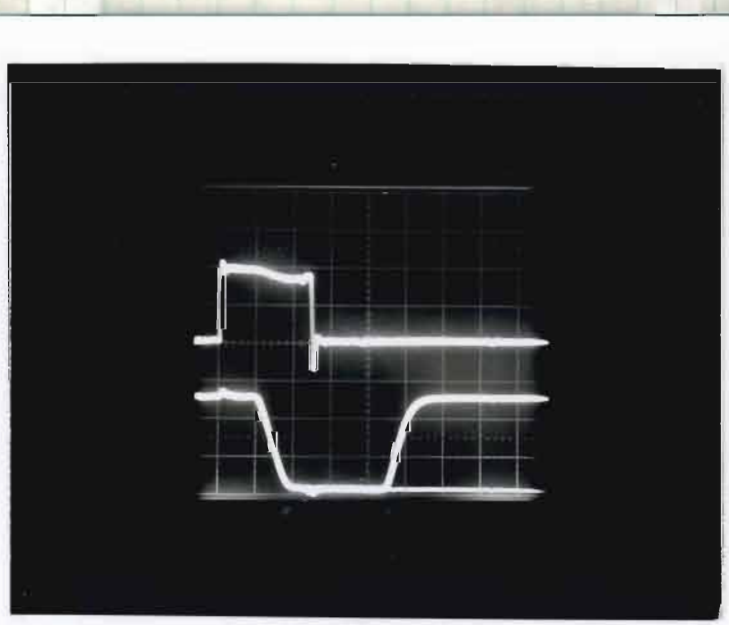


OQR
01A02 →

OQA
01A01 →

vert 2v/div
(centered)

50ns/div horiz



OQR
01A02 →

TBQE
01A03 →

2v/div vert
(centered)

100ns/div horiz

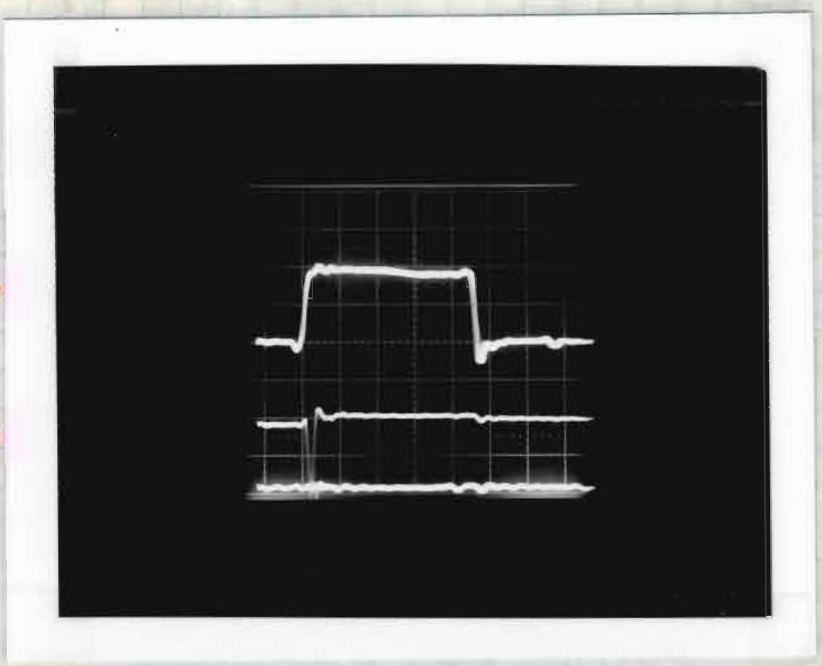
Note significant overlap.

No glitch.

23 Jan 82

Data Setup

LSTTL



IQ0
02F01 →

IQR
02F04 →

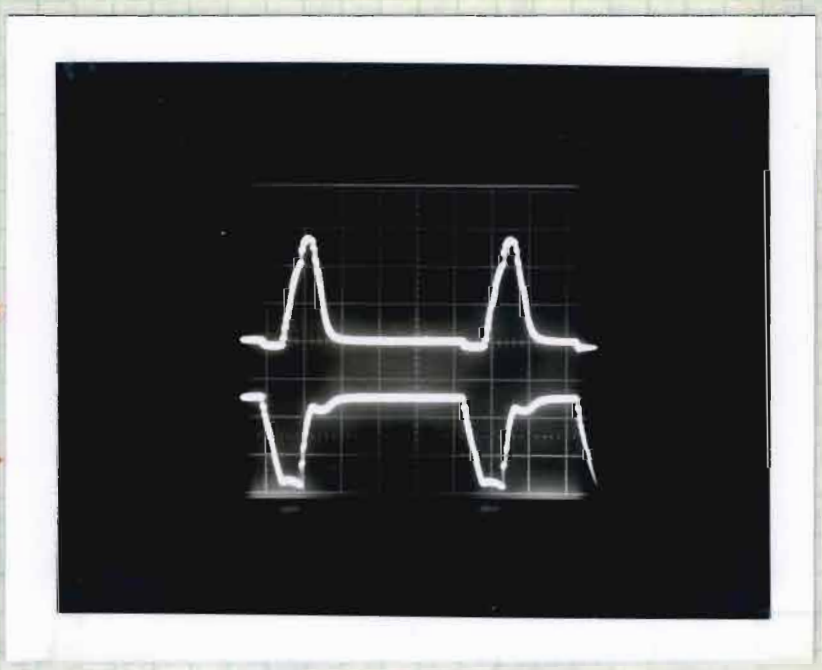
2v/div vert
(centered)
50ns/div horiz

Data Setup -30 ns

23 Jan 82

Long Cable CMOS interface

CMOS Long



60 foot

2v/div vert

5ps/div horiz

<IQA
01A10 →

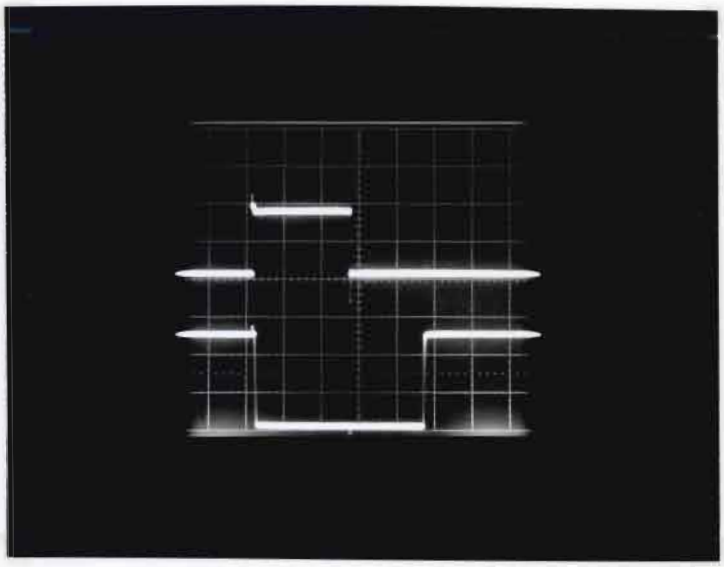
<-IQR →
01A13

Cycle 10 μs (3 of 4 phases)

TBQE Generation

23 Jan 82

CMOS Long

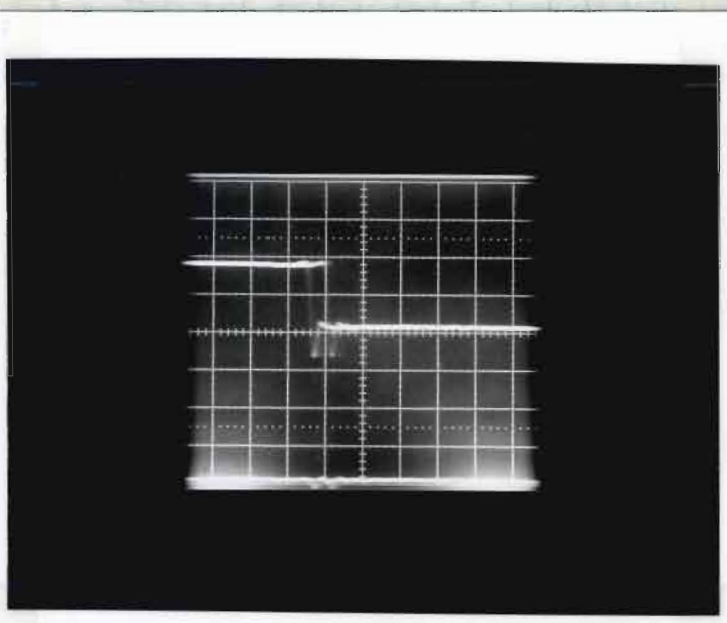


OQR
01C02 →

TBQE
01C03 →

2v/div vert
centered

2μs/div horiz



OQR
01C02 →

TBQE
01C03 →

2v/div vert
(centered)

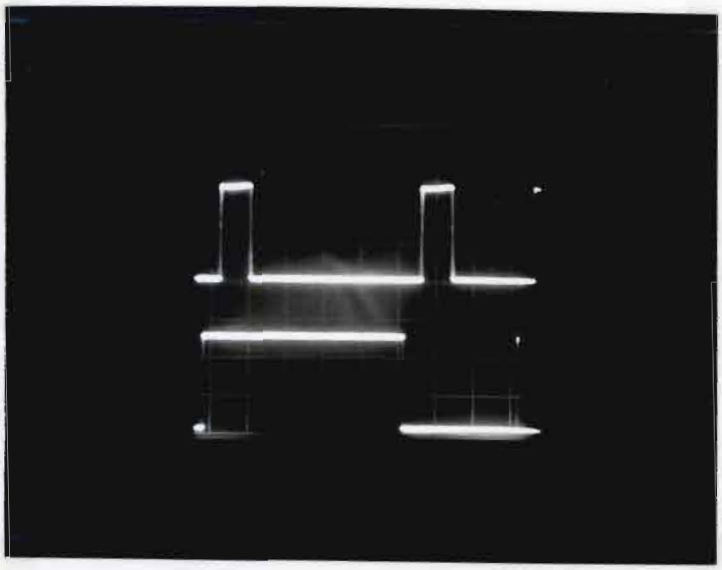
50ns/div horiz

No glitch

Data Setup

23 Jan 82

Cmos Long



Din
02F01 →

IOR
02F04 →

2v/div vert
(centered)

5μs/div horiz

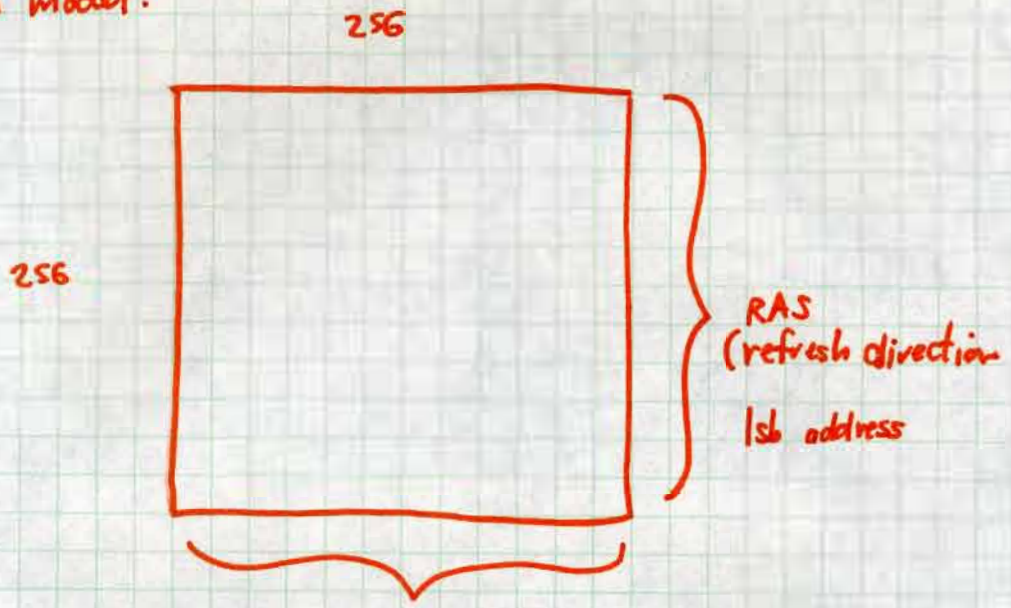
Data setup 2 μs

86-12a interrupts

		INT	SYA
0	RX INTR	82	81
1	TX INTR	90	88
2	[illegible] TMR1INTR	[illegible] 91	79
3	[illegible] CDC	70	78
4	BFI RX	69	[illegible] 77
5	BFI TX	68	[illegible] 76
6	[illegible] FIFO TX	[illegible] 66	[illegible] 75
7	[illegible] FIFO RX	[illegible] 65	[illegible] 74

RAM Death Diagnostic

RAM model:



An interesting RAM characteristic might be obtained by examining an entire row.

Locations on each row are separated by 256 addresses / 512 bytes.

Adjacent rows should be in a known (constant) state to prevent coupling.

We actually examining every 256th byte due to the funny 128 refresh stuff.

Test: Zero 16 rows and analyze only the middle one. Use feedback to adjust delay to exact threshold of one bit and observe other bits. The particular bit of interest is known to drift 0→1.

Feedback model:

Stage 1 exponentially increasing times (2^n) until 1 bit observed

Stage 2 successive approx. until convergence

Stage 3 algorithm:

Init jump = 1
dir = ∅
count from before

if direction change from last time then
jump = 1
else jump = jump + (jump+1)*2

if bit = 1 then count = count - jump
if bit = ∅ then count = count + jump
dir = bit

Output row msb tested:

Results particular unit

5F8E on screen COUNT 0578 8 2 0 A 0 8 0 0 8 0 2 0 8 A heat gun 20"

CPU fails, probably just hot! heat gun 15"

Might be unreliable ?? Can't tell.

4393 8 A 0 A 2 8 0 0 0 0 2 8 8 8

458E 8 A 0 A 2 8 0 0 0 0 2 8 8 8

Other unit

1A9F	2A2A0222A2A880
1AAD	AA2A0222A2A880
1A8F	2A2A0202A2A880
1952	AA2A0202A2A880
1986	2A2A0222A2A880
145B	2A2A0202A2A880

← POWER CYCLE

First unit

414A	0A0A2800002088
4188	8A0A2800002888
429B	8A8A2800802B8A
3FB3	0A0A2800002888
3437	8A8A2800002888

← POWER CYCLE

Speed check

65,000 packets in 6 sec

10 K packets/sec

10K · 16 160K bytes/sec

Failure:

Channel 4, receiver, board ∅

* Cables swapped - no effect
* Transmit FIFO - no effect
* 4.956 V original
  4.817 V still happens
  5.150 V still happens

Channel 4, 14001 still happens } sorry, wrong board
Channel 4, 74c04 still happens }

* Channel 4 14001 replaced still happens
* Channel 4 14c14 & 14c04 still happens
* Software swizzle of 4 & 5 still happens
* Extra software guard still happens

18 October 82

Reported ram problem, CPU #1

Flakiness at the following addresses:

55AB	75eB	D32C	D926 D927
57A8	7789	D32D	DB24
57A9	7987	D52A	DB25
5BA4	7B85 ??	D52B	DD23
5BA5			
5DA3		D728	
Program R, 580h		D729	

Action: Replace 8288 - no effect

{74LS00 with 7400} → 7400/74LS773 (adj 8288) - gone

{74LS00 with 7400} → 7400 only - gone

nothing - still there

74LS00 with another 7400

D52B D927

74LS00 with 74H00 - gone

Old 7400 saved 74H00 left in

Hits at:

11FF3	31	23 oct 82
11FF4	59	
11FF3	17	
11FF4	BF	

Cont later

23 Oct 82

Problem reported with 74H00.

Analysis: With a 74LS00 the -RAS line is overloaded and the H → L transition is slow, irregular and delayed. With a 7400 it is better, 74H00 better yet. 74S00 rings alot, but probably due to scope.

Flakey board has power supply voltage of 4.75v.

Suggestions: Use 74S373 for the RAS address driver. This improves timing under all circumstances.

Use ~~74S00~~ 74H00 (or 74S00 if the signal quality can be verified). This fixes the H→L -RAS transition.

If the RAM is slow, a 7404 instead of 74LS04 will give 3ns more RAS-CAS interval. The value of this is questionable

Use supply voltage = 5v.

Criticism: The overloaded 74LS00 is an engineering error. The source of the error was either sloppy debugging, or due to the prototype also using a 7400 (because 74LS00's not available.

The 74S373 / 74LS373 is OK either way, and the original engineering used all LS.

Supply voltage is not an engineering problem.

23 Oct 82

Problem is definitely write related. Memory write fails and previous contents are still there. Where does it go??

1	FF3	31
1	FF4	59
1	FF3	17
1	FF4	BF
1	FF2	0F
1	FF4	4F
1	FF7	18

Ram test program R3.

Designed to allow detection of a mis-write. Checks until error then calculates syndrome of memory. Syndrome will reveal if and the address of an extraneous write.

H00 → no errors, no extra writes

LS00 → 57A9 error

17A9 extra write

57A9 error

NO extra write

57A9 error

17A9 extra write (2C) in 17A9 07 error

57A9 error

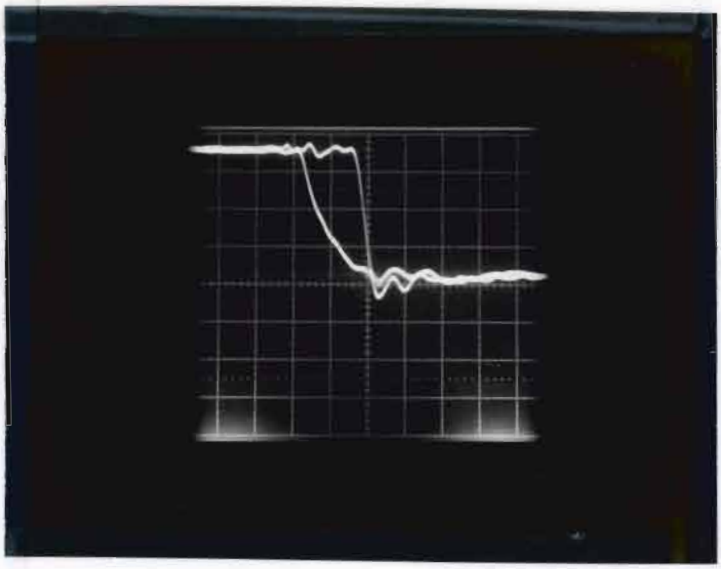
NO extra write

23 Oct 82

Changed to 74H89

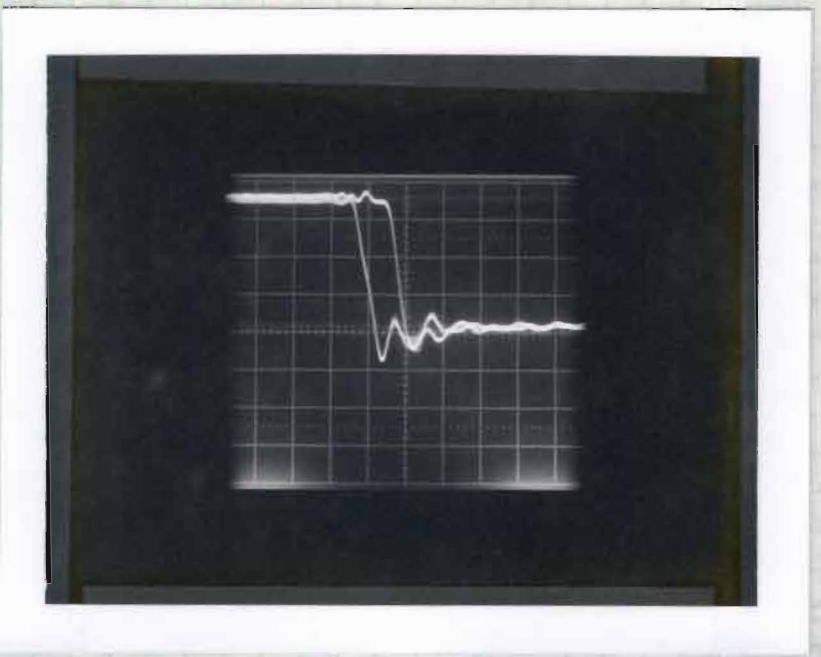
74S373 - low address

supply @ 5.0 V

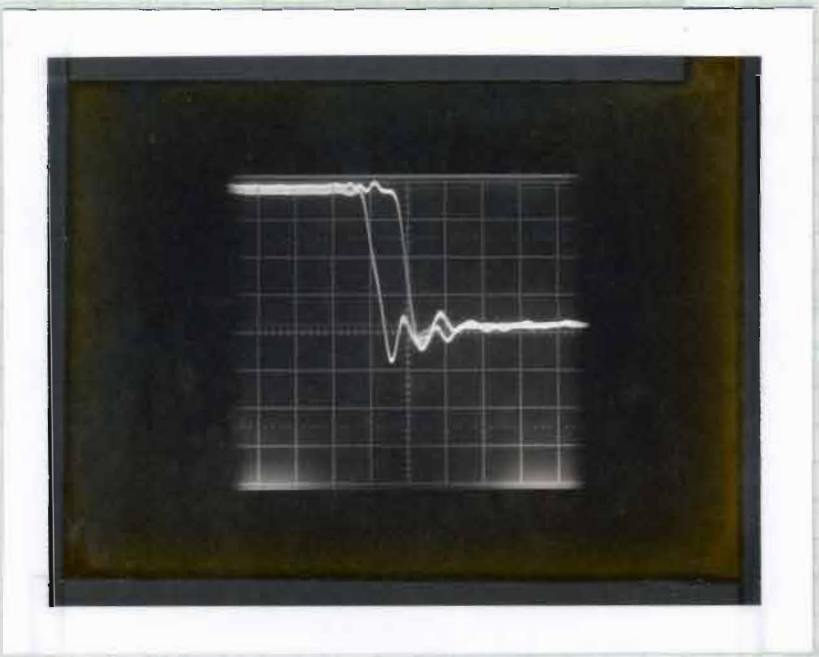


$\overline{RAS}$ & $\overline{CAS}$ 20ns/div 1v/div

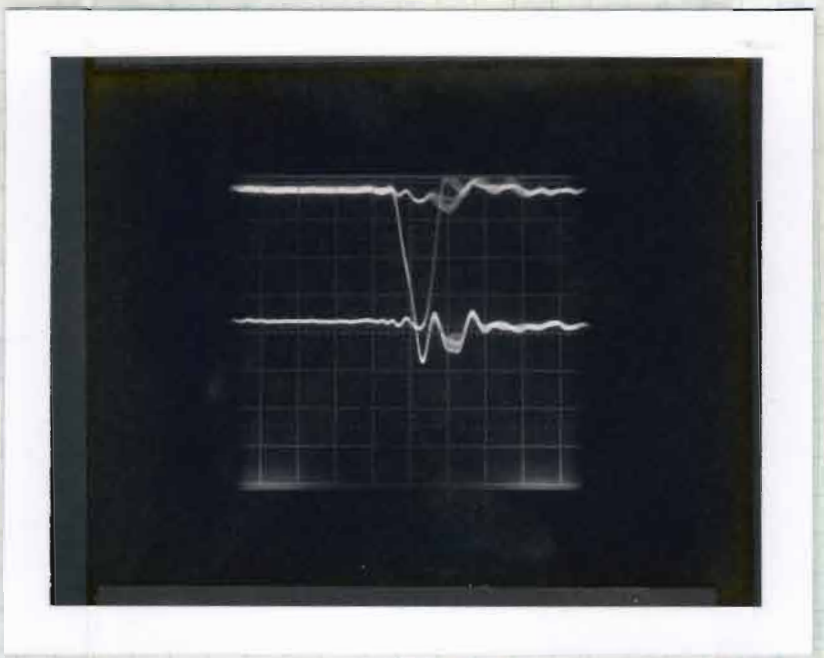
-RAS driver: 74LS00



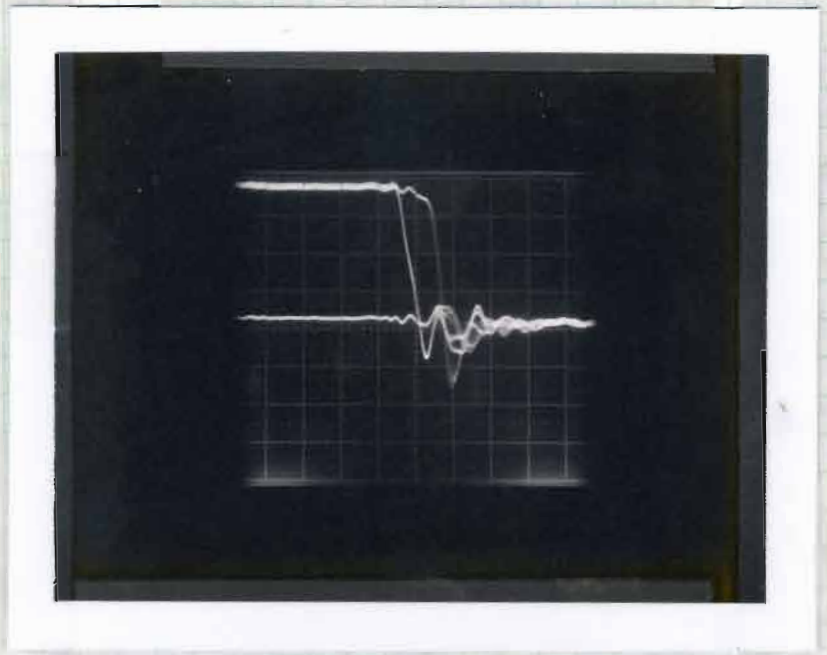
$\overline{RAS}$ & $\overline{CAS}$ 20ns/div 1V/div
using 74H00, 745373, 4.74 V supply



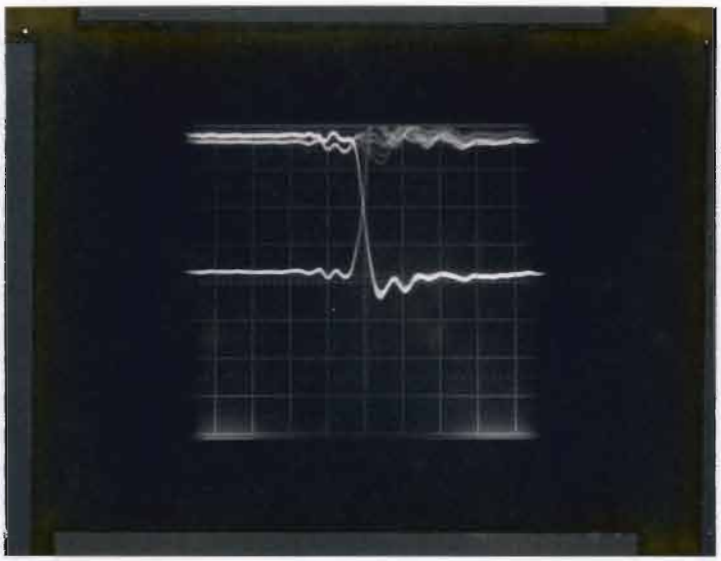
$\overline{RAS}$ & $\overline{CAS}$ 20ns/div 1V/div
using 74H00, 745373, 5.00 V supply



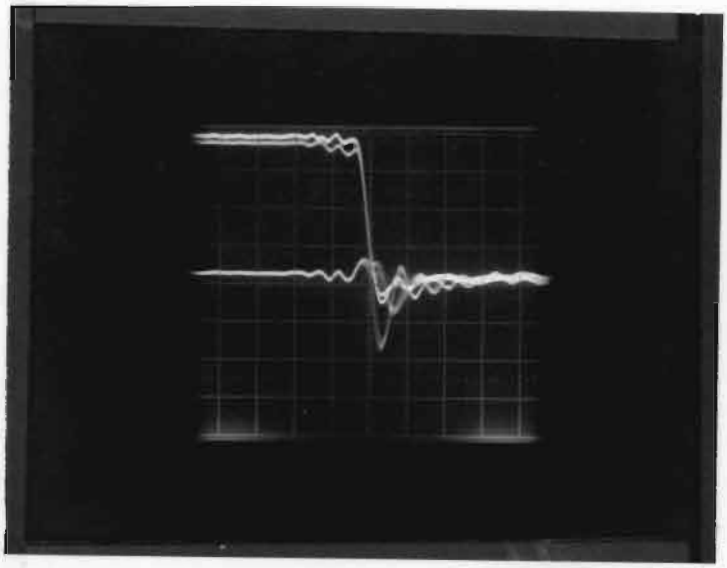
$\overline{RAS}$ & A$\emptyset$ 20ns/div 1v/div
74H$\emptyset\emptyset$, 745373, 5v supply



$\overline{RAS}$ and $\emptyset$ 20ns/div 1v/div
74H$\emptyset\emptyset$, 745373, 5v supply



$\overline{CAS}$ &and A$\emptyset$ 20ns/div 1v/div
74H$\emptyset\emptyset$, 745373, 5v supply



$\overline{CAS}$ & A$\emptyset$ 20ns/div 1v/div
74H00 & 745373, 5v supply

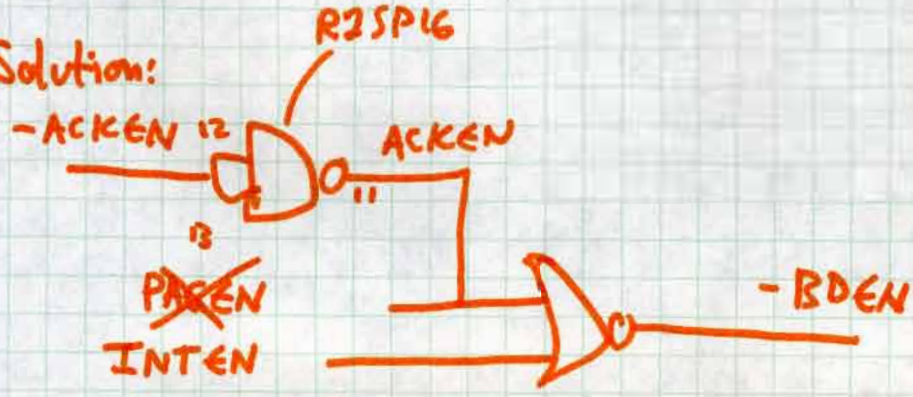
23 Oct 82

BFIB problem:

BFIB board screws up ram accesses to addresses XFFXX.

Problem: incorrect logic on BFIB board: output drivers gated with I/O address without I/O access:

Solution:



Added to BFIB to make BFIB2. Board changed. Untested.