HOMOGENEOUS MACHINE

CURRENT STUFF

The Homogeneous Machine was also called the Nearest Neighbor Concurrent Processor (NNCP) and later the Cosmic Cube

Contributions by:
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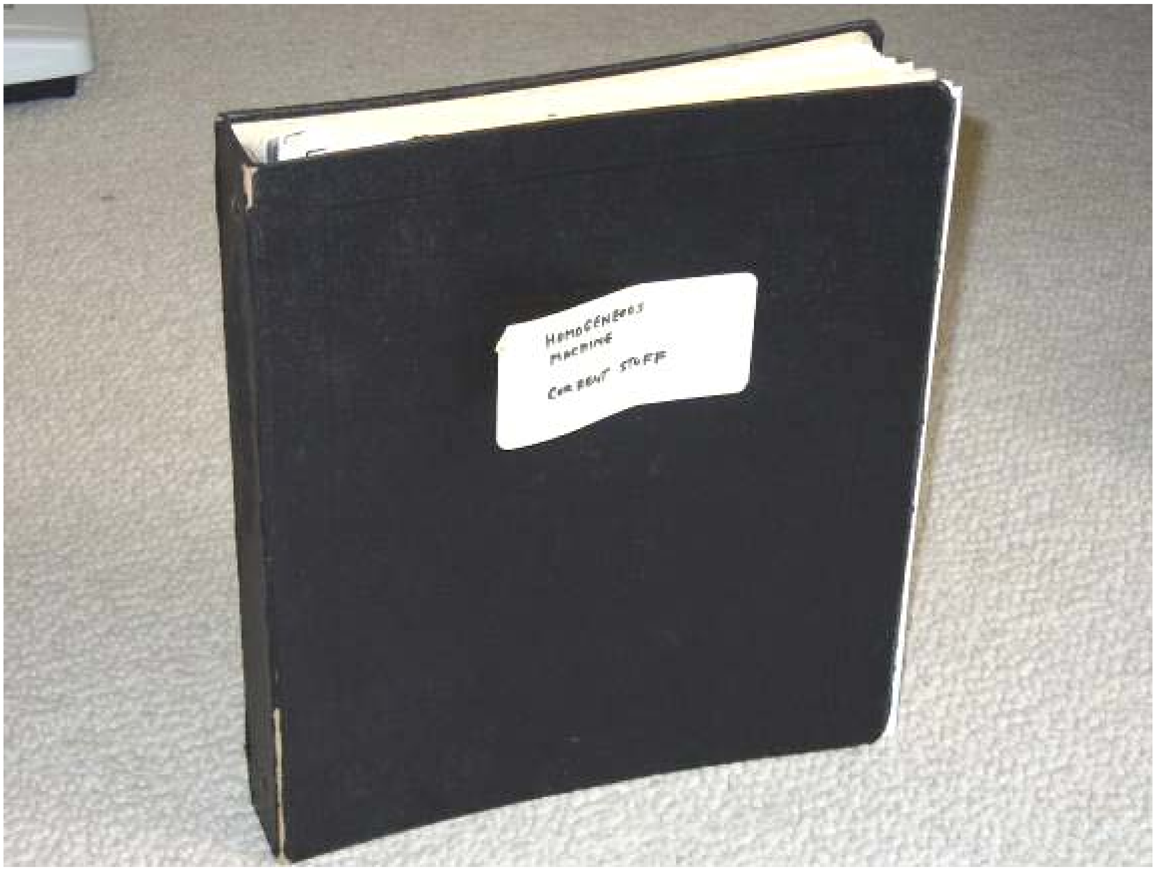

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HOMOGENEOUS MACHINE

TECHNICAL PLAN

9 January 1982

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Caltech Computer Science

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1. Introduction

This homogeneous machine project is a product of more than five years research in concurrent processing by two departments at Caltech. Research in concurrent computation in the computer science department started with theses by Browning [Browning 80] and Locanthi [Locanthi 80], and continues with a thesis in preparation by Dick Lang, and work by Chuck Seitz [Seitz 81]. All this research is shared an emphasis toward implemention with higher and higher density integrated circuits. The computer science department has been planning to construct a machine of the genere for several years.

Our colleagues in High Energy Physics have been plagued by a lack of suitable computing technology to solve some fundamental physics problems. In the course of our collaboration it became evident that our research had studied architectures of the sort ideal for their physics problems. Our collaboration with High Energy Physics has caused us to select some particular versions of the architectures that we have been studying as the most likely to be useful. Given our theoretical interest in the architectures and the practical use sought by High Energy Physics we have decided to act now to construct a homogeneous machine.

This document describes the plan of the computer science departement. The plan of High Energy Physics is described in [HEP 81].

1.1. The Proposed Machine

The homogeneous machine proposed here is a hypercube machine consisting of 64 identical microprocessors interconnected in a 1, 2, 3, and 6 dimensional array[1]. Each of the processors consists of about 77 chips, including a 8086 microprocessor, a 8087 floating point chip, 1/8th of a megabyte of RAM, and six bidirectional interfaces to other processors. The processors will be constructed on 64 printed circuit boards mounted in a custom backplane. The hypercube machine will consist of this array of processors and a single dedicated host processor that will control the array.

The class of problems that can be solved by such a machine is limited. There is absolutely no intention of the machine ever being able to execute a conventional program. Certain very limited classes of problems can be solved efficiently, and many of these problems are so large and important that a special purpose architecture is justified.

This paper will discuss the architecture, physical design, and some applications for a machine of this architecture.

2. Architectural Innovations

The architecture of the hypercube machine is new. Previous multiprocessors were constructed to allow direct implementation of many conventional computer programming constructs. These multiprocessors typically included special hardware to allow each processor access to the memory of others. Using the shared memory semaphores could be implemented, but only with extra hardware. The hypercube machine discards many of the

[1] All four dimensionalities can be obtained simultaneously with the proper structure.

conventional programming constructs, and the hardware to implement them.

2.1. Independence of Processors

A popular architectural direction in multiprocessor architecture has been to make a single sequential process execute faster by putting more processors onto the same memory. The results may be communicating sequential processes, as in C.mmp and CM*, or a high speed execution of a single sequential process, as in the dataflow machines of Dennis.

Tightly coupled multiprocessor architectures have a range of problems: the hardware cost grows faster than linearly with the size of the machine, and the efficiency of the software decreases as machine grows. The hardware will invariably contain a large switching network to route memory accesses or commands between arbitrary processors. A large switching network has a large parts inventory, and will operate slowly due to long wires and complex switching.

Research at Caltech indicates that architectures communicating through message passing have a brighter future than those with tight couplings or shared memory. Consider the effect of decreasing feature size on the design of a hypercube machine processor. Figure 1 shows the progress of the design from the present size of 50-77 chips/system to a one or two chip implementation a decade from now.

Feature Size	Chip Count
3 microns	50-77
1 micron	5-8
0.5 micron	1-2

Figure 1: Effect of Decreasing Feature Size on Processor Chip Count

Consider the advantages of a 1-2 chip/processor hypercube machine: 1) the processors would be very fast because of very few off chip delays, 2) chips would be interconnected very regularly and with very high density, and 3) the parts inventory would be small, i.e. one or two.

The hypercube machine connects processors with high bandwidth, but very loose connections. Each of the processors is quite small and standard, allowing maximal use of LSI 'glue' components. The compactness of the the system and short buses allows for high clock rates. In a nearest neighbor configuration[2] all wires are short.

2.2. Allocation of Memory

The trend in multiprocessor research is to move away from the single large computer to more and more smaller and smaller computers. This trend is almost valid because present mainframes are very much larger than an optimal computer. The trend can be followed too vigorously, however and produce computers that are too small to be cost effective.

Multiprocessors have been studied where the processors are too small. Two examples are the tree machine studied at Caltech [Browning 80] and the systolic array studied at CMU [Kung 80]. Both machines use processors that, in today's technology, would be less than one chip in size. The tree machine processors are programmable, containing about 1K bytes of RAM. The systolic array processors contain no program RAM, but are effectively programmed in their internal arithmetic layout.

[2] One (but only one) of the proposed network configurations.

In the process of tree machine research at Caltech, Browning and the author programmed a number of useful algorithms for the tree machine and studied their performance. A pattern was noticed in the results: tree machine algorithms tend to require as much time to load the problem into the machine and to unload the answer as is required to solve the problem[3].

Estimates of the necessary size of a tree machine required to solve a useful problem tend to be large. Tree machines too small to store an entire problem would have to solve a problem in parts, swapping the parts between a secondary storage and the tree machine. The effect of swapping is to degrade performance by orders of magnitude, making that an unreasonable alternative. The only solution is to make the machine large enough to store an entire problem. With only a fraction of their 1K byte storage available for data storage an unreasonably large number of processors are required.

The reason for this phenomenon is that the processors have so little memory that they cannot perform meaningful computation for very long. The solution to this problem for the hypercube machine is to reduce the number of processors and give each processor much more memory. The speed of the machine is reduced to a more reasonable level because the processors must multiplex their computations. Since a larger portion of the machine is low

[3] For example, sorting N numbers requires N steps to load the problem and N to unload the answer. Sorting is accomplished during the loading process where log N processors cooperate to load a number into the proper processor while maintaining proper order. The average number of sort operations performed by each processor is log N, whereas the number of steps to load and unload the problem is 2N.

cost memory, the cost of a machine required to perform a useful problem is reduced.

3. Potential Performance of the Hardware

Let us consider the economics of processing with an array of microprocessors operating concurrently. Another paper examines the question of whether full concurrency can ever be achieved, and also whether a large enough body of problems exist to justify constructing such a machine[HEP 81].

3.1. A Model of Computation

In this preliminary analysis we will adapt a very simple view of computation: we will assume that a problem solution requires some amount of memory, and that some number of operations are performed. Those problems that will execute efficiently on the hypercube machine will have the characteristic that they can be partitioned into a multiplicity of processors. In this partitioning, each processor will have a fraction of the total memory of the problem, and will perform the same fraction of the total operations performed in the problem. An array of *n* processors will be equivalent to a single conventional computer with *n* times the memory and *n* times the speed.

3.2. Cost/Performance

Let us consider compare the costs of such a machine and a conventional computer. The dominant cost in the hypercube machine is the cost of a single board that contains the basic processor. Let us examine the commercial viability of a hypercube machine by estimating the market cost of a hypercube machine and comparing its performance with competitive products.

Since the single board of the hypercube machine would be produced in such large volume, its cost would follow the same economics as semiconductor RAM systems today. We will estimate the cost market of a hypercube machine by analogy to a large RAM system.

At today's market prices semiconductor RAM costs $15,000 per megabyte[4]. Semiconductor RAM boards usually consist of boards populated approximately 75% with 16K RAM chips. One megabyte of RAM would consist of 512 RAM chips and 170 support chips by the above model. The cost per chip is therefore $22.

The hypercube machine described in this paper consists of a processor with 77 chips. Each processor has a 0.5 MIP performance on normal instructions, a floating point speed of 20 uS, and 1/8 mB of memory. At $22 per chip the cost is under $1700 per processor.

A DEC 11/780 (VAX) has a floating point speed of about 1 uS, and could reasonably support 10 mB of memory. A machine in such a configuration would cost $400,000. If the same $400,000 were spent on hypercube machine processors at $1700 each, 235 could be purchased. A hypercube machine of 235 processors would have an equivalent floating performance of 0.1 uS, and 30 mB of memory.

[4] These prices include power supply and backplane.

A CRAY-1 has a floating point speed of 15 nS, and costs $15 million with a large amount of memory. To obtain the equivalent floating point performance with hypercube machine processors at 20 uS per processor, 1,333 would be required. These 1,333 processors would additionally have 166 mB of memory, much more than the CRAY-1, and would cost $2.2 million.

3.3. Long Range Projections

These prices are conservative. For example, approximately 2/3 of the chips (but less than 1% of the transistors) in the processor are SSI/MSI chips in the interprocessor interface section. Should a large effort be made to build such machines, these chips could be reduced to 1 or 2 LSI chips. Also, the processor used is the oldest 16 bit CPU and the floating point unit is the first constructed by the industry.

As discussed previously, improving technology will continue to decrease the number of chips per processor to a limit of one or two. Since the processors are so amenable to IC implementation, their price/performance will increase much more rapidly than average.

In summary, the hypercube machine being constructed at present has a potential price/performance that is about 7 times better than products available today. Even given a substantial inefficiency in software, the hypercube machine will be noticeably better and either a VAX or CRAY-1. Future improvements in microprocessor technology will drastically improve this already good situation. More efficient CPUs and floating point units, and special interprocessor communication chips should reduce price/performance by an order of magnitude.

4. An Overview of the Implementation

The hypercube machine can be divided into three parts for convenience of explanation: 1) the array of microprocessors, called the main processors, 2) the dedicated host, which controls the array and interfaces to 3) the host (or hosts), which are mainframe machines the perform compiling of code for the machine. Figure 5 is an overview of these parts and their interconnections.

4.1. Main Array of Processors

The main array is essentially a multi-dimensional array of microprocessors. With one exception, these are all identical processors that connect only among themselves in a tightly connected network. One of the processors has one extra connection, however that connects the array to the rest of the world.

All of the main processors are connected by a control bus. This bus allows sharing of functions that are same for all processors, such as clock and memory refresh. The control bus also provides a flexible but low bandwidth global communications capability for use by diagnostics and as a network-wide software debugging aid.

The processors are interconnected by fully asynchronous bidirectional connections. The hardware supports a 64 bit interprocessor message by generating interrupts only when complete messages can be input or output.

4.2. Dedicated Host

The dedicated host is the interface between the general purpose host computers and the array. The dedicated host interfaces to the array through one asynchronous connection and is the master of the control bus. The dedicated host also interfaces to the mainframe hosts and to console terminals.

In addition to serving as a hardware interface to the array, the dedicated host fulfills an important function in some algorithms, see [HEP 81]. For this reason, the dedicated host will have a substantial amount of RAM: 512Kb-1Mb.

An unsuspected function of the dedicated host is the running of diagnostics on the entire array. The dedicated host will have the ability to control the supply voltage and clock frequency as well as control the master reset and RAM refresh rate of the entire array. These abilities will aid diagnostic programs in locating faulty boards.

The present plans are to construct the dedicated host with the same CPU as the main processors, for reasons of software compatibility. Future plans may call for more than one dedicated host, or a processor that is faster than the main processors.

4.3. Mainframe Hosts

Since neither the array nor the dedicated host will have any secondary storage, they would be inappropriate for compilers. Compiling will occur on either the HEP VAX or the CS DEC-20 and the machine code will be downloaded to the dedicated host and then to the array. At present it appears that the CS DEC-20 will be used for assembly level system software developement and the HEP VAX will be used for applications programming in C.

5. Proposed Plan of Action

A project to evaluate this architecture will consist of three phases:

1. Construction of a 64 processor prototype array and dedicated host.

2. Development of system software.

3. Application of the machine to different problems.

4. Construction of a 1024 processor hypercube machine.

This document will be concerned only with items 1,2, and 4. Caltech's High Energy Physics group is eager to apply such a machine to real physics problems [HEP 81].

5.1. Current Status

Work has already begun on constructing the hypercube machine. Funds were provided in anticipation in the computer science ARPA budget for work on building a concurrent machine. These funds, amounting to a non-renewable $20,000, are being used at present. ARPA interest in the project is considerable, but in a general atmosphere of budget cutting, funds to construct a useful hypercube machine will be difficult to obtain. Additional funding is being persued with ARPA as well as with others.

As of January 1982 approximately 50% of the engineering has been completed. Engineering is proceeding on the remainder of the machine and will be completed before any additional funding could have an effect.

5.2. Timetable for Future Work

The only part of the machine that has not yet been funded is the construction of the actual array[5]. A proposed timetable for future work is shown below:

Phase I - 64 processor machine

1 September 1981
Project to build 64 processor test model of the hypercube machine begins. Hardware design and prototyping begins immediately.

1 January 1982 Working model of the main processor. Software development begins now.

1 March 1982 Design of main processor is complete and the design is submitted to a contractor for PC layout and fabrication of 64 units. A complete software model of the hypercube machine is complete, including the dedicated host and at least two main processors.

1 July 1982 Primitive system software is completed. Boards to construct a 64 processor array are delivered by the contractor. Boards are now assembled into an array and tested.

1 October 1982 64 processor system is fully operational. Programs of the approximate complexity of Laplace's equation run. A technology evaluation is performed to determine if better chips are available for any part of the system. If necessary, redesign begins.

Phase II - 1024 processor machine

1 March 1983 A potentially redesigned main processor is submitted to a contractor for construction of 1024 units. Some physics research problems should be complete by this time.

1 October 1983 1024 unit hypercube machine becomes fully operational.

[5] Other parts of the machine are used only in quantity one, and engineering prototypes will be used.

5.3. Cost Estimates

An estimate of the cost of constructing one hypercube machine processor and building it into a processor array is shown in figure 2.

It will be noted that in figure 2 the cost is largely influenced by the $400.00 cost of the 8087 floating point chip. As of January 1982 the 8087 chips are scheduled for delivery to suppliers on a 4-6 week basis at a retail cost of $400. It is expected that the price of these chips will drop very significantly in the following few months.

Besides the 8087, the price of other parts is dropping rapidly now. In particular, the 8086 processor and the 64K RAM chips should be available for less than the proposed price. Figure 3 is a prediction of the actual cost of producing the array on a per unit basis. These figures only are used in the later cost estimates.

Figure 4 is a schedule of the expenses that would be required to complete the project if funding were available.

Considerable graduate student and faculty interest has been expressed in the Computer Science Department in communications software for the hypercube machine. Funding of research in this topic can proceed after the machine is in operation. To get the machine into a basic operation it will be necessary to have a primitive network operating system and diagnostics. A manpower budget for this is included in figure 4.

Item	Quantity	Cost	Extension
Double sided PC board:	1	$50.00	$50.00
8087 floating point:	1	$400.00	$400.00
8086 microprocessor:	1	$100.00	$100.00
64K RAM (2164):	16	$14.00	$224.00
8529A interrupt:	2	$18.00	$36.00
74S225 fifo:	12	$4.50	$54.00
misc IC:	many	$40.00	$40.00
Share power supply (2A/5V)	1/10th	$300.00	$30.00
Share backplane	1/64th	$4000.00	$63.00
sub-total:			$997.00
Assembly and testing:		$250.00	$250.00
total:			$1247.00

Figure 2: Per Processor Costs

March 1982	$1200
March 1983	$800

Figure 3: Estimated Cost of the Main Processor on a Per Unit Basis

	Period		
	1-Mar-82-	1-Oct-82-	1-Mar-83-
	30-Sep-82	28-Feb-83	1-Oct-83
64 processor prototype:	$76,800		
(64 processors at $1200 each)			
1023 processor array:			$819,000
(1024 processors at $800 each)			
Staff (quantity):			
DeBenedictis	1	1	1
Graduate Student:			
Hardware work:	1	0	1
Software work:	3	4	3
Technical:			
Hardware work:	1	1	4
Software work:	1	0	0

Figure 4: Expense Schedule for Construction of the Hypercube Machine

HOMOGENEOUS MACHINE

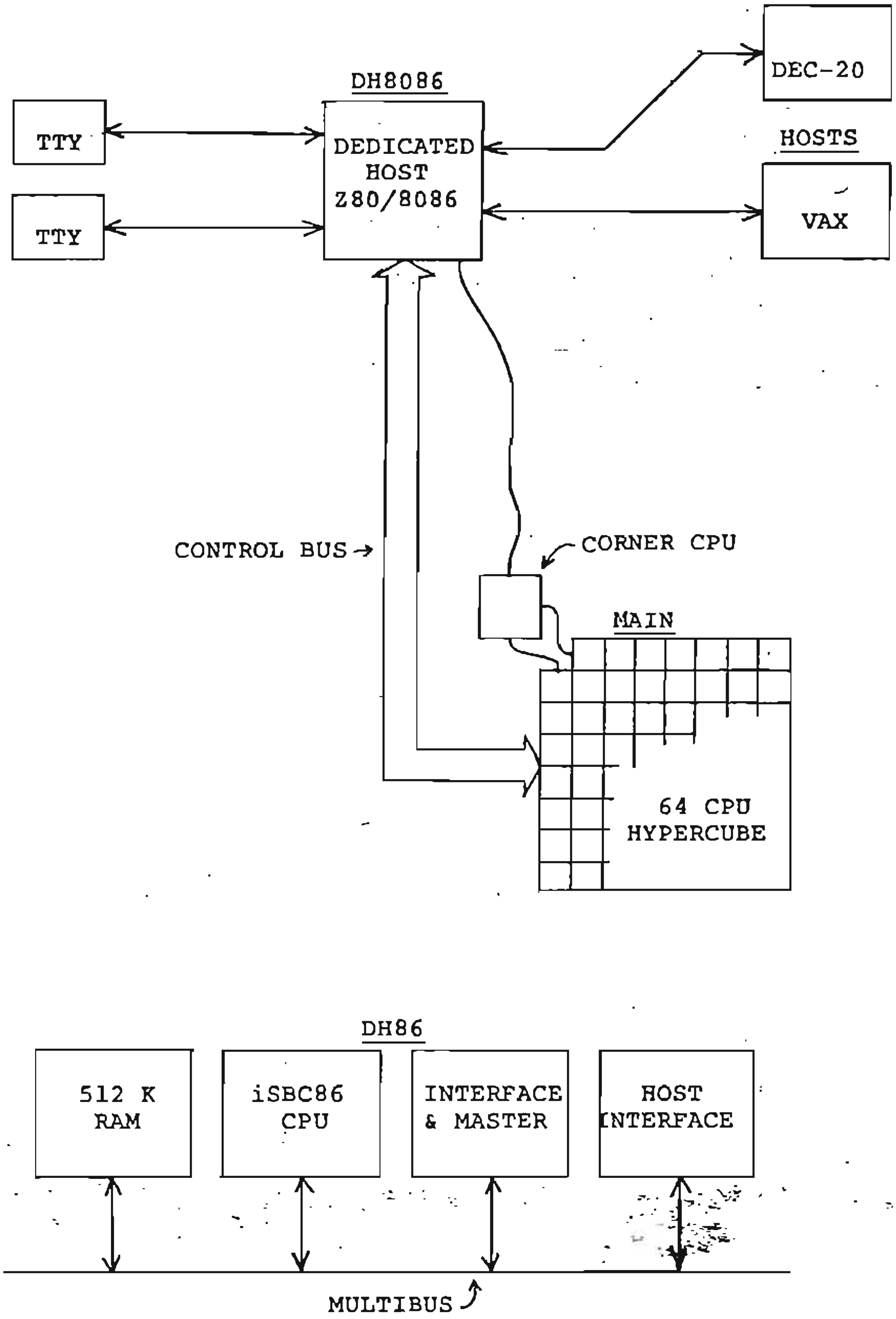

Figure 5: An Overview of the Hypercube Machine

Figure 6: Engineering Prototype of the Main Processor

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A Communications Operating System for the Homogeneous Machine

13 January 1982

Erik DeBenedictis

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1. Introduction

What communications primitives will be available to programs running on the homogeneous machine? One requirement is that the CPU overhead be low when the communications is simple (e.g. systolic). On the other hand, the communications must be general enough to support dynamically allocated processes (e.g. COPE). If a general communications strategy existed that was compatible with these requirements it could be implemented as part of the ROM resident operating system.

2. Types of Problems and Necessary Communications Capabilities

A spectrum of communications strategies have been proposed. Each strategy trades simplicity and efficiency for capability. These are listed below:

Systolic: In systolic communication both the sender and the receiver must be waiting on the same communication event for the event to proceed. Systolic communication is modeled by two monitor calls: one to send a message over a particular channel, and one to receive a message. The characteristics of the calls is that they hang until function can be completed, locking out any other processor activity. No interrupts are required.

Processor Directed: In processor directed communication each message is accompanied by a specification of the processor that is to receive it. When a message enters a processor that message is either delivered to the program running in that processor or relayed to another processor. If relaying must occur the operating system decides which link is most appropriate to forward the message. Queueing can be implemented for relayed messages and/or for messages destined for the processor. Interrupts are required.

Process Directed: In process directed communication there may be more than one process in each processor. Furthermore, processes may move around between processors. Communication is directed to a particular process, even though the processor where that process is currently resident may not be known. Implementation of this scheme is very involved.

3. Processor Directed Communication

Processor directed communication offers extremely high speed and sufficient generality to be the best choice.' The communications primatives appropriate for this type of communication are shown below:

int outA(Dest) — Specifies a message to another processor. Dest is the destination processor (0-63).

int outB(Buf,Len) — Sends message data to the selected processor. Buf is pointer to an integer array that contains the information to be transmitted. Len bytes starting at Buf are transmitted. The value returned is 0 if the transmission was successful or -1 if output buffer space was full.

int inA() — Receives a message. The value returned is the identification of the sending processor, or -1 if no message was available.

int inB(Buf,Len) — Receives a message. Buf is a pointer to a Len word block where the message is deposited. If the remaining message is longer than the buffer, the buffer is filled with as much of the message as possible and 0 is returned. If the message fits in the buffer, the number of bytes transferred is returned.

4. Deadlock

Deadlock can potentially occur for two reasons: 1) the user program assumes too much queueing, or 2) the message passing system deadlocks. The following rule will prevent a user program from deadlocking:

User program deadlock prevention rule:

> A user program may not wait on a failed out call unless in calls are processed during the wait.

The message passing system uses a deadlock free routing algorithm. This algorithm is described below (refer to figure 1 for notation):

```
    +------------------------------------------->110010
    |       +----------------------------------->000010
    |       |       +--------------------------->011010
    |       |       |       +------------------->010110
    |       |       |       |       +----------->010000
    |       |       |       |       |       +--->010011
    |       |       |       |       |       |
+-----------------------------------------------+
|   a       b       c       d       e       f   |
| link    link    link    link    link    link  |
|                                               |
|              processor (010010)               |
|      (a,b,c,d,e,f) is (0,1,0,0,1,0)           |
+-----------------------------------------------+
```

Figure 1: Notation Concerning Processors in a Hypercube

- Let processors be identified by their coordinate in the hypercube: (a.b.c.d.e.f). The letters a.b.c.d.e.f are either zero or one, and are transmitted as a binary number abcdef.

- Let the links to other processors be labeled a, b, c, d, e, and f. The labeling is chosen to correspond to the bit labeling of the previous paragraph. (I.e. the processors on either end of link c have identifications that differ only in the c bit.)

- When a message is available from a link the identification of its destination processor is analyzed before it is removed from the input queue. Analysis consists of XORing the destination processor identification with the identification of the processor with the message and performing one of two functions:

  1. If the identifications are the same then the message is destined for that processor. The message is made available for input. If the input buffer is full, the operating system runs the user program until that is no longer so.

  2. If the identifications are different then the message must be forwarded. The link to forward is determined by the following algorithm: the leftmost bit in the difference is located and that determines the forwarding link.

This system does not deadlock for the following reason: If a message arrives on link f (least significant bit) then it must be destined for that processor. This is true because to be forwarded to link f by the previous processor all other bits must match. The user program on the processor must remove the message eventually. The system therefore cannot deadlock with messages in link f.

Now consider link e. If a message has arrived in link e, bits a-e must match. If bit f matches then the message can be made available for input and there is no problem. If bit f does not match the message is forwarded to link f. Since the system cannot deadlock with a message in link f, it will not deadlock in this condition. Therefore the system will not deadlock with a message in link e or f.

By induction, it has been proven that all links to the right of link x do not deadlock. If a message arrives on link x then it is known that all bits to the left and including x match. Therefore the message will either match exactly, or it will be forwarded to a link to the right of x. If an exact match occurs, the message is consumed by the user program. If the message is forwarded deadlock cannot occur because all links to the right of x do not deadlock. Therefore, link x does not deadlock.

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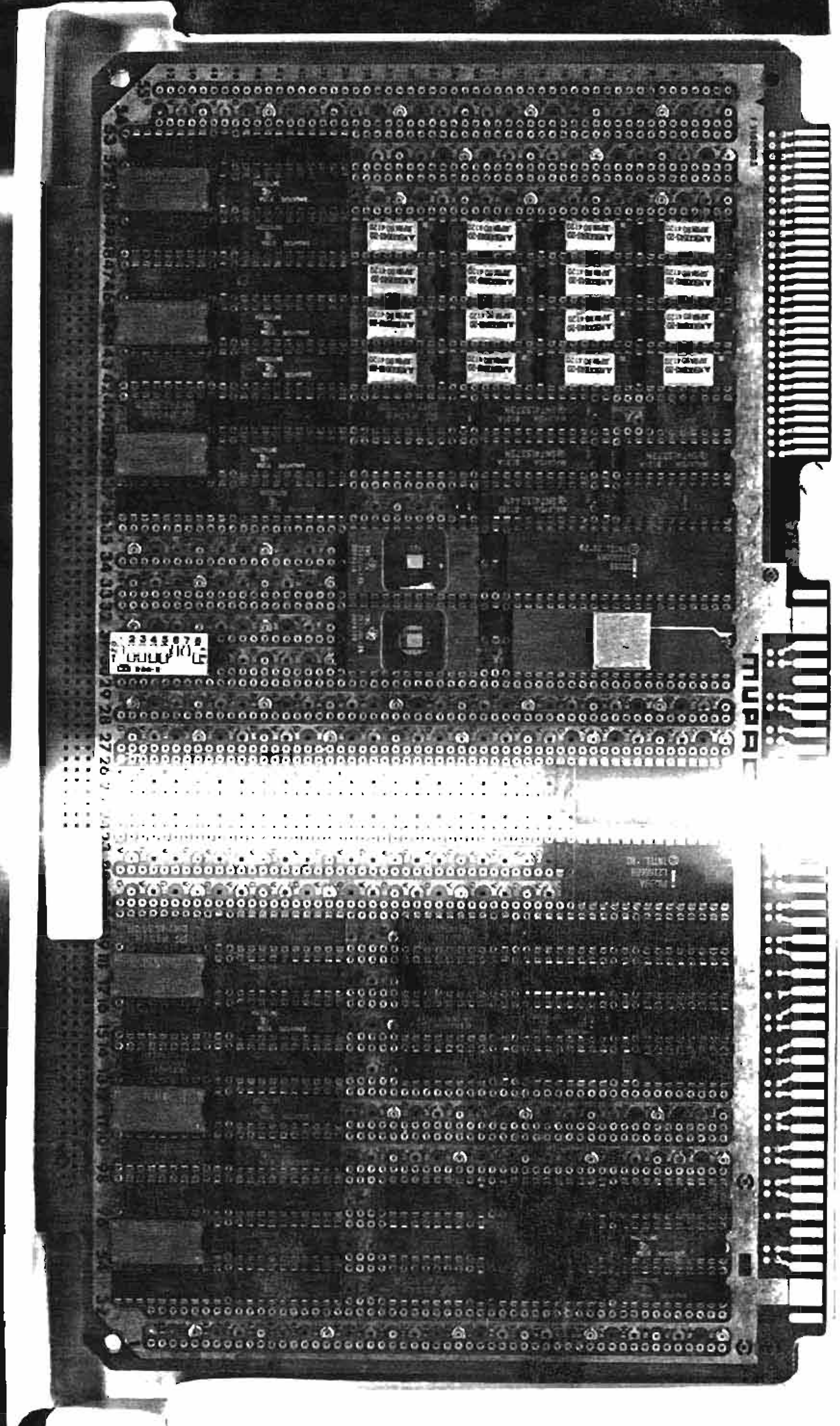
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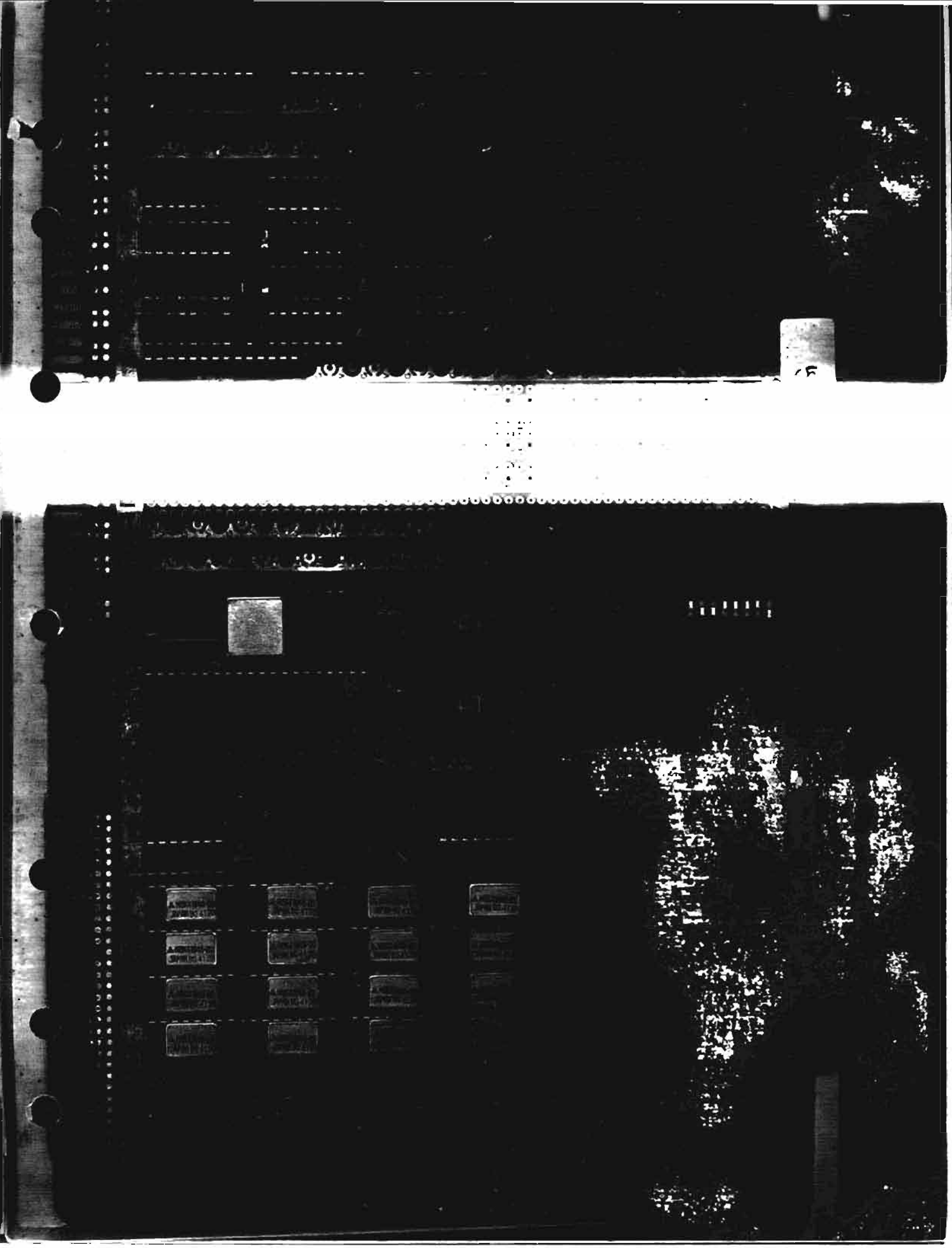

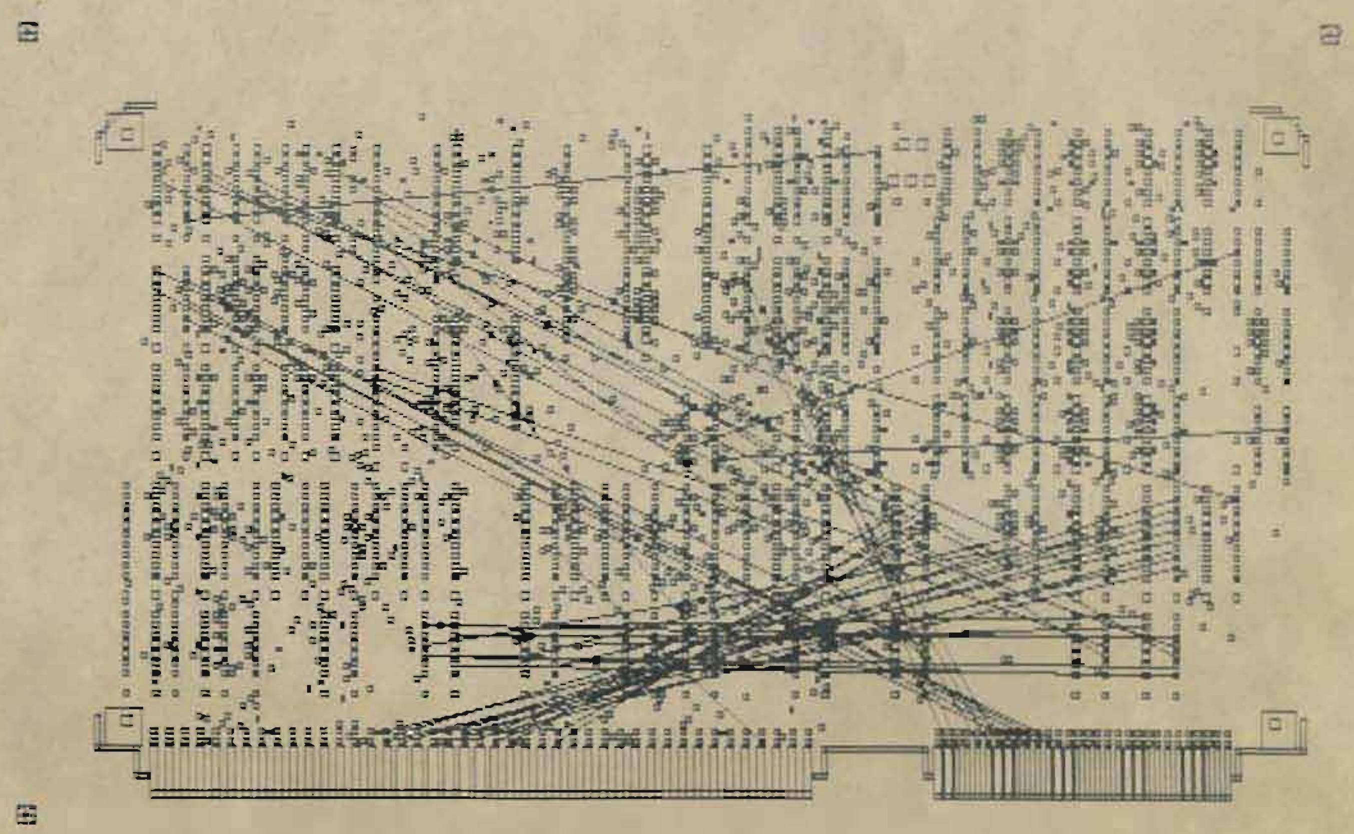

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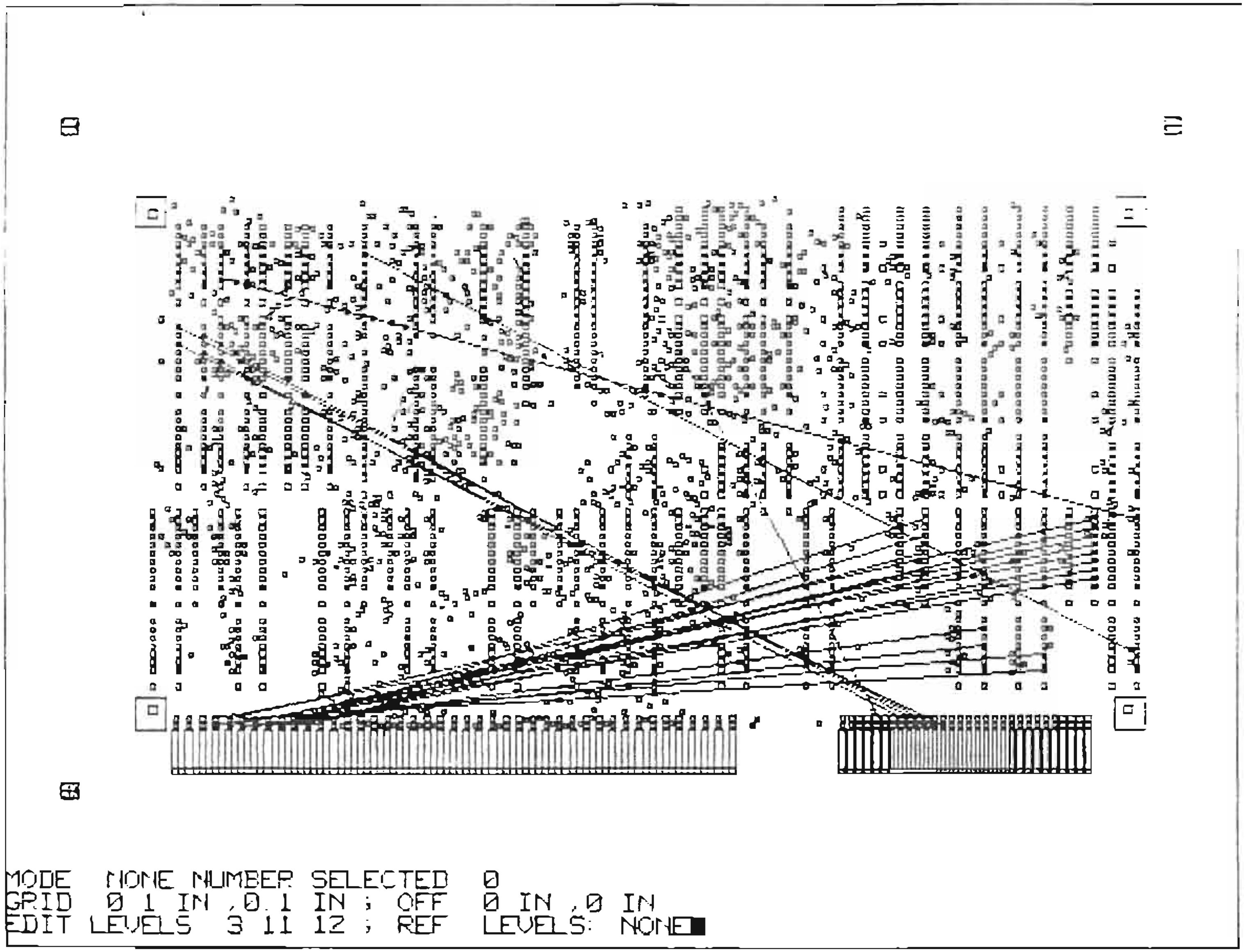

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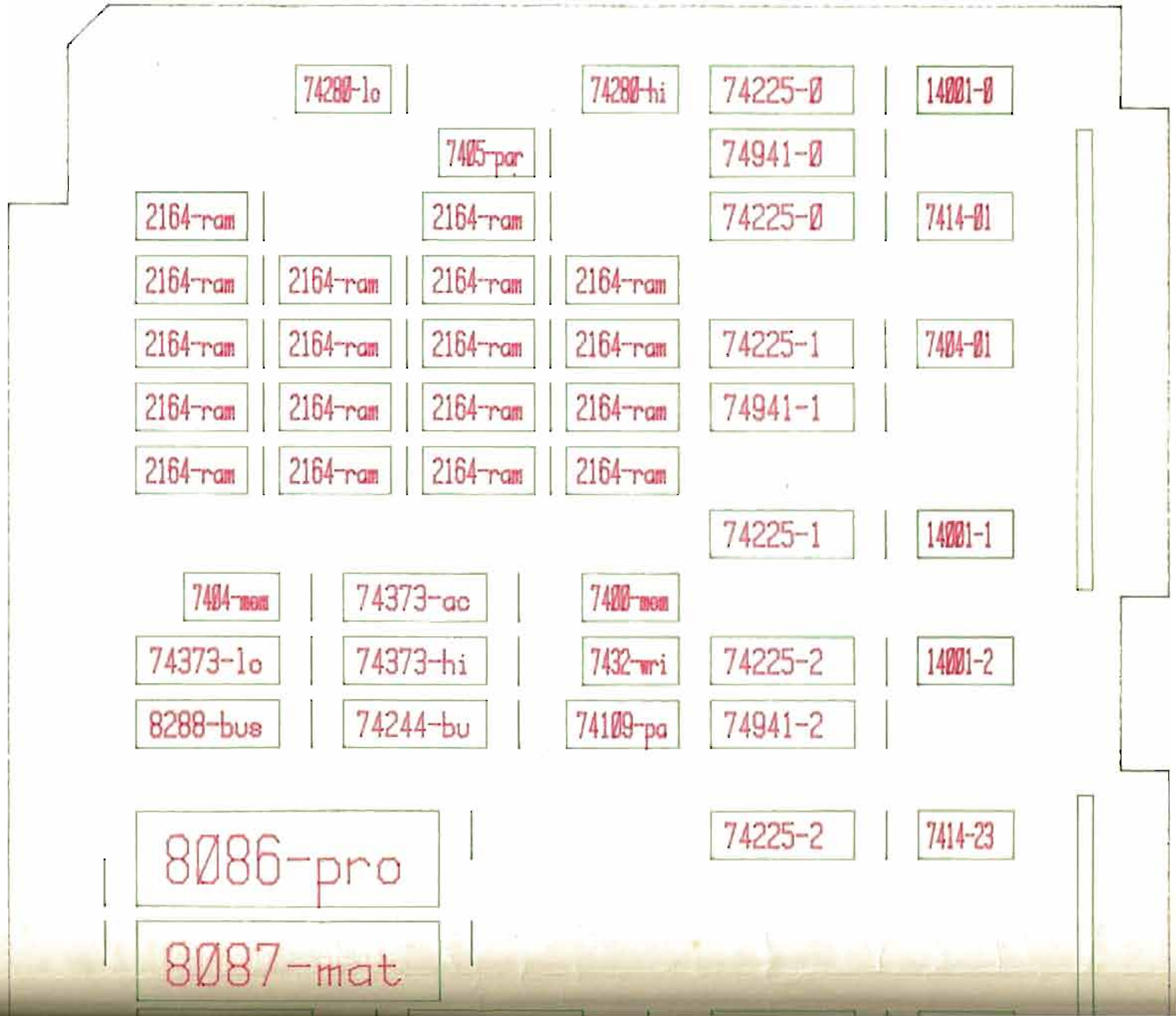
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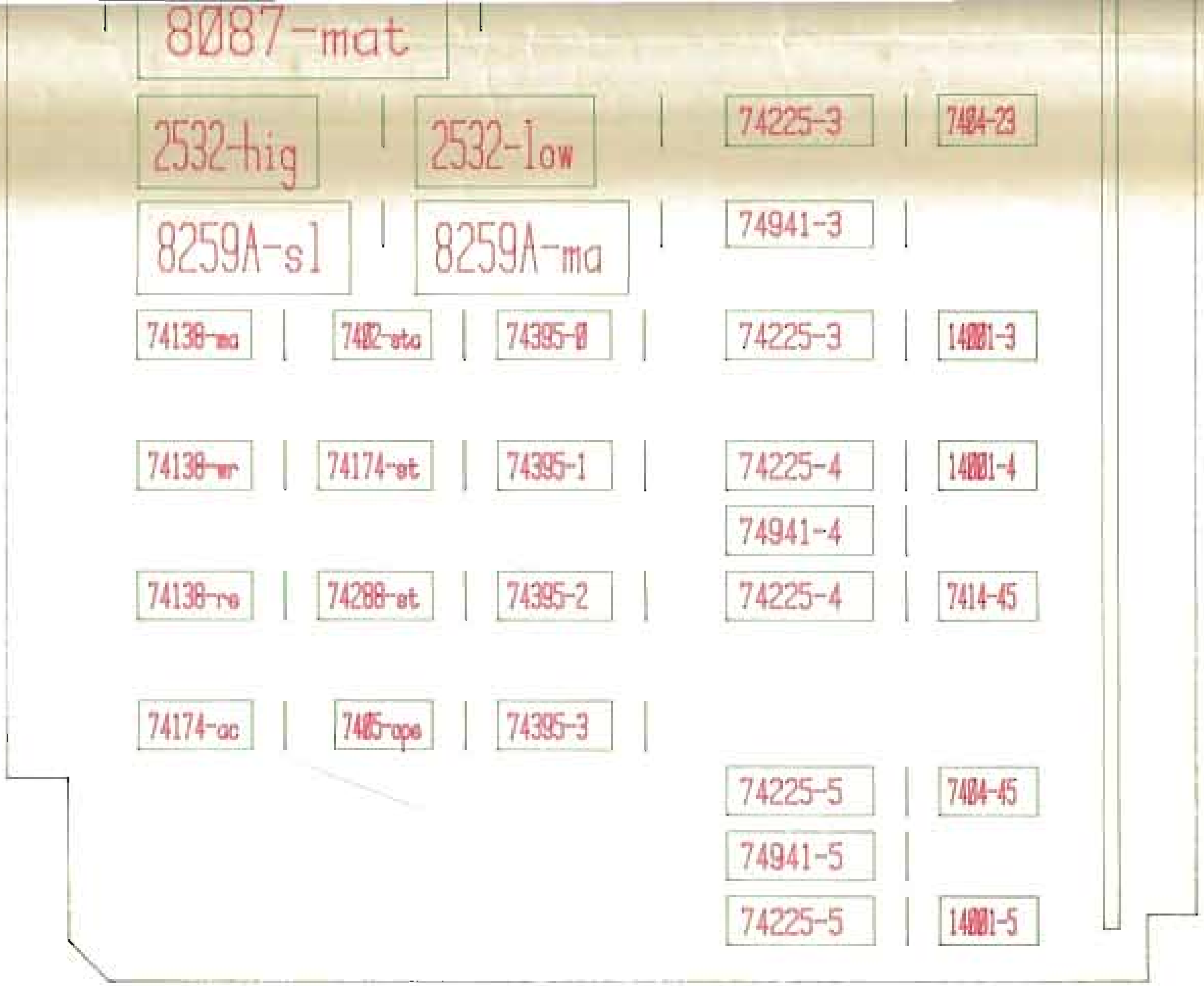
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74395-1
74225-4
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74941-4
74138-re
74288-st
74395-2
74225-4
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74174-ac
74Ø5-ope
74395-3
74225-5
74Ø4-45
74941-5
74225-5
14ØØ1-5

12 char max (6)

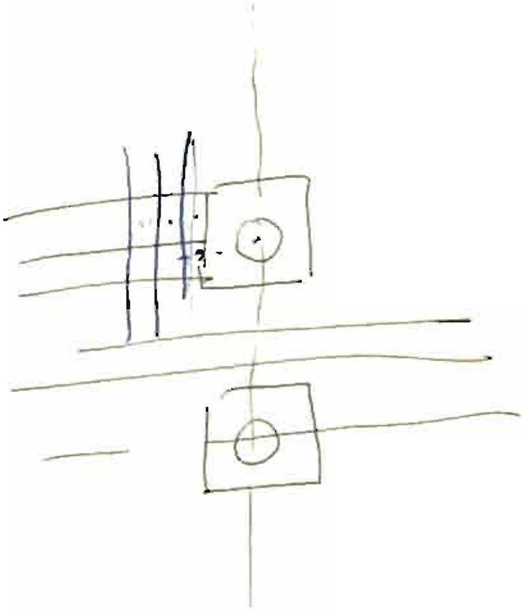
VCC

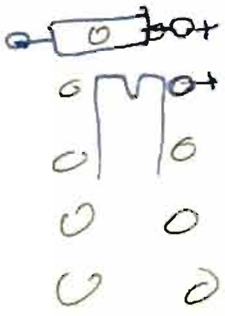
GND

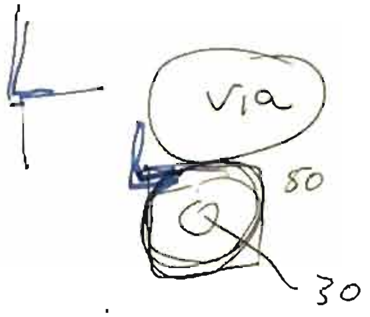
no numeric first

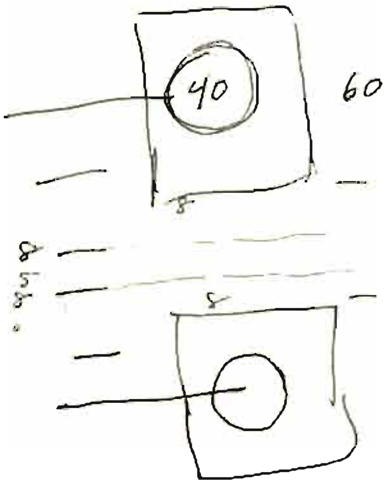
no NC - just delete.

pin #'s Uxx - Ø4







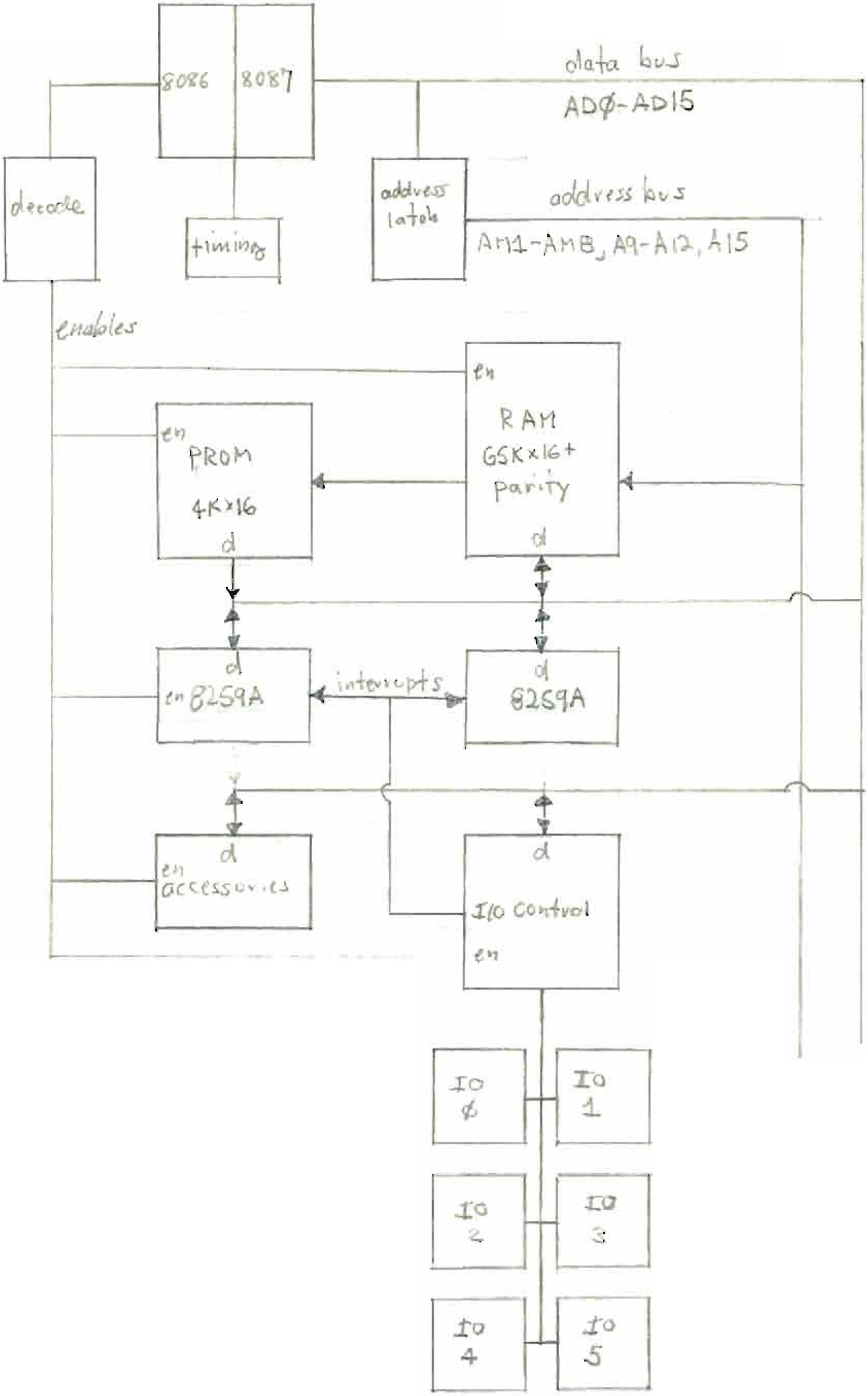


40 mils

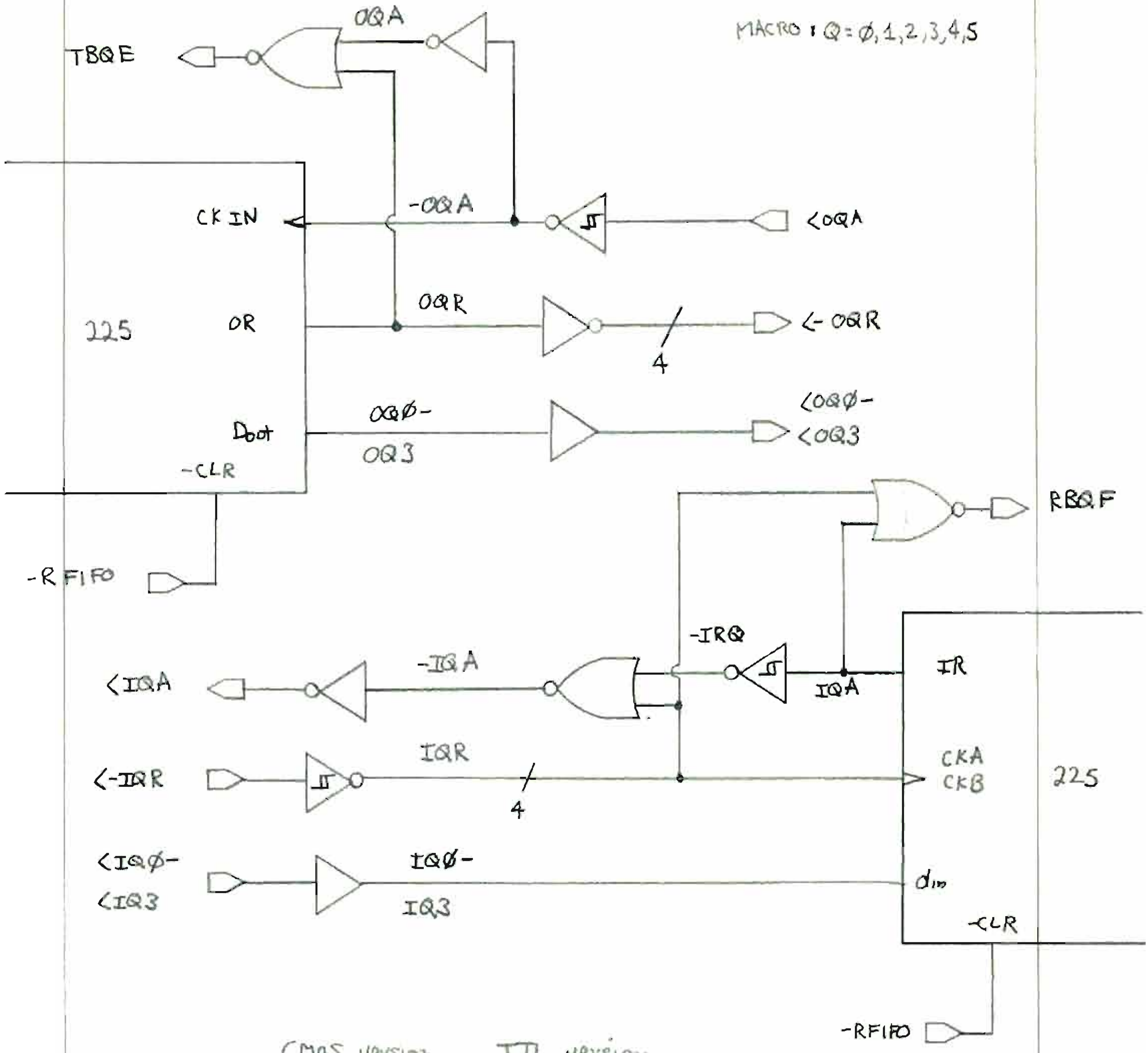
National Technology
Santa Ana.
mass prod of multilayer ~ 8 mil.

[illegible]

MNCP Node, Overview

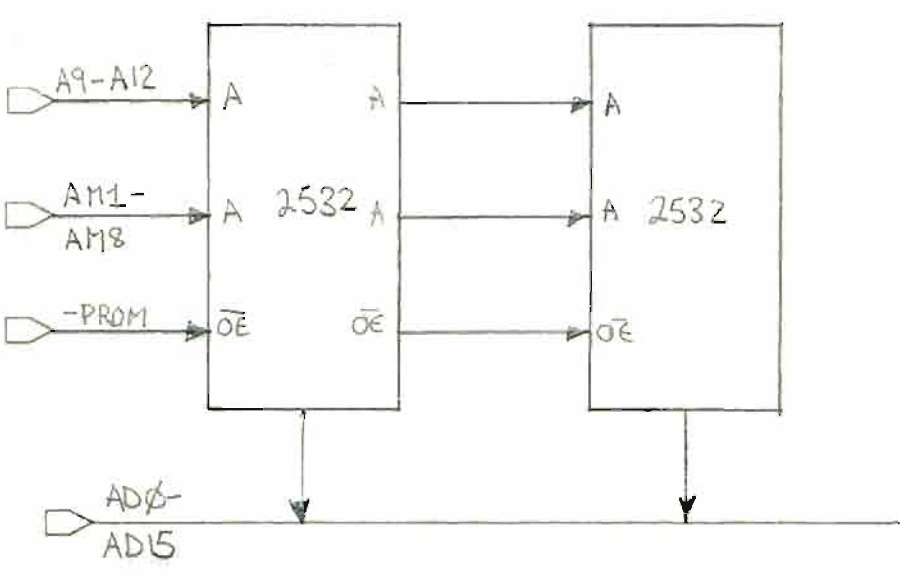


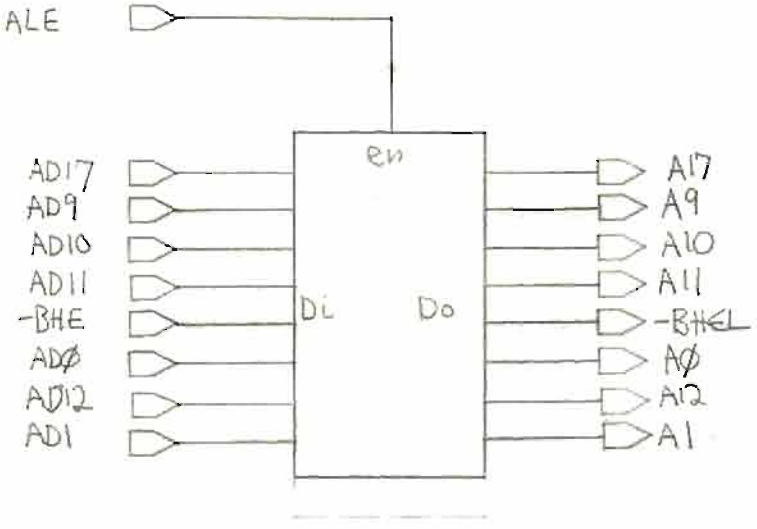
FIFO EXTERNAL



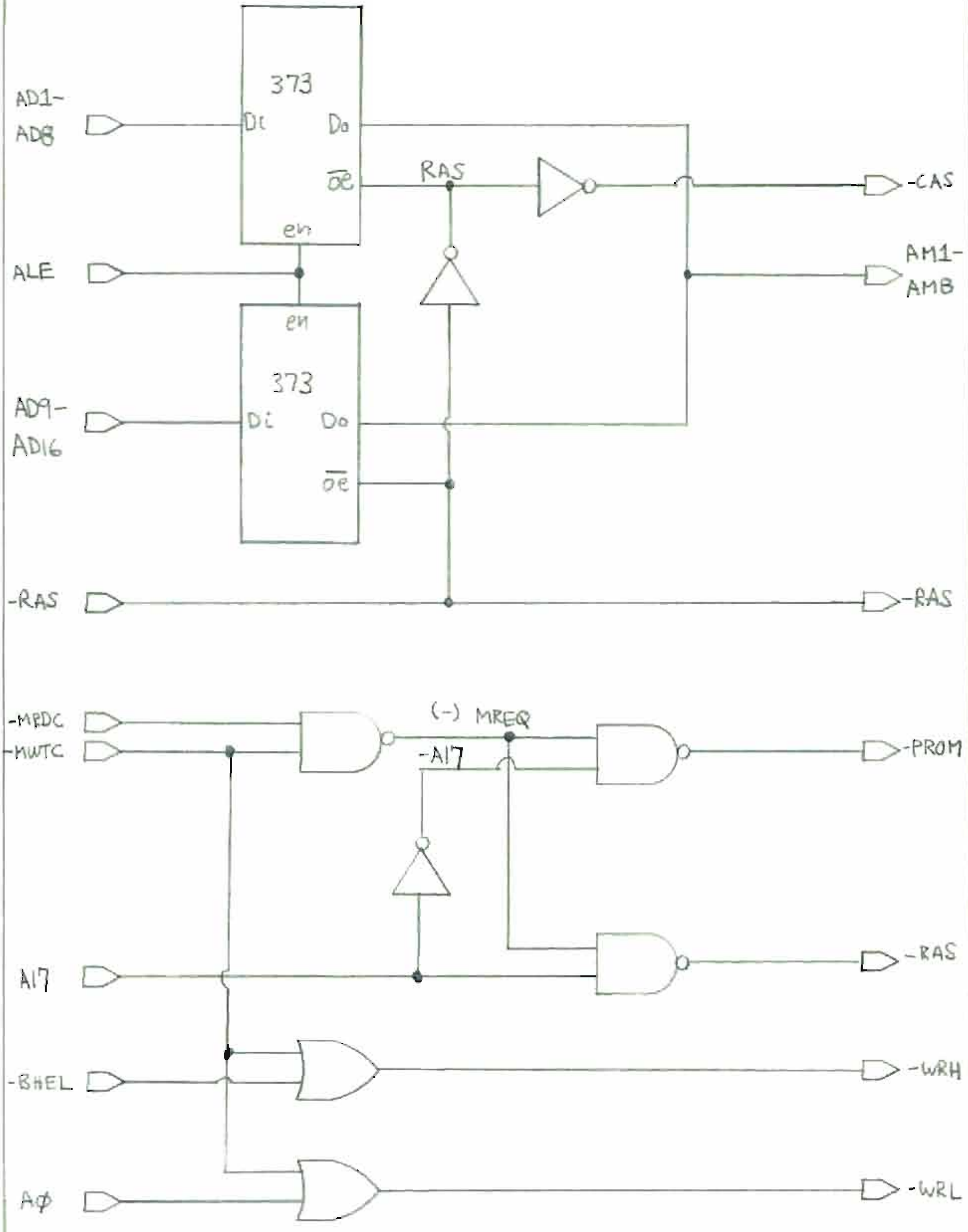
	CMOS version	TTL version
Schmitt	74LS14	74LS14
Buffer	74C941	74LS244
Nor	4001	4001
Inverter	4069	74LS04

PROM / ADDRESS

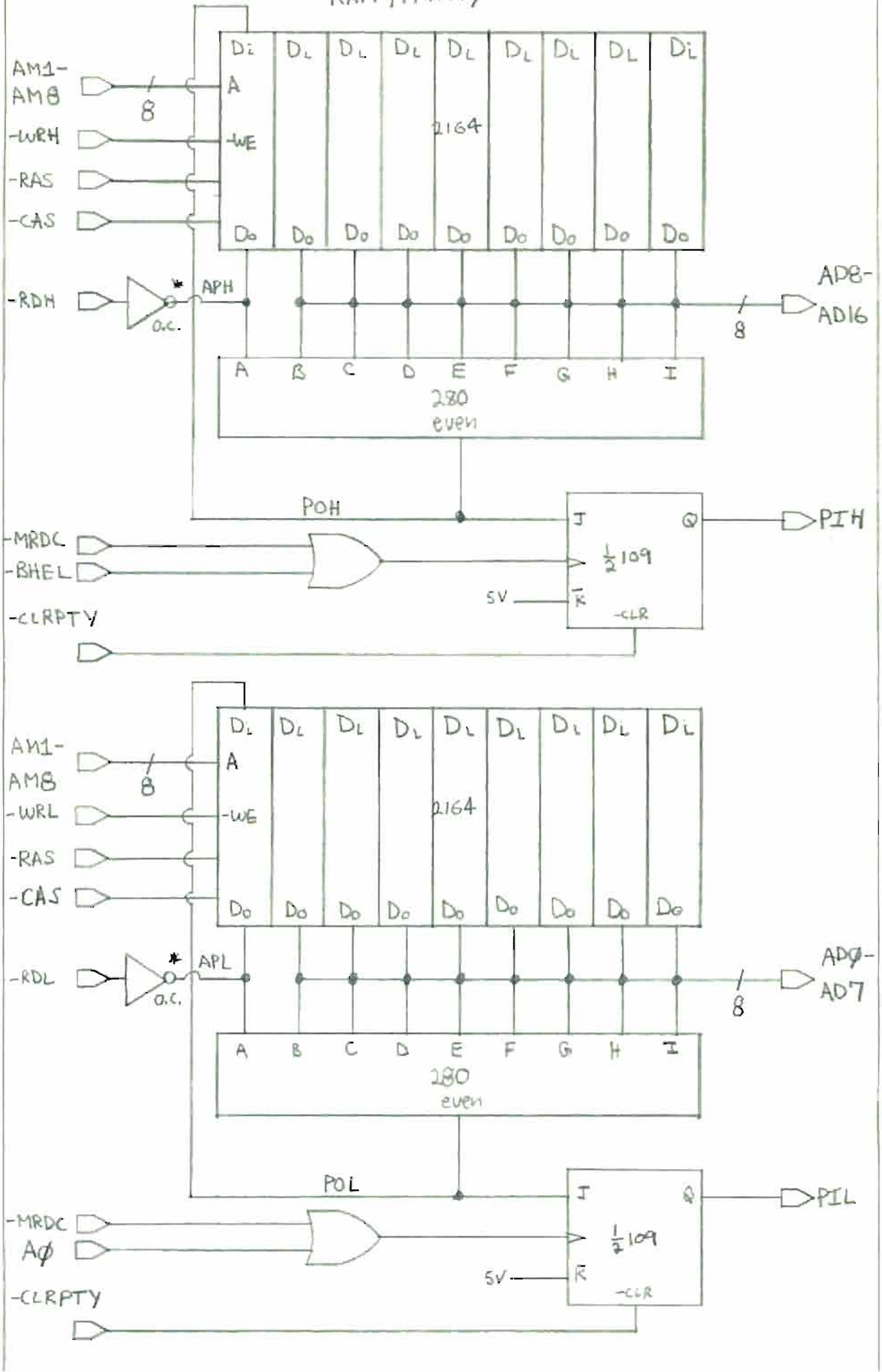




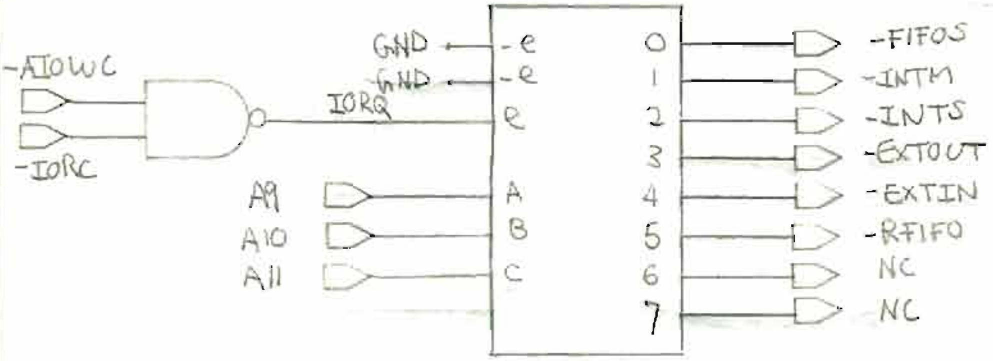
TIMING


AD1-
AD8
373
Di
Do
oe
en
RAS
-CAS
ALE
AM1-
AMB
en
373
AD9-
AD16
Di
Do
oe
-RAS
-RAS
-MRDC
-MWTC
(-) MREQ
-A17
-PROM
A17
-RAS
-BHEL
-WRH
Aφ
-WRL

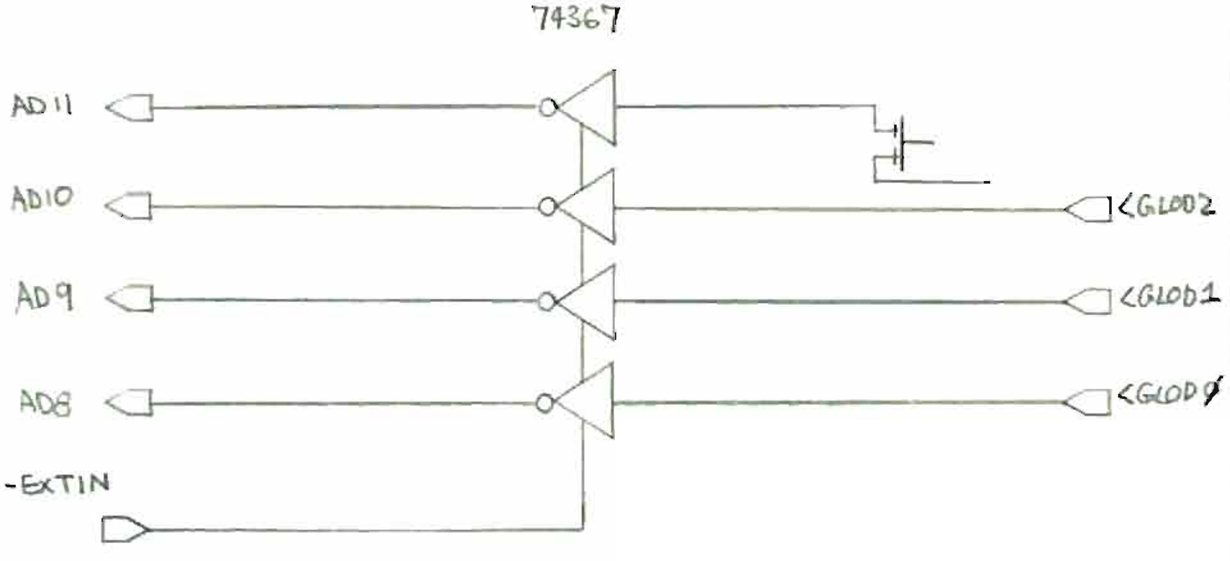
RAM /PARITY

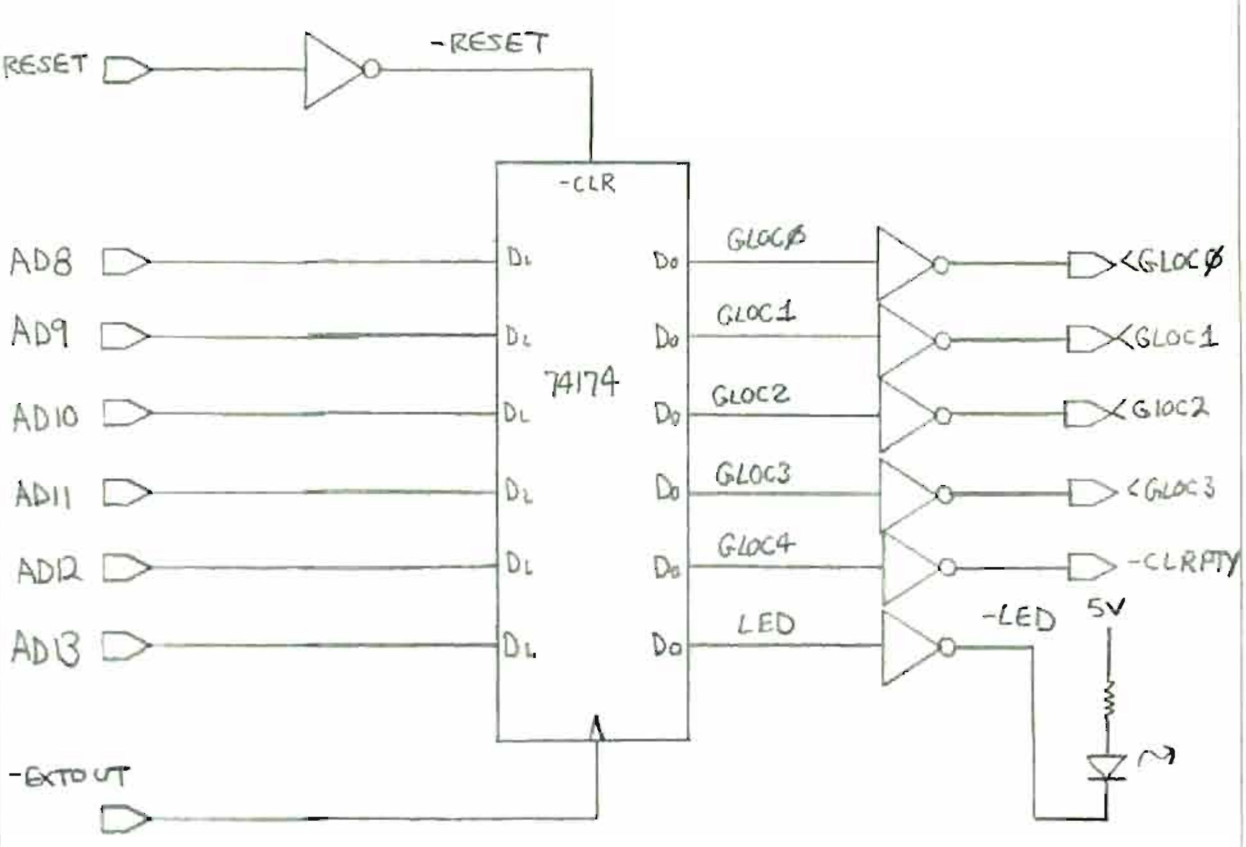

AM1-
AM8
8
-WRH
-RAS
-CAS
-RDH
O.C.
*
APH
Di
DL
A
-WE
2164
Do
AD8-
AD16
8
A
B
C
D
E
F
G
H
I
280
even
POH
J
Q
PIH
-MRDC
-BHEL
1/2 109
5V
K̄
-CLR
-CLRPTY
AM1-
AM8
8
-WRL
-RAS
-CAS
-RDL
O.C.
*
APL
DL
A
-WE
2164
Do
AD∅-
AD7
8
A
B
C
D
E
F
G
H
I
280
even
POL
J
Q
PIL
-MRDC
A∅
1/2 109
5V
K̄
-CLR
-CLRPTY

IO DECODE

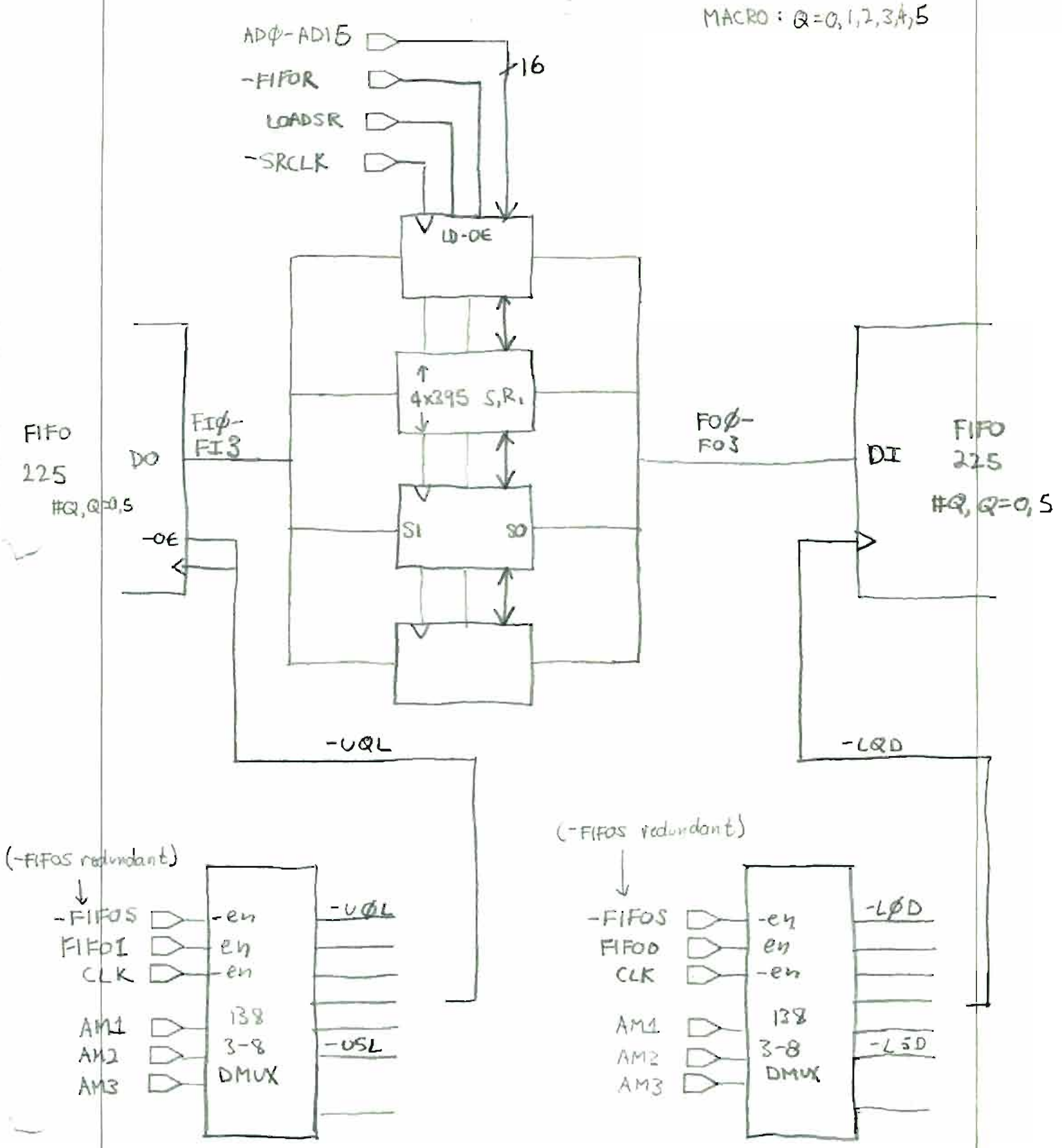

-AIOWC
-IORC
IORQ
GND
GND
-e
-e
e
A9
A10
A11
A
B
C
0
1
2
3
4
5
6
7
-FIFOS
-INTM
-INTS
-EXTOUT
-EXTIN
-RFIFO
NC
NC

ACCESSORIES

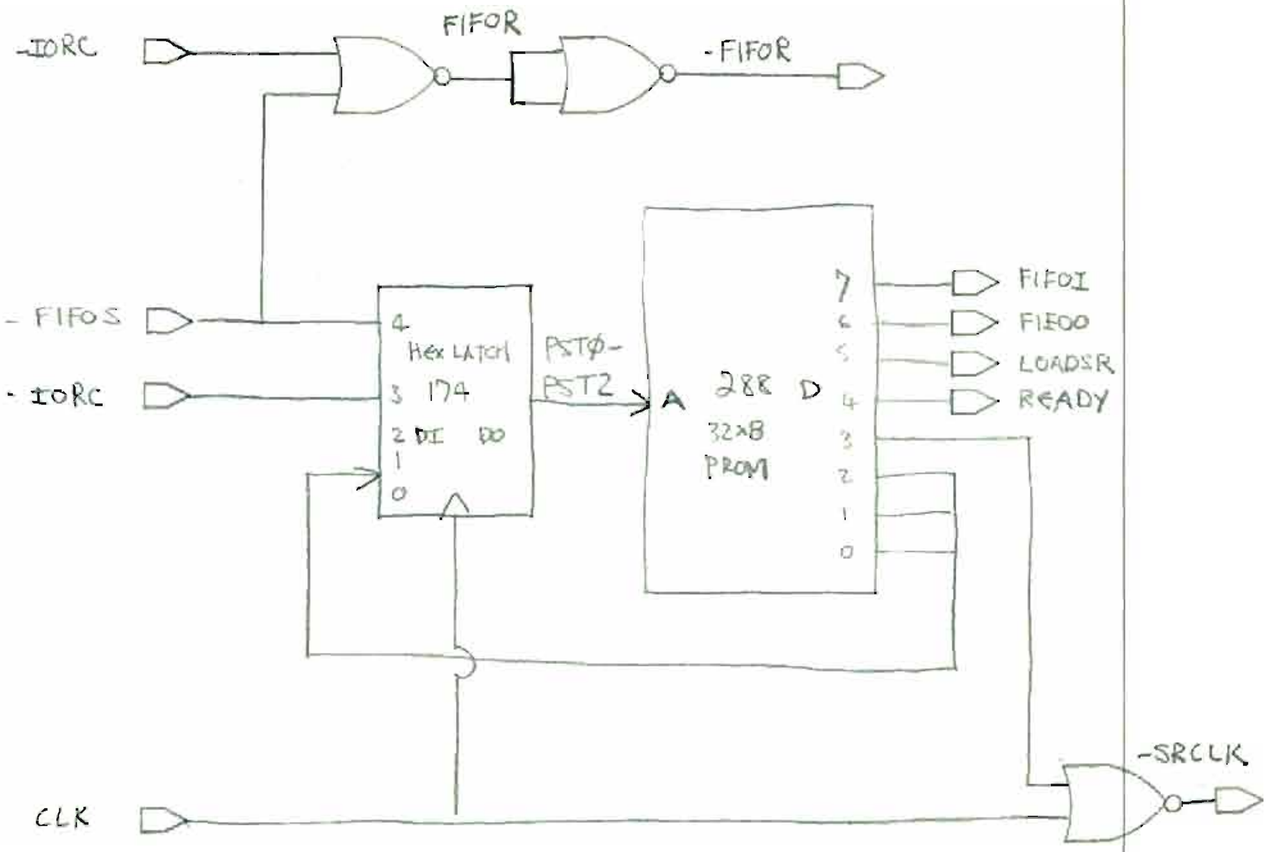




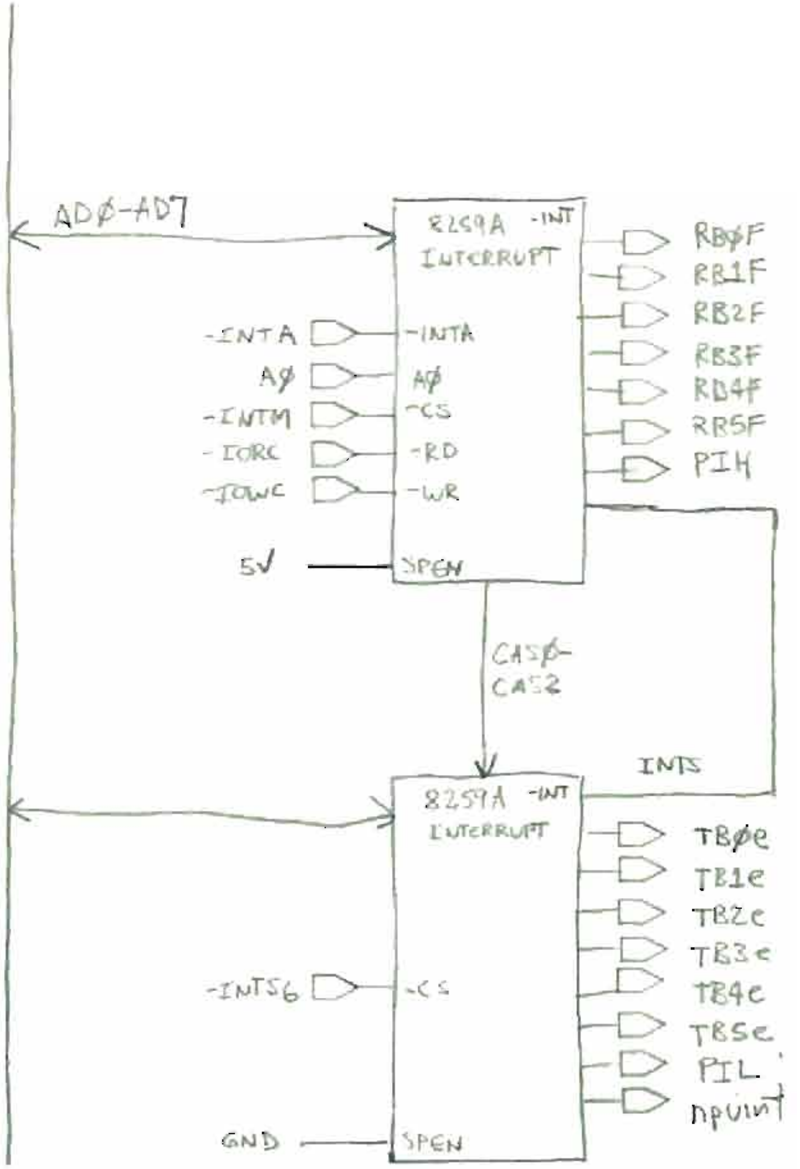
FIFO 4-16-4 Converter



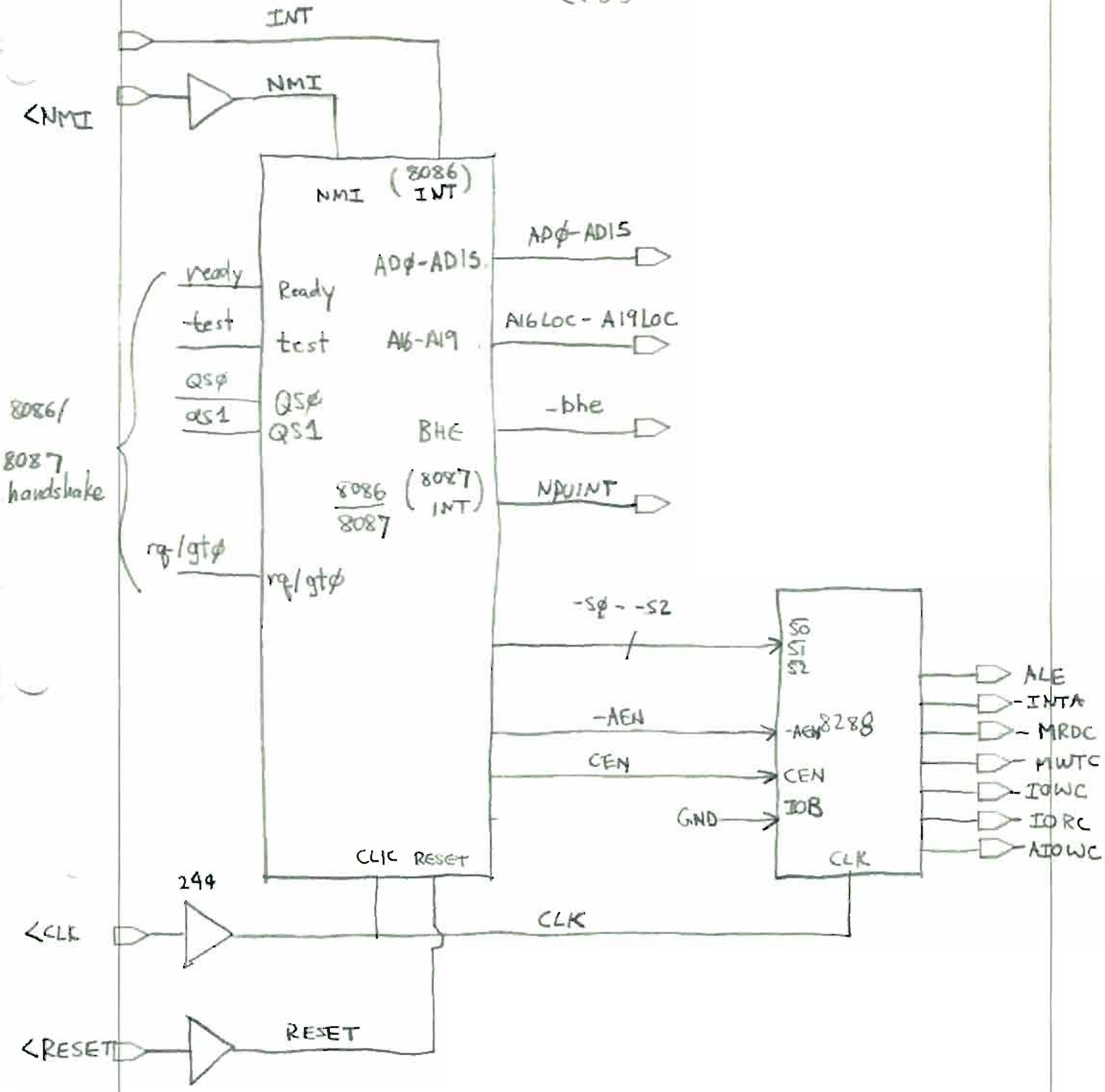
State Machine



8259c


ADØ-AD7
8259A
-INT
INTERRUPT
-INTA
-INTA
AØ
AØ
-INTM
-CS
-IORC
-RD
-IOWC
-WR
5V
SPEN
RBØF
RB1F
RB2F
RB3F
RD4F
RR5F
PIH
CASØ-
CAS2
INTS
8259A
-INT
INTERRUPT
-INTS6
-CS
GND
SPEN
TBØe
TB1e
TB2e
TB3e
TB4e
TB5e
PIL
npuint

CPUS


INT
NMI
<NMI
NMI
(8086)
INT
AD∅-AD15
AD∅-AD15
A16LOC - A19LOC
A16-A19
-bhe
BHE
8086/
8087 handshake
ready
Ready
-test
test
QS∅
QS∅
QS1
QS1
8086
8087
(8087
INT)
NPUINT
rq/gt∅
rq/gt∅
-S∅ - -S2
S0
S1
S2
-AEN
-AEN
8288
CEN
CEN
GND
IOB
ALE
-INTA
- MRDC
- MWTC
-IOWC
- IORC
-AIOWC
CLK
CLK
RESET
244
<CLK
CLK
<RESET
RESET

CONTROL BUS

CLK	GND
RESET	GND
NMI	GND
NC	GND
<GLODØ	GND
<GLOD1	GND
<GLOD2	GND
< NC	GND
< GLOCØ	GND
<GLOC1	GND
<GLOC2	GND
<GLOC3	GND
<GLOC 4	GND
<NC	GND

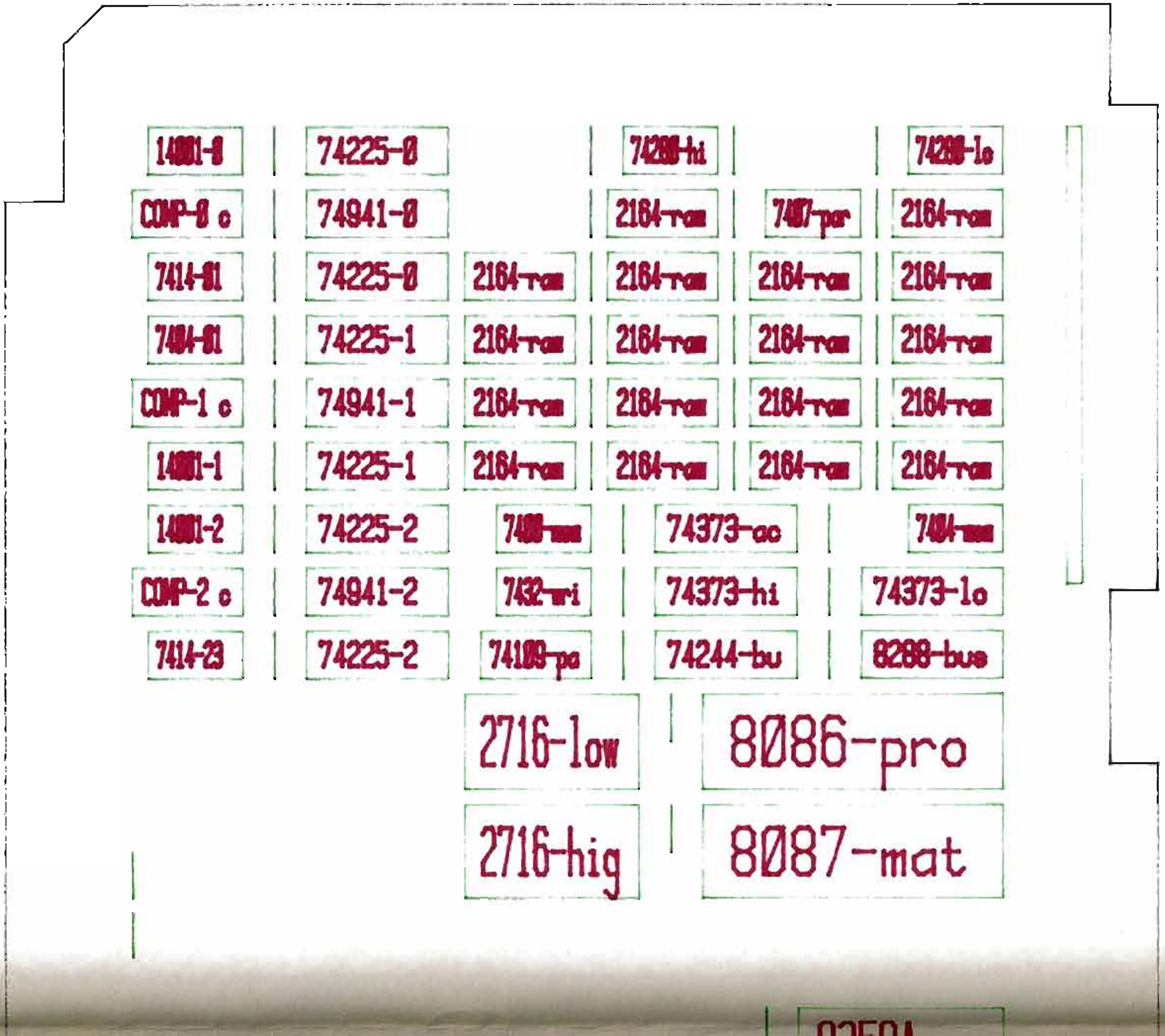
NC
↓

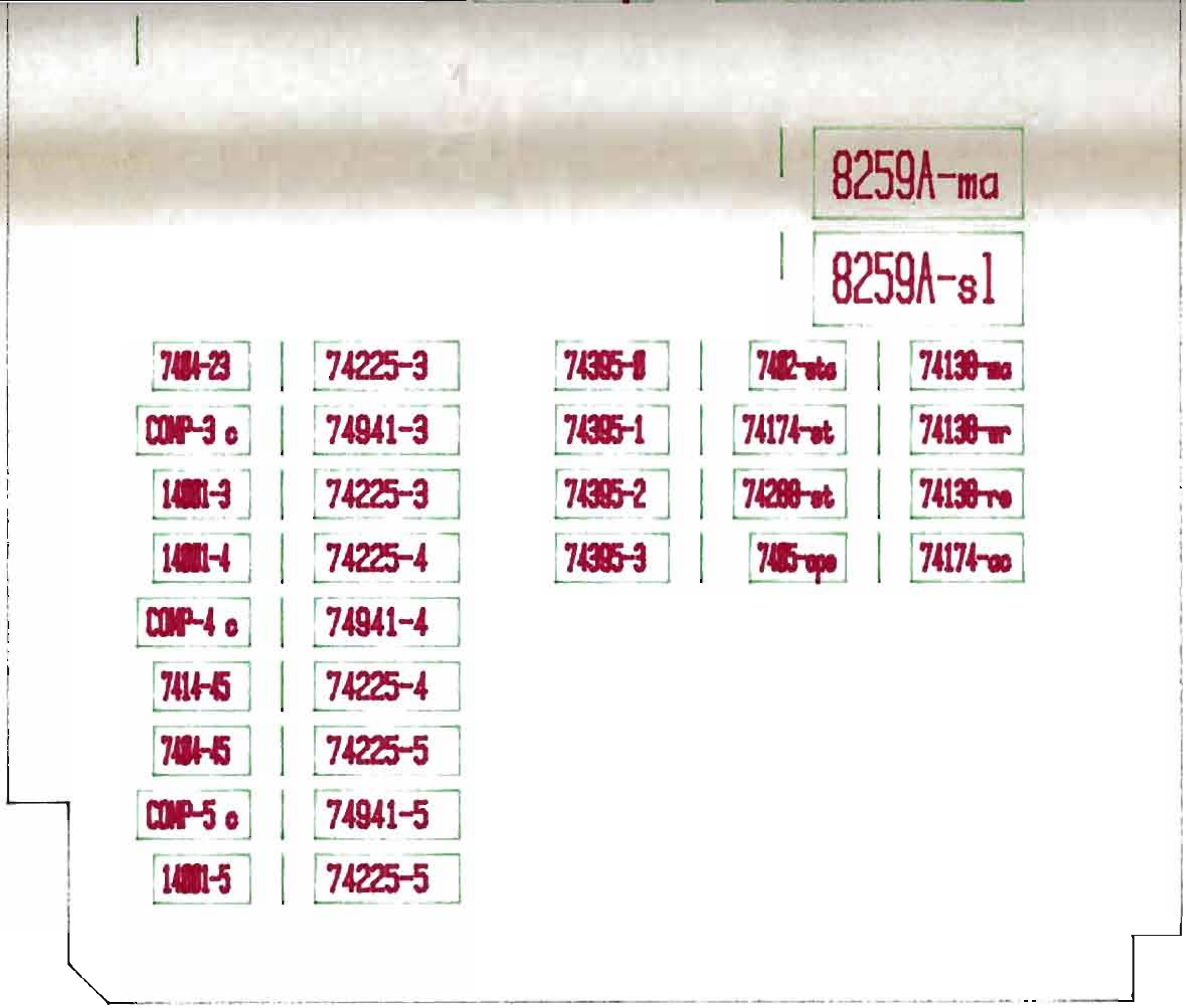
ASYNC CABLE

<OQØ	<OQ1
<OQ2	<OQ3
GND	< OQA
<OQR	GND
GND	←IQR
<IQA	GND
< IQ3	<IQ2
<IQ1	<IQ0

[illegible]

III, CHP


14001-Ø
74225-Ø
74280-hi
74280-lo
COMP-Ø c
74941-Ø
2164-ram
7407-par
2164-ram
7414-01
74225-Ø
2164-ram
2164-ram
2164-ram
2164-ram
7404-01
74225-1
2164-ram
2164-ram
2164-ram
2164-ram
COMP-1 c
74941-1
2164-ram
2164-ram
2164-ram
2164-ram
14001-1
74225-1
2164-ram
2164-ram
2164-ram
2164-ram
14001-2
74225-2
7400-mem
74373-ac
7404-mem
COMP-2 c
74941-2
7432-wri
74373-hi
74373-lo
7414-23
74225-2
74109-pa
74244-bu
8288-bus
2716-low
8Ø86-pro
2716-hig
8Ø87-mat


8259A-ma
8259A-sl
74395-0
7402-sts
74138-ma
74395-1
74174-st
74138-wr
74395-2
74288-st
74138-re
74395-3
7405-ope
74174-oc
7404-23
74225-3
COMP-3 c
74941-3
14001-3
74225-3
14001-4
74225-4
COMP-4 c
74941-4
7414-45
74225-4
7404-45
74225-5
COMP-5 c
74941-5
14001-5
74225-5

Jeffery

Cavallaro

Thu Apr 22 17:47:19 1982

break.chp

```
Apr 22 17:43 1982  break.chp Page 1


Sorted List:
PINS                                     +5/GND                   X:  0.00 Y:  0.00
R01+01 PINS     1   :5V                  +5/GND                   X:  0.10 Y:  0.00
R03+01 PINS     2   :GND                 +5/GND                   X:  0.50 Y:  0.00
R05+01 PINS     3   :5V                  +5/GND                   X:  0.90 Y:  0.00
R07+01 PINS     4   :GND                 +5/GND                   X:  1.30 Y:  0.00
R09+01 PINS     5   :5V                  +5/GND                   X:  1.70 Y:  0.00
R11+01 PINS     6   :GND                 +5/GND                   X:  2.10 Y:  0.00
R13+01 PINS     7   :5V                  +5/GND                   X:  2.50 Y:  0.00
R15+01 PINS     8   :GND                 +5/GND                   X:  2.90 Y:  0.00
R17+01 PINS     9   :5V                  +5/GND                   X:  3.30 Y:  0.00
R19+01 PINS    10   :GND                 +5/GND                   X:  3.70 Y:  0.00
R21+01 PINS    11   :5V                  +5/GND                   X:  4.10 Y:  0.00
R22+01 PINS    12   :GND                 +5/GND                   X:  4.40 Y:  0.00
R24+01 PINS    13   :5V                  +5/GND                   X:  4.80 Y:  0.00
R25+01 PINS    14   :GND                 +5/GND                   X:  5.10 Y:  0.00
R27+01 PINS    15   :5V                  +5/GND                   X:  5.50 Y:  0.00
R28+01 PINS    16   :GND                 +5/GND                   X:  5.80 Y:  0.00
R30+01 PINS    17   :5V                  +5/GND                   X:  6.20 Y:  0.00
R31+01 PINS    18   :GND                 +5/GND                   X:  6.50 Y:  0.00
R33+01 PINS    19   :5V                  +5/GND                   X:  6.90 Y:  0.00
R34+01 PINS    20   :GND                 +5/GND                   X:  7.20 Y:  0.00
R36+01 PINS    21   :5V                  +5/GND                   X:  7.60 Y:  0.00
R38+01 PINS    22   :GND                 +5/GND                   X:  8.00 Y:  0.00
R40+01 PINS    23   :5V                  +5/GND                   X:  8.40 Y:  0.00
R42+01 PINS    24   :GND                 +5/GND                   X:  8.80 Y:  0.00
R44+01 PINS    25   :5V                  +5/GND                   X:  9.20 Y:  0.00
R46+01 PINS    26   :GND                 +5/GND                   X:  9.60 Y:  0.00
R48+01 PINS    27   :5V                  +5/GND                   X:10.00 Y:  0.00
R50+01 PINS    28   :GND                 +5/GND                   X:10.40 Y:  0.00
R52+01 PINS    29   :5V                  +5/GND                   X:10.80 Y:  0.00
R54+01 PINS    30   :GND                 +5/GND                   X:11.20 Y`  0.00
R01+13 PINS    31   :5V                  +5/GND                   X:  0.10 Y:-1.20
R03+13 PINS    32   :GND                 +5/GND                   X:  0.50 Y:-1.20
R05+13 PINS    33   :5V                  +5/GND                   X:  0.90 Y:-1.20
R07+13 PINS    34   :GND                 +5/GND                   X:  1.30 Y:-1.20
R09+13 PINS    35   :5V                  +5/GND                   X:  1.70 Y:-1.20
R11+13 PINS    36   :GND                 +5/GND                   X:  2.10 Y:-1.20
R13+13 PINS    37   :5V                  +5/GND                   X:  2.50 Y:-1.20
R15+13 PINS    38   :GND                 +5/GND                   X:  2.90 Y:-1.20
R17+13 PINS    39   :5V                  +5/GND                   X:  3.30 Y:-1.20
R19+13 PINS    40   :GND                 +5/GND                   X:  3.70 Y:-1.20
R21+13 PINS    41   :5V                  +5/GND                   X:  4.10 Y:-1.20
R22+13 PINS    42   :GND                 +5/GND                   X:  4.40 Y:-1.20
R24+13 PINS    43   :5V                  +5/GND                   X:  4.80 Y:-1.20
R25+13 PINS    44   :GND                 +5/GND                   X:  5.10 Y:-1.20
R27+13 PINS    45   :5V                  +5/GND                   X:  5.50 Y:-1.20
R28+13 PINS    46   :GND                 +5/GND                   X:  5.80 Y:-1.20
R30+13 PINS    47   :5V                  +5/GND                   X:  6.20 Y:-1.20
R31+13 PINS    48   :GND                 +5/GND                   X:  6.50 Y:-1.20
R33+13 PINS    49   :5V                  +5/GND                   X:  6.90 Y:-1.20
R34+13 PINS    50   :GND                 +5/GND                   X:  7.20 Y:-1.20
R36+13 PINS    51   :5V                  +5/GND                   X:  7.60 Y:-1.20
R38+13 PINS    52   :GND                 +5/GND                   X:  8.00 Y:-1.20
R40+13 PINS    53   :5V                  +5/GND                   X:  8.40 Y:-1.20
R42+13 PINS    54   :GND                 +5/GND                   X:  8.80 Y:-1.20
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R44+13 PINS    55   :5V             +5/GND                       X: 9.20 Y:-1.20
R46+13 PINS    56   :GND            +5/GND                       X: 9.60 Y:-1.20
R48+13 PINS    57   :5V             +5/GND                       X:10.00 Y:-1.20
R50+13 PINS    58   :GND            +5/GND                       X:10.40 Y:-1.20
R52+13 PINS    59   :5V             +5/GND                       X:10.80 Y:-1.20
R54+13 PINS    60   :GND            +5/GND                       X:11.20 Y:-1.20
R01+25 PINS    61   :5V             +5/GND                       X: 0.10 Y:-2.40
R03+25 PINS    62   :GND            +5/GND                       X: 0.50 Y:-2.40
R05+25 PINS    63   :5V             +5/GND                       X: 0.90 Y:-2.40
R07+25 PINS    64   :GND            +5/GND                       X: 1.30 Y:-2.40
R09+25 PINS    65   :5V             +5/GND                       X: 1.70 Y:-2.40
R11+25 PINS    66   :GND            +5/GND                       X: 2.10 Y:-2.40
R13+25 PINS    67   :5V             +5/GND                       X: 2.50 Y:-2.40
R15+25 PINS    68   :GND            +5/GND                       X: 2.90 Y:-2.40
R17+25 PINS    69   :5V             +5/GND                       X: 3.30 Y:-2.40
R19+25 PINS    70   :GND            +5/GND                       X: 3.70 Y:-2.40
R21+25 PINS    71   :5V             +5/GND                       X: 4.10 Y:-2.40
R22+25 PINS    72   :GND            +5/GND                       X: 4.40 Y:-2.40
R24+25 PINS    73   :5V             +5/GND                       X: 4.80 Y:-2.40
R25+25 PINS    74   :GND            +5/GND                       X: 5.10 Y:-2.40
R27+25 PINS    75   :5V             +5/GND                       X: 5.50 Y:-2.40
R28+25 PINS    76   :GND            +5/GND                       X: 5.80 Y:-2.40
R30+25 PINS    77   :5V             +5/GND                       X: 6.20 Y:-2.40
R31+25 PINS    78   :GND            +5/GND                       X: 6.50 Y:-2.40
R33+25 PINS    79   :5V             +5/GND                       X: 6.90 Y:-2.40
R34+25 PINS    80   :GND            +5/GND                       X: 7.20 Y:-2.40
R36+25 PINS    81   :5V             +5/GND                       X: 7.60 Y:-2.40
R38+25 PINS    82   :GND            +5/GND                       X: 8.00 Y:-2.40
R40+25 PINS    83   :5V             +5/GND                       X: 8.40 Y:-2.40
R42+25 PINS    84   :GND            +5/GND                       X: 8.80 Y:-2.40
R44+25 PINS    85   :5V             +5/GND                       X: 9.20 Y:-2.40
R46+25 PINS    86   :GND            +5/GND                       X: 9.60 Y:-2.40
R48+25 PINS    87   :5V             +5/GND                       X:10.00 Y:-2.40
R50+25 PINS    88   :GND            +5/GND                       X:10.40 Y:-2.40
R52+25 PINS    89   :5V             +5/GND                       X:10.80 Y:-2.40
R54+25 PINS    90   :GND            +5/GND                       X:11.20 Y:-2.40
R01+37 PINS    91   :5V             +5/GND                       X: 0.10 Y:-3.60
R03+37 PINS    92   :GND            +5/GND                       X: 0.50 Y:-3.60
R05+37 PINS    93   :5V             +5/GND                       X: 0.90 Y:-3.60
R07+37 PINS    94   :GND            +5/GND                       X: 1.30 Y:-3.60
R09+37 PINS    95   :5V             +5/GND                       X: 1.70 Y:-3.60
R11+37 PINS    96   :GND            +5/GND                       X: 2.10 Y:-3.60
R13+37 PINS    97   :5V             +5/GND                       X: 2.50 Y:-3.60
R15+37 PINS    98   :GND            +5/GND                       X: 2.90 Y:-3.60
R17+37 PINS    99   :5V             +5/GND                       X: 3.30 Y:-3.60
R19+37 PINS   100   :GND            +5/GND                       X: 3.70 Y:-3.60
R21+37 PINS   101   :5V             +5/GND                       X: 4.10 Y:-3.60
R22+37 PINS   102   :GND            +5/GND                       X: 4.40 Y:-3.60
R24+37 PINS   103   :5V             +5/GND                       X: 4.80 Y:-3.60
R25+37 PINS   104   :GND            +5/GND                       X: 5.10 Y:-3.60
R27+37 PINS   105   :5V             +5/GND                       X: 5.50 Y:-3.60
R28+37 PINS   106   :GND            +5/GND                       X: 5.80 Y:-3.60
R30+37 PINS   107   :5V             +5/GND                       X: 6.20 Y:-3.60
R31+37 PINS   108   :GND            +5/GND                       X: 6.50 Y:-3.60
R33+37 PINS   109   :5V             +5/GND                       X: 6.90 Y:-3.60
R34+37 PINS   110   :GND            +5/GND                       X: 7.20 Y:-3.60
```

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R36+37 PINS   111   :5V             +5/GND                  X: 7.60 Y:-3.60
R38+37 PINS   112   :GND            +5/GND                  X: 8.00 Y:-3.60
R40+37 PINS   113   :5V             +5/GND                  X: 8.40 Y:-3.60
R42+37 PINS   114   :GND            +5/GND                  X: 8.80 Y:-3.60
R44+37 PINS   115   :5V             +5/GND                  X: 9.20 Y:-3.60
R46+37 PINS   116   :GND            +5/GND                  X: 9.60 Y:-3.60
R48+37 PINS   117   :5V             +5/GND                  X:10.00 Y:-3.60
R50+37 PINS   118   :GND            +5/GND                  X:10.40 Y:-3.60
R52+37 PINS   119   :5V             +5/GND                  X:10.80 Y:-3.60
R54+37 PINS   120   :GND            +5/GND                  X:11.20 Y:-3.60
R01+49 PINS   121   :5V             +5/GND                  X: 0.10 Y:-4.80
R03+49 PINS   122   :GND            +5/GND                  X: 0.50 Y:-4.80
R05+49 PINS   123   :5V             +5/GND                  X: 0.90 Y:-4.80
R07+49 PINS   124   :GND            +5/GND                  X: 1.30 Y:-4.80
R09+49 PINS   125   :5V             +5/GND                  X: 1.70 Y:-4.80
R11+49 PINS   126   :GND            +5/GND                  X: 2.10 Y:-4.80
R13+49 PINS   127   :5V             +5/GND                  X: 2.50 Y:-4.80
R15+49 PINS   128   :GND            +5/GND                  X: 2.90 Y:-4.80
R17+49 PINS   129   :5V             +5/GND                  X: 3.30 Y:-4.80
R19+49 PINS   130   :GND            +5/GND                  X: 3.70 Y:-4.80
R21+49 PINS   131   :5V             +5/GND                  X: 4.10 Y:-4.80
R22+49 PINS   132   :GND            +5/GND                  X: 4.40 Y:-4.80
R24+49 PINS   133   :5V             +5/GND                  X: 4.80 Y:-4.80
R25+49 PINS   134   :GND            +5/GND                  X: 5.10 Y:-4.80
R27+49 PINS   135   :5V             +5/GND                  X: 5.50 Y:-4.80
R28+49 PINS   136   :GND            +5/GND                  X: 5.80 Y:-4.80
R30+49 PINS   137   :5V             +5/GND                  X: 6.20 Y:-4.80
R31+49 PINS   138   :GND            +5/GND                  X: 6.50 Y:-4.80
R33+49 PINS   139   :5V             +5/GND                  X: 6.90 Y:-4.80
R34+49 PINS   140   :GND            +5/GND                  X: 7.20 Y:-4.80
R36+49 PINS   141   :5V             +5/GND                  X: 7.60 Y:-4.80
R38+49 PINS   142   :GND            +5/GND                  X: 8.00 Y:-4.80
R40+49 PINS   143   :5V             +5/GND                  X: 8.40 Y:-4.80
R42+49 PINS   144   :GND            +5/GND                  X: 8.80 Y:-4.80
R44+49 PINS   145   :5V             +5/GND                  X: 9.20 Y:-4.80
R46+49 PINS   146   :GND            +5/GND                  X: 9.60 Y:-4.80
R48+49 PINS   147   :5V             +5/GND                  X:10.00 Y:-4.80
R50+49 PINS   148   :GND            +5/GND                  X:10.40 Y:-4.80
R52+49 PINS   149   :5V             +5/GND                  X:10.80 Y:-4.80
R54+49 PINS   150   :GND            +5/GND                  X:11.20 Y:-4.80
R01+07 PINS   151   :GND            +5/GND                  X: 0.10 Y:-0.60
R03+07 PINS   152   :5V             +5/GND                  X: 0.50 Y:-0.60
R05+07 PINS   153   :GND            +5/GND                  X: 0.90 Y:-0.60
R07+07 PINS   154   :5V             +5/GND                  X: 1.30 Y:-0.60
R09+07 PINS   155   :GND            +5/GND                  X: 1.70 Y:-0.60
R11+07 PINS   156   :5V             +5/GND                  X: 2.10 Y:-0.60
R13+07 PINS   157   :GND            +5/GND                  X: 2.50 Y:-0.60
R15+07 PINS   158   :5V             +5/GND                  X: 2.90 Y:-0.60
R17+07 PINS   159   :GND            +5/GND                  X: 3.30 Y:-0.60
R19+07 PINS   160   :5V             +5/GND                  X: 3.70 Y:-0.60
R21+07 PINS   161   :GND            +5/GND                  X: 4.10 Y:-0.60
R22+07 PINS   162   :5V             +5/GND                  X: 4.40 Y:-0.60
R24+07 PINS   163   :GND            +5/GND                  X: 4.80 Y:-0.60
R25+07 PINS   164   :5V             +5/GND                  X: 5.10 Y:-0.60
R27+07 PINS   165   :GND            +5/GND                  X: 5.50 Y:-0.60
R28+07 PINS   166   :5V             +5/GND                  X: 5.80 Y:-0.60
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R30+07 PINS    167   :GND               +5/GND                        X: 6.20 Y:-0.60
R31+07 PINS    168   :5V                +5/GND                        X: 6.50 Y:-0.60
R33+07 PINS    169   :GND               +5/GND                        X: 6.90 Y:-0.60
R34+07 PINS    170   :5V                +5/GND                        X: 7.20 Y:-0.60
R36+07 PINS    171   :GND               +5/GND                        X: 7.60 Y:-0.60
R38+07 PINS    172   :5V                +5/GND                        X: 8.00 Y:-0.60
R40+07 PINS    173   :GND               +5/GND                        X: 8.40 Y:-0.60
R42+07 PINS    174   :5V                +5/GND                        X: 8.80 Y:-0.60
R44+07 PINS    175   :GND               +5/GND                        X: 9.20 Y:-0.60
R46+07 PINS    176   :5V                +5/GND                        X: 9.60 Y:-0.60
R48+07 PINS    177   :GND               +5/GND                        X:10.00 Y:-0.60
R50+07 PINS    178   :5V                +5/GND                        X:10.40 Y:-0.60
R52+07 PINS    179   :GND               +5/GND                        X:10.80 Y:-0.60
R54+07 PINS    180   :5V                +5/GND                        X:11.20 Y:-0.60
R01+19 PINS    181   :GND               +5/GND                        X: 0.10 Y:-1.80
R03+19 PINS    182   :5V                +5/GND                        X: 0.50 Y:-1.80
R05+19 PINS    183   :GND               +5/GND                        X: 0.90 Y:-1.80
R07+19 PINS    184   :5V                +5/GND                        X: 1.30 Y:-1.80
R09+19 PINS    185   :GND               +5/GND                        X: 1.70 Y:-1.80
R11+19 PINS    186   :5V                +5/GND                        X: 2.10 Y:-1.80
R13+19 PINS    187   :GND               +5/GND                        X: 2.50 Y:-1.80
R15+19 PINS    188   :5V                +5/GND                        X: 2.90 Y:-1.80
R17+19 PINS    189   :GND               +5/GND                        X: 3.30 Y:-1.80
R19+19 PINS    190   :5V                +5/GND                        X: 3.70 Y:-1.80
R21+19 PINS    191   :GND               +5/GND                        X: 4.10 Y:-1.80
R22+19 PINS    192   :5V                +5/GND                        X: 4.40 Y:-1.80
R24+19 PINS    193   :GND               +5/GND                        X: 4.80 Y:-1.80
R25+19 PINS    194   :5V                +5/GND                        X: 5.10 Y:-1.80
R27+19 PINS    195   :GND               +5/GND                        X: 5.50 Y:-1.80
R28+19 PINS    196   :5V                +5/GND                        X: 5.80 Y:-1.80
R30+19 PINS    197   :GND               +5/GND                        X: 6.20 Y:-1.80
R31+19 PINS    198   :5V                +5/GND                        X: 6.50 Y:-1.80
R33+19 PINS    199   :GND               +5/GND                        X: 6.90 Y:-1.80
R34+19 PINS    200   :5V                +5/GND                        X: 7.20 Y:-1.80
R36+19 PINS    201   :GND               +5/GND                        X: 7.60 Y:-1.80
R38+19 PINS    202   :5V                +5/GND                        X: 8.00 Y:-1.80
R40+19 PINS    203   :GND               +5/GND                        X: 8.40 Y:-1.80
R42+19 PINS    204   :5V                +5/GND                        X: 8.80 Y:-1.80
R44+19 PINS    205   :GND               +5/GND                        X: 9.20 Y:-1.80
R46+19 PINS    206   :5V                +5/GND                        X: 9.60 Y:-1.80
R48+19 PINS    207   :GND               +5/GND                        X:10.00 Y:-1.80
R50+19 PINS    208   :5V                +5/GND                        X:10.40 Y:-1.80
R52+19 PINS    209   :GND               +5/GND                        X:10.80 Y:-1.80
R54+19 PINS    210   :5V                +5/GND                        X:11.20 Y:-1.80
R01+31 PINS    211   :GND               +5/GND                        X: 0.10 Y:-3.00
R03+31 PINS    212   :5V                +5/GND                        X: 0.50 Y:-3.00
R05+31 PINS    213   :GND               +5/GND                        X: 0.90 Y:-3.00
R07+31 PINS    214   :5V                +5/GND                        X: 1.30 Y:-3.00
R09+31 PINS    215   :GND               +5/GND                        X: 1.70 Y:-3.00
R11+31 PINS    216   :5V                +5/GND                        X: 2.10 Y:-3.00
R13+31 PINS    217   :GND               +5/GND                        X: 2.50 Y:-3.00
R15+31 PINS    218   :5V                +5/GND                        X: 2.90 Y:-3.00
R17+31 PINS    219   :GND               +5/GND                        X: 3.30 Y:-3.00
R19+31 PINS    220   :5V                +5/GND                        X: 3.70 Y:-3.00
R21+31 PINS    221   :GND               +5/GND                        X: 4.10 Y:-3.00
R22+31 PINS    222   :5V                +5/GND                        X: 4.40 Y:-3.00
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R24+31 PINS   223  :GND              +5/GND                   X: 4.80 Y:-3.00
R25+31 PINS   224  :5V               +5/GND                   X: 5.10 Y:-3.00
R27+31 PINS   225  :GND              +5/GND                   X: 5.50 Y:-3.00
R28+31 PINS   226  :5V               +5/GND                   X: 5.80 Y:-3.00
R30+31 PINS   227  :GND              +5/GND                   X: 6.20 Y:-3.00
R31+31 PINS   228  :5V               +5/GND                   X: 6.50 Y:-3.00
R33+31 PINS   229  :GND              +5/GND                   X: 6.90 Y:-3.00
R34+31 PINS   230  :5V               +5/GND                   X: 7.20 Y:-3.00
R36+31 PINS   231  :GND              +5/GND                   X: 7.60 Y:-3.00
R38+31 PINS   232  :5V               +5/GND                   X: 8.00 Y:-3.00
R40+31 PINS   233  :GND              +5/GND                   X: 8.40 Y:-3.00
R42+31 PINS   234  :5V               +5/GND                   X: 8.80 Y:-3.00
R44+31 PINS   235  :GND              +5/GND                   X: 9.20 Y:-3.00
R46+31 PINS   236  :5V               +5/GND                   X: 9.60 Y:-3.00
R48+31 PINS   237  :GND              +5/GND                   X:10.00 Y:-3.00
R50+31 PINS   238  :5V               +5/GND                   X:10.40 Y:-3.00
R52+31 PINS   239  :GND              +5/GND                   X:10.80 Y:-3.00
R54+31 PINS   240  :5V               +5/GND                   X:11.20 Y:-3.00
R01+43 PINS   241  :GND              +5/GND                   X: 0.10 Y:-4.20
R03+43 PINS   242  :5V               +5/GND                   X: 0.50 Y:-4.20
R05+43 PINS   243  :GND              +5/GND                   X: 0.90 Y:-4.20
R07+43 PINS   244  :5V               +5/GND                   X: 1.30 Y:-4.20
R09+43 PINS   245  :GND              +5/GND                   X: 1.70 Y:-4.20
R11+43 PINS   246  :5V               +5/GND                   X: 2.10 Y:-4.20
R13+43 PINS   247  :GND              +5/GND                   X: 2.50 Y:-4.20
R15+43 PINS   248  :5V               +5/GND                   X: 2.90 Y:-4.20
R17+43 PINS   249  :GND              +5/GND                   X: 3.30 Y:-4.20
R19+43 PINS   250  :5V               +5/GND                   X: 3.70 Y:-4.20
R21+43 PINS   251  :GND              +5/GND                   X: 4.10 Y:-4.20
R22+43 PINS   252  :5V               +5/GND                   X: 4.40 Y:-4.20
R24+43 PINS   253  :GND              +5/GND                   X: 4.80 Y:-4.20
R25+43 PINS   254  :5V               +5/GND                   X: 5.10 Y:-4.20
R27+43 PINS   255  :GND              +5/GND                   X: 5.50 Y:-4.20
R28+43 PINS   256  :5V               +5/GND                   X: 5.80 Y:-4.20
R30+43 PINS   257  :GND              +5/GND                   X: 6.20 Y:-4.20
R31+43 PINS   258  :5V               +5/GND                   X: 6.50 Y:-4.20
R33+43 PINS   259  :GND              +5/GND                   X: 6.90 Y:-4.20
R34+43 PINS   260  :5V               +5/GND                   X: 7.20 Y:-4.20
R36+43 PINS   261  :GND              +5/GND                   X: 7.60 Y:-4.20
R38+43 PINS   262  :5V               +5/GND                   X: 8.00 Y:-4.20
R40+43 PINS   263  :GND              +5/GND                   X: 8.40 Y:-4.20
R42+43 PINS   264  :5V               +5/GND                   X: 8.80 Y:-4.20
R44+43 PINS   265  :GND              +5/GND                   X: 9.20 Y:-4.20
R46+43 PINS   266  :5V               +5/GND                   X: 9.60 Y:-4.20
R48+43 PINS   267  :GND              +5/GND                   X:10.00 Y:-4.20
R50+43 PINS   268  :5V               +5/GND                   X:10.40 Y:-4.20
R52+43 PINS   269  :GND              +5/GND                   X:10.80 Y:-4.20
R54+43 PINS   270  :5V               +5/GND                   X:11.20 Y:-4.20
R03+55 PINS   271  :5V               +5/GND                   X: 0.50 Y:-5.40
R05+55 PINS   272  :GND              +5/GND                   X: 0.90 Y:-5.40
R07+55 PINS   273  :5V               +5/GND                   X: 1.30 Y:-5.40
R09+55 PINS   274  :GND              +5/GND                   X: 1.70 Y:-5.40
R11+55 PINS   275  :5V               +5/GND                   X: 2.10 Y:-5.40
R13+55 PINS   276  :GND              +5/GND                   X: 2.50 Y:-5.40
R15+55 PINS   277  :5V               +5/GND                   X: 2.90 Y:-5.40
R17+55 PINS   278  :GND              +5/GND                   X: 3.30 Y:-5.40
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R19+55 PINS    279   :5V                  +5/GND                       X: 3.70 Y:-5.40
R21+55 PINS    280   :GND                 +5/GND                       X: 4.10 Y:-5.40
R22+55 PINS    281   :5V                  +5/GND                       X: 4.40 Y:-5.40
R24+55 PINS    282   :GND                 +5/GND                       X: 4.80 Y:-5.40
R25+55 PINS    283   :5V                  +5/GND                       X: 5.10 Y:-5.40
R27+55 PINS    284   :GND                 +5/GND                       X: 5.50 Y:-5.40
R28+55 PINS    285   :5V                  +5/GND                       X: 5.80 Y:-5.40
R30+55 PINS    286   :GND                 +5/GND                       X: 6.20 Y:-5.40
R31+55 PINS    287   :5V                  +5/GND                       X: 6.50 Y:-5.40
R33+55 PINS    288   :GND                 +5/GND                       X: 6.90 Y:-5.40
R34+55 PINS    289   :5V                  +5/GND                       X: 7.20 Y:-5.40
R36+55 PINS    290   :GND                 +5/GND                       X: 7.60 Y:-5.40
R38+55 PINS    291   :5V                  +5/GND                       X: 8.00 Y:-5.40
R40+55 PINS    292   :GND                 +5/GND                       X: 8.40 Y:-5.40
R42+55 PINS    293   :5V                  +5/GND                       X: 8.80 Y:-5.40
R44+55 PINS    294   :GND                 +5/GND                       X: 9.20 Y:-5.40
R46+55 PINS    295   :5V                  +5/GND                       X: 9.60 Y:-5.40
R48+55 PINS    296   :GND                 +5/GND                       X:10.00 Y:-5.40
R50+55 PINS    297   :5V                  +5/GND                       X:10.40 Y:-5.40
R52+55 PINS    298   :GND                 +5/GND                       X:10.80 Y:-5.40

PINS                                       Multibus connector          X: 0.00 Y: 0.00
R05OFF PINS      1    NC                   Multibus connector          X: 0.00 Y: 0.50
R05OFF PINS      2    NC                   Multibus connector          X: 0.80 Y: 0.40
R05OFF PINS      3    NC                   Multibus connector          X: 0.90 Y: 0.50
R05OFF PINS      4    NC                   Multibus connector          X: 0.90 Y: 0.40
R07OFF PINS      5    NC                   Multibus connector          X: 1.20 Y: 0.50
R07OFF PINS      6   ^INIT/                Multibus connector          X: 1.20 Y: 0.40
R08OFF PINS      7    NC                   Multibus connector          X: 1.40 Y: 0.50
R08OFF PINS      8    NC                   Multibus connector          X: 1.40 Y: 0.40
R08OFF PINS      9    NC                   Multibus connector          X: 1.50 Y: 0.50
R08OFF PINS     10    NC                   Multibus connector          X: 1.50 Y: 0.40
R09OFF PINS     11    NC                   Multibus connector          X: 1.70 Y: 0.50
R09OFF PINS     12    NC                   Multibus connector          X: 1.70 Y: 0.40
R10OFF PINS     13    NC                   Multibus connector          X: 1.80 Y: 0.50
R10OFF PINS     14    NC                   Multibus connector          X: 1.80 Y: 0.40
R11OFF PINS     15    NC                   Multibus connector          X: 2.00 Y: 0.50
R11OFF PINS     16    NC                   Multibus connector          X: 2.00 Y: 0.40
R11OFF PINS     17    NC                   Multibus connector          X: 2.10 Y: 0.50
R11OFF PINS     18    NC                   Multibus connector          X: 2.10 Y: 0.40
R12OFF PINS     19    NC                   Multibus connector          X: 2.30 Y: 0.50
R12OFF PINS     20    NC                   Multibus connector          X: 2.30 Y: 0.40
R13OFF PINS     21    NC                   Multibus connector          X: 2.40 Y: 0.50
R13OFF PINS     22    NC                   Multibus connector          X: 2.40 Y: 0.40
R14OFF PINS     23    NC                   Multibus connector          X: 2.60 Y: 0.50
R14OFF PINS     24    NC                   Multibus connector          X: 2.60 Y: 0.40
R14OFF PINS     25    NC                   Multibus connector          X: 2.70 Y: 0.50
R14OFF PINS     26    NC                   Multibus connector          X: 2.70 Y: 0.40
R15OFF PINS     27    NC                   Multibus connector          X: 2.90 Y: 0.50
R15OFF PINS     28    NC                   Multibus connector          X: 2.90 Y: 0.40
R16OFF PINS     29    NC                   Multibus connector          X: 3.00 Y: 0.50
R16OFF PINS     30    NC                   Multibus connector          X: 3.00 Y: 0.40
R17OFF PINS     31    NC                   Multibus connector          X: 3.20 Y: 0.50
R17OFF PINS     32    NC                   Multibus connector          X: 3.20 Y: 0.40
R18OFF PINS     33    NC                   Multibus connector          X: 3.40 Y: 0.50
R18OFF PINS     34    NC                   Multibus connector          X: 3.40 Y: 0.40
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R19OFF PINS     35   NC                 Multibus connector      X: 3.60 Y: 0.50
R19OFF PINS     36   NC                 Multibus connector      X: 3.60 Y: 0.40
R19OFF PINS     37   NC                 Multibus connector      X: 3.70 Y: 0.50
R19OFF PINS     38   NC                 Multibus connector      X: 3.70 Y: 0.40
R20OFF PINS     39   NC                 Multibus connector      X: 3.90 Y: 0.50
R20OFF PINS     40   NC                 Multibus connector      X: 3.90 Y: 0.40
R21OFF PINS     41   NC                 Multibus connector      X: 4.00 Y: 0.50
R21OFF PINS     42   NC                 Multibus connector      X: 4.00 Y: 0.40
R22OFF PINS     43   NC                 Multibus connector      X: 4.20 Y: 0.50
R22OFF PINS     44   NC                 Multibus connector      X: 4.20 Y: 0.40
R22OFF PINS     45   NC                 Multibus connector      X: 4.30 Y: 0.50
R22OFF PINS     46   NC                 Multibus connector      X: 4.30 Y: 0.40
R23OFF PINS     47   NC                 Multibus connector      X: 4.50 Y: 0.50
R23OFF PINS     48   NC                 Multibus connector      X: 4.50 Y: 0.40
R23OFF PINS     49   NC                 Multibus connector      X: 4.60 Y: 0.50
R23OFF PINS     50   NC                 Multibus connector      X: 4.60 Y: 0.40
R24OFF PINS     51   NC                 Multibus connector      X: 4.80 Y: 0.50
R24OFF PINS     52   NC                 Multibus connector      X: 4.80 Y: 0.40
R25OFF PINS     53   NC                 Multibus connector      X: 4.90 Y: 0.50
R25OFF PINS     54   NC                 Multibus connector      X: 4.90 Y: 0.40
R25OFF PINS     55   NC                 Multibus connector      X: 5.10 Y: 0.50
R25OFF PINS     56   NC                 Multibus connector      X: 5.10 Y: 0.40
R26OFF PINS     57   NC                 Multibus connector      X: 5.30 Y: 0.50
R26OFF PINS     58   NC                 Multibus connector      X: 5.30 Y: 0.40
R27OFF PINS     59   NC                 Multibus connector      X: 5.50 Y: 0.50
R27OFF PINS     60   NC                 Multibus connector      X: 5.50 Y: 0.40
R28OFF PINS     61   NC                 Multibus connector      X: 5.60 Y: 0.50
R28OFF PINS     62   NC                 Multibus connector      X: 5.60 Y: 0.40
R28OFF PINS     63   NC                 Multibus connector      X: 5.80 Y: 0.50
R28OFF PINS     64   NC                 Multibus connector      X: 5.80 Y: 0.40
R29OFF PINS     65   NC                 Multibus connector      X: 5.90 Y: 0.50
R29OFF PINS     66   NC                 Multibus connector      X: 5.90 Y: 0.40
R30OFF PINS     67   NC                 Multibus connector      X: 6.20 Y: 0.50
R30OFF PINS     68   NC                 Multibus connector      X: 6.20 Y: 0.40
R31OFF PINS     69   NC                 Multibus connector      X: 6.30 Y: 0.50
R31OFF PINS     70   NC                 Multibus connector      X: 6.30 Y: 0.40

R06P03 DIP14                   7407-OUTPUT MULTIBUS DRIVER (OPENX: 1.10 Y:-0.20
R06P03 R06P03   1   RCV        7407-OUTPUT MULTIBUS DRIVER (OPENX: 1.10 Y:-0.20
R06P04 R06P03   2  *DELAY      7407-OUTPUT MULTIBUS DRIVER (OPENX: 1.10 Y:-0.30
R06P05 R06P03   3   -RESET     7407-OUTPUT MULTIBUS DRIVER (OPENX: 1.10 Y:-0.40
R06P06 R06P03   4  *INIT/      7407-OUTPUT MULTIBUS DRIVER (OPENX: 1.10 Y:-0.50
R06P07 R06P03   5   NC         7407-OUTPUT MULTIBUS DRIVER (OPENX: 1.10 Y:-0.60
R06P08 R06P03   6  $NC         7407-OUTPUT MULTIBUS DRIVER (OPENX: 1.10 Y:-0.70
R06P09 R06P03   7   GND        7407-OUTPUT MULTIBUS DRIVER (OPENX: 1.10 Y:-0.80
R05P09 R06P03   8  $NC         7407-OUTPUT MULTIBUS DRIVER (OPENX: 0.80 Y:-0.80
R05P08 R06P03   9   NC         7407-OUTPUT MULTIBUS DRIVER (OPENX: 0.80 Y:-0.70
R05P07 R06P03  10  $NC         7407-OUTPUT MULTIBUS DRIVER (OPENX: 0.80 Y:-0.60
R05P06 R06P03  11   NC         7407-OUTPUT MULTIBUS DRIVER (OPENX: 0.80 Y:-0.50
R05P05 R06P03  12  $NC         7407-OUTPUT MULTIBUS DRIVER (OPENX: 0.80 Y:-0.40
R05P04 R06P03  13   NC         7407-OUTPUT MULTIBUS DRIVER (OPENX: 0.80 Y:-0.30
R05P03 R06P03  14   5V         7407-OUTPUT MULTIBUS DRIVER (OPENX: 0.80 Y:-0.20

R10P03 DIP14                   7414-LEVEL DETECTOR (74C14 SCHMITX: 1.90 Y:-0.20
R10P03 R10P03   1   DELAY      7414-LEVEL DETECTOR (74C14 SCHMITX: 1.90 Y:-0.20
R10P04 R10P03   2  $-RESET     7414-LEVEL DETECTOR (74C14 SCHMITX: 1.90 Y:-0.30
R10P05 R10P03   3   -RCV     7414-LEVEL DETECTOR (74C14 SCHMITX: 1.90 Y:-0.40
R10P06 R10P03   4  $RCV      7414-LEVEL DETECTOR (74C14 SCHMITX: 1.90 Y:-0.50
R10P07 R10P03   5   NC       7414-LEVEL DETECTOR (74C14 SCHMITX: 1.90 Y:-0.60
R10P08 R10P03   6  $NC       7414-LEVEL DETECTOR (74C14 SCHMITX: 1.90 Y:-0.70
R10P09 R10P03   7   GND      7414-LEVEL DETECTOR (74C14 SCHMITX: 1.90 Y:-0.80
R09P09 R10P03   8  $NC       7414-LEVEL DETECTOR (74C14 SCHMITX: 1.60 Y:-0.80
R09P08 R10P03   9   NC       7414-LEVEL DETECTOR (74C14 SCHMITX: 1.60 Y:-0.70
R09P07 R10P03  10  $NC       7414-LEVEL DETECTOR (74C14 SCHMITX: 1.60 Y:-0.60
R09P06 R10P03  11   NC       7414-LEVEL DETECTOR (74C14 SCHMITX: 1.60 Y:-0.50
R09P05 R10P03  12  $NC       7414-LEVEL DETECTOR (74C14 SCHMITX: 1.60 Y:-0.40
R09P04 R10P03  13   NC       7414-LEVEL DETECTOR (74C14 SCHMITX: 1.60 Y:-0.30
R09P03 R10P03  14   5V       7414-LEVEL DETECTOR (74C14 SCHMITX: 1.60 Y:-0.20

R04P03 DIP14                 75189-INPUT RS232 TO TTL RECEIVERX: 0.70 Y:-0.20
R04P03 R04P03   1   <RCV     75189-INPUT RS232 TO TTL RECEIVERX: 0.70 Y:-0.20
R04P04 R04P03   2   NC       75189-INPUT RS232 TO TTL RECEIVERX: 0.70 Y:-0.30
R04P05 R04P03   3  $-RCV     75189-INPUT RS232 TO TTL RECEIVERX: 0.70 Y:-0.40
R04P06 R04P03   4   NC       75189-INPUT RS232 TO TTL RECEIVERX: 0.70 Y:-0.50
R04P07 R04P03   5   NC       75189-INPUT RS232 TO TTL RECEIVERX: 0.70 Y:-0.60
R04P08 R04P03   6  $NC       75189-INPUT RS232 TO TTL RECEIVERX: 0.70 Y:-0.70
R04P09 R04P03   7   GND      75189-INPUT RS232 TO TTL RECEIVERX: 0.70 Y:-0.80
R03P09 R04P03   8  $NC       75189-INPUT RS232 TO TTL RECEIVERX: 0.40 Y:-0.80
R03P08 R04P03   9   NC       75189-INPUT RS232 TO TTL RECEIVERX: 0.40 Y:-0.70
R03P07 R04P03  10   NC       75189-INPUT RS232 TO TTL RECEIVERX: 0.40 Y:-0.60
R03P06 R04P03  11  $NC       75189-INPUT RS232 TO TTL RECEIVERX: 0.40 Y:-0.50
R03P05 R04P03  12   NC       75189-INPUT RS232 TO TTL RECEIVERX: 0.40 Y:-0.40
R03P04 R04P03  13   NC       75189-INPUT RS232 TO TTL RECEIVERX: 0.40 Y:-0.30
R03P03 R04P03  14   5V       75189-INPUT RS232 TO TTL RECEIVERX: 0.40 Y:-0.20

R04P01 CAP                   CAP-5V BYPASS                      X: 0.70 Y: 0.00
R04P01 R04P01   1  ;GND      CAP-5V BYPASS                      X: 0.70 Y: 0.00
R03P01 R04P01   2  ;5V       CAP-5V BYPASS                      X: 0.40 Y: 0.00

R06P01 CAP                   CAP-5V BYPASS                      X: 1.10 Y: 0.00
R06P01 R06P01   1  ;GND      CAP-5V BYPASS                      X: 1.10 Y: 0.00
R05P01 R06P01   2  ;5V       CAP-5V BYPASS                      X: 0.80 Y: 0.00

R08P01 CAP                   CAP-5V BYPASS                      X: 1.50 Y: 0.00
R08P01 R08P01   1  ;GND      CAP-5V BYPASS                      X: 1.50 Y: 0.00
R07P01 R08P01   2  ;5V       CAP-5V BYPASS                      X: 1.20 Y: 0.00

R10P01 CAP                   CAP-5V BYPASS                      X: 1.90 Y: 0.00
R10P01 R10P01   1  ;GND      CAP-5V BYPASS                      X: 1.90 Y: 0.00
R09P01 R10P01   2  ;5V       CAP-5V BYPASS                      X: 1.60 Y: 0.00

R04P12 CAP                   CAP-5V BYPASS                      X: 0.70 Y:-1.10
R04P12 R04P12   1  ;GND      CAP-5V BYPASS                      X: 0.70 Y:-1.10
R03P12 R04P12   2  ;5V       CAP-5V BYPASS                      X: 0.40 Y:-1.10

R06P12 CAP                   CAP-5V BYPASS                      X: 1.10 Y:-1.10
R06P12 R06P12   1  ;GND      CAP-5V BYPASS                      X: 1.10 Y:-1.10
R05P12 R06P12   2  ;5V       CAP-5V BYPASS                      X: 0.80 Y:-1.10

R08P12 CAP                   CAP-5V BYPASS                      X: 1.50 Y:-1.10
R08P12 R08P12   1  ;GND      CAP-5V BYPASS                      X: 1.50 Y:-1.10
R07P12 R08P12   2  ;5V       CAP-5V BYPASS                      X: 1.20 Y:-1.10
```

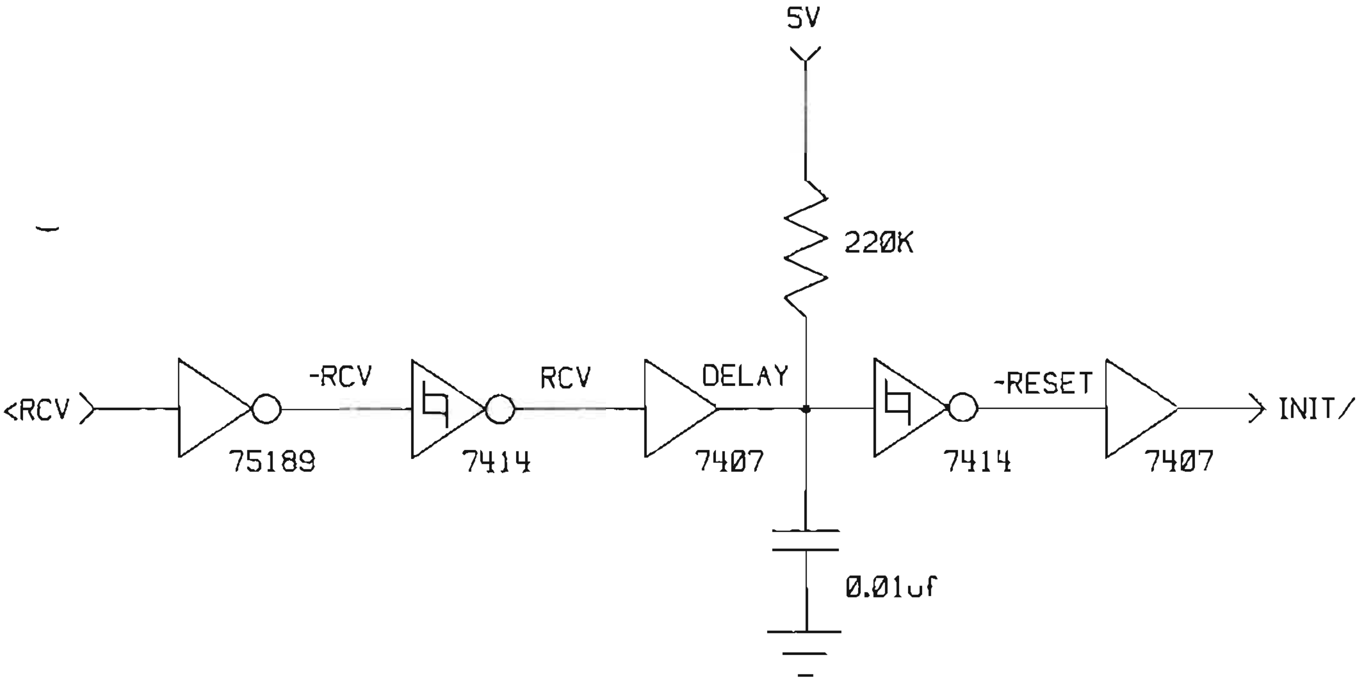
```
R10P12 CAP                    CAP-5V BYPASS                    X: 1.90 Y:-1.10
R10P12 R10P12   1  ;GND       CAP-5V BYPASS                    X: 1.90 Y:-1.10
R09P12 R10P12   2  ;5V        CAP-5V BYPASS                    X: 1.60 Y:-1.10

R08P03 DIP16                  COMP-RESET ANALOG                X: 1.50 Y:-0.20
R08P03 R08P03   1   NC        COMP-RESET ANALOG                X: 1.50 Y:-0.20
R08P04 R08P03   2   NC        COMP-RESET ANALOG                X: 1.50 Y:-0.30
R08P05 R08P03   3   NC        COMP-RESET ANALOG                X: 1.50 Y:-0.40
R08P06 R08P03   4   NC        COMP-RESET ANALOG                X: 1.50 Y:-0.50
R08P07 R08P03   5  !DELAY     COMP-RESET ANALOG                X: 1.50 Y:-0.60
R08P08 R08P03   6   NC        COMP-RESET ANALOG                X: 1.50 Y:-0.70
R08P09 R08P03   7   NC        COMP-RESET ANALOG                X: 1.50 Y:-0.80
R08P10 R08P03   8  !DELAY     COMP-RESET ANALOG                X: 1.50 Y:-0.90
R07P10 R08P03   9   5V        COMP-RESET ANALOG                X: 1.20 Y:-0.90
R07P09 R08P03  10   NC        COMP-RESET ANALOG                X: 1.20 Y:-0.80
R07P08 R08P03  11   NC        COMP-RESET ANALOG                X: 1.20 Y:-0.70
R07P07 R08P03  12   GND       COMP-RESET ANALOG                X: 1.20 Y:-0.60
R07P06 R08P03  13   NC        COMP-RESET ANALOG                X: 1.20 Y:-0.50
R07P05 R08P03  14   NC        COMP-RESET ANALOG                X: 1.20 Y:-0.40
R07P04 R08P03  15   NC        COMP-RESET ANALOG                X: 1.20 Y:-0.30
R07P03 R08P03  16   NC        COMP-RESET ANALOG                X: 1.20 Y:-0.20

MANUAL RIB26                  RIB26 CONNECTOR CHANNEL 3        X: 8.80 Y:-5.80
R42OFF MANUAL   1   GND       RIB26 CONNECTOR CHANNEL 3        X: 8.80 Y:-5.80
R42OFF MANUAL   2  $NC        RIB26 CONNECTOR CHANNEL 3        X: 8.80 Y:-5.90
R43OFF MANUAL   3  $<RCV      RIB26 CONNECTOR CHANNEL 3        X: 8.90 Y:-5.80
R43OFF MANUAL   4   NC        RIB26 CONNECTOR CHANNEL 3        X: 8.90 Y:-5.90
R43OFF MANUAL   5   NC        RIB26 CONNECTOR CHANNEL 3        X: 9.00 Y:-5.80
R43OFF MANUAL   6   NC        RIB26 CONNECTOR CHANNEL 3        X: 9.00 Y:-5.90
R44OFF MANUAL   7   GND       RIB26 CONNECTOR CHANNEL 3        X: 9.10 Y:-5.80
R44OFF MANUAL   8   NC        RIB26 CONNECTOR CHANNEL 3        X: 9.10 Y:-5.90
R44OFF MANUAL   9   NC        RIB26 CONNECTOR CHANNEL 3        X: 9.20 Y:-5.80
R44OFF MANUAL  10   NC        RIB26 CONNECTOR CHANNEL 3        X: 9.20 Y:-5.90
R45OFF MANUAL  11   NC        RIB26 CONNECTOR CHANNEL 3        X: 9.30 Y:-5.80
R45OFF MANUAL  12   NC        RIB26 CONNECTOR CHANNEL 3        X: 9.30 Y:-5.90
R45OFF MANUAL  13   NC        RIB26 CONNECTOR CHANNEL 3        X: 9.40 Y:-5.80
R45OFF MANUAL  14   NC        RIB26 CONNECTOR CHANNEL 3        X: 9.40 Y:-5.90
R46OFF MANUAL  15   NC        RIB26 CONNECTOR CHANNEL 3        X: 9.50 Y:-5.80
R46OFF MANUAL  16   NC        RIB26 CONNECTOR CHANNEL 3        X: 9.50 Y:-5.90
R46OFF MANUAL  17   NC        RIB26 CONNECTOR CHANNEL 3        X: 9.60 Y:-5.80
R46OFF MANUAL  18   NC        RIB26 CONNECTOR CHANNEL 3        X: 9.60 Y:-5.90
R47OFF MANUAL  19   NC        RIB26 CONNECTOR CHANNEL 3        X: 9.70 Y:-5.80
R47OFF MANUAL  20   NC        RIB26 CONNECTOR CHANNEL 3        X: 9.70 Y:-5.90
R47OFF MANUAL  21   NC        RIB26 CONNECTOR CHANNEL 3        X: 9.80 Y:-5.80
R47OFF MANUAL  22   NC        RIB26 CONNECTOR CHANNEL 3        X: 9.80 Y:-5.90
R48OFF MANUAL  23   NC        RIB26 CONNECTOR CHANNEL 3        X: 9.90 Y:-5.80
R48OFF MANUAL  24   NC        RIB26 CONNECTOR CHANNEL 3        X: 9.90 Y:-5.90
R48OFF MANUAL  25   NC        RIB26 CONNECTOR CHANNEL 3        X:10.00 Y:-5.80
R48OFF MANUAL  26   NC        RIB26 CONNECTOR CHANNEL 3        X:10.00 Y:-5.90
```

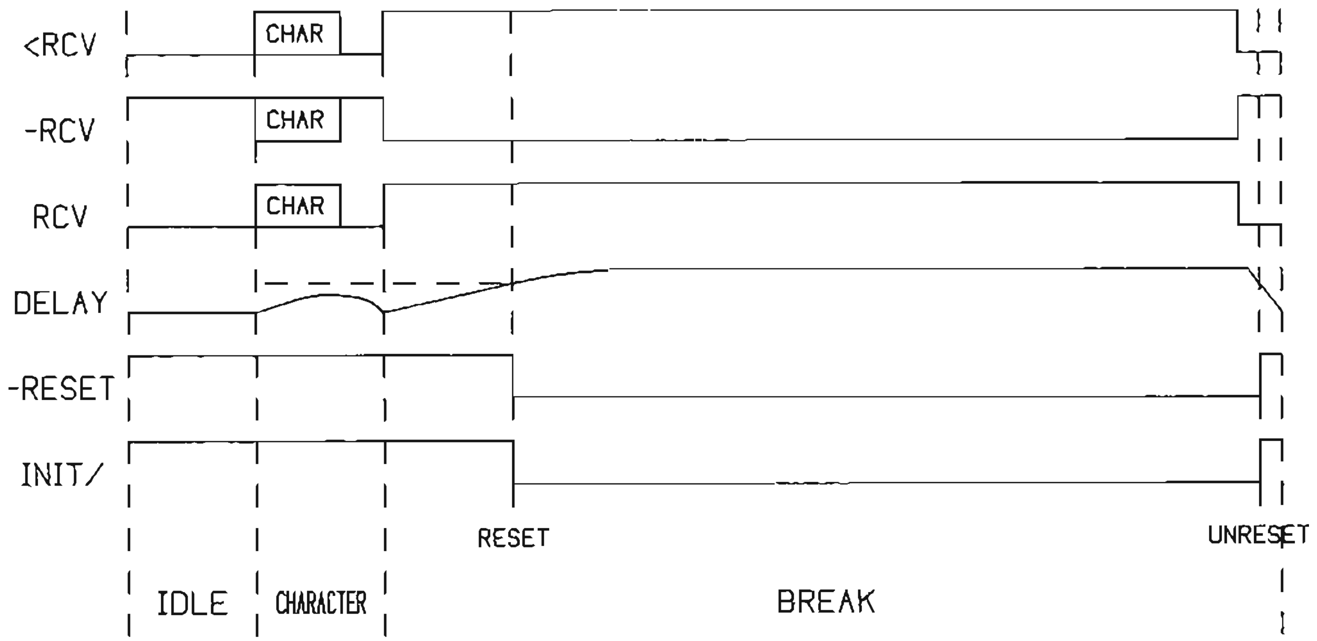
BREAK DETECTOR

Schematic Diagram



BREAK DETECTOR

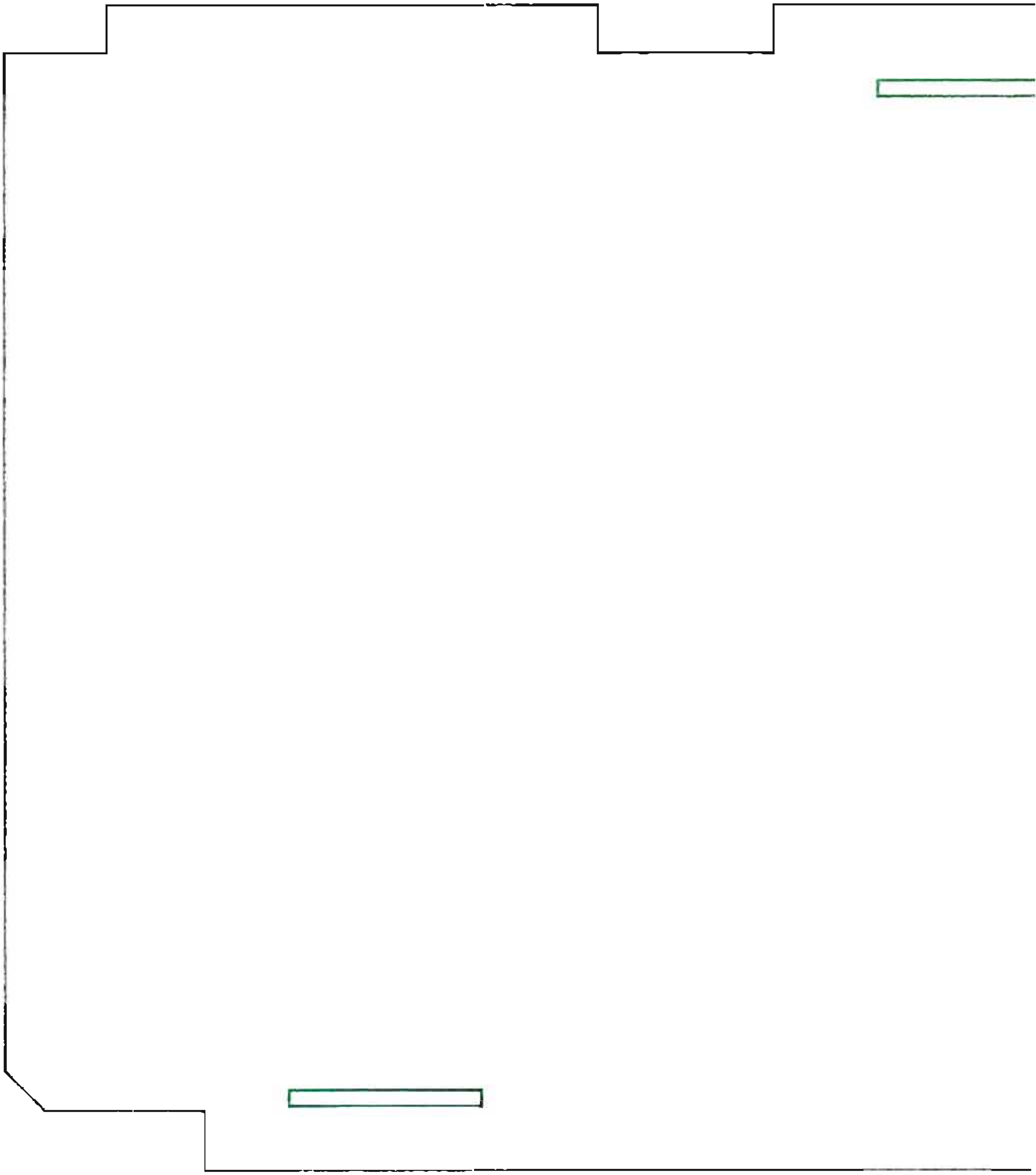
Timing Diagram



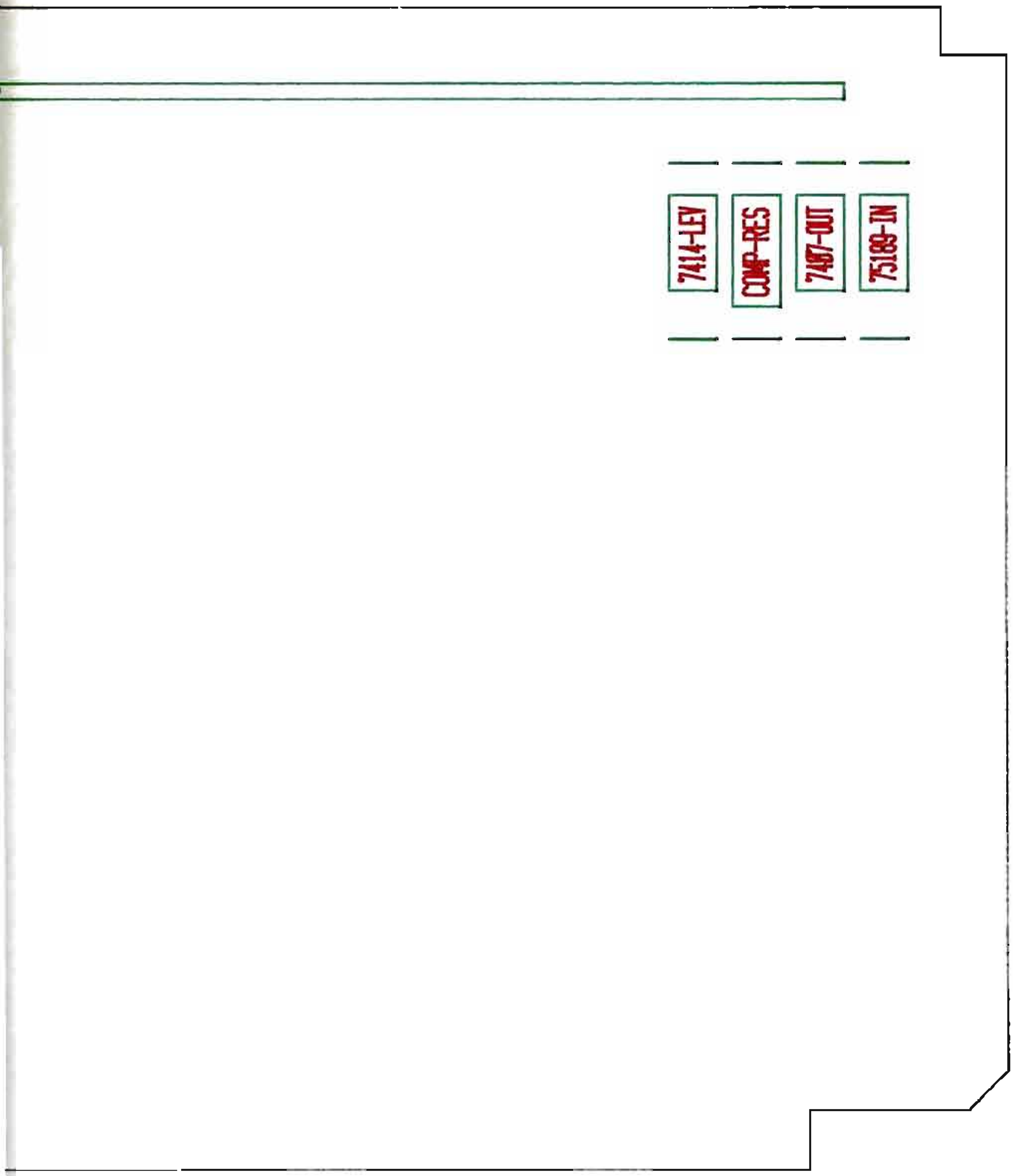
SCALE: 2ms/inch
BAUD RATE: 9600
TIME CONSTANT: 220K x 0.01uf = 2.2ms

FOLD

HEWLETT-PACKARD
9280-0180
FOR USE ON HEWLETT PACKARD RECORDERS



FOLD


7414-LEV
COMP-RES
7407-OUT
75189-IN

Part 2

FIB MEMORY MAP

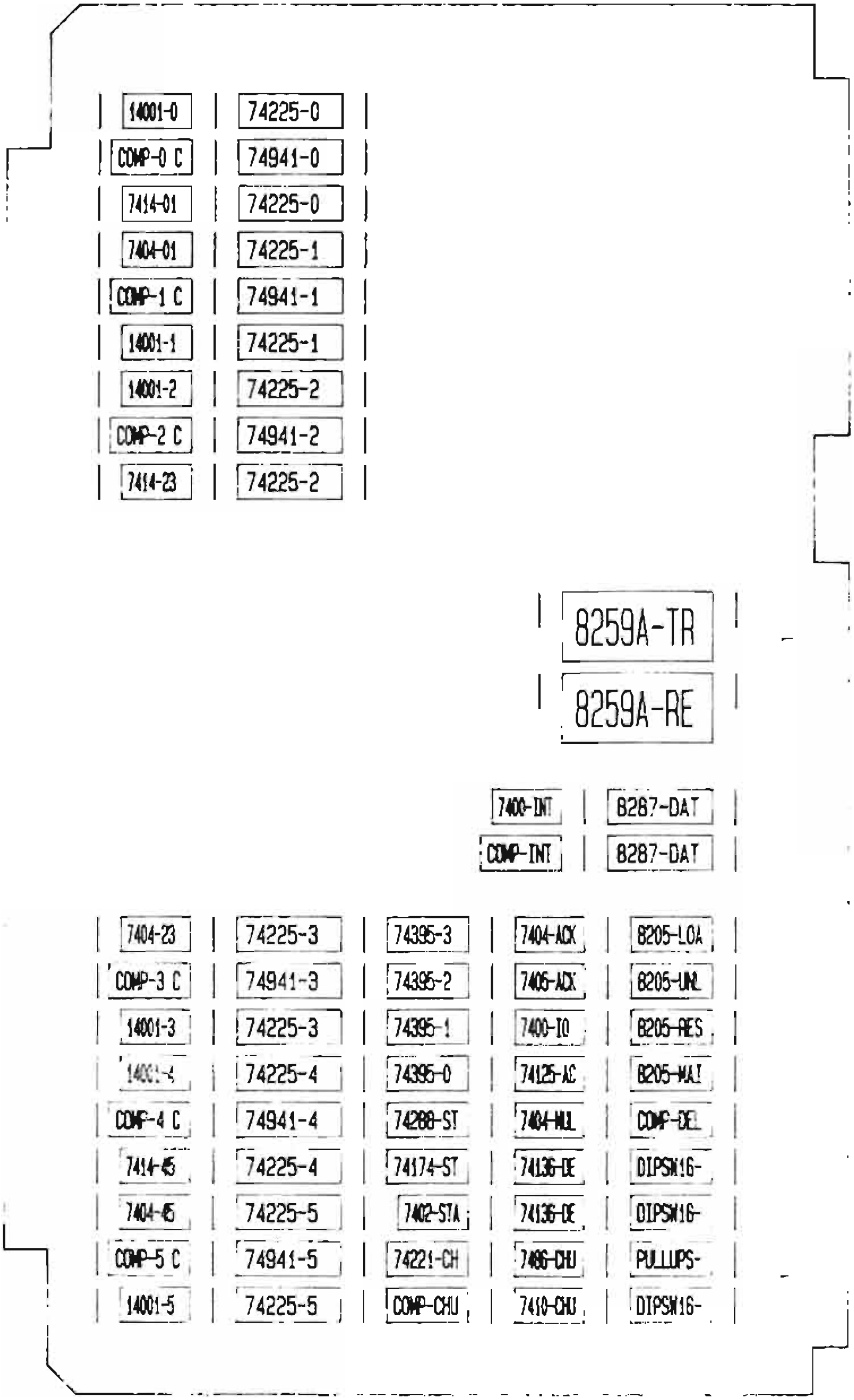
```
                --------------------
    IP32        : TX PIC READ      :
                --------------------
    IP30        : TX PIC WRITE     :
                --------------------
    IP2E        :                  :
                --------------------
                         .
                         .
                         .
                --------------------
    IP24        :                  :
                --------------------
    IP22        : RX PIC READ      :
                --------------------
    IP20        : RX PIC WRITE     :
                --------------------
    IP1E        :                  :
                --------------------
    IP1C        :                  :
                --------------------
    IP1A        : FIFO5 RESET      :
                --------------------
    IP18        : FIFO4 RESET      :
                --------------------
    IP16        : FIFO3 RESET      :
                --------------------
    IP14        : FIFO2 RESET      :
                --------------------
    IP12        : FIFO1 RESET      :
                --------------------
    IP10        : FIFO0 RESET      :
                --------------------
    IP0E        :                  :
                --------------------
    IP0C        :                  :
                --------------------
    IP0A        : FIFO5 DATA       :
                --------------------
    IP08        : FIFO4 DATA       :
                --------------------
    IP06        : FIFO3 DATA       :
                --------------------
    IP04        : FIFO2 DATA       :
                --------------------
    IP02        : FIFO1 DATA       :
                --------------------
    IP00        : FIFO0 DATA       :
                --------------------
```

```
Note:    IP is the page in the I/O segment.


-   -----------------------------------------------------------------
: adr7 : adr6 : adr5 : adr4 : adr3 : adr2 : adr1 : adr0 :
-----------------------------------------------------------------
   :      :      :      :      :      :      :      :_______ not used
   :      :      :      :      :      :      :______________ FIFO and PIC select
   :      :      :      :      :      :_____________________ FIFO select
   :      :      :      :      :____________________________ FIFO select
   :      :      :      :___________________________________ DATA/RESET enable
   :      :      :__________________________________________ FIFO/PIC enable
   :      :_________________________________________________ not used
   :________________________________________________________ not used

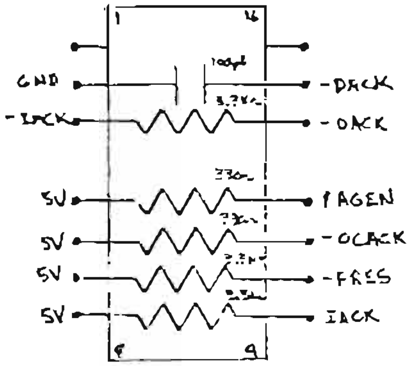

 IO            = -(-iorc ^ iowc)
```

```
;
;code for the state machine prom, 74s288
;
;   puts:
;    7        6        5        4        3        2        1        0
; -fifoi   -fifoo   loadsr   -fackx -sren    nst2     nst1     nst0
;
;inputs:
;    4        3        2        1        0
; -fifos  -iorc    nst2     nst1     nst0
;
;input meanings:
; -fifos  -iorc
;    0        0        read from fifo
;    0        1        write into fifo
;    1        0        not accessed
;    1        1        not accessed
;
fifoi    =        128
fifoo    =        64
loadsr   =        32
fackx   =        16
sren     =        8
;
        asect    0
;
        byte     1    +    fifoo+fackx
        byte     2    +    fifoo+fackx
        byte     3    +    fifoo+fackx
        byte     4    +    fifoo+fackx
        byte     4    +    fifoi+fifoo+sren;assert acknowledge and wait for reply
        byte     4    +    fifoi+fifoo+fackx+sren
        byte     4    +    fifoi+fifoo+fackx+sren
        byte     4    +    fifoi+fifoo+fackx+sren
;
        byte     1    +    fifoi+fifoo+loadsr+fackx
        byte     2    +    fifoi+sren+fackx
        byte     3    +    fifoi+fackx
        byte     4    +    fifoi+fackx
        byte     5    +    fifoi+fackx
        byte     5    +    fifoi+fifoo+sren;assert acknowledge and wait for reply
        byte     5    +    fifoi+fifoo+fackx+sren
        byte     5    +    fifoi+fifoo+fackx+sren
;
        byte     0    +    fifoi+fifoo+fackx+sren
        byte     0    +    fifoi+fifoo+fackx+sren
        byte     0    +    fifoi+fifoo+fackx+sren
        byte     0    +    fifoi+fifoo+fackx+sren
        byte     0    +    fifoi+fifoo+fackx+sren
        byte     0    +    fifoi+fifoo+fackx+sren
        byte     0    +    fifoi+fifoo+fackx+sren
        byte     0    +    fifoi+fifoo+fackx+sren
;
        byte     0    +    fifoi+fifoo+fackx+sren
        byte     0    +    fifoi+fifoo+fackx+sren
        byte     0    +    fifoi+fifoo+fackx+sren
        byte    0   +   fifoi+fifoo+fackx+sren
        byte    0   +   fifoi+fifoo+fackx+sren
        byte    0   +   fifoi+fifoo+fackx+sren
        byte    0   +   fifoi+fifoo+fackx+sren
        byte    0   +   fifoi+fifoo+fackx+sren
```

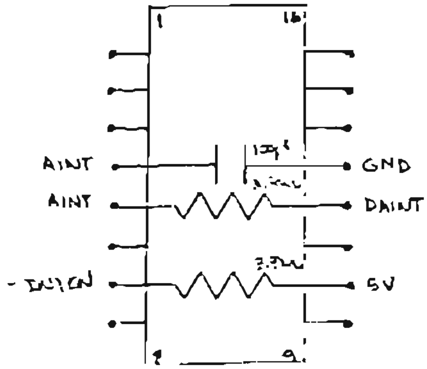

14001-0
74225-0
COMP-0 C
74941-0
7414-01
74225-0
7404-01
74225-1
COMP-1 C
74941-1
14001-1
74225-1
14001-2
74225-2
COMP-2 C
74941-2
7414-23
74225-2
8259A-TR
8259A-RE
7400-INT
8287-DAT
COMP-INT
8287-DAT
7404-23
74225-3
74395-3
7404-ACK
8205-LOA
COMP-3 C
74941-3
74395-2
7406-ACK
8205-UNL
14001-3
74225-3
74395-1
7400-IO
8205-RES
14001-4
74225-4
74395-0
74125-AC
8205-MAI
COMP-4 C
74941-4
74288-ST
7404-MUL
COMP-DEL
7414-45
74225-4
74174-ST
74136-DE
DIPSW16-
7404-45
74225-5
7402-STA
74136-DE
DIPSW16-
COMP-5 C
74941-5
74221-CH
7486-CHU
PULLUPS-
14001-5
74225-5
COMP-CHU
7410-CHU
DIPSW16-

BFIB
COMPS and DIPSWS.

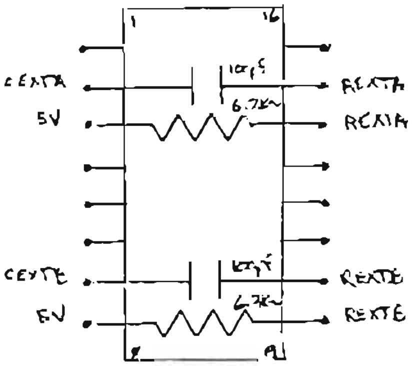
COMPS;



R12P03
DELAY AND PULLUP



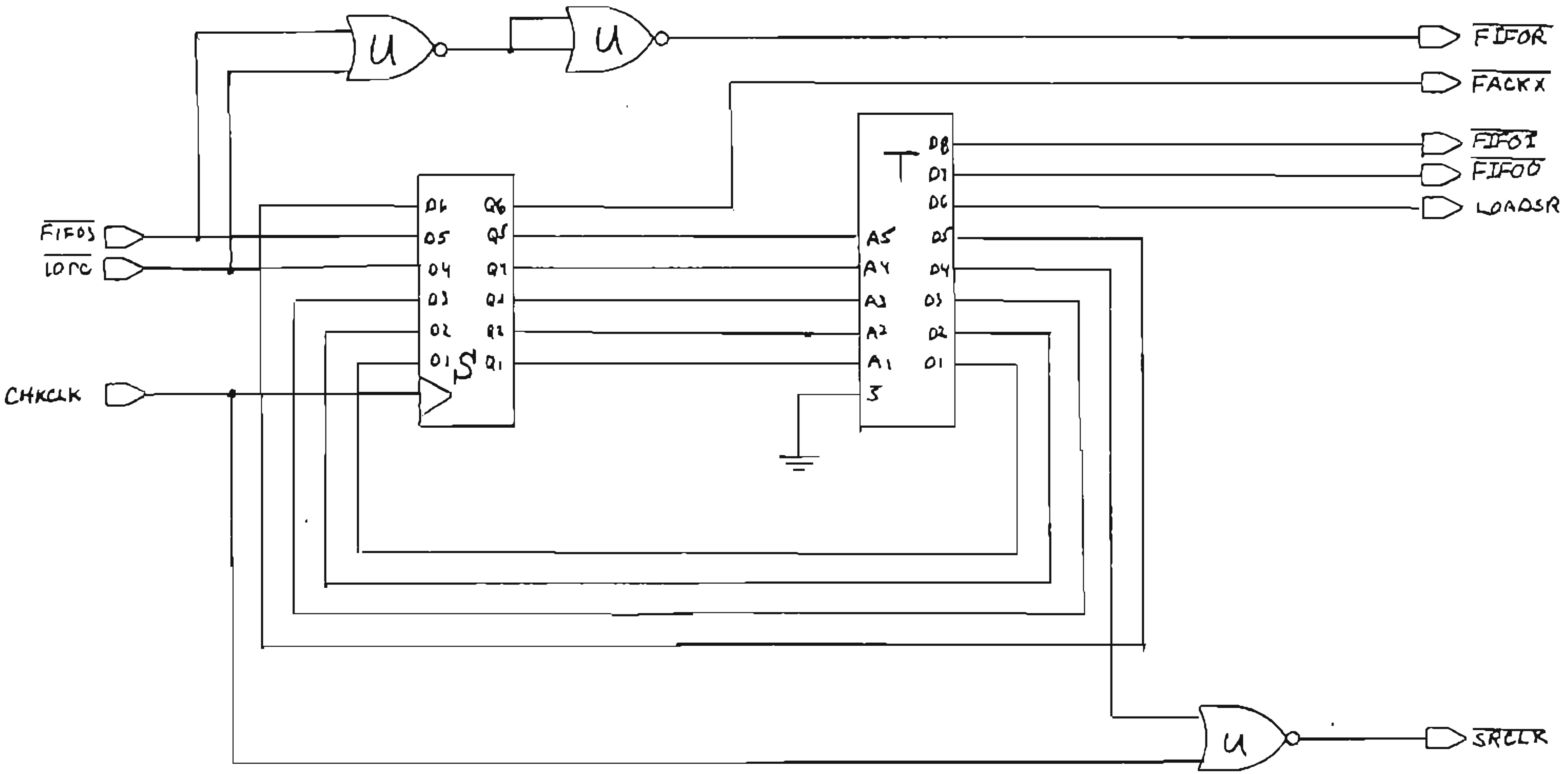
R23P16
INTERRUPT ACKNOWLEDGE



R04P24
CHUCK CLOCK

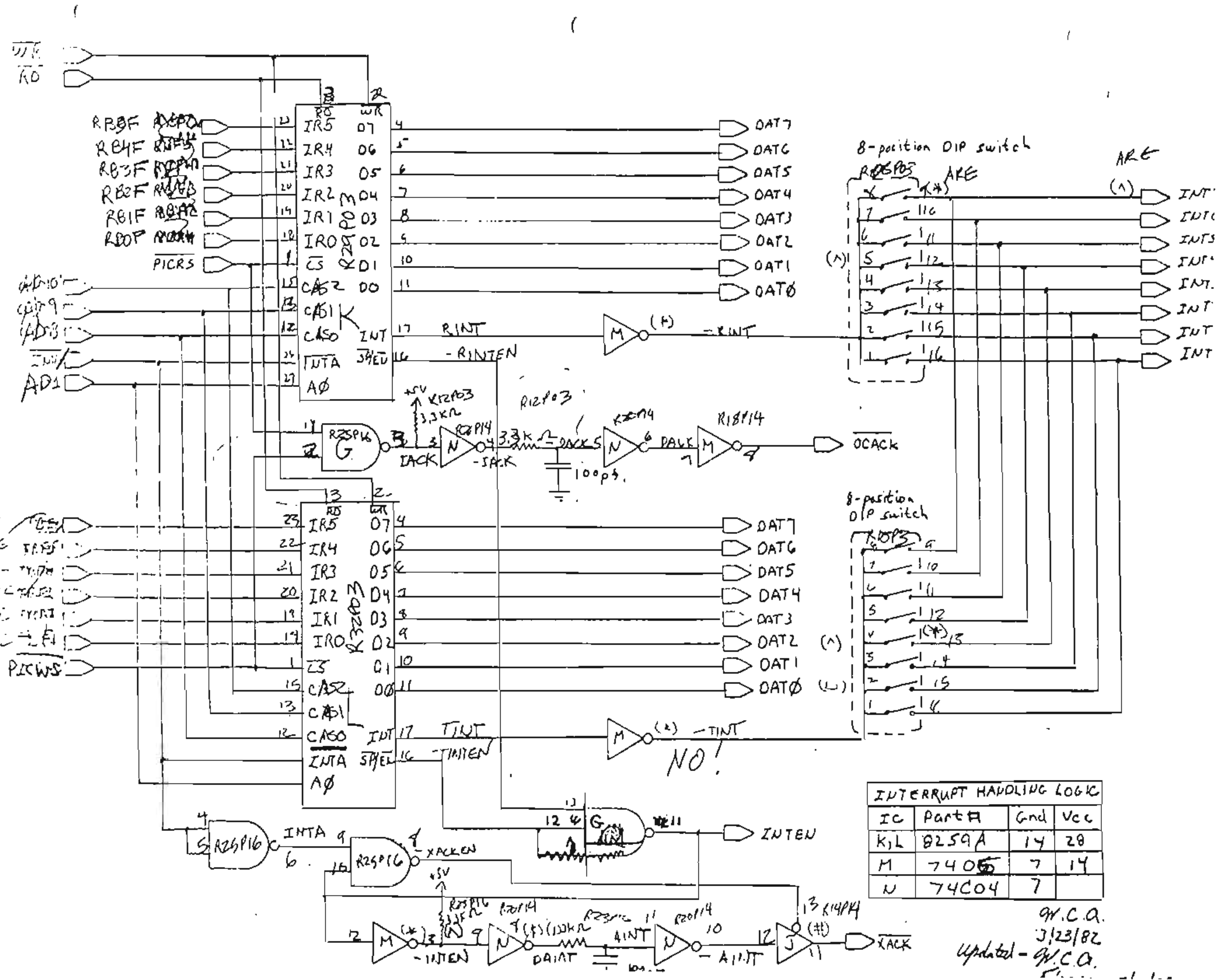
DIPSWS;

DIPSW	POSITION	ON/OFF	MEANING
R04P03	1 2 3 4 5 6 7 8	OFF OFF OFF OFF OFF OFF OFF OFF	PAGE SELECT = FF
R02P03	1 2 3 4 5 6 7 8	OFF OFF OFF ON OFF OFF OFF OFF	RECEIVE INTERRUPT NUMBER = 4
[illegible]	1 2 3 4 5 6 7 8	OFF OFF ON OFF ON OFF OFF OFF	TRANSMIT INTERRUPT NUMBER = 5



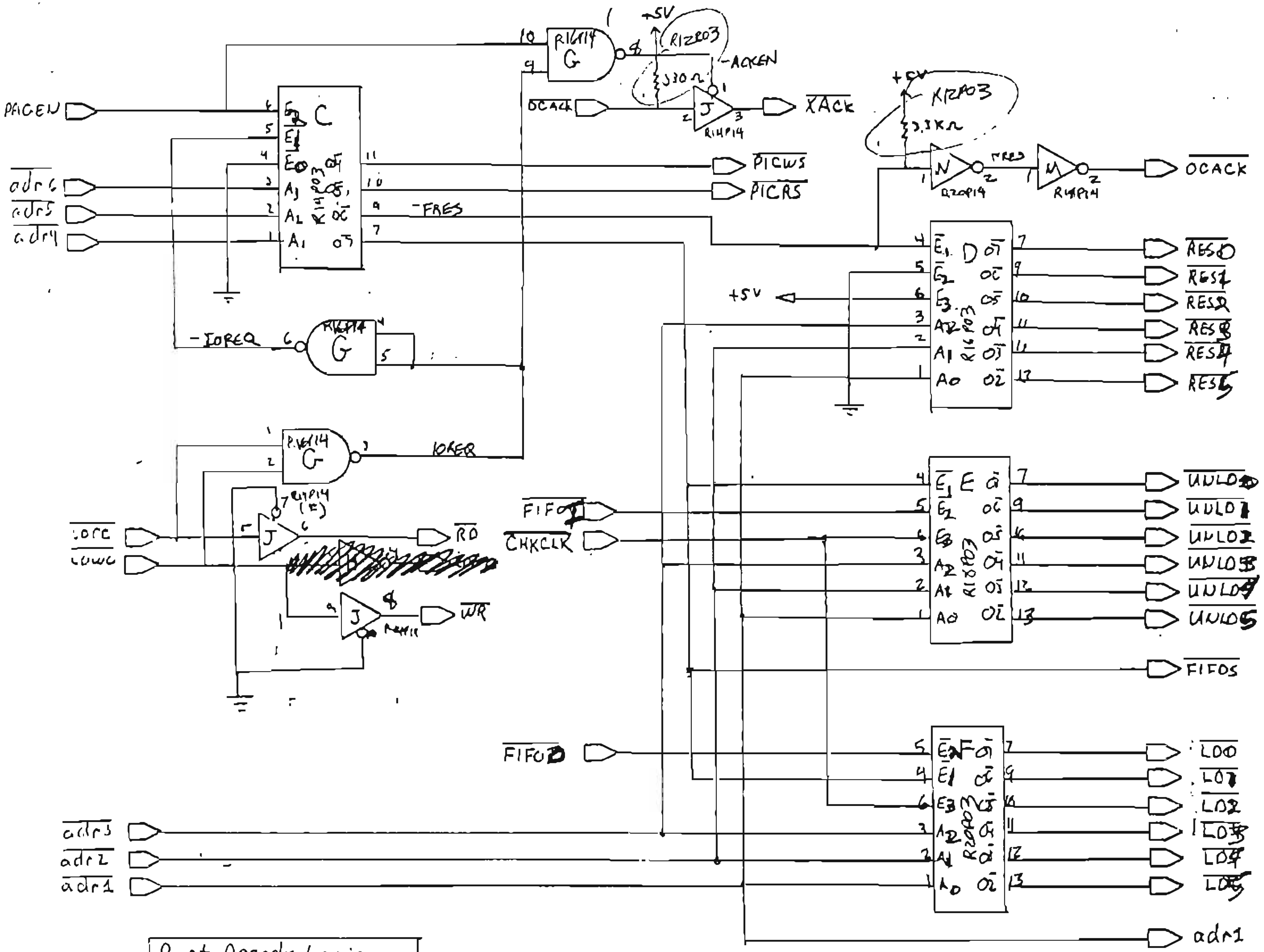
STATE MACHINE			
IC	IC #	Gnd	Vcc
S	74174	8	16
T	74S288	8	16
U	7402	7	14

W.C.O.
4/17/86



INTERRUPT HANDLING LOGIC			
IC	Part #	Gnd	Vcc
K,L	8259A	14	28
M	74065	7	14
N	74C04	7	

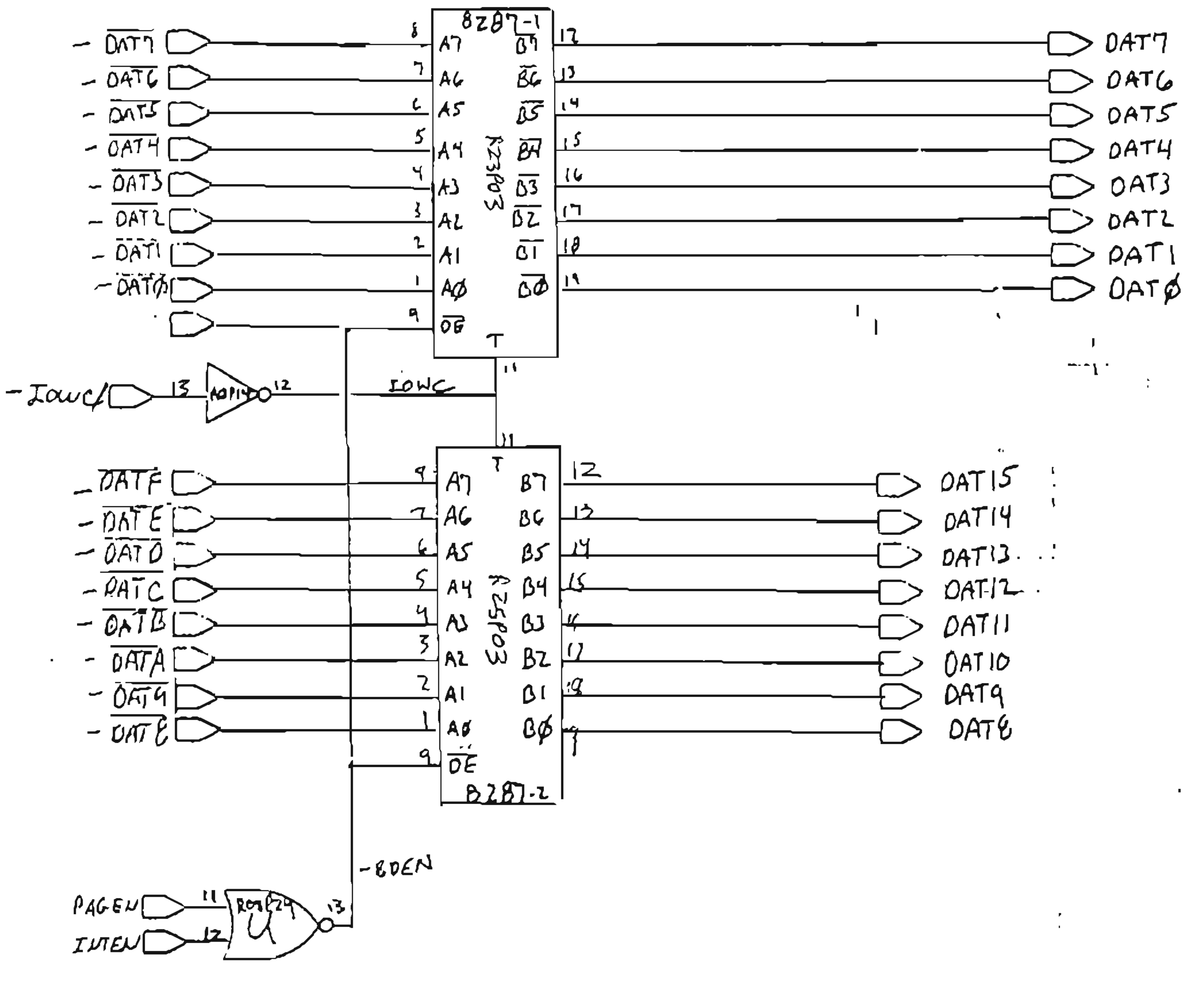
W.C.Q.
3/23/82
Updated - W.C.Q.



Port Decode Logic

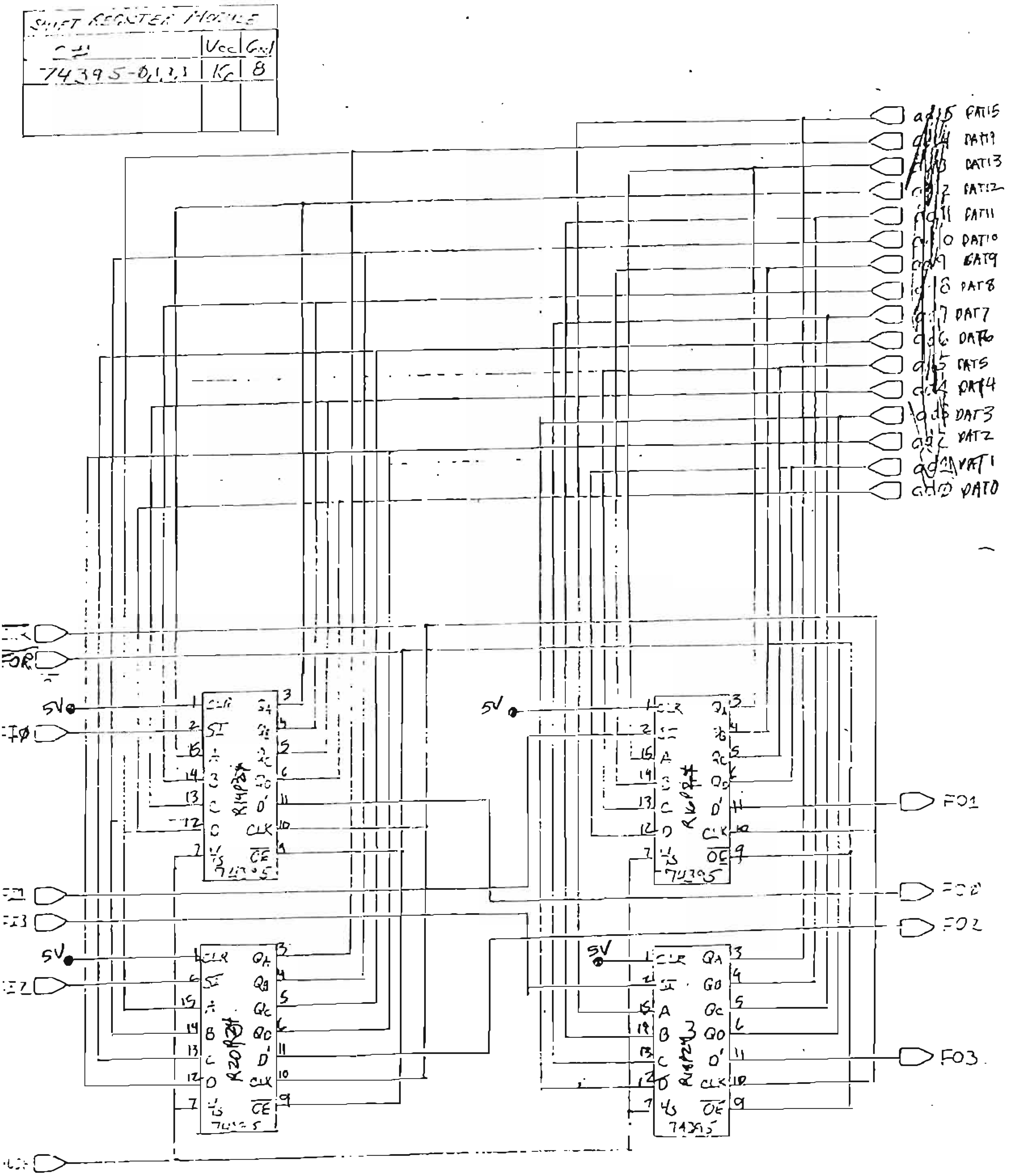
IC	Part #	gnd	Vcc
C,D,E,F	8205	8	16
G	7400	7	14
H	74S04	7	14
J	74125	7	14

gr.c.a.
4/23/82

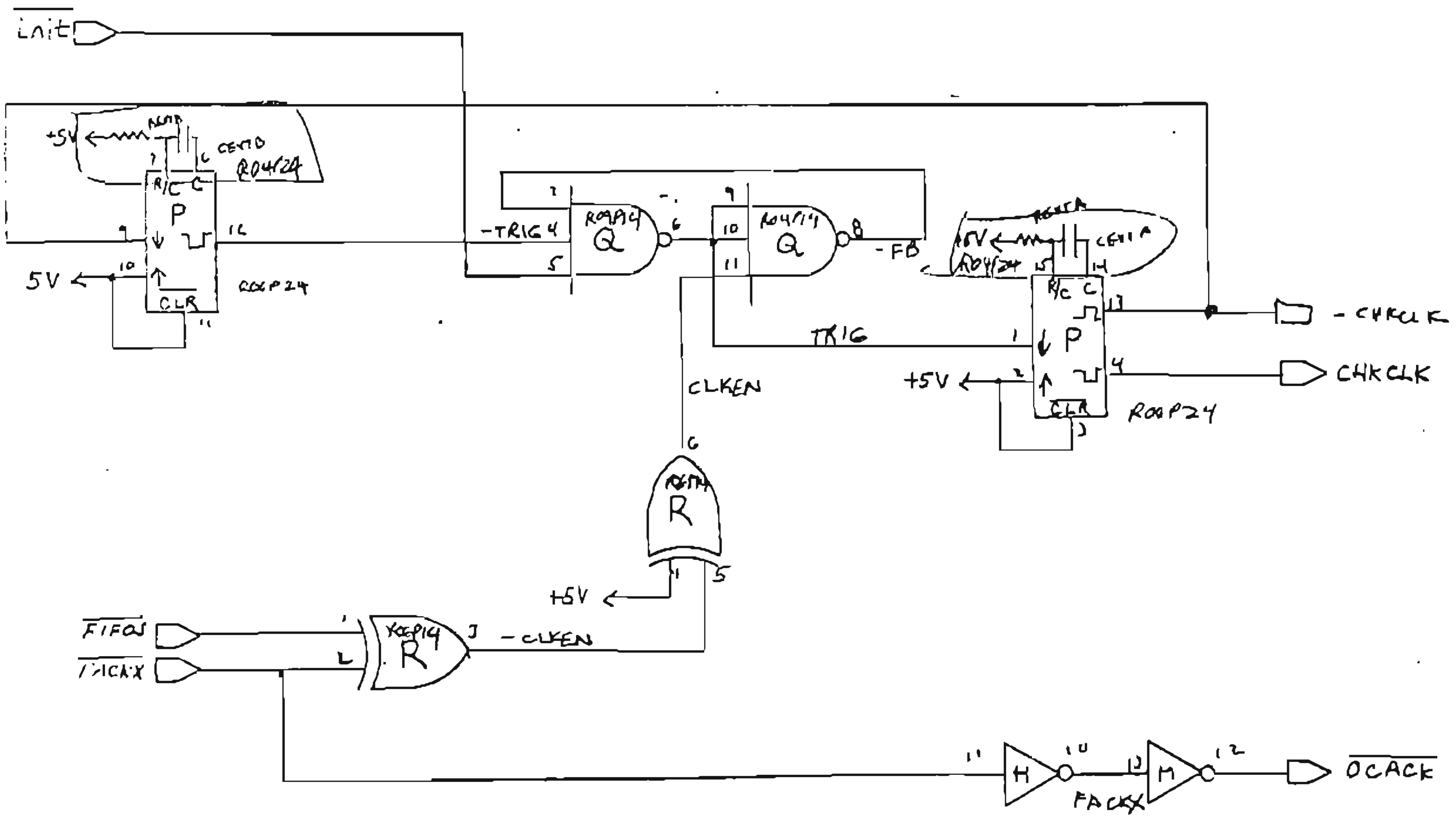


DATA BUS ISOLATION		
I.C.#	Gnd	Vcc
8287-1,2	10	20

Updated Ar. C.A.
5/28/82


SHIFT REGISTER MODULE

C#	Vcc	Gnd
74395-0,1,2,3	16	8



CHUCK CLOCK			
ICH	Part #	Gnd	Vcc
P	74221	8	16
Q	7410	7	14
R	7486	7	14

GV.C.A.
4/23/82
Updated:- GV. C.A.
5/28/82

Homogeneous Machine
Instructions for Contractor

7 June 1982

W. C. Athas

Erik P. DeBenedictis

The research described in this document was sponsored by the Defense Advanced Research Projects Agency, ARPA Order number 3771, and monitored by the Office of Naval Research under contract number N00014-79-C-0597.

1 Overall Requirements:

The California Institute of Technology (Caltech) Computer Science Department requires that the current design of its Homogeneous Machine Processor (HMP) be constructed on a printed circuit (PC) board and replicated 80 times. The wire-wrapped version of the HMP has been tested to Caltech's satisfaction and it is required that the PC version perform equally or better than the wire-wrapped version. Materials supplied by Caltech will be a set of block diagrams and the wire-wrap lists. Services required by the contractor(s) will be the following:

1. Transferring of wire-wrap lists to PC masks
2. Fabrication of PC boards from masks
3. Stuffing of PC boards with components.
4. Testing assembled boards.

2 Homogeneous Machine Tutorial:

Due to the uniqueness of the Homogeneous Machine project, the following brief explanation of the machine is given. The entire Homogeneous Machine is an interconnection of 64 HMP's configured as a Boolean 6-cube, or in other terms, a 6 dimensional hypercube. For the uninitiated, this requires that each HMP have a 6 bit binary number that uniquely determines its location in the hypercube. The 6 bit binary number represents an ordered 6-tuple where each bit represents the HMP's coordinate in a six dimensional space where each coordinate may only have the binary value of 0 or 1. Two HMP's will only be connected if and only if there 6 bit-numbers differ in exactly one location. For example, where bit 5 is the most left bit and bit 0 is the most right:

000000 and 000001 are connected since only bit 0 differ.

000000 and 000011 are not connected since bits 0 and 1 differ.

011111 and 111111 are connected since only bit 7 differ.

101010 and 010101 are not connected since all the bits differ.

Each HMP has 6 interconnections to 6 other HMP's, in addition to these connections, there is a global control bus which supplies the hyporcube with:

1. clock
2. reset
3. sync
4. miscellaneous global communication lines

3 Design Materials Provided by Caltech:

3.1 Wire Lists:

The wire lists are the definitive description of the HMP's, they will be the only document guaranteed by Caltech as being the correct description of the HMP. The wire lists describe the interconnection of all components including edge connectors which are represented as a series of wire-wrap posts. No information on component placement is available from the wire lists. Any instances where it is desired that logical elements be re-wired to simplify PC layout while maintaining the functional integrity of the HMP must have written approval from Caltech.

3.2 Block Diagrams:

A set of block diagrams will be supplied that show in detail both control and data flow.

4 Design Materials Not Provided by Caltech:

Caltech is not responsible for the following list of items:

1. Component placement
2. Placement and construction of connectors
3. Power distribution within the HMP board

5 Homogeneous Machine System Requirements:

The Homogeneous Machine System will consist of the following modules:

1. 64 HMP's
2. Chassis
3. Dedicated Host Computer
4. Power Supply

5.1 Homogeneous Machine Chassis:

The HMP's will be required to connect to a chassis that the contractor will provide. The contractor is responsible for the design of the edge connector which will mate with the chassis to provide:

1. power supply voltages
2. control bus interface
3. six interprocessor connections

The chassis will consist of a backplane for wiring all of the edge connector signals for all 64 boards. In addition is must have provisions for the dedicated host computer.

5.2 Dedicated Host Computer:

The dedicated host computer will be constructed by Caltech. It will be made available to the contractor on a limited basis for testing purposes. The dedicated host will consist of a 12 slot Multibus[1] and a separate power supply. It will be necessary that the contractor provide sufficient space within the Homogeneous Machine cabinet for the dedicated host. It will require an easily accessible front panel consisting of six switches. Space must also be provided for behind the dedicated host to accommodate numerous terminal lines and high speed data links.

5.3 Power Supply

The entire machine will require a power supply of 5 volts at 130 amps. For diagnostic purposes, the power supply must be adjustable from 4 to 6 volts. The reference voltage for the power supply will be derived from the dedicated host computer which the power supply must dynamically track.

5.4 Special HMP's:

The interfacing of the dedicated host with the Homogeneous Machine will be through HMP's which have 7 connectors instead of 6. The first six connections will interface the spatial array in the normal manner but the seventh will be connected to the dedicated host. These special HMP's will be wire-wrapped and will be provided by Caltech, but provisions for Interfacing to the dedicated host must be made by the contractor.

Although how this is actually done is left to the discretion of the contractor, the following scheme is recommended. The backplane be constructed so that it will accept a wire-wrap board in any slot, this requires that the spacing between slots be double the normal board depth. The one additional connection to the dedicated host would be made through a ribbon cable. It is recommended that the arrangement of connectors on the HMP boards agree with some standardize format, In particular, the Intel Multibus.

5.5 Further Cabinet Requirements

The HMP's must be air cooled. The dedicated host also requires air flow and is currently equipped with a fan, this fan may be removed by the contractor.

6 Components of the HMP:

6.1 Integrated Circuit Sockets:

Two types of sockots will be required based on the predicted necessity of replacing the components, all integrated circuits for the HMP will be classified as follows:

Frequent: Frequently replaceable components include those that will be replaced in the normal operation of the system, for example: EPROMS. Components classified as Frequent require an AUGAT socket or equivalent.

[1] IEEE 796 bus.

Occasional: Occasionally replaceable components include those that are expected to be replaced in the operation of the machine either due to device failure or an operational modification in the machine. These include the FIFO interface drivers and RAMs. Components classified as Occasional require a socket.

Infrequent: Components expected to be replaced infrequently are those that will only be replaced upon very infrequent failure. These devices will not be socketed.

6.2 Component testing:

The contractor will be required to supply all components for the HMP's except for the Intel 8086's and 8087's. The system will initially be constructed with 5 MHz 8086's and no 8087's. The HMP's will be expected to perform at a maximum clock speed of 10 MHz, to verify this, a small number of 10 MHz 8086's will be made available to the contractor. When the 10 MHz 8086's and the 8087's become available, they will be installed into the Homogeneous Machine by Caltech.

7 Testing of Assembled Boards:

Caltech requires that the functionality of all components on the assembled HMP's be verified, To accomplish this, Caltech will provided a testing interface and diagnostic programs. Proper execution of the diagnostics will be satisfactory verification of the assembled boards.

2. Calling Conventions

A convention for calling procedures both in user programs and in the monitor is proposed to aid in debug and to allow relocation of processes.

There are two operating modes relavant to the procedure calling conventions: user and monitor. Within each operating mode there are several conventions for procedure calls. In addition, there is a convention for user programs calling procedures in the monitor.

The distinction between user and monitor mode is based upon where the executing code is located. When the code segment register has the address of the currently executing monitor the system is in monitor mode, otherwise it is in user mode.

A procedure that executes from the monitor segment is termed a monitor procedure. Other procedures are termed user procedures. A call executed from code that is in the monitor segment is called a monitor call. Other calls are called user calls.

2.1 Conventions for User Procedures

2.1.1 Simple User Procedures

Simple calls pass arguments in the accumulators and do not alter the stack frame.

```
             Simple User Call
                                    arguments in accumulators
             call       addr        simple call
                                    return arguments in accumulators

             Simple User Procedure
addr:                               body goes here
             ret                    return
```

2.1.2 Normal User Procedures

Normal calls pass arguments on the stack and cause the establishment of a new stack frame.

```
             Normal User Call
             push       arg n       arguments in reverse order
             push         .
             push         .
             push         .
             push       arg 1       first argument
             call       addr        simple call
             add        sp,#2*n     fixup stack from pushes
```

```
            Normal User Procedure
addr:       push        bp          save old stack frame
            mov         bp,sp       new stack frame
            ...code...              body goes here, using [bp+4],
                                    [bp+6]... as arguments
            pop         bp          restore old stack frame
            ret                     return
```

2.2 Conventions for Monitor Procedures

2.2.1 Simple Monitor Procedures

Simple calls pass arguments in the accumulators and do not alter the stack frame.

```
            Simple Monitor Call
                                    arguments in accumulators
            call        addr        simple call
                                    return arguments in accumulators

            Simple Monitor Procedure
addr:       ...code...              body goes here
            ret                     return
```

2.2.2 Normal Monitor Procedures

Normal calls pass arguments on the stack and cause the establishment of a new stack frame.

```
            Normal Monitor Call
            push        arg n       arguments in reverse order
            push        .
            push        .
            push        .
            push        arg 1       first argument
            push        cs          push cs onto stack
            call        addr        simple call
            add         sp,#2*n     fixup stack from pushes

            Normal Monitor Procedure
addr:       push        bp          save old stack frame
            mov         bp,sp       new stack frame
            ...code...              body goes here, using [bp+6],
                                       [bp+8]... as arguments
            pop         bp          restore old stack frame
            retl                    long return
```

2.2.3 Interrupt Monitor Procedures

Interrupt calls are like normal calls excapt that the flags are pushed. The address of an interrupt monitor procedure can be put into the interrupt table.

```
          Interrupt Monitor Call
          push      arg n        arguments in reverse order
          push        .
          push        .
          push        .
          push      arg 1        first argument
          pushf                  push flags
          push      cs           push cs onto stack
          call      addr         simple call
          add       sp,#2*n      fixup stack from pushes

          Interrupt Monitor Procedure
addr:     push      bp           save old stack frame
          mov       bp,sp        new stack frame
          ...code...             body goes here, using [bp+8],
                                    [bp+10]... as arguments
          pop       bp           restore old stack frame
          iret                   long return
```

2.3 Monitor Entry Techniques

This section discusses techniques whereby user code can invoke monitor procedures.

2.3.1 User Call of a Simple Monitor Procedure

Cannot be done.

2.3.2 User Call of a Normal Monitor Procedure

Use of this is strongly discouraged since it is inconsistent with a relocation algorithm -- it depends on a set monitor address.

```
Direct Normal Monitor Entry
push      arg n          arguments in reverse order
push        .
push        .
push        .
push      arg 1          first argument
calll     monitr,addr simple call
add       sp,#2*n        fixup stack from pushes
```

2.3.3 User Call of a Interrupt Monitor Procedure

Use of this is strongly discouraged since It Is Inconsistent with a relocation algorithm -- It depends on a set monitor address.

```
          Direct Interrupt Monitor Entry
          push      arg n         arguments in reverse order
          push        .
          push        .
          push        .
          push      arg 1         first argument
          pushf                   push flags onto stack
          calll     monitr,addr   simple call
          add       sp,#2*n       fixup stack from pushes
```

2.3.4 Interrupt Call of a Interrupt Monitor Procedure

Monitor interrupt procedures can be invoked by software interrupts. Note that the Interrupt procedure will execute with interrupts masked unless they are enabled.

```
          Interrupt Monitor Entry
          push      arg n         arguments in reverse order
          push        .
          push        .
          push        .
          push      arg 1         first argument
          Int       numbr         numbr is the Interrupt number
          add       sp,#2*n       fixup stack from pushes
```

2.3.5 Interrupt Service Routine

Interrupt service routines are generally straightforward. Two unusual requirements exist, however:

1. If the routine has a long execution time, It may necessary to enable the interrupts within the routine. Interrupts may be enabled only after the cs register is changed to the monitor segment. This assures that the process will be recognized as In monitor mode If relocation is necesary.

2. I forget the other.

```
          Interrupt Service Routine
          ...code...              misc operations
          jmpl      monitr,xxx    jump to monitor area
xxx:      ...code...              misc operations
          sti                     enable interrupts
addr:     ...code...              normal monitor procedure
          iret                    return from interrupt
```

2.3.6 Interrupt Call of a Normal Monitor Procedure

Interrupts provide the most compact manner of invoking a procedure, but they have the disadvantages of operating under under an interrupt mask, and require an iret return (which is slightly longer than a ret). The following code will allow a software interrupt to execute a normal monitor procedure. Note that the low core interrupt table must point to the address of the appropriate Interrupt Service Routine.

Interrupt Monitor Entry

```
push    arg n       arguments in reverse order
push      .
push      .
push      .
push    arg 1       first argument
int     numbr       numbr is the interrupt number
add     sp,#2*n     fixup stack from pushes
```

Interrupt Service Routine

```
push    bp          save old stack frame
mov     bp,sp       new stack frame
xchg    ax,[bp]     ax onto stack
xchg    ax,[bp+2]   bp onto stack
xchg    ax,[bp+4]   pc onto stack
xchg    ax,[bp+6]   cs onto stack
add     bp,#2       places arguments correctly
pop     ax          restore ax
sti                 won't recognize interrupts
                       until after next instruction
jmpl    monitr,addr jump to normal routine
```

2.4 Traceback Algorithm

If the conventions described above are followed, it is possible to locate the pc addresses of all non-simple stacked procedures. A traceback method is described.

A stacked procedure is defined by two items of information:

1. A pointer to the stack frame. Both a segment register and pointer are required. This pointer will be described as sr:[di] where sr is the segment register and di is the displacement of the stack frame.
2. A flag that is true if the stacked procedure called a monitor procedure with a monitor call and false otherwise.

Traceback starts with the most nested procedure. The procedure is defined by the registers executing in the CPU as follows:

1. ss:[bp]
2. flag := (cs = monitr)

For each procedure, the next procedure is defined as follows:

If monitor mode:

1. ss:[bp]
2. flag := (ss:[bp+4] = monitr)

If user mode:

1. ss:[bp+4]
2. flag := false :=: (ss:[bp+4] = monitr)

When a process is created the bp register is set to zero. Termination of the above algorithm occurrs when the uninitialized bp register is encountered on the stack (i.e. when ss:[bp+2] = 0 the last procedure has been enountered).

[illegible]

DOC. NO. 005-23490-001 REV B

SHEET 1 OF 1

ACCEPTANCE TEST DATA
MODEL 19C- A01 - A

S/N	2194
DATE	5/1/82
BY	A.T

OUTPUT	(1) 5V @ 20A		(2) 12V @ 4A		(3) -12V @ 4A		(4) -5V @ 4A	
OUTPUT TESTS	SPEC	DATA	SPEC	DATA	SPEC	DATA	SPEC	DATA
1. Voltage Setting (VDC)	4.950-5.050	5.004	11.950-12.050	12.004	-11.950 -12.050	-11.995	-4.950 -5.050	-4.996
2. Load Regulation (mV)	20	4	48	9	48	7	20	6
3. Foldback (ADC)	38-40	38.8	5-6	5.2	5-6	5.4	5-6	5.2
4. Line Regulation (mV)	20	3	48	1	48	1	20	1
5. Ripple & Noise (mVpp)	100	100	240	70	240	50	100	40
6. Short Circuit (ADC)	5-10	7.1	1.5A max.	✓	1.5A max.	✓	1.5A max	✓
7. OV (VDC)	5.5-6.5	6.1	13-15	14.6	-13-15	-14.4	-5.5-6.5	-6.2
8.								

FUNCTION TESTS	SPEC	DATA
9. Low Line Inhibit	≤ 80VAC	43
10. Logic Inhibit	≤ 0.8VDC	0
11. Power Fail Signal	88-90VAC	—
12. Hipot Input/Output	4500VDC	✓
13. Hipot Output/Case	900VDC	✓
14. Hipot Input/Case	2700VDC	✓
15. Burn-in	2 Hrs.	✓

TEST CONDITIONS

1. 115 VAC, simultaneous 20% loads.
2. 115 VAC, vary each load 20-100%
3. 115 VAC, increase each load until foldback, with main output at min load
4. 5V @3 0A, others No load, vary line 90-132 VAC.
5. 90 VAC, 5V @ 20A, others @ 100% load one at a time.
6. 90 VAC, apply short to each output.
7. 115VAC apply over-voltage with external 1A supply.
8.
9. 5V @ 30A, lower line until output cuts off.
10. 5V @ 30A & 115 VAC, output to cut off with 0.8 VDC on INHIBIT.
11. 5V @ 30A, lower line until POWER FAIL goes 5 VDC to ≤ 0.4V.
12. Hipot input to output, 1 sec.
13. Hipot output to case, 1sec.
14. Hipot input to case, 1sec.
15. 230 VAC, Burn-in 5V @ 30A with chassis.

[illegible]

Homogeneous Machine
User's Manual

29 January 1982

This is a working document. The information contained herin may increase, or change as the machine is built and used.

The research described in this report was sponsored in part by the Defense Advanced Research Projects Agency, ARPA Order number 3771, and monitored by the Office of Naval Research under contract number N00014-79-C-0597.

1. Structure of the Main Processors

The main processors each consist of a microcomputer system with six interfaces to other processors. The microcomputer consists of an 8086/8087 with the following bus peripherials:

- Address bus: 4k bytes of PROM. This memory is at address ~~$00000-$00FFF~~. FF00 - FFFF

- Address bus: 128k bytes of dynamic RAM. This memory is at address $10000-$1FFFF. 0 - 1FFFF

- IO bus: six interfaces (starting at $0000):

  * IO address $0000: interface 0 (read/write).

  * IO address $0002: interface 1 (read/write).

  * IO address $0004: interface 2 (read/write).

  * IO address $0006: interface 3 (read/write).

  * IO address $0008: interface 4 (read/write).

  * IO address $000A: interface 5 (read/write).

  * IO address $000C: unconnected.

  * IO address $000E: unconnected.

- IO bus: master interrupt controller (starting at $0200):

  * IO Address $0200: command register.

  * IO Address $0202: IRR/ISR, IMR

RB

- IO bus: slave interrupt controller (starting at $0400):

  * IO Address $0400: command register.

  * IO Address $0402. IRR/ISR/IMR

TB

- IO bus: accessory output, address $0600.

- IO bus: accessory input, address $0800.

- IO bus: fifo initialization control address $0A00-$0BFF. Accessing one of these addresses will clear the fifos.

1.1. A Functional Description of the Interfaces

The interfaces communicate messages between processors by means of message queues. An interrupt is generated when a complete message has arrived as input, or an output is capable of accepting an entire message. Since the communication uses queues, there is no possibility of an overrun.

All messages are 64 bits, composed of four 16 bit words. It is the responsibility of the programmer to constrain message lengths to exactly this length.

Each io interface has one IO address and two interrupts associated with it. When an interrupt is active, it is possible to read or write one message from the interface. When a write is performed to the IO address, sixteen bits are written to the output interface. When a read is performed, sixteen bits are read from the input interface.

1.2. Interrupt Organization

The main processor uses two 8259A interrupt controllers organized in the standard master/slave configuration. This configuration allows 15 assigned interrupt channels. These channels are allocated as follows:

- Master $01: receive buffer full, interface 0.

- Master $02: receive buffer full, interface 1.

- Master $04: receive buffer full, interface 2.

- Master $08: receive buffer full, interface 3.

- Master $10: receive buffer full, interface 4.

- Master $20: receive buffer full, interface 5.

- Master $40: unassigned.

- Master $80: slave interrupt controller.

- Slave $01: transmit buffer empty, interface 0.

- Slave $02: transmit buffer empty, interface 1.

- Slave $04: transmit buffer empty, interface 2.

- Slave $08: transmit buffer empty, interface 3.

- Slave $10: transmit buffer empty, interface 4.

- Slave $20: transmit buffer empty, interface 5.

- Slave $40: unassigned.

- Slave $80: NPU exception interrupt.

1.3. Accessories

Each processor has a few accessory functions. There are four bits of input, and six bits of output.

The three input bits are generated by the dedicated host processor and all main processors read the same values.

The five output bits of all main processors are tied together electrically. Any processor with a 1 on the corresponding bit will cause the line to be in a 1 state for the entire array. Useful communications will occur only if processors leave these bits in a 0 state normally.

- Accessory Input (a read from IO address $0600):

  * Bit $0100: external input 0.

  * Bit $0200: external input 1.

  * Bit $0400: external input 2.

  * Bit $0800: state of processor switch (normally 1).

- Accessory Output (a write to IO address $0600):

  * Bit $0100: open collector external output 0.

  * Bit $0200: open collector external output 1.

  * Bit $0400: open collector external output 2.

  * Bit $0800: open collector external output 3.

* Bit $1000: open collecter external output 4.

* Bit $2000: state of processor LED (1 causes light).

1.4. RAM Refresh and NMI Interrupt

The processors employ dynamic RAMS with no hardware for refresh. There is a common NMI condition generated by the dedicated host that will simultaneously interrupt all processors. It is intended that the processing of the NMI include an accesses of 128 contiguous locations in RAM.

	Master $200	Slave $400	Slave 2 $C00
0	pil	tb0e	rb0f
1	pih	tb1e	rb1f
2	nc	tb2e	rb2f
3	nc	tb3e	rb3f
4	nc	tb4e	rb4f
5	npoint	tb5e	rb5f
6	intsa	tb6e	rb6f
7	ints	tb7e	rb7f

CTEST 1

PROM8

Does checksum of its prom (800-FFF) and prints on terminal. Repeats.

Should print 954B

PROMØ

Does checksum of PROMØ (0-800) and prints on terminal. Repeats.

Check with PROM burner for verification.

RAM4

Does ramcheck of ram at 4000-7FFF. Writes incrementing 16 bit patterns and compares back. Starting 16 bit value is printed each iteration.

If fail is found program checks S1 to continue

S1 up ⇒ continue

S1 down ⇒ wait

RAM8

Same as RAM4 but for RAM 8000-BFFF

RAMX

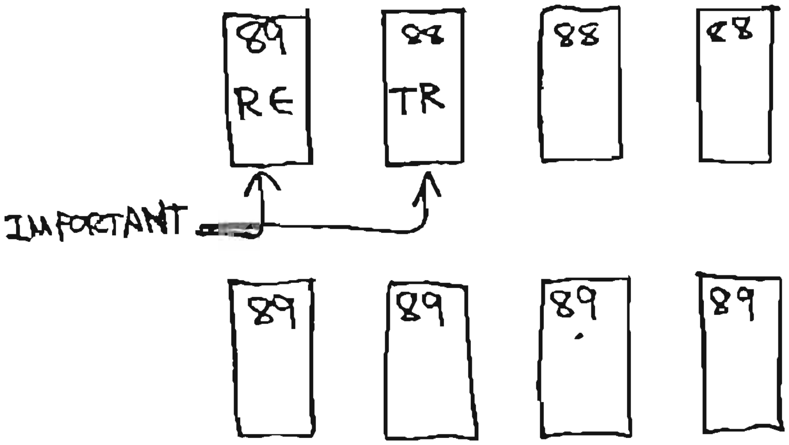
Same as RAM4 but for RAM 4000-8FFF

ECHO

Outputs message. Then inputs from terminal and echos character plus one.

I/O check: SIO/0

Ch A	RxDA	12
	TxDA	15
Ch B	RxDB	28
	TxDB	26



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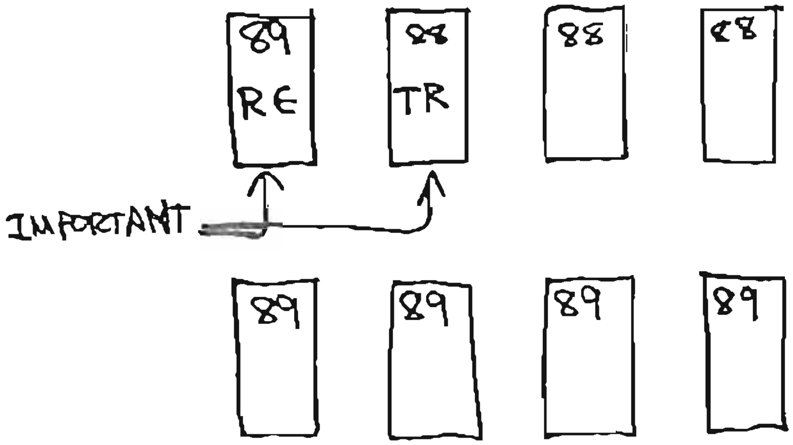
	TxDB	26



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Should print 954B

PROMØ

Does checksum of PROMØ (0-800) and prints on terminal. Repeats.

Check with PROM burner for verification.

RAM4

Does ramcheck of ram at 4000-7FFF. Writes incrementing 16 bit patterns and compares back. Starting 16 bit value is printed each iteration.

If fail is found program checks S1 to continue

S1 up ⇒ continue

S1 down ⇒ wait

RAM8

Same as RAM4 but for RAM 8000-BFFF

RAMX

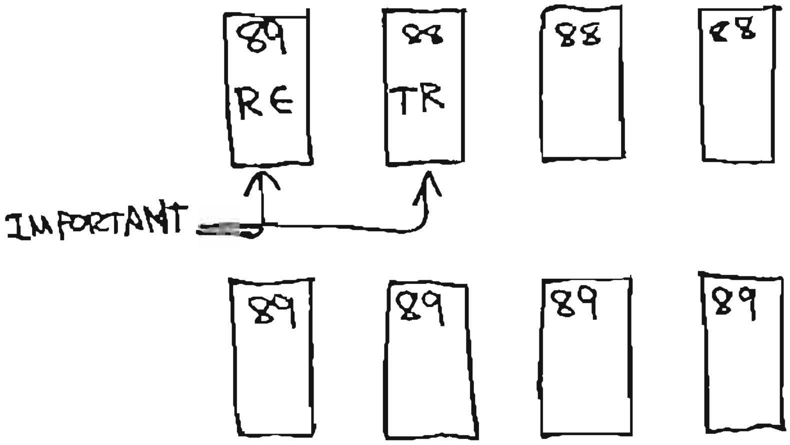
Same as RAM4 but for RAM 4000-8FFF

ECHO

Outputs message. Then inputs from terminal and echos character plus one.

I/O check: SIO/0

Ch A	RxDA	12
	TxDA	15
Ch B	RxDB	28
	TxDB	26



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Does checksum of its prom (800-FFF) and prints on terminal. Repeats.

Should print 954B

PROMØ

Does checksum of PROMØ (0-800) and prints on terminal. Repeats.

Check with PROM burner for verification.

RAM4

Does ramcheck of ram at 4000-7FFF. Writes incrementing 16 bit patterns and compares back. Starting 16 bit value is printed each iteration.

If fail is found program checks S1 to Continue

S1 up ⇒ continue

S1 down ⇒ wait

RAM8

Same as RAM4 but for RAM 8000-BFFF

RAMX

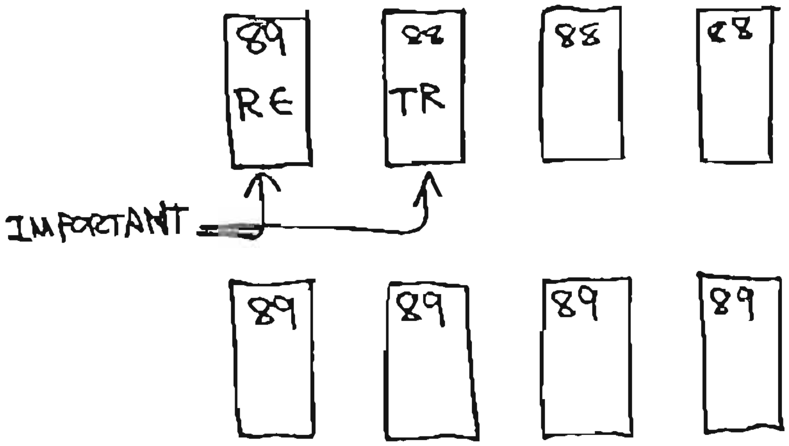
Same as RAM4 but for RAM 4000-BFFF

ECHO

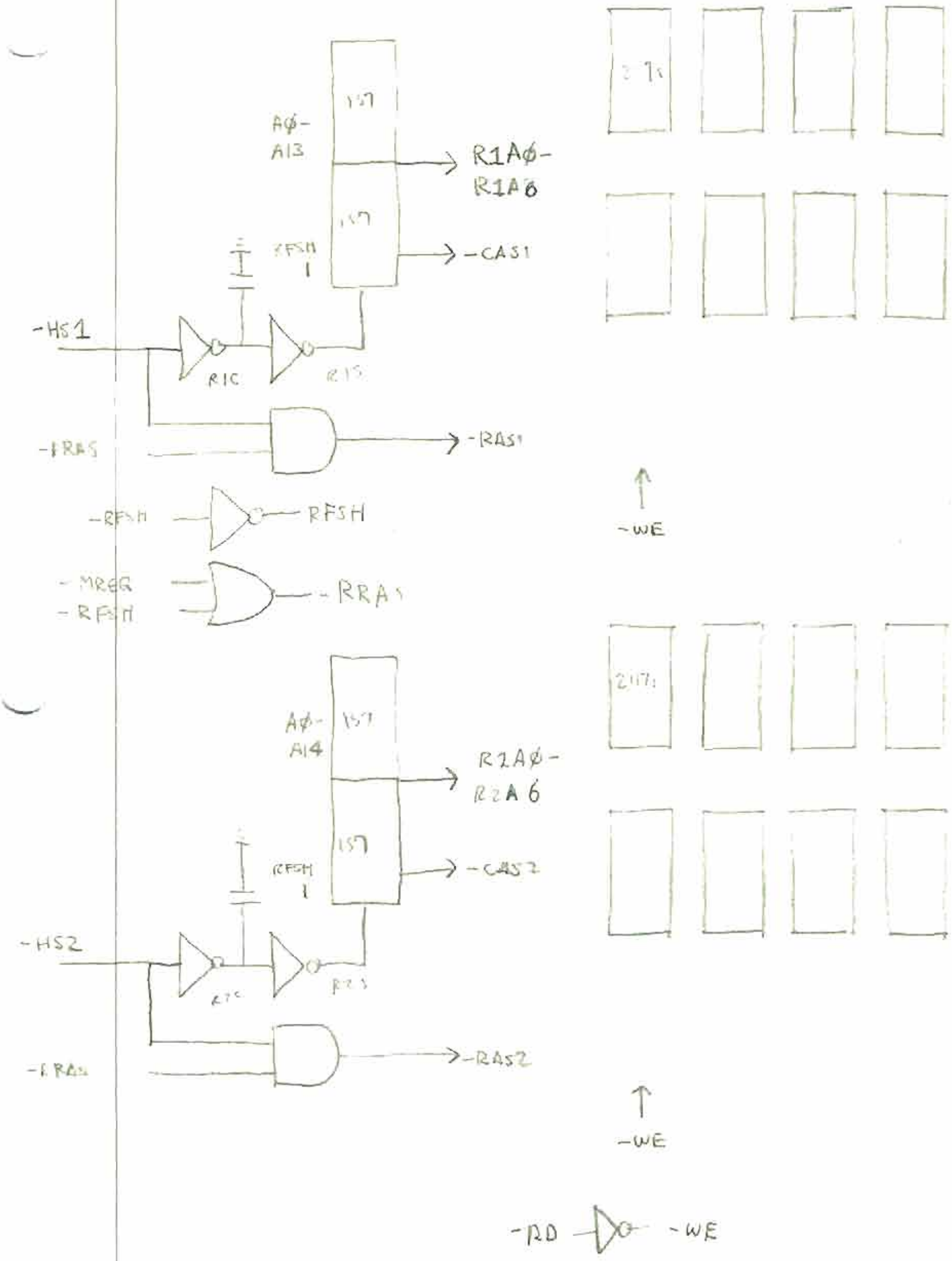
Outputs message. Then inputs from terminal and echos character plus one.

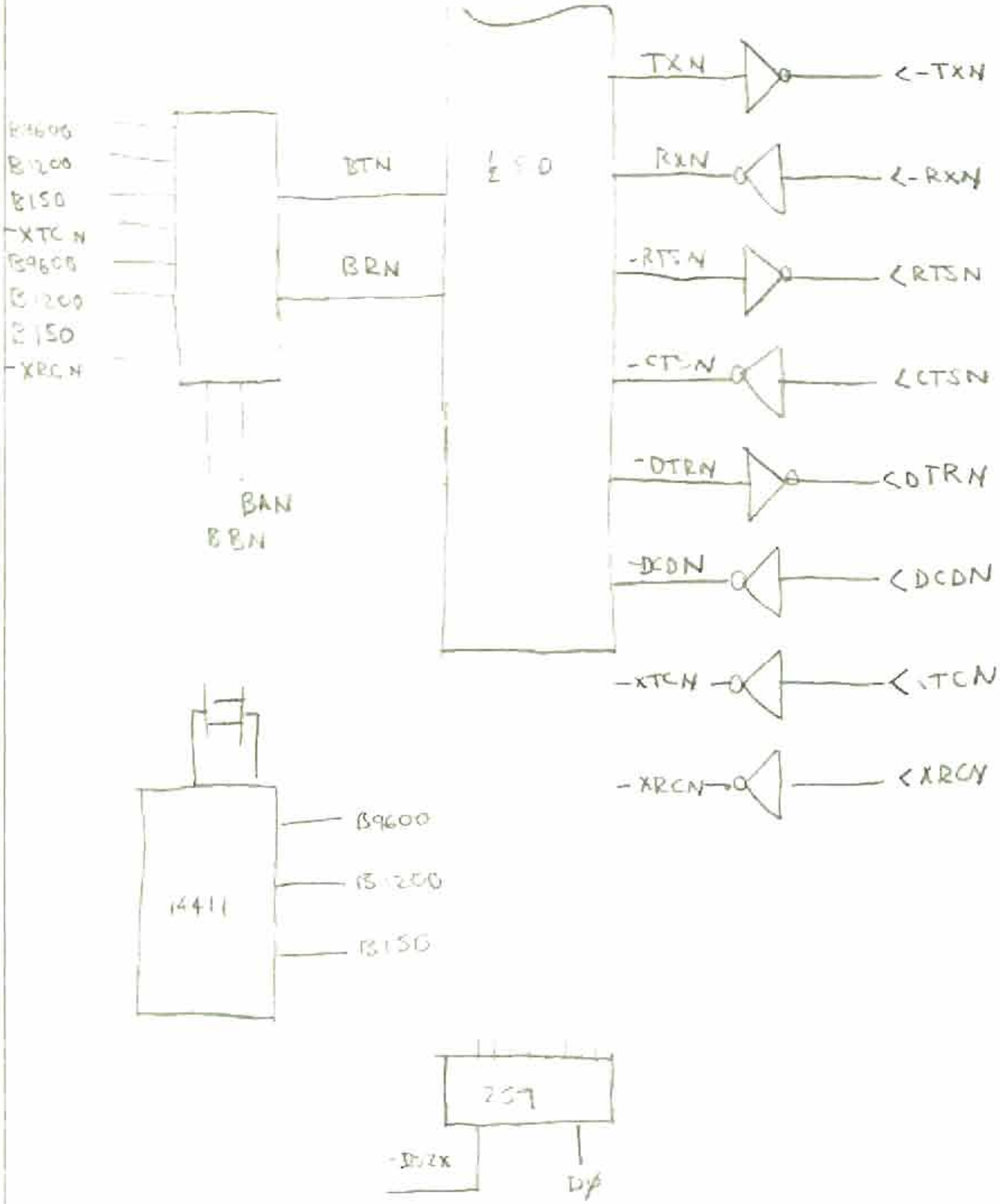
I/O check: SIO/0

Ch A	RxDA	12
	TxDA	15
Ch B	RxDB	28
	TxDB	26

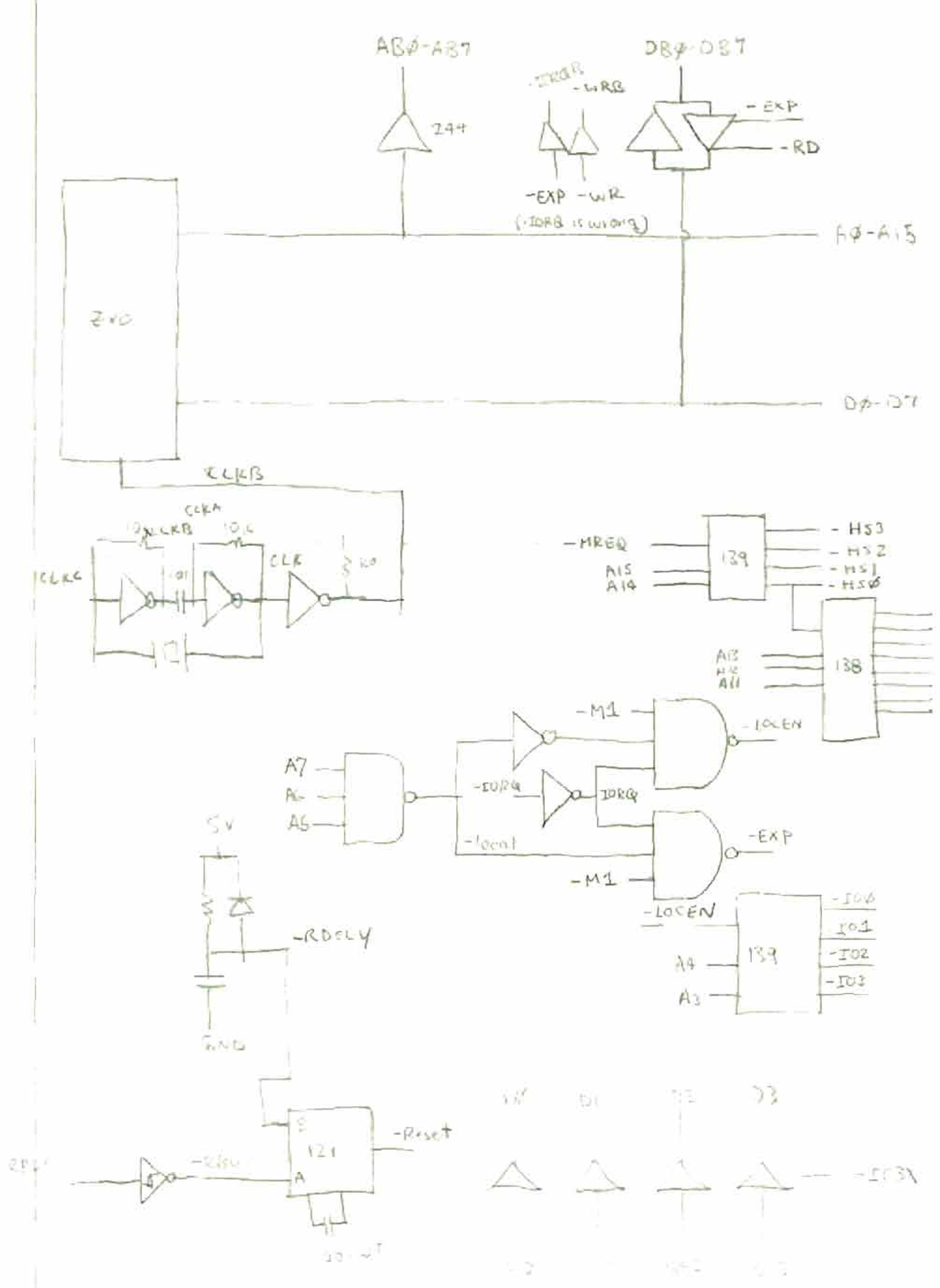


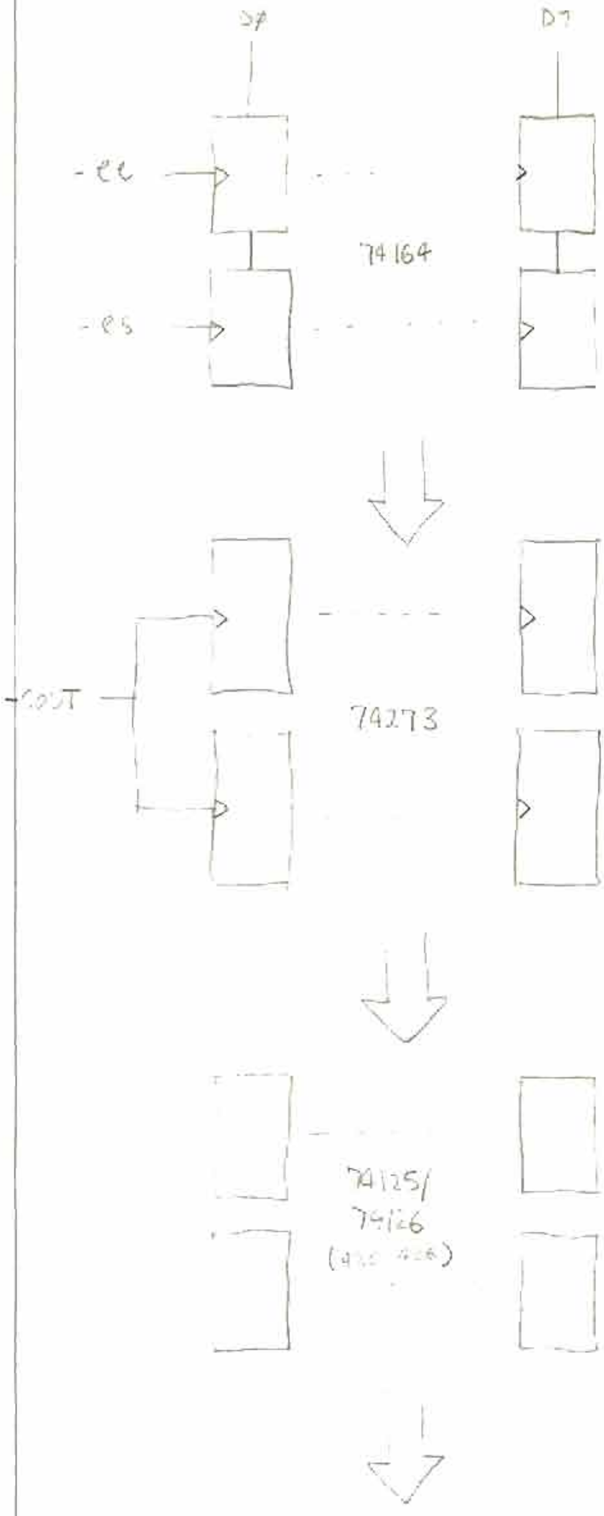
[illegible]

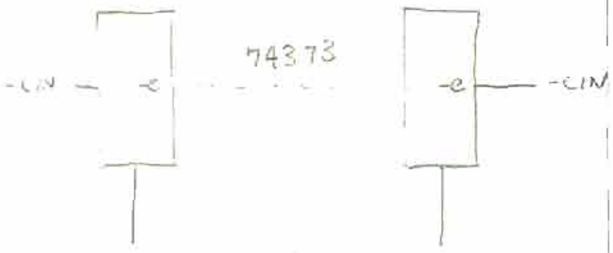

A∅-
A13
157
157
R1A∅-
R1A6
RFSH
1
-CAS1
-HS1
R1C
R1S
-RRAS
-RAS1
-RFSH
RFSH
-MREQ
-RFSH
-RRAS
-WE
2117
A∅-
A14
157
157
R2A∅-
R2A6
RFSH
1
-CAS2
-HS2
R2C
R2S
-RRAS
-RAS2
-WE
-RD
-WE



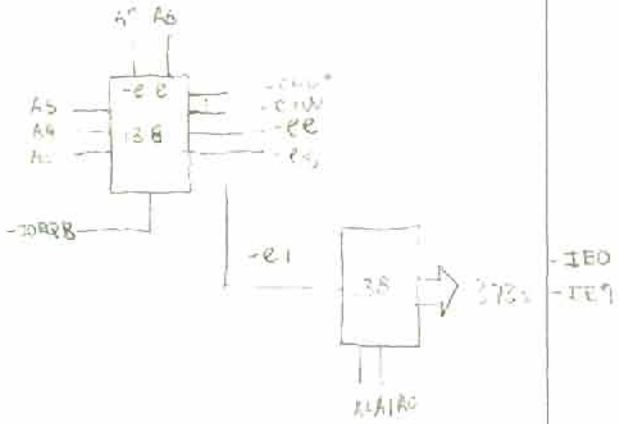
B9600
B1200
B150
-XTC N
B9600
B1200
B150
-XRC N
BTN
BRN
BAN
BBN
1/2 250
TXN
<-TXN
RXN
<-RXN
-RTSN
<RTSN
-CTSN
<CTSN
-DTRN
<DTRN
-DCDN
<DCDN
-XTCN
<\TCN
-XRCN
<XRCN
14411
B9600
B1200
B150
259
-IO2X
DØ


ABØ-AB7
244
-IORQB
-WRB
-EXP -WR
(-IORB is wrong)
DBØ-DB7
-EXP
-RD
AØ-A15
Z80
DØ-D7
CLKB
CCKA
10K CLKB
10K
CLK
CLKC
.01
1K
-MREQ
A15
A14
139
-HS3
-HS2
-HS1
-HSØ
138
A13
A12
A11
-P7
-PØ
-M1
-LOCEN
A7
A6
A5
-IORQ
IORQ
-local
-EXP
-M1
5V
-RDELY
GND
-LOCEN
A4
A3
139
-IOØ
-IO1
-IO2
-IO3
121
-Reset
-RSU
A
DØ
D1
D2
D3
-IO3

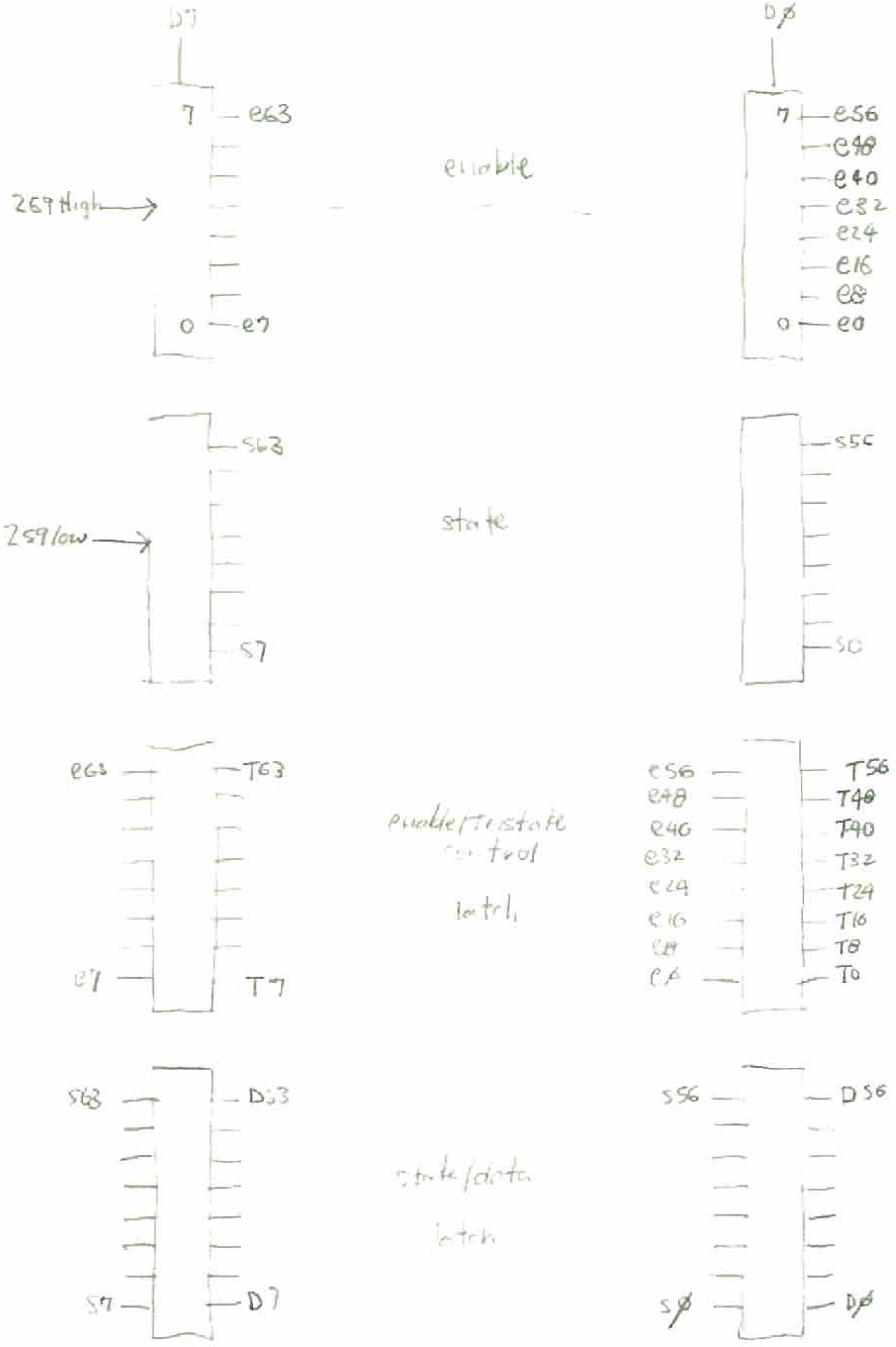


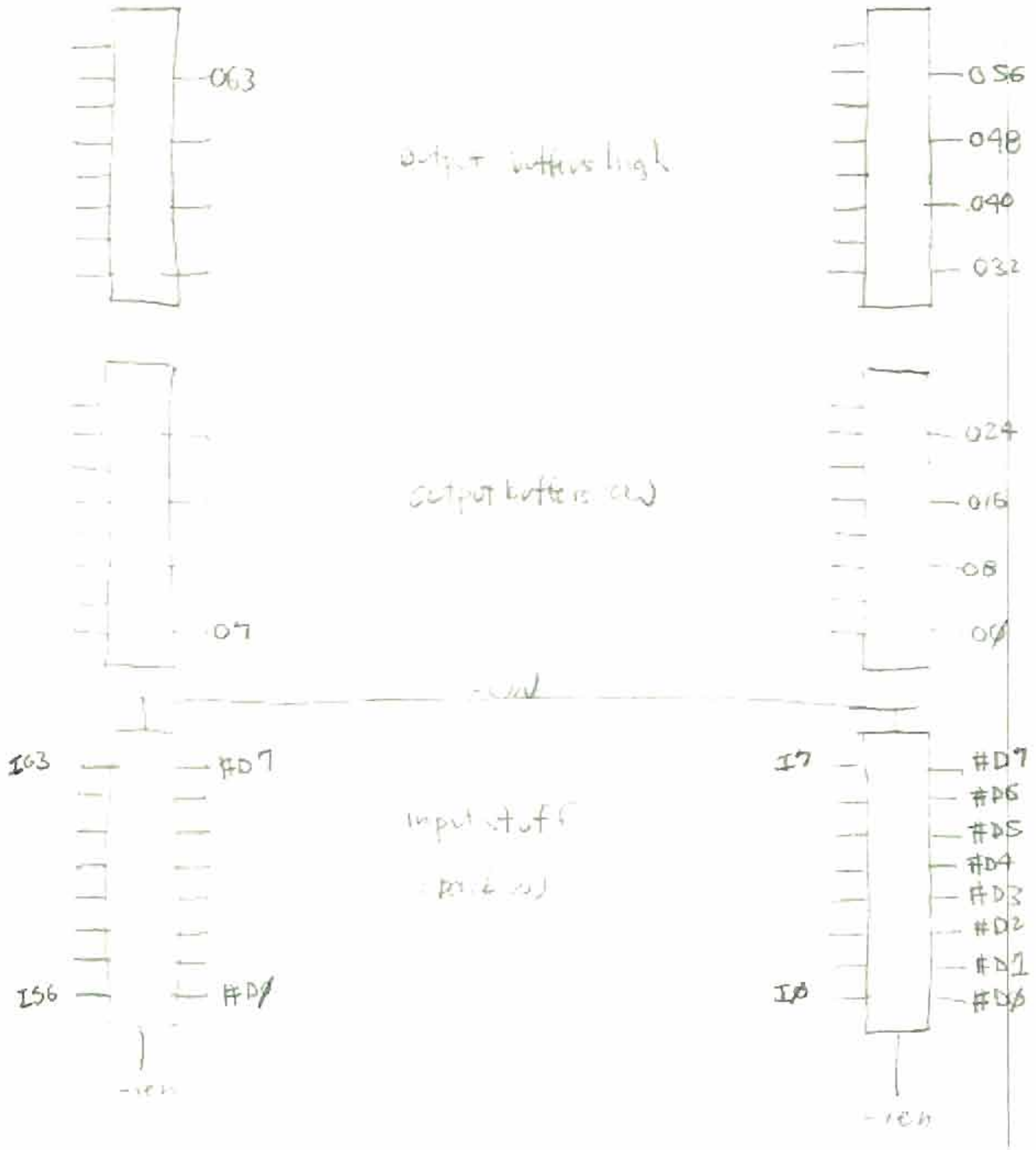


Data Bus



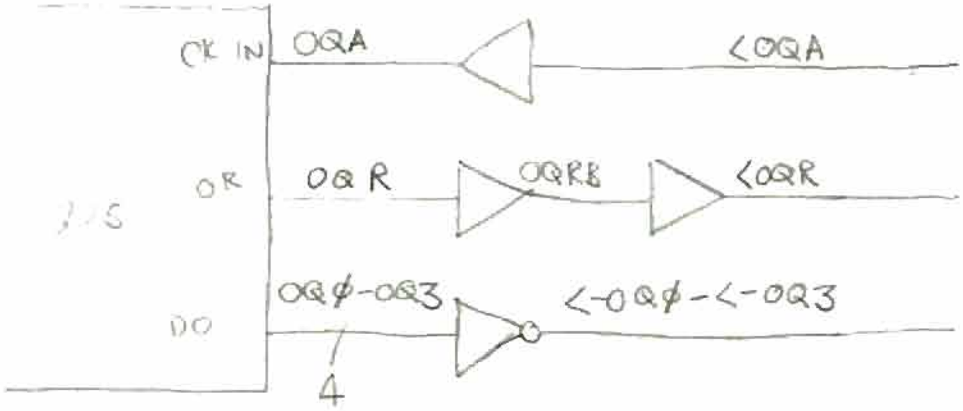
Address

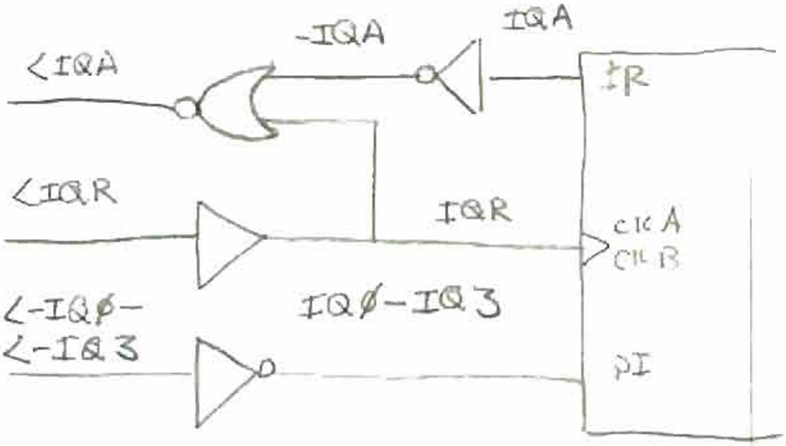

D7
Dø
7
e63
0
e7
7
e56
e48
e40
e32
e24
e16
e8
e0
0
enable
259 High
S63
S7
S56
S0
state
259 low
e63
T63
e7
T7
enable/Tristate
control
latch
e56
e48
e40
e32
e24
e16
e8
e0
T56
T48
T40
T32
T24
T16
T8
T0
S63
D63
S7
D7
state/data
latch
S56
D56
Sø
Dø



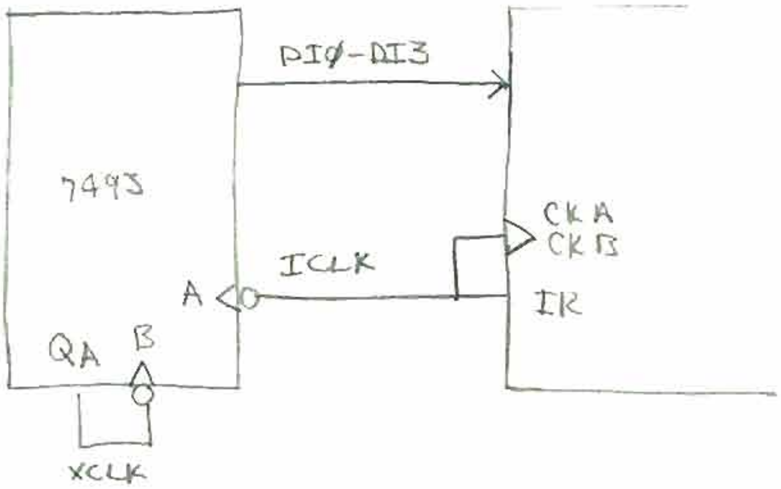
O63
O56
O48
O40
O32
output buffers high
O24
O16
O8
O7
OØ
output buffers low
-wd
I63
#D7
I7
#D7
#D6
#D5
#D4
#D3
#D2
#D1
#DØ
input stuff
(pick up)
I56
#DØ
IØ
-ren
-ren

TEST SETUP

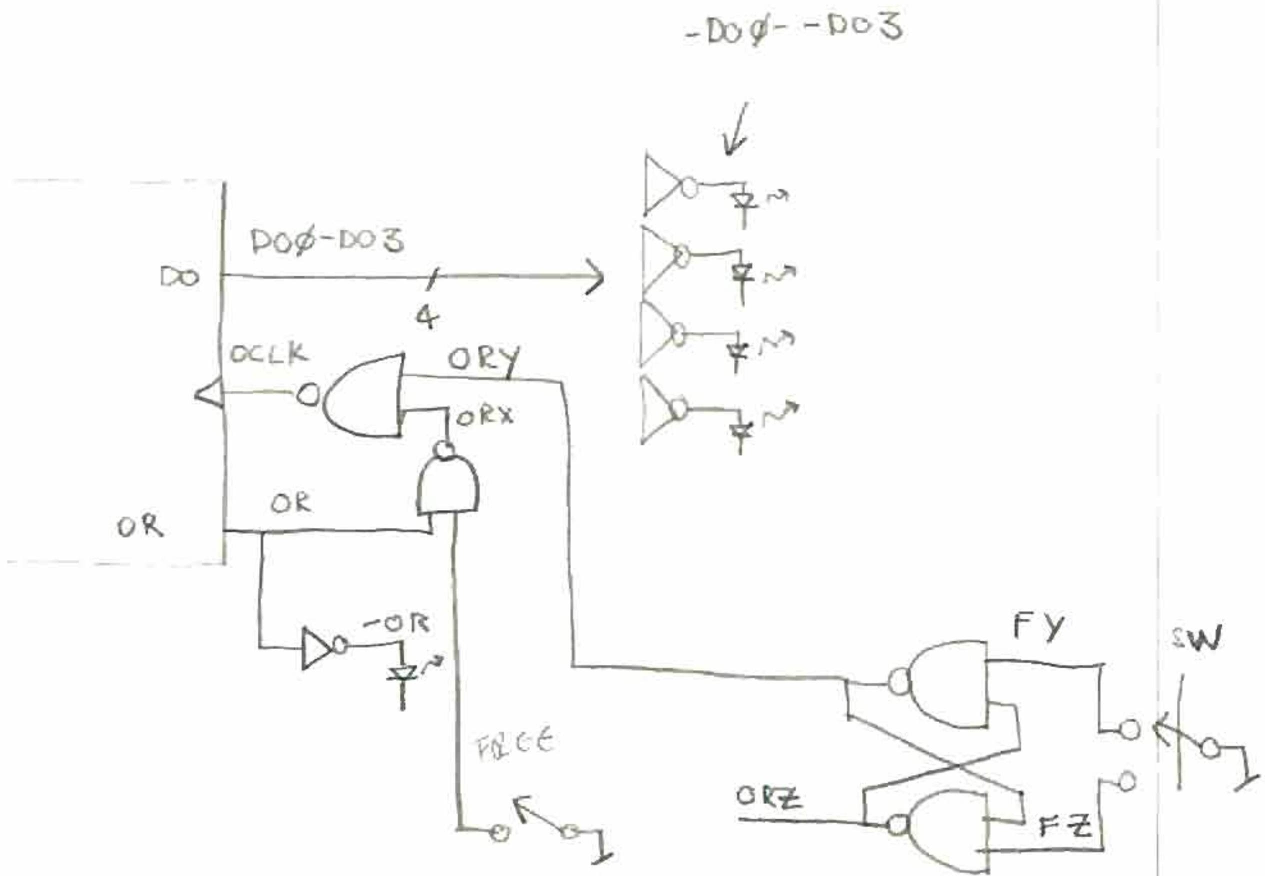

CK IN
OQA
<OQA
OR
OQ R
OQRB
<OQR
I/S
DO
OQϕ-OQ3
<-OQϕ-<-OQ3
4


IQA
-IQA
<IQA
IR
<IQR
IQR
CK A
CK B
<-IQϕ-
<-IQ3
IQϕ-IQ3
DI

INPUT GENERATOR



OUTPUT STUFF



[illegible]

ADDRESS SPACE DECODING

Address line allocations:

```
f
e
d
c
b       these address lines are jumpered to determine at which
a           io space locations this board will respond
9
8
7
6
5       on board io decoding
4
3
2       used by the devices
1
0       not used
```

On board io space decoding:

-IO0	$00	sio 0&1
IO1	$10	sio 2&3
-IO2	$20	baud rate bits

B[illegible] rates:

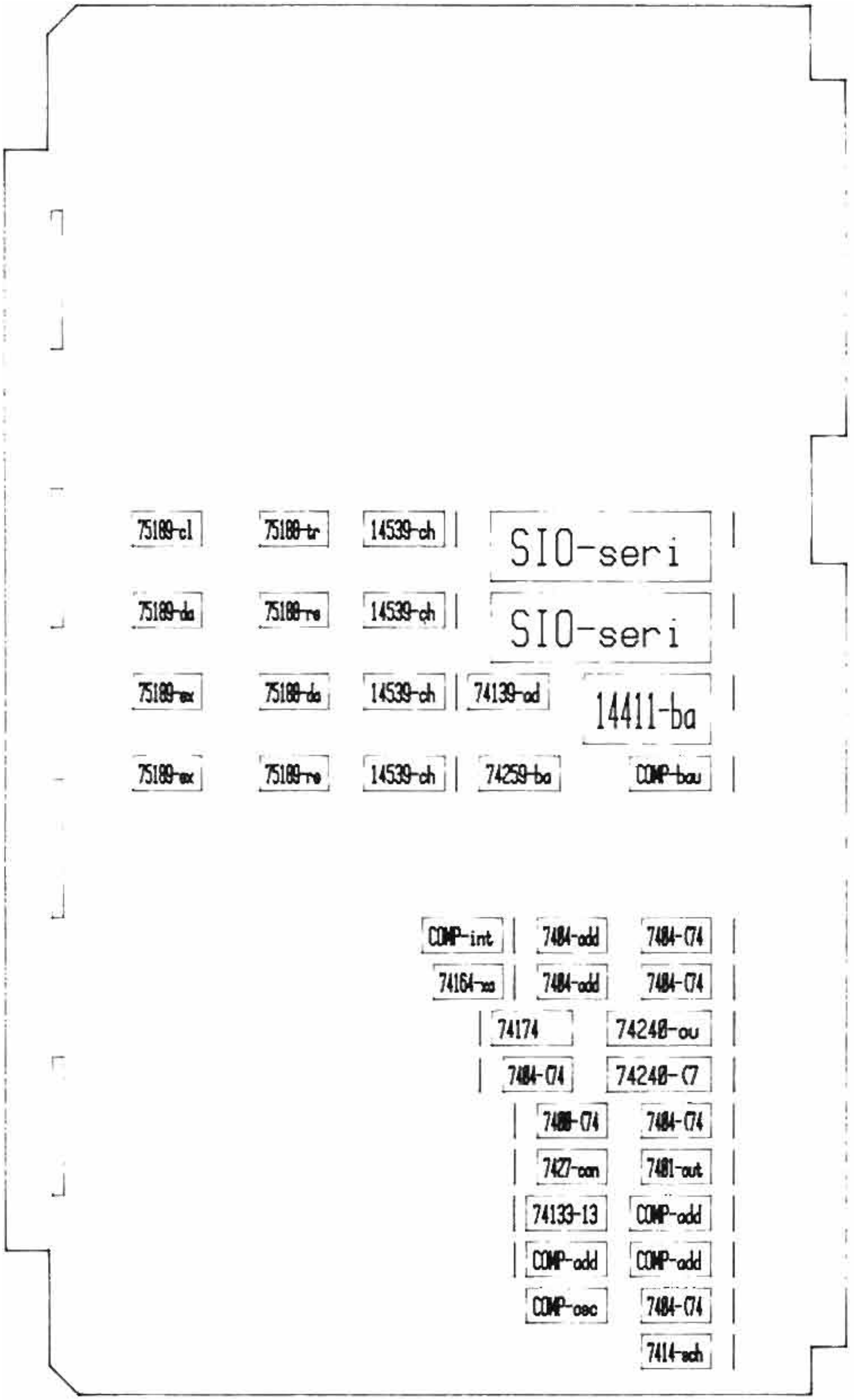
msb	lsb	/64	/32	/16
0	0	150	300	600
0	1	1200	2400	4800
1	0	9600	19K	38K
1	1	ext	ext	ext

Baud rate select addresses:

$20	lsb	ch0
$22	msb	ch0
$24	lsb	ch1
$26	msb	ch1
$28	lsb	ch2
$30	msb	ch2
$32	lsb	ch3
$34	msb	ch3

Control and Data register locations:

$00	data	ch0
$02	control	ch0
$04	data	ch1
$06	control	ch1
$10	data	ch2
$12	control	ch2
$14	data	ch3
$16	control	ch3


75189-cl
75188-tr
14539-ch
SIO-seri
75189-da
75188-re
14539-ch
SIO-seri
75189-ex
75188-da
14539-ch
74139-ad
14411-ba
75189-ex
75189-re
14539-ch
74259-ba
COMP-bau
COMP-int
7404-add
7404-C74
74164-xa
7404-add
7404-C74
74174
74240-ou
7404-C74
74240-C7
7408-C74
7404-C74
7427-con
7401-out
74133-13
COMP-add
COMP-add
COMP-add
COMP-osc
7404-C74
7414-sch

r16p15	1ST 74174
r16p23	BYPASS

Now

r16p15	1ST 74174
r16p24	BYPASS
r16p26	2nd 74174

on r32p03 sio 2-3

pin 35 From -iol to -ioll

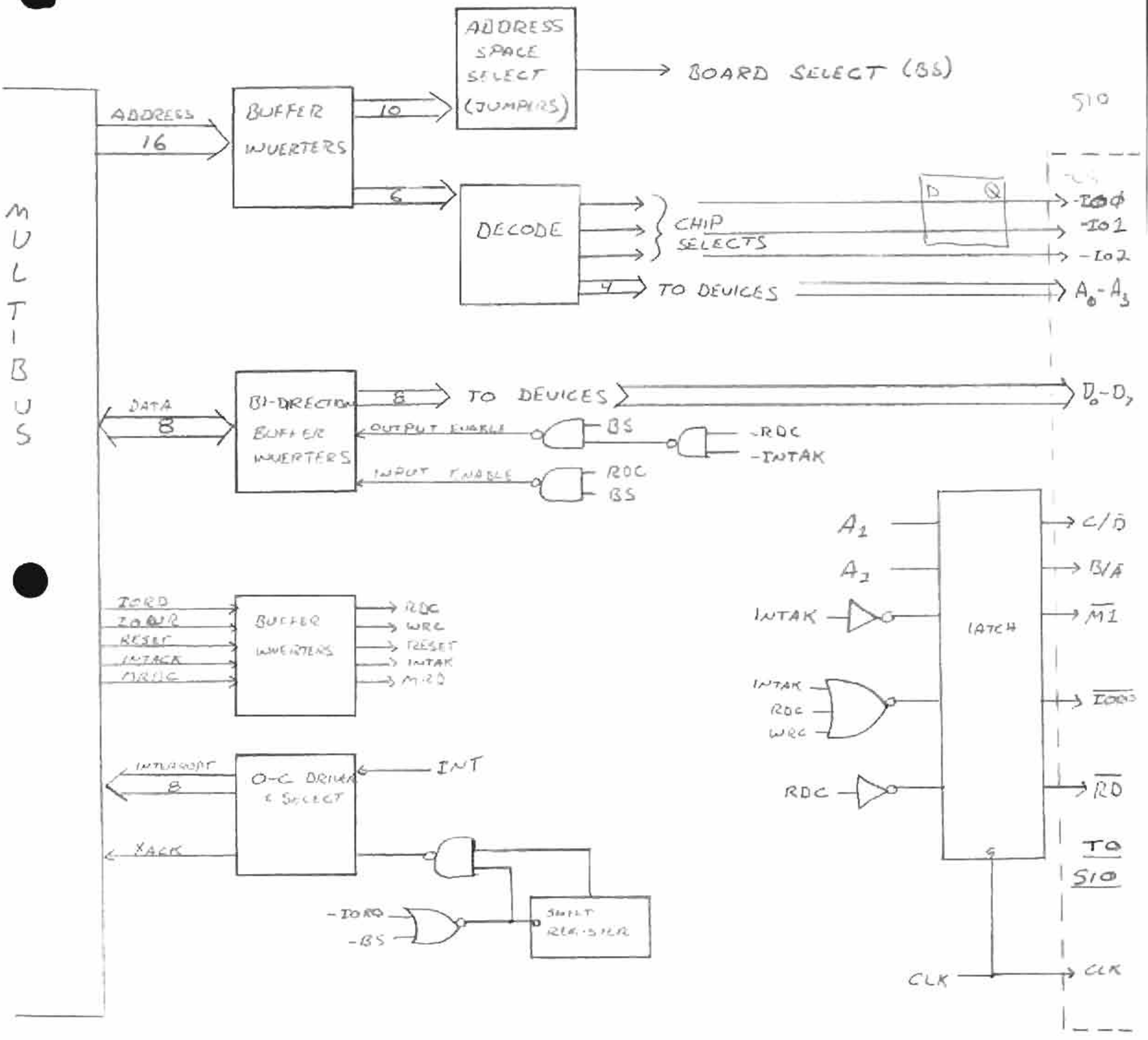
	1st	2nd
1	5V	5V
2	$-mla	$-io01
3	-ml	-io0
4	-iorq	-iol
5	$-iorqa	$-ioll
6	-rdc	nc
7	$-wrcl	$nc
8	gnd	gnd
9	clk	clk
10	$all	$nc
11	al	nc
12	$a2l	$nc
13	a2	nc
14	nc	nc
15	$nc	$nc
16	5V	5V

Broken Wire ROW20 P8

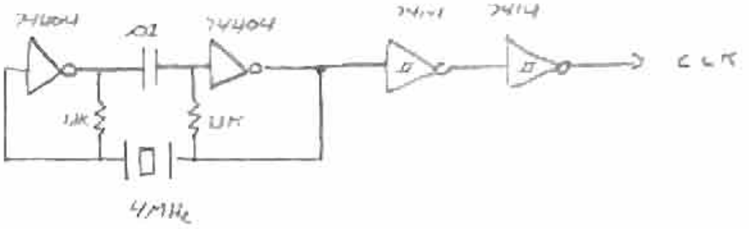
A2

R26 P17

R15 P18

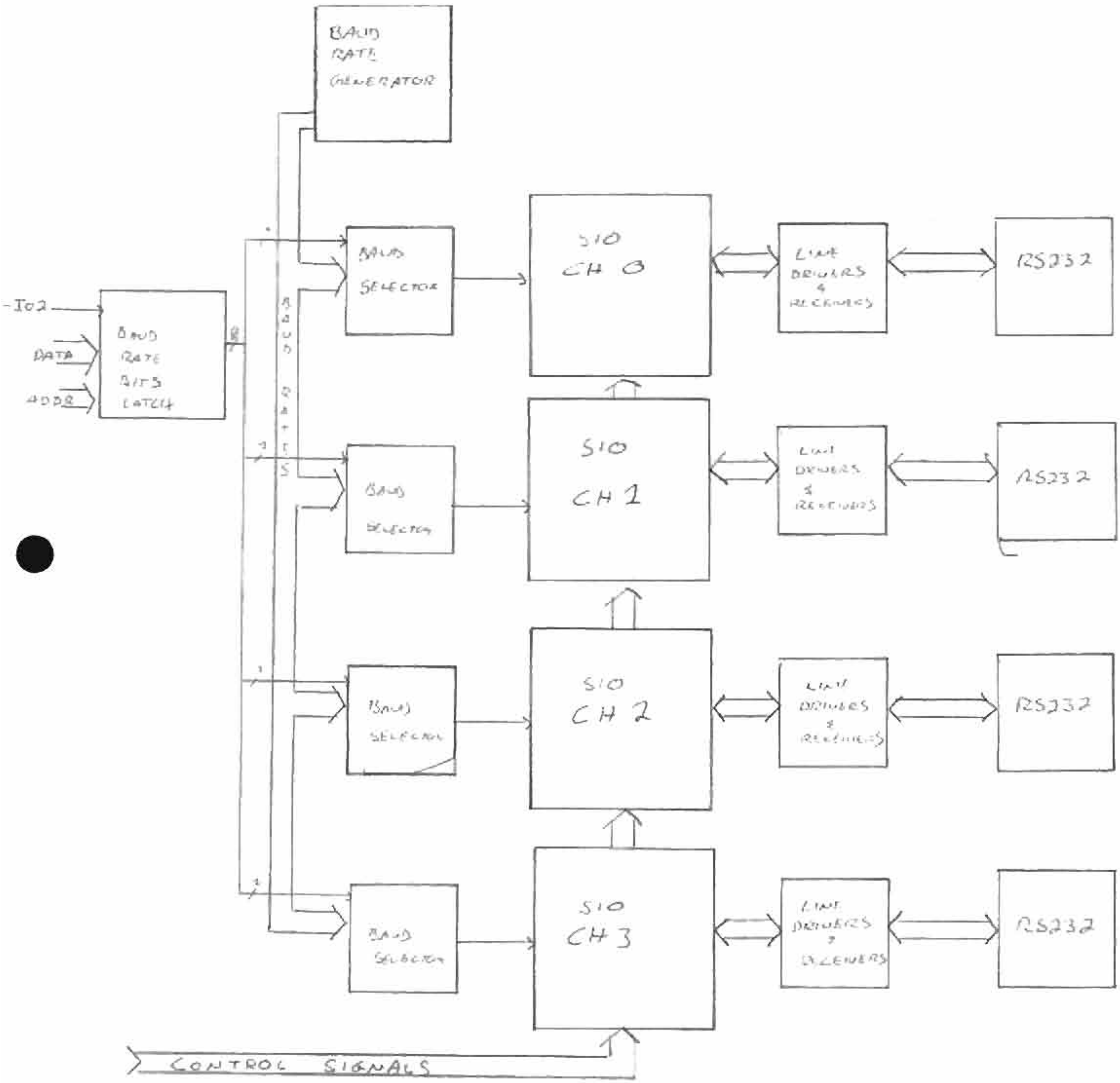


MULTIBUS
ADDRESS
16
BUFFER INVERTERS
10
ADDRESS SPACE SELECT (JUMPERS)
BOARD SELECT (BS)
SIO
6
DECODE
CHIP SELECTS
D
Q
-IO0
-IO1
-IO2
4
TO DEVICES
A_0-A_3
DATA
8
BI-DIRECTION BUFFER INVERTERS
8
TO DEVICES
D_0-D_7
OUTPUT ENABLE
BS
-RDC
-INTAK
INPUT ENABLE
RDC
BS
A_1
A_2
C/D̄
B/Ā
INTAK
$\overline{M1}$
LATCH
INTAK
RDC
WRC
$\overline{IORQ}$
RDC
$\overline{RD}$
IORD
IOWR
RESET
INTACK
MRDC
BUFFER INVERTERS
RDC
WRC
RESET
INTAK
MRD
INTERRUPT
8
O-C DRIVER & SELECT
INT
XACK
-IORQ
-BS
SHIFT REGISTER
TO SIO
CLK
CLK



7404
.01
7404
7414
7414
CLK
1K
1K
4MHz

I/O CIRCUITRY



MAC KCS

micro memory inc

9436 Irondale Ave.
Chatsworth, California 91311-6098
Telephone: (213) 998-0070

February 16, 1982

Thank you for your inquiry regarding our Multibus Compatible Memory Systems. We are happy to enclose the literature you requested. Pricing for the systems is listed below:

		Quantity		
Model No.	Description	1-4	5-9	10-24
MM-8086	32K Bytes Core	$1275.00	$1200.00	$1125.00
MM-8086/16	16K Bytes Core	875.00	835.00	795.00
MM-8080B	8K Bytes Core & EROM	790.00	760.00	730.00
MM-8080/16	16K Bytes Core	849.00	820.00	785.00
MM-8080AL	8K Bytes Core	725.00	700.00	675.00
MM-8086D/512	512K Bytes Dynamic RAM	1425.00	1350.00	1250.00
MM-8086D/256	256K Bytes Dynamic RAM	1050.00	980.00	910.00
MM-8086D/128	128K Bytes Dynamic RAM	575.00	540.00	500.00
MM-8086D/64	64K Bytes Dynamic RAM	425.00	400.00	385.00
MM-8086D/32	32K Bytes Dynamic RAM	400.00	380.00	355.00

The above price includes a Technical Manual. Terms are Net 30 days, f.o.b. Chatsworth, California and includes our 12 month return-to-factory warranty.

All units are temperature cycled and burned in before shipment.

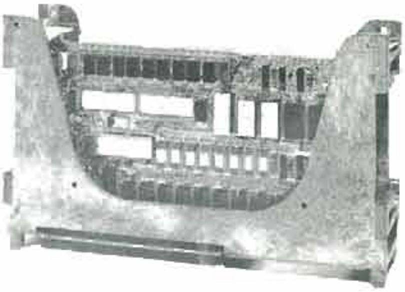
We are anxious to assist you in satisfying your memory requirements. Should you desire additional information or a quotation on larger quantities, please contact us at this office.

Sincerely.

MICRO MEMORY, INC.

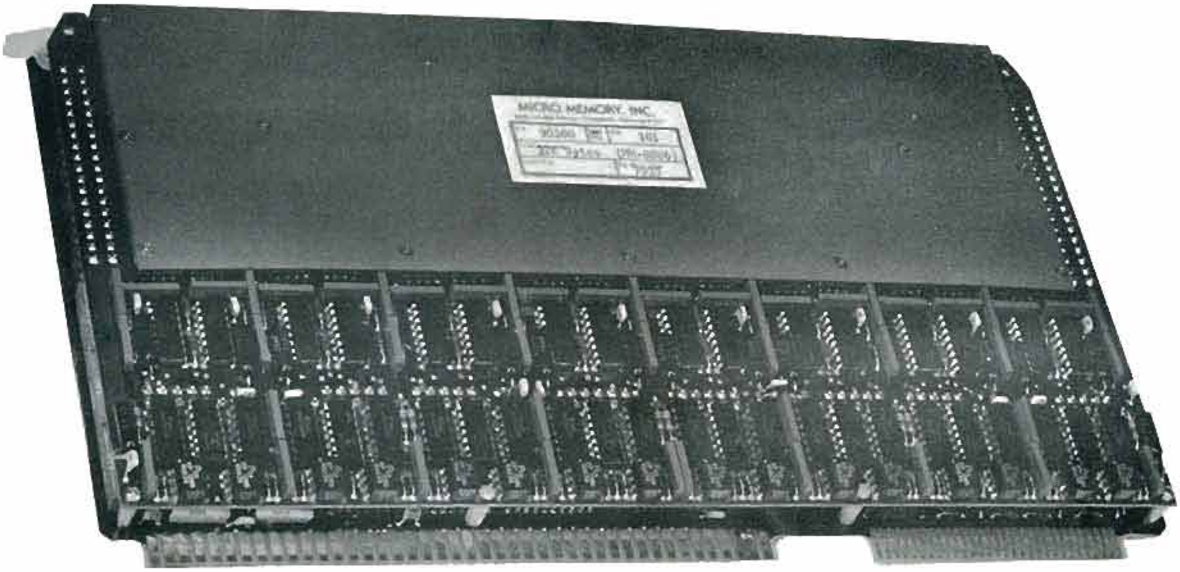
MM-8086
MICROPROCESSOR CORE MEMORY

COMPATIBLE WITH INTEL'S INTELLEC®
iSBC 86/12 AND iSBC 80/05, 10, 20, 30



FEATURES:

- 32K Bytes of Core Read/Write Add-in Memory
- Non-Volatile - Requires No Back-up Battery
- Pin-to-Pin Compatibility with the Multibus®
- Power Monitoring for Data Protection
- Write-Protect Control in 4K Bytes Increments
- Warranty - One Year on Parts and Labor
- Temperature Cycled and Burned-in During Memory Diagnostics



The MM-8086 Microprocessor Core Memory is 32K Bytes non-volatile storage. It was designed as a 16-data bits wide memory, plug compatible with iSBC 86/12 single board computer. The memory can be accessed in both bytes or words, which also makes it compatible with the 8-bit processors.

The memory has internal power monitoring circuits to detect power failure or turn-on/off conditions. These circuits provide memory-lockout for data retention. No power sequencing is required.

The MM-8086 can be switch selectable on any 4K boundries in the one Megabyte address field. The memory contains data/address registers and bidirectional drivers.

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Chatsworth, California 91311
Telephone: (213) 998-0070

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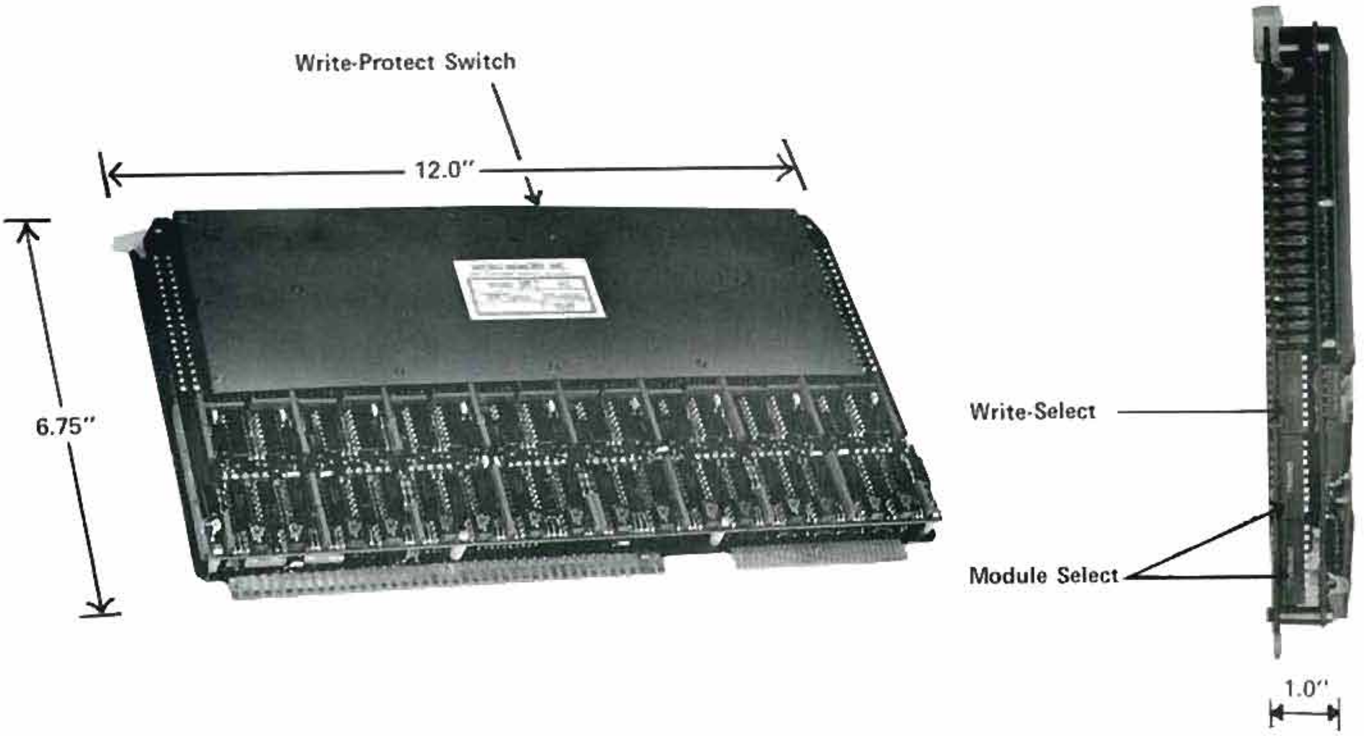
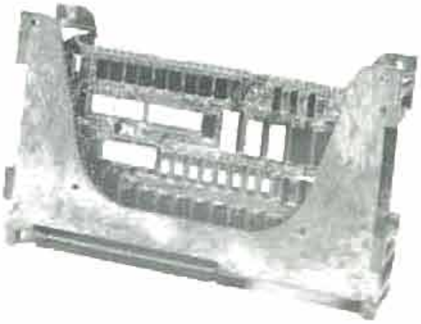


MM-8086 SPECIFICATIONS

CHARACTERISTICS	SPECIFICATIONS
Capacity	32K Bytes organized as 32Kx8 or 16Kx16
Cycle Time	1.2 micro seconds
Access Time	375 nano seconds from MRDC/
Address	20 bits (random access)
Data-in/Data-out	8/16 bits bidirectional with three-state
Modes of Operation	Read, Write and Read Only
Expansion	4K Memory Blocks up to one megabyte
Partitioning	Write-Protect with 4K increments up to 32K bytes
Interface Signals	
Inputs	TTL Compatible
Outputs	Three-state TTL Voltage Compatible
Operating Temperature	0 to 55°C (32° to 131°F)
Storage Temperature	-40 to +80°C
Relative Humidity	To 90% without condensation
Power Requirements	
Operate	+5 @ 3.75A, +12V @ 1.0A
Standby	+5 @ 2.75A, +12V @ 350ma
Data Save Trip-Points	±6% of nominal power supply voltages
Dimensions	6.75" x 12.0" x 1.00"
Connector	Dual 43-Pin on 0.156 in Centers

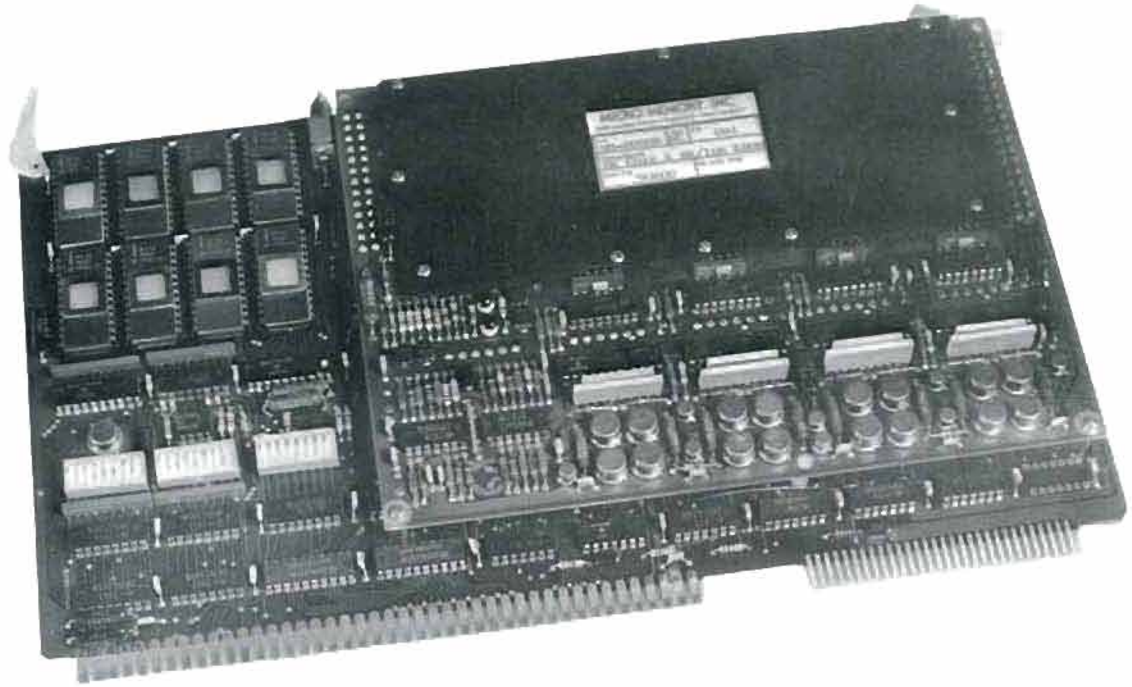
MM-8080B
MICROPROCESSOR EROM/CORE MEMORY

COMPATIBLE WITH INTEL'S INTELLEC MDS 800 AND SBC 80/05, 10, 20, 30



FEATURES:

- 8K/16K Bytes of ROM/PROM and 8K Bytes Core
- Non-Volatile – Requires No Back-up Battery
- Pin-to-Pin Compatibility with the Multibus
- Power Monitoring for Data Protection in Core
- Write-Protect Control in 1K Increments for the Core



The Microprocessor Memory MM-8080B is a non-volatile, 8K/16K Bytes of Read/Only/Memory, using 2708's or 2716's and 8K Bytes of Read/Write Core Memory. It was designed and developed to be plug-compatible with Intel's Multibus, and direct replacement for the SBC-406, 416 and 016. The memory module has internal power monitoring circuits to protect data in core from power failure or during turn on/off conditions. No battery back-up or special circuits are required for power supply sequencing. A power status signal is available as a power interrupt vector or as a power reset signal.

The memory module provides a separate module selection switch for both the 16K Bytes of ROM/PROM and the 8K Bytes of core portion in 4K increments. The memory contains Data/Address registers and bidirectional drivers.

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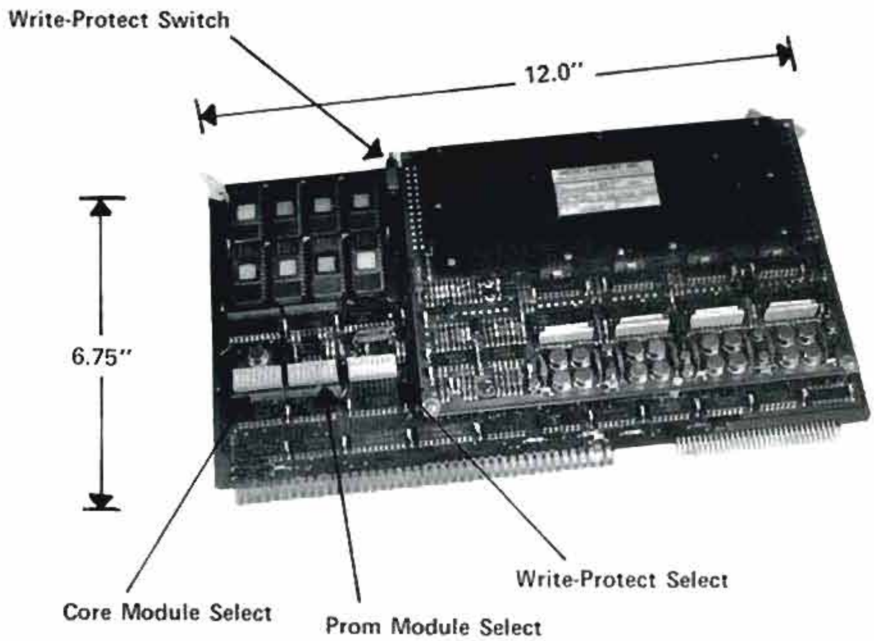
Chatsworth, California 91311
Telephone: (213) 998-0070



MM-8080B SPECIFICATIONS

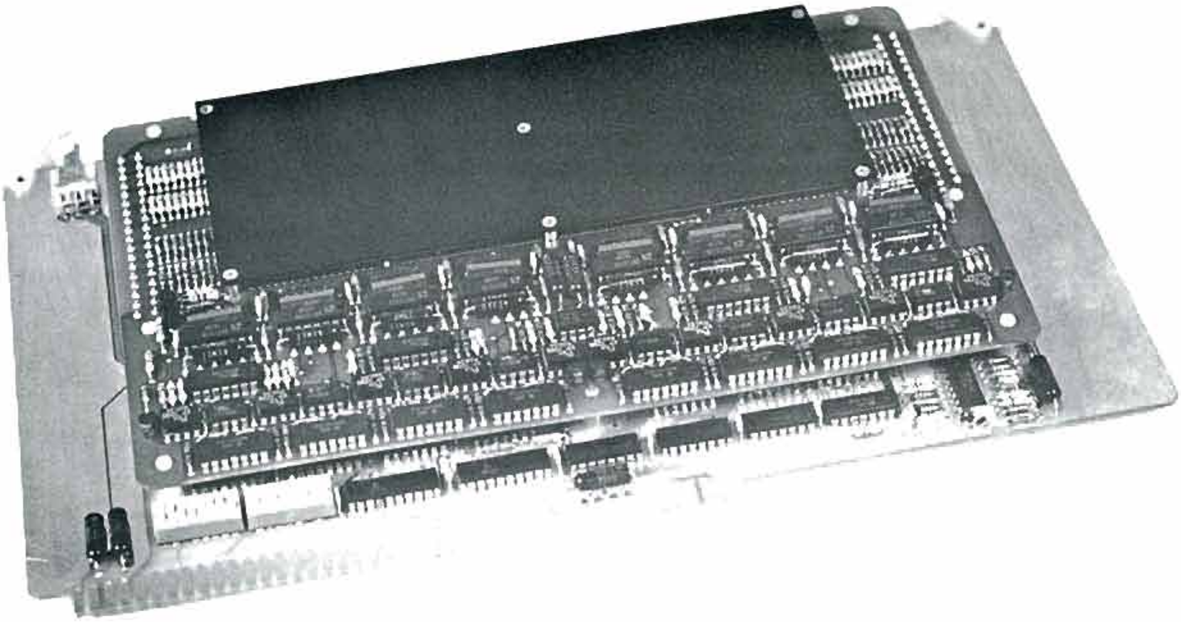
CHARACTERISTICS	SPECIFICATIONS
Capacity	8K/16K Bytes of EROM using 2708/2716 and 8K Bytes of Read/Write Core Memory
Cycle Time	1.0 micro second
Access Time	325 nano seconds from MRDC/
Address	14 Bits (random access)
Data-in/Data-out	8 bits bidirectional with three-state
Modes of Operation	Read Only with 2708/2716, Read/Write with core
Expansion	4K Memory Blocks up to 64K (switch selectable) for each of EROM and core
Partitioning	Write-Protect with 1K Increments up to 8K (switch selectable) for core
Interface Signals	
Inputs	TTL Compatible
Outputs	Three-state TTL Voltage Compatible
Operating Temperature	0 to +55°C
Storage Temperature	-40 to +80°C
Power Requirements including eight 2708/2716	
Operate	+5 @ 2.0A, +12V @ 1.0A, -12V @ 260ma
Standby	+5 @ 1.4A, +12V @ 350ma, -12V @ 260ma
Data Save Trip-Points	±6% of nominal power supply voltages
Dimensions	6.75" x 12.0" x 1.00"
Connector	Dual 43-Pin on 0.156 in Centers

MM-8080/16
MICROPROCESSOR MEMORY

**COMPATIBLE WITH INTEL'S INTELLEC ®
MDS 800 AND SBC 80/05, 10, 20**

Features:

- 16K Words x 8 Bit RAM
- Non-Volatile – Requires No Back-up Battery
- Pin-to-Pin Compatibility
- Power Monitoring for Data Protection
- Write-Protect Control in 2K Increments
- No Wait States or Refresh Delays



The Microprocessor Memory MM-8080/16, is a non-volatile 16,384 word, 8 bit per word RAM core memory. It was designed and developed to enhance or replace the memory in Intel Corporation's Intellec® MDS 800 and SBC 80/05, 10, 20. The memory module has internal power monitoring circuits to protect data from power failure or during turn-on/off conditions. No battery back-up or special circuits are required for power supply sequencing. A power status signal is available as a power interrupt vector or as a power-reset signal for the microprocessor.

The memory module will occupy only one location in the Intel SBC-604/614 module backplane and card cage, when plugged into the fourth slot. The other three slots will be available for the CPU Board and other Modules.

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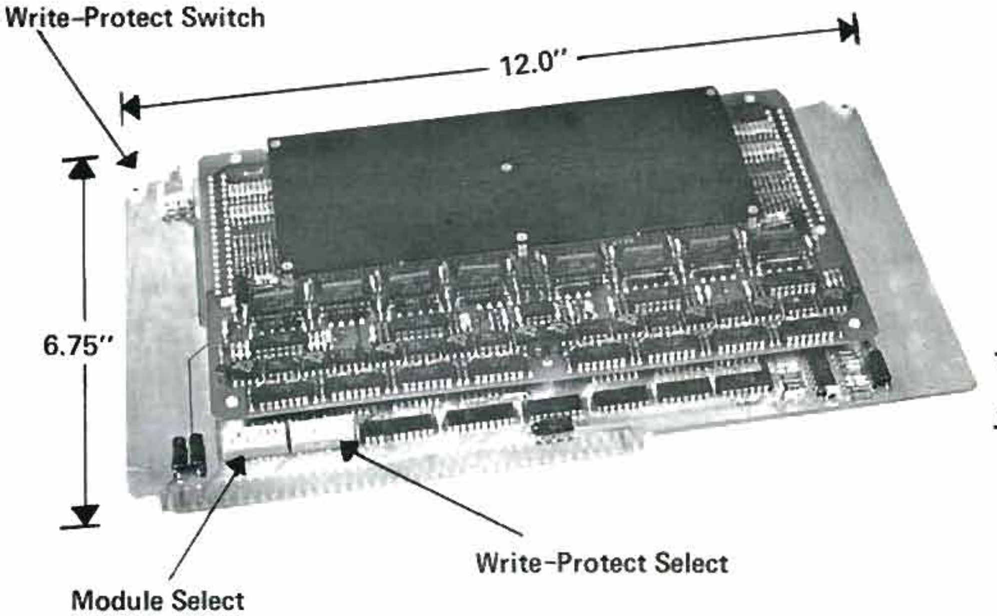
SINGLE SLOT USED
WHEN IN FOURTH POSITION ONLY

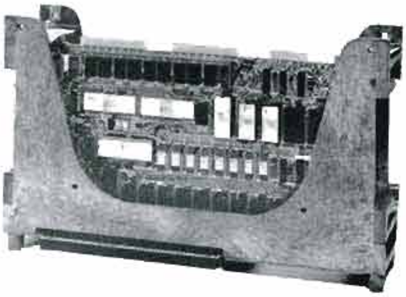


MM-8080/16 SPECIFICATIONS

CHARACTERISTICS	SPECIFICATIONS
Capacity	16,384 Bytes
Cycle Time	1.0 micro second
Access Time	325 nano seconds from MRDC/
Address	14 bits (random access)
Data-in/Data-out	8 bits bidirectional with three-state
Modes of Operation	Clear/Write, Read/Restore
Expansion	4K Memory Blocks up to 64K (switch selectable)
Partitioning	Write-Protect with 2K Increments up to 16K (switch selectable)
Interface Signals	
Inputs	TTL Compatible
Outputs	Three-state TTL Voltage Compatible
Operating Temperature	0 to +60^{o}C
Storage Temperature	-40 to +80^{o}C
Power Requirements	
Operate	+5 @ 2.0A, +12V @ 1.0A
Standby	+5 @ 1.4A, +12V @ 350ma
Data Save Trip-Points	±6% of nominal power supply voltages
Dimensions	6.75" x 12.0" x 0.80"
Connector	Dual 43-Pin on 0.156 in Centers

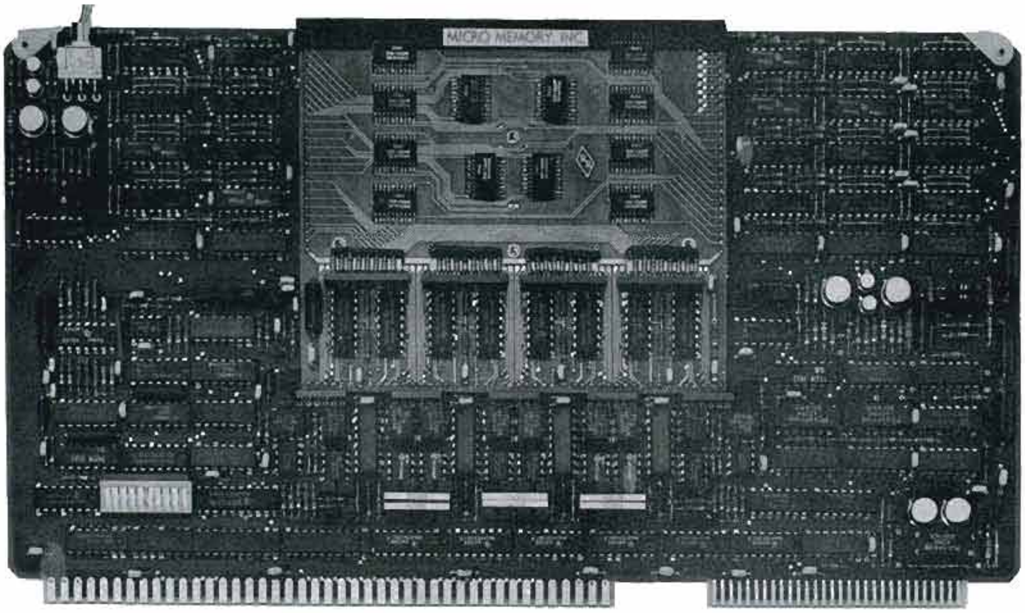
MM-8086/16
MICROPROCESSOR CORE MEMORY

COMPATIBLE WITH INTEL'S INTELLEC®
iSBC 86/12A and iSBC 80/05, 10, 20, 30



FEATURES:

- **Single Card Slot 16K Bytes of Read/Write Memory**
- **Compatible with 8 and 16 Bits Processors**
- **Non-Volatile — Requires no Back-up Battery**
- **AC/DC Power Monitoring for Data Protection**
- **Write-Protect Control in 4K Bytes Increments**
- **Warranty — One Year on Parts and Labor**
- **Temperature Cycled and Burned-in during Memory Diagnostics**



The MM-8086/16K Microprocessor Core Memory is 16K Bytes non-volatile storage, requires no battery back-up. It was designed as a 16-data bits wide memory, plug compatible with iSBC 86/12A single board computer. The memory can be accessed in both bytes or words, which also makes it compatible with the 8-bit processors.

The memory has internal power monitoring circuits to detect DC-power failure or turn-on/off conditions. A Power-Fail Interrupt is generated to the Multibus which works in conjunction with the AC low signal from iSBC 660 power supply. These circuits provide memory-lockout for data retention. No power sequence is required.

The MM-8086/16 can be switch selectable on any 16K boundaries in the one Megabyte address field. The memory contains data/address registers and bidirectional drivers.

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Telephone: (213) 998-0070

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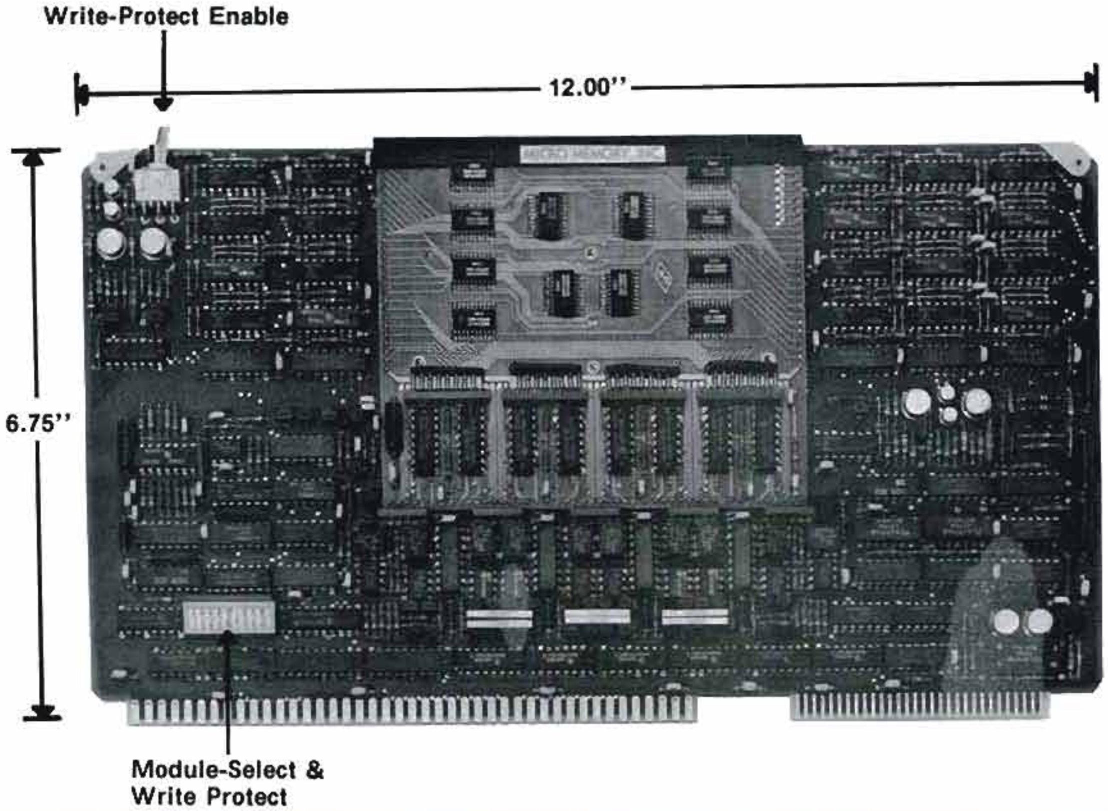


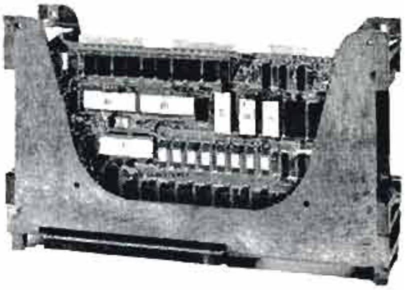
MM-8086/16 SPECIFICATIONS

CHARACTERISTICS	SPECIFICATIONS
Capacity	16K Bytes organized as 16Kx8 or 8Kx16
Cycle Time Read or Write	800 nano seconds
Access Time	280 nano seconds from MRDC/
Address	20 bits (random access)
Data-in/Data-out	8/16 bits bidirectional with three state
Modes of Operation	Read, Write and Read Only
Expansion	16K Memory Blocks up to one megabyte
Partitioning	Write-Protect with 4K increments up to 16K Bytes
Interface Signals	
Inputs	TTL Compatible
Outputs	Three-state TTL Voltage Compatible
Operating Temperature	0° to 60°C [32° to 140°F]
Storage Temperature	-40° to +80°C
Relative Humidity	to 95% without condensation
Power Requirements	
Operate	+5 @ 3.0A, +12V @ 800ma
Standby	+5 @ 2.3A, +12V @ 250ma
Data Save Trip-Points	±6% of nominal power supply voltages
Dimensions	6.75" x 12.0" x .50"
Connector	Dual 43-Pin on 0.156 in Centers

MM-8086D

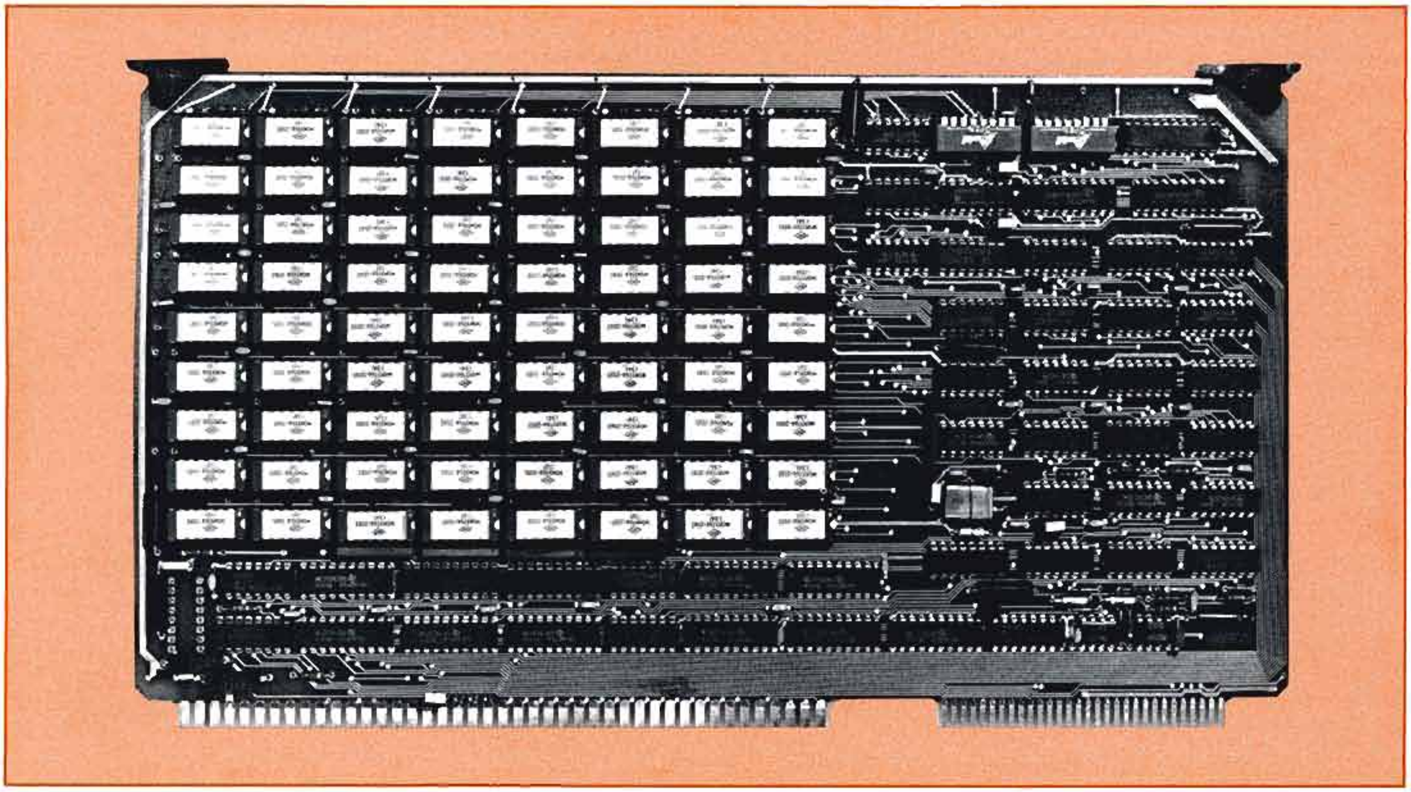
MICROPROCESSOR DYNAMIC RAM MEMORY

Compatible with Intel's Intellec® Series Microcomputer, iSBC 86/12A, and iSBC 80/05, 10, 24, 30



Features:

- 32K to 512K Bytes on a Single Board
- Multibus® Compatible with 8 and 16 bits processors
- Even Parity with output selectable to any of the Bus Interrupts
- Module Select on 4K byte Boundaries in the One Mega bytes address field
- Available in 32KB, 64KB, 96KB, 128KB, 256KB and 512KB configurations
- Warranty - One year on parts and labor
- Temperature cycled and burned-in during memory diagnostics



The MM-8086D Microprocessor memory is a high density memory utilizing 16K or 64K MMOS Dynamic RAMS. It was designed as a 16 bits wide memory module, compatible with iSBC 86/12A single board computer. The memory can be accessed in both bytes and words, which also makes it compatible with 8 bits processors without any hardware changes required.

The memory has a cycle time of 400ns and an access of 250ns. An even parity is provided with an output selectable to any of the interrupts. Module selection is on 4K byte boundaries switch selectable in the one megabytes address field.

Modules with density greater than 128K bytes require only a single +5Volts supply. All modules are temperature cycled between 0°C and 55°C during burn-in while running memory diagnostics for insured reliability.

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Chatsworth, California 91311
Telephone: (213) 998-0070

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MM-8086D SPECIFICATIONS

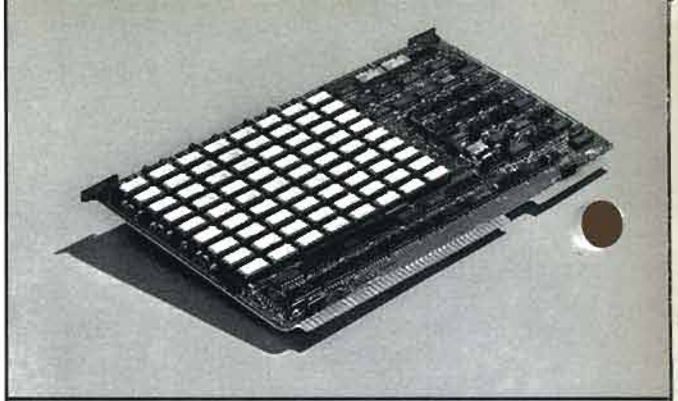
CHARACTERISTICS	SPECIFICATIONS	
Capacity	32K to 512K Bytes	
Cycle Time	400 nanoseconds	
Access Time	250 nanoseconds	
Address	20 bits (random access)	
Data-in/Data-Out	8/16 bits bidirectional with three state output	
Parity	Even parity for each 8 bits with output selectable to any of the interrupts	
Modes of Operations	Read, write	
Refresh	On board one cycle every 15 microseconds	
Expansion	4K memory blocks up to one megabytes	
Interface Signals		
Inputs:	TTL compatible	
Outputs:	Three states TTL Voltage Compatible	
Operating Temp.	0-55°C	
Storage Temp.	-40°C to 80°C	
Relative Humidity	to 95% without condensation	
Power Requirements:	Standby	Operate
+5 Volts:	1.4A	1.4
+12 Volts:	100ma	450ma
Dimensions	6.75" x 12.0"	
Connector	Dual 43-pins on 0.156 in centers.	

Add-In Memories For Microprocessor Systems

Micro Memory Inc.

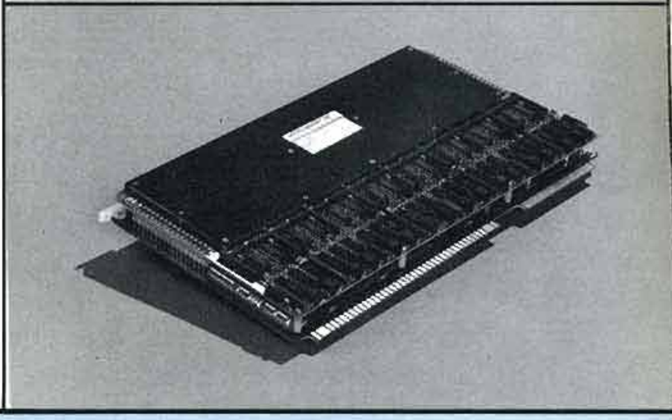
MM-8086D

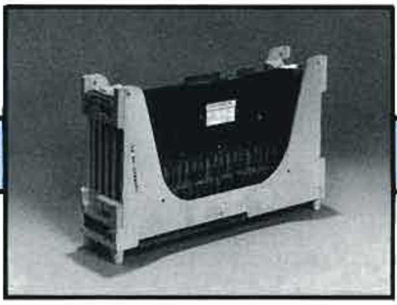
- Dynamic semiconductor RAM
- Capacity: 32K -512K bytes
- Compatible with 8- and 16-bit processors
- Module selection in 4Kbyte boundaries in a 16 Mbyte address field
- Cycle Time: 400 nsec
- Access Time: 250 nsec from MRDC/



MM-8086

- Non-volatile core memory
- Capacity: 32Kbytes
- Compatible with 8- and 16-bit processors
- Module selection in 4Kbyte boundaries in a 1 Mbyte address field
- Write protect control in 4Kbyte increments
- Cycle Time: 1.2 μsec
- Access Time: 375 nsec from MRDC/
- Power monitoring for data protection



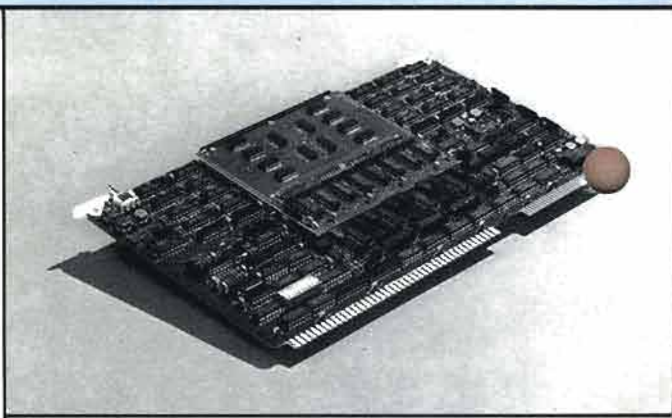


Multibus*-Compatible Memory Boards

*Trademark of Intel Corp.

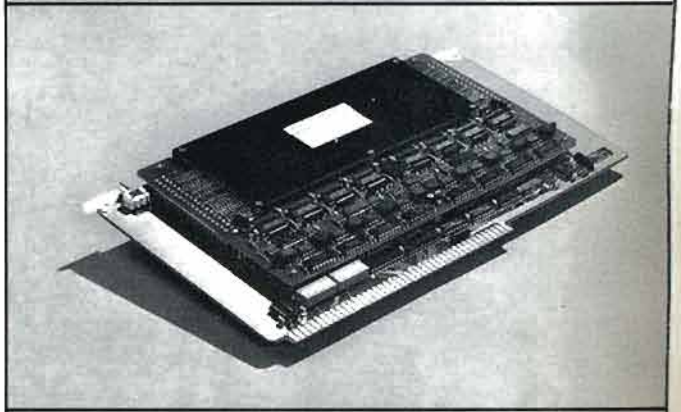
MM-8086/16

- Non-volatile core memory (single card slot)
- Capacity: 16 Kbytes
- Compatible with 8- and 16-bit processors
- Write protect control in 4Kbyte increments
- Cycle Time: 800nsec
- Access Time: 280 nsec from MRDC/
- Power monitoring for data protection



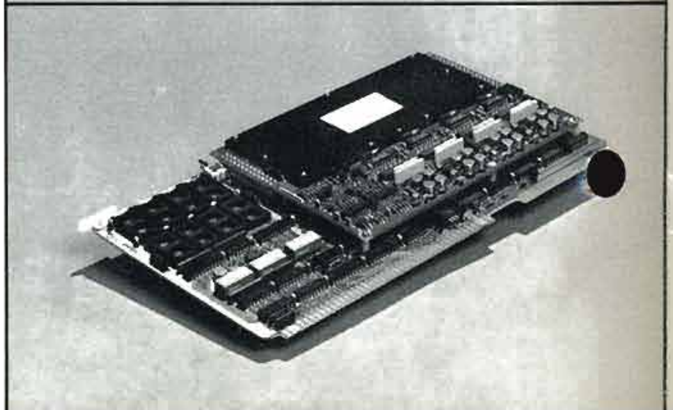
MM-8080/16

- Non-volatile core memory
- Capacity: 16Kbytes
- Module selection in 4Kbyte increments
- Write protect control in 2Kbyte increments
- Cycle Time: 1.0 μsec
- Access Time: 325 nsec from MRDC/
- Power monitoring for data protection



MM-8080B

- Non-volatile core memory and EPROM
- Capacity: 8Kbytes core memory and 8K/16K bytes EPROM
- Write protect control in 1 Kbyte increments for core memory
- Cycle Time: 1.0 μsec (core memory)
- Access Time: 325 nsec from MRDC/
- Power monitoring for data protection in core memory

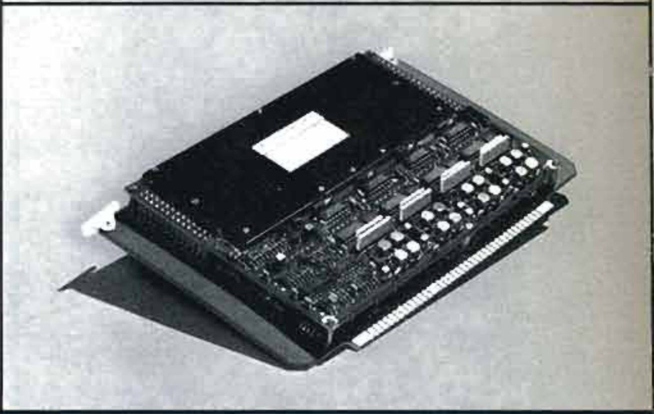


MM-6800/16

- Non-volatile core memory
- Capacity: 16Kbytes
- Operates with 1- or 2-MHz processors
- Module selection in 4Kbyte increments using VUA or VXA
- Write protect control in 2Kbyte increments
- Cycle Time: 1.0 μsec
- Access Time: 350 nsec from Memory Clock
- Power monitoring for data protection

MM-6800

- Non-volatile core memory
- Capacity: 8 Kbytes
- Cycle Time: 1.0 μsec
- Access Time: 350 nsec from Memory Clock
- Power monitoring for data protection

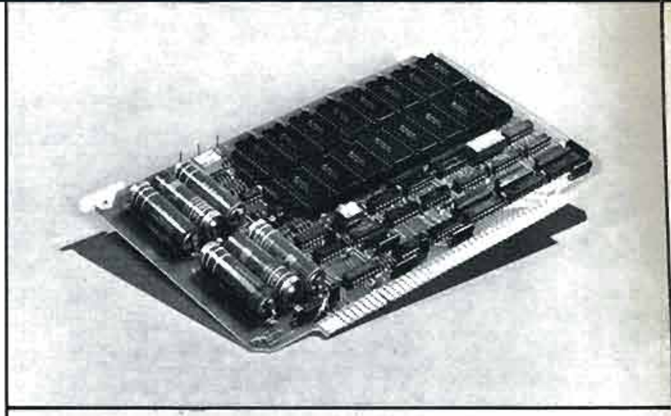


6800 EXORciser*-Compatible Memory Boards

*Trademark of Motorola Inc.

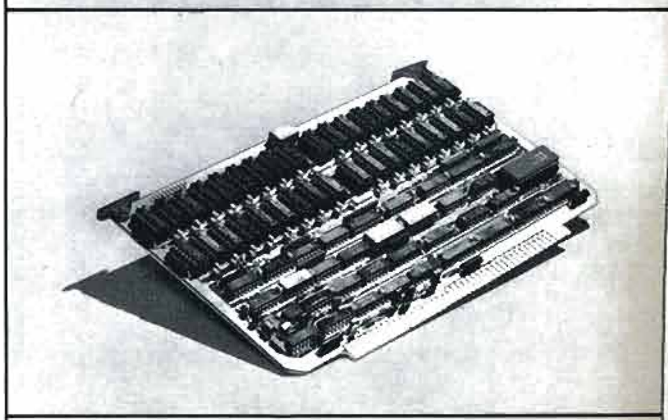
MM-6800C

- Non-volatile CMOS RAM
- Two years data retention with on-board, non-chargeable batteries
- Three months data retention with on-board chargeable batteries
- Module selection in 4Kbyte increments up to 1 Mbyte
- Capacity: 16K - 32K bytes
- Cycle Time: 250 nsec
- Access Time: 200 nsec from Memory Clock
- Power monitoring for data protection



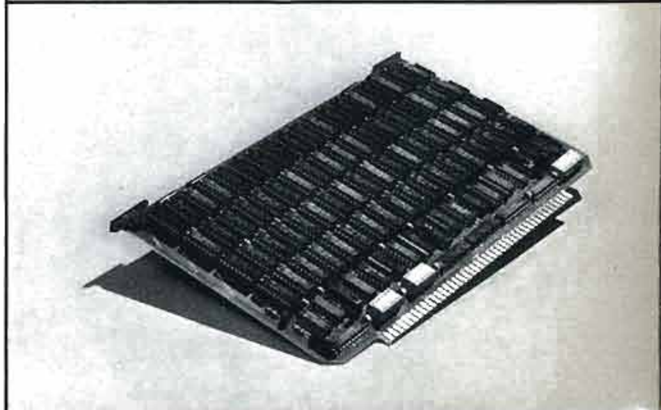
MM-6800D

- Dynamic semiconductor RAM
- Capacity: 16K - 64K bytes
- Module selection in 4Kbyte increments
- Switch-selectable, hidden or cycle-stealing refresh
- Cycle Time: 450 nsec
- Access Time: 220 nsec from Memory Clock
- Even parity with jumper-selectable output to NMI or parity error



MM-6800S

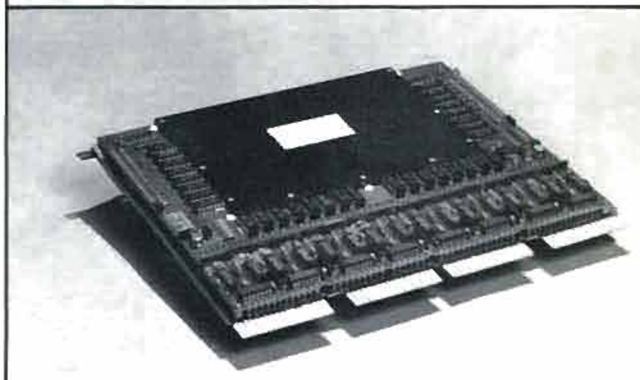
- Static semiconductor RAM
- Capacity: 32Kbytes
- Module selection in 4Kbyte increments
- Software write protect control in 8Kbyte increments
- Cycle Time: 330 nsec
- Access Time: 210 nsec from Memory Clock
- Even parity with jumper-selectable output to NMI, IRQ or parity error

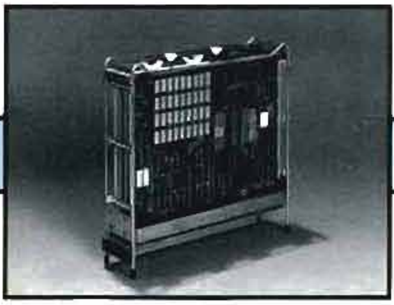


- Dynamic semiconductor RAM
- Capacity: 32K - 256K bytes on dual-wide board
- Module selection in 4Kbyte increments up to 4Mbytes
- Cycle Time: 400 nsec
- Access Time: 275 nsec
- Even parity generation and checking

MM-1103/2

- Non-volatile core memory
- Capacity: 32Kbytes
- Module selection in 4Kbyte increments up to 256Kbytes
- Write protect control in 4Kbyte increments
- Cycle Time: 1.2 μsec
- Access Time: 400 nsec from BSYNCL





DEC LSI-11*Compatible Memory Boards

*Trademark of
Digital Equipment Corp.

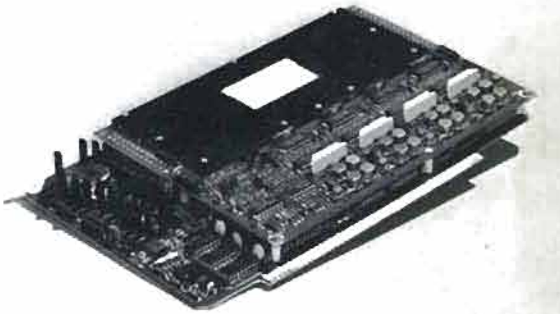
MM-1103

- Non-volatile core memory
- Capacity: 16Kbytes
- Module selection in 4Kbyte increments
- Cycle Time: 1.2 μsec
- Access Time: 400 nsec from BSYNCL

S-100 Bus Compatible Memory Boards

MM-S100

- Non-volatile core memory
- Capacity: 8Kbytes
- Module selection in 8Kbyte increments
- Cycle Time: 1.0 μsec
- Access Time: 350 nsec
- Power monitoring for data protection



micro
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9436 Irondale Ave
Chatsworth, California 91311
Telephone: (213) 998-0070

A Commitment to Reliability

Reliable memory boards are a direct result of Micro Memory Inc.'s years of experience with both core and semiconductor memories. This experience has led to a carefully-controlled reliability plan that covers all phases of design, production, and test.

From the outset, reliability is designed in at the circuit level by using proven, worst-case design techniques. Printed circuit board layout takes into account the design rules required for reliable memory system design, such as minimum power bus noise. High-quality components, from printed circuit board material to semiconductors, are selected to meet stringent MTBF criteria.

Prior to the start of board assembly, incoming parts are inspected to make sure they meet Micro Memory Inc.'s specifications. The boards are monitored by a number of Quality Assurance inspections during assembly.

When assembly is complete, 48 hours of dynamic burn-in and temperature cycling are performed on each board. This involves 90-minute intervals at alternate high and low temperatures, during which the board is exercised by memory diagnostics for worst-case pattern conditions. While the 48-hour test is in progress, a CRT terminal provides a constant record of memory board performance. The test employs the intended processor (Multibus, EXORciser, or LSI-11) in the test fixture, which gives added assurance that each board will operate reliably in its actual environment.

Backing up Micro Memory Inc.'s commitment to reliability is a one-year warranty on parts and labor.

You can count on Micro Memory Inc. for reliable microprocessor memory boards.

Micro Memory Inc.

Founded in 1976, Micro Memory Inc. was the first independent supplier of non-volatile, add-in memory boards for microprocessor systems. Later, the original line of non-volatile memories (employing core) was expanded to include static, dynamic, and CMOS semiconductor RAM.

The add-in memories are direct replacements for their counterparts used in Multibus, 6800-EXORciser, and DEC's LSI-11 microprocessor systems.

The Micro Memory boards merely plug into the backplane of the microprocessor system and use already-existing power and signal buses . . . no system modifications are necessary.

To assist the memory board user, a complete manual of instructions and schematics is provided.

Design, production and testing of the memory boards are accomplished in the Chatsworth, CA headquarters of Micro Memory Inc. Sales are handled direct and through a nationwide network of sales representatives. There is also representation in Canada and Europe.

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OKI semiconductor

APRIL 1981

MSM3764AS 65,536 × 1 BIT DYNAMIC RAM

GENERAL DESCRIPTION

The Oki MSM3764 is a fully decoded, dynamic NMOS random access memory organized as 65536 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

Multiplexed row and column address inputs permit the MSM3764 to be housed in a standard 16 pin DIP. Pin-outs conform to the JEDEC approved pin out.

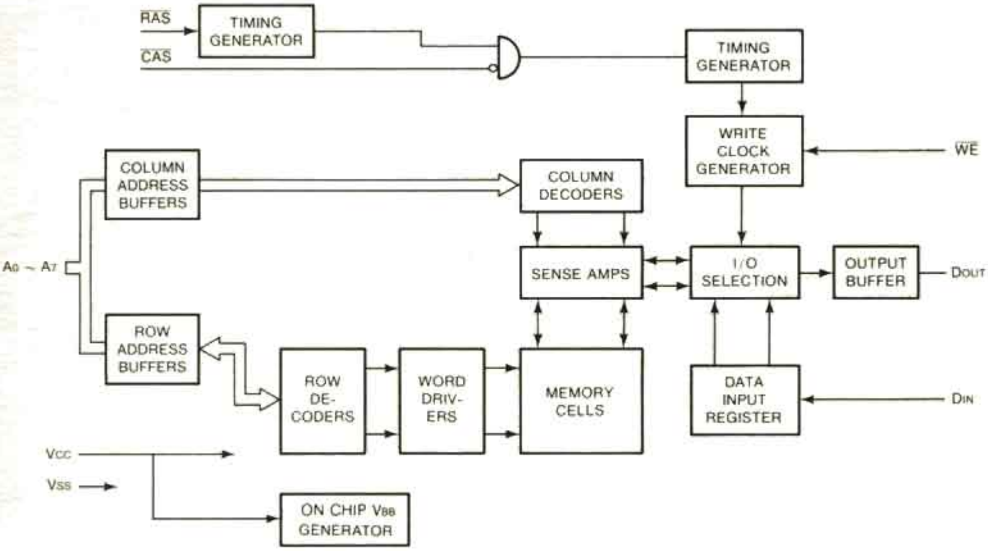
The MSM3764 is fabricated using silicon gate NMOS and Oki's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimum chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and the output are TTL compatible.

FEATURES

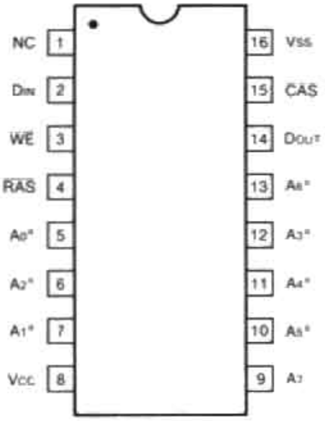
- 65,536 × 1 RAM, 16 pin package
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time,
  120 ns max (MSM3764-12)
  150 ns max (MSM3764-15)
  200 ns max (MSM3764-20)
- Cycle time,
  240 ns min (MSM3764-12)
  270 ns min (MSM3764-15)
  330 ns min (MSM3764-20)
- Low power: 248 mW active,
  28 mW max standby (MSM3764-12)
  23 mW max standby (MSM3764-15/20)
- Single +5V Supply, ±10% tolerance
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- "Gated" $\overline{\text{CAS}}$
- 128 refresh cycles/2ms
- Common I/O capability using "Early Write" operation.
- Output unlatched at cycle and allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, $\overline{\text{RAS}}$-only refresh, and Page-Mode capability
- On-chip latches for Addresses and Data-in
- On-chip substrate bias generator for high performance

FUNCTIONAL BLOCK DIAGRAM



MSM3764AS 65,536 × 1 BIT DYNAMIC RAM

PIN ASSIGNMENT



Pin Names	Function
$A_0 \sim A_7$	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output
V_{CC}	Power (+5V)
V_{SS}	Ground (0V)

*Refresh Address

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operation temperature	T_{OP}	0 to 70	°C
Storage temperature	T_{stg}	−55 to +150	°C
Power dissipation	P_D	1.0	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAPACITANCE

(T_A = 25°C, f = 1 MHZ)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance $A_0 \sim A_7$, D_{IN}	C_{IN1}	4.5	5	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	6	10	pF
Output Capacitance D_{OUT}	C_{OUT}	5	7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating Temperature
Supply Voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V V	0°C to +70°C
Input High Voltage, all inputs	V_{IH}	2.4		V_{CC} + 1.0 V	V	
Input Low Voltage, all inputs	V_{IL}	−1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min.	Max.	Unit	Notes
OPERATING CURRENT* Average power supply current ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycling; t_{RC} = min)	I_{CC1}		45	mA	
STANDBY CURRENT Power supply current ($\overline{\text{RAS}}$ = $\overline{\text{CAS}}$ = V_{IH})	I_{CC2}		5 4	mA	MSM3764-12 MSM3764-15/20
REFRESH CURRENT Average power supply current ($\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ = V_{IH}; t_{RC} = min)	I_{CC3}		35	mA	
PAGE MODE CURRENT* Average power supply current ($\overline{\text{RAS}}$ = V_{IL}, $\overline{\text{CAS}}$ cycling; t_{PC} = min)	I_{CC4}		42	mA	
CAS ONLY CYCLE Power supply current ($\overline{\text{RAS}}$ = V_{IH})	I_{CC}		5 4	mA	−12 Outputs remain H: Z −15/20
INPUT LEAKAGE CURRENT Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)	I_{LI}	−10	10	μA	
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{LO}	−10	10	μA	
OUTPUT LEVELS Output high voltage (I_{OH} = −5mA) Output low voltage (I_{OL} = 4.2mA)	 V_{OH} V_{OL}	 2.4	 0.4	 V V	

Note: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open

AC CHARACTERISTICS

Under Recommended Operating Conditions

Parameter	Symbol	Units	MSM3764-12		MSM3764-15		MSM3764-20		Note
			Min.	Max.	Min.	Max.	Min.	Max.	
Refresh period	t_{REF}	ms		2		2		2	
Random read or write cycle time	t_{RC}	ns	240		270		330		
Read-write cycle time	t_{RWC}	ns	240		270		330		
Page mode cycle time	t_{PC}	ns	150		170		225		
Access time from $\overline{\text{RAS}}$	t_{RAC}	ns		120		150		200	4,6
Access time from $\overline{\text{CAS}}$	t_{CAC}	ns		80		100		135	5,6
Output buffer turn-off delay	t_{OFF}	ns	0	35	0	40	0	50	
Transition time	t_T	ns	3	35	3	35	3	50	
$\overline{\text{RAS}}$ precharge time	t_{RP}	ns	90		100		120		
$\overline{\text{RAS}}$ pulse width	t_{RAS}	ns	120	10,000	150	10,000	200	10,000	
$\overline{\text{RAS}}$ hold time	t_{RSH}	ns	80		100		135		
$\overline{\text{CAS}}$ precharge time	t_{CP}	ns	50		60		80		
$\overline{\text{CAS}}$ pulse width	t_{CAS}	ns	80	10.000	100	10.000	135	10.000	
$\overline{\text{CAS}}$ hold time	t_{CSH}	ns	120		150		200		

AC CHARACTERISTICS con't

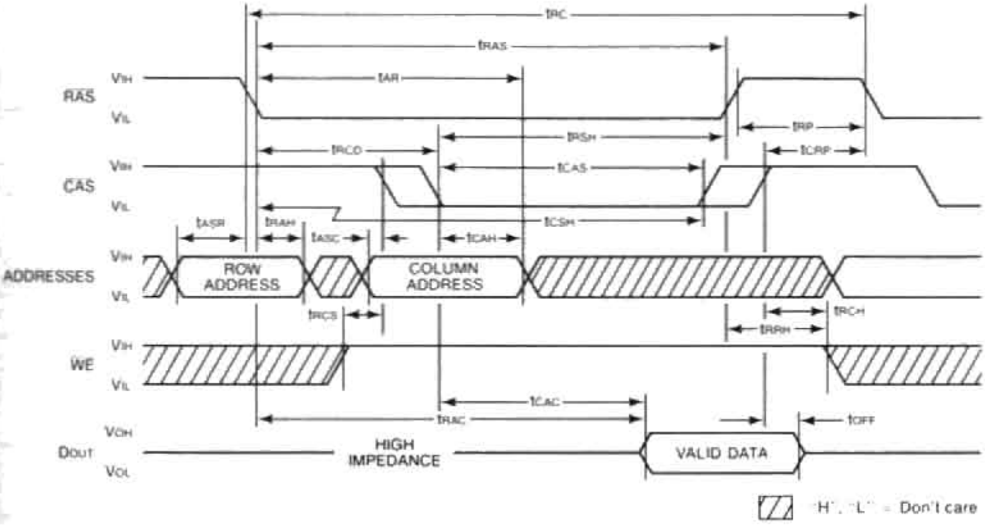
Under Recommended Operating Conditions

Parameter	Symbol	Units	MSM3764-12		MSM3764-15		MSM3764-20		Note
			Min.	Max.	Min.	Max.	Min.	Max.	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t_{RCD}	ns	20	40	20	50	25	65	7
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t_{CRP}	ns	0		0		0		
Row Address set-up time	t_{ASR}	ns	0		0		0		
Row Address hold time	t_{RAH}	ns	20		20		25		
Column Address set-up time	t_{ASC}	ns	0		0		0		
Column Address hold time	t_{CAH}	ns	40		45		55		
Column Address hold time referenced to $\overline{\text{RAS}}$	t_{AR}	ns	80		95		120		
Read command set-up time	t_{RCS}	ns	0		0		0		
Read command hold time	t_{RCH}	ns	0		0		0		
Write command set-up time	t_{WCS}	ns	−10		−10		−10		8
Write command hold time	t_{WCH}	ns	40		45		55		
Write command hold time referenced to $\overline{\text{RAS}}$	t_{WCR}	ns	80		95		120		
Write command pulse width	t_{WP}	ns	40		45		55		
Write command to $\overline{\text{RAS}}$ lead time	t_{RWL}	ns	40		45		55		
Write command to $\overline{\text{CAS}}$ lead time	t_{CWL}	ns	40		45		55		
Data-in set-up time	t_{DS}	ns	0		0		0		
Data-in hold time	t_{DH}	ns	40		45		55		
Data-in hold time referenced to $\overline{\text{RAS}}$	t_{DHR}	ns	80		95		120		
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay	t_{CWD}	ns	50		60		80		8
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay	t_{RWD}	ns	90		110		145		8
Read command hold time reference to $\overline{\text{RAS}}$	t_{RRH}	ns	20		20		25		

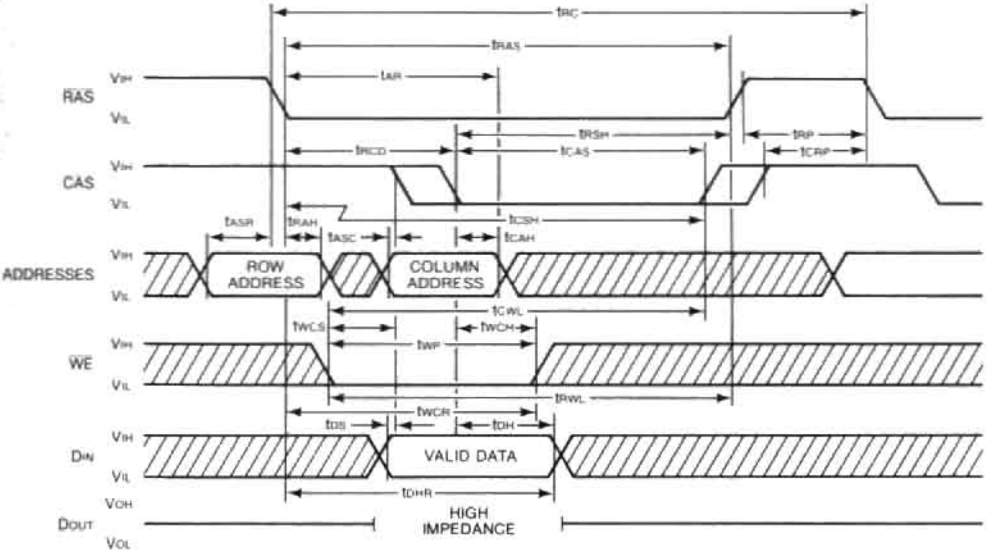
Notes:

1. An initial pause of 100μs is required after power-up followed by any 8 RAS cycles (Example: RAS only) before proper device operation is achieved.
2. AC measurements assume t_T = 5ns.
3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Assumes that $t_{RCD} \leq t_{RCD}$ (max.).
   If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max)
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max.)
6. Measured with a load circuit equivalent to 2 TTL loads and 100 pF
7. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} \geq t_{RWD}$ (min.) the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

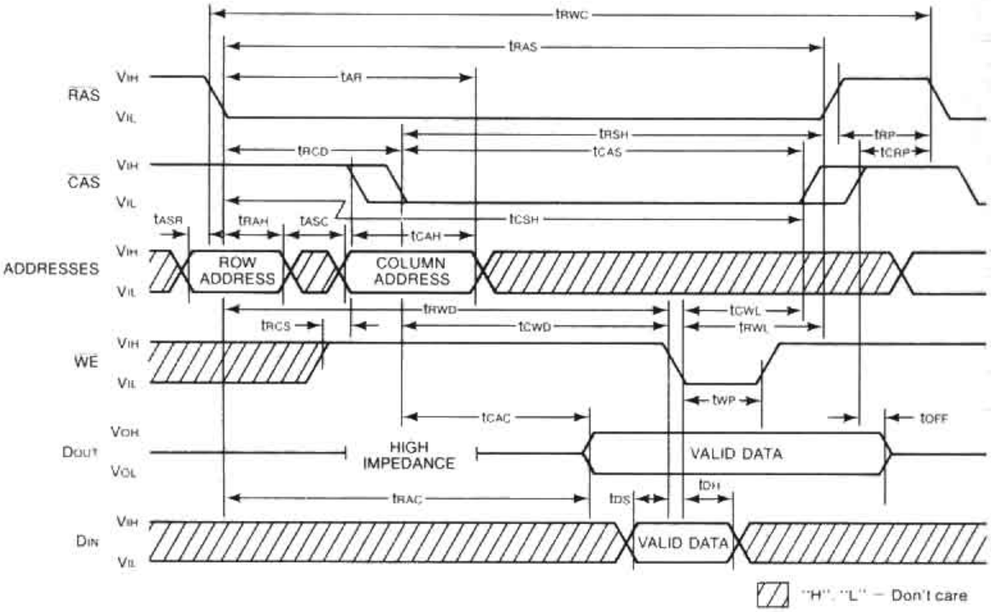
READ CYCLE TIMING



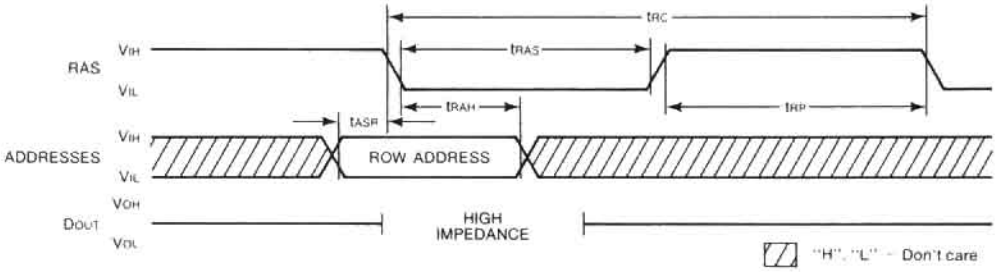
WRITE CYCLE TIMING (EARLY WRITE)



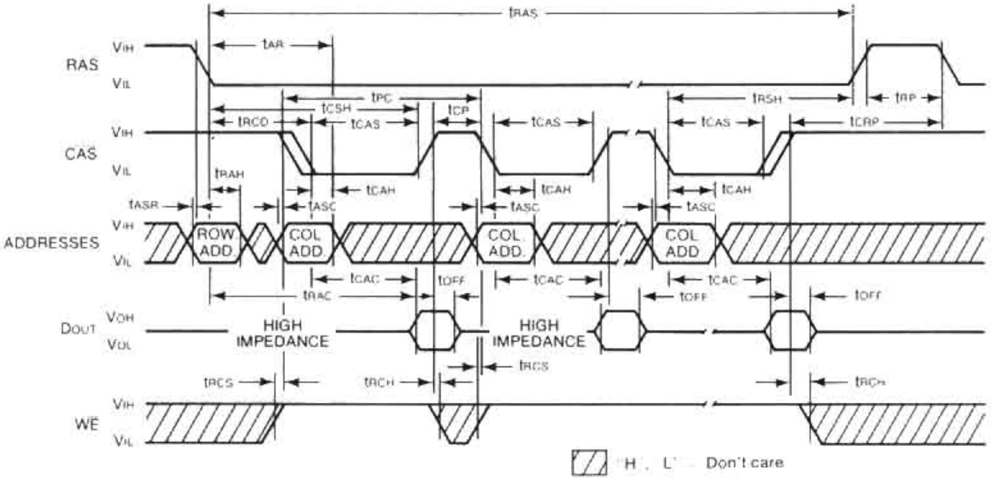
READ-WRITE/READ-MODIFY-WRITE CYCLE



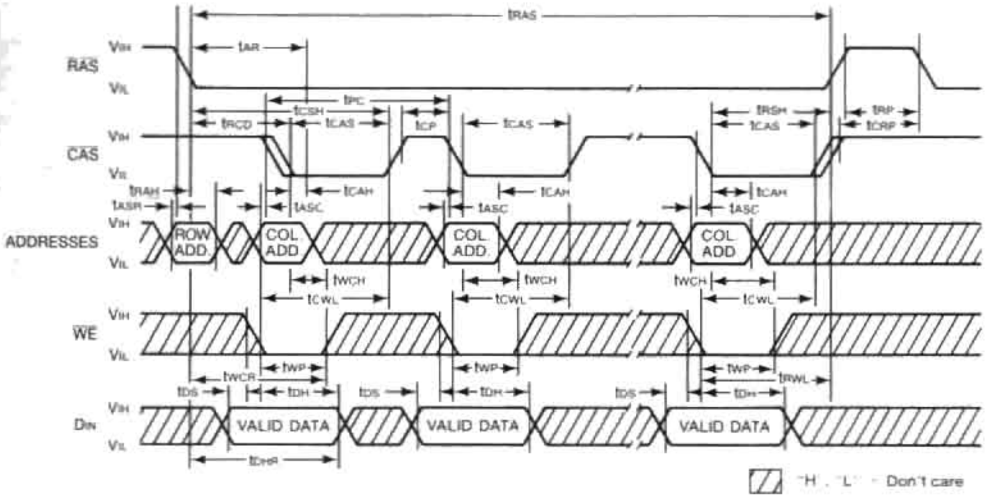
$\overline{\text{RAS}}$ ONLY REFRESH TIMING ($\overline{\text{CAS}}$: VIH, $\overline{\text{WE}}$ & Din : Don't care)



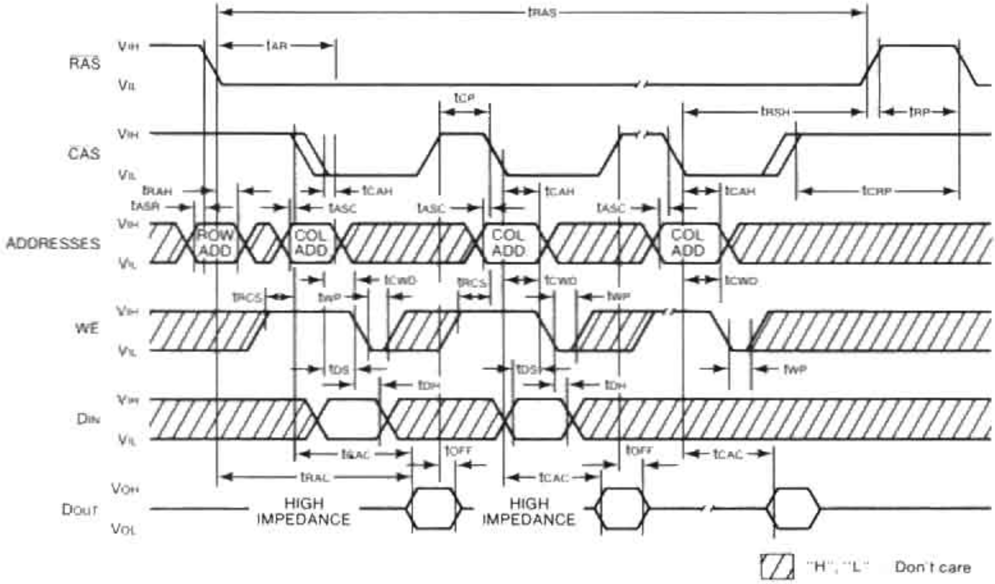
PAGE MODE READ CYCLE



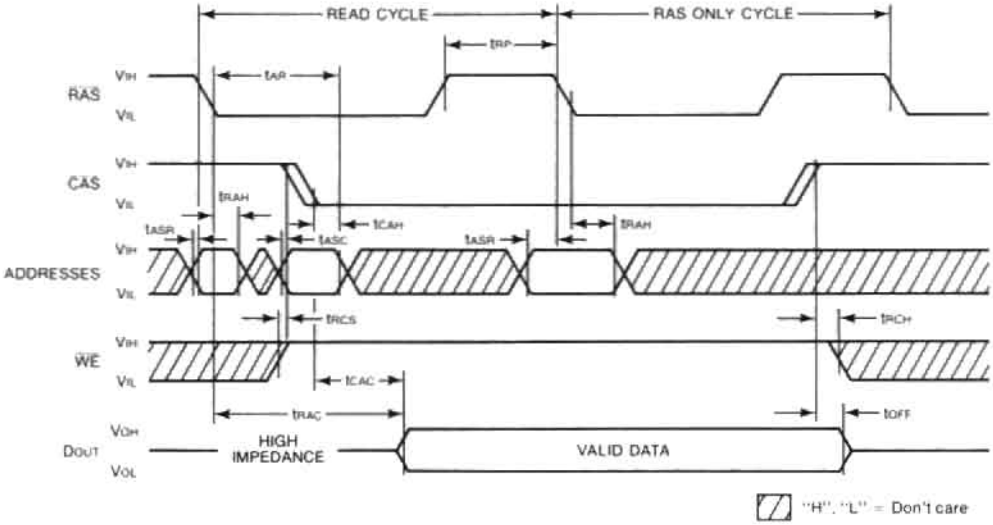
PAGE MODE WRITE CYCLE



PAGE MODE, READ-MODIFY-WRITE CYCLE

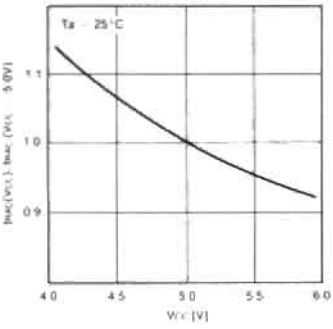


HIDDEN REFRESH

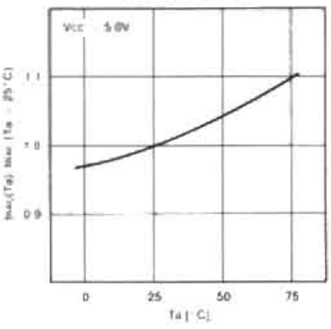


TYPICAL CHARACTERISTICS

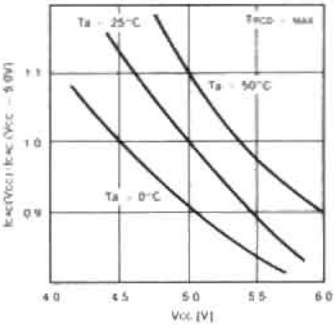
Access time from RAS
(Relative value) v.s. Vcc



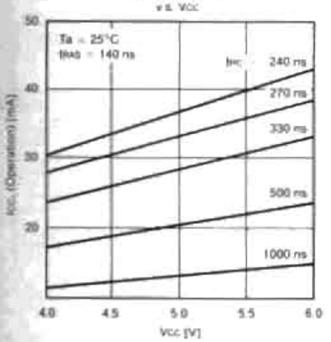
Access time from RAS
(Relative value) v.s. Ta



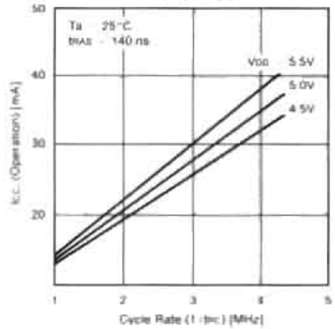
Access time from CAS
(Relative value) v.s. VCC



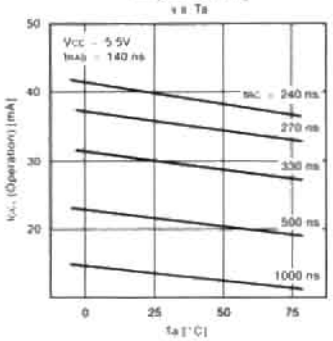
I_{CC1} (t_{RAS} Constant)
v.s. V_{CC}



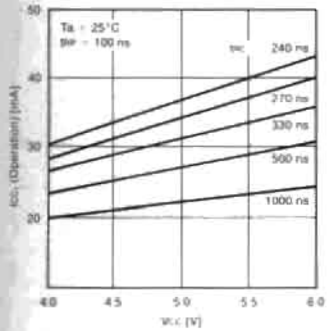
I_{CC1} (t_{RAS} Constant)
v.s. Cycle rate



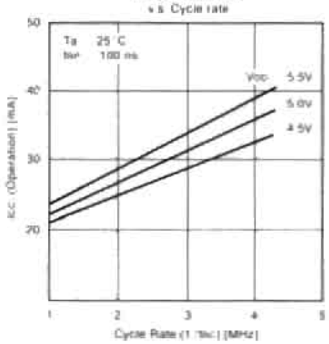
I_{CC1} (t_{RAS} Constant)
v.s. Ta



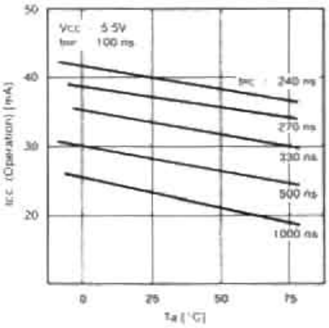
I_{CC1} (t_{RP} Constant)
v.s. V_{CC}



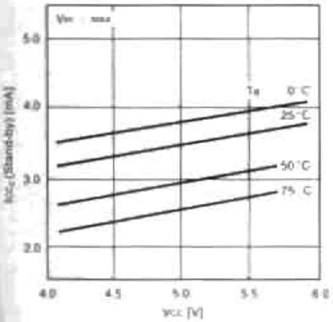
I_{CC1} (t_{RP} Constant)
v.s. Cycle rate



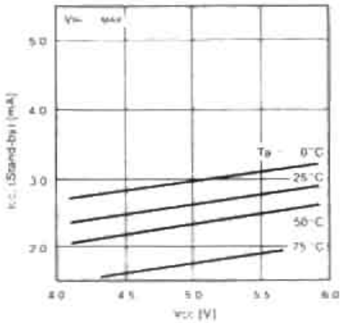
I_{CC1} (t_{RP} Constant)
v.s. Ta



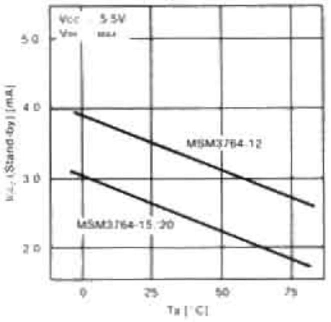
I_{CC2} (MSM3764-12)
v.s. V_{CC}



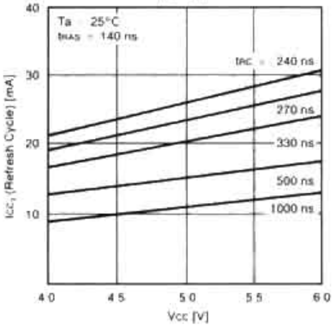
I_{CC2} (MSM3764-15, 20)
v.s. V_{CC}



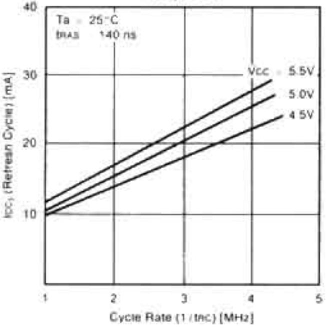
I_{CC2} v.s. Ta



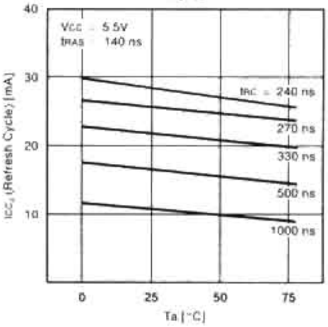
I_{CC3} (t_{RAS} Constant)
v.s. V_{CC}



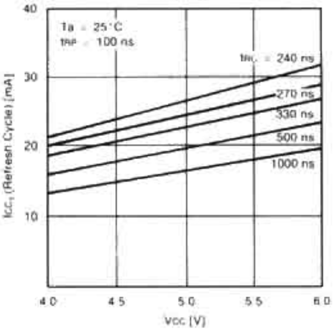
I_{CC3} (t_{RAS} Constant)
v.s. Cycle rate



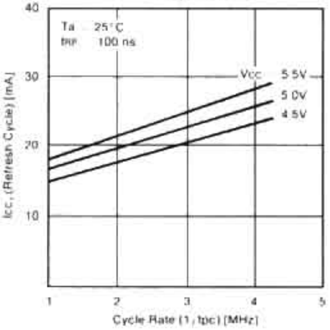
I_{CC3} (t_{RAS} Constant)
v.s. Ta



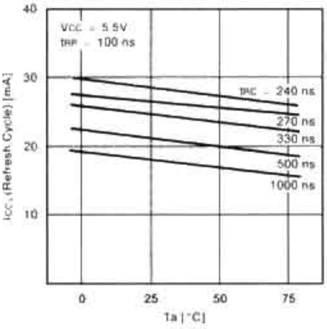
I_{CC3} (t_{RP} Constant)
v.s. V_{CC}



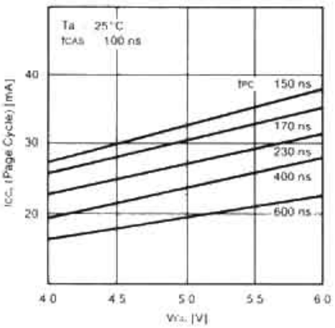
I_{CC3} (t_{RP} Constant)
v.s. Cycle rate



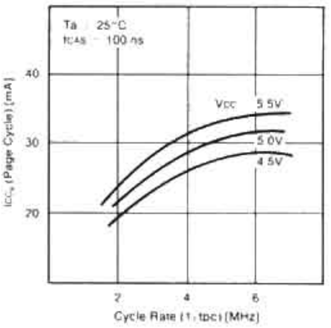
I_{CC3} (t_{RP} Constant)
v.s. Ta



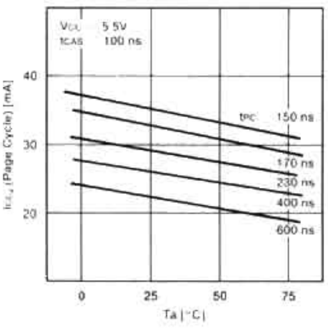
I_{CC4} (t_{CAS} Constant)
v.s. V_{CC}



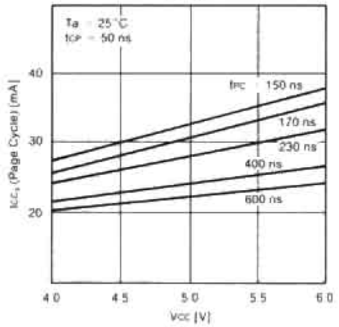
I_{CC4} (t_{CAS} Constant)
v.s. Cycle rate



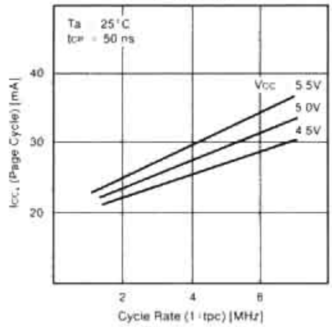
I_{CC4} (t_{CAS} Constant)
v.s. Ta



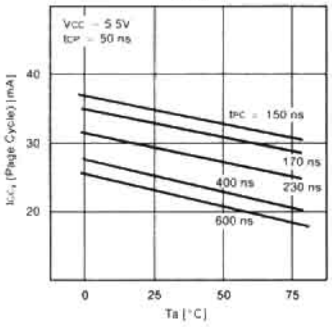
I_{CC4} (t_{CP} Constant)
v.s. V_{CC}



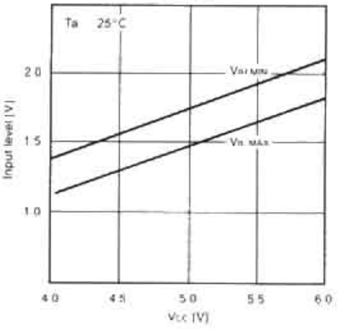
I_{CC4} (t_{CP} Constant)
v.s. Cycle rate



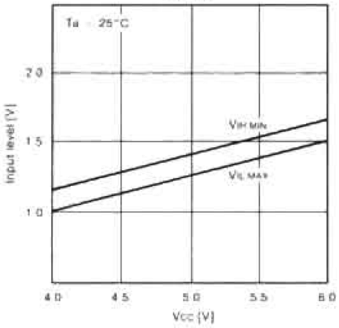
I_{CC4} (t_{CP} Constant)
v.s. Ta



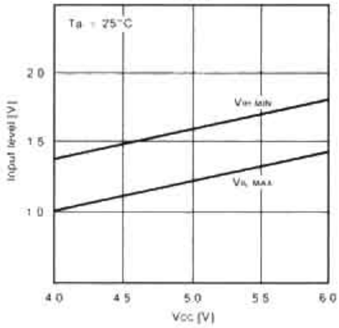
Address Input
v.s. V_{CC}



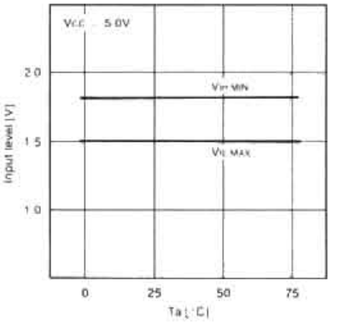
Data Input
v.s. V_{CC}



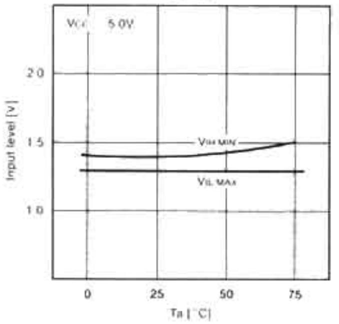
Clock Input
v.s. V_{CC}



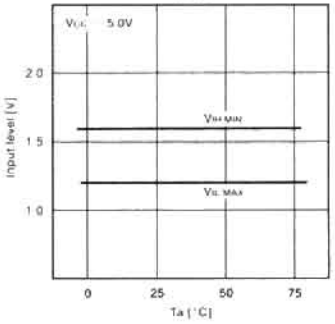
Address Input
v.s. Ta



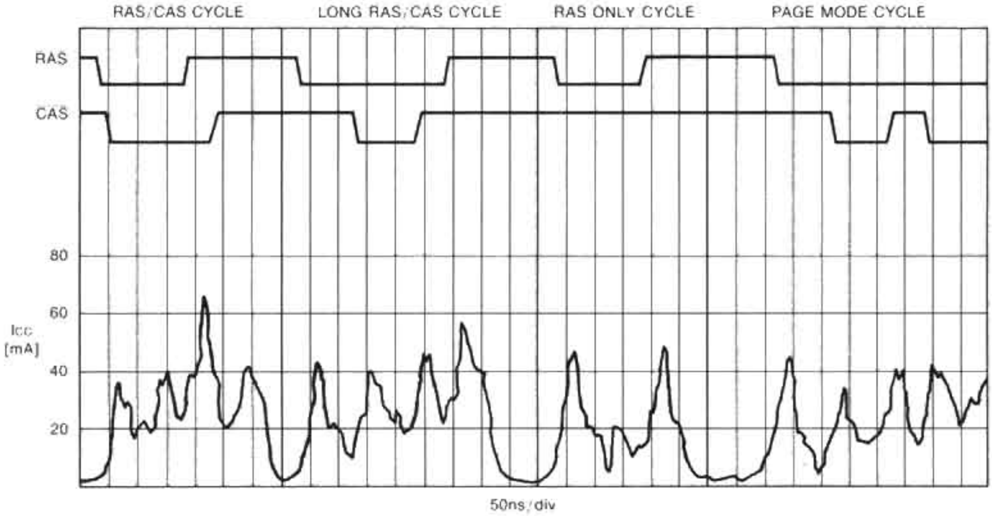
Data Input
v.s. Ta



Clock Input
v.s. Ta



TYPICAL SUPPLY CURRENT WAVE FORMS



FUNCTIONAL DESCRIPTION

ADDRESS INPUTS: A total of sixteen binary input address bits are required to decode any 1 of 65,536 storage cell locations within the MSM3764. Eight row-address bits are established on the input pins (A_0 through A_7) and latched with the Row Address Strobe ($\overline{RAS}$). The eight column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

WRITE ENABLE: The read mode or write mode is selected with the $\overline{WE}$ input. A logic high (1) on $\overline{WE}$ dictates read mode; logic low (0) dictates write mode. Data input is disabled when read mode is selected.

DATA INPUT: Data is written into the MSM3764 during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before CAS, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

DATA OUTPUT: The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remain valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

PAGE MODE: Page-mode operation permits strobing the row-address into the MSM3764 while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

REFRESH: Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row-addresses (A_0 ~ A_6) at least every two milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_7. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 128 row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further, $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

HIDDEN REFRESH: RAS ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ as V_{IL} from a previous memory read cycle.

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FUJITSU
MICROELECTRONICS

MB8264N
MB8264E

NMOS 65,536-BIT DYNAMIC [redacted]
RANDOM ACCESS MEMORY

VEMBER 1980

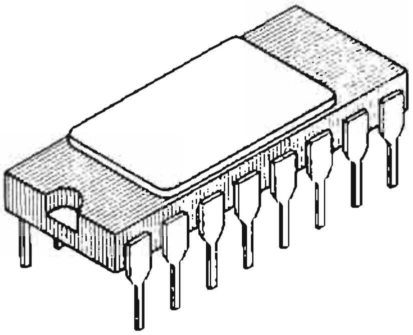
DESCRIPTION

The Fujitsu MB8264 is a fully decoded, dynamic NMOS random access memory organized as 65536 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

Multiplexed row and column address inputs permit the MB8264 to be housed in a standard 16 pin DIP. Pin-outs conform to the JEDEC approved pin out.

The MB8264 is fabricated using silicon-gate NMOS and Fujitsu's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are noncritical, and power supply tolerance is ± 10%. All inputs/outputs are TTL compatible.

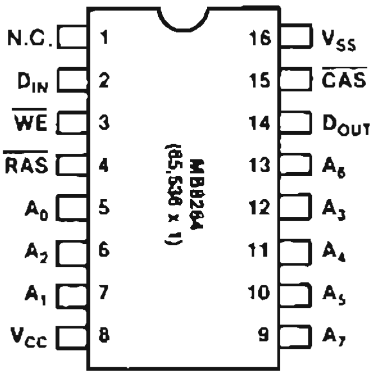


CASE DIP 16C-A01
CERAMIC PACKAGE

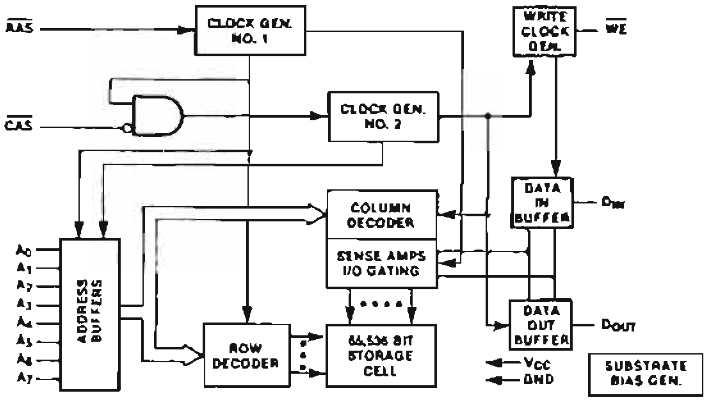
FEATURES

- 65,536 x 1 RAM, 16 pin package
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time,
  150ns Max (MB8264E)
  200ns Max (MB8264N)
- Cycle time,
  270ns Min MB8264E
  330ns Min MB8264N
- Low power: 28 mW MAX standby
  248 mW Max Active (MB8264N)
  303 mW Max Active (MB8264E)
- ± 10% tolerance on +5 volt supply
- On chip substrate bias generator
- All inputs/outputs TTL compatible, low capacitive load
- Output three-state
- "Gated" $\overline{CAS}$
- 128 refresh cycles
- Common I/O capability using "Early Write" operation
- Output unlatched at cycle end allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-Mode capability
- On-chip latches for Addresses and Data-In
- Hidden Refresh Capability

PIN ASSIGNMENT



MB8264 BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Voltage on any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply relative to V_{SS}	V_{CC}	−1 to +7.0	V
Operating Temperature	T_{OP}	0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C
Power Dissipation	P_D	1.0	W
Short Circuit Output Current	I_{OS}	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Value			Unit	Temperature
		Min	Typ	Max		
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0	—	0.8	V	

CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Capacitance A_0 ~ A_7, D_{IN}	C_{IN1}	—	—	5	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	—	—	8	pF
Output Capacitance D_{OUT}	C_{OUT}	—	—	7	pF

STATIC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
OPERATING CURRENT* (MB8264N)	I_{CC1}		45	mA
Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min) (MB8264E)	I_{CC1}	—	55	mA
STANDBY CURRENT* Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	5	mA
REFRESH CURRENT (MB8264N)	I_{CC3}		36	mA
Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min) (MB8264E)	I_{CC3}	—	42	mA
PAGE MODE CURRENT Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = min)	I_{CC4}	—	34	mA
INPUT LEAKAGE CURRENT Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V) all pins not under test = 0V)	I_{IL}	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OL}	−10	10	μA
OUTPUT LEVEL Output low voltage (I_{OL} = 4.2mA)	V_{OL}	—	0.4	V
OUTPUT LEVEL Output high voltage (I_{OH} = −5mA)	V_{OH}	2.4	—	V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

DYNAMIC CHARACTERISTICS Notes 1,2,3

(Recommended operating conditions unless otherwise notes.)

Parameter	Notes	Symbol	MB8264N Min	MB8264N Typ	MB8264N Max	MB8264E Min	MB8264E Typ	MB8264E Max	Unit
Time between Refresh		t_{REF}	—	—	2	—	—	2	ms
Random Read/Write Cycle Time		t_{RC}	330	—	—	270	—	—	ns
Read-Write Cycle Time		t_{RWC}	375	—	—	300	—	—	ns
Page Mode Cycle Time		t_{PC}	225	—	—	170	—	—	ns
Access Time from $\overline{RAS}$	4 6	t_{RAC}	—	—	200	—	—	150	ns
Access Time from $\overline{CAS}$	5 6	t_{CAC}	—	—	135	—	—	100	ns
Output Buffer Turn Off Delay		t_{OFF}	0	—	50	0	—	40	ns
Transition Time		t_T	3	—	50	3	—	35	ns
$\overline{RAS}$ Precharge Time		t_{RP}	120	—	—	100	—	—	ns
$\overline{RAS}$ Pulse Width		t_{RAS}	200	—	10000	150	—	10000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	135	—	—	100	—	—	ns
$\overline{CAS}$ Precharge Time		t_{CP}	80	—	—	60	—	—	ns
$\overline{CAS}$ Pulse Width		t_{CAS}	135	—	10000	100	—	10000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	200	—	—	150	—	—	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	7 8	t_{RCD}	30	—	65	25	—	50	ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	—	0	—	—	ns
Row Address Set Up Time		t_{ASR}	0	—	—	0	—	—	ns
Row Address Hold Time		t_{RAH}	20	—	—	15	—	—	ns
Column Address Set Up Time		t_{ASC}	0	—	—	0	—	—	ns
Column Address Hold Time		t_{CAH}	55	—	—	45	—	—	ns
Column Address Hold Time Referenced to RAS		t_{AR}	120	—	—	95	—	—	ns
Read Command Set Up Time		t_{RCS}	0	—	—	0	—	—	ns
Read Command Hold Time		t_{RCH}	0	—	—	0	—	—	ns
Write Command Set Up Time	9	t_{WCS}	– 10	—	—	– 10	—	—	ns
Write Command Hold Time		t_{WCH}	55	—	—	45	—	—	ns
Write Command Hold Time Referenced to $\overline{RAS}$		t_{WCR}	120	—	—	95	—	—	ns
Write Command Pulse Width		t_{WP}	55	—	—	45	—	—	ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	80	—	—	60	—	—	ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	80	—	—	60	—	—	ns
Data In Set Up Time		t_{DS}	0	—	—	0	—	—	ns
Data In Hold Time		t_{DH}	55	—	—	45	—	—	ns
Data In Hold Time Referenced to $\overline{RAS}$		t_{DHR}	120	—	—	95	—	—	ns
$\overline{CAS}$ to $\overline{WE}$ Delay	9	t_{CWD}	95	—	—	70	—	—	ns
$\overline{RAS}$ to $\overline{WE}$ Delay	9	t_{RWD}	160	—	—	120	—	—	ns
Read Command Hold Time Referenced to RAS		t_{RRH}	25	—	—	20	—	—	ns

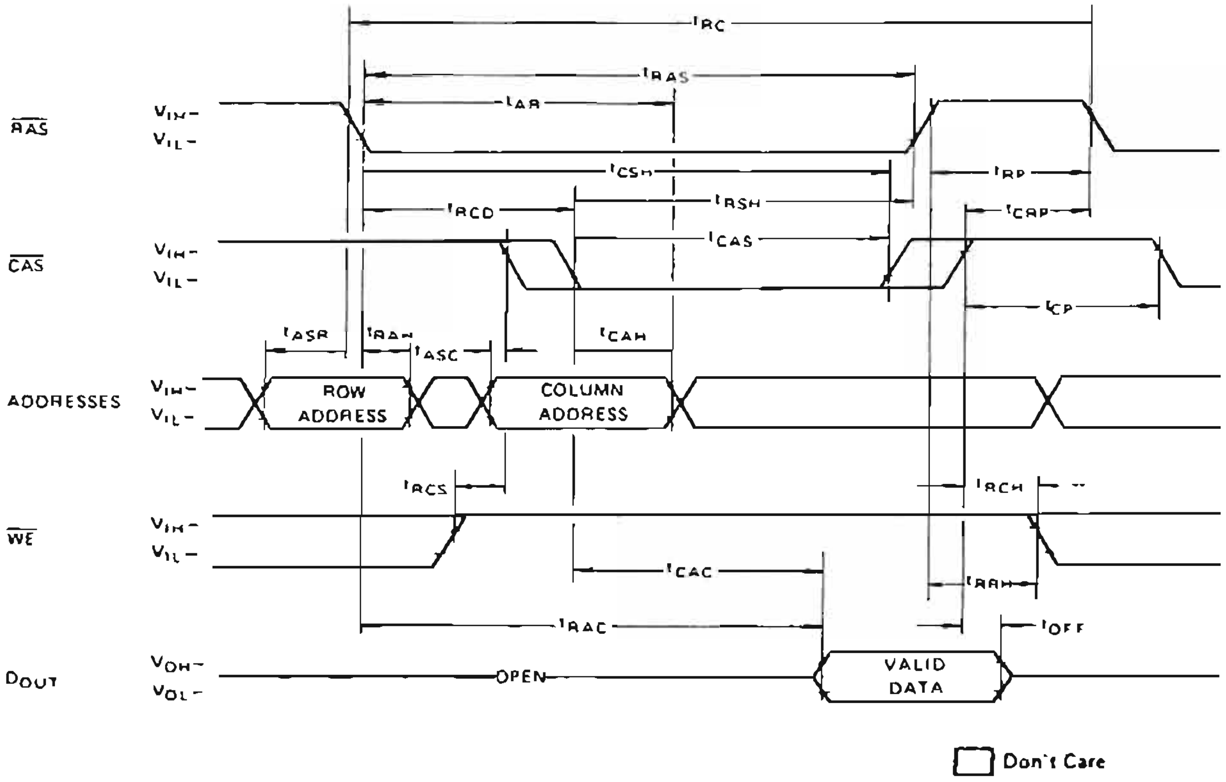
Notes:

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{\text{RAS}}$ cycles before proper device operation is achieved.
2. Dynamic measurements assume t_T = 5ns.
3. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH}(min) and V_{IL}(max).
4. Assumes that $t_{RCD} \leq t_{RCD}$(max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. Measured with a load equivalent to 2 TTL loads and 100 pF.
7. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{RCD}(min) = t_{RAH}(min) + $2t_T$(t_T = 5ns) + t_{ASC}(min).
9. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle.

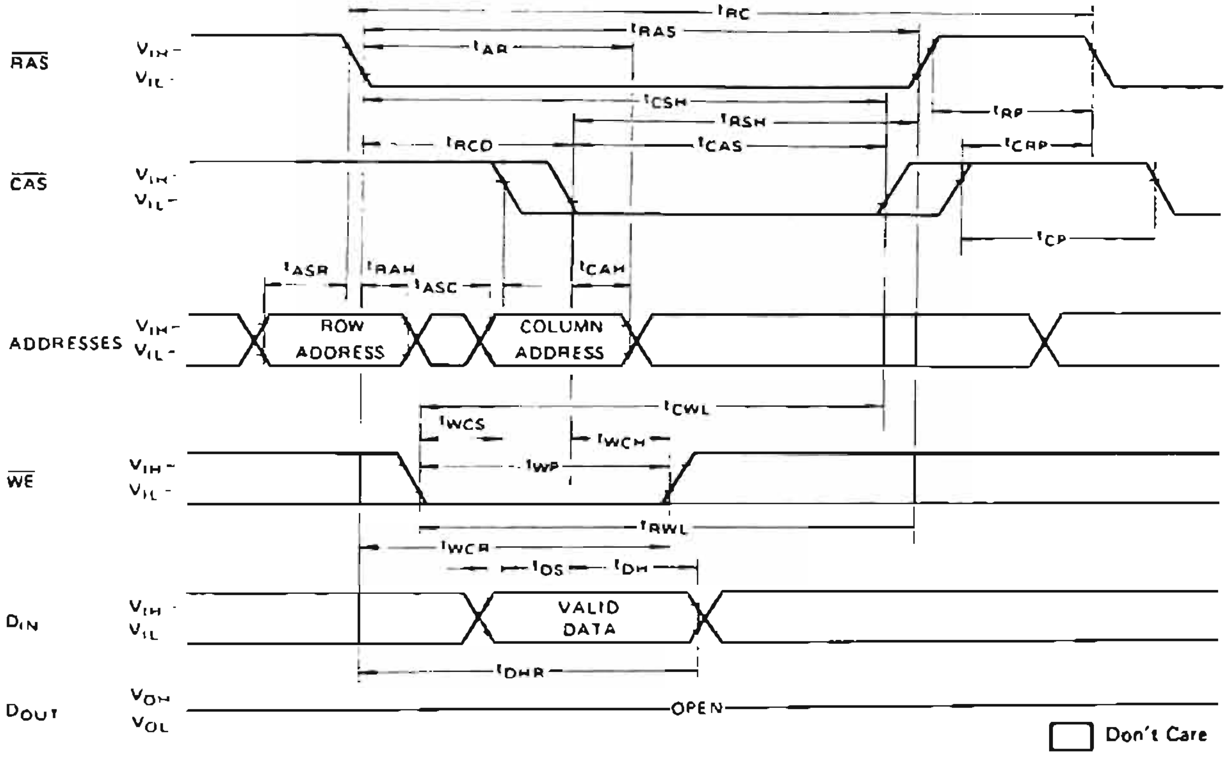
   If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.

TIMING DIAGRAMS

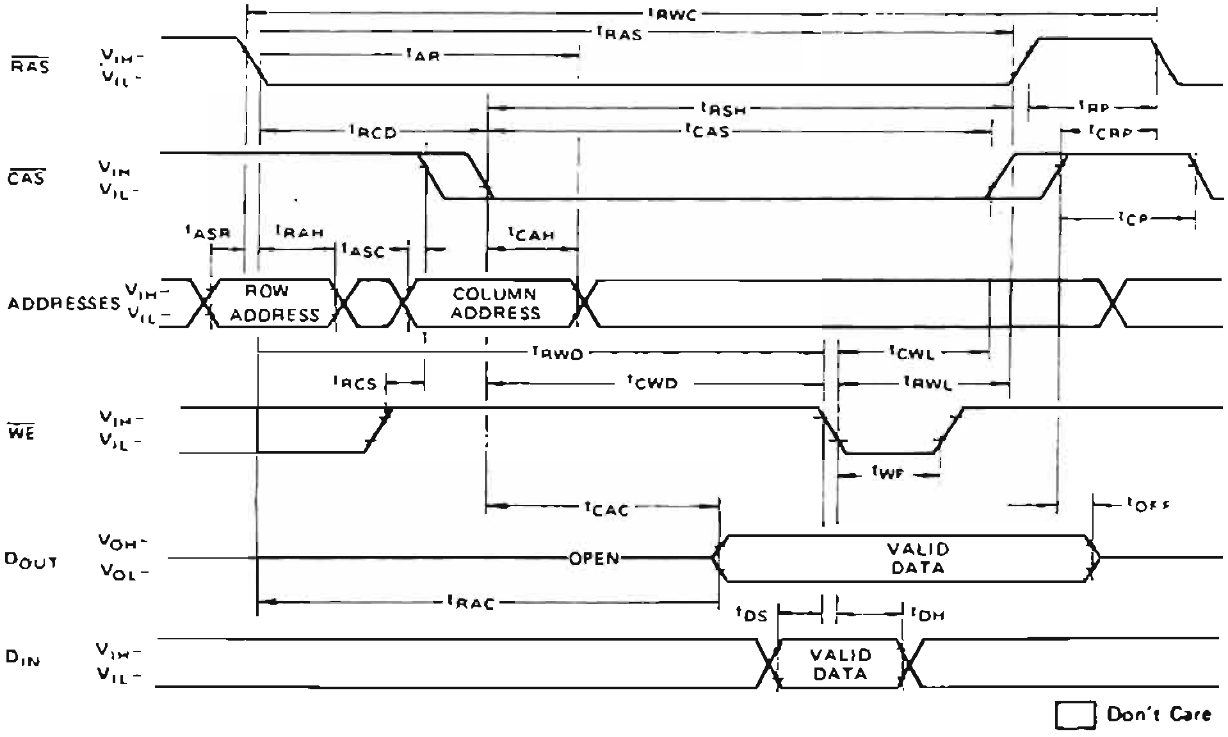
READ CYCLE TIMING DIAGRAM



WRITE CYCLE (EARLY WRITE)

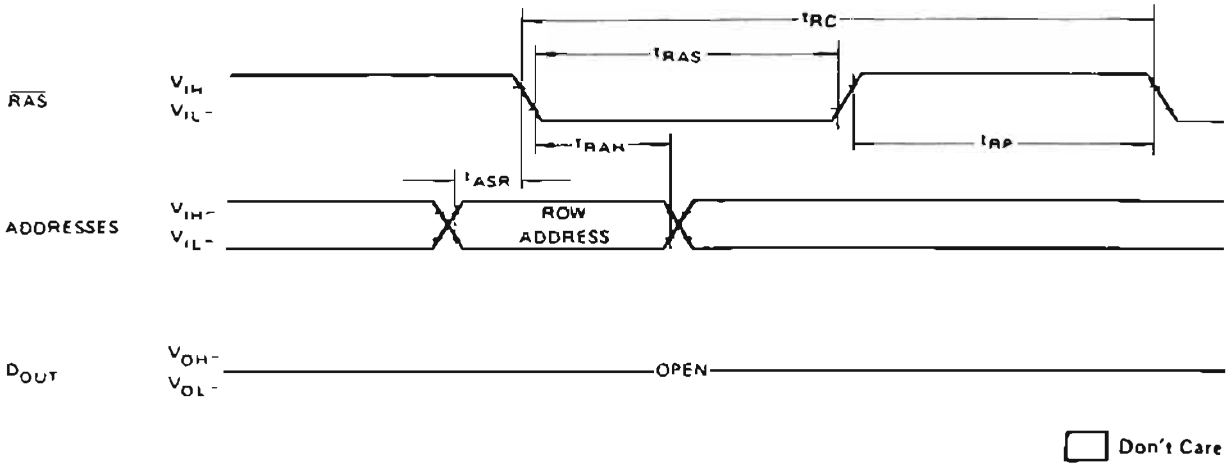


READ-WRITE/READ-MODIFY-WRITE CYCLE

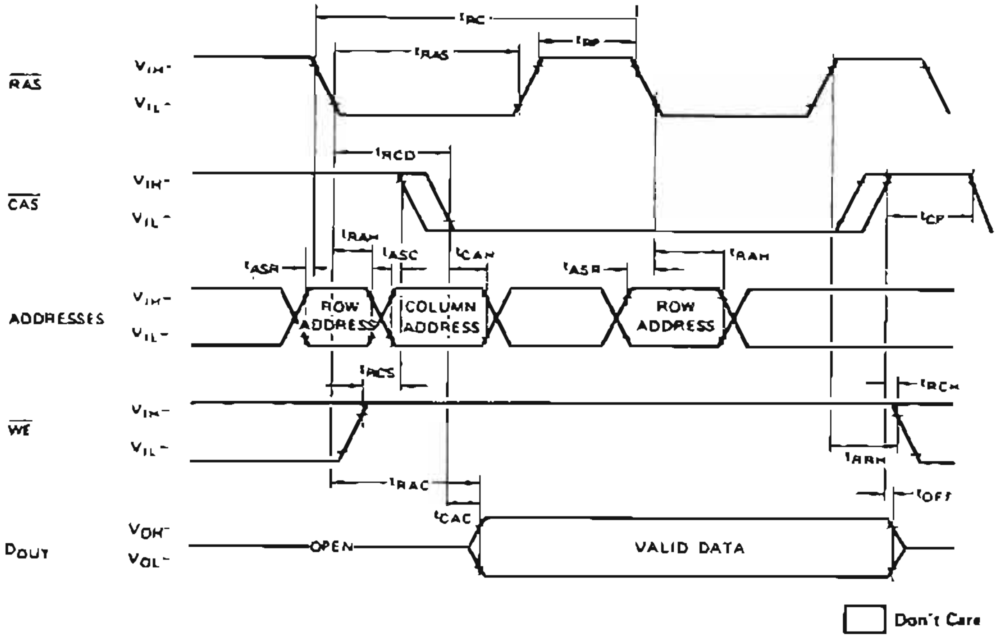


"$\overline{\text{RAS}}$-ONLY" REFRESH CYCLE

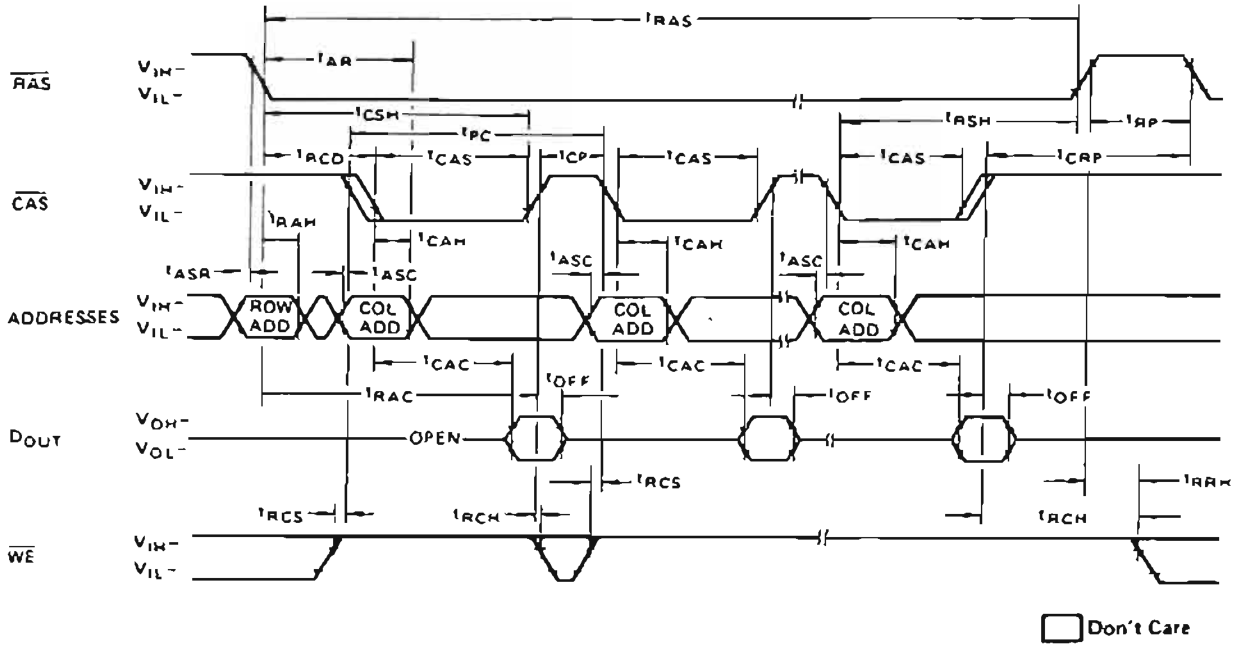
NOTE: $\overline{\text{CAS}}$ = V_{IH}, $\overline{\text{WE}}$ = Don't care



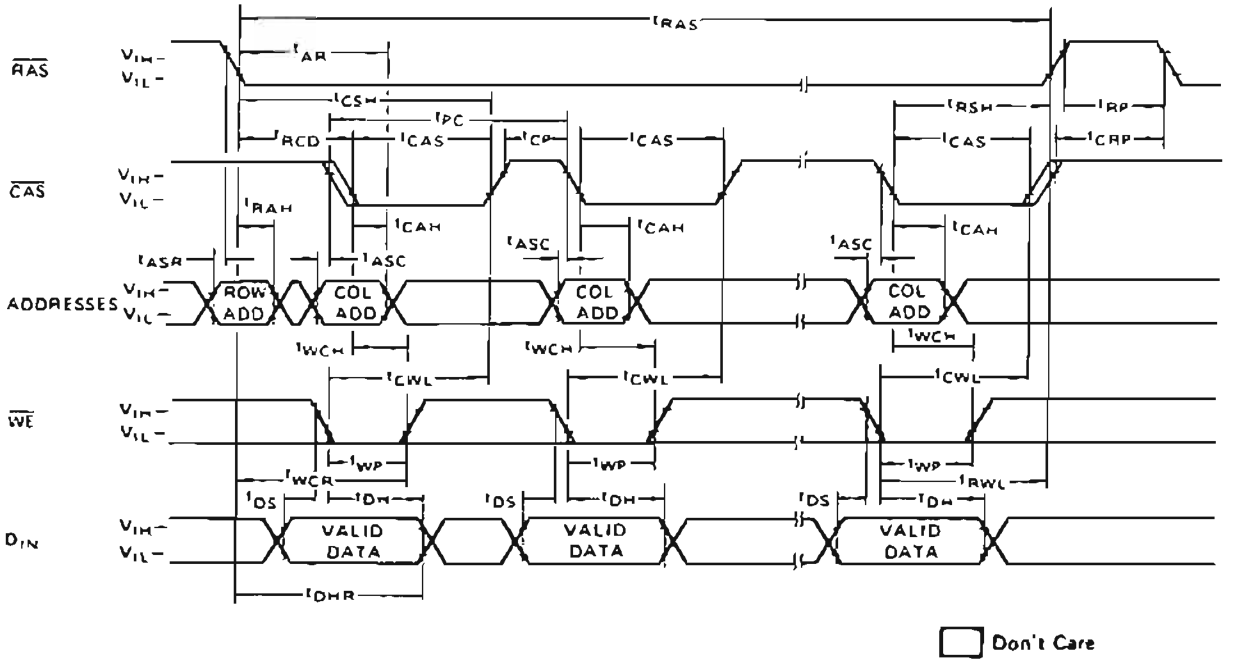
HIDDEN REFRESH



PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



DESCRIPTION

Address Inputs:

A total of sixteen binary input address bits are required to decode any 1 of 65536 storage cell locations within the MB 8264. Eight row-address bits are established on the input pins (A_0 through A_7) and latched with the Row Address Strobe ($\overline{\text{RAS}}$). The eight column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{\text{CAS}}$). All input addresses must be stable on or before the falling edge of $\overline{\text{RAS}}$. $\overline{\text{CAS}}$ is internally inhibited (or "gated") by $\overline{\text{RAS}}$ to permit triggering of $\overline{\text{CAS}}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read mode or write mode is selected with the $\overline{\text{WE}}$ input. A logic high (1) on $\overline{\text{WE}}$ dictates read mode; logic low(0) dictates write mode. Data input is disabled when read mode is selected.

Data Input:

Data is written into the MB 8264 during a write or read-write cycle. The last falling edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{\text{WE}}$ is brought low (write mode) before $\overline{\text{CAS}}$, D_{IN} is strobed by $\overline{\text{CAS}}$, and the set-up and hold times are referenced to $\overline{\text{CAS}}$. In a read-write cycle, $\overline{\text{WE}}$ will be delayed until $\overline{\text{CAS}}$ has made its negative transition. Thus D_{IN} is strobed by $\overline{\text{WE}}$, and set-up and hold times are referenced to $\overline{\text{WE}}$.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{\text{CAS}}$ is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from transition of $\overline{\text{RAS}}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{\text{CAS}}$ when the transition occurs after t_{RCD} (max). Data remain valid until $\overline{\text{CAS}}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page Mode:

Page-mode operation permits strobing the row-address into the MB 8264 while maintaining $\overline{\text{RAS}}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{\text{RAS}}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

Refresh:

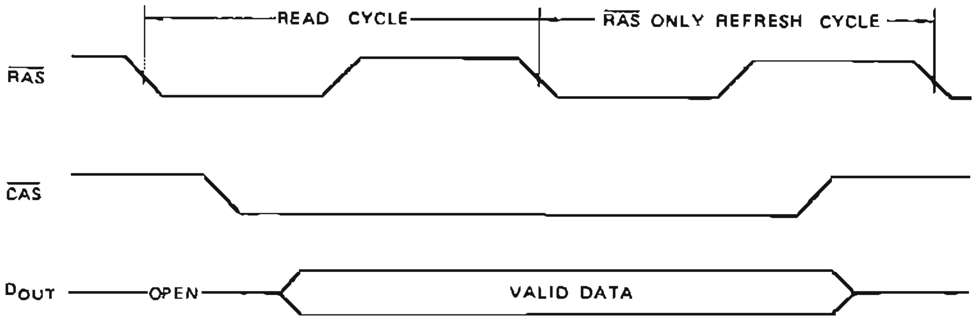
Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row-addresses ($A_0 \sim A_6$) at least every two milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_7. $\overline{\text{RAS}}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{\text{CAS}}$ is brought low. Strobing each of 128 row-addresses with $\overline{\text{RAS}}$ will cause all bits in each row to be refreshed. Further $\overline{\text{RAS}}$-only refresh results in a substantial reduction in power dissipation.

Hidden Refresh:

$\overline{\text{RAS}}$ ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.

Hidden Refresh is performed by holding $\overline{\text{CAS}}$ as V_{IL} from a previous memory read cycle. (see Figure below)

FIG. 2 — HIDDEN REFRESH



TYPICAL CHARACTERISTICS CURVES

FIG. 3 — SUPPLY CURRENT vs V_{CC} DURING POWER UP

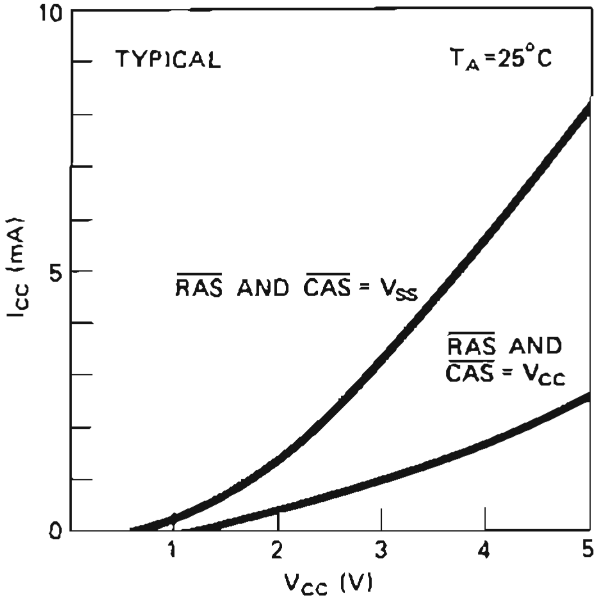


FIG. 4 — $\overline{RAS}$ ACCESS TIME vs SUPPLY VOLTAGE

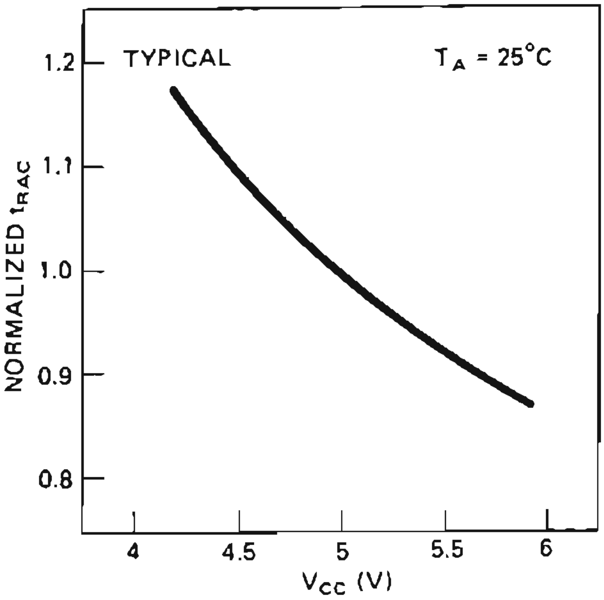


FIG. 5 — $\overline{CAS}$ ACCESS TIME vs SUPPLY VOLTAGE

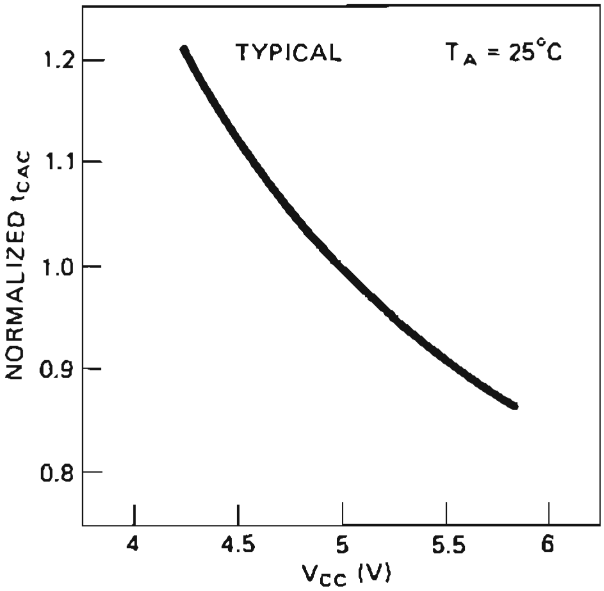
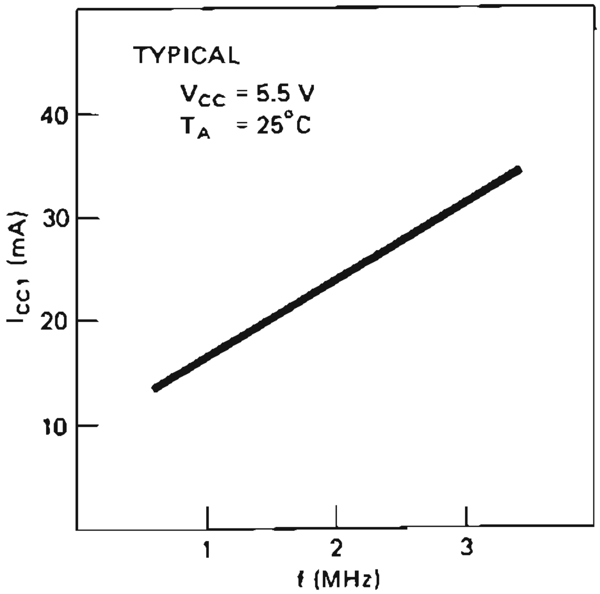
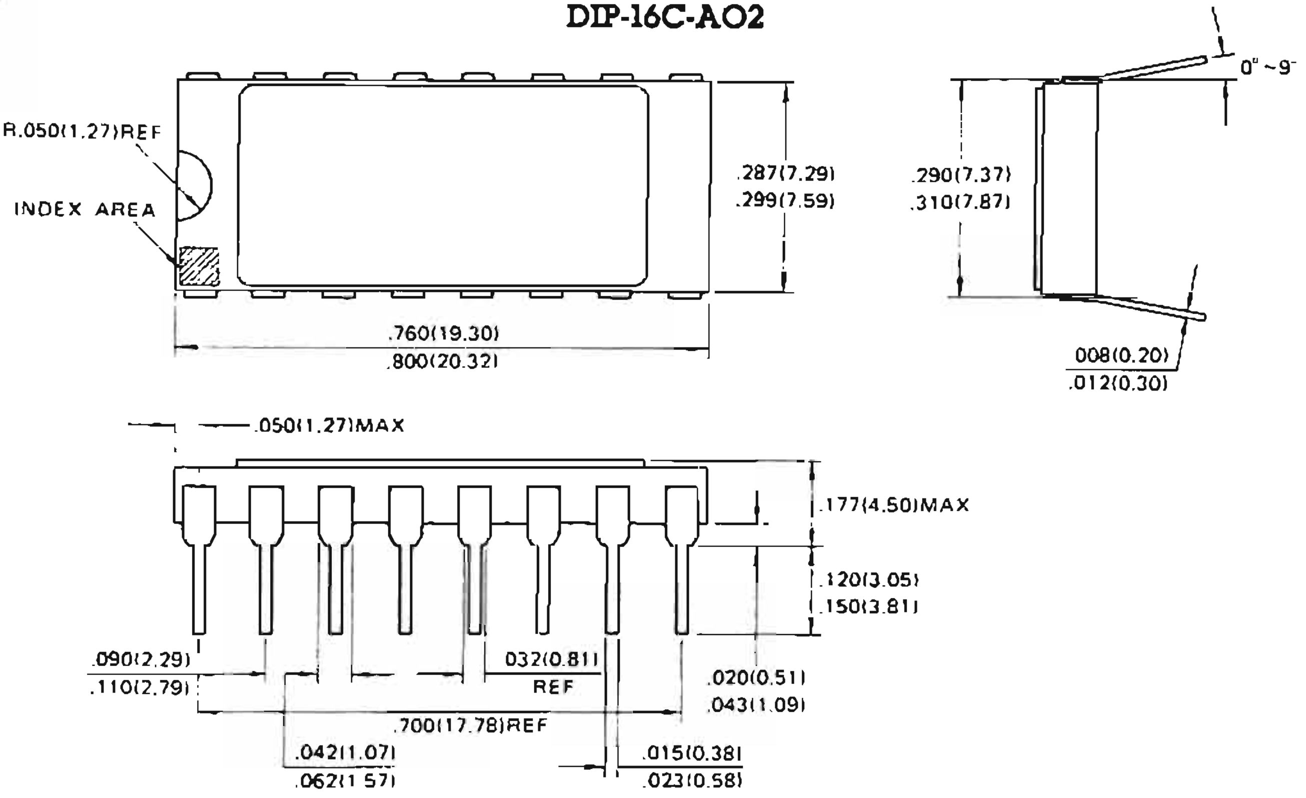


FIG. 6 — SUPPLY CURRENT vs FREQUENCY



ACKAGE DIMENSIONS Dimensions in inches (millimeters)

16-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE DIP-16C-AO2



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MB8264N

~~Jim Cain~~

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Manufacturer	Board characteristics				
	Type (Note 1)	Capacity (bytes): word length (bits) (Note 2)	Segmentation (Note 3)	Maximum clock frequency (MHz)	Typical/ maximum current (mA)
MULTIBUS					
Advanced Digital Technology	DRAM	64K to 96K; 8/16 + 6 ECC	S(32K), B, E	2 0	2500/3000
	DRAM	128K to 1M; 8/16 + 6 ECC	S(16K), B, E	2.5	3000/3500
Bubbl-Tec	bubble	92K; 8		1	400/500
Central Data Corp.	PROM	128K, 8/16 D			300/500
	SRAM	32K, 8/16 D	S(16K), E		4100/5800
	DRAM	128K; 8/16 D	S(16K), E		1700/2300
Comark Corp.	DRAM	64K to 512K; 8/16 D, P	S(128K), B, E	22-1184	2000
Heurikon Corp.	SRAM	16K to 32K; 8	B, E	2.0	
	DRAM	64K to 512K; 8/16 D	B, E	2.0	2000/3000
Intel Corp.	DRAM	4K; 8/16	S(4K)		800/1700
	bubble	128K or 512K; 8			300/2400
	DRAM	16K; 8/16 D	S(4K), E	25	2700/3300
	DRAM	32K; 8/16 D, P	S(4K), E	25	3200/4000
	DRAM	64K; 8/16 D	S(4K), E	25	3000/3800
	DRAM	64K, 8/16 D, P	S(4K), E	25	3200/4000
	DRAM	128K; 8/16 D, P	S(4K), E	25	3600/4600
	DRAM	256K, 8/16 D, P	S(4K), E	25	3600/4600
	→ DRAM	512K, 8/16 D, P	S(4K), E	25	3500/4800
	DRAM/EPROM	8K, 32K, 8 D	S(4K), E		3000/3820
	DRAM/EPROM	16K, 32K, 8	S(4K), E		3000/3820
	EPROM	16K; 8	S(4K)		2100/2700
	EPROM	64K; 8/16	S(4), E		
Micro Memory, Inc.	Core	32K, 8/16	S(4K)	1 0	1000/3750
	→ DRAM	512K, 8/16	S(4K)	2 0	1400
	Core	8K to 16K, 8	S(4K), B	1.0	1000/2000
	Core & PROM	32K, 8	S(4K), B	1 0	1000/2000
	Core	16K, 8/16	S(16K), B	1 25	800/3000
National Semiconductor	DRAM	128K, 8 + 1P/ 16 + 2P	S(4K), E	2.5	
	→ DRAM	512K, 8 + 1P/ 16 + 2P	S(4K), E	2 5	3200/3600
	DRAM	16K to 64K; 8/16 D	S(16K), B, E	1.5	2000/3000
	DRAM	16K to 64K, 8	S(16K), B, E	2.0	2000
	EPROM, PROM, ROM	32K to 128K; 8/16 D	S(16K), B, E	1.4	1700/2700

Memory chip characteristics			Price and delivery				
Model number/ type (Note 1)	Organization (n x m bits)	Access time (nsec.)	Fully assembled unit price (Q - 1; Q - 100) (Note 4)	Unpopulated unit price (Q - 1; Q - 100) (Note 5)	Delivery time (weeks ARO)	Date first shipped	For more information circle no.
	16K x 1	150	$1850 to $2050; $1125 to $1350 M, T		4 to 6	9/79	313
8264	64K x 1	150	$2350 to $8650; $1425 to $5300 M, T		4 to 8	9/80	314
TIB 0203	92K x 1	2500	$2400, $1500 M, T			12/79	315
2758, 2764/ PROM	1K x 8, 8K x 8		$185, $120 M, T	$185, $120 S	6	3/80	316
6104/SRAM	4K x 1	200	$1445, $925 M, T	$815, $520 S	6	3/80	317
4116/DRAM	16K x 1	150	$1775, $1135 M, T	$700, $450 S	6	6/80	318
4116	16K x 1 or 64K x 1	350	$940 (64K), $1450 (128K), M, T		4	9/81	319
	4K x 1		$595 to $895, M, T		4 to 6		320
	32K x 1, 64K x 1	200	$1833 to $6115 M, T		4 to 6		322
5101	128 x 1		$1150, T		stock	1976	323
7110-1	1M x 1	4800	$1600 to $6250; $1215 to $4360 T		4	12/80	321
2110	8K x 1	120	$705 T, M		stock	8/81	324
2110	8K x 1	120	$955 T, M		stock	8/81	325
2117	16K x 1	120	$1150 T, M		stock	6/76	326
2118	16K x 1	120	$1310 T, M		stock	8/81	327
2164	64K x 1	200	$1810 T, M		stock	8/81	328
2164	64K x 1	200	$3195 M, T		stock	8/81	329
2164	64K x 1	200	$3995 M, T		4	8/81	330
2117	16K x 1	120	$980 T, M		stock	1/80	331
2117	16K x 1	120	$1185 M, T		stock	1/80	332
2708	2K x 8		$380 M, T		stock	1976	333
2716/2732	4K x 8		$570 M, T		stock	1/79	334
			$1275; $975 T		4	12/79	335
4164		150	$2000, $1500 T		3	8/81	336
			$725 to $849, $592 to $680 T		4	1/78 to 8/78	337
			$790, $690 T		4	1/79	338
			$875, $690 T		4	12/80	339
5290	16K x 1	200	$1430 M, T		4	6/81	340
4164	64K x 1	200	$3645 M, T		4	8/81	341
MM5290, 5298	16K x 1, 8K x 1	200	$1210; $910 M, T		4	6/78	342
MM5290	16K x 1	200	$1300 to $1730	$910 to $1211 M, T	4	12/80	343
2758, 2716, 2732 2764, 2316, 2332	1K x 8, 2K x 8 4K x 8 8K x 8	400		$570, $428 S	4	8/81	344

Manufacturer	Board characteristics				
	Type (Note 1)	Capacity (bytes): word length (bits) (Note 2)	Segmentation (Note 3)	Maximum clock frequency (MHz)	Typical/ maximum current (mA)
MULTIBUS					
	DRAM/PROM/ROM	4K to 16K, 8/16 D	S(4K), B, E	1.5	4100/4600
	EPROM/PROM/ROM	16K to 32K, 8/16 D	S(4K or 8K), B, E	1.4	100/1400
Plessy Microsystems	SRAM	64K; 8/16	S(16K), B, E	5.0	/1500
	→ DRAM	512K; 8/16 + 6 ECC	S(16K), B, E	2.0	1500/2000
	DRAM	64K; 8	S(16K), B, E	2.0	/1500
Relational Memory Systems, Inc.	DRAM	256K; 8/16	S(64K), B, E	4.0	300
	SRAM	16K, 8/16 D	S(4K), B, E	5.0	400
	DRAM	64K, 8/16 D	S(16K), B, E	4.0	150
Syscom, Inc.	PROM	64K; 8/16	S(4K), B		1600
Texas Instruments	→ DRAM	(64K, 128K, 256K, 512K)/16 + 6 ECC	S(4K), E		
Zendex Corp.	SRAM	16K; 8/16 D	S(64K), B, E	5.0	1200/1500
	DRAM	128K; 8/16	128K, E	5.0	900/1000
STD BUS					
Applied Micro Technology, Inc.	SRAM	16K, 8	S(16K), B, E	6.0	2500
	DRAM	64K; 8	S(16K), B, E	6.0	200
	EPROM/RAM	32K; 8	S(8K, 16K, or 32K), B, E	6.0	150
Desert Microsystems, Inc.	DRAM	64K; 8	S(64K), E	5.0	/800 to 870
	PROM	64K; 8	S(16K, 32K, or 64K), E	5.0	280
Digital Dynamics, Inc.	DRAM	2K, 8	S(1K)	2.5	360/580
	PROM	32K; 8	S(8K), B, E	4.0	380/600
Enterprise Systems Corp.	SRAM	8K; 8	S(4K), B, E	4	300/1000
Matrix Corp.	RAM/EPROM	32K; 8	S(4K)		
Mostek	DRAM	16K to 32K, 8	S(8K, 16K, 32K)	4.0	375/600
	EPROM	16K; 8	S(4K or 8K)	4.0	800/1200
	UMC	32K, 8	S(4K, 8K, or 16K)	4.0	800/1200
	SRAM	4K to 8K, 8	S(4K or 8K)	4.0	600/1000
	SRAM	2K to 4K, 8	S(2K or 4K)	4.0	700/1000
	DRAM	128K, 16 + 1P	S(16K), B, E		3000
	DRAM	256, 16 + 5 or 6 ECC	S(16K), B, E		4560
	DRAM	2M; 32 + 7 ECC	S(64K), E		7700
Transwave Corp.	SRAM	8K, 8		4	900

Memory chip characteristics			Price and delivery				
Model number/ type (Note 1)	Organization (n x m bits)	Access time (nsec.)	Fully assembled unit price (Q = 1; Q - 100) (Note 4)	Unpopulated unit price (Q = 1; Q = 100) (Note 5)	Delivery time (weeks ARO)	Date first shipped	For more information circle no.
ROM: MM2308, 2316E, 2708, 2716 RAM: MM4027, 4116	ROM: 1K x 8, 1K x 16, RAM, 4K x 1, 16K x 1	200 (RAM), 400 (ROM)	$780 to $1077; $585 to $808 M, T		4	6/79	345
MM2308, 2316E, 2708, 2716	1K x 8, 1K x 16	400		$343 to $377; $258 to $283 S	stock	8/79	346
HM 6116LP	2K x 8	120	$2200 T		10	12/80	347
HM 4864	64K x 1	275	$4750 T		10	6/81	348
4716	16K x 1	275	$700 T		10	4/79	349
		210	$2600, $2160 M, T		2	9/81	350
		150	$745; $460 M, T		2	6/80	351
		250	$995, $560 M, T		2	1/80	352
2716, 2732, 2532	2K x 8, 4K x 8		$495, $380 M, T		4	11/80	353
4532, 4164			M, T		4 to 6	4/81	354
MK 4118-2	1K x 8	150	$1504; $1203 T		4	8/81	355
4116	16K x 1	300	$1280; $825		4	6/80	356
2114	1K x 4	150 or 400	$325; $260 M, T	$120; $96 S	1	1/80	357
4116	16K x 1	250	$700, $560 M, T		1	10/79	358
		250	$200; $160 M, T	$125; $100 S	1	1/81	359
2118, 4116	16K x 1	250	$750 to $950; $525 to $665 M, T		4	2/81	360
2716, 2732, 2764				$195; $137 S	4	10/80	361
6514	1K x 4	450	$295 M, T		10	4/80	362
2716, 2732	2K x 8, 4K x 8			$225; $180 S	6	6/80	363
444	1K x 4	450, 250	$550; $395 M, T		2-4	9/80	364
2716			$170 to $490 M, T				365
MK 4116	16K x 1	200 or 350	$235 to $275 M, T		2	2/79	366
MK 2716	16K x 8	450	$499		2	9/79	367
MK 2732	4K x 8	450	$160		2	9/79	368
MK 4118	1K x 8	250	$245 to $295 M, T		2	6/79	369
HM6514	1K x 4	300	$399 to $450 M, T		2	6/80	370
MK 4116	16K x 1	135	$3145 M, T		4	10/77	371
MK 4116	16K x 1	135	$5180 to $5280 M, T		4	8/80	372
MK 4564, MK 4116	16K x 1	135	$7995 M, T		6	8/81	373
2114	512 x 8	450	$262; $222 M, T			5/81	374

[illegible]