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Submittal Details

Document Info

Title : Program for Workshop on the Frontiers of Extreme Computing
Document Number : 5232620 SAND Number : 2005-6637 P
Review Type : Electronic Status : Approved
Sandia Contact : DEBENEDICTIS,ERIK P. Submittal Type : Book/Book Chapter
Requestor : DEBENEDICTIS,ERIK P. Submit Date : 10/18/2005
Comments : Release for the program of a workshop. Program contains abstracts by the listed authors as well as orignal expository material by the General Chairman (DeBenedictis)
Peer Reviewed? : N

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Partnership Info

Partnership Involved : No
Partner Approval : Agreement Number :

Patent Info

Scientific or Technical in Content : Yes
Technical Advance : No TA Form Filed : No
SD Number :

Classification and Sensitivity Info

Title : Unclassified-Unlimited Abstract : Document : Unclassified-Unlimited
Additional Limited Release Info : None.
DUSA : None.

Routing Details

Role	Routed To	Approved By	Approval Date
Derivative Classifier Approver	SUMMERS,RANDALL M.	SUMMERS,RANDALL M.	10/18/2005
Conditions:			
Common Look & Feel Approver	BRITTENHAM,PHILLIP W.	BRITTENHAM,PHILLIP W.	10/19/2005
Conditions:			
Manager Approver	PUNDIT,NEIL D.	PUNDIT,NEIL D.	10/20/2005
Conditions:			
Administrator Approver	LUCERO,ARLENE M.	KRAMER,SAMUEL	09/07/2007

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FRONTIERS OF EXTREME COMPUTING

Chaminade Executive Conference Center
Santa Cruz, California, USA
October 24-27, 2005

Experts representing computer and computational science will meet to create a comprehensive picture of future computing.

Technologies	Applications Areas
Moore's Law (transistors)	Scientific Research
Advanced Architectures	Defense Problems
New Devices	Engineering
Reversible Logic	Robotics
Quantum Computing	

The workshop's product is to be a report with a picture of computing, including all the major options, and describing a proper role for each in context

ZETTA FLOPS

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On the Web at:
http://www.zettaflops.org

Approved for release: Sandia National Laboratories SAND 2005-6637P

Locations

General Session, Monday - Thursday	Santa Cruz
Breakout Sessions, Monday - Thursday	Cowell, Natural Bridges, and Executive Suite 116
Breakfast (Monday - Thursday)	Sunset Dining Room
Lunch (Monday - Thursday)	Sunset Dining Room
Dinner (Sunday & Monday)	Sunset Dining Room
Banquet Dinner (Tuesday) & Private Dinner (Wednesday)	New Brighton
AM/PM Breaks	Linwoods (1st Floor) and Seacliff Lounge & Terrace (2nd Floor)

Note on Sunset Dining Room hours:
Breakfast is served 7:00 am -10:00 am
Lunch is served 11:30 am-1:30 pm
Dinner is served 5:00 pm-8:00 pm

A New Conference on the Frontiers of Extreme Computing: Transitioning Moore's Law to the Next Generation

Date
October 24-27, 2005

Location
Chaminade conference center, Santa Cruz, CA

Sponsors
DOE (Sandia National Laboratories, Lawrence Berkeley National Laboratories), National Science Foundation, Florida State University

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- David Keyes, Columbia University
- Thomas Sterling, Louisiana State University
- Thomas Theis, IBM

General Conference Chair
- Erik DeBenedictis, Sandia

Workshop on the Frontiers of Extreme Computing – Overview of the Workshop

Erik P. DeBenedictis, Sandia National Laboratories

***Abstract*—While it is widely believed that increased computer power will enable computers to do more good things for society, this argument needs more detail to be persuasive and compelling. The Frontiers of Extreme Computing Workshop will study specific problems facing society that are amenable to solution by computer and match them to computer technologies that could be used to solve them.**

The problems facing society addressed in the talks are the general use of scientific simulation for advancing science and technology, specific challenge problems like understanding and mitigating global warming, the generation of abundant low-cost, and clean electricity from seawater through nuclear fusion, and national security improvements through extensive data analysis. Robotics for terrestrial use and space exploration will require physically smaller computers, but equally advanced technology.

Solving the problems above will require a range of computers, including both incremental enhancements to what is available today and new approaches. The workshop includes participants covering the whole range – the industry roadmap for transistors, computer architecture, emerging superconducting, nanotech, and molecular devices, and other forms of computing including reversible logic and quantum computing.

The workshop will also include discussion of algorithmic and software issues that will emerge as changing hardware is required to address existing problems at larger scale as well as entirely new problems.

The workshop's objective is to connect important problems for society with the computer technology necessary to solve each problem. This includes proposing a series of technology levels (such as "transistorized," "post-transistor," "reversible," and "quantum"), tying them to the problems they should be able solve for society ("global warming," "Mars rovers," etc.) and forming an action plan for reaching each level.

I. The Value of Computers to Society

Much of this workshop's organization is illustrated in figures 1 and 2.

The left side of figure 1 plots some important future uses of computers. These figures are limited to supercomputers that would be measured in FLOPS, although the workshop is not limited to this single class of performance metrics.

David Bader will give the "application keynote" Monday morning at 9 AM on the use of supercomputers to address and mitigate problems related to global warming. The study in the SCaLeS report (described below) estimates the amount of increased computer performance necessary to address more and more aspects of the global warming problem, reaching full solution near or at 1 Zettaflops of supercomputer throughput.

Steve Jardin will give a presentation Tuesday 9:30 AM on the simulation of plasma fusion via computers for the design of electric power generation systems that would convert seawater into electricity. The SCaLeS study included computer performance estimates (with uncertainty bounds causing points to be represented as ellipses) for the portions of a coupled multi-physics simulation reproduced in figure 1.

While there is no speaker on the topic, it is widely known that certain problems in code breaking would be significantly above the top of this chart.

David Keyes will give an overview Tuesday 9 AM of many

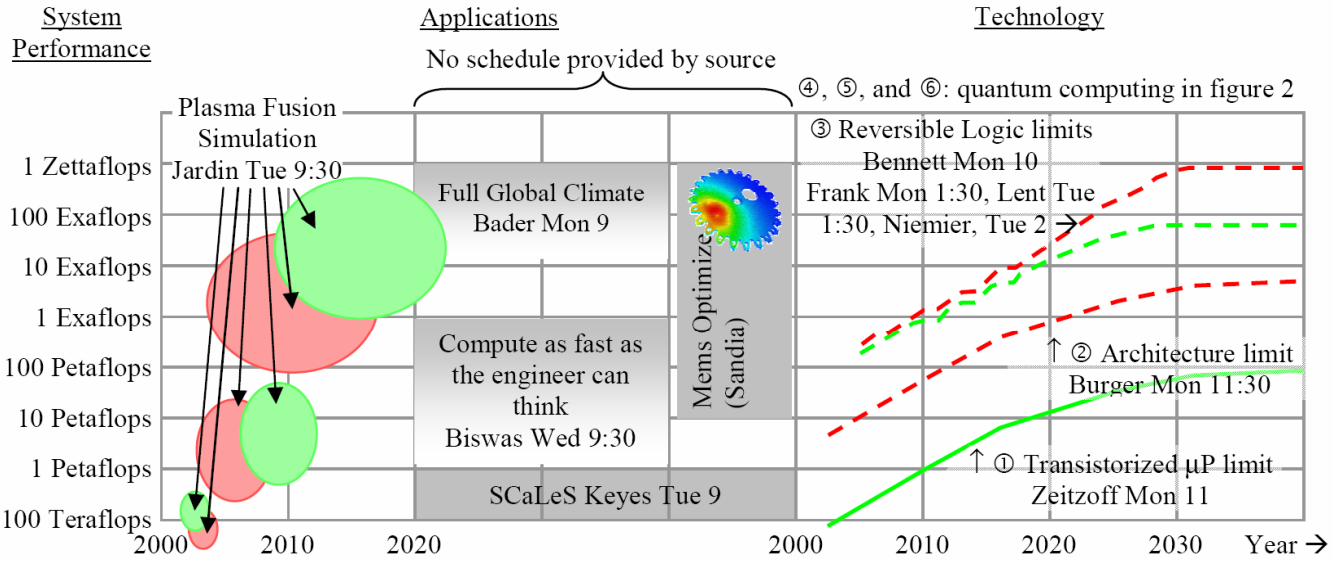

Figure 1. Supercomputer applications and technology projections.

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areas in science for which supercomputing can drive progress. This overview was motivated by the SCaLeS study, mentioned above.

Jeff Nichols will give a presentation Wednesday 11 AM of the computing program at ORNL implementing and supporting DOE's agenda in science.

Bill Dally will give a presentation Tuesday 10 AM on the National Academy of Sciences (NAS) report on the future of supercomputing, of which he is a contributor.

We might expect that changing circumstances will lead to new applications of computers. Since FLOPS might not be the best measure for these applications, they are listed below without being represented on figure 1:

Bruce Hendrickson will speak Wednesday 9 AM on problems solvable with graph algorithms. The specific problems are related to homeland and national defense and tend to require large-memory computers capable of making inferential connections across large data sets.

Rupak Biswas of NASA will speak Wednesday 9:30 AM on computing requirements at NASA. NASA does both ground-based and space-based computing. Space-based computers will be much smaller than megawatt-level supercomputers, yet the performance per chip, pound, watt, reliability etc. may be superior to a behemoth supercomputer.

II. Advances Due To Moore's Law

The right side of figure 1 illustrates the limits of "Moore's Law" based on a $100M budget but different assumptions on computer use. One immediately notices that some applications lie above some of the technology performance curves. While Moore's Law officially describes an observed exponential increase over time of the number of transistors on an integrated circuit, people often apply the idea more broadly. The curves labeled ①, ②, ③, and then the curves in figure 2 are performance limits the chairman created based on increasingly broad assumptions on computer use. The technology speakers will broadly fall into categories based on these assumptions.

Curve ① represents users of advanced computers. These users typically view Moore's Law as an exponential increase in the speed of their code over time (given their computer is replaced with the "latest version" every couple years at constant budget). This interpretation precludes recoding software. While computer architecture is permitted to change, the fact that "legacy" code is highly dependent on architecture constrains these changes. The primary opportunity for advancement is to speed the underlying devices (transistors) and increase parallelism. It is also important that device density increase and cost decline.

Peter Zeitzoff will speak Monday at 11:30 on the International Semiconductor Roadmap for Semiconductors (ITRS). This is the planning study of the semiconductor industry that predicts future progress of Moore's Law and ties it to research and development at the device level. While the ITRS roadmap predicts exponential performance increases over perhaps the next decade, certain fundamental physical properties of transistors will become more and more pronounced and shift the nature of improvements.

Doug Burger will speak Monday at 11:30 AM on the limits of system performance given the semiconductor improvements of the ITRS. Doug will speak about the degree to which improvements in device speed, density, interconnect speed, and so forth will improve overall system throughput.

III. Architectural Advances

In framing the discussion on architecture, the chairman has drawn curve ② 100× above curve ① even though recent computers suffer from sustained performance being a declining fraction of peak (suggesting curve ② should be below curve ① rather than above it).

A program in execution will demand a varying mix of resources, such as arithmetic, memory access, and communications. The static arrangement of devices comprising the computer's architecture is chosen to:

1. Perform operations in parallel; up to the extent parallelism is available in the algorithm.
2. Execute operations on the algorithm's critical path as quickly as possible, since the overall running time is most strongly influenced by the critical path.
3. Mitigate the effects of latency, such as signal propagation delays between processors and memories.
4. Balance bandwidth to avoid bottlenecks and minimize resource access contention.

All the talks on devices suggest future performance gains will come mostly through increased parallelism rather than increased speed. Increasing parallelism creates more activities (threads) to coordinate, creating pressure for more sophisticated architectures.

Bill Dally will give a presentation on how to choose the right commodity hardware components to be most effective for software and applications.

Thomas Sterling will give an overview of Continuum Computer Architecture (CCA), giving general principles for balancing processing, memory, and intercommunications in hardware so that new but effective programming techniques can be applied.

However, the items enumerated above must be deployed effectively yet without excess. Without an effective architecture, the floating-point units (which are the only architectural components that contribute to performance as measured in figure 1) will not be utilized efficiently. On the other hand, the items above are implemented by devices that take up chip area and consume power that in principle could be used by more floating point units.

Curve ② in figure 1 is 100× above curve ① because current microprocessors devote around 1% of their chip area and power budget to the floating-point unit. One could imagine a computing system where this factor approaches 100%. Such a device would look like a solidly packed array of floating point units, similar to a radar signal processor.

Guang Gao will discuss systems software he and his

students are developing for the Cyclops supercomputer. Cyclops has 80 floating-point units per chip (driven by 160 cores units), attaining this high number by cutting down on resources devoted to the enumerated architectural items above. Programming such a design creates challenges, which are the topic of Gao's talk.

The ideas presented to this point will offer extraordinary improvements over today's technologies, but insufficient to address the most ambitious applications. The asymptote of curve ② (~8 Exaflops) has been drawn to illustrate the performance of a $100M system where the chips are solidly packed floating-point units. To exceed this performance level will require a fundamental change in the way computers are constructed.

IV. New Approaches

In the "technology keynote" Monday 10 AM, Charles Bennett will address principles of physics that may someday enable a "frontal assault" on the limits of transistors and make it possible to address problems lying above curve ②. Charles will talk about thermodynamic reversibility and quantum computing, both fields of which he is a founding contributor and which are crucial to the operation of many of the advanced devices discussed later.

Ed Fredkin will give the banquet speech Tuesday evening on Salt computing. [Chairman's Note: This paragraph was written based on a verbal discussion. The abstract Ed provided is somewhat less specific.] Salt computing is an "out of the box" idea based on using pairs of ions in a salt crystal to form a reversible logic gate. The performance boost from salt computing would come from the fact that there are Avogadro's number (6×10^{23}) of pairs of ions in a few grams of salt!

Mike Frank will speak specifically on reversible logic. In layman's terms, reversibility is a way to cut power consumption by recycling the energy in 0s and 1s inside a computer. In reaching the limits of curves ① and ②, the amount of power in each 0 or 1 signal drops so far that the signals can be distinguished from random fluctuations due to thermal motion with just enough reliability. Furthermore, power and apparatus for handling power (including cooling) will dominate the cost of operating a large computer in this year. In reversible logic, 0 and 1 signals are propagated through many levels of logic before being turned into heat. This cuts average energy dissipation, permitting more logic for a system of a given cost.

Energy recycling in reversible logic is readily demonstrable today, yet energy recycling sufficient to exceed the limits of end-of-the-roadmap transistors has not been demonstrated and will be a substantial challenge (in fact, end-of-the-roadmap transistors have not been demonstrated either). As will be described in the paragraphs below, superconducting, nanotech, and molecular device technologies may use the principle of reversibility.

Reversible logic puts additional burden on algorithms because it both raises performance through increased parallelism and changes the nature of logic. This point comes up later.

Quantum computing may boost computer performance by making operations on each bit (called a "qubit") more powerful as opposed to just faster, but introduces substantial complications. Quantum computing will be described more below.

V. Advanced Devices

The approaches to computing described above will frame the discussion of advanced devices. New devices can and should be evaluated for their potential to propel a computer to a high level in figure 1, yet real devices present challenges in materials, manufacturability, and other issues. These challenges often limit device performance. Of course, these limits apply to transistors as well. A number of advanced classical (i. e. non-quantum) technologies will be represented at the workshop. Each of these device technologies could challenge transistors now or at the "end of the roadmap."

Tom Theis of IBM will speak in more detail on this overall topic Tuesday noon, giving a perspective on R&D efforts of the National Nanotech Initiative (NNI) and IBM in this area. IBM's R&D activities include advancing transistor technology, advanced non-transistor devices, and quantum computing.

Arnold Silver will speak Monday at noon on superconducting technologies. These devices offer higher speed than transistors and operate at very low power levels.

Stan Williams will speak Tuesday 11 AM on nanotech research at Hewlett-Packard. HP's R&D activities include advancing transistor technology, advanced non-transistor devices, and quantum computing. [The chairman doesn't have a clear idea of the scope of Stan's presentation.]

Andre DeHon will speak Tuesday 11:30 AM on very high-density logic constructed from nanowires.

Craig Lent and Mike Niemier will speak Tuesday 1 PM and 1:30 PM on Quantum Dot Cellular Automata (QDCA). Craig will speak on the underlying devices, which are of very high density and can operate as reversible logic. Mike will speak on architectural issues in combining molecular-level cellular automata into computational devices.

VI. Quantum Computing

To frame the discussion of quantum computing, figure 2 illustrates how the concept of quantum speedup transforms "Moore's Law." Figure 2 reproduces graphs ① and ② from figure 1, but the scale has been substantially expanded so the curves are much more horizontal.

The quantum computing section will begin with Mike Foster Wednesday 1:30 PM of NSF giving an overview of quantum computing and/or information from a programmatic perspective.

Mark Oskin will give a presentation Wednesday 2 PM related to work on the architecture and feasibility of building quantum computer. This would be a quantum computer that would perform at about the level of 1 integer (or floating

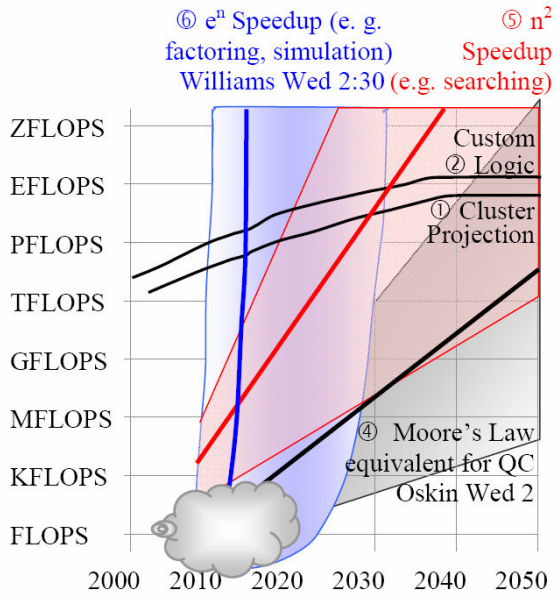

Figure 2: QC algorithm opportunity. Black curves ① & ② illustrate "Moore's Law" improvements for transistorized supercomputers per figure 1 whereas curve ④ illustrates the same growth rate applied to QCs. However, suitably selected quantum algorithms can solve a problem in fewer total operations, with some algorithms achieving quadratic ⑤ and exponential ⑥ speedup over a classical computer (and graphed as the exponential and square of curve ④ with appropriate scaling. Shaded regions indicate realm of uncertainty. Some physical simulations will follow curve ⑥.

point) operation per second.

How long it would take to do the science and engineering called for in Mark's paper is unclear, so we draw a cloud in figure 2 at this point – but this will not affect the idea of the figure. Given that conventional computers operate today at about 1 Petaflops, this would put quantum computers at handicap of at least 15 orders of magnitude.

The heaviest black line and gray region in figure 2 illustrate a hypothetical "Moore's Law" for quantum computers, starting from 1 FLOPS. While it is plausible that quantum computers would be subject to an exponential performance pattern, we have no idea what the "doubling time" would be – so we draw a wide range. It should be readily apparent that quantum computers are unlikely to exceed the performance classical computers within the lifetime of anybody attending this workshop.

However, the enhanced features of qubits will permit some quantum computer algorithms of n quantum operations to be equivalent to classical algorithms of n^2 or e^n operations (subject to constant or polynomial factors). The heaviest red and blue lines (with red and blue uncertainty regions corresponding to the gray uncertainty region) illustrate the speed of a classical computer required to match the throughput of a quantum computer benefiting from quantum speedup. Conclusions can be drawn from these curves, notwithstanding the starting points (under the cloud) or the width of the uncertainty region:

Quadratic quantum speedup (shown in the red graph and pink uncertainty region) doubles the "Moore's Law" slope. This suggests that under optimistic assumptions quantum computers running quadratic speedup algorithms could play a role within the lifetimes of the younger people at this workshop.

Exponential quantum speedup (shown in the blue graph and blue uncertainty region) would translate to a doubly exponential performance growth over time, or an exponential curve on figure 2's log scale. Once the exponential speedup blue curves gather momentum, they quickly overcome 15 orders of magnitude handicap and overtake the fastest classical computers.

Colin Williams presentation Wednesday 2:30 on quantum simulation will address the potential impact of quantum computers to important problems. The value of quantum computers will depend on whether problems of interest fall into the gray, red, or blue regions of figure 2. The expected ability of quantum computers to perform numerical algorithms (like factoring) with exponential speedup has been widely reported in the literature. However, quantum computers are also expected to be able to perform some physical simulation problems with exponential speedup. Physical simulation and searching (the red graph in figure 2) are the major classes of applications for supercomputers today.

VII. Algorithms

Bill Gropp will give a talk and run a session on the very challenging topic of how algorithms and software must adapt over the timeframe covered by this workshop.

Present day algorithms do not have enough parallelism to match emerging hardware. Most programmers write purely sequential code, with the small minority who write parallel code creating 10-10,000 way parallelism. However, all the classical (i. e. non-quantum) computing innovations discussed in this workshop will increase performance through a large increase in parallelism and just a little more speed. It seems inevitable that future computing trends will exhaust existing parallelism and then require further work.

As discussed by Doug Burger, computers will be disproportionately slowed down by code that accesses a lot of memory from the inner loop. However, few existing algorithms pay much attention to locality of inner loop memory access.

There may be other factors.

Quantum computing offers the opportunity to disrupt algorithms. Most mathematicians/programmers have good intuition about what can be easily accomplished in *n* scalar arithmetic operations. Quantum computers offer exponential speedup on Quantum Fourier Transforms (QFTs), making some algorithms that use QFTs dramatically powerful. However, people don't seem to have good intuition about what can be easily accomplished in *n* QFTs.

Abstracts

David Bader - Climate Simulation for Climate Change Studies

Climate modeling is one of the most well-known simulation problems that require high-end computing, data and network resources. Because it is impossible to build a physical laboratory to study climate, climate simulation models are the only tools, with which scientists can integrate their knowledge to gain understanding of this highly nonlinear and complex system. Climate simulation has advanced dramatically over the last two decades, in large part because of demands to study the potential climate changes brought about by human activities, principally the increase in atmospheric carbon dioxide concentrations that result from combustion of carbon-based fossil fuels for energy production.

This presentation will provide a brief introduction to the scientific aspects of climate science and their representation within climate simulation models. The primary focus of the presentation will be on the use of models to simulate climate change. The practical limitations imposed by throughput considerations, computer architectures, programming tools, and available computer resources will be identified.

In the last two years, several visionary conceptual models have been proposed that assume computer hardware were no longer a limitation. These ideas take the concept of climate modeling much closer to a "first principles" approach to simulation that makes reliance on "parameterizations", or closure schemes for important, unresolved processes, much less important. As will be shown, however, a "perfect" simulation is still impossible. Equally important to advances in computer hardware is the necessity for complementary advances in software and programming models, which has not been the case over the past decade. This talk will highlight some of the shortcomings in this area that have prevented climate modeling, and other simulation science applications, from advancing at a rate commensurate with the rate of advance in hardware.

Charles Bennett - Quantum computing -- its promise and limitations

The theory of reversible computation, and more recently quantum computation, have drawn attention to previously neglected physical aspects of information processing, and each has offered some hope of overcoming what were previously thought to be fundamental limits. Neither, however, offers general cure for the anticipated end of Moore's law.

Rupak Biswas – NASA's Science and Engineering Applications in the Future

NASA scientists and engineers have dared to dream about the kinds of applications that could be done if computing resources were unlimited. Imagine aeronautics high-lift wing calculations done in real time, instead of countless hours of run time; digital flight simulations computed with six degrees of freedom, and re-entry structure/fluid interactions made possible; and convergence problems on high-resolution global climate models resolved. Limitless compute power would greatly alter the types of science and engineering applications done and approaches taken as compared with those in use today on the 10,240-processor Columbia supercomputer. In the foreseeable future, computer architectures and operating systems will be customized to specific applications for the space agency. Even so, certain problems will exist regardless of the amount of computing power available, and new paradigms are needed to harness vast numbers of processors.

Doug Burger - The End of Silicon: Implications and Predictions for HPC Systems

Moore's Law has persisted longer than many thought possible. Nevertheless, the end for CMOS is in

sight. Before we get there, power, leakage, and reliability challenges will change computer systems substantively. In this talk, I will project how architectures and systems are likely to evolve between the present and the last conventional computer system.

W. Dally - Custom vs. Commodity Processors (and Memory Systems): The Right Hardware Makes Software Easier

W. Dally – Report on NAS Supercomptuing Study

No abstracts provided.

Andre DeHon – Nanowire-Based Computing Systems

Chemists can now construct wires which are a few atoms in diameter; these wires can be selectively field-effect gated, and wire crossings can act as programmable diodes. The tiny feature sizes offer a path to economically scale to atomic dimensions. However, the associated bottom-up synthesis techniques only produce highly regular structures and have high defect rates and minimal assembly control. We develop architectures to bridge between lithographic and atomic-scale dimensions and tolerate defective and stochastic assembly. Using 10nm pitch nanowires, these nanowire-based programmable architectures offer one to two orders of magnitude greater mapped-logic density than defect-free lithographic FPGAs at 22nm.

Michael Frank - The Reversible Computing Question: A Crucial Challenge for Computing

The computing world is rapidly approaching a power-performance crisis. Over the course of the next few decades, all the usual tricks and techniques for improving computer energy efficiency will, one by one, approach fixed limits. As this happens, the performance that can be maintained per watt consumed (and ops performed per dollar spent, barring cheaper energy) will gradually flatten out, and stay flat for ever!

For, as von Neumann first pointed out in 1949, fundamental thermodynamics imposes a strict limit on the energy efficiency of conventional "irreversible" binary operations, and conventional algorithms for a given task will always require some minimum number of these.

However, this crisis might be avoided, and computer energy efficiency might resume an indefinite upward climb, if only we can practically implement an unconventional approach known as "reversible computing," which avoids using irreversible operations. Instead, in a high-performance "ballistic" reversible computer, the physical and logical state of its circuits essentially "coasts" along the desired trajectory through the machine's configuration space, like a roller coaster along its track, with an energy dissipation that, in theory, can approach arbitrarily close to zero as the technology is further refined.

Unfortunately, the question of whether reversible computing can be made to work efficiently in practice remains open at this time. Various theoretical models and "proof of concept" prototypes of reversible machines exist, but can all be criticized as either too inefficient or too incomplete to be convincing. On the other hand, all of the many attempts by skeptics to prove reversible computing impossible (or permanently impractical) have also been invalid or incomplete, often relying on demonstrably incorrect assumptions about how a computer must work.

The reversible computing question is very deep and important, and it deserves increased attention. But it is also extremely subtle, and quite difficult to resolve. In this talk, I review the major results and open issues in the field, and propose what we must do in order to make progress towards answering this crucial question, and possibly opening the door to a future of unbounded improvements in computer energy

efficiency.

Ed Fredkin – What Else Can Physics Do for Us?

It would be nice if the interplay between new computation technologies and the laws of physics could bring real progress. Quantum computing, so far, has been interesting physics with no resulting computation. Further, the range of applicability of QC, if it ever becomes practical, may be limited to a tiny slice of the universe of tomorrow's computational workload. It is interesting to raise the question: "What else can physics offer with respect to real world computational problems?" The answers aren't clear but there are new insights and possibilities. We should understand that QC is not the only way to bend the basic physical properties of matter and energy to the task of general computation. We will report on physics based concepts that result in conventional computational structures; differing only by having speed and capacity that leapfrog Moore's Law.

Guang Gao – A glimpse on Cyclops-64 system software design - What challenges we may be facing when scaling up to manage a zetta-scale computer ?

In this talk, we report our experience in the design and development of system software for the IBM Cyclops-64 supercomputer architecture that employs a unique multiprocessor-on-a-chip design with a very large number of hardware thread units and embedded memory. In particular, we present a thread virtual machine, called TNT (or TiNy-Threads) as the cornerstone of the C64 system software targeted to managing one million hardware threads. We highlight how to achieve efficiency by mapping (and matching) the TNT thread model directly to the Cyclops ISA features assisted by a native TNT thread runtime library. Based on our experience in this process, we discuss the challenges when scaling up to manage a exa/zetta-scale supercomputer where billions (or even trillions) of hardware threads need to be programmed and managed.

William Gropp – How to Replace MPI as the Programming Model of the Future

There are now legacy MPI codes that future architectures and systems will need to support, either directly through a high-quality MPI implementation or with advanced code transformation aids. Why has MPI been so successful? What properties must any replacement have? This talk will look at some of the reasons (other than portability) for MPI's success and what lessons they provide for current challengers, such as the PGAS languages. The interaction of system architecture and hardware support for programming models and for algorithms will also be discussed, with particular emphasis on the importance of balanced performance features on programming models and algorithms for high end computing.

Bruce Hendrickson – Parallel Graph Algorithms: Architectural Demands of Pathological Applications

Many important applications of high performance computing involve frequent, unstructured memory accesses. Among these applications are graph algorithms which arise in a wide range of important applications including linear algebra, biology and informatics. Graph operations often involve following sequences of edges, which requires minimal computation but frequent accesses to unpredictable locations in global memory. These characteristics result in poor performance on traditional microprocessors, and even worse performance on common parallel computers.

In recent work, we have explored the performance of graph algorithms on the massively multithreaded Cray MTA-2.

The MTA's latency tolerance and fine-grained synchronization mechanisms allow for high performance of single processor and parallel graph algorithms. We will present these results and discuss their lessons for

future developments in computer architecture.

Joint work with Jon Berry, Richard Murphy and Keith Underwood.

Steve Jardin - Towards Comprehensive Simulation of Fusion Plasmas

In Magnetic Fusion Energy (MFE) experiments, high-temperature (100 million degrees centigrade) plasmas are produced in the laboratory in order to create the conditions where hydrogen isotopes (deuterium and tritium) can undergo nuclear fusion and release energy (the same process that fuels our sun). Devices called tokamaks and stellarators are "magnetic bottles" that confine the hot plasma away from material walls, allowing fusion to occur. Confining the ultra-hot plasma is a daunting technical challenge. The level of micro-turbulence in the plasma determines the amount of time it takes for the plasma to "leak out" of the confinement region. Also, global stability considerations limit the amount of plasma a given magnetic configuration can confine and thus determines the maximum fusion rate and power output. Present capability is such that we can apply our most complete computational models to realistically simulate both nonlinear macroscopic stability and microscopic turbulent transport in the smaller fusion experiments that exist today, at least for short times. Anticipated increases in both hardware and algorithms during the next 5-10+ years will enable application of even more advanced models to the largest present-day experiments and to the proposed burning plasma experiments such as the International Thermonuclear Experimental Reactor (ITER). The present thrust in computational plasma science is to merge together the now separate macroscopic and microscopic models, and to extend the physical realism of these by the inclusion of detailed models of such phenomena as RF heating and atomic and molecular physical processes (important in plasma-material interactions), so as to provide a true integrated computational model of a fusion experiment. This is the goal of a new initiative known as the Fusion Simulation Project. Such an integrated modeling capability will greatly facilitate the process whereby plasma scientists develop understanding and insights into these amazingly complex systems that will be critical in realizing the long term goal of creating an environmentally and economically sustainable source of energy.

David Keyes - Drivers from Science and Engineering Applications

Relying on the input of hundreds of members of the U.S. computational science community at the 2003 Science-based Case for Large-scale Simulation (SCaLeS) workshop, the March 2004 whitepapers of Scientific Discovery through Advanced Computing (SciDAC) project of the U.S. DOE, and a collection of recent Gordon Bell Prize finalist papers, we define and motivate some aspirations for high-end science and engineering simulations in the five-year horizon. Looking at some hurdles to progress in high-end simulation, we note in passing that not all are architectural in nature, then concentrate further on those that apparently are. Looking at some kernels of high-end simulation, we note apparent hurdles to their scalability and draw inspiration from the flexibility of algorithm designers to get around hurdles that have presented themselves in the past.

Craig S. Lent - Molecular quantum-dot cellular automata and the limits of binary switch scaling

Molecular quantum-dot cellular automata (QCA) is an approach to electronic computing at the single-molecule level which encodes binary information using the molecular charge configuration. This approach differs fundamentally from efforts to reproduce conventional transistors and wires using molecules. A QCA molecular cell has multiple redox centers which act as quantum dots. The arrangement of mobile charge among these dots represents the bit. The interaction from one molecule to the next is through the Coulomb coupling—no charge flows from cell to cell. Prototype single-electron QCA devices have been built using small metal dots and tunnel junctions. Logic gates and shift registers have been demonstrated, though at

cryogenic temperatures. Molecular QCA would work at room temperature. Molecular implementations have been explored and the basic switching mechanism confirmed. Clocked control of QCA device arrays is possible and requires creative rethinking of computer architecture paradigms. By not using molecules as current switches, the QCA paradigm may offer a solution to the fundamental problem of excess heat dissipation in computation.

Jeff Nichols - National Leadership Computing Facility - Bringing Capability Computing to Science

The National Center for Computational Sciences (NCCS) maintains and operates a user facility to develop and deploy leadership-computing systems with the goal of providing computational capability that is at least 100 times greater than what is generally available for advanced scientific and engineering problems. We work with industry, laboratories, and academia to deploy a computational environment that enables the scientific community to exploit this extraordinary capability, achieving substantially higher effective performance than is available elsewhere. A non-traditional access and support model has been proposed in order to achieve a high level of scientific productivity and address challenges in climate, fusion, astrophysics, nanoscience, chemistry, biology, combustion, accelerator physics, engineering, and other science disciplines. The NCCS brings together world-class researchers; a proven, aggressive, and sustainable hardware path; an experienced operational team; a strategy for delivering true capability computing; and modern computing facilities connected to the national infrastructure through state-of-the-art networking to deliver breakthrough science. Combining these resources and building on expertise and resources of the partnership, the NCCS enables scientific computation and breakthrough science at an unprecedented scale.

Michael Niemier - What can 'baseline' QCA do?

Whether or not the end of the CMOS curve does indeed come to pass, speculation – combined with other technological advances – have helped to fuel a wealth of research related to alternative means of computation. Much of this work has either focused on the lowest levels of device physics or, at best, very simple circuits. But most importantly, it has often led to a publication that discusses the demonstration and performance of a single device. While this is an undeniably important and necessary first step, we must ultimately consider how "Device X" will be used to form a computational system, as well as the fact that we will need many Device X's to do so – not just one. Given the increasing number of proposed novel devices, we should explicitly consider both of the above issues beginning in the initial stages of a device's development – even before the first paper demonstrating Device X is published.

However, by involving computer architects during device development, we will not just be looking at a single device in isolation – rather, we will be evaluating a reasonably sized system with an initial computational goal in mind. Moreover, by assuming a set of very pessimistic implementation constraints, we can establish a true baseline for Device X – defining our best-foreseen application in the worst-foreseen operational environment. If expectations (i.e. with regard to power, area, speed, etc.) for end-of-the-roadmap silicon and other emergent devices – for the same application – are plotted simultaneously, we can make significant headway into discovering what niche roles Device X can realistically play in computing.

What has been done and, in the speaker's opinion, what needs to be done will be discussed in the context of Quantum-dot Cellular Automata (QCA).

Mark Oskin - Engineering a Quantum Computer: Bridging the Theoretical and Practical Divide

Theoretically, quantum computers offer great promise to solve formally intractable problems. Experimentally, small-scale quantum computers have been demonstrated. The next phase of research is to

construct large-scale quantum computers capable of proving the technology and further validating the theoretical foundations. Such devices will consist of 10's to 100's of quantum bits. At this scale, proper engineering of the devices becomes critical.

This talk will present a broad overview of our work in exploring the engineering challenges and design trade-offs involved with large-scale quantum systems. We have found that noise will significantly constrain scalability and that the micro-architecture of these devices needs to be tuned to minimize decoherence. This talk will conclude by sketching future work to be done in this area.

Arnold H. Silver – Superconductor Single Flux Quantum Computing Technologies

Single flux quantum (SFQ) digital electronics is a near-term candidate for very high performance computation. It offers much faster clock rates than CMOS, thereby reducing the number of processors and parallelism required for a given level of computation. A small number (4 - 10K) of SFQ processors operating at clock frequencies from 50 to 100 GHz could produce a computing engine that exceeds petaFLOPs capability within ~ 1-m3 package at an affordable power, including the 4 Kelvin refrigeration. The HTMT architecture study projected 4K RSFQ processors as high-speed computing engines for a petaFLOPs machine. In order to capitalize on SFQ technology, we need to resolve hardware issues and make a significant investment to create an industrial-level infrastructure that supports SFQ electronics:

- A wafer manufacturing line with lithographic and other tools close to CMOS capability
- Fast, dense cryogenic RAM
- Wideband I/O between the cryogenic and room temperature platforms
- A source of MCMs that are capable of sustaining 50+ GHz data transfer.

Additionally, we need to address the microarchitecture issues that arise from very fast clocks and consequently short distances accessible within a clock period. This is not an SFQ issue; it is a fast clock issue.

SFQ chips are not off-the-shelf parts; we need mature chip design and manufacturing capabilities. A few organizations have been making significant progress with SFQ technology for small-scale digital and mixed signal applications on very small budgets. For example, Northrop Grumman developed an 8-bit μprocessor demonstration at the 60K junction, 5K-gate, 20 GHz clock level. It is not possible to produce ≥ Mgate processors with the existing infrastructure.

There are attractive candidates that promise to fill the cryogenic RAM void.

Wideband I/O issue is an engineering trade-off between conflicting electrical and thermal requirements.

A unique need is for a cost-effective source of complex MCMs that can deliver 50 GHz serial data transfer rate.

Future engineering improvements that bring SFQ chip design and manufacturing capability in line with CMOS at 90 nm could produce Mega-gate chips at clock rates about 200 GHz. This could enable > 100 X increase in computing power. Development of advanced cryogenic RAM, such as hybrid SFQ-MRAM, would complement the cryogenic processor.

SFQ technology (including RSFQ, or Rapid SFQ) is a recent cryogenic electronics technology based on the generation, storage, and transmission of identical picosecond pulses. Each pulse represents one magnetic flux quantum,

$$\Phi_0 \equiv h/2e \cong 2 \text{ millivolt-picosecond.}$$

SFQ pulses are localized and stored in small, integrated inductors. The millivolt energy and picosecond times associated with the flux quantum enables digital computation at very high speed (approaching 1,000 GHz) and simultaneously at very low power (~nW/GHz/gate). Practical SFQ electronics is an IC technology based on superconducting Nb thin films and thin film Josephson tunnel junctions that operate at ≤ 4.5 to 5 Kelvin. SFQ chips are fabricated on standard Si wafers using tools similar to semiconductor fabrication. SFQ fabrication requires only metal/dielectric film depositions and lithographic etching, no

diffusion or epitaxial growth.

Thomas Sterling - Continuum Computer Architecture for Nano-scale Technologies

As the feature size of logic devices decreases with Moore's Law ultimately achieving the domain of nano-scale technology, the ratio of 'remote' versus 'local' action will escalate dramatically demanding entirely new computing models and structures to efficiently exploit these future technologies and lead to Exaflops capability and beyond. Continuum Computer Architecture (CCA) is a new family of parallel computer architectures under development at LSU to harness convergent device technologies beyond Moore's Law that respond to the challenges implied by the emerging disparity between local and global operations. CCA provides one possible framework for employing nano-scale technology for future convergent system architectures at the end of Moore's Law. CCA is a cellular architecture merging data storage, logical manipulation, and nearest neighbor transfers in a single simple element or cell. In physical structure, CCA is reminiscent of cellular automata. But logically, CCA is very different. It supports a general global parallel model of computation through the management of a distributed virtual name space for both data and parallel continuations which are data structures that dynamically and adaptively govern fine grain parallel execution. The semantics of the CCA system borrows from the ParalleX model of computation that combines message driven computing, multi-threading, and the futures synchronization construct to replace the venerable and conventional barrier controlled communicating sequential processes. This presentation will describe ParalleX and its potential implementation through Continuum Computer Architecture with nano-scale technology for Exaflops and beyond.

Tom Theis - Devices for Computing: Present Problems and Future Solutions

The biggest problems limiting the further development of the silicon field-effect-transistor are power dissipation and device-to-device variability. Despite some pessimistic predictions, it looks like the technology can be extended for at least another 10 years. Research into transistors based on carbon nanotubes or semiconductor nanowires can be viewed as a quest for the "ultimate" field-effect-transistor. Looking beyond the field-effect transistor, major US Semiconductor manufacturers have recently announced the Nanoelectronics Research Initiative (NRI) which will fund university research aimed at entirely new logical switches. Beyond the stated research goals of NRI, I will briefly survey the prospects for devices that efficiently implement reversible logic and quantum logic.

Colin P. Williams - Quantum Simulation

While it is widely known that quantum computers can factor composite integers and compute discrete logarithms in polynomial time, other applications of quantum computers have not been publicized as well. In this talk I will discuss some of the ways quantum computers could be used in scientific computation, especially in simulation, quantum chemistry, signal processing, and solving differential equations. Such applications of quantum computers have the potential to have greater scientific and commercial impact than those related to factoring and code-breaking.

Stan Williams - Manufacturability and Computability at the nano-Scale

Nano-Scale electronics offer the possibility to build much higher density circuits than those that are presently available, but there are major issues to resolve before they become a reality. A significant issue is the cost of manufacturing, which will lead to new fabrication technologies and geometrically simpler circuit designs. A second is that at some scale, the physics of the field-effect transistor will not longer operate, and new devices enabled by quantum effects will be needed. I will review our latest developments in the areas of nano-imprint lithography, switching devices, and crossbar architectures.

Peter Zeitzoff – ITRS MOSFET Scaling Trends, Challenges, and Key Technology Innovations

This presentation will focus on the scaling trends for MOSFETs as projected by the International Technology Roadmap for Semiconductors (ITRS), as well as the important challenges and the main technology innovations that are expected. The ITRS projects that CMOS transistors will scale through 2020, with gate length of well under 10 nm expected by then and the transistor intrinsic speed increasing at a consistent rate of 17% per year, which matches the historical rate. Important scaling challenges include rapidly increasing gate leakage current, increasing impact of depletion in the polysilicon gate electrode, and significant difficulties with scaling the current standard planar bulk MOSFETs. Also included is the challenge of gaining adequate control of short channel effects and transistor subthreshold leakage current while sharply increasing the transistor saturation drive current as the MOSFET is scaled. Key technology innovations that are aimed at dealing with the challenges include high-k gate dielectrics and metal gate electrodes, enhanced MOSFET mobility, and the eventual implementation of advanced CMOS transistors: ultra-thin body fully depleted silicon-on-insulator (SOI) and multiple-gate MOSFETs (an example of the latter is the FinFET).

Working Groups

The goal of the working groups will be to contribute to the first long-term roadmap for the future of high performance computing from the near-term range of Petaflops-scale through to the asymptotic realm of extreme computing beyond an Exaflops as determined by the capabilities and limitations of future enabling technologies in order to identify critical research directions for continued growth in sustained performance for future applications and to determine the ultimate bounds on real world problems.

The organizers recommend the following process for working groups – although the organizers recognize that spontaneity is often a hallmark of originality and the working groups may something else altogether. Organizers recommend that during the meeting times Monday-Wednesday 3:30-6 pm and Thursday morning, the group leader and participants organize the ideas and resources presented by workshop participants, including any debate among participants (that will become difficult after people leave the workshop). There will be a two-fold objective: (1) To prepare viewgraphs for an out brief on Thursday morning. The out brief sessions will be on 30 minute intervals, and are expected to comprise 10-20 minutes of viewgraph presentation with the remainder of time in a "panel" session. (2) There is advanced planning for the output of the workshop to be put into a written form. In support of this second phase, the working groups should prepare and turn over supporting materials to the people who will carry out this subsequent work.

Working Group 1: Is There a Gap Between COTS and Post-Transistor Computing?

We have pursued over a decade of architectures based on the premise of building scalable architectures based on inexpensive Commodity Off The Shelf (COTS) microprocessors that were driven by the intensity of the desktop market.

Now, due to various trends (exposed in the workshop), variables in that COTS desktop market equation are changing (rise of gaming processors, general purpose CPUs going multi-core, slow down in the increase of clock rates, and Instruction Level Parallelism (ILP), etc.), thus calling that strategy into question for the next decade. The question becomes what progress can we make on re-visiting this notion of custom cores and will the investment time (to create the scalable architectures) take so long that the end result gets eclipsed by progress in nano, quantum, superconducting?

Group Leader: Candy Culhane

Working Group 2: Adaptations of Software and Algorithms needed to Accommodate Emerging Hardware

Even though it is difficult to program hardware that doesn't exist, physics is behind certain common trends that can be analyzed in general. Some of the clearest trends are (1) hardware will achieve increased performance mainly through increased parallelism and (2) latency of both memory accesses and inter-processor communications will become more significant. These trends alone suggest advancing hardware will quickly exhaust parallelism and "locality" in existing algorithms. This group will ask when this issue will become a critical issue and how its consequences can be mitigated.

Group Leader: Bill Gropp

Working Group 3: Post Transistor Technologies

Nano-scale technology of the future will permit the definition, design, and fabrication of logic devices at near atomic scale that will yield component densities unlikely to be exceeded due to quantum limitations. Technologies like RSFQ logic exploit superconductivity to deliver unprecedented switching rates (100s of GHz) at low power. Such innovations in asymptotic technologies will achieve ultimate capabilities from physical devices still operating within the domain of Boolean logic. Beyond the domain of Boolean logic lie other technologies that are a part of the overall agenda (i. e. reversible and quantum). This group will determine the level of performance that may be achieved within this technology realm, the computational structures and architectures that may be required and employed to exploit it, and the applications that may be enabled by it.

Group Leader: Baron Mills

List of Participants (Oct. 21, 2005)

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Program At A Glance

Day	Monday General Methods	Tuesday Specific Methods	Wednesday Future Methods	Thursday Report
8:15 am	Registration			
9:00 am	Workshop Introduction, Overview, and Goals, E. DeBenedictis, Sandia	Drivers from Science and Engineering Applications, D. Keyes, Columbia Un.	Custom vs. Commodity Processors and Memory, W. Dally, Stanford	WG Session 4: Develop report
9:30 am	Applications Keynote: Simulating the Earth's Environment, D. Bader, LLNL	Simulating Plasma Fusion, S. Jardin, PPPL	A glimpse at Cyclops-64 system software design, G. Gao, U. Delaware	
10:00 am	Technology Keynote: Quantum Computing – its Promise and Limitations, CH Bennett, IBM	NAS Supercomputing Report, W. Dally, Stanford	How to Replace MPI as the Programming Model of the Future, W. Gropp, ANL	
10:30 am	Break	Break	Break	Break
11:00 am	The ITRS MOSFET Scaling Trends, Challenges, and Key Technology Innovations, P. Zeitzoff, Sematech	Manufacturability and Computability at the Nano-Scale, S. Williams, HP	Problems Soluable with Graph Algorithms, B. Hendrickson, Sandia	WG 1 Report
11:30 am	The End of Silicon: Implications and Predictions for HPC Systems, D. Burger, UT Austin	Nanowire-based Computing Systems, A. DeHon, Caltech	Space Applications, R. Biswas, NASA	WG 2 Report
Noon	Superconducting Technologies, A. Silver	Future Technologies, T. Theis, IBM	National Leadership Computing Facility, J. Nichols, ORNL	WG 3 Report & closing remarks
12:30 pm	Lunch	Lunch	Lunch	Lunch
1:30 pm	Reversible Computing, Mike Frank, FSU	QDCA Hardware, C. Lent, Notre Dame	Programmatic Perspectives on Quantum Computing, M. Foster, NSF	
2:00 pm	Continuum Computer Architecture, T. Sterling, LSU	QDCA Systems, M. Neimier, Ga Tech	Architecture of a Quantum Computer, M. Oskin, U. Washington	
2:30 pm	Charter to the Working Groups	Reserved	Quantum Simulation, C. Williams, JPL	
3:00 pm	Break	Break	Break	
3:30 pm	WG Session 1	WG Session 2	WG Session 3	
6:30 pm	Dinner	Dinner	Dinner	
7:00 pm		Banquet Speech: What Else can Physics Do for Us, E. Fredkin, CMU		
7:45 pm	Social	Social	Social	