
# CoreExpress®
# SPECIFICATION

## Revision 2.1

## February 23, 2010

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Please send comments via electronic mail to info@sff-sig.org.

## Revision History

| Revision | Issue Date | Comments |
|---|---|---|
| 2.1 | 2/23/10 | Initial Release |

# Table of Contents

# 1.0 Introduction

## 1.1 Purpose

This document defines the CoreExpress® standard for Computer On Modules, based on new chip architectures from chip suppliers introducing small and powerful solutions combined with less thermal design power.

CoreExpress® is a modular design, which is able to handle the technological advancements and serves as a base for new and future embedded PC applications. With a focus on the future all legacy interfaces and functions have been eliminated. The analog interfaces and circuit traces have been removed from the CoreExpress® module to avoid signal interference between digital and analog elements interspersed on the same module. Components have been and will be selected with guaranteed availability for seven years or more. Industrial applications may typically run pretty much unchanged for even longer periods of time. They may be upgraded or expanded from time to time with the same or compatible qualified products.

A CoreExpress® module does not handle legacy I/O. These functions can be implemented easily on the carrier board using USB bridges, if required. There are no analog signals on CoreExpress® modules. The purely digital concept gives the user maximum flexibility when selecting component for the required interfaces. Problems of signal level attenuation and similar analog issues are avoided with this 'digital only' concept.

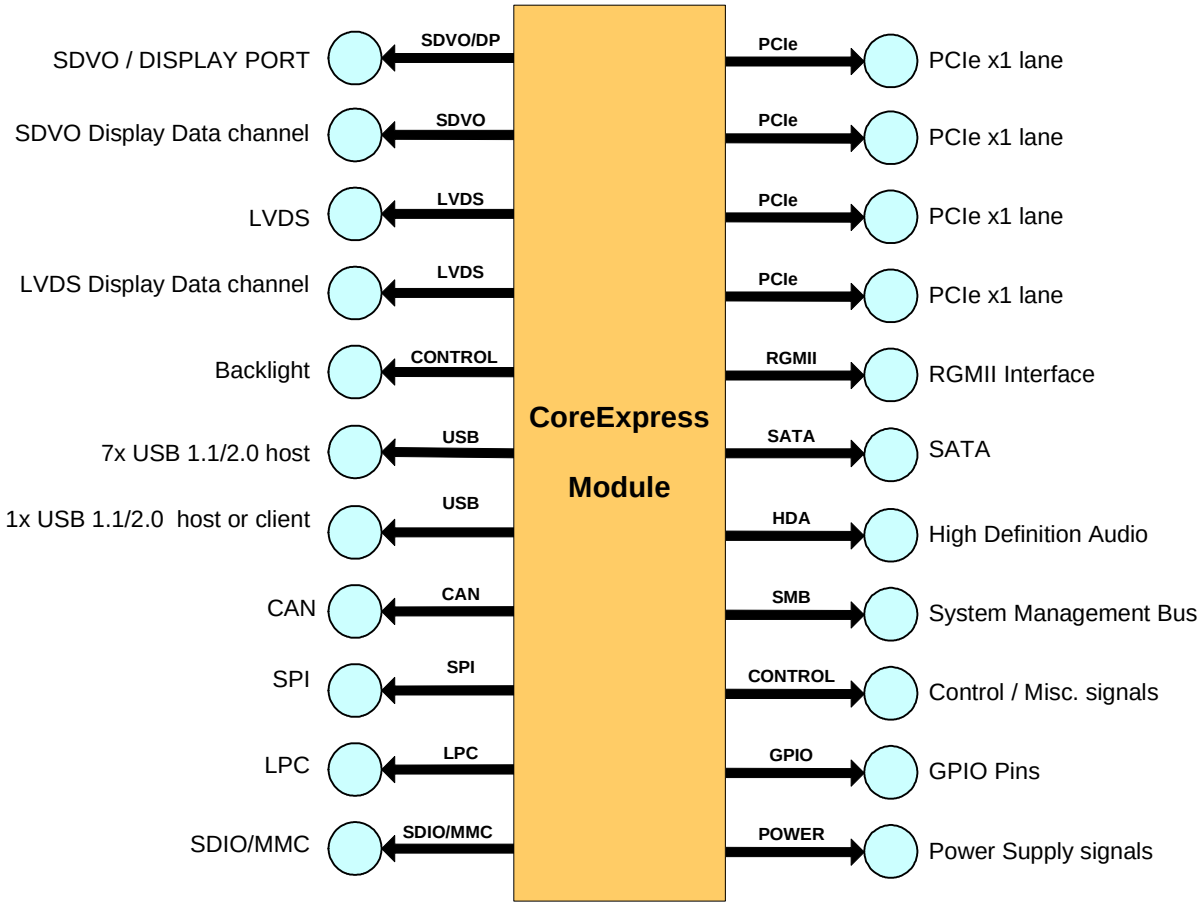
The CoreExpress® standard should not be restricted to any existing available chipset / CPU platform. Future Small Form Factor (SFF) chipsets, which are suitable for industrial, medical or military applications can also be used. The CoreExpress® design is flexible enough to support such embedded PC platforms.

## 1.2 Description

The CoreExpress® format is poised to take advantage of new processors and chipsets. The small thermal design power of these chips allows very dense designs requiring minimal cooling. Additional CoreExpress® is designed to combine EMC protection with a cooling solution.

CoreExpress® modules are processor-independent entire plug-in processing units and come complete with memory, graphics and communication interfaces on a small module size of 65 mm x 58 mm. A 220 pin connector brings these interface signals to an application specific carrier board. Because all of the CPU complexity is handled on the CoreExpress® module, the carrier board can be designed using a low-complexity printed circuit board that can be built very economically. This results in short time-to-market and very attractive pricing for the whole problem solution.

**Block diagram:**




CoreExpress® defines all the following standard interfaces on the connector:

- 4 x PCI-Express x1 lanes, can be combined as one PCI-Express x 4 lane
- RGMII (Reduced Gigabit Media) Ethernet Interface
- 2 x SATA ports
- 1 x CAN interface
- 8 x USB 2.0 ports
- one USB port can work as USB client
- Low Pin Count Bus (LPC Bus)
- System Management Bus (SMBus)
- High Definition Audio Interface
- SDVO port or DISPLAY PORT
- 24 Bit LVDS for displays

- backlight control signals
- Display Data channels for SDVO, LVDS
- SD/SDIO/MMC 8 Bit interface
- Miscellaneous signals
- 8 reserved pins for future use

## 1.3 Minimum Feature Set

Not all interfaces need to be supported by the module. Please refer to the modules documentation, which interfaces are actually supported. The following table shows minimum / maximum number of each interface that shall be supplied by the module.

| Interface | Minimum | Maximum |
|---|---|---|
| PCI Express lanes | 1 | 4 |
| RGMII Interface | 0 | 1 |
| SATA ports | 0 | 2 |
| SDVO interface / DISPLAY PORT interface | 0 | 1 |
| LVDS interface | 1 | 1 |
| USB ports (including 1 client port) | 2 | 8 |
| CAN interface | 0 | 1 |
| SPI interface | 0 | 1 |
| LPC interface | 1 | 1 |
| SDIO interface | 0 | 1 |
| GPIO pins | 0 | 4 |
| SMB interface | 1 | 1 |
| HDA interface | 1 | 1 |

## 1.4 Connector

A surface mount, fine pitch stacking Board-to-Board connector receptacle with 220 pins in two rows from Tyco's High Speed Interface line, part number Tyco 3-6318490-6, is used as the module connector.

Different stacking height is possible by using different mating connector plugs. Two different heights are available:

5.00 mm stacking height: Tyco 3-1827253-6 or equivalent

8.00 mm stacking height: Tyco 3-6318491-6 or equivalent

## 1.5 Module Interoperability

To ensure module interoperability all modules should pass a interface compliance test to guarantee a possible exchange of modules with the same feature set from different vendors. Depending on the usage of different CPU/chipsets on modules from different vendors software changes might also be necessary if a module should be exchanged by another.

## 1.6 Related Documentation and Organizations

**CoreExpress®** Specification

Small Form Factor Special Interest Group
2784 Homestead Road #269
Santa Clara, CA 95051 USA
Phone: +1-650-961-2473
http://www.SFF-SIG.org

**PCI-Express**

PCI Express Specification, Revision 1.1

PCI-SIG
3855 SW 153rd Drive
Beaverton, OR 97006 USA
Phone: +1-503-619-0569
http://www.pcisig.com/specifications/pciexpress/

**GLCI/LCI/SDVO/SPI/SDIO**

Datasheets of various Intel Chipsets

http://www.intel.com

**LVDS**

Low Voltage Differential Signaling (LVDS) Interface
http://www.interfacebus.com/Design_Connector_LVDS.html

**SATA**

Serial ATA international organization

www.serialata.org

**USB**

Universal Serial Bus (USB) connects computers, peripherals and more
USB Implementers Forum, Inc.
3855 SW 153rd Drive
Beaverton, OR 97006
http://www.usb.org

**HDA**

High Definition Audio specification http://www.intel.com/standards/hdaudio

**LPC**

Low Pin Count specification

Intel Corporation
Santa Clara, CA USA
http://www.intel.com/design/chipsets/industry/lpc.htm

**SMB**

System Management Bus (SMBus)

System Management Interface Forum, Inc.
100 N. Central Expressway
Suite 600
Richardson, Texas 75080-5323 USA
Fax: +1-972-238-1286
http://www.smbus.org

**ACPI**

Advanced Configuration and Power Interface Specification (ACPI), Revision 3.0

http://www.acpi.info/spec.htm

**CAN**

Controller Area Network specification

http://www.can-cia.org

**Connector**

http://catalog.tycoelectronics.com/TE/bin/TE.Connect?C=1&M=BYPN&PID=425175&PN=3-6318490-6&I=13

# 2.0 Module Connector

## 2.1 Signal Naming Convention

The signals on the connector are named so that signal groupings are obvious. The fields in a signal name go from general to specific, e.g. the PCI Express signals start with the characters “PCIE,” followed by “TX”, “RX”, or “CLK” for Transmit, Receive, or Clock respectively. Next is the lane number in alphabetic order. Last is “p” or “n” for the positive and negative signal in the differential pair.

A signal on the connector is designated “transmit” or “receive” in a Host-centric manner. The “transmit” pin on the Host connects to the “T” (transmit) pin of the connector. From there, the signal connects to “receive” pin of the Device. In a PCI Express system the transmit pins of the chip are always connected to the receive pins of the other chip in the link, and vice-versa. For example, for a specific link, transmit on the Host chip is connected to receive on the Device chip, and receive on the Host is connected. Other non-PCI Express signals follow a similar convention.

All signal names ending with a hash sign '#' indicate a low active signal.

## 2.2 Signal Description

**Power and Ground Signal Pins:**

The board is powered by applying 5 volt at all these pins

**+5V0:** 5 volt power supply pins

**GND:** GND power supply pins

**+5V-Always:** 5 volt power supply pin for sleep state

***Note:*** Use and functionality of +5V-Always is depending on the module. Please refer to the technical manual of the module

**External Battery:**

An external battery (3.0 V … 3.6 V) should be connected to the CoreExpress® connector pin BAT_IN. It can be used to supply a real time clock and buffering CMOS data.

**PCI-Express Lanes:**

There are up to four PCI Express root ports available on the CoreExpress® connector. The PCI Express signals are compatible with PCI Express 1.0a Signaling Environment AC Specifications.

The following PCI Express signals are located on the CoreExpress® connector:

**PCIE_TXAn, PCIE_TXAp,**
**PCIE_TXBn, PCIE_TXBp**
**PCIE_TXCn, PCIE_TXCp,**
**PCIE_TXDn, PCIE_TXDp**

**Type:** differential output, AC coupled

PCI Express Transmit: PCIE_TX[A:B] are PCI Express ports A:B transmit pair (P and N) signals. The serial capacitors are included on the module.

**PCIE_RXAn, PCIE_RXAp,**
**PCIE_RXBn, PCIE_RXBp**
**PCIE_RXCn, PCIE_RXCp,**
**PCIE_RXDn, PCIE_RXDp,**

**Type:** differential input, AC coupled

PCI Express Receive: PCIE_RX[A:B] PCI Express ports A:B receive pair (P and N) signals. The serial capacitors must be placed on the baseboard at the PCI Express device.

**PCIE_CLKAn, PCIE_CLKAp,**
**PCIE_CLKBn, PCIE_CLKBp,**
**PCIE_CLKCn, PCIE_CLKCp,**
**PCIE_CLKDn, PCIE_CLKDp, ,**

**Type:** differential output, 3.3 volt

PCI Express Clock: 100MHz differential clock signals.

**PCIE_CLKREQA#,**
**PCIE_CLKREQB#,**
**PCIE_CLKREQC#,**

**PCIE_CLKREQD#,**

**Type:** Input, 3.3 volt, internal Pull-Up

PCI Express Clock Request: Output enable for PCIexpress clocks

***Note*** The four PCI Express x1 lanes A to D can be combined together to build one PCI Express x 4 lane.

**RGMII Ethernet:**

The RGMII is intended to be an alternative to the IEEE802.3u MII, the IEEE802.3z GMII and the TBI. The principle objective is to reduce the number of pins required to interconnect the MAC and the PHY from a maximum of 28 pins (TBI) to 12 pins in a cost effective and technology independent manner. In order to accomplish this objective, the data paths and all associated control signals will be reduced and control signals will be multiplexed together and both edges of the clock will be used. For Gigabit operation, the clocks will operate at 125MHz, and for 10/100 operation, the clocks will operate at 2.5MHz or 25MHz respectively.

The RGMII signals (including MDIO/MDC) will be based upon 2.5v CMOS interface voltages as defined by JEDEC EIA/JESD8-5.

**RGMII_TD[3:0]**

**Type:** output

Transmit Data: The LAN controller uses these signals to transfer data to the PHY.

**RGMII_TXC**

**Type:** output

Transmit reference clock: will be 125MHz, 25MHz, or 2.5MHz +- 50ppm depending on speed.

**RGMII_TXCTL**

**Type:** output

Transmit control signal to the PHY.

**RGMII_RD[3:0]**

**Type:** input

Received Data: The LAN controller uses these signals to receive data from the PHY.

**RGMII_RXC**

**Type:** input

The continuous receive reference clock will be 125MHz, 25MHz, or 2.5MHz +- 50ppm. and shall be derived from the received data stream

**RGMII_RXCTL**

**Type:** input

Receive control signal from the PHY.

**RGMII Management Interface**

**RGMII_MDC**

**Type:** input

Management Data Clock

**RGMII_MDIO**

**Type:** input/output

Input / Output of Management Data

## SDVO / DISPLAY PORT:

SDVO and DISPLAY PORT signals are shared on same pins, only one type of interface is supported by the module. Please refer to the specific module specification which interface is supported.

All SDVO and DISPLAY PORT signals are AC-coupled. The serial capacitors are included on the module.

The following SDVO signals are located on the CoreExpress® connector:

**SDVO_RED, SDVO_RED#**

**Type:** differential output, AC coupled

Serial Digital Video Channel Red: SDVO_RED is a differential data pair that provides red pixel data for the SDVO channel during active periods. During

blanking periods it may provide additional such as sync information, auxiliary configuration data, etc. This data pair must be sampled with respect to the SDVO_CLK signal pair.

**SDVO_GREEN, SDVO_GREEN#**

**Type:** differential output, AC coupled

Serial Digital Video Channel Green: SDVO_GREEN is a differential data pair that provides green pixel data for the SDVO channel during active periods. During blanking periods it may provide additional such as sync information, auxiliary configuration data, etc. This data pair must be sampled with respect to the SDVO_CLK signal pair.

**SDVO_BLUE, SDVO_BLUE#**

**Type:** differential output, AC coupled

Serial Digital Video Channel Blue: SDVO_BLUE is a differential data pair that provides blue pixel data for the SDVO channel during active periods. During blanking periods it may provide additional such as sync information, auxiliary configuration data, etc. This data pair must be sampled with respect to the SDVO_CLK signal pair.

**SDVO_CLK, SDVO_CLK#**

**Type:** differential output, AC coupled

Serial Digital Video Channel Clock: This differential clock signal pair is generated by the System controller Hub internal PLL and runs between 100MHz and 200MHz. If TV-out mode is used, the SDVO_TVCLKIN clock input is used as the frequency reference for the PLL. The SDVO_CLK output pair is then driven back to the SDVO device.

**SDVO_INT, SDVO_INT#**

**Type:** differential input, AC coupled

Serial Digital Video Input Interrupt: Differential input pair that may be used as an interrupt notification from the SDVO device to the System Controller Hub. This signal pair can be used to monitor hot plug attach/detach notifications for a monitor driven by an SDVO device.

**SDVO_TVCLKIN, SDVO_TVCLK#**

**Type:** differential input, AC coupled

Serial Digital Video TV-Out Synchronization Clock: Differential clock pair that is driven by the SDVO device to the System Controller Hub. If SDVO_TVCLKIN is used, it becomes the frequency reference for the system controller hub dot clock PLL, but will be driven back to the SDVO device through the SDVO_CLK differential pair. This signal pair has an operating range of 100 —200MHz, so if the desired display frequency is less than 100MHz, the SDVO device must apply a multiplier to get the SDVO_TVCLKIN frequency into the 100- to 200-MHz range.

**SDVO_STALL, SDVO_STALL#**

**Type:** differential input, AC coupled

Serial Digital Video Field Stall: Differential input pair that allows a scaling SDVO device to stall the pixel pipeline.

**SDVO_CTRLCLK**

**Type:** input/output, CMOS 3.3 volt, internal Pull-Up

SDVO Control Clock: Single-ended control clock line to the SDVO device. Similar to $I^2C$ clock functionality, but may run at faster frequencies. SDVO_CTRLCLK is used in conjunction with SDVO_CTRLDATA to transfer device configuration, PROM, and monitor DDC information. This interface directly connects the system controller hub to the SDVO device.

**SDVO_CTRLDATA**

**Type:** input/output, CMOS 3.3 volt, internal Pull Up

SDVO Control Data: SDVO_CTRLDATA is used in conjunction with SDVO_CTRLCLK to transfer device configuration, PROM, and monitor DDC information. This interface directly connects to the SDVO device.

The following DISPLAY PORT signals are located on the CoreExpress® connector:

**DP_LANE0_p, DP_LANE0_n,**
**DP_LANE1_p, DP_LANE1_n,**
**DP_LANE2_p, DP_LANE2_n,**
**DP_LANE3_p, DP_LANE3_n,**
**DP_AUX_p, DP_AUX_n**

**Type:** differential output, AC coupled

Lane signals and Lane complement signals for Display Port 0 to 3 and Aux channel.

**HP_DET**

**Type:** input, CMOS 3.3 volt

Hot Plug Detect Signal: input to generate interrupts.

**LVDS:**

The LVDS data and clock signals are Low Voltage Differential Signal buffers. These signals should drive across a 100-Ohm resistor at the receiver when driving.

The following LVDS signals are located on the CoreExpress® connector:

**LA_DATAp[3:0]**
**LA_DATAn[3:0]**

**Type:** differential output, low voltage

Channel A Differential Data Output: Differential signal pair.

**LA_CLKp**
**LA_CLKn**

**Type:** differential output, low voltage

Channel A Differential Clock Output: Differential signal pair.

**L_DDC_CLK**

**Type:** input/output, CMOS 3.3 volt

Display Data Channel Clock: I2C-based control signal (Clock) for EDID control.

**L_DDC_DATA**

**Type:** input/output, CMOS 3.3 volt

Display Data Channel Data: I2C-based control signal (Data) for EDID control.

**L_CTLB_CLK**

**Type:** input/output, CMOS 3.3 volt

Control B Clock: Can be used to control external clock chip for SSC – optional.

**L_CTLB_DATA**

**Type:** input/output, CMOS 3.3 volt

Control B Data: Can be used to control external clock chip for SSC – optional.

**L_DETECT**

**Type:** input, CMOS 3.3 volt

LCD Detect signal: t.b.d.

**Backlight:**

The following signals for backlight control are located on the CoreExpress® connector:

**L_VDDEN**

**Type:** output, CMOS 3.3 volt

LCD Power Enable: Panel power enable control.

**L_BKLTEN**

**Type:** output, CMOS 3.3 volt

LCD Backlight Enable: Panel backlight enable control.

**L_BKLTCTL**

**Type:** output, CMOS 3.3 volt

LCD Backlight Control: This signal allows control of LCD brightness.

**SATA Ports:**

Up to two SATA ports are supported by the CoreExpress® connector:

**SATA_RXAp, SATA_RXAn,**
**SATA_RXBp, SATA_RXBn,**

**Type:** input, CMOS 3.3 volt

Serial ATA Differential Receive Pair: These are inbound high-speed differential signals from SATA Ports.

**SATA_TXAp, SATA_TXAn,**
**SATA_TXBp, SATA_TXBn,**
**Type:** output, CMOS 3.3 volt

Serial ATA differential transmit pair: These are outbound high-speed differential signals to SATA Ports.

**SATA_LED#**

**Type:** output, CMOS 3.3 volt

This signal is an open-drain output pin driven during SATA command activity. It is to be connected to external circuitry that can provide the current to drive a platform LED. When active, the LED is on. When tri-stated, the LED is off. An external pull-up resistor to 3.3 volt required.

## CAN Port:

**CAN_TX**

**Type:** output, 3.3 volt

CAN Bus: Transmit data signal. Connect to the appropriate TxD of the external driver.

**CAN_RX**

**Type:** input, 3.3 volt

CAN Bus: Receive data signal. Connect to the appropriate RxD of the external driver.

## USB Ports:

All data signals of the eight USB 2.0 ports are located on the on the CoreExpress® connector. They are counted from USB_A to USB_H with their positive (p) and negative (n) Data lines. The port USB_C can also work as USB client. The over-current signals of port A/B, C/D, EF, G/H are wired ORed together on one signal.

**USB_Ap, USB_An, USB_Bp, USB_Bn, USB_CAp, USB_Cn, USB_Dp, USB_Dn**
**USB_Ep, USB_En, USB_Fp, USB_Fn**

**Type:** input/output, CMOS 3.3 volt

USB Port A:F Differentials: Bus Data/Address/Command Bus: These differential pairs are used to transmit data/address/command signals for ports A through F.

**USB_Gp, USB_Gn, USB_Hp, USB_Hn**

**Type:** input/output, CMOS 3.3 volt

USB Port G:H Differentials: Bus Data/Address/Command Bus: These differential pairs are used to transmit data/address/command signals for ports G and H.

**USB_A/B_OC#, USB_C/D_OC#, USB_E/F_OC#, USB_G/H_OC#**

**Type:** input, CMOS 3.3 volt

Over current Indicators: These signals set corresponding bits in the USB controllers to indicate that an over current condition has occurred. NOTE: These signals are not 5 V tolerant.

**USB_C_Device**

**Type:** input/output, CMOS 3.3 volt

USB Client Connect: This signal may be used in systems where USB port C is configured for client mode. This indicates connection to an external USB host has been established.

NOTE: If USB Client support is enabled, then this signal is dedicated for USB Client Connect.

**SDIO Port:**

The following SDIO signals are located on the CoreExpress® connector:

**SD0_DATA[7:0]**

**Type:** output, CMOS 3.3 volt

SDIO Controller 0 Data: These signals operate in push-pull mode. The SD card includes internal pull-up resistors for all data lines. By default, after power-up, only SD0_DATA0 is used for data transfer. Wider data bus widths can be configured for data transfer.

**SD0_CMD**

**Type:** output, CMOS 3.3 volt

SDIO Controller 0 Command: This signal is used for card initialization and transfer of commands. It has two operating modes: open-drain for initialization mode, and push-pull for fast command transfer.

**SD0_CLK**

**Type:** output, CMOS 3.3 volt

SDIO Controller 0: With each cycle of this signal a one-bit transfer on the command and each data line occurs. This signal is generated by System Controller Hub at a maximum frequency of:24 MHz for SD and SDIO, 48 MHz for MMC.

**SD0_WP**

**Type:** input, CMOS 3.3 volt

SDIO Controller 0 Write Protect: These signal denote the state of the write-protect tab on SD cards.

**SD0_CD#**

**Type:** input, CMOS 3.3 volt

SDIO Controller 0 Card Detect: Indicates when a card is present in an external slot.

**SD0_LED**

**Type:** output, CMOS 3.3 volt

SDIO Controller 0 LED: Can be used to drive an external LED and indicate when transfers are occurring on the bus.

**SD0_PWR#**

**Type:** output, CMOS 3.3 volt

SDIO/MMC Power Enable: These pins can be used to enable the power being supplied to an SDIO/MMC device.

## High Definition Audio Interface:

The following audio signals are located on the CoreExpress® connector:

**HDA_RST#**

**Type:** output, CMOS 3.3 volt or 1.8 volt

HD Audio Reset: This signal is the reset for external Codecs

**HDA_SYNC**

**Type:** output, CMOS 3.3 volt or 1.8 volt

HD Audio Sync: This signal is a fixed sample rate sync at 48 KHz to the Codec(s). It is also used to encode the stream number.

**HDA_BITCLK**

**Type:** output, CMOS 3.3 volt or 1.8 volt

HD Audio Clock (Output): This signal is a 24.000-MHz serial data clock generated by the High Definition Audio controller. This signal contains an integrated pull-down resistor so that it does not float when a High Definition Audio CODEC (or no CODEC) is connected.

**HDA_SDATAOUT**

**Type:** output, CMOS 3.3 volt or 1.8 volt

HD Audio Serial Data Out: This signal is a serial TDM data output to the Codec(s). The serial output is double-pumped for a bit rate of 48 MB/s for HD Audio

**HDA_SDATAIN1, HDA_SDATAIN0**

**Type:** input, CMOS 3.3 volt or 1.8 volt

HD Audio Serial Data In: These serial inputs are single-pumped for a bit rate of 24 MB/s. They have integrated pull-down resistors that are always enabled.

**HDA_DOCKEN#**

**Type:** output, CMOS 3.3 volt or 1.8 volt

HD Audio Dock Enable: This active low signal controls the external HD Audio docking isolation logic. When de-asserted, the external docking switch is in isolate mode. When asserted, the external docking switch electrically connects the HD Audio dock signals to the corresponding System Controller Hub signals.

**HDA_DOCKRST#**

**Type:** output, CMOS 3.3 volt or 1.8 volt

HD Audio Dock Reset: This signal is a dedicated reset signal for the codec(s) in the docking station. It works similar to, but independent of, the normal HDA_RST# signal.

**HDA_SPEAKER**

**Type:** output, CMOS 3.3 volt

Speaker: This signal drives an external speaker driver device, which in turn drives the system speaker.

## Low Pin Count Bus:

The following LPC signals are located on the CoreExpress® connector:

**LPC_AD[3:0]**

**Type:** output, CMOS 3.3 volt

LPC Address/Data: Multiplexed Command, Address, Data

**LPC_FRAME#**

**Type:** output, CMOS 3.3 volt

LPC Frame: This signal indicates the start of an LPC/FWH cycle.

**LPC_SERIRQ**

**Type:** input/output, CMOS 3.3 volt

Serial Interrupt Request: This signal conveys the serial interrupt protocol.

**LPC_CLKOUT[2:1]**

**Type:** output, CMOS 3.3 volt

LPC Clock: These signals are the clocks driven to LPC devices. Each clock can support up to two loads.

## SPI Interface:

The following Serial Peripheral Interface signals are located on the CoreExpress® connector:

**SPI_CS#**

**Type:** output, CMOS 3.3 volt

SPI Chip Select 0: Used as the SPI bus request signal.

**SPI_MISO**

**Type:** input, CMOS 3.3 volt

SPI Master IN Slave OUT: Data input pin.

**SPI_MOSI**

**Type:** output, CMOS 3.3 volt

SPI Master OUT Slave IN: Data output pin.

**SPI_CLK**

**Type:** output, CMOS 3.3 volt

SPI Clock: SPI clock signal, during idle the bus owner will drive the clock signal low. 17.86 MHz and 31.25 MHz.

## System Management Bus (SMB)

The host controller on the module provides a mechanism for the CPU to initiate communications with SMB peripherals (slaves).

The following SMB signals are located on the CoreExpress® connector:

**SMB_DATA**

**Type:** output, CMOS 3.3 volt open drain, internal Pull-up

SMBus Data: This signal is the SMBus data pin.

**SMB_CLK**

**Type:** output, CMOS 3.3 volt open drain, internal Pull-up

SMBus Clock: This signal is the SMBus clock pin.

**SMB_ALERT#**I CMOS3.3_OD

**Type:** input, CMOS 3.3 volt open drain, internal Pull-up

SMBus Alert: This signal can be used to wake the system, generate an interrupt, or generate an SMI#.

## Miscellaneous Signals

The following miscellaneous signals are located on the CoreExpress® connector:

### External POWER_BUTTON

**Type:** input, CMOS 3.3 volt

The power button signal is located on the CoreExpress® connector at pin PWR_BTN#. To activate the signal, PWR_BTN# must be pulled to ground. This function depends on the operating system used.

### External WAKE_UP Button

**Type:** input, CMOS 3.3 volt

The wake-up button signal is located on the CoreExpress® connector at pin WAKE#. To activate the signal, WAKE# must be pulled to ground. Its function depends on the operating system used.

### RESET_IN Signal

**Type:** input, CMOS 3.3 volt

The RESET-IN signal is located on the CoreExpress® connector at pin RST_IN#. To reset the board, RESET-IN must be pulled to GND.

### RESET_OUT Signal

**Type:** output, CMOS 3.3 volt

The RESET-OUT signal is located on the CoreExpress® connector at pin RST_OUT#. The signal will go low during RESET cycle.

### POWER_GOOD Signal

**Type:** input, CMOS 3.3 volt

The PowerGood signal is located on the CoreExpress® connector at pin PWR_GOOD. The signal should go high to indicate that the power supplies on the baseboard are active and within their valid ranges

### PS_ON

**Type:** output, CMOS 3.3 volt

The PowerSupply-on signal is located on the CoreExpress® connector at pin PS_ON. The signal will go high to switch on the external power supplies on the baseboard.

### BIOS_INIT Signal

**Type:** input, CMOS 3.3 volt

The BIOS_INIT# signal will force the bios to load setup defaults if connected to GND during power-on. If this function should be supported on the baseboard, it is recommended to route this signal to a jumper header on the baseboard.

### BIOS_DISABLE Signal

**Type:** input, CMOS 3.3 volt

The BIOS_DISABLE signal is located on the CoreExpress® connector at pin BIOS_DISABLE#. If pulled low, the onboard bios FWH will be disabled and an external FWH on the LPC bus can be used as bios source.

### WDOUT Signal

**Type:** output, CMOS 3.3 volt

The Watchdog-Out signal is located on the CoreExpress® connector at pin WD_OUT. It indicates a Watchdog timeout event with a high level. The watchdog timeout event indication is cleared on power-up and reset.

### SUS_S3# Signal

**Type:** output, CMOS 3.3 volt

The SUS_S3# signal will remain low if the system is in sleep state (ACPI S3 mode)

### SUS_S4/5# Signal

**Type:** output, CMOS 3.3 volt

The SUS_S4/5# signal will remain low if the system is in suspend state (ACPI S4/S5 mode)

### GPIO Pins

**GPIO0**
**GPIO1**

**GPIO2**
**GPIO3**

**Type:** input/output, CMOS 3.3 volt

These Pins are used as general input or output pins.

## 2.3 Pin Assignment

Signals were assigned to pins to simplify breakout and reduce trace lengths of the signals around the connector.

| Pin# | Signal Name | | Bus | | Voltage Level | Diff. Sig. |
|---|---|---|---|---|---|---|
| A1 | GND *(connected to metal shroud)* | | POWER | | 0V | no |
| A2 | PCIE_TXAn | | PCIexpress | | AC coupled | yes |
| A3 | PCIE_TXAp | | PCIexpress | | AC coupled | yes |
| A4 | PCIE_CLKAn | | PCIexpress | | 3.3V | yes |
| A5 | PCIE_CLKAp | | PCIexpress | | 3.3V | yes |
| A6 | GND | | POWER | | 0V | no |
| A7 | PCIE_TXBn | | PCIexpress | | AC coupled | yes |
| A8 | PCIE_TXBp | | PCIexpress | | AC coupled | yes |
| A9 | PCIE_TXCn | | PCIexpress | | AC coupled | yes |
| A10 | PCIE_TXCp | | PCIexpress | | AC coupled | yes |
| A11 | GND *(connected to metal shroud)* | | POWER | | 0V | no |
| A12 | PCIE_CLKCn | | PCIexpress | | AC coupled | yes |
| A13 | PCIE_CLKCp | | PCIexpress | | AC coupled | yes |
| A14 | PCIE_TXDn | | PCIexpress | | AC coupled | yes |
| A15 | PCIE_TXDp | | PCIexpress | | AC coupled | yes |
| A16 | GND | | POWER | | 0V | no |
| A17 | CLKREQA# | | PCIexpress | | 3.3V | no |
| A18 | CLKREQC# | | PCIexpress | | 3.3V | no |
| A19 | SDVO_CLK# | DP_LANE0_n | SDVO | DP | AC coupled | yes |
| A20 | SDVO_CLK | DP_LANE0_p | SDVO | DP | AC coupled | yes |
| A21 | GND *(connected to metal shroud)* | | POWER | | 0V | no |
| A22 | SDVO_GREEN | DP_LANE1_p | SDVO | DP | AC coupled | yes |
| A23 | SDVO_GREEN# | DP_LANE1_n | SDVO | DP | AC coupled | yes |
| A24 | SDVO_TVCLKIN# | NC | SDVO | | AC coupled | yes |
| A25 | SDVO_TVCLKIN | NC | SDVO | | AC coupled | yes |
| A26 | GND | | POWER | | 0V | no |
| A27 | SDVO_RED | DP_LANE3_p | SDVO | DP | AC coupled | yes |
| A28 | SDVO_RED# | DP_LANE3_n | SDVO | DP | AC coupled | yes |
| A29 | LA_DATA0p | | LVDS | | Low voltage | yes |
| A30 | LA_DATA0n | | LVDS | | Low voltage | yes |

| Pin# | Signal Name | Bus | Voltage Level | Diff. Sig. |
|---|---|---|---|---|
| A31 | GND *(connected to metal shroud)* | POWER | 0V | no |
| A32 | LA_DATA2p | LVDS | Low voltage | yes |
| A33 | LA_DATA2n | LVDS | Low voltage | yes |
| A34 | LA_DATA3p | LVDS | Low voltage | yes |
| A35 | LA_DATA3n | LVDS | Low voltage | yes |
| A36 | GND | POWER | 0V | no |
| A37 | L_DDC_DATA | LVDS | 3.3V | no |
| A38 | L_DDC_CLK | LVDS | 3.3V | no |
| A39 | USB_Ap | USB2.0 | Low voltage | yes |
| A40 | USB_An | USB2.0 | Low voltage | yes |
| A41 | GND *(connected to metal shroud)* | POWER | 0V | no |
| A42 | USB_Cp | USB2.0 | Low voltage | yes |
| A43 | USB_Cn | USB2.0 | Low voltage | yes |
| A44 | USB_Ep | USB2.0 | Low voltage | yes |
| A45 | USB_En | USB2.0 | Low voltage | yes |
| A46 | GND | POWER | 0V | no |
| A47 | USB_Gp | USB2.0 | Low voltage | yes |
| A48 | USB_Gn | USB2.0 | Low voltage | yes |
| A49 | USB_A/B_OC# | USB2.0 | 3.3V | no |
| A50 | USB_E/F_OC# | USB2.0 | 3.3V | no |
| A51 | GND *(connected to metal shroud)* | POWER | 0V | no |
| A52 | RGMII-TD0 | RGMII | 2.5 V | no |
| A53 | RGMII-TD1 | RGMII | 2.5 V | no |
| A54 | RGMII-TD2 | RGMII | 2.5 V | no |
| A55 | RGMII-TD3 | RGMII | 2.5 V | no |
| A56 | SMB_CLK | SMB | 3.3V | no |
| A57 | SMB_DATA | SMB | 3.3V | no |
| A58 | SMB_ALERT# | SMB | 3.3V | no |
| A59 | SATA_LED# | SATA2 | 3.3V | no |
| A60 | GND *(connected to metal shroud)* | POWER | 0V | no |
| A61 | SATA_TXAp | SATA2 | AC coupled | yes |
| A62 | SATA_TXAn | SATA2 | AC coupled | yes |
| A63 | SATA_RXAp | SATA2 | AC coupled | yes |
| A64 | SATA_RXAn | SATA2 | AC coupled | yes |
| A65 | GND | POWER | 0V | no |
| A66 | Reserved for future use | | | yes |
| A67 | Reserved for future use | | | yes |
| A68 | Reserved for future use | | | yes |
| A69 | Reserved for future use | | | yes |
| A70 | GND *(connected to metal shroud)* | POWER | 0V | no |

| Pin# | Signal Name | Bus | Voltage Level | Diff. Sig. |
|---|---|---|---|---|
| A71 | RGMII-TXC | RGMII | 2.5 V | no |
| A72 | RGMII-TXCTL | RGMII | 2.5 V | no |
| A73 | NC | | | no |
| A74 | RGMII-MDC | RGMII | 2.5 V | no |
| A75 | RGMII-MDIO | RGMII | 2.5 V | no |
| A76 | LPC_AD3 | LPC | 3.3V | no |
| A77 | LPC_AD1 | LPC | 3.3V | no |
| A78 | LPC_AD0 | LPC | 3.3V | no |
| A79 | LPC_FRAME# | LPC | 3.3V | no |
| A80 | GND *(connected to metal shroud)* | POWER | 0V | no |
| A81 | SD0_WP | SDIO 8Bit | 3.3V | no |
| A82 | SD0_CD# | SDIO 8Bit | 3.3V | no |
| A83 | SD0_CLK | SDIO 8Bit | 3.3V | no |
| A84 | SD0_DATA1 | SDIO 8Bit | 3.3V | no |
| A85 | SD0_DATA3 | SDIO 8Bit | 3.3V | no |
| A86 | SD0_DATA5 | SDIO 8Bit | 3.3V | no |
| A87 | SD0_DATA6 | SDIO 8Bit | 3.3V | no |
| A88 | L_CTLB_DATA | LVDS | 3.3V | no |
| A89 | L_CTLB_CLK | LVDS | 3.3V | no |
| A90 | GND *(connected to metal shroud)* | POWER | 0V | no |
| A91 | HDA_DOCK_EN# | HD Audio | 1.8V or 3.3V | no |
| A92 | HDA_SDATAIN1 | HD Audio | 1.8V or 3.3V | no |
| A93 | HDA_SDATAOUT | HD Audio | 1.8V or 3.3V | no |
| A94 | HDA_RST# | HD Audio | 1.8V or 3.3V | no |
| A95 | NC | | | no |
| A96 | GPIO0 | CONTROL | 3.3V | no |
| A97 | GPIO1 | CONTROL | 3.3V | no |
| A98 | GPIO2 | CONTROL | 3.3V | no |
| A99 | GPIO3 | CONTROL | 3.3V | no |
| A100 | GND *(connected to metal shroud)* | POWER | 0V | no |
| A101 | RESET_OUT# | CONTROL | 3.3V | no |
| A102 | RESET_IN# | CONTROL | 3.3V | no |
| A103 | WAKE# | CONTROL | 3.3V | no |
| A104 | +5V0 | POWER | 5V | no |
| A105 | +5V0 | POWER | 5V | no |
| A106 | +5V0 | POWER | 5V | no |
| A107 | +5V0 | POWER | 5V | no |
| A108 | +5V0 | POWER | 5V | no |
| A109 | +5V0 | POWER | 5V | no |
| A110 | GND *(connected to metal shroud)* | POWER | 0V | no |

| Pin# | Signal Name | | Bus | | Voltage Level | | Diff. Sig. | |
|---|---|---|---|---|---|---|---|---|
| B1 | GND *(connected to metal shroud)* | | POWER | | 0V | | no | |
| B2 | PCIE_RXAn | | PCIexpress | | AC coupled | | yes | |
| B3 | PCIE_RXAp | | PCIexpress | | AC coupled | | yes | |
| B4 | PCIE_CLKBn | | PCIexpress | | 3.3V | | yes | |
| B5 | PCIE_CLKBp | | PCIexpress | | 3.3V | | yes | |
| B6 | GND | | POWER | | 0V | | no | |
| B7 | PCIE_RXBn | | PCIexpress | | AC coupled | | yes | |
| B8 | PCIE_RXBp | | PCIexpress | | AC coupled | | yes | |
| B9 | PCIE_RXCn | | PCIexpress | | AC coupled | | yes | |
| B10 | PCIE_RXCp | | PCIexpress | | AC coupled | | yes | |
| B11 | GND *(connected to metal shroud)* | | POWER | | 0V | | no | |
| B12 | PCIE_CLKDn | | PCIexpress | | 3.3V | | yes | |
| B13 | PCIE_CLKDp | | PCIexpress | | 3.3V | | yes | |
| B14 | PCIE_RXDn | | PCIexpress | | AC coupled | | yes | |
| B15 | PCIE_RXDp | | PCIexpress | | AC coupled | | yes | |
| B16 | GND | | POWER | | 0V | | no | |
| B17 | CLKREQB# | | PCIexpress | | 3.3V | | no | |
| B18 | CLKREQD# | | PCIexpress | | 3.3V | | no | |
| B19 | SDVO_INT# | | SDVO | | AC coupled | | yes | |
| B20 | SDVO_INT | | SDVO | | AC coupled | | yes | |
| B21 | GND *(connected to metal shroud)* | | POWER | | 0V | | no | |
| B22 | SDVO_BLUE | DP_LANE2_p | SDVO | DP | AC coupled | | yes | |
| B23 | SDVO_BLUE# | DP_LANE2_n | SDVO | DP | AC coupled | | yes | |
| B24 | SDVO_STALL | DP_AUX_p | SDVO | DP | AC coupled | | yes | |
| B25 | SDVO_STALL# | DP_AUX_n | SDVO | DP | AC coupled | | yes | |
| B26 | GND | | POWER | | 0V | | no | |
| B27 | SDVO_CTRL_CLK | NC | SDVO | | AC coupled | | yes | |
| B28 | SDVO_CTRL_DAT | HP_DET | SDVO | DP | AC coupled | 3.3V | yes | no |
| B29 | LA_DATA1p | | LVDS | | Low voltage | | yes | |
| B30 | LA_DATA1n | | LVDS | | Low voltage | | yes | |
| B31 | GND *(connected to metal shroud)* | | POWER | | 0V | | no | |
| B32 | LA_CLKp | | LVDS | | Low voltage | | yes | |
| B33 | LA_CLKn | | LVDS | | Low voltage | | yes | |
| B34 | L_BKLTCTL | | LVDS | | 3.3V | | no | |
| B35 | L_BKLTEN | | LVDS | | 3.3V | | no | |
| B36 | L_DETECT | | LVDS | | 3.3V | | no | |
| B37 | L_VDDEN | | LVDS | | 3.3V | | no | |
| B38 | USB_C_DEVICE | | USB2.0 | | 3.3V | | no | |
| B39 | USB_Bp | | USB2.0 | | Low voltage | | yes | |
| B40 | USB_Bn | | USB2.0 | | Low voltage | | yes | |

| Pin# | Signal Name | Bus | Voltage Level | Diff. Sig. |
|---|---|---|---|---|
| B41 | GND *(connected to metal shroud)* | POWER | 0V | no |
| B42 | USB_Dp | USB2.0 | Low voltage | yes |
| B43 | USB_Dn | USB2.0 | Low voltage | yes |
| B44 | USB_Fp | USB2.0 | Low voltage | yes |
| B45 | USB_Fn | USB2.0 | Low voltage | yes |
| B46 | GND | POWER | 0V | no |
| B47 | USB_Hp | USB2.0 | Low voltage | yes |
| B48 | USB_Hn | USB2.0 | Low voltage | yes |
| B49 | USB_C/D_OC# | USB2.0 | 3.3V | no |
| B50 | USB_G/H_OC# | USB2.0 | 3.3V | no |
| B51 | GND *(connected to metal shroud)* | POWER | 0V | no |
| B52 | RGMII-RD0 | RGMII | 2.5 V | no |
| B53 | RGMII-RD1 | RGMII | 2.5 V | no |
| B54 | RGMII-RD2 | RGMII | 2.5 V | no |
| B55 | RGMII-RD3 | RGMII | 2.5 V | no |
| B56 | SPI_MISO | SPI | 3.3V | no |
| B57 | SPI_MOSI | SPI | 3.3V | no |
| B58 | SPI_CS# | SPI | 3.3V | no |
| B59 | SPI_CLK | SPI | 3.3V | no |
| B60 | GND *(connected to metal shroud)* | POWER | 0V | no |
| B61 | SATA_TXBp | SATA2 | AC coupled | yes |
| B62 | SATA_TXBn | SATA2 | AC coupled | yes |
| B63 | SATA_RXBp | SATA2 | AC coupled | yes |
| B64 | SATA_RXBn | SATA2 | AC coupled | yes |
| B65 | GND | POWER | 0V | no |
| B66 | Reserved for future use | | | |
| B67 | Reserved for future use | | | |
| B68 | Reserved for future use | | | |
| B69 | Reserved for future use | | | |
| B70 | GND *(connected to metal shroud)* | POWER | 0V | no |

| Pin# | Signal Name | Bus | Voltage Level | Diff. Sig. |
|---|---|---|---|---|
| B71 | RGMII-RXC | RGMII | 2.5 V | yes |
| B72 | RGMII-RXCTL | RGMII | 2.5 V | yes |
| B73 | NC | NC | NC | no |
| B74 | CAN_TX | CAN | 3.3V | yes |
| B75 | CAN_RX | CAN | 3.3V | yes |
| B76 | LPC_CLK_OUT2 | LPC | 3.3V | no |
| B77 | LPC_CLK_OUT1 | LPC | 3.3V | no |
| B78 | LPC_SERIRQ | LPC | 3.3V | no |
| B79 | LPC_AD2 | LPC | 3.3V | no |
| B80 | GND *(connected to metal shroud)* | POWER | 0V | no |
| B81 | SD0_DATA7 | SDIO 8Bit | 3.3V | no |
| B82 | SD0_PWR# | SDIO 8Bit | 3.3V | no |
| B83 | SD0_DATA2 | SDIO 8Bit | 3.3V | no |
| B84 | SD0_LED | SDIO 8Bit | 3.3V | no |
| B85 | SD0_DATA4 | SDIO 8Bit | 3.3V | no |
| B86 | SD0_DATA0 | SDIO 8Bit | 3.3V | no |
| B87 | SD0_CMD | SDIO 8Bit | 3.3V | no |
| B88 | WD_OUT | CONTROL | 3.3V | no |
| B89 | HDA_SPKR | HD Audio | 3.3V | no |
| B90 | GND *(connected to metal shroud)* | POWER | 0V | no |
| B91 | HDA_BITCLK | HD Audio | 1.8V or 3.3V | no |
| B92 | HDA_DOCK_RST# | HD Audio | 1.8V or 3.3V | no |
| B93 | HDA_SDATAIN0 | HD Audio | 1.8V or 3.3V | no |
| B94 | HDA_SYNC | HD Audio | 1.8V or 3.3V | no |
| B95 | BIOS_INIT# | CONTROL | 3.3 V | no |
| B96 | PWR_GOOD | CONTROL | 3.3 V | no |
| B97 | PS_ON | CONTROL | 3.3 V | no |
| B98 | PWR_BTN# | CONTROL | 3.3 V | no |
| B99 | SUS_S3# | CONTROL | 3.3 V | no |
| B100 | GND *(connected to metal shroud)* | POWER | 0V | no |
| B101 | SUS_S4/5# | CONTROL | 3.3 V | no |
| B102 | BIOS_DISABLE# | CONTROL | 3.3 V | no |
| B103 | BAT_IN | POWER | 2.8 – 3.3 V | no |
| B104 | +5V0-ALWAYS | POWER | 5V | no |
| B105 | +5V0 | POWER | 5V | no |
| B106 | +5V0 | POWER | 5V | no |
| B107 | +5V0 | POWER | 5V | no |
| B108 | +5V0 | POWER | 5V | no |
| B109 | +5V0 | POWER | 5V | no |
| B110 | GND *(connected to metal shroud)* | POWER | 0V | no |

# 3.0 Electrical specification

## 3.1 Power and Ground

Power on the connector A comes from +5V and +5V-ALWAYS. The current carrying capacities of the pins are shown in the table below. The maximum total power is calculated on the minimum voltage with 15 % derating for higher temperature.

| Voltage | minimum voltage (V) | maximum voltage (V) | Number of pins | Current per pin (A) | Total current (A) | Total power (W), with minimum voltage and 15 % derating on higher temperature |
|---|---|---|---|---|---|---|
| +5V-ALWAYS | 4.75 | 5.25 | 1 | 0.5 | 0.5 | 2 |
| +5V | 4.75 | 5.25 | 11 | 0.5 | 5.5 | 22 |

## 3.2 AC/DC Signal Specifications

For full details on the electrical requirements of the connector signals refer to the links in Appendix B.

## 3.3 Mounting Holes

The specification defines four mounting holes for mounting the module on a baseboard. The copper pad should have a minimum outer diameter of 5.0 mm to give enough room for the metric spacers, the diameter should be 2.2 mm. The mounting holes should not be connected directly to ground but they should be electrical coupled by using a 1Mohm resistor and 10nF capacitor in parallel to GND.

# 4.0 Layout Guidelines

These guidelines should be used as design information for CoreExpress® baseboard designs.

## 4.1 General Routing Guidelines

Use the following general routing and placement guidelines to layout a new design.

- Single ended and most differential signals must be ground referenced. If changing reference plane is completely unavoidable (i.e. ground reference to power reference), proper placement of stitching caps can minimize the adverse effects of EMI and signal quality performance caused by reference plane change. Stitching capacitors are small-valued capacitors (1 µF or lower in value) that bridge the power and ground planes close to where a high-speed signal changes layers. Stitching capacitors provide a high frequency current return path between different reference planes. They minimize the impedance discontinuity and current loop area that crossing different reference planes created.
- Route all traces over continuous GND planes, with no interruptions. Avoid crossing over anti-etch if possible at all. Any discontinuity or split in the ground plane can cause signal reflections and should be avoided. Minimize layer changes. Via count should include thru-hole connector as an effective via. If routing differential signals and a layer change is necessary, ensure that trace matching for either transmit or receive pair occurs within the same layer. Recommend minimal use of vias.
- DO NOT route high speed signal traces under power connectors, other interface connectors, crystals, oscillators, clock synthesizers, magnetic devices or IC's that use and/or duplicate clocks.
- DO NOT place stubs, test points, test vias on the route to minimize reflection on high speed signals. Utilize vias and connector pads as test points instead.
- DO NOT route high speed signal traces with tight bends. Match number of left and right turn bends if possible.
- E.g. for SATA and PCI Express, it can be helpful for testability to route the TX and RX pairs for a given port on the same layer and close to each other to help ensure that the pairs share similar signaling characteristics. If the groups of traces are similar, a measure of RX pair layout quality can be approximated by using the results from actively testing the TX pair's signal quality.
- Each net within a differential pair should be length matched on a segment-by segment basis at the point of discontinuity. Total length mismatch must not be more than 5 mils. Examples of segments might include breakout areas, routes running between two vias, routes between an AC coupling capacitor and a connector pin, and so forth. The points of discontinuity would be the via, the capacitor pad, or the connector pin.
- Recommend keeping high speed signal traces as SATA and PCI Express 20 mils from any traces, vias and pads on the motherboard whenever possible.
- AC coupling capacitors for the TX lines are all placed on the module. (Note: except for SATA).

## 4.2 General Notes

- Pair-to-pair pitch is defined as the distance from the center of either trace in a differential pair to the same point of reference on an adjacent differential pair.
- Bus-to-Bus spacing mentioned in this table is the amount of space between two differential pairs.

## 4.3 PCI-Express

The PCI-Express interface on the CoreExpress® connector uses differential signaling as defined by the PCI-Express specification.

- Single Ended Impedance: 55 Ω ±15 %
- Differential Impedance: 100 Ω ±20 %
- Pair-to-pair pitch: min. 35 mils
- Bus-to-Bus spacing: min. 20 mils
- Maximum trace length: 6.1"
- Maximum via count: 4
- AC coupling capacitor value: 100 nF / 0402

Length matching between the differential pairs is not needed. Place devices AC coupling caps (only at transmit lines) near device. Unused PCI-Express ports may be left unconnected.

## 4.4 SDVO / Display Port

- Single Ended Impedance: 55 Ω ±15 %
- Differential Impedance: 100 Ω ±20 %
- Pair-to-pair pitch: min. 35 mils
- Bus-to-Bus spacing: min. 20 mils
- Maximum total trace length: 3.2"
- Maximum via count: 4
- AC coupling capacitor value: 100 nF / 0402

Length matching between all the differential pairs within the SDVO channel is required to be within 1" of each other. Place devices AC coupling caps (only at transmit lines) near device.

## 4.5 SDIO

- total maximum trace length: 3.5"
- series resistor value: 48.7 Ω / 1 %

Trace length matching is not needed. Place series resistor for data and clock as near as possible to the CoreExpress® connector.

## 4.6 LVDS

**LVDS CLK and Data Signals**

- Single Ended Impedance: 55 Ω ±15 %
- Differential Impedance: 100 Ω ±20 %
- Pair-to-pair pitch: min. 35 mils
- Bus-to-Bus spacing: min. 20 mils
- Maximum trace length: 4.3''
- Maximum via count: 2

Length matching between all the differential pairs within the LVDS channel is required to be within 10 mils of each other, for the entire route to help minimize latency.

**LVDS Control Bus Signals**

Single ended L_DDC_CLK and L_DDC_DATA signals should be routed together with a maximum length of 8".

These signals have a 2.2 kΩ pull-up resistor to 3.3V on the module.

The minimum edge to edge spacing of the LVDS control bus signals (L_DDC_CLK and L_DDC_DATA) to all the other LVDS signals should be 30 mils to avoid potential noise issues. Note that this spacing requirement should be met throughout the board routes including the breakout and breaking regions.

If the control bus from the flat panel device has a different signaling voltage than 3.3 V used by the L_DDC_CLK and L_DDC_DATA signals, then a bi-directional level shifting device will be required to properly translate the voltage levels.

## 4.7 USB 2.0

USB lines are routed directly to the CoreExpress® connector. Common Mode chokes and ESD protection diodes must be placed on the baseboard.

- Single Ended Impedance: 55 Ω ±15 %

- Differential Impedance: 90 Ω ±15 %
- Pair-to-pair pitch: min. 35 mils
- Bus-to-Bus spacing: min. 20 mils
- Spacing to CLK signals: min. 50 mils
- CoreExpress® connector to EMI choke: 8.0'' max trace length
- EMI choke to ESD diode: 0.5'' max trace length
- ESD diode to connector: 0.2'' max trace length
- Maximum total trace length: 10.5''
- Maximum via count: 2

Length matching between the differential pairs is not needed.

## 4.8 HD-Audio

- Core-Express connector to series resistor: 5.5'' max trace length
- Series resistor to Audio Codec: 1.0'' max trace length
- Series resistor value: 33 Ω / 1 %

Trace length matching is not needed. Place series resistors near to the respective signal source.

## 4.9 SATA

- Single Ended Impedance: 55 Ω ±15 %
- Differential Impedance: 100 Ω ±20 %
- Pair-to-pair pitch: min. 35 mils
- Bus-to-Bus spacing: min. 20 mils
- Maximum trace length: 4.5''
- Maximum via count: 2
- AC coupling capacitor value: 10nF / 0402

Length matching between the differential pairs is not needed. Place devices AC coupling caps near SATA connectors. Unused SATA ports may be left unconnected.

**SATA_LED# Implementation**

The CoreExpress® connector provides a signal (SATA_LED#) to simplify the indication of SATA devices activity. The SATA_LED# signal has a weak internal pull-up (10-kΩ) to 3.3V on the module. When low, SATA_LED# indicates SATA device activity and should activate the Hard Drive LED. The SATA_LED# represents SATA activity on any SATA ports.

## 4.10 SPI

- Single Ended Impedance: 55 Ω ±15 %
- Maximum trace length: 6.0''
- series resistor value: 33 Ω / 1 %

Trace length matching is not needed. Place series resistors near to the respective signal source. If SPI_CS# is not needed, tie to 3.3V with a 1kΩ resistor.

## 4.11 SMBus

Bus capacitance must not exceed 200pF. If the bus capacitance is exceeded, then a bus bridge like the Philips PCA9515 must be used to obtain a second SMBus segment with an additional capacitance of 400pF.

Cumulate the pin capacitance of the SMBus devices and add 4pF per inch of trace length on the baseboard. The result is the bus capacitance.

## 4.12 LPC Bus

There are no special design rules for the LPC Bus. No series resistors are needed.

# 5.0 Mechanical specification

## 5.1 Connector on Module

The module uses a surface mount, fine pitch stacking board-to-board connector receptacle with 220 pins in two rows. An equivalent connector can also be used.

**Part Number**

Tyco 3-6318490-6 or equivalent

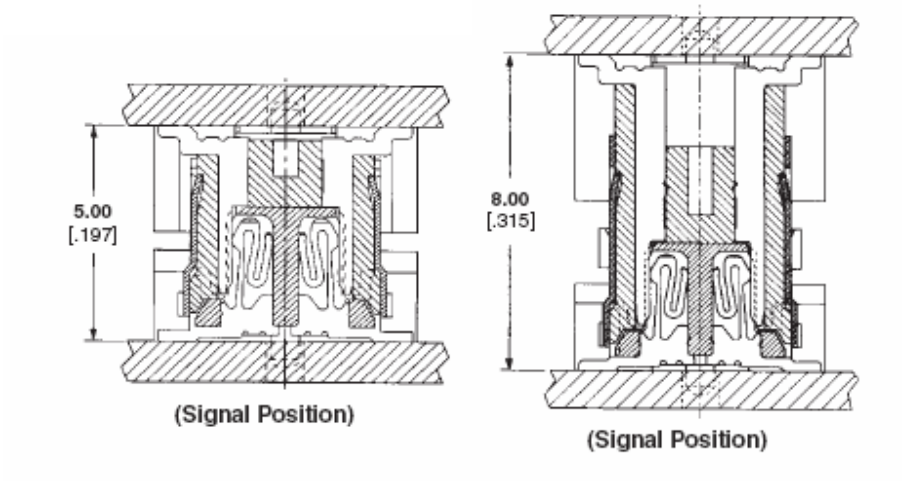
## 5.2 Connector on Baseboard

The mating connector plugs from are used as the baseboard connector. The connector plug is available in different stacking heights. The standard height is 5.00 mm.

**Part Number**

5.00 mm stacking height: Tyco 3-1827253-6 or equivalent

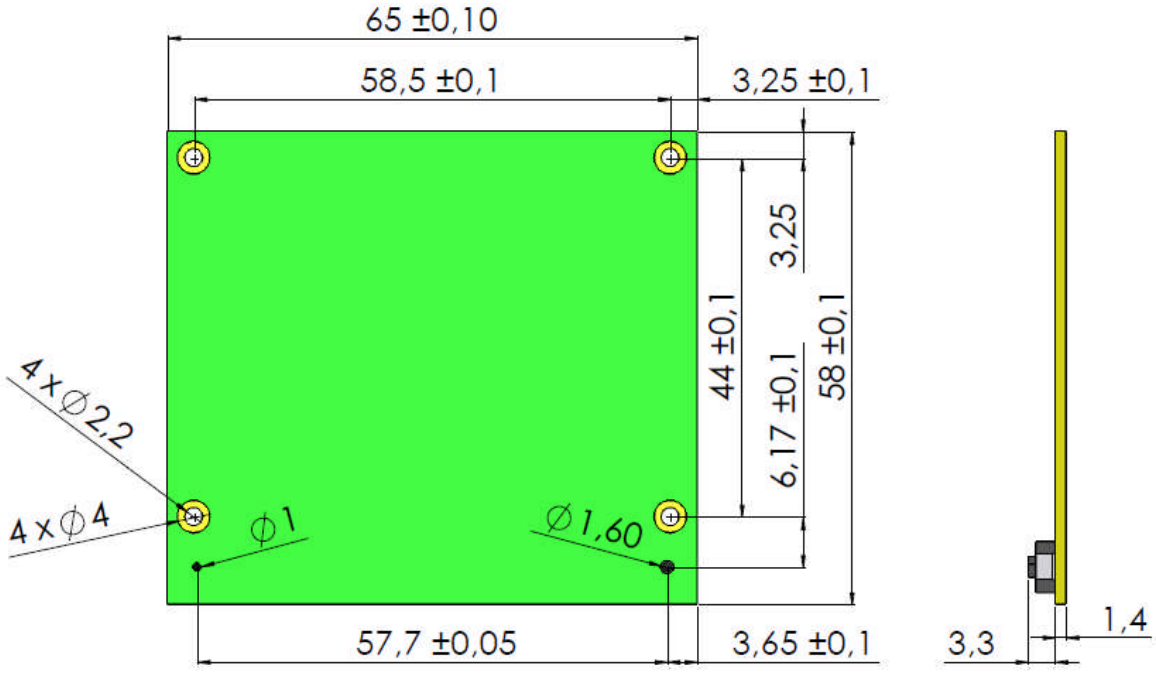
8.00 mm stacking height: Tyco 3-6318491-6 or equivalent



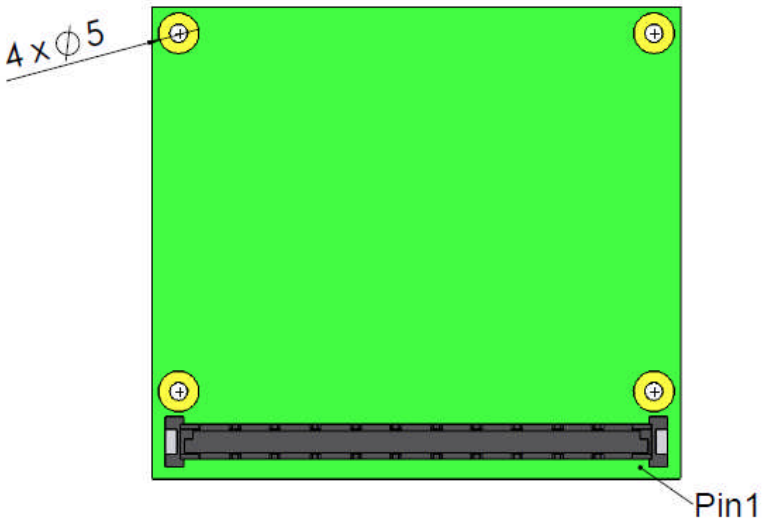

5 mm stacking height 8 mm stacking height

## 5.3 Mechanical View

**Top** (all dimensions are in mm)



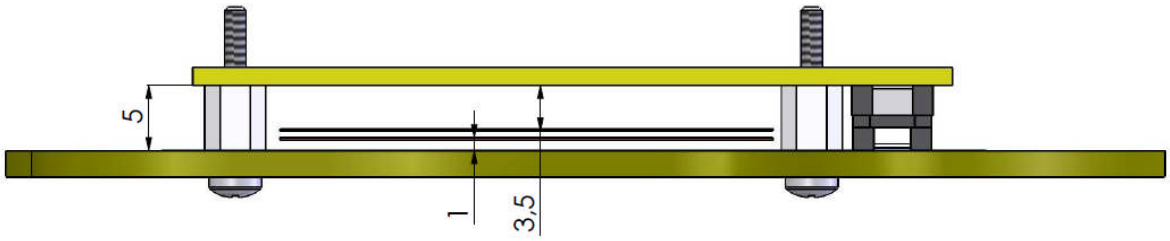

**Bottom**



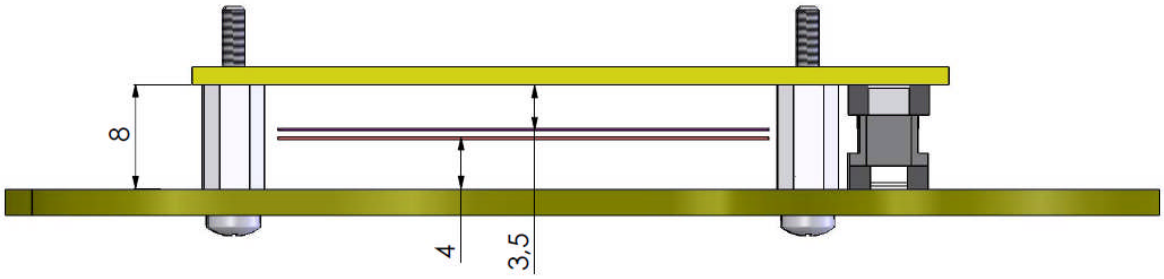
## 5.4 Component Height

Parts mounted on the bottom side of the module in the space between the bottom surface of the module PCB and the baseboard shall have a maximum height of 3.5 mm.

If the baseboard is using the connector with 5 mm stacking height the clearance between the baseboard and the bottom surface of the module's PCB is 5 mm. Components placed on the baseboard topside underneath the module shall be limited to a maximum height of 1 mm with the exception of the mating connectors.




If the baseboard is using the connector with 8 mm stacking height the clearance between the baseboard and the bottom surface of the module's PCB is 8 mm. Components placed on the baseboard topside underneath the module shall be limited to a maximum height of 4 mm with the exception of the mating connectors.




With this limitation the gap between baseboard topside components and module bottom side components is 0.5 mm.

## 5.5 Standoff

Standoffs are used to ensure stacked boards retain their connectivity. The preferred standoffs are made of stainless-steel to provide maximum strength and height tolerance. Pads must be provided for the standoffs. The width of the standoff must be able to fit on the standoff pad called out on the Mechanical View section. The width of the threaded section must be able to fit into the standoff pad hole called out in the Mechanical View section.

## 5.6 Mounting

The module is mounted on a baseboard by using metric spacers M2 male with the matching length of the baseboard connector. For this purpose the module offers four mounting holes at the edges of the board. The standard length of the spacers is 5.00 mm, optional 8.00 mm.

**Caution** For mounting the module hold it in parallel above the baseboard connector and press it down gently into the baseboard connector. Use four M2 screws with a length of 6 mm (assuming a baseboard thickness of 1.4 mm) to fix the module by screwing from below the baseboard.

**Caution** For dismounting the module, release the mounting screws and pull out the module gently from the baseboard connector. Do not bend the module to left or right. This might damage the module or baseboard connector.