

Busbar Design: How to Spare Nanohenries ?

JM.Guichon¹, J.Aimé¹, JL.Schanen¹, C.Martin¹, J.Roudet¹, E.Clavel¹
M.Arpillière², R.Pasterczyk³, Y.Le Floch⁴

¹ Laboratoire d'Electrotechnique de Grenoble,
CNRS UMR 5529 INPG/UJF
ENSIEG, B.P.46, 38402, SMH Cedex, Grenoble France

² Schneider Toshiba Inverter Europe (STIE)
Rue André Blanchet, 27120 Pacy sur Eure France

³ MGE UPS SYSTEM,
140 av Jean Kuntzmann – 38334 Saint Ismier Cedex France

⁴ CEDRAT
15, Chemin de Malacher
ZIRST 38246 MEYLAN Cedex France

Abstract— This paper intends to compare the many different solutions available to design a busbar interconnection. Starting from a single copper plate and going to multilayer busbars, the influence of the external shape of the sheet, of the number and the nature of holes and apertures are considered. Simulations and measurements are used to determine the stray inductance of the different busbars. Design rules are deduced from the many case studies, based on industrial examples

I. INTRODUCTION

Power Electronics often requires very low inductive interconnections, especially in the medium-high power range. The most common solution to reach stray inductance values around some tens of nanohenries and even below is to use a busbar structure. This "simple" assembly of copper sheets is intended to link several points of the structure, and to stay as equipotential as possible.

This part of a power electronics converter seems obvious to design, however, this is not so simple: mechanical considerations, economical constraints can lead to modify the first geometry proposed by electrical engineers. Some small changes during the mechanical design, decided by non specialist engineers, may lead to dramatic increase of the stray inductance.

The aim of this paper is to start from the most basic busbar, a simple sheet, and to show the various impacts of a change in the geometry, on both current repartition in the plate, and impedance of the interconnection. Then, multilayer busbars will be investigated, using industrial examples. The effect of the number of layers, of the position and shape of all necessary holes and apertures will be studied.

This study will be achieved using simulations, using PEEC method (Partial Element Equivalent Circuit [1-2]), which has shown a great ability to handle all complex structures of power electronics, compared to more conventional Finite Elements Methods [3]. Indeed, PEEC method uses integral formulations, which avoid the meshing of the air.

Some measurements are also provided, in order to confirm the conclusions of the simulations. As a conclusion, some interesting design rules are given, which may be useful to avoid the degradation of the electrical properties of a busbar

(e.g. the stray inductance), when going outside the electrical engineering to enter into the mechanical design...

II. THE MOST BASIC BUSBAR

The role of a busbar is to link several points of a power electronics converter: capacitors, semiconductors, ... and often to achieve series or parallel association of these devices. The very basic concept is to use a simple copper sheet. Indeed, it can be shown that a flat conductor exhibits a smaller inductance than a massive one (Fig. 1) [4]. Another well known property is that the copper volume also brings an impedance reduction. The resistance but also the inductance decrease, with the increase of the amount of copper (Fig. 2). Additionally, thermal and mechanical behaviour are improved, for larger sheet thickness. However, price and weight increase in the same time, what is not desired.

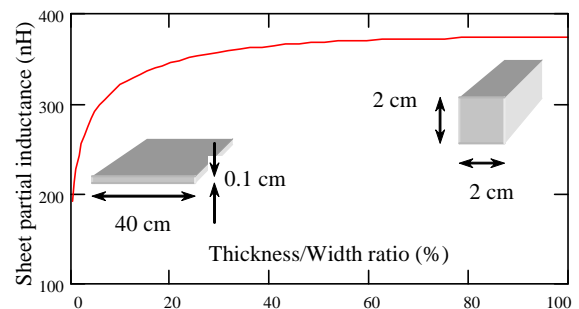


Fig. 1. Influence of the shape of the cross section of the sheet on its partial inductance, for the same copper volume

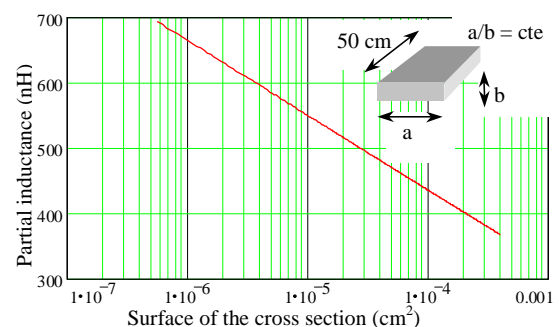


Fig. 2. Influence of the shape of the cross section of the sheet on its partial inductance, for the same width/thickness ratio.

When using a simple copper sheets, a drawback may be a large unbalance between the different access points. The example of Fig. 3 illustrates this effects, in the case of two paralleled IGBT modules. To compensate this unbalance, apertures in the sheet can be machined, as shown in Fig. 4.

This result is obtained after an optimization procedure, detailed in [5]. To sum up briefly, the sheet is meshed in small elements, represented by a simple R,L circuit and couplings (according to PEEC Method). The different impedances and the current repartition between the two IGBTs are computed from the assembly of all these small R, L circuits in a large impedance matrix. Apertures are simply built by deleting small elements in the complete matrix. Genetic algorithm is used for optimization. At the end of optimization, some artefacts remain (small holes distributed among the sheet), which can be "refilled" without any consequence on the results (Fig. 4).

However, it may be seen in Table 1 that if the current is well balanced, the aperture results in an increase of partial inductance, especially the one of Branch1.

An interesting property of holes and various apertures in conductors is as follows: the effect of a hole on the inductance value can be very different if it is located in the middle of the sheet, or near the edges. Indeed, in this latter case, the external magnetic field is greatly modified [6]. Therefore, it can be shown that inserting a hole in the middle of a copper plane has less repercussion on its impedance than machining apertures on the edges. This property, linked to the modification of the external field, will be illustrated in section IV, on the example of an industrial busbar.

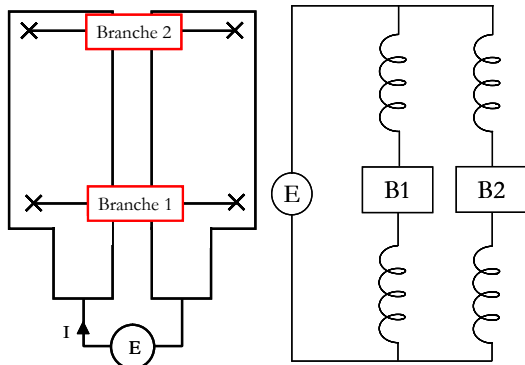


Fig. 3. Example of two single sheets to achieve a parallel association of two IGBTs (Branch1 –B1, and Branch2 – B2)

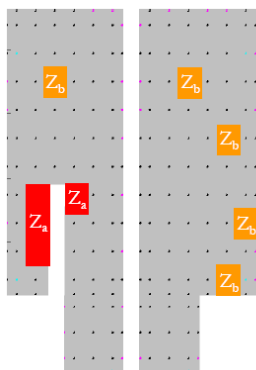


Fig. 4. Optimized aperture to better balance the currents in Branch 1 and Branch2. Some "refilled" holes.

Table 1. Inductance values of Branch1 and Branch2 path. Comparison without and with the aperture.

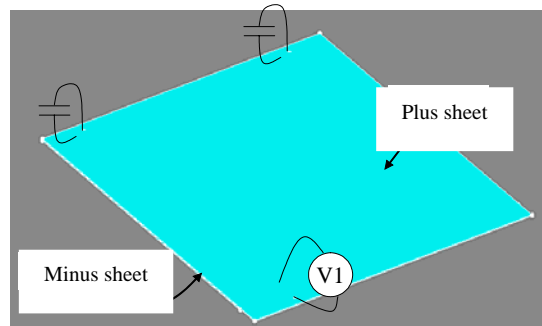
Without Aperture	Current (% I)	Inductance
Branch 1	84%	73nH
Branch 2	16%	144nH

With Aperture	Current (% I)	Inductance
Branch 1	50.67%	155nH
Branch 2	49.33%	157nH

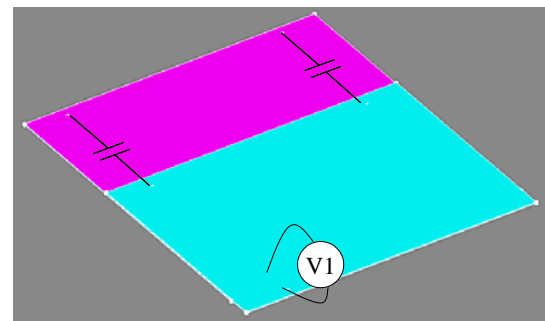
III. TWO LAYERS BUSBAR

Even if a copper sheet is less inductive than conventional wires, the stray inductance is still too high regarding the large current variations of power electronics. Thus, the next step is to use two close sheets: it allows to reduce the inductance, taking advantage of the large coupling between the sheets. Indeed, the equivalent inductance of a set of two sheets is equal to $Ls1+Ls2-2.Ms12$, and the $Ms12$ value may be very large, as illustrated in the example of Fig. 5. In this example, two sheets are associated to insure the link between a source and two paralleled capacitors. It is clear that the overlap between the two conductors is a key point to reach low inductance.

Another interesting point of this strong coupling is that it provides an important immunity related to external magnetic interferences [7]. Indeed, the two plates "see" nearly the same magnetic field, which induces more or less the same voltage: therefore, the differential voltage between the two sheets is nearly zero. Numerical simulations have been carried out in a specific case: starting from a coupling coefficient of 0.96 between two sheets, this coefficient falls to 0.024 if the two sheets are replaced by two busbars.



$$L=5.1 \text{ nH} - (Ls1=Ls2=108.9; M=106.35)$$



$$L=26.0 \text{ nH} - (Ls1=74,3; Ls2=108,9 M=78.6)$$

Fig. 5. Two layers busbar with identical external dimensions – Top: perfect overlap results in a low inductance – Bottom: a not complete overlap implies a reduced mutual coupling and a higher loop inductance

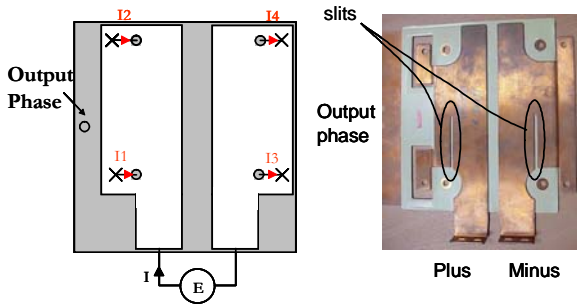


Fig. 6: Two layers IGBT busbar for inverter leg.

If the use of two layers busbars reduces drastically the inductance, the problem of current repartition between all components connected to the busbar may still be present. For instance, Fig. 6 depicts the realization of an inverter leg, using two paralleled IGBTs. Due to the dissymmetry of the power bus location (on the bottom of the busbar in the figure), the designers may try to insert some slits as in the case of the sheet of section II. However, in this case, it has no impact on the current repartition, as illustrated in Table 2. This is due to the current path, which is very different in this geometry, and implies many mutual couplings. This example shows how intuition is tricky in electromagnetism...

Table 2. Current repartition between the four IGBTs.

	I1	I2	I3	I4
Initial	51.95%	48.05%	53.01%	46.99%
With slits	49.75%	50.25%	50.01%	49.99%

Table 3 shows that the loop inductance of each path of the busbar (either through IGBTs 1 and 3, or 2 and 4) is in the range of 80 nH, what is high compared to the result of the ideal case of Fig. 5 (more or less the same dimensions). This is due to the fact that the "plus" and "minus" sheets are not stacked together: therefore, the mutual coefficient is low.

Table 3. Comparison between 2 loop inductances

	L_{1-3}	L_{2-4}
Simulation with slits	95.6nH	87.1nH
Simulation without slit	81nH	88nH

Another geometry would greatly reduce the inductance: in fact this busbar is a two layer technology, but takes no advantages from the overlap between arrival and return path, like in Fig. 5-top.

Unfortunately, since there is a need of three different potentials in this application (DC Bus and output phase), three sheets of copper are needed, and the best geometry would be a three layer busbar, which implies a higher cost.

IV. MULTILAYER BUSBAR AND INDUSTRIAL EXAMPLE

Let us now consider an industrial example using a more complex multilayer busbar. It is the classical variable speed application, using a three phases rectifier, feeding a three phases voltage inverter, including an additional chopper, for braking purpose. The busbar of Fig. 7 contains all the interconnects for this application. Three IGBT modules are connected to V1, V2, V3, and the additional module for braking circuit is connected to Vac.

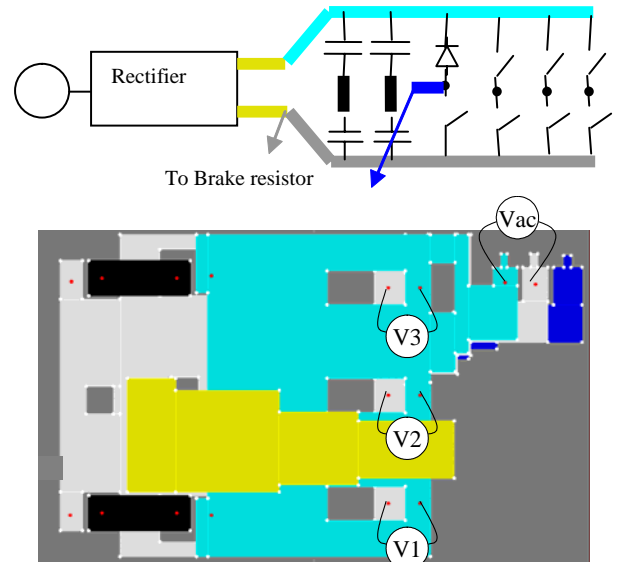


Fig. 7. Multilayer busbar for a complete inverter. On the Top of the Figure: electrical scheme with the same colours of the busbar copper sheets.

The first remark before analysing this busbar is that all conductive sheets do not participate directly to the switching cell. At the very top, a set of two conductors (yellow) forms an independent busbar, which links a rectifier to the inverter (feeding the DC bus). At the very bottom a dedicated conductor (dark blue) connects the DC bus to a braking circuit, using another IGBT.

Even if these additional conductors do not participate to the switching cell, they may modify a little the magnetic field, and thus the stray inductance. To investigate this possibility, two simulations have been carried out, one with the complete geometry, and the other keeping the "active" plates only. The aim of these simulations was to compute 4 impedance: the braking circuit switching cell inductance (Vac) and the three inductances "seen" from the IGBT modules of the inverter (V1, V2 and V3). To close the loops, the capacitors (connected between the black plates and the grey and cyan ones) have been short circuited. Simulations have been carried out at 1 MHz, which corresponds to the equivalent frequency of the IGBTs transitions.

The results show the very little influence of the additional plates on the stray inductance of the busbar: the differences are less than 1%. This is in good coherence with the remark of section III: the influence of external conductors on the loop inductance of a busbar is weak.

The rest of the paper will thus focus only on the three "actives" sheets of copper: the DC Bus (cyan and grey) and the capacitor interconnection (black).

The first design of this busbar, from electrical engineers, is described in Fig. 8. This busbar will be referred as EEBB in the following. Compared to the version of Fig. 7, referred as MEBB, some "small" modifications can be noticed: additional holes have been added by mechanical engineers.

The four switching cells are used for comparison purpose. The signification of this matrix can be explained as follows: the inductance L11 is obtained when feeding loop V1 with a current, and measuring voltage across loop V1.

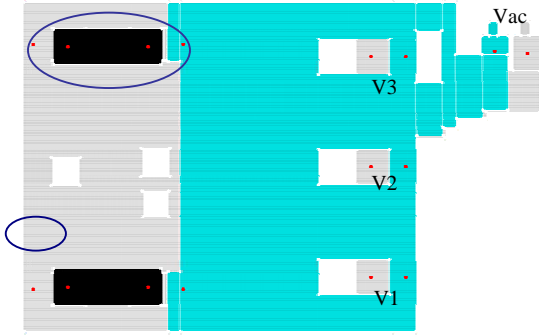


Fig. 8. The initial geometry proposed by electrical engineers, with an highlight on the modifications proposed by the mechanical staff (Fig. 7).

In the same idea, L32 is obtained when feeding loop V3, and measuring across V2. This is illustrated in Fig. 9. The current source is a rising current, and voltage drop measurement allows the determination of the element of the impedance matrix. Table 4 shows the impedance matrix of the electrical engineers busbar, EEBB (Fig. 8). To be noticed that all terms of this impedance matrix exhibit a real and an imaginary part, since the circuits have many common parts. Fig. 10 shows an example of measurement. The order of magnitude of the results (16.6 nH vs 19.9 estimated) is correct, taking into account the difficulty of measurement (parasitic coupling between the feeding circuit and the busbar, non perfect short circuits to replace capacitors...).

Table 4: Values of impedance matrix from electrical engineers busbar. Real part in $\mu\Omega$, imaginary part in nH (computed at 1MHz)

Real [$\mu\Omega$]	Vac	V3	V2	V1
Vac	264,71	-105,29	-93,45	-75,81
V3	-105,29	134,27	88,53	74,31
V2	-93,45	88,53	122,03	87,09
V1	-75,81	74,31	87,09	134,97
Imag.[nH]	Vac	V3	V2	V1
Vac	39,27	-19,27	-18,75	-18,44
V3	-19,27	26,91	19,86	18,62
V2	-18,75	19,86	26,17	19,59
V1	-18,44	18,62	19,59	27,15

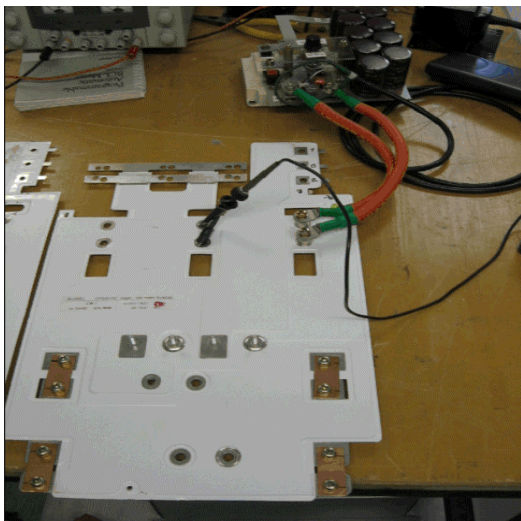


Fig. 9. Experimental setup to test the busbar: L32 Measurement.

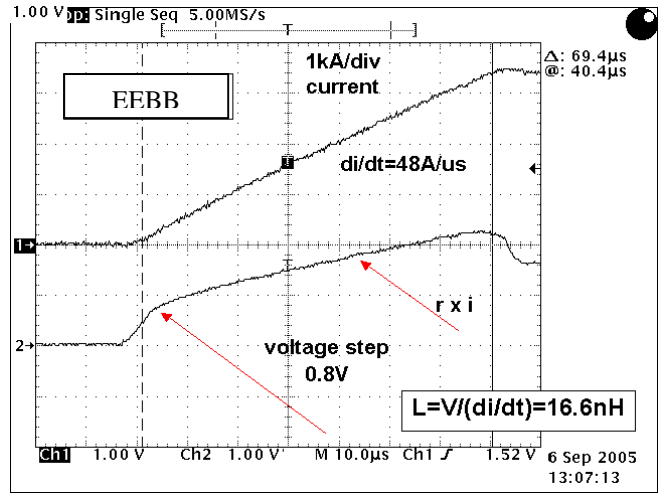


Fig. 10. Example of experimental measurement of L32.

Table 5 shows the impedance matrix of MEBB busbar, which has to be compared to the results of Table 4. It is clear from these results that the modifications brought by mechanical engineers have depredated the busbar quality: a degradation between 16% and 40% in all switching loop inductances has been found.

Table 5: Values of impedance matrix from mechanical engineers busbar. Real part in $\mu\Omega$, imaginary part in nH (computed at 1MHz)

Real [$\mu\Omega$]	Vac	V3	V2	V1
Vac	308,96	-135,45	-122,91	-101,95
V3	-135,45	167,48	116,71	99,74
V2	-122,91	116,71	153,05	114,93
V1	-101,95	99,74	114,93	168,35
Imag.[nH]	Vac	V3	V2	V1
Vac	46,66	-27,10	-26,45	-26,03
V3	-27,10	34,78	27,48	26,20
V2	-26,45	27,48	33,86	27,14
V1	-26,03	26,20	27,14	35,00

The rest of this section will investigate the causes of this degradation. First of all, it can be noticed that the value of L11 is far from the ideal case of Fig. 5 (27.1 nH for EEBB, 35.0 nH for MEBB, versus 5.1 nH for the ideal case).

A first cause of this gap between the actual busbar and the ideal case is related to the non perfect overlap between plus and minus sheet, as explained in section III. Like in Fig. 5, Fig. 8 shows that it is clearly the case. Consequently, minimum inductance cannot be lower than 26 nH. However, the small plates corresponding to the capacitor link (the green sheets in Fig. 11, or the black ones in Fig. 8) contribute to the mutual inductance between plus and minus sheets, and therefore to the reduction of the loop inductance. Consequently, with this small sheets of copper, the reduction of inductance is significant: 11 nH for the idealised case of Fig. 11. The main explanation for the large value of MEBB inductance is thus that under these small copper sheets, a hole has been machined (Fig. 7). In this case, the mutual inductance is significantly reduced, and the simulation in the idealised case of Fig. 11 shows an inductance increased to 19.4 nH.

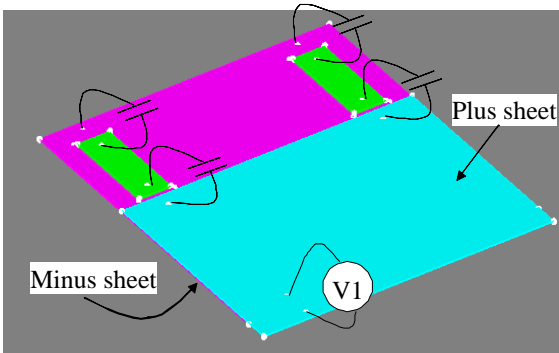


Fig. 11. $L=19,4$ nH with holes under the green conductors, 11nH with plain sheet. V1 loop between plus sheet (cyan) and minus sheet (magenta).

This very simple example shows the importance of the overlap between the copper sheets. The remaining difference between this simple example and the actual busbars is due to the various holes, which contribute to the increase of the inductance.

As explained in section II, the influence of the holes in the sheets greatly depends on their position on the sheet: if they modify the current path, or if there are located near the edge, it has a great influence. In the case of the treated busbar, the most important hole is the one highlighted in Fig. 8.

V. CONCLUSION

The aim of this paper was to give design rules for the electrical engineer faced to a busbar. Some of them are well known: using large sheets, multilayer if possible, and overlapping as much as possible the return path with the rest of the structure. Some others are not obvious, such as the influence of holes and apertures. In this case, intuition becomes often useless, and simulation useful...

VI. REFERENCES

- [1] A.E. Ruehli, "Inductance calculations in a complex integrated circuit environment", IBM Journal on R&D, Sept. 1972.
- [2] C. Martin, J.L. Schanen, R. Pasterczyk "Inside a Power Module", IEEE IAS 04, 2-7 octobre 2004, Seattle
- [3] Jones, M.; Kelley, A.W. "Wideband circuit model for busbar impedance" APEC 2000. Fifteenth Annual IEEE Volume 2, 6-10 Feb. 2000 Page(s):839 - 845 vol.2
- [4] Schanen, J.L. Clavel, E.; Roudet, J. "Modeling of low inductive busbar connections" Industry Applications Magazine, IEEE Volume 2, Issue 5, Sept.-Oct. 1996 Page(s):39 - 43
- [5] C.Martin, J.M.Guichon, J.L.Schanen, R.Pasterczyk "Planar busbar optimization regarding current sharing and stray inductance minimization", EPE'05, sept 05, Dresden
- [6] E.Clavel, J.L.Schanen, J.Roudet, Y.Maréchal "Influence of an impedance step in interconnection inductances calculation" IEEE-Transactions on Magnetics May 96 vol 32 n°3 pp 824-827
- [7] Fu Zhengcai; Xu Lin; Du Yaping "Power frequency magnetic fields around busbar trunking risers" Electromagnetic Compatibility, 2002 3rd International Symposium on, 21-24 May 2002 Page(s):354 - 357