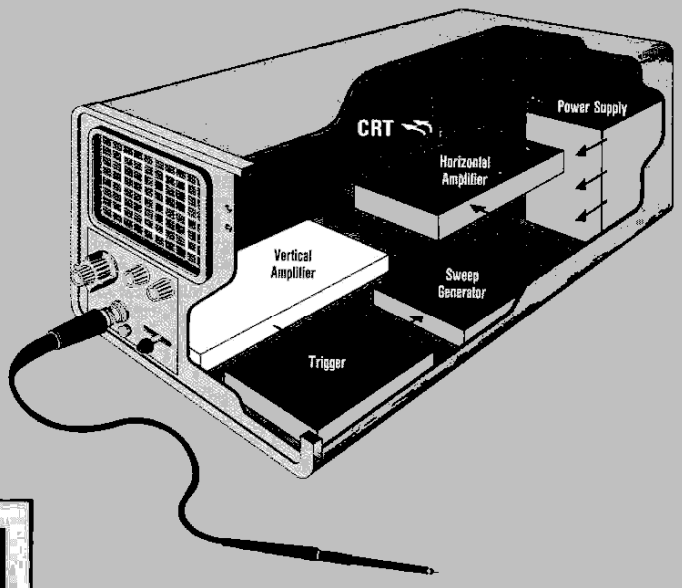
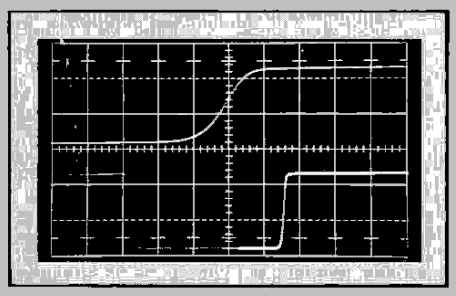
Vertical Amplifier Circuits





Circuit Concepts Series

prepared by Pius Steiner 10/2009 for **www.radiomuseum.org**

OSCILLOSCOPE VERTICAL AMPLIFIERS

BY

BOB ORWILER

CIRCUIT CONCEPTS

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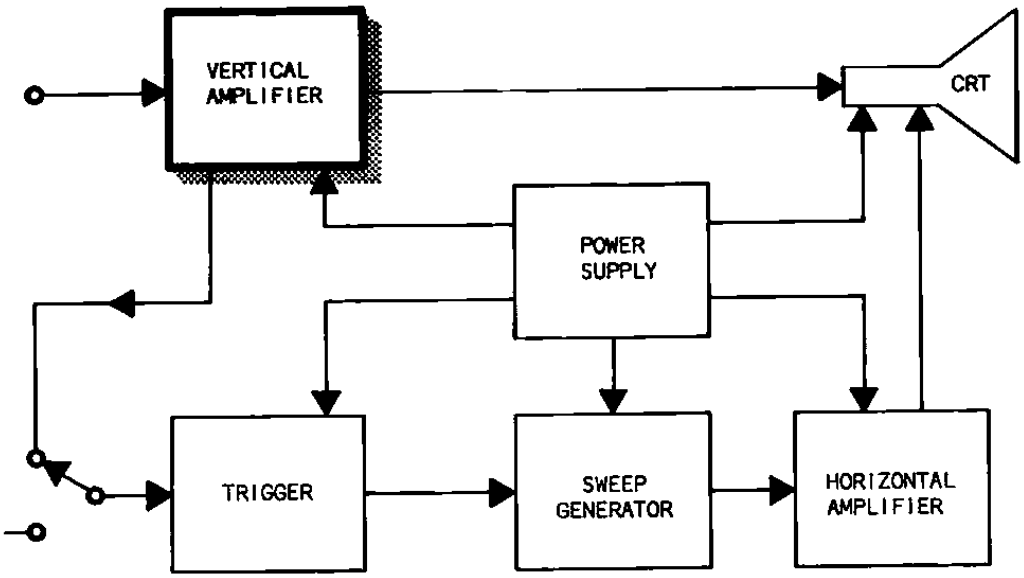

VERTICAL
AMPLIFIER
CRT
POWER
SUPPLY
TRIGGER
SWEEP
GENERATOR
HORIZONTAL
AMPLIFIER

1 INTRODUCTION

In a study of conventional oscilloscopes, the various circuits of the instrument fall into general groupings: the power supply, cathode-ray tube, trigger circuit, sweep generator, horizontal amplifier and the vertical amplifier.

Each performs an important function. Combinations of individual contributions determine instrument performance.

power supply

The *power* supply converts some form of available power (depending on the type and location of the instrument) to DC operating potentials for all the active circuits of the oscilloscope. Regulation holds most of these potentials to narrow tolerances, guaranteeing precise circuit performance. A power supply might also contain filament power for vacuum-tube circuits, overload protection and facilities for adapting the instrument to various local power conditions.

cathode-ray tube

The *cathode-ray tube* (CRT) displays light on a two-dimensional phosphor screen. It conveys intelligence in the form of alphanumerics, picture images or graphs. Graphical presentations offer an analytical approach: Actual measurements taken with a graticule along the “X” and “Y” screen axis.

The *CRT electron gun* is sealed inside an envelope. A vacuum minimizes collisions between free gas particles and the electron beam. High-voltage power supplies create controllable electrostatic fields which accelerate free electrons from the heated cathode to form an electron beam. The beam of electrons then transit an electron lens which converges or focuses the beam on a phosphor screen. When the high-velocity electrons collide with phosphor atoms at the focal point, photons of light emit towards the viewer.

Varying the electrostatic fields between a set of "X" and "Y" deflection plates positions the light source on the screen. Thus the electron beam creates a display anywhere within the viewing screen area. Since electrons have an extremely small mass, they can be deflected or scanned over the entire screen area millions of times per second. This permits the viewer to observe changing phenomena in real time.

The CRT must not unduly load either the vertical or horizontal amplifier nor require a greater dynamic-deflection range of voltage than the amplifiers can supply. In practice, the CRT and deflection amplifiers are designed together for maximum performance and efficiency.

trigger circuit

Input signals take a wide variety of shapes and amplitudes, many unsuitable as sweep-initiating triggers. For this reason a *trigger circuit* converts these signals to pulses of uniform amplitude and shape. This trigger circuit makes it possible to start the sweep with a pulse that has a constant size, eliminating variations of the sweep-circuit operation caused by changing input signals. The operator now uses either slope of the waveform to start the sweep, selects any voltage level on the rising or falling slope of the waveform, and, in some instances, eliminates selected frequencies of the input signal with ease and repeatability.

sweep generator

The *sweep generator* produces a sawtooth waveform for processing by the horizontal amplifier which then deflects the CRT beam. The sweep generator produces a sawtooth waveform, with the proper rate-of-rise, amplitude and linearity, suitable as a time-measuring reference.

horizontal amplifier

Primarily, the *horizontal amplifier* converts the time-base ramp, developed in the sweep generator, to deflection voltage for the horizontal CRT deflection plates. The resulting trace is the reference for Y-T displays (voltage plotted as a function of time). In those instruments offering X-Y capabilities (where both X and Y inputs are dependent variables) the horizontal amplifier reacts to the external (X) input as a linear amplifier. It exhibits a frequency response comparable to that of the vertical amplifier. Additionally, the horizontal amplifier provides DC-level and amplifier gain controls which permit positioning of the horizontal trace and sweep magnification (expansion) respectively. The latter facility extends instrument sweep speed without imposing additional sweep-rate requirements on the sweep generator.

vertical amplifier

The *vertical amplifier* determines the useful bandwidth and gain of the instrument. Vertical amplifiers take three general forms: a fixed vertical, a complete vertical in a plug-in form or a fixed main vertical amplifier preceded by a plug-in preamplifier. Selection of plug-ins allows a range of characteristics. An additional type of instrument takes the drive directly to the CRT plates without passing through *any* type of amplifier.

The general-purpose oscilloscope provides a faithful display of an input voltage. For meaningful results, displayed waveforms contain few aberrations and these but a few percent of the total waveform amplitude.

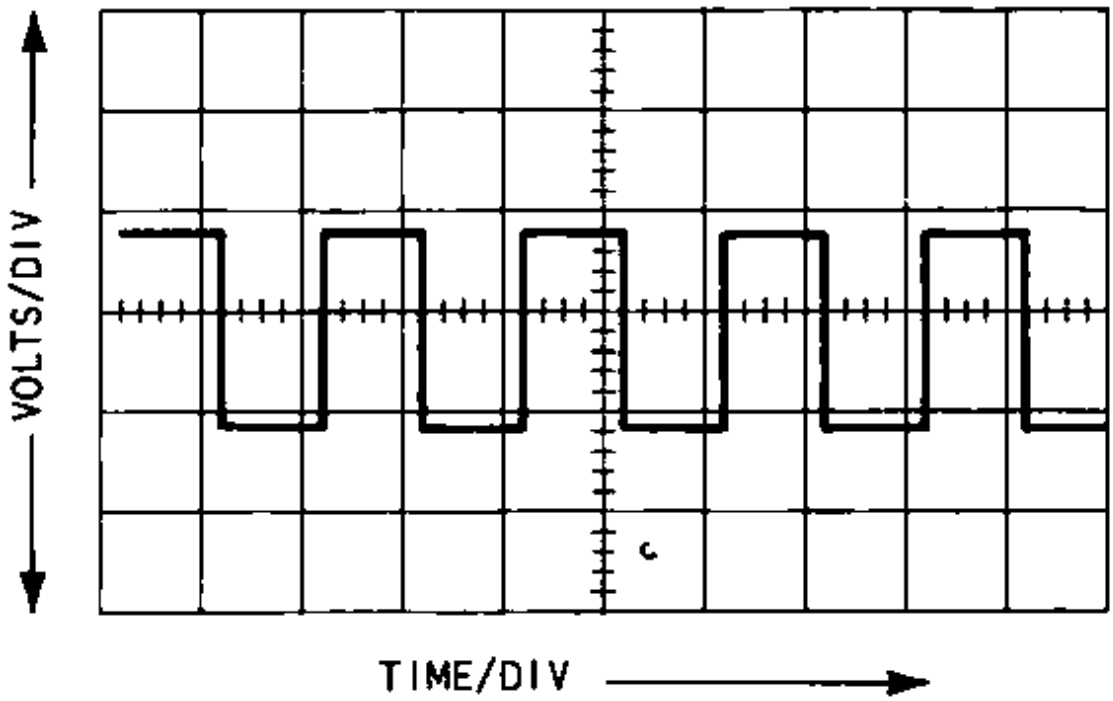


Fig. 1-1. Oscilloscope display.

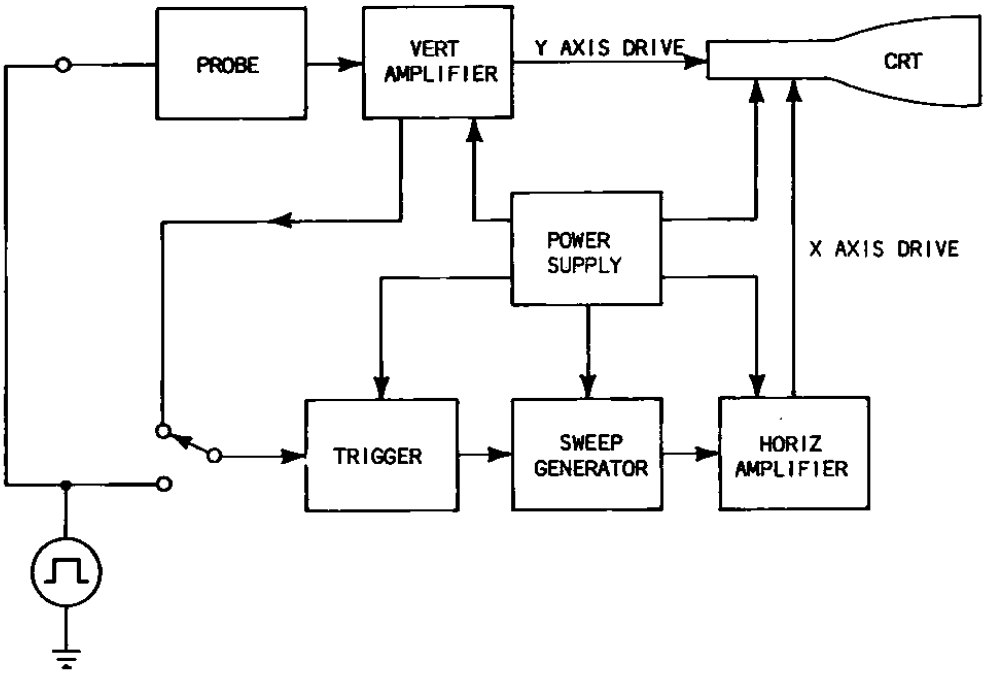


Fig. 1-2. Basic oscilloscope block diagram.

2 VERTICAL AMPLIFIERS

Vertical amplifiers meet requirements briefly summarized below:

1. Buffer the signal source (probe) and the CRT.
2. Provide various modes of operation such as: direct or AC coupling, multiple trace, and, perhaps, selectable differential modes.
3. Finally, the amplifier faithfully reproduces voltage waveforms within specified *risetime-bandwidth-amplitude* limits.

Why these items are important and how they are accomplished by Tektronix is what this book is about.

An oscilloscope graphically displays signals of interest, as shown in Fig. 1-1. Here periodic rectangular pulses appear superimposed on a grid graticulecalled the graticule. Equal divisions divide thegraticule X and Y axes. Fig. 1-1 shows ten major *horizontal (X)* divisions and six major *vertical (Y)* divisions. Small markings along the center lines describe minor division dimensions at 20% of a major division.

The horizontal base is calibrated in units of time per division; the vertical in units of voltage per division. For example, if each vertical increment is 0.5 volts and horizontal is 0.5 milliseconds per division, then Fig. 1-1 depicts a 1-volt pulse train with pulses recurring each milli-second.

Accurate information from *both* horizontal and vertical circuits creates faithful reproductions of the input waveforms. To accomplish this an oscilloscope generally requires the basic blocks shown in Fig. 1-2.

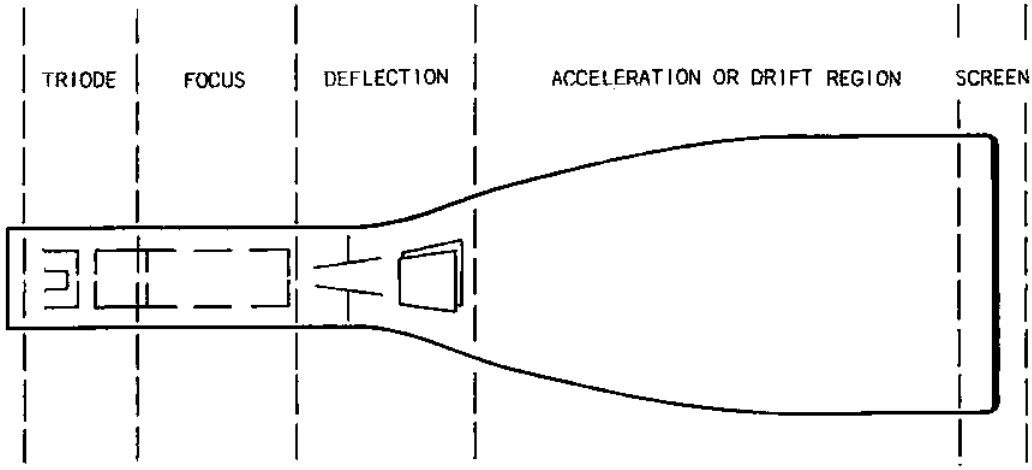


Fig. 1-3. CRT sections.

CRT

Cathode-ray tubes present a reactive load to deflection amplifiers. CRT construction and applied voltages cause a beam of the electrons, emitted by the CRT cathode, to form. The beam forms during electron travel from cathode to phosphor-coated faceplate. Energy contained in this concentrated mass of electrons striking the faceplate or screen is partially converted to light. Deflecting the beam vertically (Y) and horizontally (X) graphically reproduces waveforms. Deflection may be either electrostatic or electromagnetic. Since very few oscilloscopes use magnetic deflection, this book covers electrostatic deflection only.

Two pairs of plates mounted at right angles, as shown in Fig. 1-3, deflect the beam when energized. Leads from each plate penetrate the CRT envelope for connection to external excitation sources. The beam in the CRT shown passes first between the vertical deflection plates, then the horizontal.

A CRT and power supply alone function as a crude oscilloscope. Fig. 1-4 shows such an arrangement.

horizontal plates connect to Dl-D2 and vertical plates to D3-D4. D1, D2 and D4 connect to a common voltage, shown as ground. D3 connects to a signal source represented by the three-position switch. Applying zero volts to D3 centers the beam. Throwing the switch to +V attracts the beam toward D3. Repelling occurs with -V applied to D3.

Connecting either D1 or D2 to a signal source results in horizontal deflection.

A vertical deflection system like this one has one advantage -- simplicity. Unfortunately, there are disadvantages. Some are:

Low sensitivity.
Signal source loading.
Nonlinearity.

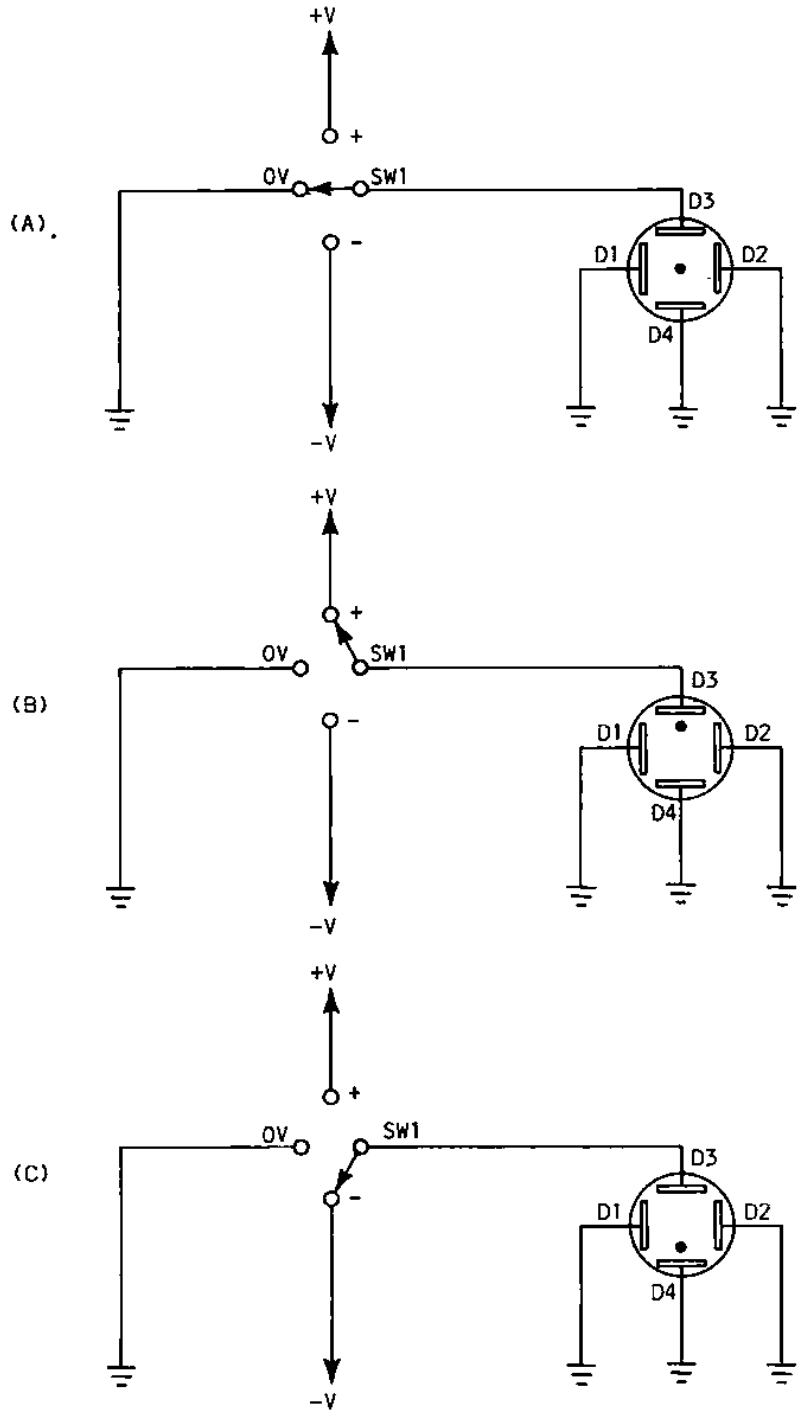


Fig. 1-4. A vertical system utilizing the CRT only.

deflection sensitivity

One needs a means of measuring deflection. Assume a vertical scale inscribed on the CRT faceplate. Scale increments begin at the center extending three divisions up and three divisions down. One needs to know the *deflection sensitivity* to calibrate the scale; i.e., how many scale divisions each volt deflects the electron beam. If divisions were scaled one centimeter apart (a representative dimension) the ratio cm/V expresses deflection sensitivity. 0.1 cm-per-volt represents a general deflection sensitivity. This restricts practical direct measurements to one volt minimum signal. Deflection sensitivity and screen diameter fix the maximum measurable level.

signal source and isolated

Inserting a probe and an amplifier increases deflection sensitivity and isolates signal source CRT. The deflection plates appear as capacitive circuit components. Connected directly this reactance might drastically change monitored circuit characteristics. The probe - vertical amplifier - CRT combination presents a high impedance to the circuit under test, allowing measurements to represent nominal circuit conditions. This vertical deflection system by including an amplifier implies voltage gain. Vertical amplifiers can increase deflection sensitivity. Further, the amplifiers contain calibrated step control of gain and attenuation extending input deflection sensitivity from, perhaps, 0.04 div/V to 100 div/V in several steps.

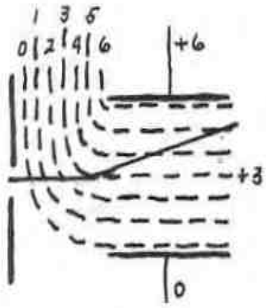
sensitivity improved

deflection factor

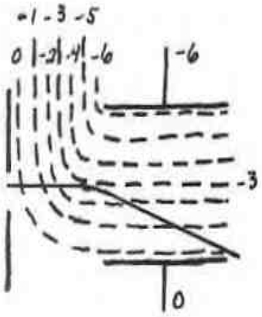
Division-per-volt terminology usually requires calculation for meaningful observations. Tektronix, therefore, uses *deflection factor* to conveniently express sensitivity. Deflection factor is the inverse of deflection sensitivity and is listed as volts-per-division (V/div): The CRT was earlier assigned a deflection sensitivity of 0.1 div/V. This is a deflection factor of 10 V/div. Including an amplifier increased vertical-deflection sensitivity to 100 div/V -- in terms of deflection factor, 10 mV/div. Rather than say the input sensitivity is selectable in eight steps from 0.04 div/V to 100 div/V, one states the steps, in terms of deflection factor, as from 25 V/div to 10 mV/div. Each observed division of CRT deflection now reads directly.

linearity improved

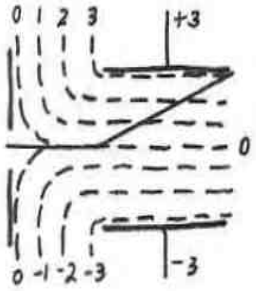
Almost all oscilloscopes use push-pull vertical and horizontal amplifiers. Push-pull CRT drive combats deflection nonlinearity. This is because single-ended drive develops a zero-volt equipotential surface near the grounded plate, while push-pull deflection centers the zero-volt equipotential surface between plates.



Consider a single-ended system with a positive signal voltage applied. An electron approaching the plates encounters positive equipotential surfaces; axial velocity therefore increases. Assume this results in two divisions of deflection above center.



Nonlinearity shows upon application of an equal-amplitude opposite-polarity signal. An electron now decelerates as it approaches the deflection plates due to negative equipotential surfaces encountered. The beam then deflects further below center, perhaps by one division, than in the case above. Nonlinearity to this degree is unacceptable.



Push-pull voltages applied to both Dl-D2 and D3-D4 eliminate nonlinearity of single-plate drive. Equal signal voltages of opposite polarity appear on the plates. Deflection voltage develops across the plates but the zero-volt equipotential surface remains centered between plates. An electron approaching the deflection plates encounters a surface approximating anode voltage. It then experiences neither acceleration nor deceleration. Deflection signals cause equal radial velocity either side of center.

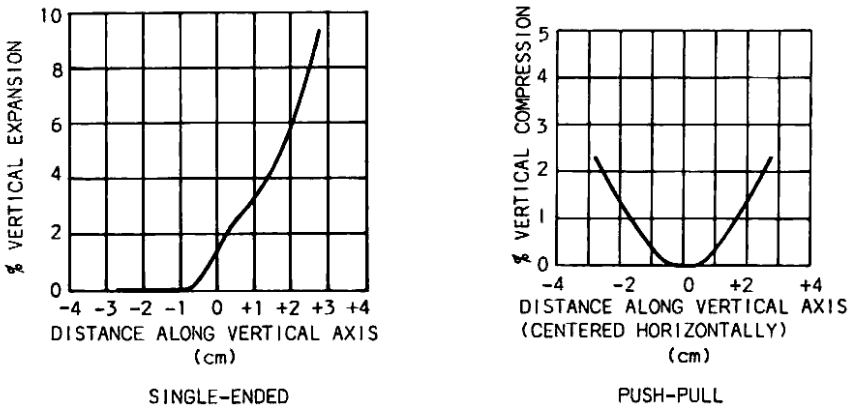


Fig. 1-5. Linearity comparison.

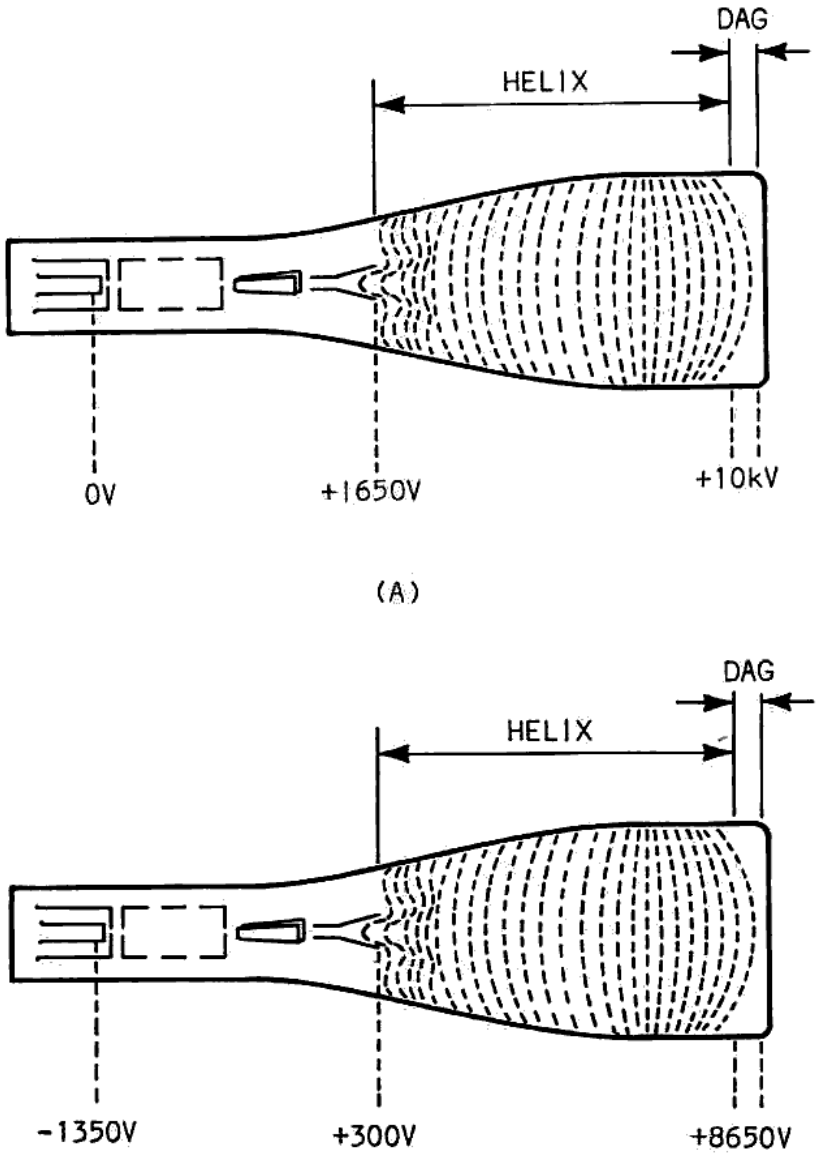


Fig. 1-6. Locating the deflection-plate voltage gradient (not to scale).

push-pull and single-ended linearity contrasted

Each type of CRT does exhibit characteristic nonlinearity. However, dramatic improvement results from push-pull drive. Compare the graphs of Fig. 1-5 to contrast the linearity between push-pull and single-ended deflection. These graphs are of the same tube type under nearly identical conditions.
Even the linearity characteristics vary between drives. Push-pull suffers a low percentage of compression; single-ended creates unacceptable expansion.

CRT design holds deflection-plate rest potential to specific limits. This calls for deflection amplifiers designed to operate around these levels.

The voltage gradient between CRT cathode and aquadag (dag) creates the restrictive deflection-plate operating levels. Fig. 1-6A is a cut-away CRT which includes the equipotential surfaces in the post-deflection-acceleration (PDA) region. Gradients develop between the cathode and the low-voltage end of the helix. The deflection plates set in an area bisected by the 1600-to-1700-volt equipotential surface. To prevent severe distortion of surfaces in the PDA region, external deflection-plate leads should connect to a voltage source equal to the internal voltage environment -- in this case between 1600 and 1700 volts. Deflection amplifiers driving these deflection plates maintain quiescent deflection-plate voltage 1600 to 1700 volts above the CRT cathode.

Operating amplifiers above 1.5 kV is a bit unreasonable. This among other reasons, is why operating voltages are as shown in Fig. 1-6B. Operating with the cathode below ground reduces the positive operating level, required by the deflection plates, to a reasonable value.

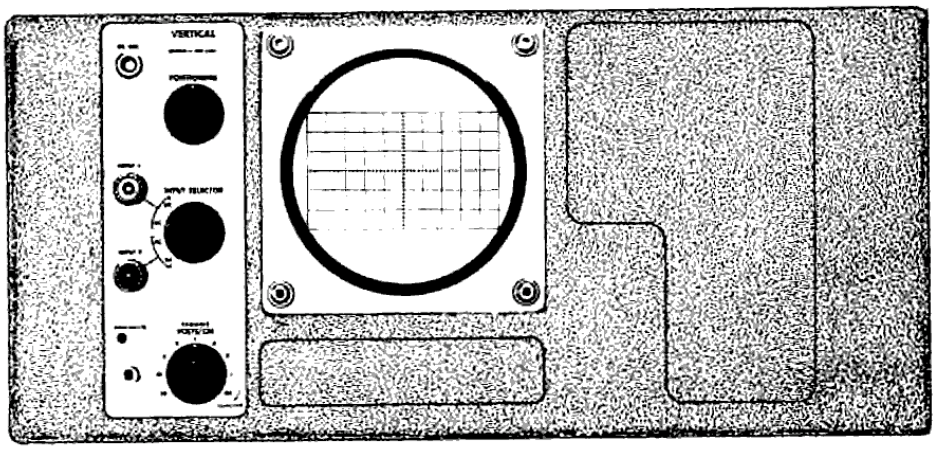
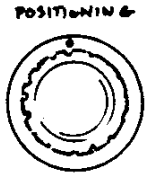


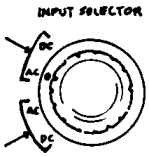
Fig. 1-7. Oscilloscope vertical controls.

operating controls

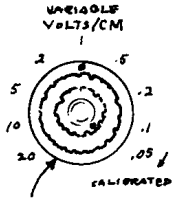
Fig. 1-7 is a representative oscilloscope with all controls, other than vertical, blanked out. The instrument illustrated includes basic front-panel vertical-amplifier controls: Vertical POSITION, INPUT SELECTOR, VOLTS/CM selector and the VARIABLE control.

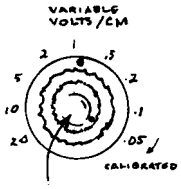


Adjusting the vertical-POSITION control moves the CRT display up and down along Y axis. Centering the vertical POSITION and restricting the input to zero volts centers the vertical CRT display.



The INPUT SELECTOR allows the operator to choose either of two input connectors. It further extends his choice to a direct connection (DC) or capacitive coupling (AC) from input connector to vertical amplifier.





VOLTS/CM and VARIABLE mount on concentric shafts. The VOLTS/CM selector is shown as an input deflection-factor selector. One selects, in nine calibrated steps, input deflection factors between 0.05 V/cm and 20 V/cm. This is the deflection factor at the input connectors. The continuously adjustable VARIABLE provides between-step, uncalibrated, deflection-factor control: With the VOLTS/CM set to 1, the VARIABLE may set input deflection factor at any point between 1 V/cm and approximately 2 V/cm. This control slips into a detent at the extreme clockwise position allowing calibrated input deflection factor. Placing the VARIABLE in detent, one reads deflection factor as indicated by the VOLTS/CM selector. These controls and connectors are a part of circuits generally located in the *vertical preamplifier.*

vertical preamplifier

Subdividing vertical amplifiers into preamplifiersand main amplifiers helps simplify concept development. Two tests separate vertical preamplifiers and main vertical amplifiers: (1) Circuits which contain front-panel controls most commonly occur in preamplifiers, and (2) a vertical circuit into which a connector could be inserted to allow preamplifier plug-in capability is a main amplifier.

main vertical amplifier

The *main-vertical-amplifier* tag evolved from main-frame vertical amplifier. The advent of plug-incapability required a vertical-amplifier separation -- one portion removable and the other a permanent part of the oscilloscope *main frame,* thus the tag: *main frame* vertical. Common usage shortened the name by dropping "frame."

The vertical preamplifier acts upon signals appearing at the input connector. It then converts the signal to push-pull. Vertical preamps also provide gain as selected with the volts-per-division selector. Preamplifier gain is that necessary to provide a constant deflection factor at the preamplifier output. A push-pull signal of 100 millivolts-per-division is representative. The main vertical amplifier then is a push-pull amplifier of fixed gain. Amplification is as needed to match the constant input deflection factor to that of the CRT. An internal gain calibration frequently constitutes a part of the main vertical amplifier.

gain

$Av = \frac{V_0}{V_{in}}$

$Av = \frac{DF_0}{DF_{in}}$

Gain in this book refers to voltage gain. Since oscilloscope vertical amplifiers are basically voltage-actuated devices, gain in terms other than voltage has Av = little direct meaning. A simple expression, output voltage divided by input voltage, defines voltage gain. Substitute deflection factors for voltages in the gain ratio to determine required amplifier gain. *As* an example, assume the CRT deflection factor is 20 V/div and the VOLTS/DIV selector sets at 1 V/div. Ratio $\frac{20\ V/div}{1\ V/div}$ expresses the required vertical-amplifier gain. Overall vertical-amplifier gain may be unity, less than unity or greater than unity.

One seldom refers to gain directly when describing the characteristics of a vertical amplifier. He does describe input deflection factor such as: the VOLTS/DIV selector of Fig. 1-7 allows selection of input deflection factors between 0.05 VOLTS/DIV and 20 VOLTS/DIV or, as used earlier, as an expression of amplifier sensitivity. This partially describes the limits or capabilities of the instrument.

bandwidth

Bandwidth expands oscilloscope descriptions. Bandwidth, applied to a specific vertical amplifier, defines the frequency limits of calibrated input deflection factors. That is, a one-volt input signal, to a vertical amplifier set at one volt-per-division input deflection factor, deflects the CRT one division *only* if the signal frequency is within the capabilities of the vertical amplifier. Oscilloscope bandwidth specifications express frequency capabilities of the vertical amplifiers.

One type of Tektronix instrument is advertised as a DC-to-10 MHz oscilloscope. In the same advertisement, under vertical characteristic summary: bandwidth DC-coupled, DC. to 10 MHz. AC-coupled, 2 Hz to 10 MHz. This specification should have the same meaning to everyone.

However, an oscilloscope vertical amplifier must also be capable of faithfully reproducing complex waveshapes, and *this requires good transient response characteristics. Stated another way, we need to have a linear phase-versus-frequency response.*

bandwidth plot

Fig. 1-8 graphically shows the described bandwidth. One constructs a graph of this type by applying, to the vertical amplifier input, signals of varying frequency but constant amplitude. He then plots displayed amplitude versus input frequency. The solid line of Fig. 1-8 represents a bandwidth of DC-to-10 MHz. Displayed signal voltage remains essentially the same between 0 Hz (DC) and 1 MHz.

Refer to this as 0-dB attenuation. As the input frequency increases (input voltage held constant) the displayed signal amplitude decreases, reaching 70.7% of zero-hertz (DC) voltage at 10 MHz.

upper-frequency limit

Refer to this point as 3-dB attenuation. The upper- and lower-frequency 3-dB-down points define bandwidth. No lower-frequency 3-dB point appears

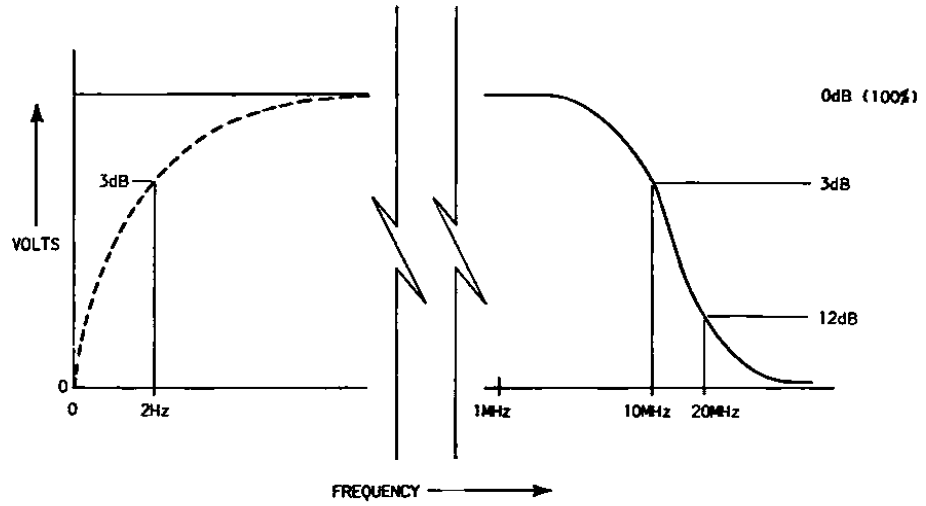


Fig. 1-8. Bandwidth curve.

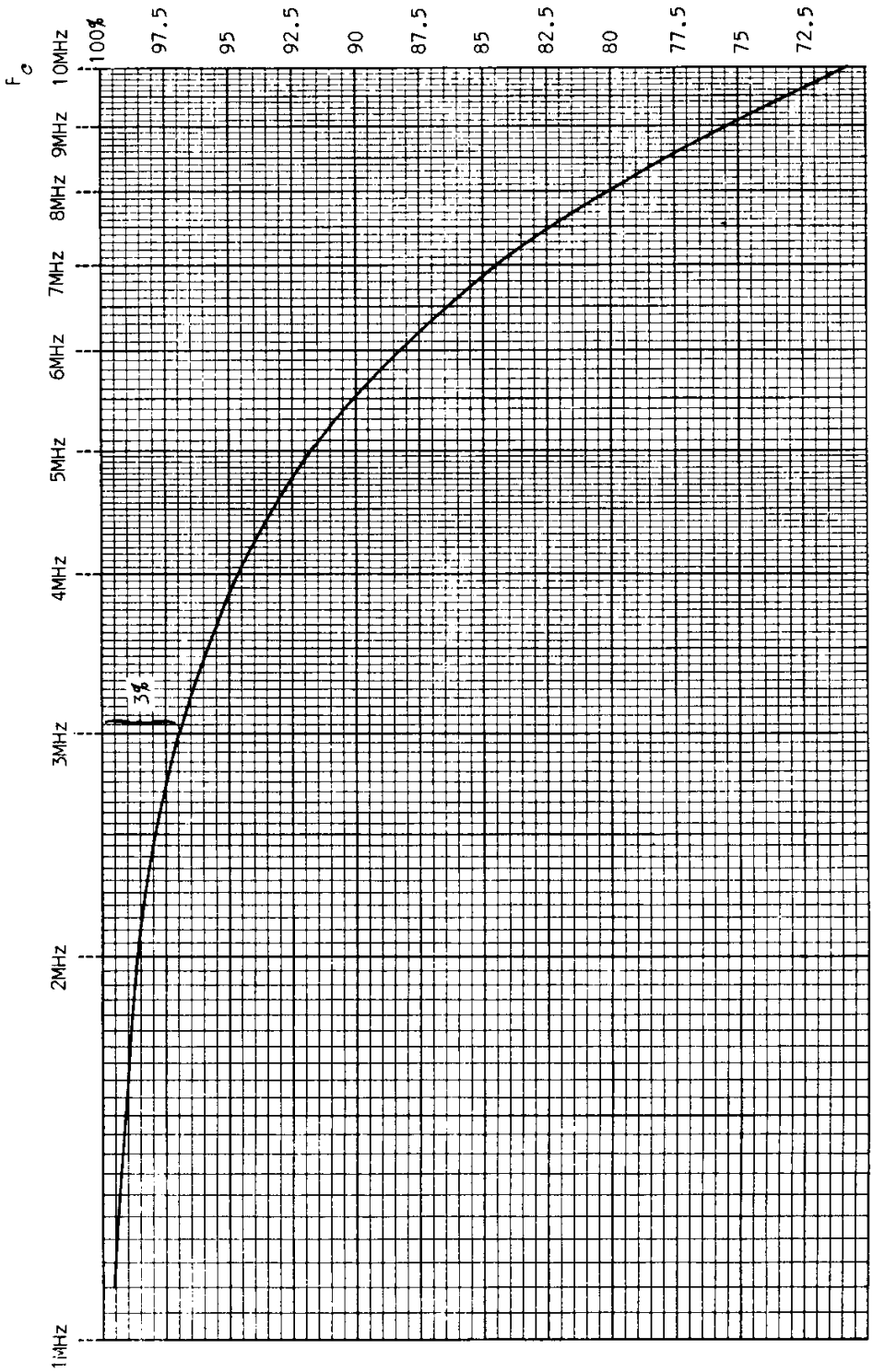


Fig. 1-9. Expanded frequency curve.

Fig. 1-9. Expanded frequency curve.

on the solid line graph. This is characteristic of direct-coupled instruments. Thus, one frequently refers only to the upper-frequency limitation: "This is a ten-megahertz scope."

lower-frequency limit

A precise description of an AC-coupled instrument must include the lower-frequency 3-dB point. The dotted line on Fig. 1-8 follows the slope of low-frequency response. 3-dB attenuation occurs at 2 Hz. Midfrequency and high frequency remain as for direct-coupling. 2 Hz is a low frequency and the majority of general-purpose oscilloscopes must respond to DC. Therefore, the upper 3-dB-down frequency (F0) receives greatest attention.

The bandwidth curve of Fig. 1-8 has neither square corners, nor does it actually achieve a flat top. Beginning at the lower (2 Hz) 3-dB point, the curve ascends from 70% of maximum to exceed 99% at 20 Hz. Response continues to ascend until reaching maximum, then descends again dropping to 99.5% at 1 MHz. Fig. 1-9 expands the upper frequency portion of the curve between 1 MHz and 10 MHz. This curve

measurement errors

indicates that one experiences voltage *display* errors of discrete frequencies above 1 MHz: 0.5% at 1 MHz, 1.5% at 2 MHz, 5.5% at 4 MHz, 12% at 6 MHz, 20% at 8 MHz and 30% at 10 MHz (F0). This is why some use the "thumb rule of 5:" That the scope bandwidth should exceed the highest frequency to be measured by five. The error at 20% of cutoff (Fc) is less than 2%. If one were satisfied with a 3% display error he could economize by using a scope whose F_0 exceeded maximum measurement needs by 3.

Incidentally, the curve of Fig. 1-9 applies to most oscilloscopes. One need only apply Fc to the upper 3-dB point of his instrument and assign percentage values to the listed frequencies: 8 MHz is 80% of F*c* , **6** MHz is 60% of F. . . .and 1 MHz is 10% of F Using the chart to correct for display errors gives an accurate amplitude measurement of sinewaves.

One might wonder why he pays for frequency response he is not using. Why not provide him with a scope with a flat response between frequencies which then drops abruptly to zero? This would give him accurate displays within the specified frequencies and reject all frequencies above and below these limits.

Actually he uses all of the bandwidth he buys. The proposed abrupt response considers only frequency not time delay or phase shift. Phase relationships come into play during reproduction of nonsinusoidal waveforms. Even persons concentrating exclusively on frequency domain areas seldom, if ever, encounter a pure sinewave. An aberration of interest or a circuit distortion, such as clipping, creates complex waveforms. Accurate display of these waveforms depends upon vertical-amplifier phase-gain characteristics.

squarewave evaluation

One method of performance evaluation applies periodic rectangular waveshapes (squarewaves) to the vertical-amplifier input. This allows one to demonstrate frequency and phase response of a vertical system.

transient voltage

Fig. 1-10 shows three cycles of a periodic rectangular wave. There are two theoretical methods of constructing a squarewave: the voltage and the sinewave method. In terms of transient-voltage method, the voltage of Fig. 1-10 remains set from T_0 to T_1 at -2 volts; changes abruptly at T_1 to +2 volts; remains at +2 volts until T_2 suddenly changes to -2 volts; the level remains at -2 volts until T_3, and so on.

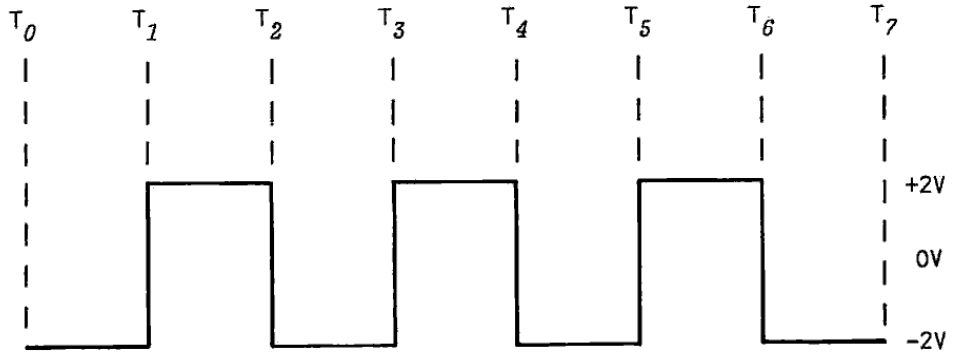


Fig. 1-10. Squarewaves.

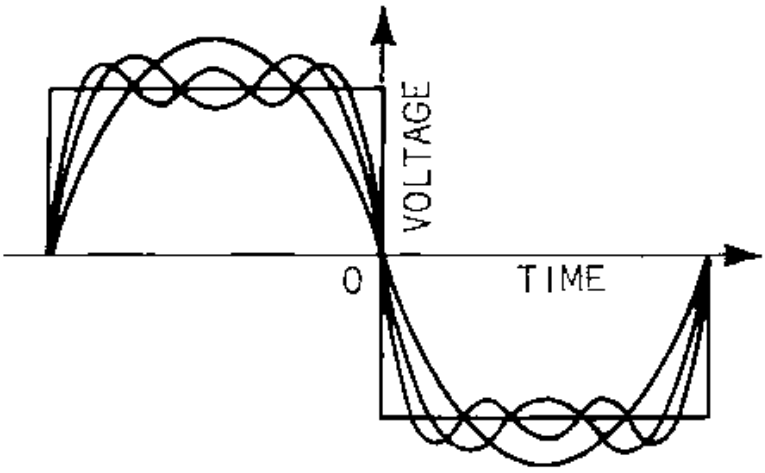
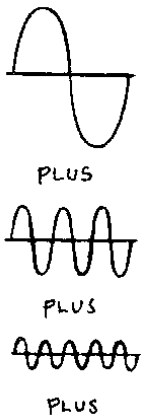


Fig. 1-11. The addition of successively higher-order harmonics to a fundamental sinewave to produce a close approximation of a squarewave.

frequency components

The sinewave method follows the assumption that a squarewave contains a number of frequencies. Fig. 1-11 shows the reproduction of a symmetrical squarewave. It shows three frequency summations superimposed on an "ideal" squarewave. First the fundamental sinewave establishes the basic rate. Next the third harmonic algebraically adds to the fundamental. Finally, the fifth harmonic adds to the waveform resulting from the first and third. This waveform only begins to resemble a squarewave. The corners are rounded and the top is not flat. Each additional harmonic sharpens the corners and flattens the top.



These harmonics bear both proper phase and amplitude relationship. As the fundamental frequency begins in a positive direction, all harmonics must also ascend. And at the completion of one fundamental cycle, as the fundamental intercepts zero amplitude from the negative, so must all harmonics. The fundamental completed 360°; the 3rd harmonic, 1080°; the 5th, 1800°; and so on through the odd-order harmonics.

Amplitude relationships must also be maintained. The 3rd harmonic is 1/3 of fundamental amplitude, the 5th is 1/5 and so on . . . .

A squarewave allows one to evaluate vertical amplifiers. For example, assume a "perfect" squarewave input appears on the CRT with rounded corners. Fourier analysis predicts higher harmonics sharpen the corners, therefore, the vertical amplifier suffers high-frequency attenuation.

waveform contains frequency information

Fig.1-12 locates frequency information on one pulse. Notice that both the corners and vertical pulse excursions contain high-frequency information. Notice also the rounded pulse corners and vertical slopes. Properly extending an amplifier's frequency response preserves pulse corners, vertical slopes and "flat" tops.

time domain

Time-domain studies are concerned with the transit time from one voltage level to another. When discussing time-domain methods one encounters the term *step function.* This waveform results when a voltage "steps" from one level to another. Fig. 1-13 illustrates the two forms of the step function. In Fig. 1-13A the voltage sets at a level then abruptly changes to and remains at a more positive level. Fig. 1-13B illustrates a transit to a more negative voltage. Both figures imply a single change in voltage.

time function

pulses as step functions

Repetitive signals are generally more practical than single events. Thus, one finds periodic rectangular pulses used as step functions. Fig. 1-14 shows such a pulse. To consider pulses as step functions, pulse duration must be long compared to voltage level transit time.

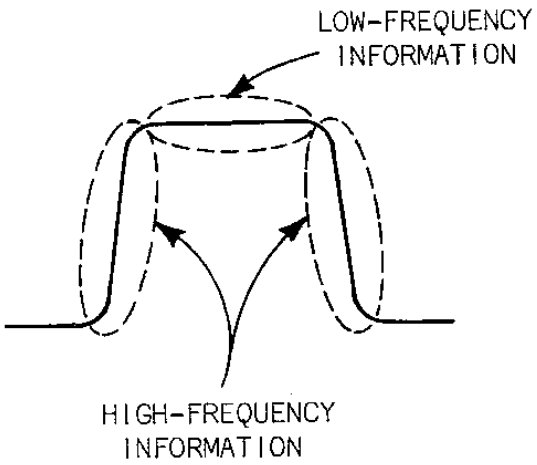


Fig. 1-12. A summary of the low- and high-frequency information found in a squarewave.

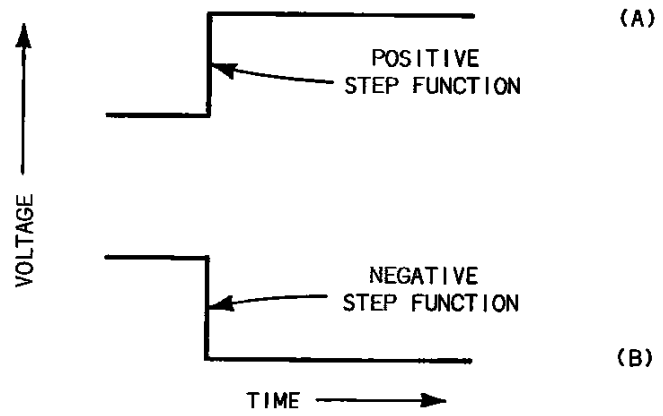


Fig. 1-13. Positive-going and negative-going step functions.

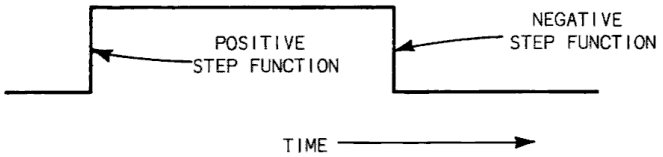


Fig. 1-14. Positive and negative step functions.

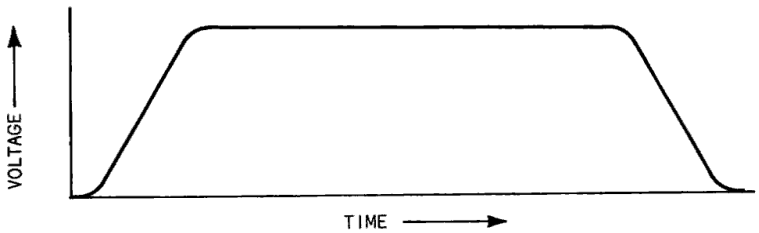


Fig. 1-15. Pulse shape.

How well vertical amplifiers reproduce ideal step functions is a measure of performance. Step functions of Fig. 1-14 are ideal, voltage transition occurs in zero time. Applying the "ideal" step to a vertical amplifier results in a display having rounded corners and a slope to voltage excursions. Fig. 1-15 shows such a response.

risetime

The term *risetime* refers to voltage-level transition time. Risetime applies to either positive or negative step response. However, a displayed falltime negative excursion is popularly termed *falltime.*

One measures risetime along a portion of the slope only. Initial and final portions of an excursion make close measurement arbitrary, at best. Risetime refers to only the middle 80% of a step function. Fig. 1-16 illustrates proper oscilloscope risetime measurement. This figure indicates risetime as the transit time between 10% of maximum voltage and 90% of maximum voltage.

2.2 RC

Applying a step function to an RC network results in risetime dependent upon network time constant. The leading edge follows an RC curve, such as shown in Fig. 1-17. Risetime resolves to 2.2 RC: 10% of maximum occurs in 0.1 RC and 90% in 2.3 RC, the difference is 2.2 RC.

$$\text{Risetime } (t_r) = 2.2\ RC.$$

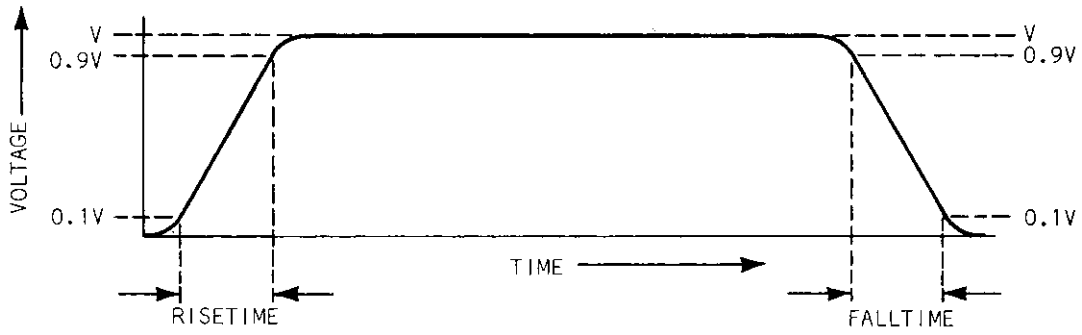


Fig. 1-16. Pulse measurement.

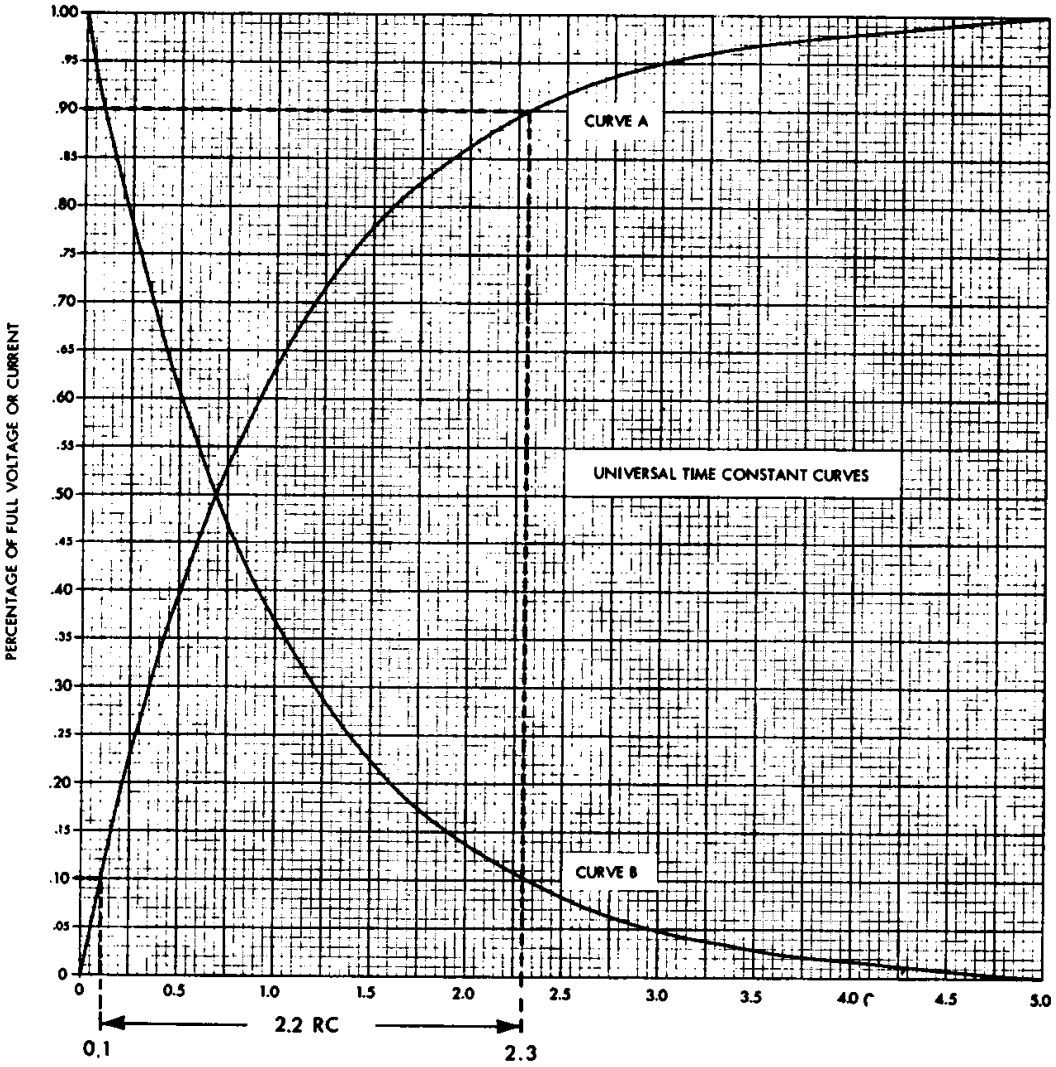

PERCENTAGE OF FULL VOLTAGE OR CURRENT
1.00
.95
.90
.85
.80
.75
.70
.65
.60
.55
.50
.45
.40
.35
.30
.25
.20
.15
.10
.05
0
0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
CURVE A
UNIVERSAL TIME CONSTANT CURVES
CURVE B
2.2 RC
0.1
2.3

Fig. 1-17.

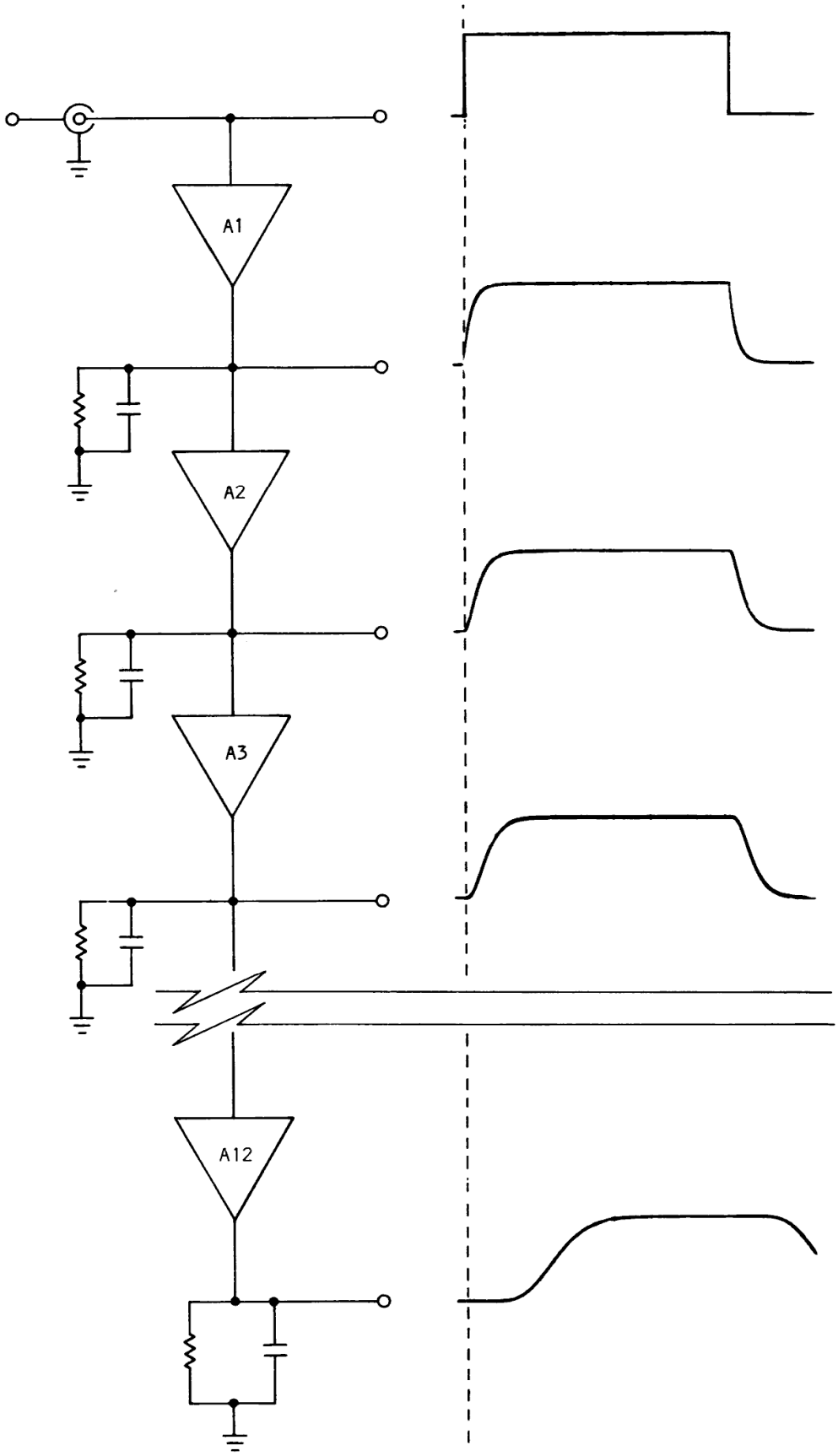


Fig. 1-18. Cascaded RC amplifier response to an ideal step.

A solitary RC circuit response is fairly easy to visualize. But, how does a cascade of RC amplifiers react to an approximation of the ideal step?

Ultimate risetime occurs later, rises slower and assumes a new shape. Fig. 1-18 shows these effects. Consider each amplifier increment:

Input The amplifier input step has zero rise-time, both 10% and 90% points occur at T0.

A1 Output risetime follows the curve of a universal time constant. Risetime increases and a small delay occurs. The step reaches 10% at 0.1 RC ascending to 90% 2.2 RC later. This is the input to A2.

A2 A2 receives an input with a varying change-of-voltage-per-unit-time. The output, developing across an RC network, ascends to 10% at a different slope rate. A small curve develops.
A greater time also lapses between 10% and 90%.

A3 The 10% point here occurs still later and risetime (t_r) again increases. At this output the curve between minimum amplitude and 10% begins to resemble the curve between 90% and maximum amplitude. This condition continues with each stage contributing an increase in time delay and risetime. And with each stage the upper and lower step halves approach mirror-image shapes. After an infinite number of stages the step in fact assumes a mirror-image shape.

A12 Here there is a considerable delay between T_0 and the 10% point. Risetime has noticeably increased and response appears to be symmetrical about the 50% point. The curve between minimum and 10% approximates the curve between 90% and maximum. This approximates a gaussian step response.

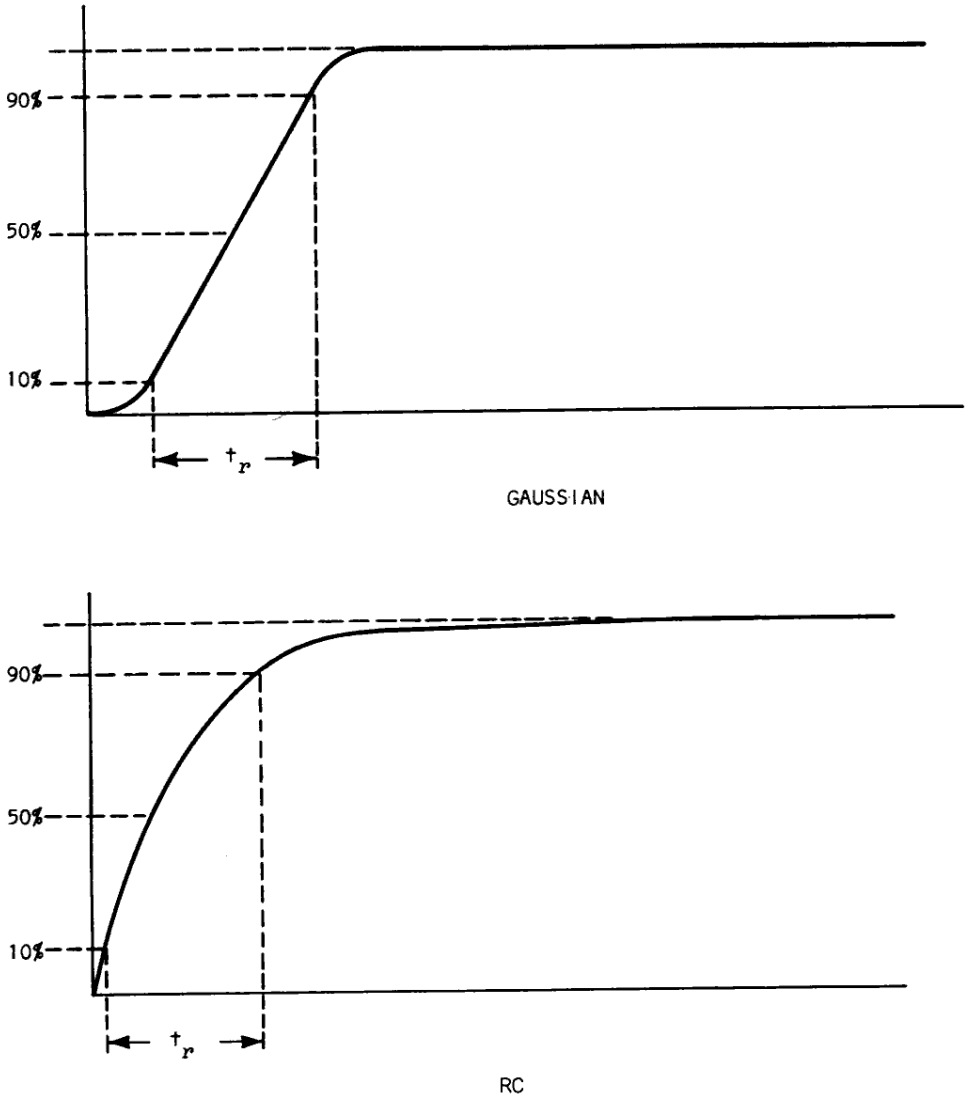


Fig. 1-19. Step response.

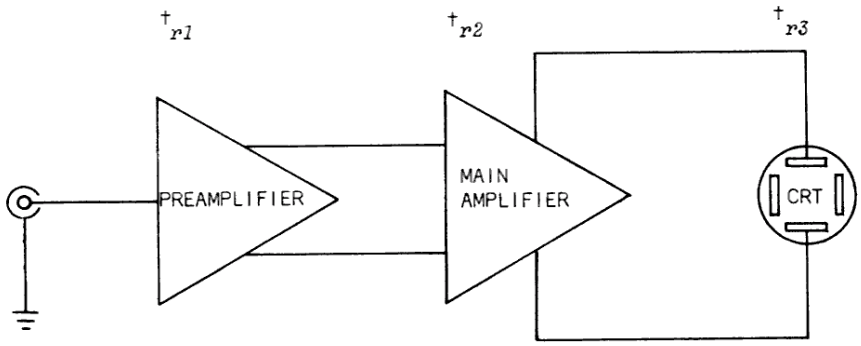


Fig. 1-20. System risetime results from individual amplifier risetimes:
$t_r^2 = t_{r1}^2 + t_{r2}^2 + t_{r3}^2$

Fig. 1-19 compares a gaussian and an RC step response of equal risetime. The RC step rises abruptly, at an almost linear rate, from zero to 10%. Rate of rise then changes, requiring as much time from 90% to 99% as from zero to 90%.

On the other hand, gaussian responses rise from zero to 10% more slowly, assuming an almost linear slope between 10% and 90%, then ascend the last 10% in a curve equal to the first 10%.

Oscilloscope vertical-amplifier step response, except for a few specialized types, falls between the RC and the gaussian. Gaussian responses receive more detailed treatment later. For now, realize that a *true* gaussian amplifier is impossible. Vertical amplifiers do, however, very closely approach a gaussian response.

When an ideal step function passes through amplifiers in cascade, each amplifier contributes to risetime deterioration in a predictable manner. Fig. 1-18 showed this pictorially but failed in indicating predictability. Refer to Fig. 1-20 and assume the following conditions: An ideal step-function applied to a vertical input passes through two cascaded amplifiers and is displayed on a CRT. One predicts displayed risetime by applying the formula:

$$t_r = \sqrt{t_{r1}^2 + t_{r2}^2 + t_{r3}^2}$$

where:

tr = displayed risetime of the amplifiers and CRT.

tr1 = risetime of the preamplifier operating alone.

tr2 = risetime of the main amplifier alone.

tr3 = CRT risetime.

For example, assign values:
t_{r1} = 3 microseconds
t_{r2} = 4 microseconds
t_{r3} = 10 nanoseconds

$$t_r^2 = (3 \times 10^{-6})^2 + (4 \times 10^{-6})^2 + (10 \times 10^{-9})^2$$
$$\approx (9 + 16)10^{-12}$$
$$t_r = \sqrt{25 \times 10^{-12}} = 5 \times 10^{-6} \text{ seconds}$$

Displayed risetime resulting from an ideal step function is about 5.0 microseconds.

vertical risetime must be less than test device

One now might ask, how can an oscilloscope user measure risetime? To do so the oscilloscope vertical amplifier must have a risetime much less than the device being measured. Suppose one wishes to display a given waveform. He also requires the displayed waveform to be within 2% of the input test device waveform. Fig. 1-21 indicates oscilloscope performance for the required result. For example, 2% (Y axis) intercepts the graph slope at the ratio of 5 (X axis). This tells an operator that to observe a 50-nanosecond risetime waveform, with 2% accuracy, his oscilloscope must have 10-nanoseconds risetime or less.

Fig. 1-21 was calculated from the square root of the sum of the squares equation. A modification of this formula allows one to determine true risetime of a circuit under test:

$$t_{rA}^2 = t_{rg}^2 - t_{rd}^2 - t_{rO}^2$$

where:
t_rA = Amplifier risetime (amplifier under test).
t_rd = Displayed risetime.
t_rg = Risetime of the squarewave generator (or other source).
t_r0 = Oscilloscope vertical-amplifier risetime.

Using these calculations one moves from "ideal" restrictions to reality. Fig. 1-22 shows a possible condition. A squarewave generator develops the step function with risetime, trg. The amplifier under test increases risetime as does the vertical-amplifier system. All devices contribute to risetime displayed, trd. Thus an operator must know the risetime of the step-function source and his oscilloscope *from the probe tip.* He then substitutes the known and measured values into the formula for true risetime of the amplifier under test.

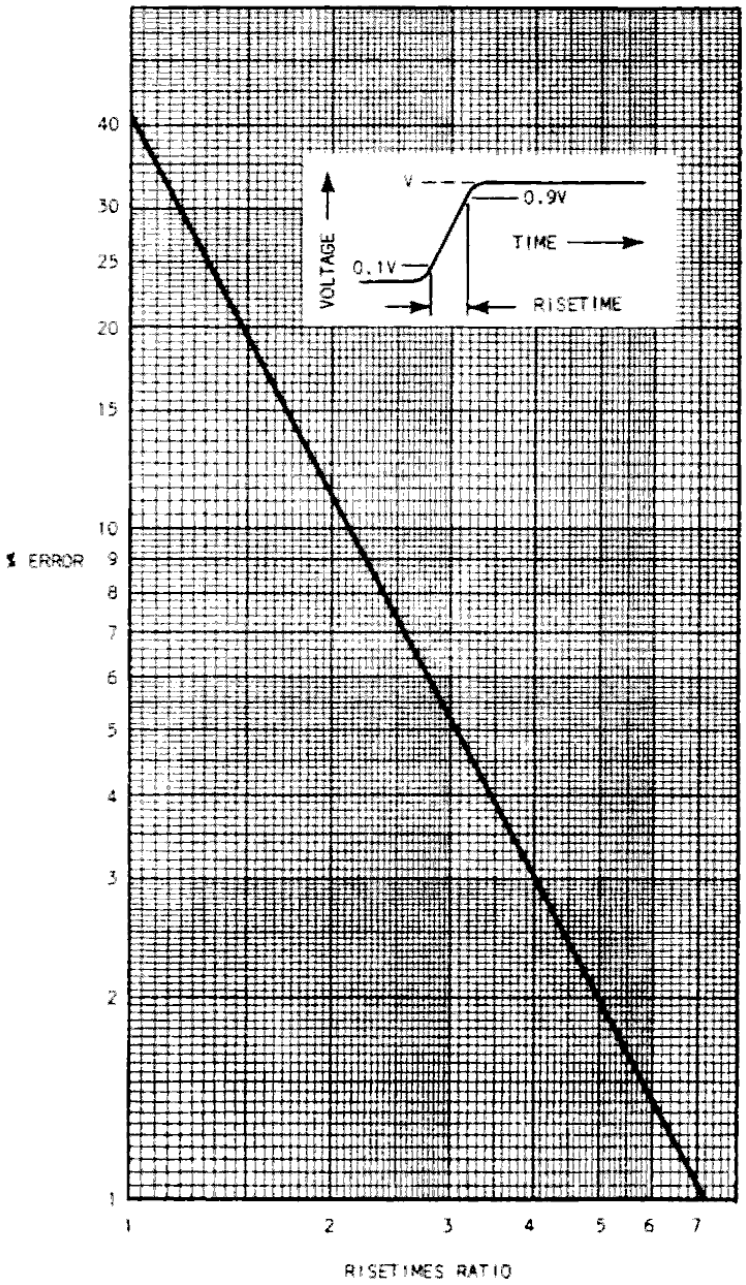


Fig. 1-21. Percent error in risetime measurement (Y axis) plotted against ratio of input waveform risetime to oscilloscope risetime (X axis).

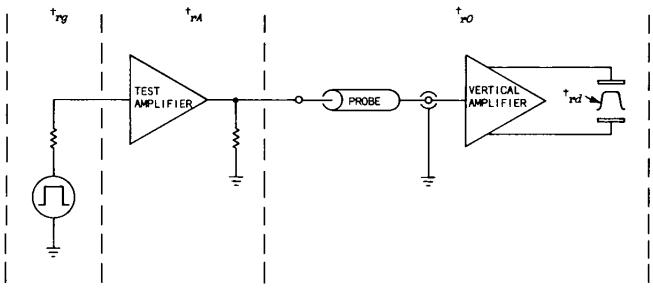


Fig. 1-22. Factors determining actual

risetimeof a circuit under test.

One note of caution about oscilloscope risetime. One Tektronix oscilloscope type, specified at 7 ns, actually meets a performance of 6 ns or better when it leaves the factory. On the other hand, instrument risetime can be considerably degraded without user awareness. Whether due to conservative pecifications or eroded performance, the calculat-ions may be in error. Measure your instrument performance.

Vertical amplifiers have so far been considered fromtwo standpoints, risetime and bandwidth. A definite relationship exists between risetime and bandwidth.

risetime-bandwidth product

This is expressed as a constant, *K,* equal to the risetime-bandwidth product: tr • bw = *K*. *K* = 0.35 in the case of RC amplifiers. *K* results from a combination of the risetime formula and the -3 dB frequency formula:

$$t_r = 2.2\ RC$$

and

$$F_c = \frac{1}{2\pi RC} \quad \text{or} \quad RC = \frac{1}{2\pi F_c}$$

substituting,

$$t_r = 2.2\left(\frac{1}{2\pi F_c}\right) = \frac{2.2}{2\pi F_c} = \frac{0.35}{F_c}$$

$$t_r F_c = 0.35$$

If one considers F0 as bandwidth then:

$$tr \cdot bw = 0.35$$

The above derivations apply only to an amplifier whose bandwidth is RC limited. Cascading a number of such amplifiers or proper compensation in a single-stage amplifier results in an essentially gaussian response. In this case the risetime-bandwidth product also partially describes the amplifier.

gaussian circuit

A *true* gaussian response resolves to tr • bw = 0.32. Because of several factors oscilloscope amplifiers don't meet the requirement for *true* gaussian res-ponse. "Gaussian" circuits are thus essentially gaussian. Empirical products, arrived at through years of research, define these "gaussian" circuits. For a gaussian response, tr • bw = 0.35 to 0.45. Higher products indicate least risetime. However, overshoot

accompanies the risetime reduction. A product of 0.45 results in about 5% overshoot and when tr • bw = 0.35 there is little, if any, overshoot in the step response. Tektronix usually establishes the product at *K* = 0.35, sacrificing risetime for minimum overshoot.

Fig. 1-23 compares *relative* bandwidth rolloff to step response. The bandwidth rolloff of Fig. 1-23A approximates gaussian. Step response, symmetrical about the 50% point, exhibits fastest rise *without* overshoot.

overshoot

Overshoot appears in Fig. 1-23B. In this figure upper frequency response falls off too steeply to be gaussian. Step response rises above then returns to 100% voltage level. This is called overshoot. Frequently associated with overshoot, a damped

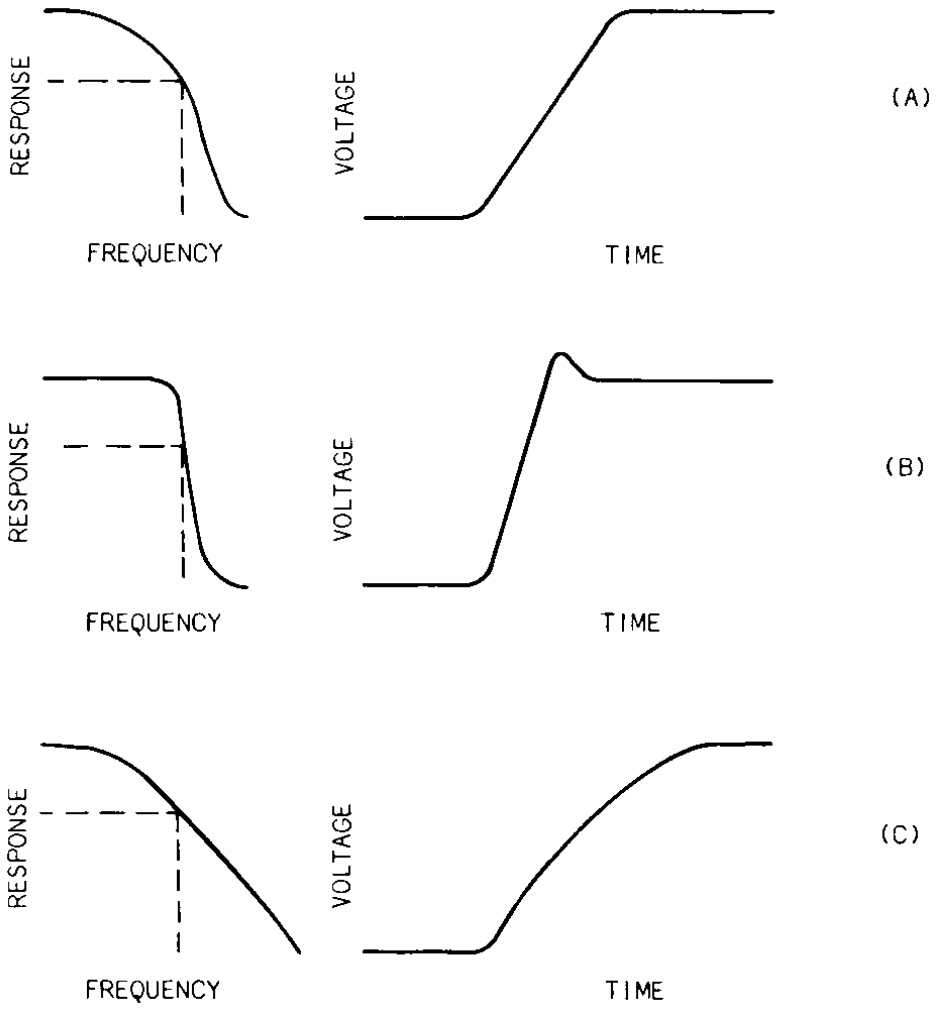


Fig. 1-23. Bandwidth versus frequency

oscillation may appear along the top of the wave. A few percent overshoot can represent an acceptable level when optimizing a system for least risetime.

slow rise

In Fig. 1-23C, the frequency-response curve falls off too slowly. The corresponding step responsetakes undue transit time.

phase shift linear

The gaussian rolloff expresses step-function response because of frequency-phase relationships. A circuit must impose two related phase characteristics for optimum step response: A linear shift with frequency or all frequencies equally delayed. Reactive components which attenuate also affect a phase shift. Impedances with gaussian attenuation shift phases linearly with frequency.

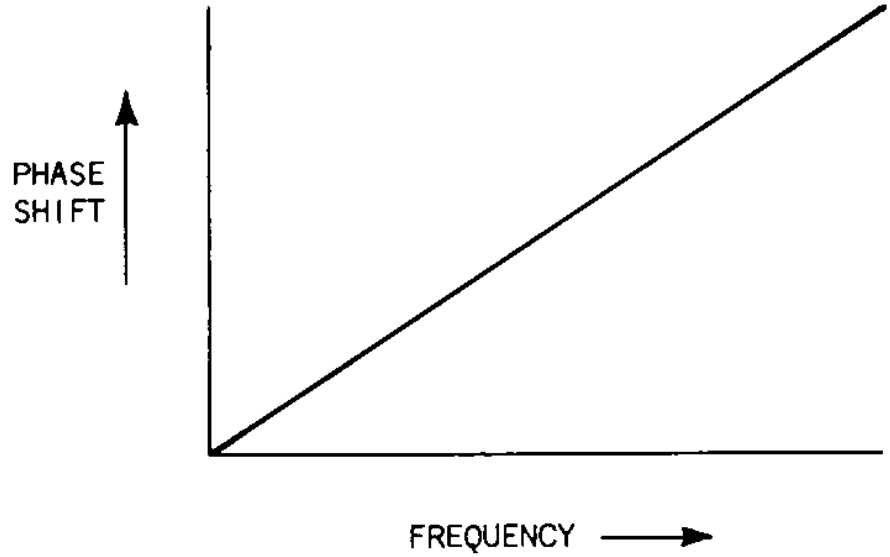


Fig. 1-24. Phase shift linear with frequency.

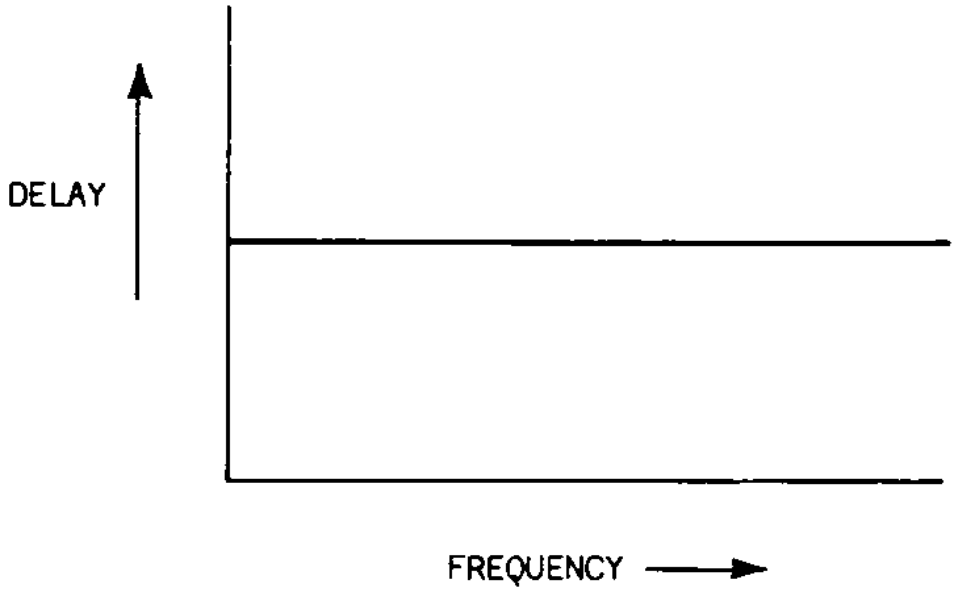


Fig. 1-25. Delay constant with frequency.

group delay

Fig. 1-24 shows phase shift-frequency relationship necessary for gaussian response. For optimum step response all frequency components must be equally delayed (Fig. 1-25). In other words, the frequency components of a pulse transiting a gaussian network experience phase shift increasing linearly with frequency. Also, all pulse-forming frequencies arrive at the termination simultaneously.

Now that a vocabulary has been established, a much more compact statement will summarize the amplifier description. Completely describing a linear amplifier by means of steady-state sinewave testing requires two plots:

1. Amplitude versus frequency, and,

2. Phase versus frequency.

Theoretically, given the amplitude and phase characteristics, one can calculate step response.

The most common input for amplifier testing is the step signal. This describes a linear amplifier by means of the time response to any input signal. Complete step response contains all of the information that amplitude and phase plots contain.

Theoretically, given a complete step response one can calculate the amplitude and phase characteristic. The tool used to deduce one information set from the other is the Fourier transform. Frequency response (amplitude and phase versus frequency) is the Fourier transform of an impulse response. The impulse response is basically the time derivative of the step response.

The step response of an amplifier with abrupt upper-frequency rolloff contains both preshoot and overshoot. Fig. 1-26A.

Nonlinearity of the phase characteristic adds distortion. Fig. 1-26B shows three types of phase characteristics. These are plotted in terms of phase and delay:

a. Ideal,

b. Insufficient delay of high frequencies,

c. Peaks, or excessive delay at high frequencies.

Fig. 1-26C approximates the step response resulting from nonideal phase characteristics.

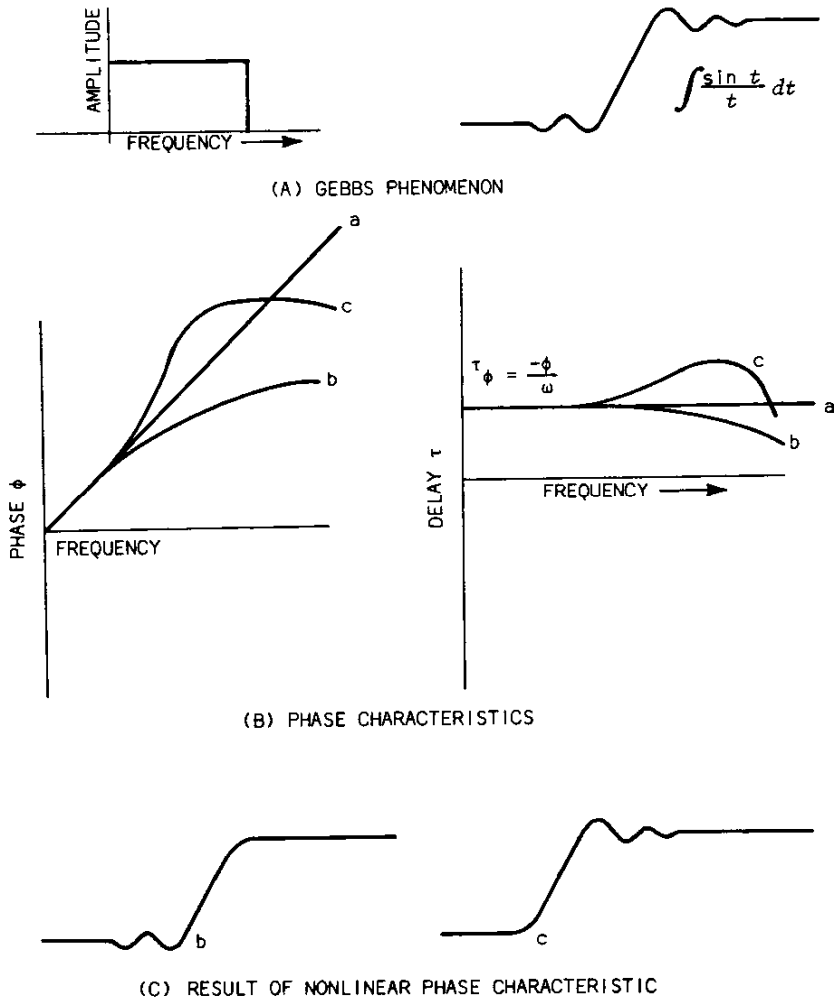


Fig. 1-26. Frequency response -- step-response interdependence.

These interrelationships can also be demonstrated by shifting and attenuating the harmonic content of a squarewave.

Fig. 1-27 shows three of many frequency components contained in a squarewave. The fundamental completes one cycle between To and T4; during the same interval the 3rd harmonic completes three cycles; the 5th completes five and so on through all odd harmonics. This relationship must be maintained for squarewave reproduction. Should the fundamental be shifted 90° (T1) the third harmonic must shift 270° and the 5th 450°. 3 x 90 = 270, 5 x 90 = 450. Further, to maintain this phase relationship all frequency components must be delayed equally: If the fundamental is delayed 5 µs, then all harmonics must also be delayed 5 µs.

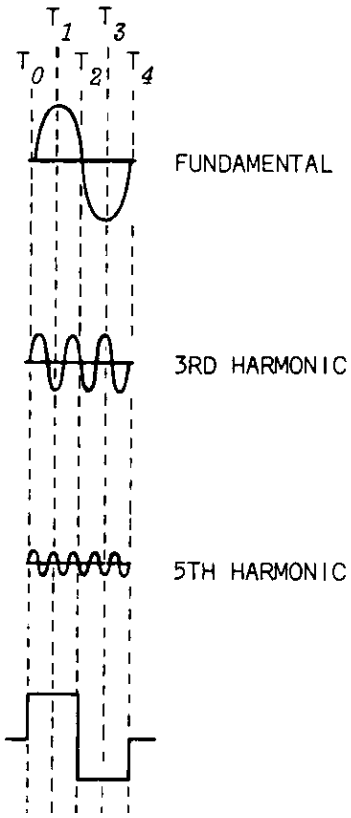


Fig. 1-27. Equal group delay.

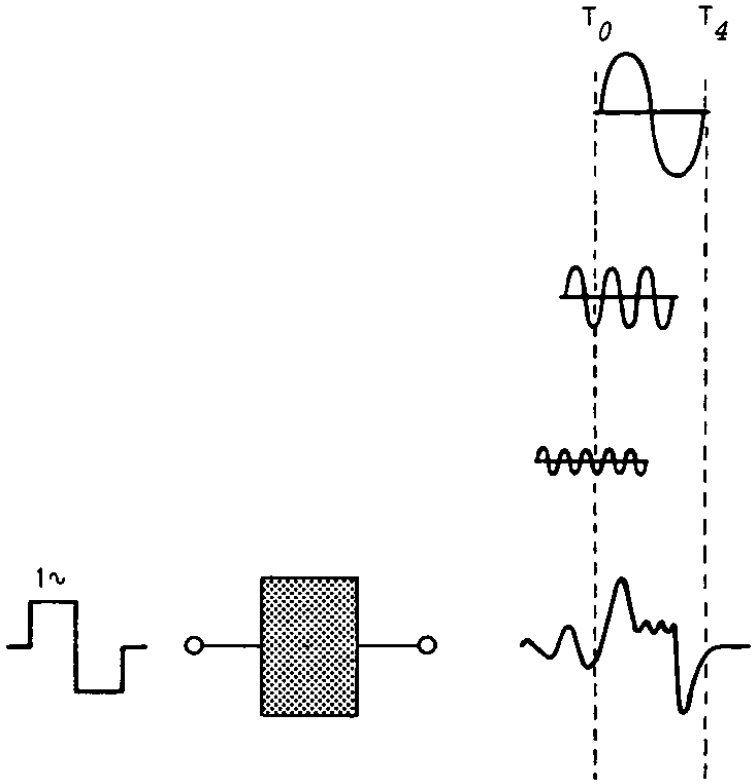


Fig. 1-28. Unequal group delay.

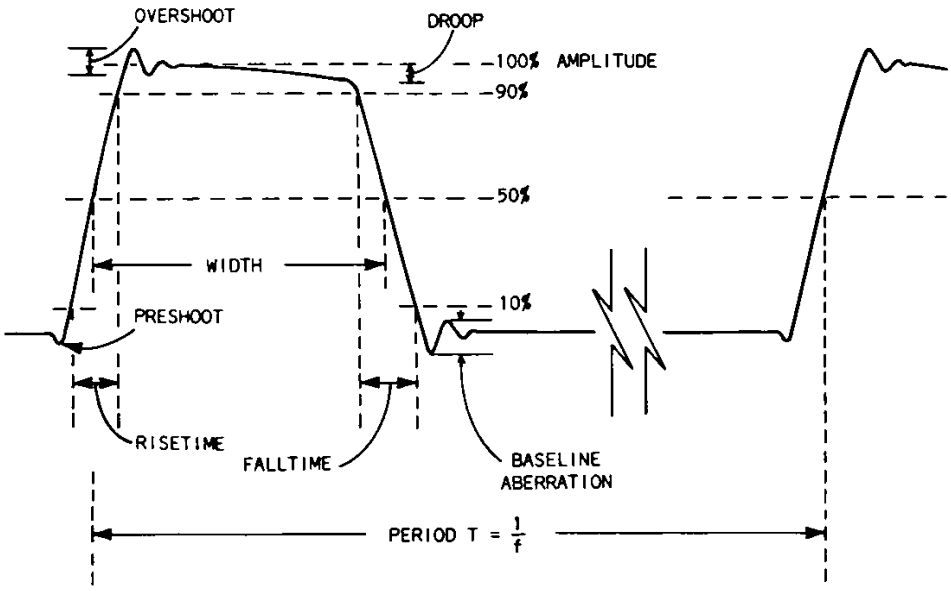


Fig. 1-29. Pulse nomenclature.

unequal group delay

Fig. 1-28 represents the results of unequal delay. High frequencies transit the network faster than low frequencies. High-frequency energy appears to arrive at the output before T0. A distorted output waveform results. In this figure the output waveform was approximated using only a few odd harmonics to show aberrations preceding the main output pulse.

These requirements for linear phase shift or flat delay apply to all waveshape reproduction.

risetime

falltime

pulse width

Apply the nomenclature covered to the simulated display of Fig. 1-29. Risetime measurements occur along the leading edge of the pulse, falltime at the trailing edge. The terms risetime and falltime become ambiguous on an inverted pulse. Therefore, risetime is always measured along the leading edge.

Pulse width and pulse-recurrence time are both measured at the 50% amplitude points.

aberrations

baseline shift

preshoot

overshoot

droop

This illustration includes fast and slow deviations. Fast deviations appear as baseline and top aberrations. Droop (tilt) indicates slow deviations.

In this case the vertical amplifier apparently imposes unequal frequency delay: High frequencies transit faster than low, creating preshoot. Overshoot also results since unequal group delay makes linear phase shift impossible. Droop is also an unequal group delay indicator. Droop shows excessive low-frequency delay. The baseline ringing, like overshoot, occurs during nonlinear phase shift/frequency relationships.

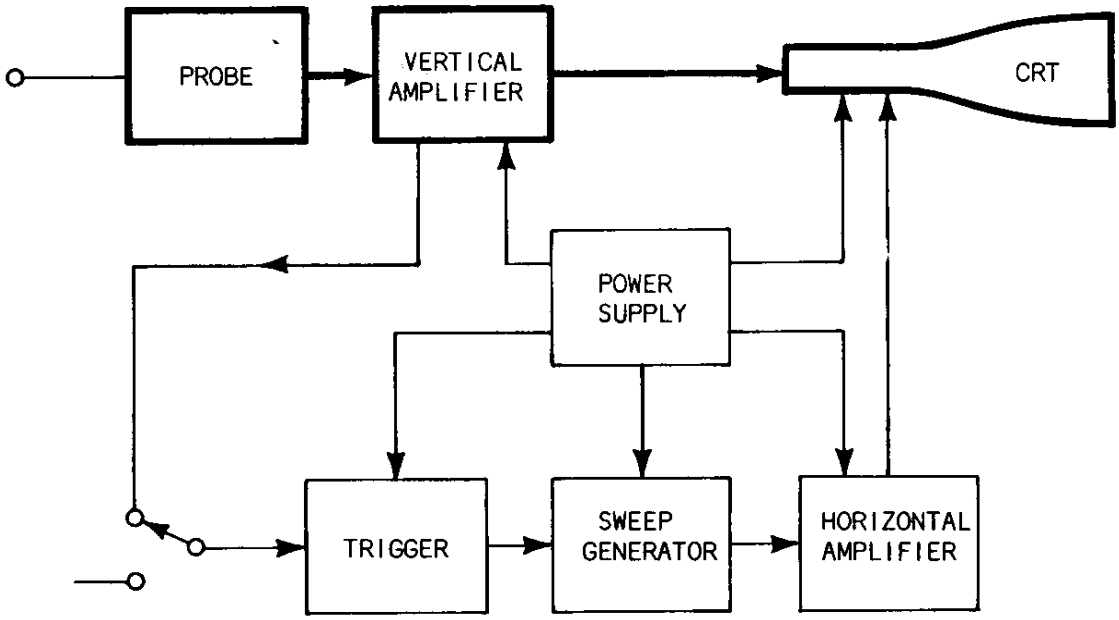


Fig. 2-1. Vertical amplifier.

3 INPUT CIRCUITS AND COMPENSATED ATTENUATORS

The first vertical circuits to affect an input signal are the input selector and input attenuator. Fig. 2-2 shows an input selector, attenuator and input amplifier block.

The INPUT SELECTOR determines lower-frequency bandwidth. Placing the input selector to AC capacitively couples signals, appearing at input connector J1, to the input attenuator. Switching to GND opens J1 and grounds the attenuator input. DC, the position shown, directly connects the attenuator to Jl.

switching

Fig. 2-3 shows improved switching logic. As an logic operator switches from DC to AC he grounds the input attenuator temporarily. This action discharges

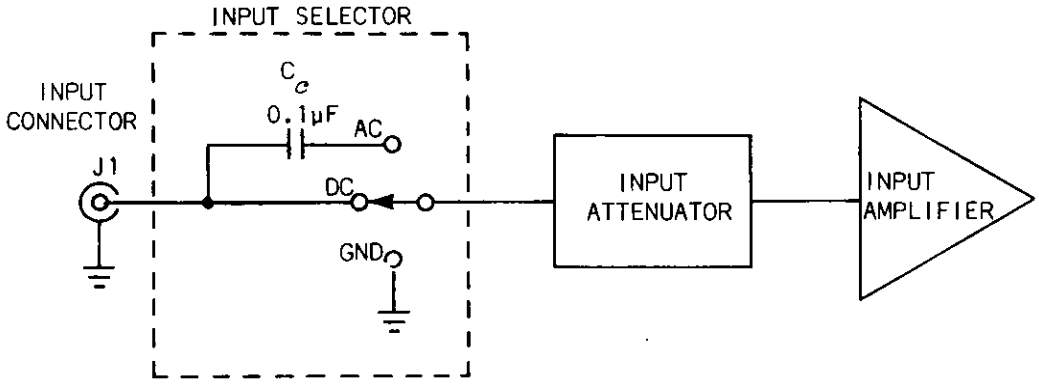


Fig. 2-2. Input-selector switching.

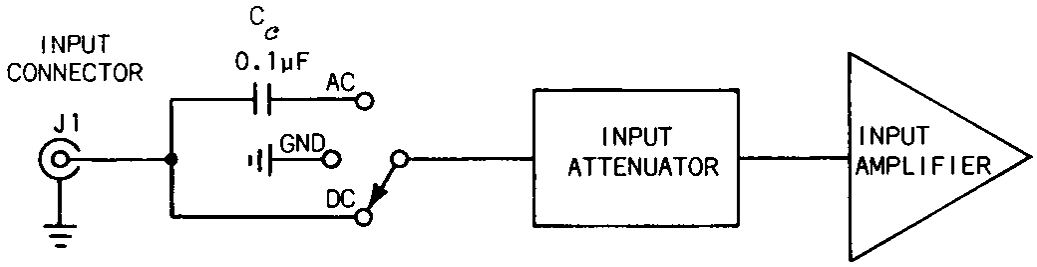


Fig. 2-3. Improved input-selector switching.

input attenuator capacitance, reducing the quantity of Cc charge current which must flow through the attenuator networks.

input charge current

Some consider the input circuit charge current negligible -- not so: There have been instances of switch contact destruction. Consider the effects of the following sequence: An oscilloscope user checks or sets the level of the -150 volt supply. The input selector is set to DC. He then decides to measure ripple content of the +150 volt supply. To do this he removes the probe from the -150 volt supply, switches to AC and connects the probe to the +150 supply.

C_C in Fig. 2-2 initially charges toward 300 volts. The input attenuator contains -150 volts charge and +150 appears at input connector J1.

In Fig. 2-3, charge current is reduced by half. When the input selector moves from DC to AC it contacts GND, removing stored charge in the input attenuator. C_C charges to the *applied* voltage.

The user certainly can reduce charge current by placing the input selector to GND between measurements. The circuit in Fig. 2-3 removes this memory burden.

C_C charge current flows through the attenuator in both cases. The vertical amplifier reacts during charge time as though a signal were applied. At best, this causes a measurement delay while the display follows the changing input charge signal. Further, C_C could have retained an additive charge from some previous measurement. This is because C_C is an open circuit in input selector positions other than AC. Adding a resistor to the circuit in Fig. 2-3 from the AC contact to the attenuator would close the loop in any input selector position.

Fig. 2-4 includes resistance R_C which closes the C_C charge path. C_C charges to the input voltage through R_C with DC or GND selected. Selecting AC shorts R_C to prevent unnecessary attenuation of input signals. This accomplishes two purposes: First, it reduces the charge current through the attenuator and the switch contacts; second, C_C cannot contain an unknown captive charge.

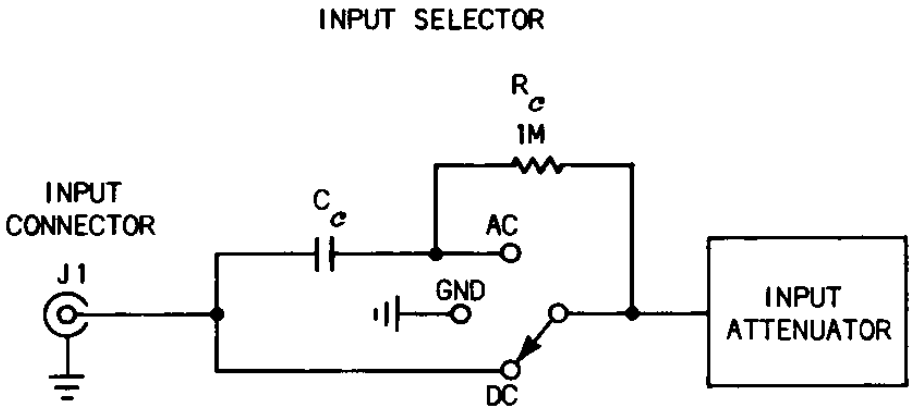


Fig. 2-4. Providing Cc an additional charge path.

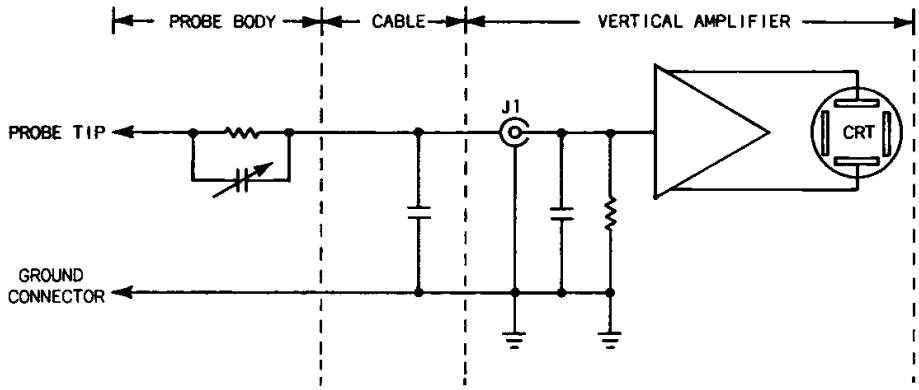


Fig. 2-5. Input circuit of a vertical system.

fixed input RC

Oscilloscopes have a fixed input RC. The attenuator changes the input deflection factor (volts per division) but not the input RC. Maintaining a constant RC eliminates probe recompensation with attenuation changes.

probe

One must couple the signal of interest to the vertical-amplifier input. Simple test leads work for some low-frequency applications. Generally, use of an oscilloscope probe results in greater convenience and accuracy. Assume the probe is connected to J1 of Fig. 2-4 and the selector switch positioned to DC.

Fig. 2-5 represents circuit equivalents of the probe and vertical-amplifier input. The probe body consists of a resistor shunted by a variable

capacitor. A single capacitor represents distributed cable capacitance. An RC network appears to the right of J1. This parallel circuit is the fixed-input time constant of the vertical amplifier.

Lumping fixed cable and vertical-amplifier input capacitance evolves the circuit of Fig. 2-6. In this figure Vi_n represents the signal of interest; V_0 the vertical-amplifier signal; R_P, probe resistance; C_P, probe capacitance; R_i, vertical-amplifier input resistance; C_i, vertical-amplifier input and cable capacitance.

Vi_n

Fig. 2-6 is a compensated voltage divider as long as time constant R_iC_i equals time constant R_PC_P . C_p and C_i form a capacitive divider creating voltage division across the capacitors equal to the division

across R_P and R_i. Ratio $\frac{R_P + R_i}{R_i}$ defines basic DC attenuation. C_P and C_i form a capacitive divider of the same ratio so that the resultant time constants equal, $R_PC_P = R_iC_i$.

attenuation ratio

compensation

An adjustable C_P allows one to adjust the probe time constant to match a specific vertical-amplifier-input time constant. This probe compensation must take place each time one connects the probe to an oscilloscope since input capacitance varies between instruments. Examples of input-time-constant specifications are listed below:

1 MΩ x 15 pF
1 MΩ x 20 pF
1 MΩ x 24 pF
1 MΩ x 33 pF
1 MΩ x 47 pF.

The listing shows a wide variation of input RC between different type oscilloscopes. Oscilloscopes of one type also vary, but to a much lesser degree. For a specific vertical amplifier one need compensate the probe once only. An input attenuator must be designed and calibrated to meet this criteria.

Compensated voltage dividers create a number of misunderstandings. Therefore, one needs to imbed the concepts of compensated voltage dividers in his mind. Fig. 2-6, the equivalent probe-scope input

circuit, contains the basic compensated voltage-divider components. And probe compensation offers an oscilloscope user a vehicle for demonstrating the effects of voltage-divider compensation.

Some say that a compensated voltage divider presents a constant impedance. **No!** Impedance *ratio* remains constant, but total impedance changes with frequency. Compensating a voltage divider sets up an impedance *ratio* independent of frequency.

Input voltage (V_{in}), Fig. 2-6, develops across an impedance (Z_T) which changes with frequency. The impedance of the probe (Z_P) and of the input (Z_i) also changes but when compensated, the ratio remains constant. This occurs when the RC time of one network matches the RC time of the other network: $R_pC_p = R_iC_i$.
If R_p = 9 MΩ , R_i = 1 MΩ, C_p = 2.2 pF and C_i = 20 pF, then $R_pC_p = R_iC_i$.

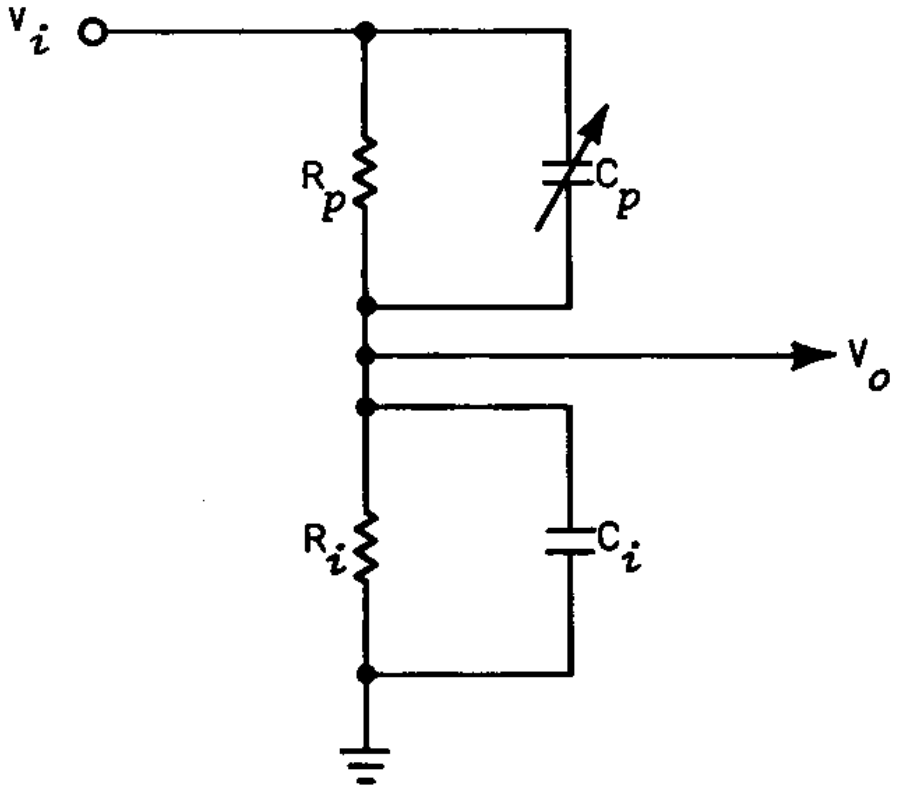


Fig. 2-6. Equivalent input circuit of a vertical system.

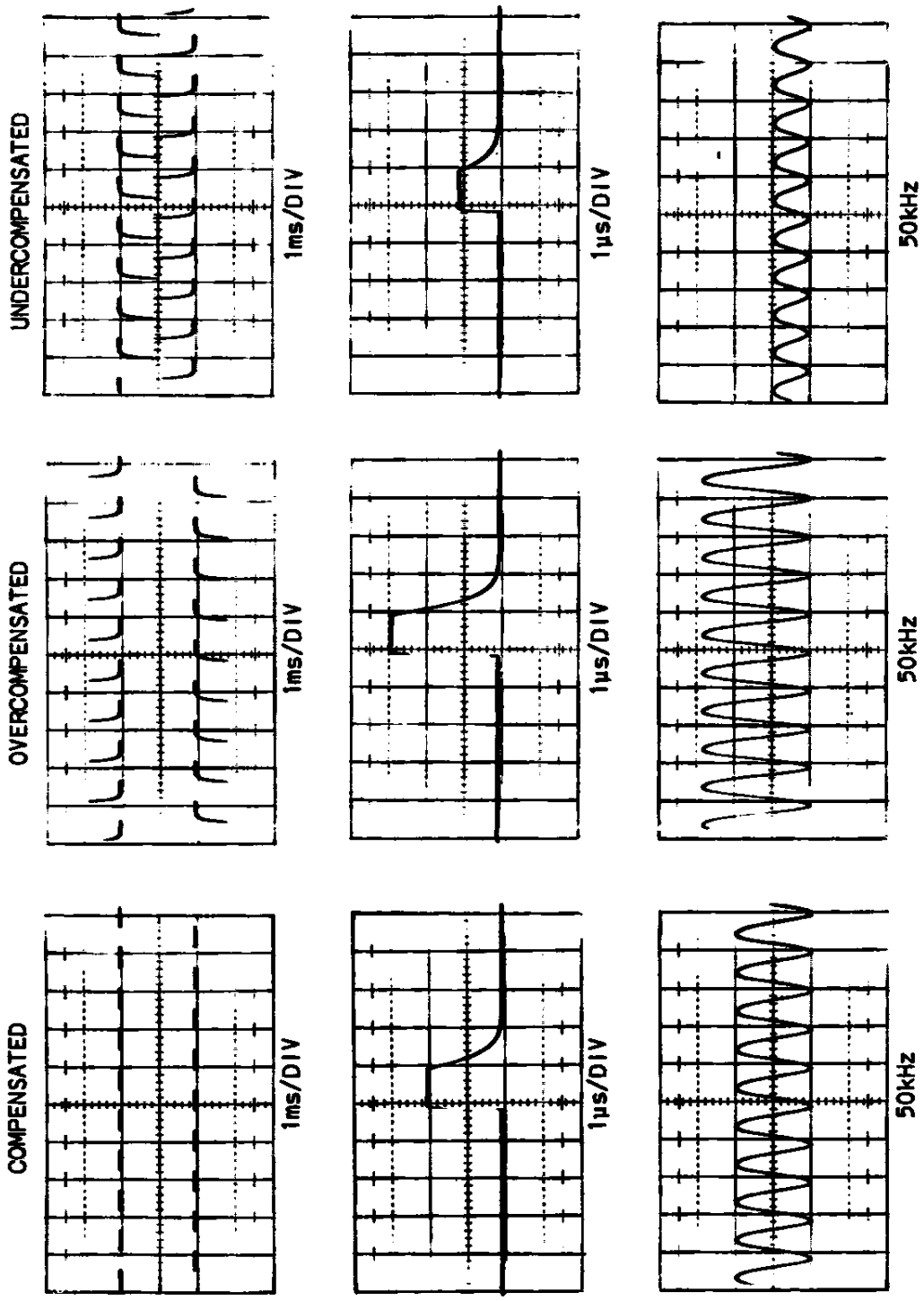


Fig. 2-7. Effects of probe compensation.

Fig. 2-7 demonstrates the effects of probe compensation. To compensate his probe one connects to a squarewave source, such as the calibrator output on most oscilloscopes. These pulses may be much slower than the vertical amplifier system.

correctly compensate

Compensate the probe by adjusting for fastest risetime without overshoot. Accurate measurements are now possible whether they be pulses or high-frequency sinewaves -- within the instrument risetime-bandwidth limits.

overcompensated

Overcompensation shows as overshoot in the calibrator waveform. Both narrow pulses and discrete high frequencies appear larger than life.

undercompensation

Rounded calibrator waveforms indicate under-compensation. Narrow pulses and high-frequency sinewaves suffer excessive attenuation.

Notice that neither the sinewaves nor *narrow* pulses change shape. This is one of the dangers. Overall waveshape does not necessarily indicate proper probe compensation.

The probe offered a logical circuit point to describe compensated voltage dividers. Mentally disconnect the probe and consider input attenuators alone. The input attenuator consists of selected voltage dividers controlled at the front panel by the VOLTS/DIVISION selector. The VOLTS/DIVISION selector is calibrated in terms of deflection factor at the input connector. To expand the discussion of input attenuator functions, assume the following vertical-amplifier conditions:

1. 33 pF x 1 MΩ specifies the fixed time constant at the input connector.

2. DC selected by the INPUT SELECTOR.

3. 10 millivolts per division is the basic input deflection factor.

4. The VOLTS/DIVISION selector steps in a 1-2-5 sequence; 0.01, 0.02, 0.05, 0.1, 0.2, 0.5, 1, 2, 5, 10 and 20 V/div.

The above assumptions relate to Fig. 2-8. To the right of the attenuator block is the grid RC of input amplifier, V1. R1 and C1 remain in the circuit at all times. They always form a part of the attenuator network. All network switching, however, takes place in the attenuator block.

X1

Placing the VOLTS/DIV selector to 0.01 switches the attenuator to X1. Selecting X1 attenuation directly connects the top of R1 to the input. Distributed capacitance (Cd) forms an appreciable portion of the input RC, and specified at the input: 1 MΩ must shunt 33 pF. R1 meets the resistive requirement, but C1 contributes only 3.3 pF. C_d then must appear as 31.7 pF:

distributed capacitance

RC_i = 1 MΩ x 33 pF; R1 = 1 MΩ; C1= 3.3 pF;
33.0 - 3.3 = 29.7 pF.

Consider distributed capacitance a component in all vertical-amplifier input circuits.

X2

Selecting 0.02 VOLTS/DIV switches the attenuator to X2 voltage attenuation. Fig. 2-9 shows the X2 attenuator schematic. Signal voltage applied to J1 appears at the top of C20, R21 and C21. 50% of the input voltage develops at the grid of V1.

Basic attenuation consists of R21, R22 and R1. 500kΩ, total resistance of parallel network R22-R1, matches the resistance of R21. Resistance, thus voltage, division is equal. 1 MΩ appears from J1 to ground.

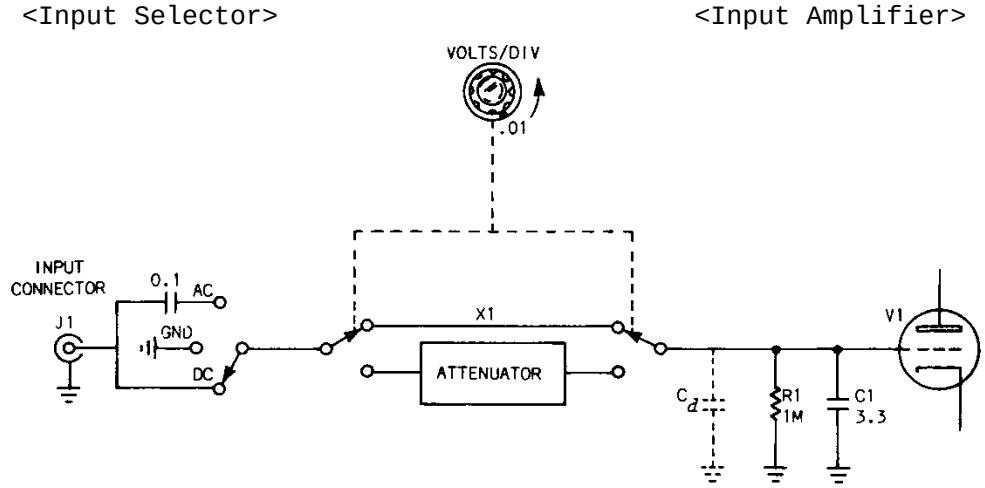


Fig. 2-8. X1 input attenuation.

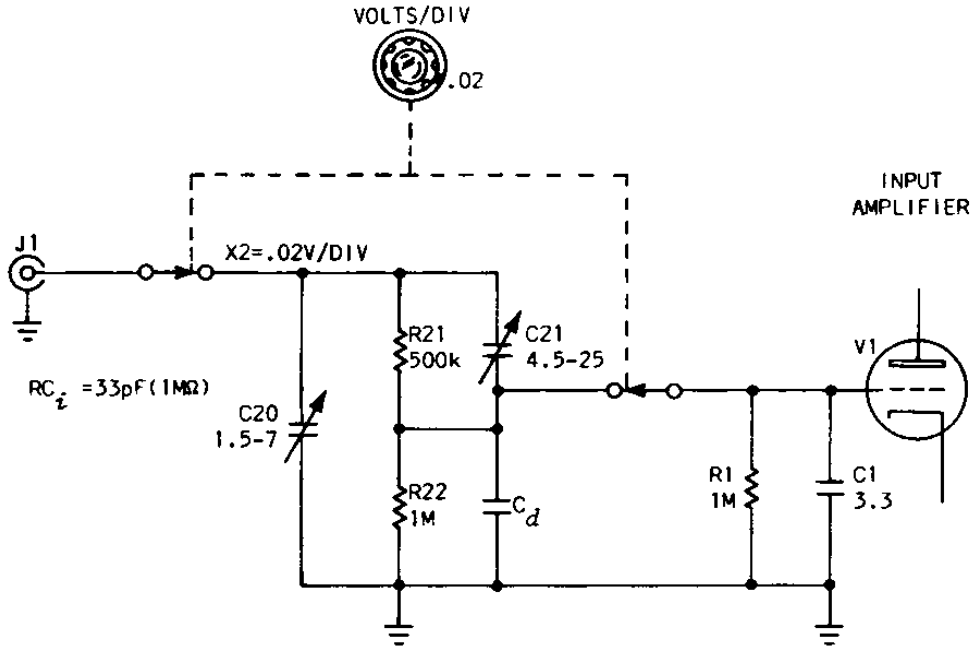


Fig. 2-9. X2 input-voltage division.

voltage divider compensation

C1 and parallel distributed capacitance (Cd) shunt the lower divider leg. One adjusts C21, across R21, to match the upper leg RC to the lower leg RC.

input compensation

Input RC = 33 pF x 1 MΩ. Switching to X2 maintained input resistance but altered capacitance. C20 shunts this network providing adjustment for 33-pF total input capacitance. Although C_d changed due to stray capacitance at the input lead, the input C altered mainly from the series effect of C21
with C_d and Cl:

$$C_i = \frac{C21(C_d + C1)}{C21 + C_d + C1}$$

C20 shunting the attenuator thus raises total input shunt capacitance to the standardized value:
C_i + C20 = 33 pF.

Moving the VOLTS/DIV selector through its range step-selects additional attenuator networks of appropriate ratios. All of the attenuator networks use the same concept: Simple RC voltage dividers which maintain a set ratio to one another and present to the input a resistance of 1 MΩ and a capacitance of 33 pF.

X100

Fig. 2-10 contains circuitry resulting from a VOLTS/DIV selection of 1.0. The operator switched in the X100 attenuator. The basic divider consists of: R202, paralleled by R1, in series with R201. C202, C_d and C1 shunt the lower resistive leg forming a capacitive voltage divider with C201. Adjusting C201 compensates the voltage divider. Adjusting C200 matches total input capacitance to other attenuator positions.

component quality

Input attenuator parts must be of high quality. They are not only close tolerance resistive or capacitive values, but also must contribute small and predictable amounts of alien components. Resistors contain capacitance or inductance or both. Capacitors also contain resistance or inductance or both. These components should be as pure as possible for use in the input attenuator. Quantity production requires physical repeatability and predictability which usually calls for purity compromises. Therefore, capacitors add L and R, and resistors add L and C.

Interconnecting and component leads are inductors. Long leads or those with a bend impose more inductance than short straight leads. Leads also contribute capacitance, dependent upon conductor spacing.

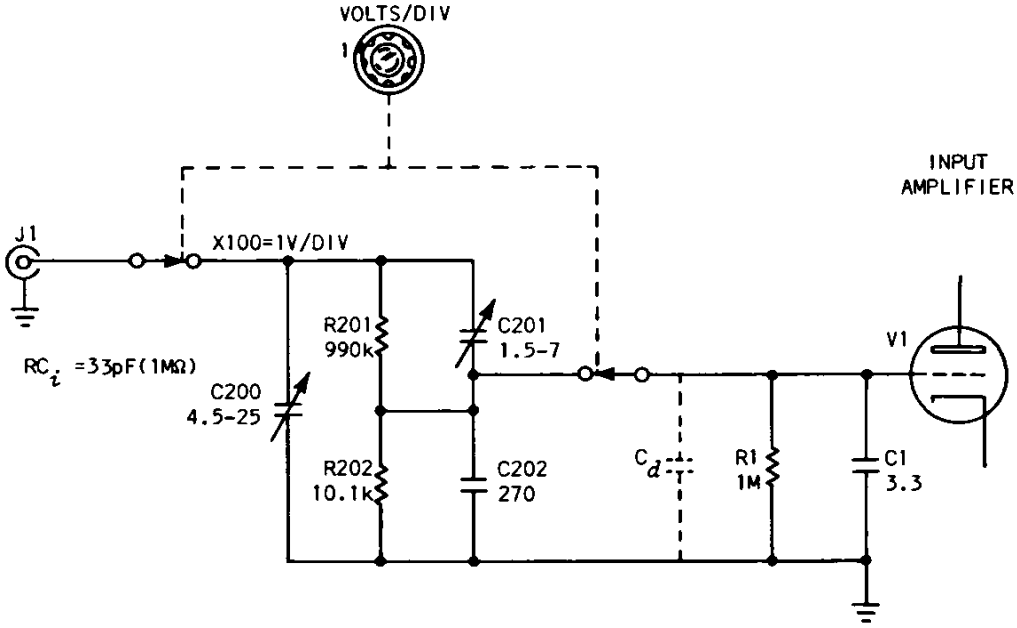


Fig. 2-10. X100 input-voltage division.

Capacitance develops between switch terminals and contacts, between circuit-board strips and so on. Any connection, in fact, is a potential capacitor. The relatively slow effect is hook. *Hook* is a small dip, of short duration, on the flat top of a displayed step, immediately following the leading edge. The capacitance variation that causes hook usually results from dielectric alterations during transit time. Dielectrics involved can be attenuator capacitors, active device input capacitance, terminal stand-off insulation, or that of a circuit board. Terminals or circuit boards are the most common offenders. This dielectric modification occurs during the step-transit time. Following pulse or step transition, the dielectric returns to normal, creating a discharge current with a time constant much slower than the input-step risetime. The discharge current develops a voltage across the output, which subtracts from the input level. Tektronix corrects for hook at the attenuator by component selection, circuit layout and circuit-board construction.

hook correction

Selected components, careful layout and quality assembly reduces stray reactances to a practical tolerance for instruments of medium risetime. As a rule-of-thumb, which will have several exceptions, assume instruments with risetimes of 10 ns or longer contain simple attenuators as shown in Figs. 2-9 and 2-10. Verticals in the 7-10 ns range may contain input attenuators as in Figs. 2-9 and 2-10, or the attenuators may reflect the techniques of the "faster" instruments.

stray components

"Fast" instruments react to stray components of sometimes obscure origins, such as the paint on components. Vertical amplifiers capable of reproducing steps of 7 ns or less have extra parts which counter component-induced distortion. This distortion takes two forms: Rolloff, due to *changing* input capacitance, and overshoot (ringing), caused by adding inductance.

Varying input capacitance is the input amplifier's response to a fast step. This "negative-input-resistance characteristic" receives treatment in the next chapter. At the input attenuator the change takes the form of additional capacitive current. Series-peaking networks provide one solution.

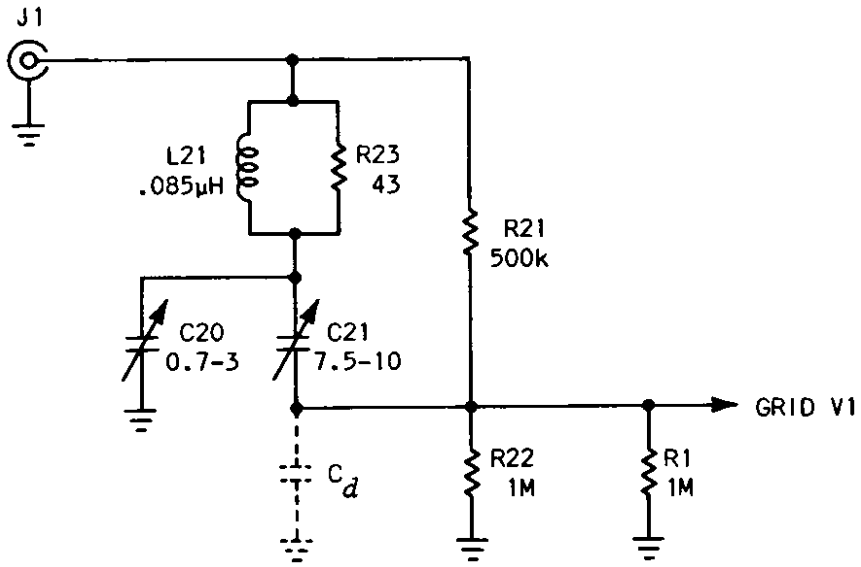


Fig. 2-11. X2 attenuator with series peaking.

series peaking

Fig. 2-11 shows series-peaking network L21 and R23 added to a X2 attenuator. This circuit is taken from a preamplifier with an overall risetime of about 2 ns. L21 and R23 maintain a delicate balance between signal and regenerative currents.

Input voltages which change levels in a few nanoseconds demand maximum capacitive current from the attenuator. The grid of V1 also draws additional capacitive current. However, during signal transit, L21 presents maximum opposition to signal-current flow. R23 then establishes total attenuator signal-current flow. If R23 signal-current reduction equals the current drawn by V1, the attenuator achieves a voltage division of 2. This only results from delicate part selection and placement. Components involved are L21, R23, C20, C21, Cd and the capacitive *change* in the V1 grid circuit. Should the components be improperly proportioned the input either rings or degrades risetime.

Precise RLC responses are very complex. For this reason only basic ideas explain peaking-network action here. R23 shunts the peaking coil. For explanatory purposes a small resistor shunting the coil has the same effect as a large series resistor. A series RLC circuit responds to a step function in one of two basic ways: It develops a

overdamped

underdamped

pulse of current, or it rings. Overdamped response (a current pulse) occurs when the L-to-C ratio is small and the series resistance is correspondingly large. Underdamped response (ringing) results from a large L-to-C ratio and a small series resistance. Curves of Fig. 2-12 show circuit current relative to L, C and R values.

Since damping is the same, a small resistance shunts L21 rather than a large series component. Keeping R23 small negates effects on all but the "fast" signals.

The overdamped response current only occurs in attenuator reactances. 1 MΩ resistance shunts the reactive leg, so when the reactive current drops to zero, total signal current flows through the 1 MΩ resistance.

In the case of Fig. 2-13, L21 and R23 separate C1 from C_d during signal transitions. C_i consists of quiescent input capacitance modified by V1 negative

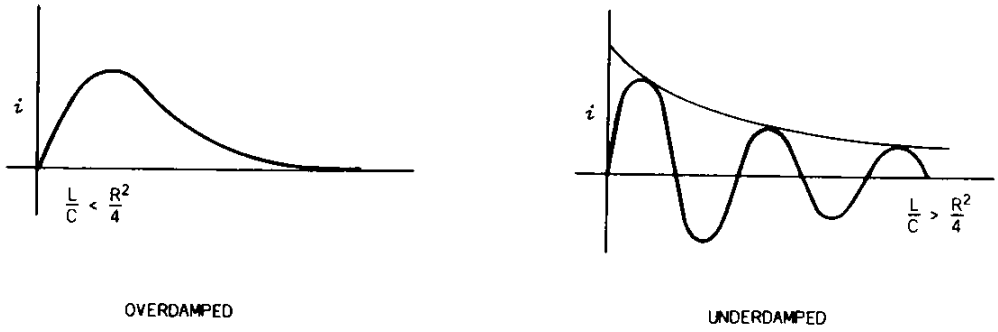


Fig. 2-12. Comparison of overdamped and underdamped response.

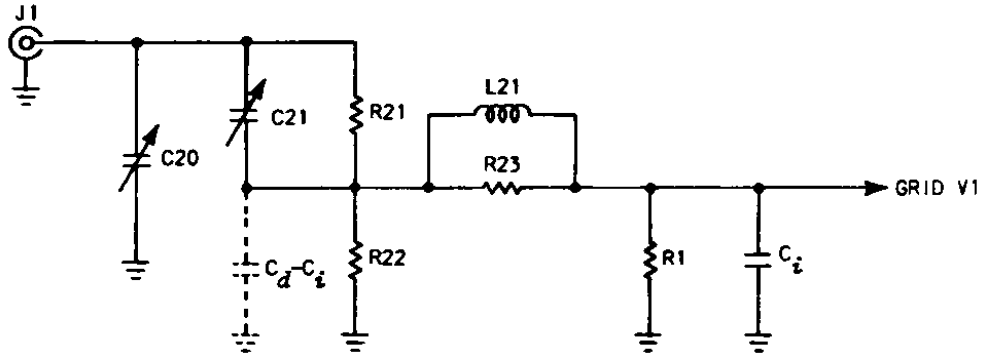


Fig. 2-13. Alternate location of X2-attenuator series peaking.

input characteristics and, possibly, circuit-board dielectric loss. L21 and R23 probably do not retain the values listed in Fig. 2-11. L and R values must combine with circuit capacitance to form an underdamped response.

RLC appear as part of the input attenuator only when the changing capacitance is an appreciable percentage of the capacitive divider. Increasing attenuation reduces the need for peaking. This is because component capacitance shunting the grid line becomes larger. The preamplifier from which Fig. 2-11 was taken has an RLC network in the X2, X5, X10, X20 and X50 voltage dividers. The X100, X200 and X500 have none, neither of course does the X1.

high-value dividers

Fig. 2-14, the X100 divider, includes no LR network. Two capacitances, C200 and C202 are much larger values than counterparts, C20 and C_d, in the X2 attenuator. The smaller value of C201 makes this necessary. Series capacitance C201 establishes total divider capacitance. Therefore, C200 must be large enough to set the input RC equal to the X1 RC at J1. C202 added to C_d should approximately compensate the divider at the midrange setting of C201: R1C1 = R2C2.

Changing capacitance at the grid line, or due to C201 dielectric deviations, represents too small a percentage of the total capacitance to consider a peaking network necessary.

ringing

R203 loads the circuit to damp oscillations. This ringing results from stray inductances, inherently a part of the capacitors, resistors and attenuator wiring. R203 adds but 1/2% error to the voltage divider.

eliminating input networks

Eliminating attenuator components reduces production costs and stray reactances. There are two major techniques used to eliminate networks: Stacking and amplifier-gain switching.

stacking

Stacking reduces only production cost. Stacking input attenuators reduces the total number of parts required for a given range of input deflection factors. The representative VOLTS/DIV selector (shown in Fig. 2-15A) and information so far presented, leads one to believe each switch position

is a separate attenuator circuit. This 11-position selector indicates 10 RC voltage dividers. (X1 is not considered a voltage divider.) There are not necessarily 10 networks. Five networks, eliminating a number of parts but adding a slightly more complex switching system, provide the same result as 10.

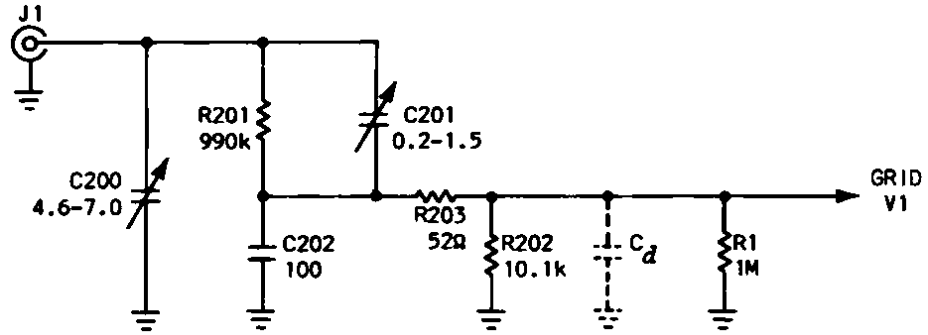
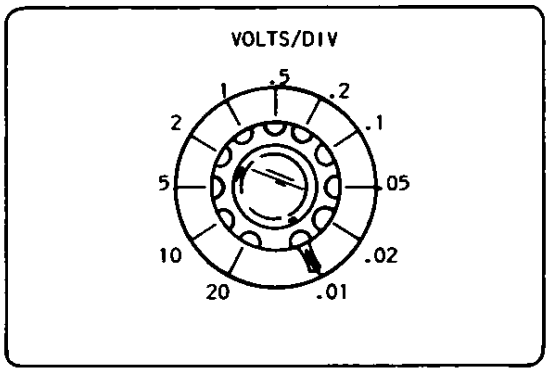


Fig. 2-14. The X100 attenuator of a "fast" preamplifier.



(A)

VOLTS/DIV	NETWORK	STACKED WITH
0.01		
0.02	(±) X2	
0.05	(±) X5	
0.1	(±) X10	
0.2	(±) X10	(±) X2
0.5	(±) X10	(±) X5
1.0	(±) X100	
2.0	(±) X100	(±) X2
5.0	(±) X100	(±) X5
10.0	(±) X1000	
20.0	(±) X1000	(±) X2

Fig. 2-15. Stacked-attenuator switching logic.

stacking program

Stacking cascades, by switch selection, voltage dividers to multiply attenuation ratios. Fig. 2-15B lists a stacking program. The first column lists selected input deflection factors; the second, primary attenuators selected; and the last column, the selected cascaded attenuator. For input deflection factors 0.01 VOLTS/DIV through 0.1 VOLTS/DIV only primary attenuators appear. Selections 0.2 VOLTS/DIV through 20 VOLTS/DIV utilize X2 and X5 attenuators in cascade; of this group 1 VOLTS/DIV and 10 VOLTS/DIV utilize primary attenuator selections alone.

and X inter. changeable

Symbols (1) and (X) both appear in Fig. 2-15B. These symbols are interchangeable and either may appear on a schematic diagram. Read X2 as an attenuation of 2; and 12 as a voltage division of 2.

Compare Fig. 2-15B and Fig. 2-16. Fig. 2-16 illustrates a stacked X20 or 120 input attenuator. Fig. 2-15B indicates attenuation results from selection of 0.2-VOLTS/DIV input deflection factor. Each attenuator network presents 1-MΩ input impedance. Therefore, connecting the X2 network across R102 shunts the same as R102 connected to the grid of Vl. R1 does parallel R22. Both X10 and X2 attenuators then load as though connected in the circuit alone. Proper voltage division occurs:

1. 200 millivolts at J1 develop 20 millivolts at junction R101-R102.

2. 20 millivolts across the X2 attenuator develop 10 millivolts at the grid of V1.

Stated in terms of deflection factor:

1. 200 millivolts/division at Jl.

2. 20 millivolts/division input to the X2 attenuator.

3. 10 millivolts/division at the grid of V1.

Selecting 0.5 VOLTS/DIV substitutes a X5 attenuator. Input voltages now receive an attenuation of 50. Concepts remain the same for all stacked configurations.

compensation

One compensates these dividers in switch positions that place single networks in the circuit. From Fig. 2-15B, these positions of the VOLTS/DIV selector would be: 0.02, 0.05, 0.1, 1.0 and 10. Selecting stacked positions creates the need for compromise adjustment. Unfortunately, stacking limits minimum input capacitance. The electro-mechanical effects of each stack adds capacitance.

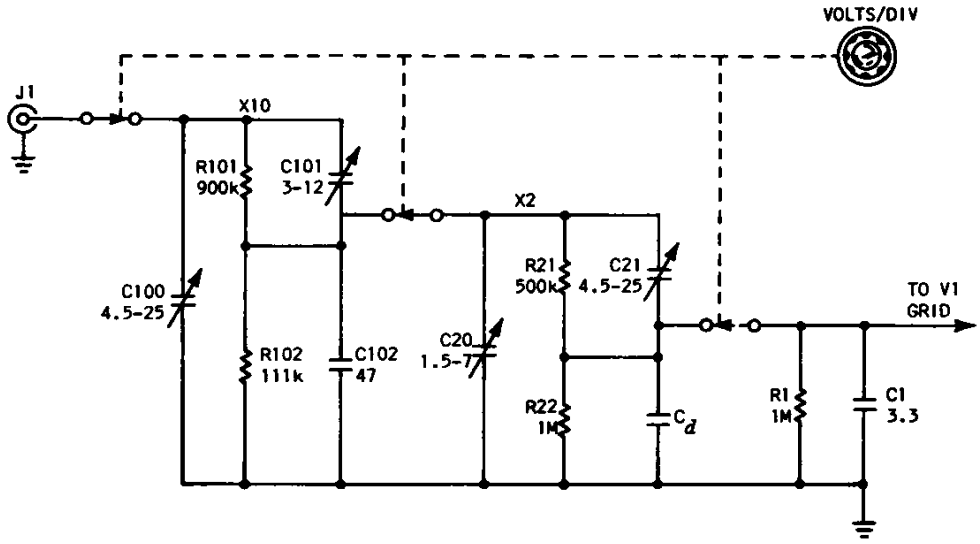


Fig. 2-16. X20 or ÷20 stacked attenuator.

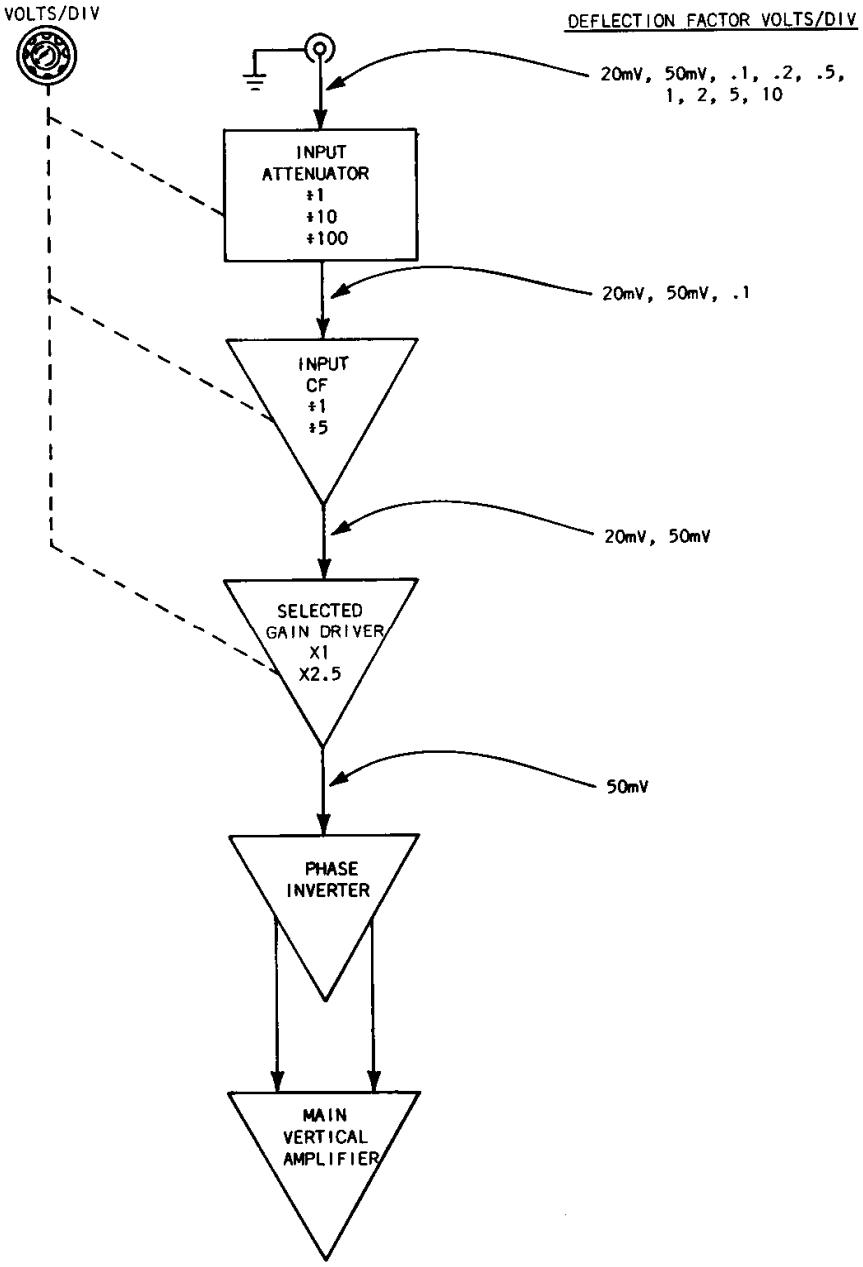


Fig. 2-17. Preamplifier switching logic.

gain switching

Amplifier-gain switching, mechanically ganged to the input attenuator, provides the present solution for numerically reducing input attenuator networks. Fig. 2-17 shows in block form the switching logic

input attenuator

necessary to drive a phase inverter at a constant deflection factor. Blocks labeled Input Attenuator, Input Cathode-Follower and Selected-Gain Driver mechanically gang to the VOLTS/DIV selector. Deflection factor at the input jack is from 20

input CF

millivolts to 10 volts per division, step-selected in a 1-2-5 sequence. The three input dividers reduce the nine input deflection factors to three: 20 millivolts, 50 millivolts and 100 millivolts.

selected-gain driver

Selecting cathode-follower gain of 1 or 1/5 gives an input deflection factor to the selected-gain driver of 20 and 50 millivolts per division. The selected-gain driver can now have a constant output deflection factor.

Wafer switches contribute significantly to total capacitance, even to the simplest input attenuators. Stacking compounds the difficulty. Stray inductance increases due to wiring complexity as well as stray capacitance.

turret attenuator

The device which reduces stray reactances the most is the seldom used turret attenuator. Fig. 2-18 is a photograph of one type of Tektronix turret attenuator. The body of the turret holds voltage-divider components. These parts need have very short leads thereby reducing inductance. Rotating the turret body moves voltage-divider parts and associated connectors to the single set of switch contacts. No method yet devised contributes as few reactances as the turret attenuator.

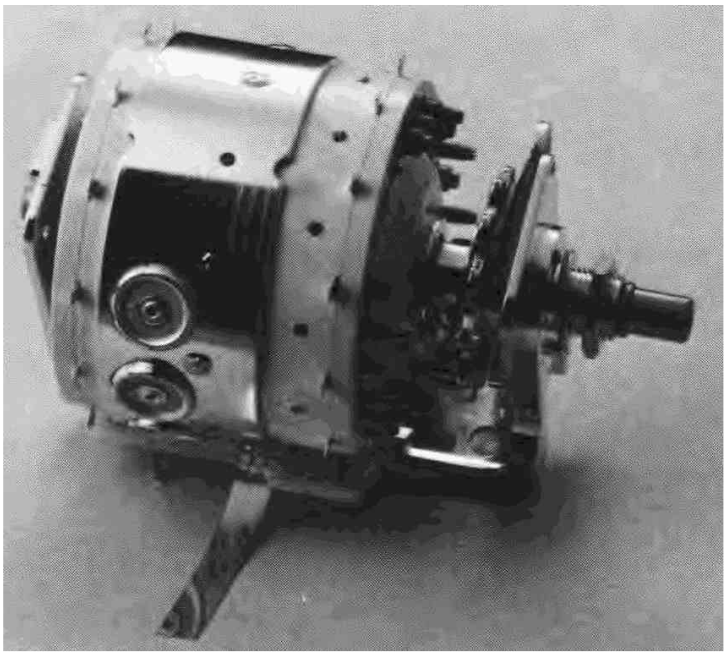


Fig. 2-18. Turret attenuator.

Turret attenuators at present just don't lend themselves to quantity production. For this reason only a few Tektronix instrument types contain turret attenuators.

Modern oscilloscopes have a constant input RC. The input attenuator consists of compensated voltage dividers. Deflection factors change in one of three basic methods:

1. Selecting one of a group of compensated voltage dividers.

2. Program selecting stacked compensated voltage dividers.

3. Amplifier-gain switching combined with one of the above techniques.

4 FOLLOWERS

three basic configu-rations

Followers consist of three basic circuit configurations: Cathode followers, source followers and emitter followers. Follower circuits might appear in any stage of oscilloscope circuitry. Basic follower characteristics justify such wide usage. Characteristics necessary to achieve uniform frequency response over a wide range of input frequencies and amplitudes are indigenous to followers:

1. Low input capacitance (high input impedance).
2. Low output impedance.
3. Linear amplification.
4. Gain stability.
5. Can handle large input voltage swings.

Additionally, there are peculiar characteristics of followers that are made use of:

6. Gain is less than one but can be made to approximate unity.
7. No signal inversion.
8. Quiescent level is easily set.
9. Supply voltage fluctuations are greatly attenuated at the output.

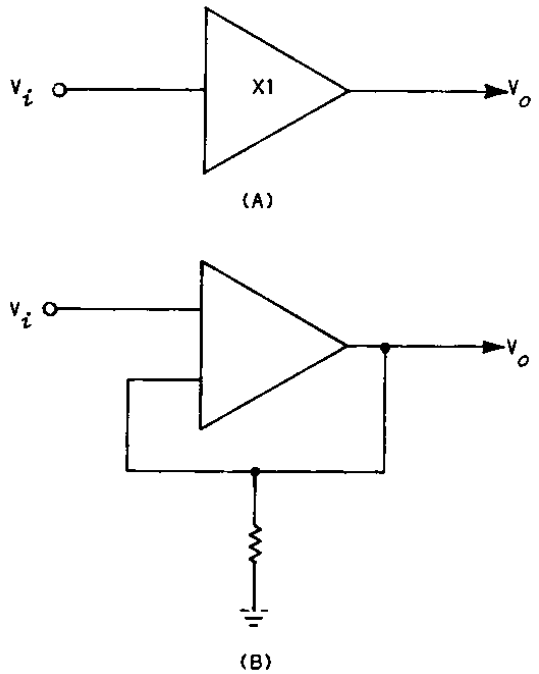


Fig. 3-1. Follower symbols.

circuit symbols

Circuit symbols, as shown in Fig. 3-1, apply to followers. (A) symbolizes a unity gain amplifier. However, one might interpret (A) to indicate phase inversion unless the initials CF, SF, or EF appear within the triangle. CF abbreviates cathode follower; SF, source follower; and EF, emitter follower. On the other hand, symbol (B) is exclusive to followers. This symbol indicates noninverted unity gain. Both symbols appear in block diagrams through this book.

CF, SF and EF abbreviations

low input capacitance

Any discussion of follower circuitry in wideband amplifiers utilizes the terms impedance transfer or isolation. These terms generally apply to all characteristics but specifically consider the first two: low input capacitance (another term for high input impedance) and low output resistance.

low output R

risetime improvement

Fig. 3-2 illustrates the principle of placing afollower between a large resistive output and a large capacitive input to improve risetime. Risetime (bandpass) of an amplifier is a function of the product of resistance and capacitance. 2.2 RC defines circuit risetime. Follower amplifier A2 shunts the large output resistance of A1 with a small capacitance. A2 also presents to A3 a small Ro to shunt the large input capacitance of A3. The resultant risetime is less than connecting A1 directly to A3.

input amplifier

Followers are not restricted to interstage isolation. They also function as output amplifiers or, as shown in Fig. 3-3, input amplifiers. The followers' high input impedance shunts the attenuator very little, allowing passive device values to set input impedance at J1. Of the three basic follower configurations, cathode followers currently appear most frequently as input amplifiers.

cathode follower

Fig. 3-4 shows a cathode follower. In this figure, a pulse applied to the grid develops at the cathode with corners rounded and attenuated. Consider first the signal attenuation. Attenuation implies

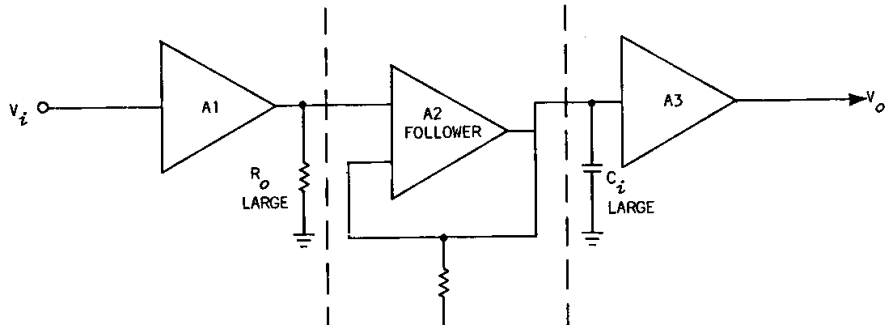


Fig. 3-2. Isolation block diagram.

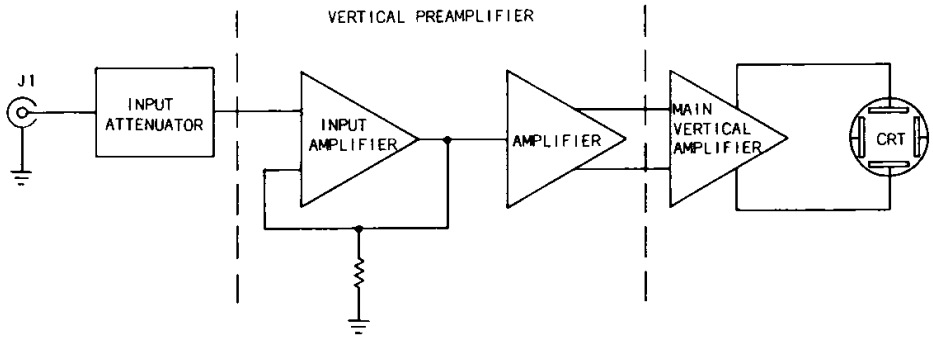


Fig. 3-3. Vertical-amplifier block diagram.

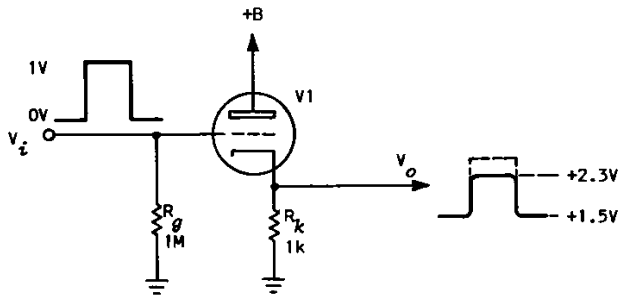


Fig. 3-4. Cathode follower.

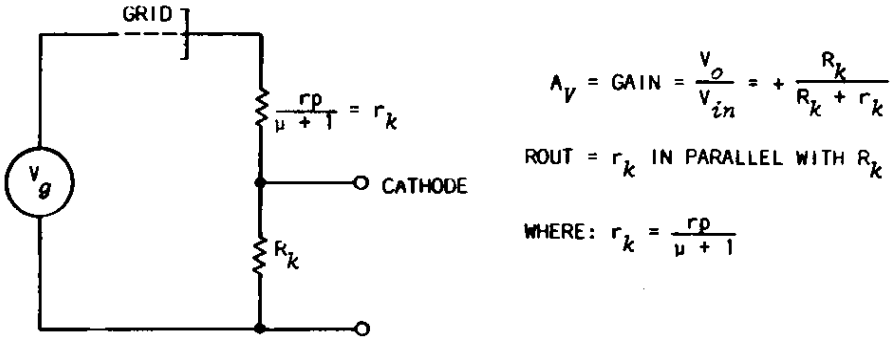


Fig. 3-5. Equivalent CF circuit (1).

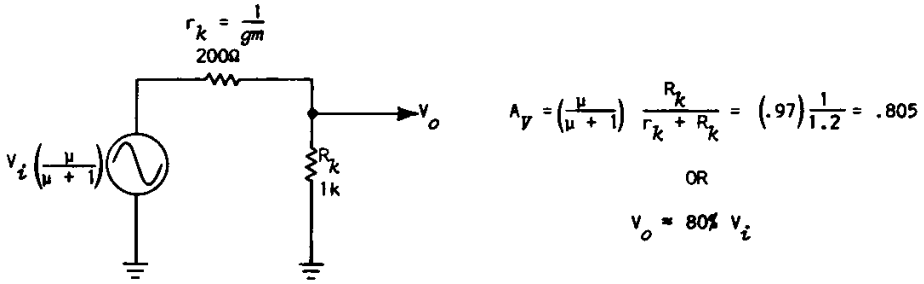


Fig. 3-6. Equivalent CF circuit (2).

voltage-divider action and that is just what happens. The voltage applied to the grid develops across Rk and the internal impedance of V1.

Fig. 3-5 depicts a cathode-follower model. A theoretical voltage generator, or source, drives the control grid. Grid voltage (V_G) develops across a voltage divider consisting of external cathode load (R_K) and internal tube impedance (r_K). Formulas included in Fig. 3-5 define gain as a voltage-divider ratio. They also show that output impedance at the cathode terminal results from (R_K) paralleling (r_K).

Active device parameters such as amplification factor (μ) and plate resistance (rp) must be considered. Because transconductance *(gm)* applies to any active device, it appears more often in this book than any other dynamic parameter.

Using parameters μ and *gm,* one builds the cathode-follower model shown in Fig. 3-6. This figure assumes μ = 30 and *gm* = 5000 μmho. The voltage source applies grid voltage, modified by μ, across voltage divider r_k and R_k. Both models (Figs. 3-5 and 3-6) develop gain of 0.8, indicating active parameter interdependence.

gain approximations ignore μ

Usually satisfactory approximations result from using transconductance alone. Discarding μ in the gain formula of Fig. 3-6 leaves the resistance ratio only. Gain now resolves to 0.83, sufficiently accurate for most circuit analysis.

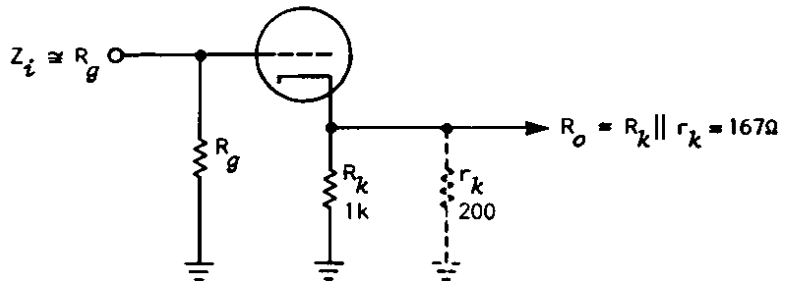
transconductance determines output impedance

Parameter *gm* establishes output impedance as shown in Fig. 3-7. Output circuits connect to the junction of R_k and r_k. Therefore, output impedance (R_0) cannot exceed the value of $r_k(1/gm)$. High *gm* devices out present a smaller R_0 to output circuits than low *gm* devices.

plate current affects *gm*

Plate current affects *gm,* causing questionable gain stability of the circuit shown in Fig. 3-8. For small signals this circuit might be satisfactory. But large signal gain stability does not exist because of the large change in plate current. The circuit as shown experiences 65% plate current change. Plate current and *gm* relate directly and gain is a function of *gm:*

$$r_k = \frac{1}{gm}.$$



IF *gm* = 5000μmho, $r_k \cong \frac{1}{} = 200\Omega$

Fig. 3-7. CF output impedance.

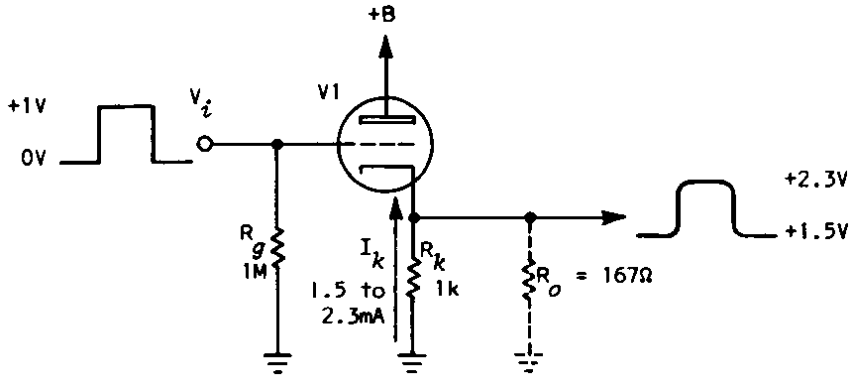


Fig. 3-8. CF signal current.

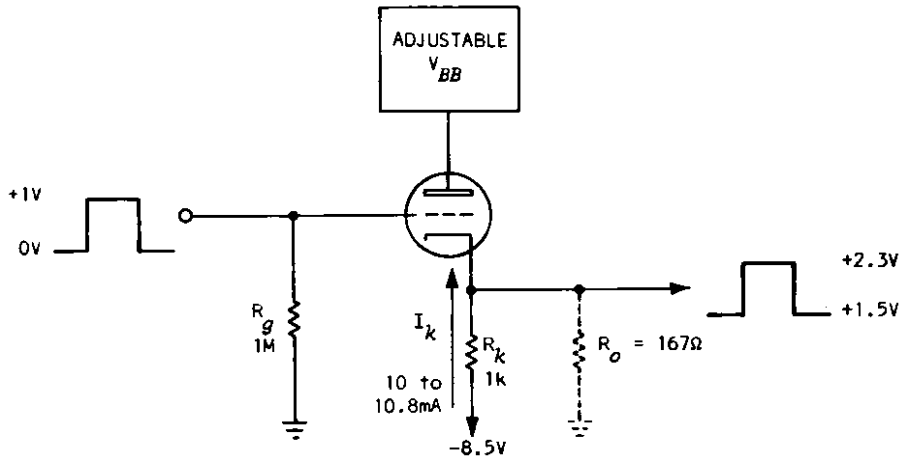


Fig. 3-9. Plate voltage determines output level.

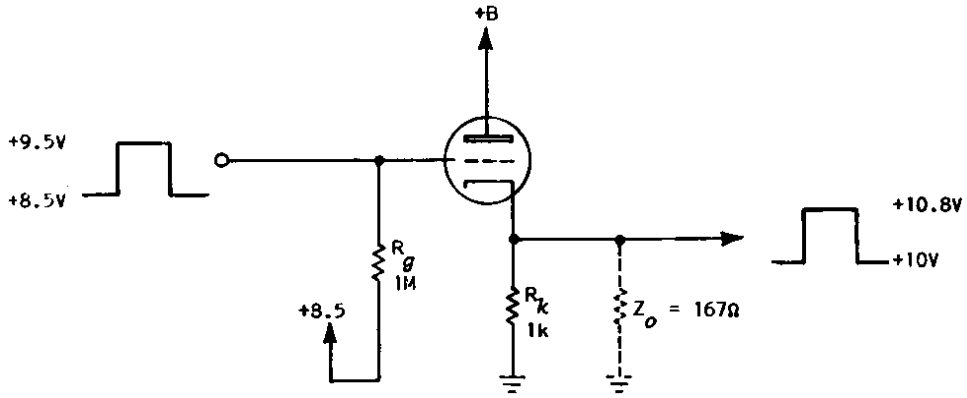


Fig. 3-10. Positive grid return equivalent to negative cathode return.

gain stability results from constant plate current

Fig. 3-9 represents an improvement. Notice that output DC levels, output impedance and gain are the same as in Fig. 3-8. An adjustable plate return sets the quiescent output DC level. Plate current is determined by self-bias, R_k and the negative cathode supply voltage. The positive signal excursion now causes only 8% change in plate current. This percentage reduces further when both R_k and the negative return increase. For example, if R_k were 2 kΩ returned to a -18.5 V supply, an input signal of 1 V would cause 4% plate-current change. The external components free the circuit to act as a constant-current device. Fig. 3-10 functions the same as the circuit in Fig. 3-9 except the cathode resistor returns to ground.

longtailing

A method of current driving an active device, so popular it has a name, is shown in Fig. 3-11. This is a *longtail* circuit. The name derives from the large cathode resistor. Ratio of r_k to R_k is such that output impedance is 1/gm and gain is μ /(μ+1)

constant I_p stabilizes *gm*

One volt signal causes less than 3/4% change in plate current, stabilizing transconductance.

The cathode returns to -150 volts through 30 kΩ. Operating characteristics demand cathode potential of +1.5 volts at quiescence. 5.05 mA then flows under no signal conditions. Increasing grid voltage 1 volt increases cathode current by 0.03 mA or a total of 5.08-mA plate current.

This small change hardly affects *gm.* Notice that gain approaches unity. The longtailed cathode follower meets most of the follower requirements.

Fig. 3-12 shows a longtail configuration returning R_k to ground. Concepts remain as explained.

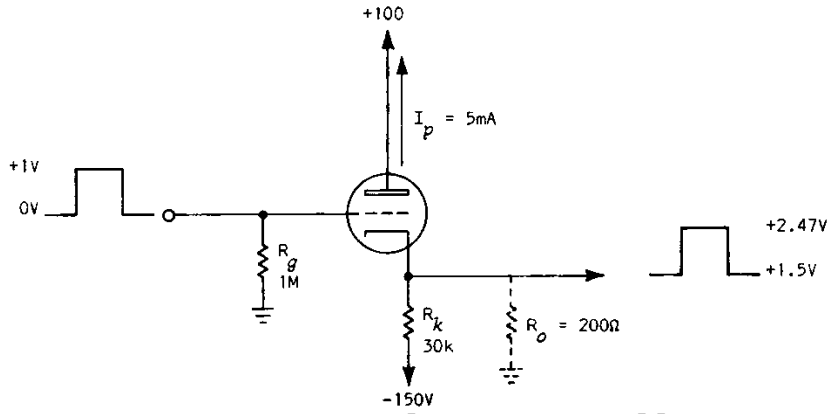


Fig. 3-11. Longtail cathode follower.

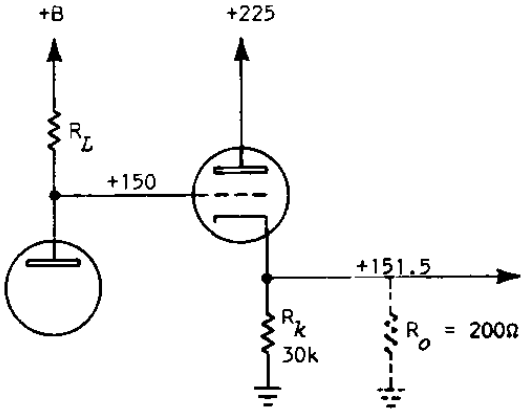


Fig. 3-12. Longtail CF with cathode returned to ground potential.

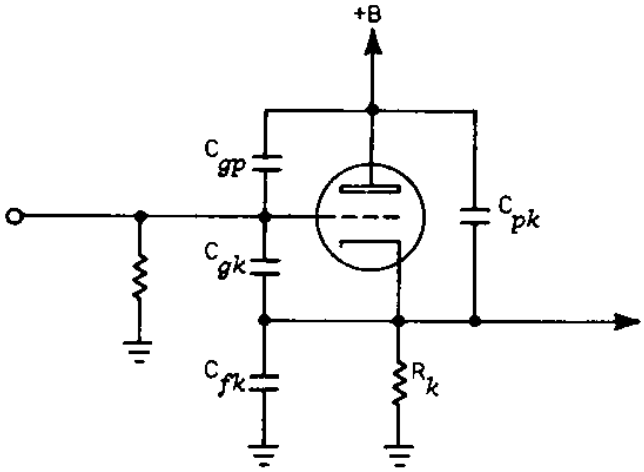


Fig. 3-13. Interelectrode capacitance.

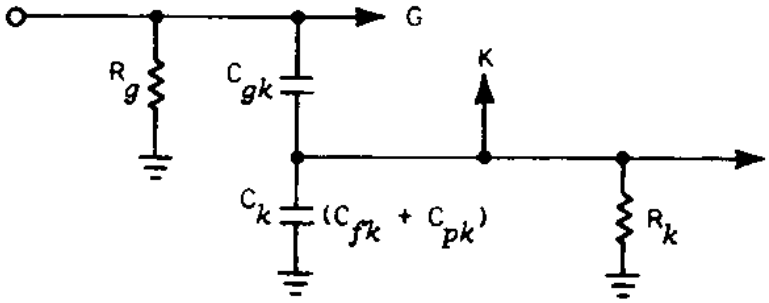


Fig. 3-14. Input capacitance.

The presentation assumed only resistive components acted upon signals, yet reactive elements exist in any circuit. Reactive components within the tube, grid-to-plate and grid-to-cathode capacitance, are of greatest concern. The effect of these capacitors depends upon circuit design. Fig. 3-13 identifies triode capacitances.

triode capacitances

How much a capacitor affects a signal is determined by the signal voltage across the capacitor. C*gp* and V1 plate return to a low-impedance voltage supply. Cathode follower design then innately reduces the effect of C*gp,* although still a circuit component.

gain and grid-to-cathode

If unity gain could be realized, capacitance from grid to cathode could be ignored. With no voltage difference across the capacitor, equivalent capacitance is zero. Equivalent grid capacitance then is C*gk* multiplied by one minus voltage gain: [Cg = C*gk* (1 - Ay)]. Another reduction is illustrated in Fig. 3-14. Capacitance, filament-to-cathode and plate-to-cathode, appears in series with

capacitances establish input capacitances

C *k*. Assume cathode follower input capacitance falls between less than one picofarad and two picofarads.

output impedance provides charge path for output capacitance

Capacitance, associated with cathode-follower output, rapidly charges through the low-output impedance. This capacitance affects the performance of "fast-rise" amplifiers and as such receives attention later in the chapter. Ignore, for now, cathode-follower output capacitance.

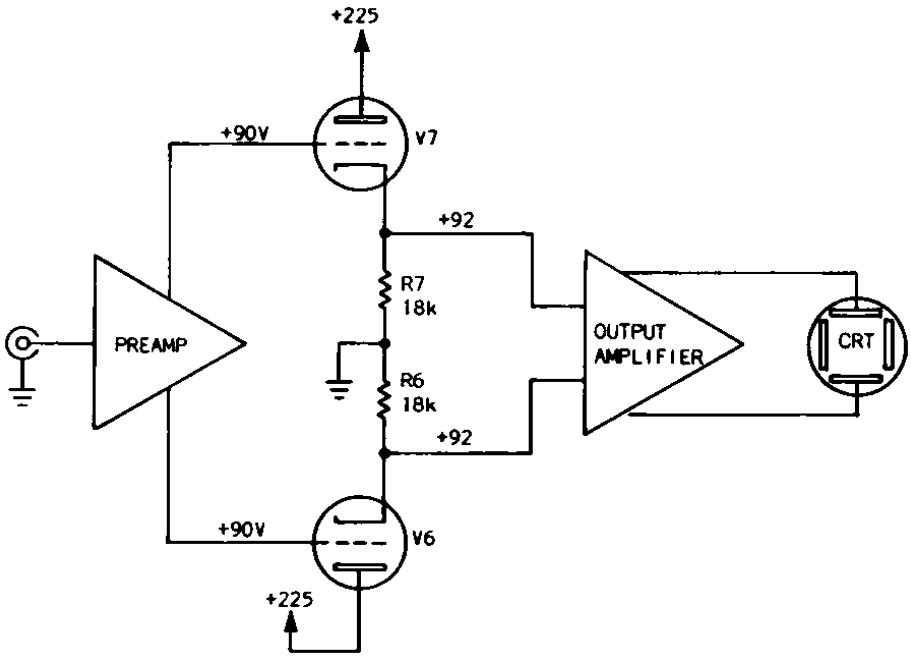
typical circuits

Vertical amplifiers having a frequency response of DC to ten megahertz or so contain cathode followers as developed. Fig. 3-15 through 3-20 are examples of typical oscilloscope circuits using concepts presented.

Fig. 3-15 shows a pair of cathode followers driven push-pull. These longtailed circuits function to breakup parallel capacitive networks.

V6 and V7 operate independently to act as a kind of coupling circuit. R6 and R7, in conjunction with the positive grid potentials, longtail V6 and V7. DC levels and signal amplitudes applied to the output amplifier approximate values applied to V6 and V7 grids.

Both the preamplifier and main vertical output amplifiers are plate loaded. A longtailed cathode follower presents much less input capacitance and



output impedance than a plate-loaded amplifier. Placing the cathode followers between the plate-loaded amplifiers then improves risetime. The small input capacitance of V6 and V7 shunts the pre-amplifier output, while the relatively large input capacitance of the output amplifier rapidly charges and discharges through the small Ro of V6 and V7.

risetime improvement

Series peaking coils may appear in the output leads of V6 and V7.

Fig. 3-16 depicts a cathode-follower circuit, used to improve bandwidth (risetime), which includes a balance control within the longtail network.

Driven push-pull, V1 and V2 operate independently. Grid DC and signal levels originate within the preamplifier. The cathode followers merely couple preamplifier voltages to the driver amplifier, elevated by a DC level representing self bias.

coupling devices

R4 serves to reduce the positive supply voltage to the correct operating level at V1 and V2 plates. R4 is common to V1 and V2 plate current. Push-pull signal currents flow in V1 and V2 and these equal-amplitude opposite-phase currents maintain a constant drop across R4. A capacitor bypassing R4 is thus superfluous.

centering control

One sets R3 for a vertically centered CRT display. Most main vertical amplifiers consist of cascaded direct-coupled push-pull stages. Any imbalance at the input, amplified, deflects the CRT as a signal. This is the correct action for DC measurements. Quiescently however, the CRT display must center. Placing a ground at input connector J1, one adjusts R3 to compensate for: An unbalanced preamplifier, small differences between V1 and V2, and unbalanced conditions of following stages.

centering empirical

Changing R3 changes V1 and V2 plate currents in opposite quantities. Plate current and *gm* track. Therefore, adjusting R3 affects small changes in cathode-follower gain in opposite quantities.

Breaking up capacitive networks to improve high-frequency response or risetime sums up the purpose of the circuit in Fig. 3-17.

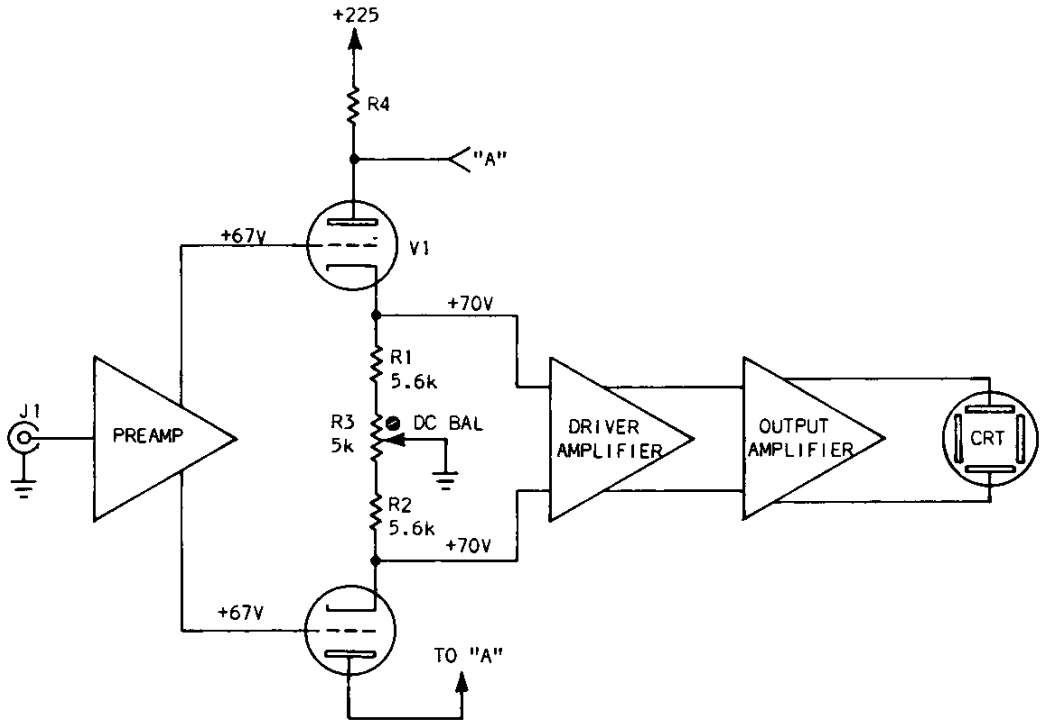


Fig. 3-16. Main vertical input amplifier.

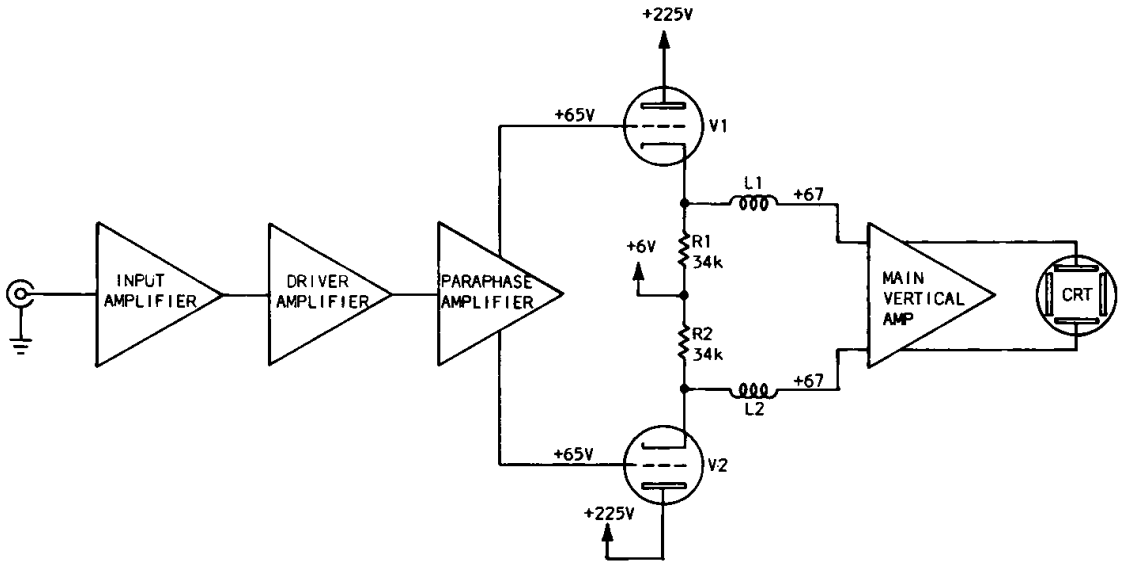


Fig. 3-17. Preamplifier output amplifier.

V1 and V2 drive, both signal and DC level, originates in the phase inverter; this is a direct-coupled push-pull cathode-follower stage. The circuit is longtailed by Ri and R2 grid levels and cathode return supply. Amplitude of drive is also a factor in longtailing, and this circuit is a case in point.

Voltage drop across R1 and R2 is much less than circuits thus far presented but consider the signal magnitude. A typical deflection factor is 100 mV (push-pull) per division. Translated to one grid, 50-mV signal drive to V1 results in one-division vertical deflection at the CRT. 500 mV deflects 10 divisions, but causes less than 1% change in V1 or V2 cathode current.

connector capacitance increases risetime

Preamplifiers are frequently plug-in units. Interconnecting plugs have an appreciable capacitance. High-impedance drive, such as the output of the phase inverter, charges and discharges this capacitance slowly enough to cause risetime or high-frequency deterioration. Placing a cathode follower between the two improves conditions. Capacitance of the interchassis connector is driven by a small output impedance, and the high impedance of the phase inverter drives a very small capacitance. L1 and L2 series-peak to improve high-frequency response.

The push-pull longtailed cathode follower shown in Fig. 3-18 drives a capacitive load. This circuit includes beam-position indicators as an operator aid.

Cathode followers V1 and V2 provide a low-impedance charge path for the capacitance presented by the vertical deflection plates. R1 and R2, cathode return supply, and grid voltages longtail V1 and V2. Network R3, B1, B2, R4 and R5, shunts longtailing but this network imposes negligible loading.

beam-position indicators

Located on the front panel, neon lamps Bl and B2 indicate relative vertical displacement:

Both lamps off, display centered.
Up lamp (B1) on, display deflected above center.
Down lamp (B2) on, display deflected below center.

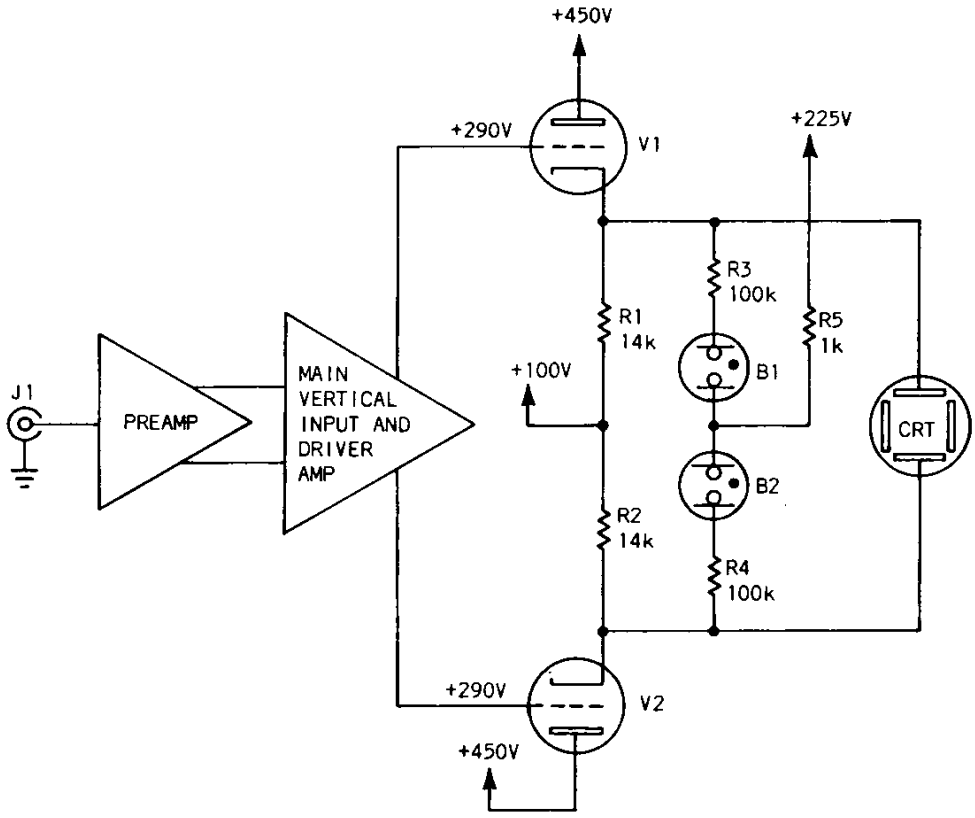


Fig. 3-18. Output amplifier.

Under no signal conditions, with the trace centered, neither neon fires. Cathodes of V1 and V2 are not quite positive enough for firing potential across the glow tubes. Positioning the trace upward raises V1 cathode and B1 fires. Positioning the trace below center raises the cathode of V2 and B2 fires.

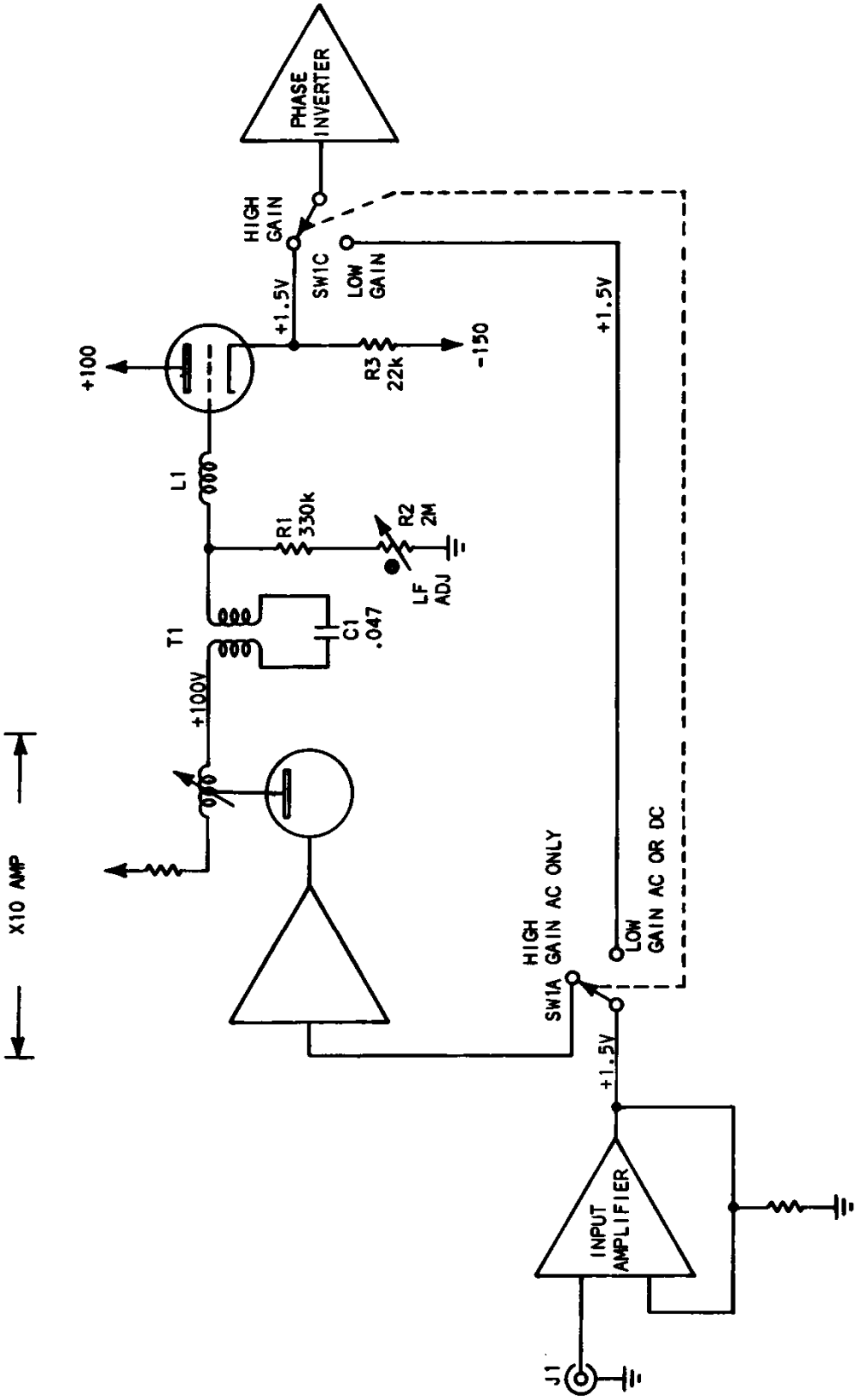


Fig. 3-19. AC coupled follower.

small signals AC only

Frequently one needs to observe small AC voltages superimposed on a relatively high DC level. An AC-coupled vertical amplifier allows one to monitor only the small AC component at low input deflection factors. Fig. 3-19 represents a preamplifier capable of amplifying small AC signals.

high gain

Positioning SW1 to HIGH GAIN AC ONLY, as shown, routes input amplifier signals to the X10 amplifier; then via cathode follower V4 to the phase inverter.

low gain

Throwing SW1 to LOW GAIN AC OR DC directly connects the input amplifier and phase inverter.

The X10 amplifier increases small signal voltages to amplitudes appropriate to the phase-inverter input deflection factor. But, these signals suffer a frequency-dependent phase shift; and the quiescent DC level at both contacts of SW1C should equal.

X10 amplifier compensation appears in longtailed cathode-follower V4 circuitry. This circuit has several functions:

1. Isolates the high-impedance X10 amplifier and phase inverter.
2. Matches the input-amplifier output DC level.
3. Broadband input coupling.
4. High-frequency compensation.
5. Low-frequency phase compensation.

quiescent output of X10 and input amplifier match

Switching from high gain to low gain one should observe very little vertical trace movement. To accomplish this the quiescent output of the X10 amplifier and input amplifier must closely match. AC coupling (C1) allows a ground return for the grid of V4. Stabilized by longtailing the self-biased operating point for V4 equals the output DC level of the input amplifier.

T1 couples signals around C1

C1 couples low frequencies and T1 couples high frequencies around Cl. C1 is both hero and villain. It must have a voltage rating high enough to prevent breakdown and enough capacitance to pass low frequencies. These requirements determine physical construction of C1. Shunt capacitance to the chassis, due to physical properties and placement of Cl, deteriorates high-frequency response. The primary of

T1 is in series with C1 and as shunt capacitive current increases, transformer action increases. The circuit suffers very little high-frequency signal loss.

L1 series peaks

Both amplitude and phase compensation are shown. L1 and the input capacitance of V4 develop series peaking for high-frequency amplitude compensation.

C1, R1 and R2 phase compensate

Low-frequency phase compensation depends on the time constant of RC network, Cl, R1 and R2. One adjusts R2 for optimum presentation, such as pulse train symmetry.

triode connected

One frequently sees, in equipment designed a few years earlier than this writing, triode-connected pentodes as cathode followers. Consider these devices as high-gm triodes.

pentodes as cathode followers

The active device in Fig. 3-20 is a pentode. Cathode-follower-connected pentodes function as described for triodes, keeping in mind the difference in tube characteristics.

For example: $\mathbf{r_k = \mu / gm}$, but μ in a pentode is so large that formula $\mathbf{\mu / \mu + 1}$ meaningless. Therefore, assume the signal voltage across divider r_k and R_k equal to control-grid signal voltage.

The circuitry of Fig. 3-20 makes use of the screen-grid to improve signal-to-noise ratio at low signal levels.

screen grid decoupled in "AC" only

Ganged switches SW1A and SW1B select high-gain or low-gain amplification. SW1 (positioned as shown) in the LOW GAIN position sets the input deflection factor to 50 millivolts per division. That is, a 50-millivolt control-grid signal results in one division deflection at the CRT. Placing SW1 to HIGH GAIN increases input sensitivity by a factor of ten. The high-gain amplifier has an input deflection factor of 5 millivolts per division *AC only.*

screen decoupling degenerates cathode DC signals

In low-gain operation both AC and DC are amplified. Putting high-impedance decoupling networks in the screen circuit, such as R2-C1, degenerate DC signals at the cathode. Therefore, the screen grid returns to a low-impedance regulated supply. The supply has ripple and transients, which reflect into the cathode as signals. In the low-gain mode these signals are too small to notice.

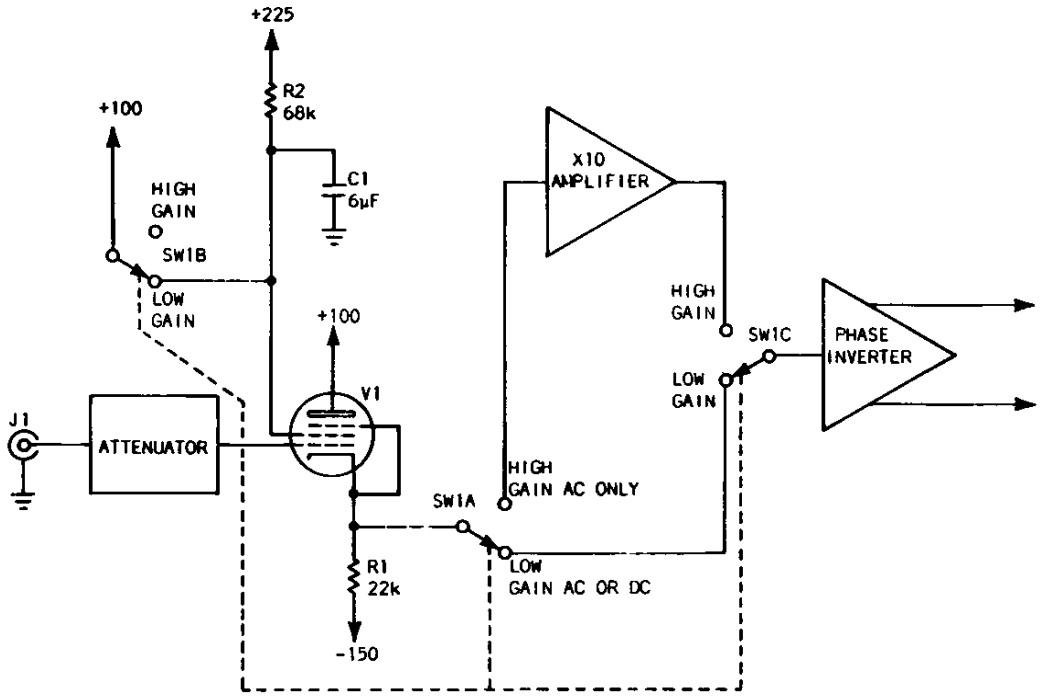


Fig. 3-20. Pentode cathode follower with switched screen grid decoupling.

Increasing the sensitivity (switching to high gain) means a smaller voltage may be monitored, but it also means that the screen grid-induced signals become objectionable. A large decoupling network returned to a higher supply results in a clean signal.

Cathode-follower circuits are a good medium for presenting protective and corrective devices. Protection frequently provides for either operator error or component failure. Corrective devices compensate for unusual or unwanted circuit parameters.

Some circuits correct for undesirable characteristics of active devices that are not apparent or objectionable until very small amplitude signals must be amplified. As an example, control grid current exists in any electron tube. In tubes employing unipotential cathodes, both positive and negative grid currents flow. Positive grid current consists of electrons emitted by the cathode and intercepted by the control grid. Negative grid current results when a heated negative control grid emits electrons to the cathode, adding to the effects of gas molecules and leakage current between the control grid and other tube elements.

positive grid current

negative grid current

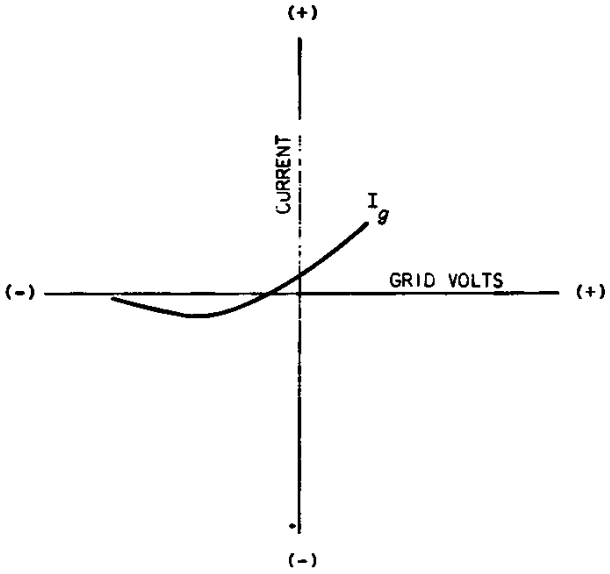


Fig. 3-21. Control grid current versus bias.

Fig. 3-21 graphically illustrates grid current versus grid bias voltage. The horizontal axis extends from a few volts negative through zero to a few volts positive. The vertical current axis extends from a small negative quantity (grid-to-cathode flow) through zero to a small positive quantity (cathode-to-grid flow). At extreme negative bias a small negative grid current flows.

grid current bias intercept

Reducing bias toward zero, negative grid current increases then decreases, intercepting the horizontal at a low negative-bias level. Incremental axis values vary between tube types and to a smaller degree between the same type of different manufacture. Generally, the grid-current grid-bias intercept occurs at less than -1.5 volts.

negative grid current minute

Magnitude of negative control grid current is so small that it is sometimes ignored. When an amplifier must amplify low-level signals (1 to 20 millivolts), this grid current can no longer be neglected. 5 nanoamps of grid current through R1 of Fig. 3-22 raises the grid potential to a level of 5 millivolts. A solution, returning R1 to a negative 5 millivolt supply, results in zero volts from grid to ground.

negative grid return cancellation

Negative grid current continues to flow developing positive grid voltage (Fig. 3-23). When negative grid current develops a voltage across R1 equal to the voltage at the wiper of R4, zero volts appears

between control grid and ground. One checks the setting of R4 by shorting the control grid of V1 to ground. R4 is properly set when the short application and removal causes no displayed vertical deflection.

Positive grid current can be used to advantage. To set up conditions, suppose an operator is measuring ripple on a 500-volt DC power supply. His instrument in X1 attenuation, he inadvertently

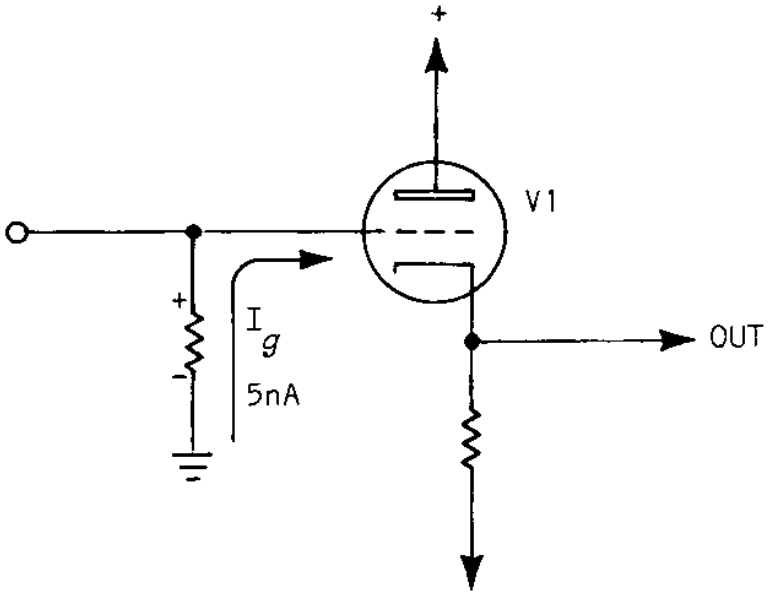


Fig. 3-22. Negative grid current.

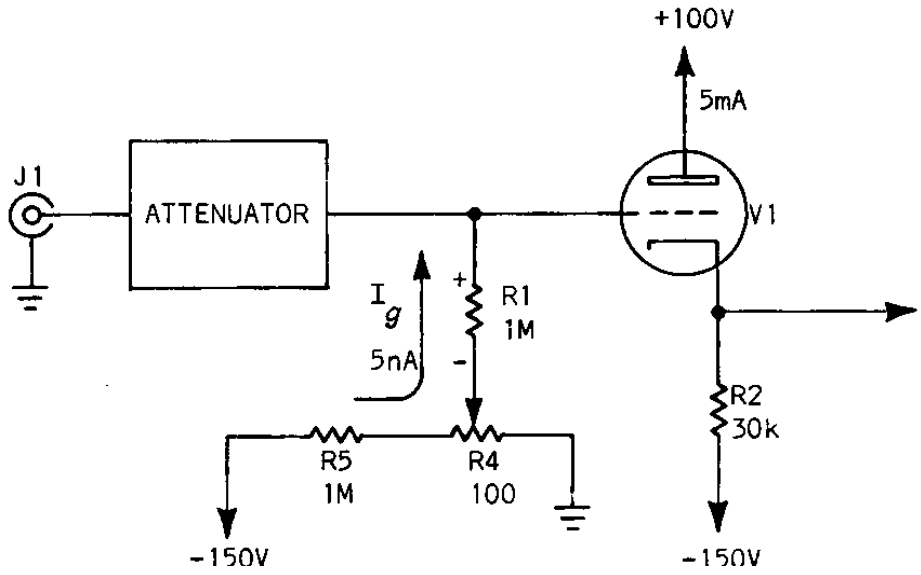


Fig. 3-23. Input-amplifier grid-current adjustment.

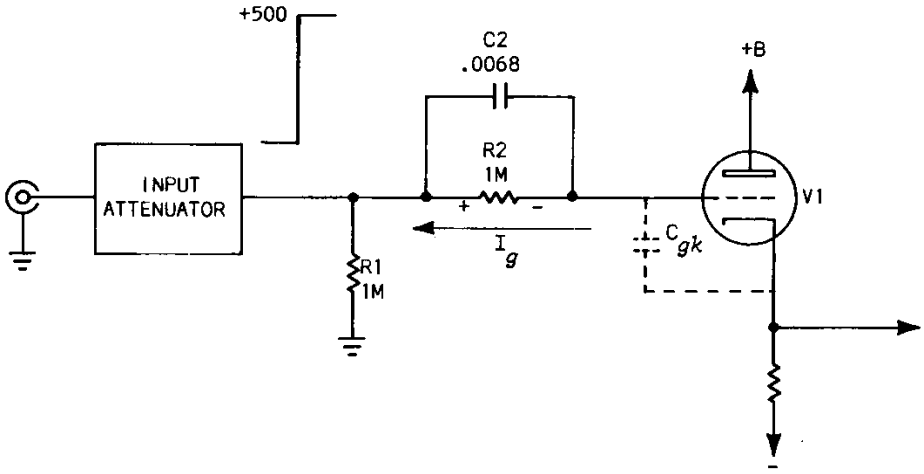


Fig. 3-24. Grid limiting.

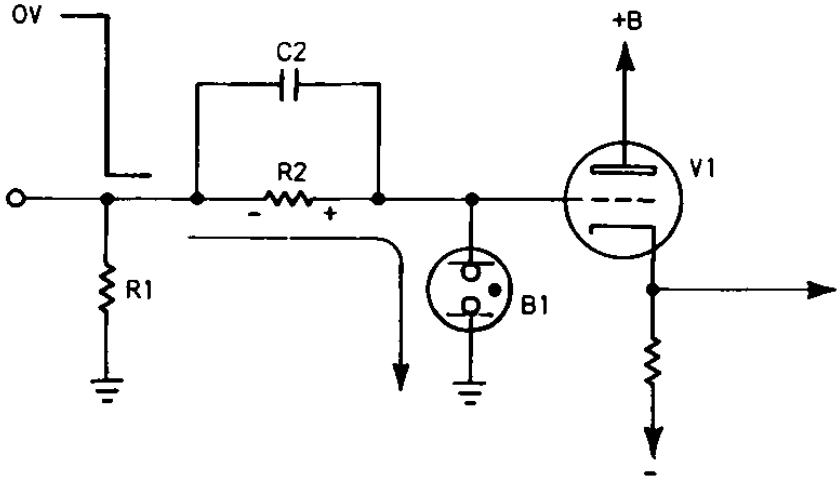


Fig. 3-25. Neon-lamp clamping.

leaves the input selector at DC. Refer to Fig. 3-24. Positive grid current in this circuit prevents a catastrophic failure. 500 volts to an input-amplifier grid requires more power than the tube or associated components safely dissipate. However, grid limiting due to positive grid current and R2 maintains tube current at a safe value.

grid limiting

C2 charges Cgk

C2 bypasses R2 so the network does not affect normal signal inputs. C2 provides a current source for discharge of Cgk which accumulates a charge during any voltage drop across R2.

neon protection

Fig. 3-25 shows protection from excessive negative as well as positive excursions at an input-amplifier grid. Excessive potential fires B1. Until this

voltage is removed B1 holds the control grid to "on" voltage for Bl. B1 extinguishes upon removal of excess input voltage.

Protective circuits incorporated as part of an input amplifier frequently protect following stages (Fig. 3-26). Keep in mind the high probability of direct coupling to following stages. Excessive CF output voltage can result in following stage part damage.

output clamps

D1 and D2 clamp to prevent large output-voltage excursions. Interruption of V1 conduction, such as open filaments, allows the output DC level to seek the -150 volt level to which Rk returns. D1 turns on to clamp as negative output voltages extend below ground potential. Large positive signals turn D2 on. D2 clamps when output-signal excursions exceed +5 volts. D1 and D2 allow a voltage "window" of 5 to 7 volts.

output voltage window

Semiconductor junctions (diodes) require a "turn-on" or forward bias dependent upon chemical make-up. Once turned on these devices maintain a voltage drop across the junction approximating turn-on potential. Assume that turn-on and diode voltage drop are equal. The list below includes semiconductor type and junction voltage drop:

1. Gallium Arsenide (GaAs) 1-V turn-on.

2. Germanium (Ge) 0.2-V turn-on.

3. Silicon (Si) 0.6-V turn-on.

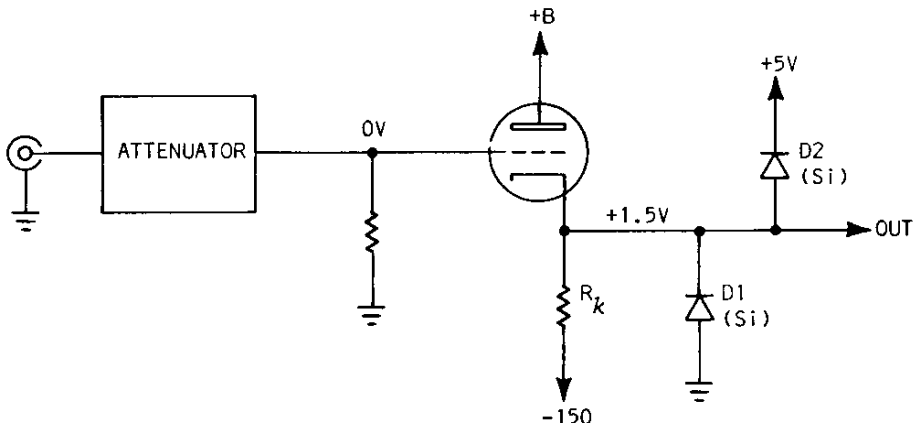


Fig. 3-26. Diode protection.

Although these values are not precise, they suffice for the purpose of this book. All following discussions consider the above as true conditions. Further, all semiconductors in this book are identified as: GaAs, Ge, or Si, when applicable.

2.1-volts negative voltage swing

Diode D1, of Fig. 3-26, conducts when cathode voltage reaches -0.6 V; then clamps at -0.6 V; and turns off when cathode voltage becomes more positive than -0.6 V. Negative signals may vary from quiescence, +1.5 V to -0.6 V -- a maximum negative voltage change of 2.1 V.

4.1-volts positive voltage swing

Clamping circuitry allows 4.1-volts positive-voltage changes. The cathode of D2 returns to +5 V. Therefore, when V1 output rises to +5.6 V, D2 turns on. This represents 4.1 volts more positive than quiescence. Output voltage then extends from -0.6 V to +5.6 V, or a "voltage window" of 6.2 V.

positive clamp endangers tube

A positive clamp (D2) in the circuit creates the need to protect V1. Assume a positive 10 volts appears at V1 grid. D2 clamps as V1 cathode passes +5.6 volts and, since a positive bias condition exists, tube current increases sharply. Positive tube elements must dissipate excessive power.

Fig. 3-27 includes a protective circuit which reduces electrode power-dissipation requirements. Components D3, C8 and R8 function to reduce plate voltage during overload conditions.

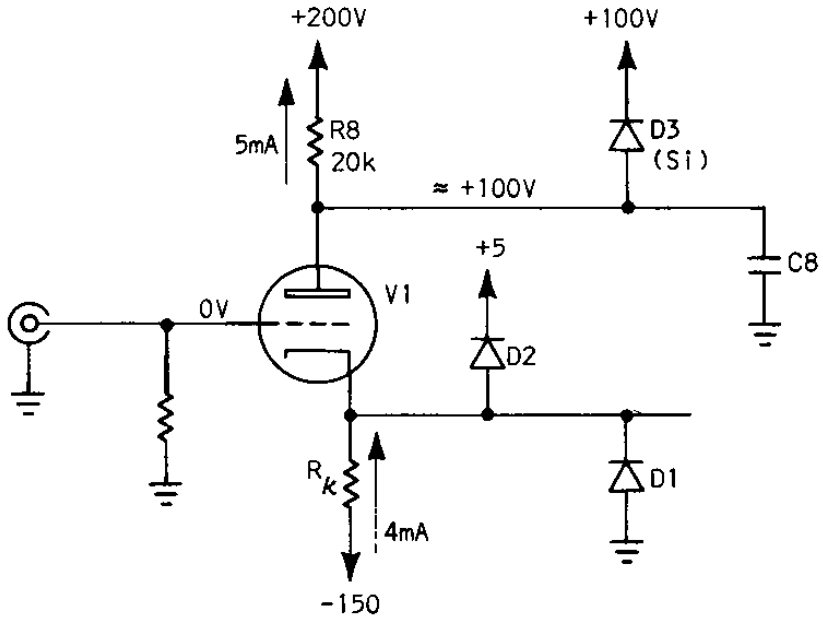


Fig. 3-27. Diode protection.

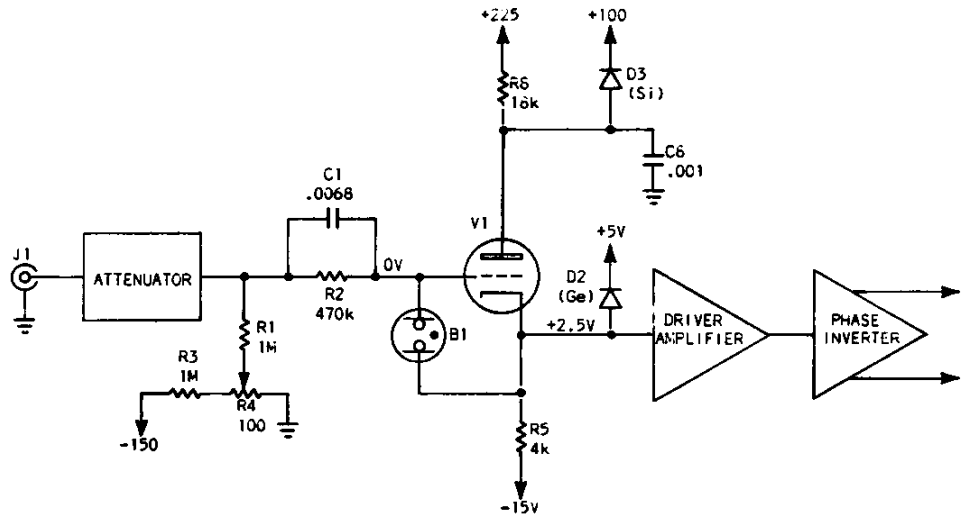


Fig. 3-28. Input amplifier.

At quiescence both V1 plate current and D3 current flows through R8 developing about +100 V plate voltage. C8 filters diode noise. Protective action begins when D3 disconnects. Assume again +10 volts at the control grid: D2 clamps causing a large plate current increase. This increased tube current drops more than 100 volts across R8, disconnecting D3. For each mA increase in plate current, plate voltage drops 20 volts. Tube parameters change drastically, but tube power (EI) remains at a safe level.

protection and correction

The longtailed input amplifier of Fig. 3-28 incorporates most of the protective and corrective concepts covered.

negative grid current

Grid resistor RI returns to a negative voltage source. With R4 properly adjusted, negative grid current develops zero volts from V1 control grid to ground.

positive grid current

Positive grid current through R2 limits during large positive input excursions. Bypass capacitor C1 acts as a current source to discharge input capacitance.

glow lamp

Neon glow lamp B1 fires to maintain grid-to-cathode difference at a maximum of 50 to 60 volts.

output clamp

Diode D2 protects the driver amplifier by clamping when positive signal excursions reach +5.2 volts. The driver amplifier includes a negative clamp.

Longtailed cathode followers, as described, have two major disadvantages:

1. They do not follow negative-going signals with the same fidelity as positive-going signals.

2. High voltage is required.

positive risetime "faster" than negative

Output capacitance charge time is restricted only by internal impedance (rk) for positive signal swings. Therefore, positive signal swings are at a *gm* determined rate. On the other hand, charge time for negative signal swings is determined by external cathode resistance. RC time for negative and positive signal swings can differ by hundreds of units. There is no cure for single-ended longtailed amplifiers. The negative slope always exceeds positive risetime. However, the negative slope should be linear for a wide range of signal amplitudes. To do this the longtail must provide a constant current over the range of signal amplitudes.

active device longtailing

pentode longtail

One solution makes Rk dynamic. (Fig. 3-29). A pentode substitutes for Rk. Pentodes operate with a very high plate resistance. This extends the negative supply many hundreds of volts and makes the constant-current characteristics extremely flat. 5-mA longtail current flows during both positive and negative input excursions. During positive excursions output capacitance charges through rk of the cathode follower. Negative signals reduce follower conduction, but 5-mA longtail current continues to flow. The quantity of longtail current now flowing as cathode current is available to charge Co. The circuit is very successful but requires rather high voltage supplies.

transistor longtail

Transistors have characteristics very similar to pentodes (Fig. 3-30). Q1 determines total circuit current and adjusting base voltage sets the output DC level to near zero volts. Supply voltages are low and constant-current characteristics are excellent.

feedback

Another solution is possible when driving a cathode-follower stage push-pull. The longtail is passive but an additional current source charges output capacitances (Fig. 3-31).

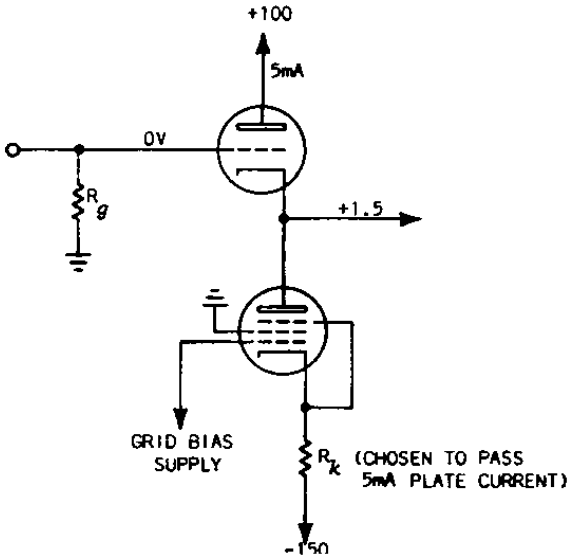


Fig. 3-29. Dynamic longtail using an electron tube.

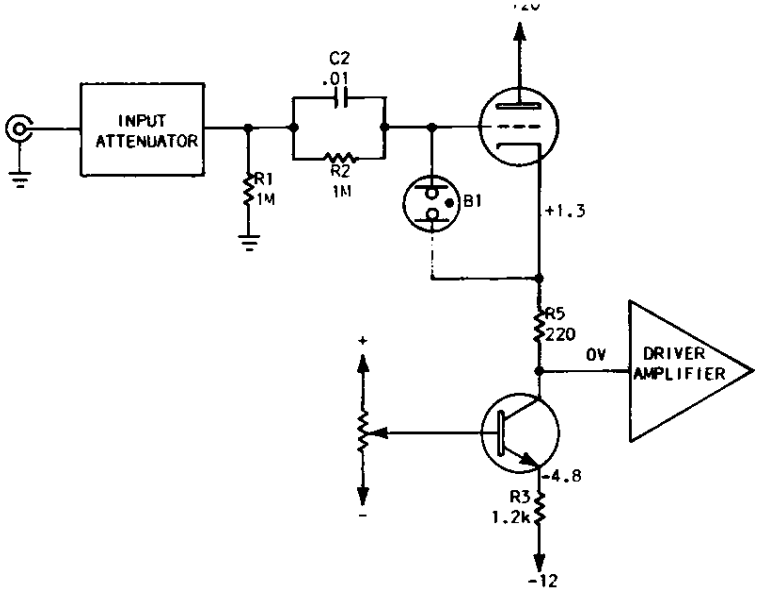


Fig. 3-30. Dynamic longtail using atransistor.

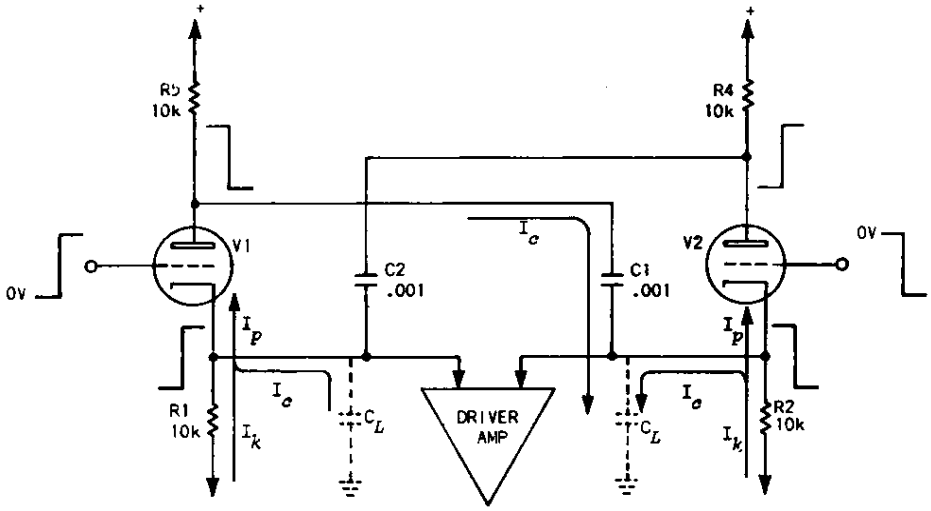


Fig. 3-31. Cathode followers with feedback.

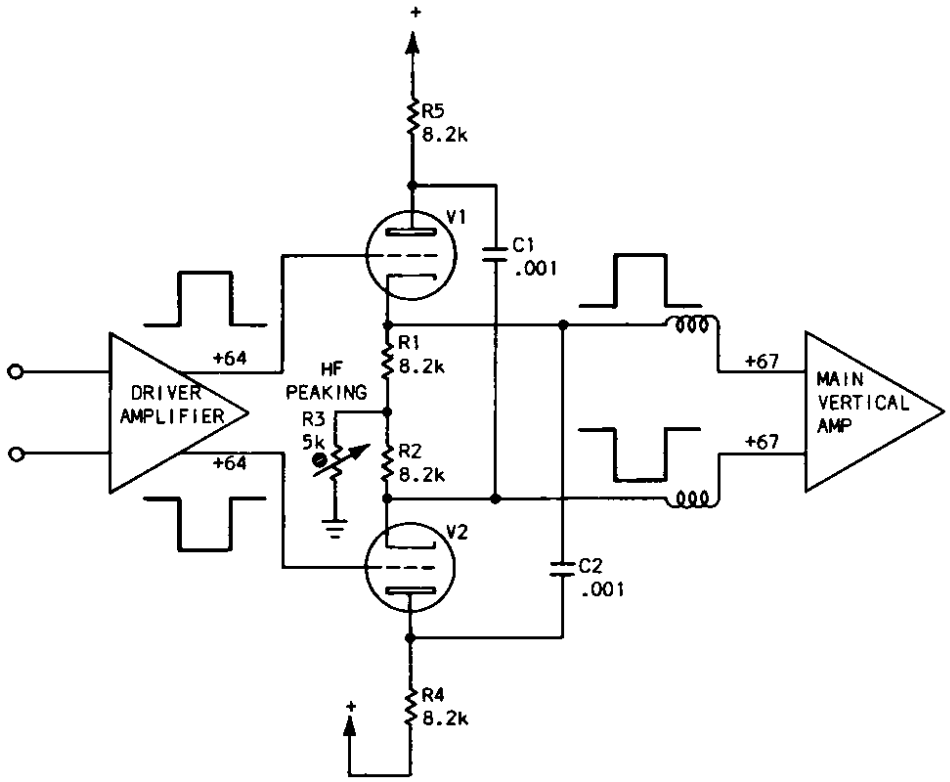


Fig. 3-32. Output amplifier with feedback.

V1 and V2 are push-pull driven cathode followers. Assume a positive step waveform applied to the grid of V1. A step of opposite phase but equal amplitude drives V2. Full cathode current and load capacitance determine V1 following rate. Time constant R2CL normally controls V2 following rate. However, V1 plate goes negative at V1 cathode rate and this signal couples to V2 cathode. Coupling capacitor

unity gain at plate or cathode

C1 is large compared to CL so load capacitance quickly charges, allowing V2 cathode to swing negative at the signal rate. C2 develops no charge since the stage has unity gain viewed from cathode or plate and the in-phase signals change at the same rate. Action is the same with phase reversal except the negative-going current source (plate of V2) assists V1 cathode.

In Fig. 3-32 the concept just discussed is shown as a preamplifier output stage, essentially a push-pull cathode follower with high-frequency balancing networks.

gm adjust termed HF PEAKING

Full cathode current and load capacitance determine the rate at which a cathode follower follows a positive-going signal; so adjusting R3 controls high-frequency response, thus the name HF PEAKING.

Miller-effect

A small Miller-effect, due to plate loading is present. For this reason cathode followers frequently drive this stage.

negative-input character-istics

Miller-effect, a degenerative signal fed to the grid from the plate by the grid-to-plate interelectrode capacitance, increases the input capacitance to an amplifier. Usually considered a disadvantage, Miller-effect can be utilized to improve overall response of an amplifier. It is one method of combating "negative-input resistance characteristics." These negative" properties, to which a longtailed follower is especially prone, distort input waveforms.

input waveforms distorted

ringing

Under some conditions, a follower (cathode, emitter, or source) rings when a high-amplitude "fast" step is applied. This explains the name "negative-input resistance characteristic." The major effect upon vertical amplifiers occurs at the input amplifier. Capacitance at the grid changes during signal transit, upsetting the input attenuator compensation. Input capacitance is greater during "fast" signal changes than "slow." The cure increases quiescent capacitance so that input capacitance remains the same for all input waveforms.

Earlier the point was made that CF gain reduced C_{gk} because of the reduced voltage across the capacitance: $C_g = C_{gk}(1 - AV)$, if AV = 0.95, then only 5% of the input voltage develops across C_{gk}. C_{gk} is only 5% of listed value.

Fig. 3-33 and 34 show an initial AV of 0.5. C_gk then is 50% of listed value. This is the change of input capacitance that affects compensation of the input attenuator. Total circuit reaction is rolloff.

From the standpoint of "negative-input resistance" the explanation takes a different tack but states the same thing.

charging input capacitances

Understanding properties of a "negative-input" requires, initially, application of current-voltage relation for a charging capacitor (Fig. 3-33). Capacitances involved are those making up input-capacitance of a cathode follower. Assume a "perfect" step applied. The input rises from a quiescent level to its peak voltage (V_{pk}) in zero seconds (T_0). Output cathode voltage rises from quiescence to V/ at the input rate. Amplitude of voltage V1 depends on the values of the capacitive voltage divider, C_gk and C_k.

I_P increases

Full-step amplitude appears at the grid while a portion develops across C_k. The initial voltage difference, positive bias, creates an increased plate-current demand (Fig. 3-34). This increased current charges C_k toward grid potential but also flows through C_gk.

regeneration

Input capacitance charging current (I_x) originates in the signal source flowing through internal source impedance R_i. This reactive current develops a voltage across R_i which adds to the grid voltage, which increases IP' which increases I_x, which increases the drop across R_i, which . . . . Even if grid clamping occurs, initial regeneration distorts the input waveform.

Since the current flows through C_gk, label it reactive: I_x, and since the effect of Ix reduces input impedance, give it a negative sign.

negative resistance

The initial exponential rise from V1 toward peak, across C_k, indicates a resistive component. This resistance has a relationship to R_k and r_k which decreases with I increases. Give this resistive element a negative value also.

-RC effect

If both a negative reactive current and a negative resistance are indicated, then an RC equivalent represents the effect.

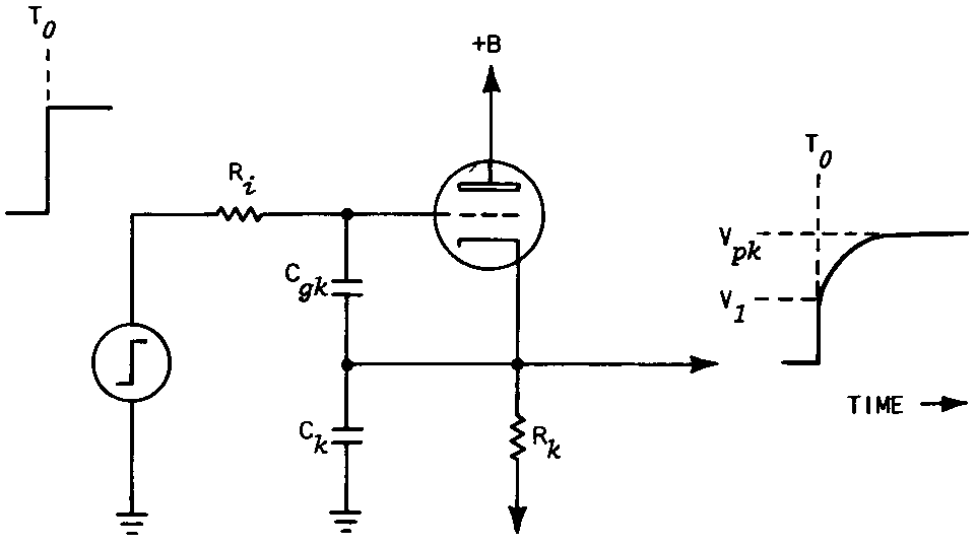


Fig. 3-33. Cathode-follower inputcapacitance.

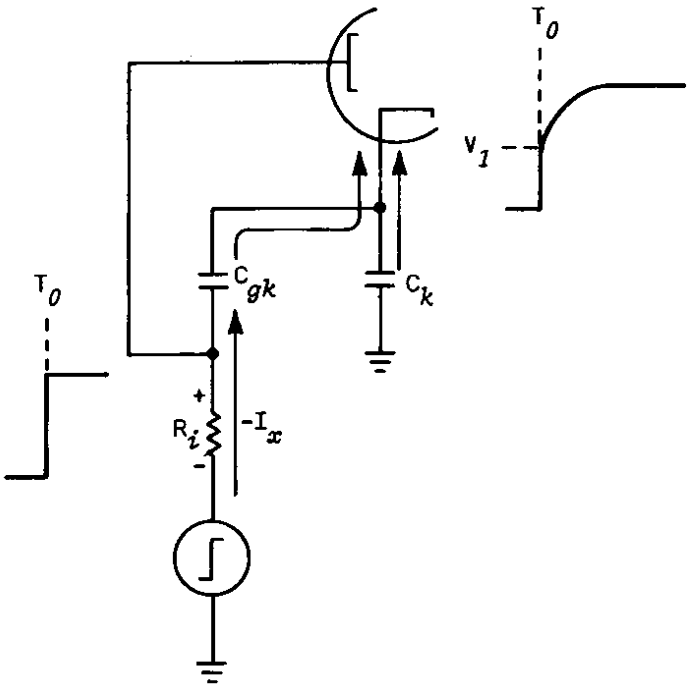


Fig. 3-34. Negative input characteristic current.

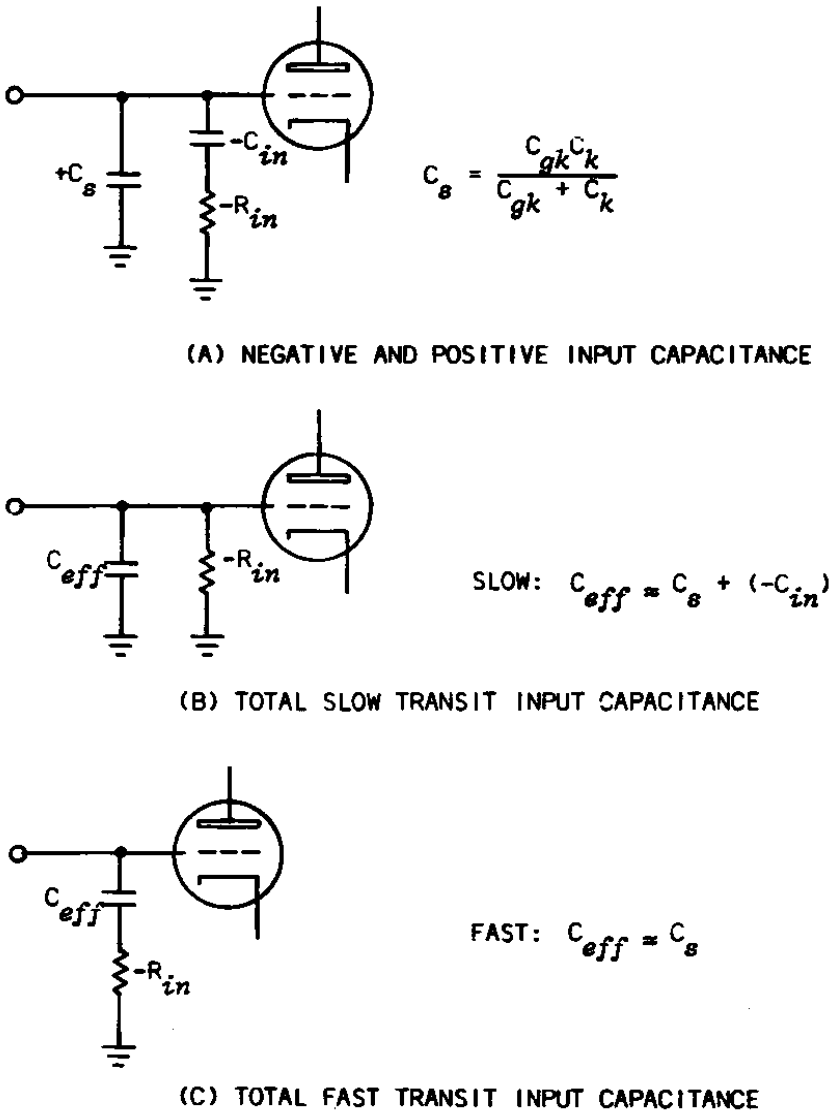


Fig. 3-35. Input capacitance

equivalent circuits

Refer to Fig. 3-35, a schematic of equivalent input circuits. These three equivalent circuits are the basis for illustrating compensation concepts. (A) shows input capacitance lumped into one component, C_s. (B) and (C) illustrate the change in effective input capacitance (C_{eff}) with signal transit time.

input C lowest at low frequencies

At low frequencies, where $-I_x$ flows and exhibits capacitive phase shift, C_s and $-Ci_n$ add:

$$C_{eff} \approx - Ci_n = 1.9 \text{ pF},$$

Higher frequencies cause less $-I_x$ phase shift until the current appears resistive. At this point C_s defines total input capacitance:

If $C_s = 2.4$ pF and $- Ci_n = 1.9$ pF,

then:

$$C_{eff} \approx Ci_n + C_s \approx -1.9 + 2.4$$

$$C_{eff} \approx 0.5 \text{ pF at low frequencies,}$$

and:

$$C_{eff} \approx C_s \approx 2.4 \text{ pF at high frequencies.}$$

The information given leads one to think that a designer should either increase grid-signal losses or make input capacitance flat over the input bandwidth. This is a fair approximation of compensation techniques: Grid-signal losses are introduced, or C_{eff} *is made* to appear constant at all frequencies, or the techniques are combined.

Two methods, shunt RC compensation and Miller-effect degeneration, prevent $-I_x$ flow in R_i. These methods thus maintain input capacitance constant.

R_cC_c the source for $-I_x$

Shunt RC compensation appears in the grid circuit. Fig. 3-36 includes compensation components shown as C_c and R_c. R_cC_c equal the predicted value of $-(R_{in}\ C_{in})$. When the "negative" components demand current, the compensating components demand equal-amplitude "positive" current. $-I_x$ then flows in a "positive" direction through R_cC_c to charge $-Ci_n$. None of the reactive current flows in R_i, therefore capacitive source loading, C_s, is flat.

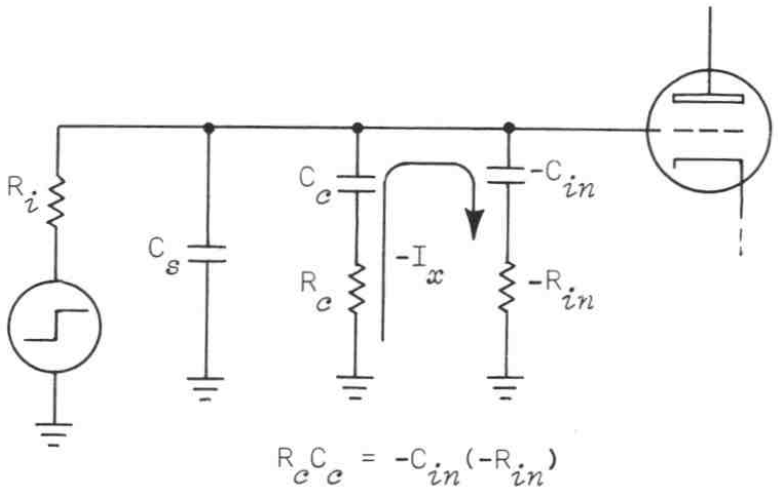


Fig. 3-36. Shunt RC compensation.

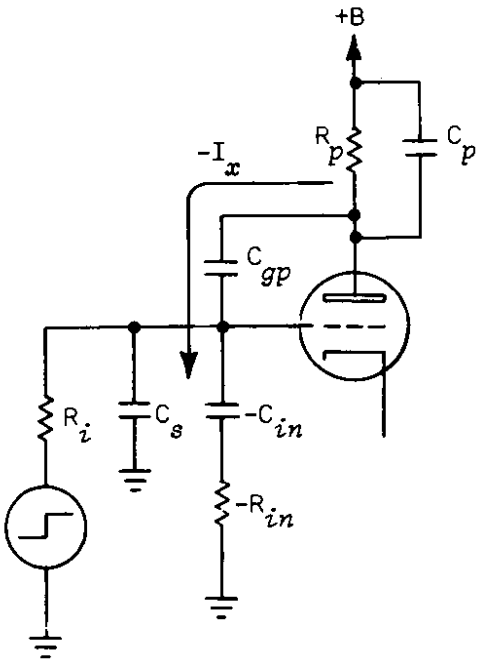


Fig. 3-37. Compensation using Miller effect.

Plate-compensation (Miller-effect) also contains $-I_x$ within the grid circuit, causing a constant input capacitance. Fig. 3-37 shows the plate circuit functioning as the source for $-I_x$. Here a signal, out-of-phase with the input, develops across R_p. A portion of this signal energy couples back through the Miller capacitance as $-I_x$. Again, no current flows in R_i so Cs can represent input capacitance to all signals.

Miller capacitance, the source for $-I_x$

C_{gp} is interelement capacitance which is supplemented in a few cases by an additional shunt capacitance. C_{gp} has a component value which changes with plate gain: If the plate were to do the impossible and follow input signals 1:1, no voltage difference would appear across C_{gp} and no current would flow. C_{gp} would be some infinitely small value. In earlier descriptions C_{gp} returned to signal ground, +B. Input signals across C_{gp} caused reactive current flow. Current quantity depended upon the component value of C_{gp} and the voltage across it. Imposing plate gain, as in Fig. 3-37, increases the voltage across C_{gp}, therefore the current quantity. To input circuitry, capacitance appears to increase with gain. One expresses shunt Miller capacitance by the formula: $C_m = C_{gp}\ (1+A_V)$; if C_{gp} were 3 pF, and A_V were 10, then C_m would be 11. This is the concept used to compensate for "negative input characteristics."

Miller capacitance increases with AV

plate gain creates feedback current

A change in cathode current causes a voltage change across R_p, which in turn creates feedback current from plate to grid. Plate risetime determines plate cμrrentsignal amplitude or A_V. For slow rise signals R_p sets gain. However, C_p shunts R_p during fast rise signals reducing gain toward zero. Feedback current and input capacitance decrease with risetime. This is in keeping with $-I_X$ demand.

feedback exponential

Initially the cathode waveform follows the input step. During this rapid change, C_p shunts R_p preventing plate gain thus feedback current. When the cathode begins to ascend exponentially, plate-current rate-of-change reduces, developing a plate signal across R_p. Plate-to-grid feedback now becomes $-I_X$. R_p C_p gain characteristics are exponential, as the cathode, providing feedback current that satisfies $--I_X$ demand. Here also, no reactive current flows in R_i so C_s represents a fixed input capacitance.

From a frequency standpoint C_p shunts R_p more at high frequencies than low. Gain decreases exponentially with frequency. C_m, then increases low-frequency input capacitance, decreasing with frequency so that effective input capacitance will be flat at all frequencies.

suppressor resistors

Stray inductive components can resonate with changing input capacitance causing overshoot (ringing). A small suppressor resistor in series with the grid signal imposes losses. These resistors in values of 10 to 50 ohms damp the regenerative power.

None of the methods function perfectly and individual characteristics overlap. Therefore, one may expect to find individual or combined methods.

Generally one finds in slowest rise circuits a suppressor resistor, then in decreasing risetime order: plate compensation, plate compensation combined with a suppressor, shunt RC compensation and shunt RC combined with plate compensation.

"Negative-input-characteristics" compensation appears in many amplifier configurations whether the active device be electron tube or semiconductor Fast-rise input amplifiers always use compensation.

plate compensation

The circuit of Fig. 3-38 uses Miller-effect to compensate negative-input characteristics. A small voltage out-of-phase with the input signal develops across R5 at low frequencies. Capacitance, plate-to-grid, couples this degenerative signal to the control grid preventing oscillations. Shunting of R5 by C5 increases with frequency, reducing plate-signal amplitude. Quantity of feedback increases with plate-signal amplitude. Degeneration, thus, capacitance due to Miller-effect develops most at low frequencies, decreasing with an increase in frequency. The result is equal input capacitance at all frequencies. Or, negative current flows from plate to grid rather than through input circuit components.

suppressor resistor

Suppressor resistors, as R3 in Fig. 3-39, oppose current flow, minimizing the quantity of negative current. Suppressor resistors, used alone at the input amplifier, generally indicate narrower bandwidth than instruments employing plate compensation.

shunt RC compensation

Currently popular shunt RC compensation is shown in Fig. 3-40. C3 and R3 act as a current source for negative input components. The positive-current demand of R3C3 equals the negative-current demand of $-(R_{in}\, C_{in})$.

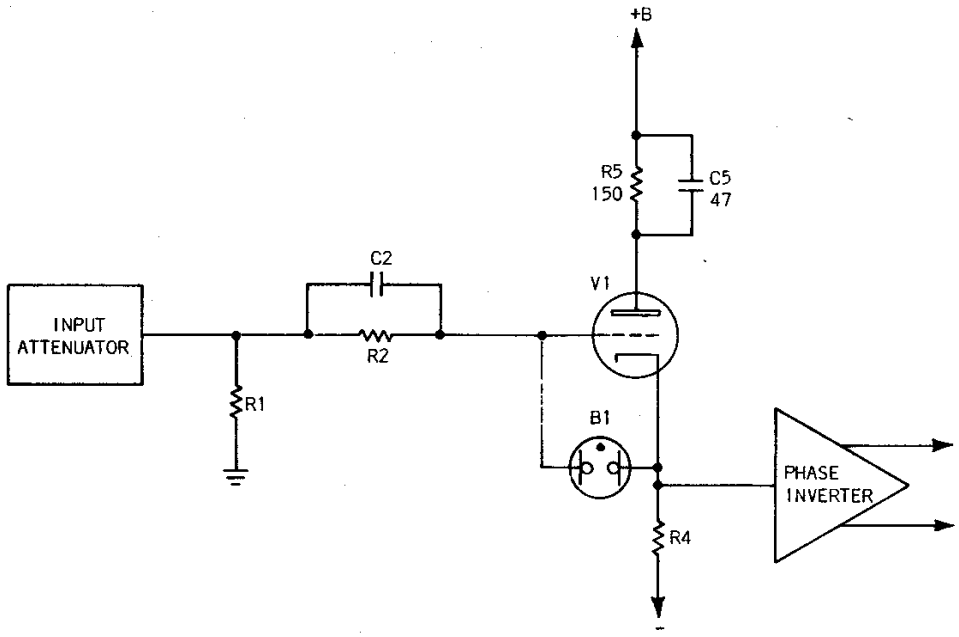


Fig. 3-38. Plate compensated input amplifier.

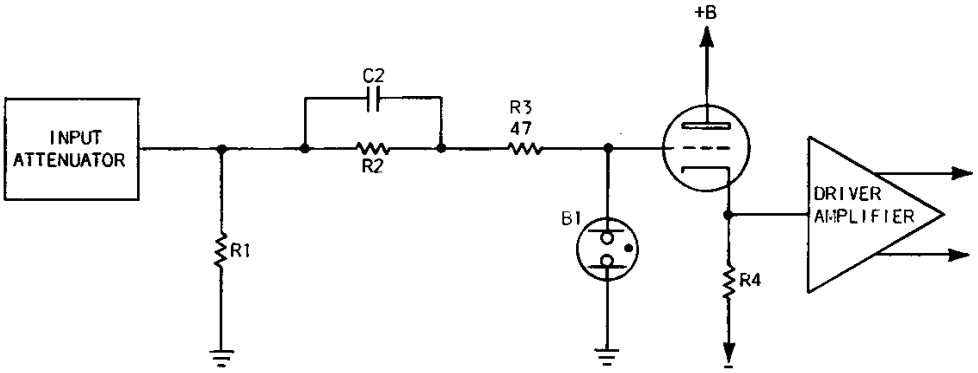


Fig. 3-39. Input amplifier with suppressor.

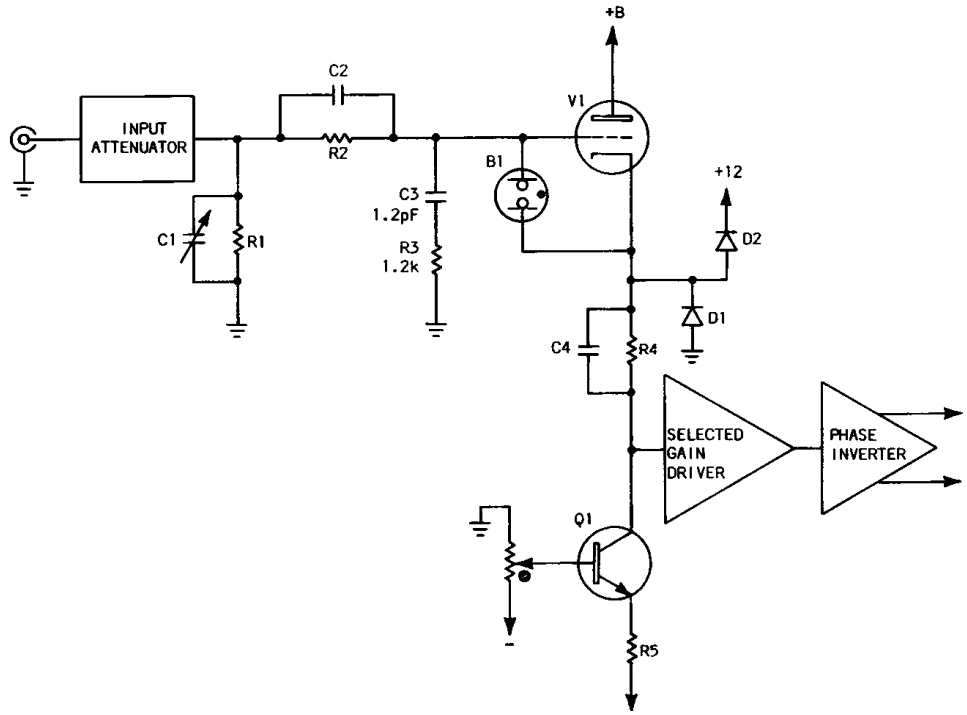


Fig. 3-40. Input-amplifier shunt RC compensated.

Fig. 3-40 incorporates many of the cathode-follower concepts presented:

C1 shunts grid resistor R1, providing input-voltage-divider compensation.

C2 bypasses grid-limiting resistor R2.

C3 and R3 compensate for negative-input characteristics.

Neon lamp B1 protects against grid-to-cathode overload.

Diodes D1 and D2 clamp to protect the input circuit of the selected-gain driver.

R4 is a dropping resistor. V1 self biases about 1.5-volts positive. Cathode current through R4 allows one to adjust the voltage at the collector of Q1.

Q1 dynamically longtails V1. One adjusts base bias for near zero volts to the selected-gain driver.

switched-gain block

Fig. 3-40 is the basic circuit of a switched-gain input amplifier. Chapter 2 pointed out how input deflection factor was extended by two methods: "Stacking" attenuators or, to reduce input capacitance, gain switching amplifiers in calibrated steps.

Fig. 3-41 is a block diagram of switching logic necessary to drive a phase inverter at a constant deflection factor. Blocks labeled Input Attenuator, Input CF and Selected-Gain Driver mechanically gang to the VOLTS/DIV selector. Deflection factor, at the input jack, is from 20 millivolts to 10 volts per division selected in a 1-2-5 sequence. The input dividers reduce the nine input-deflection factors to three: 20 millivolts, 50 millivolts and 100 millivolts. Selecting cathode-follower gain of 1 or 1/5 gives an input-deflection factor to the selected-gain driver of 20 or 50 millivolts per division. The selected-gain driver can now have a constant output-deflection factor. The circuit concepts of interest are those of the input cathode follower.

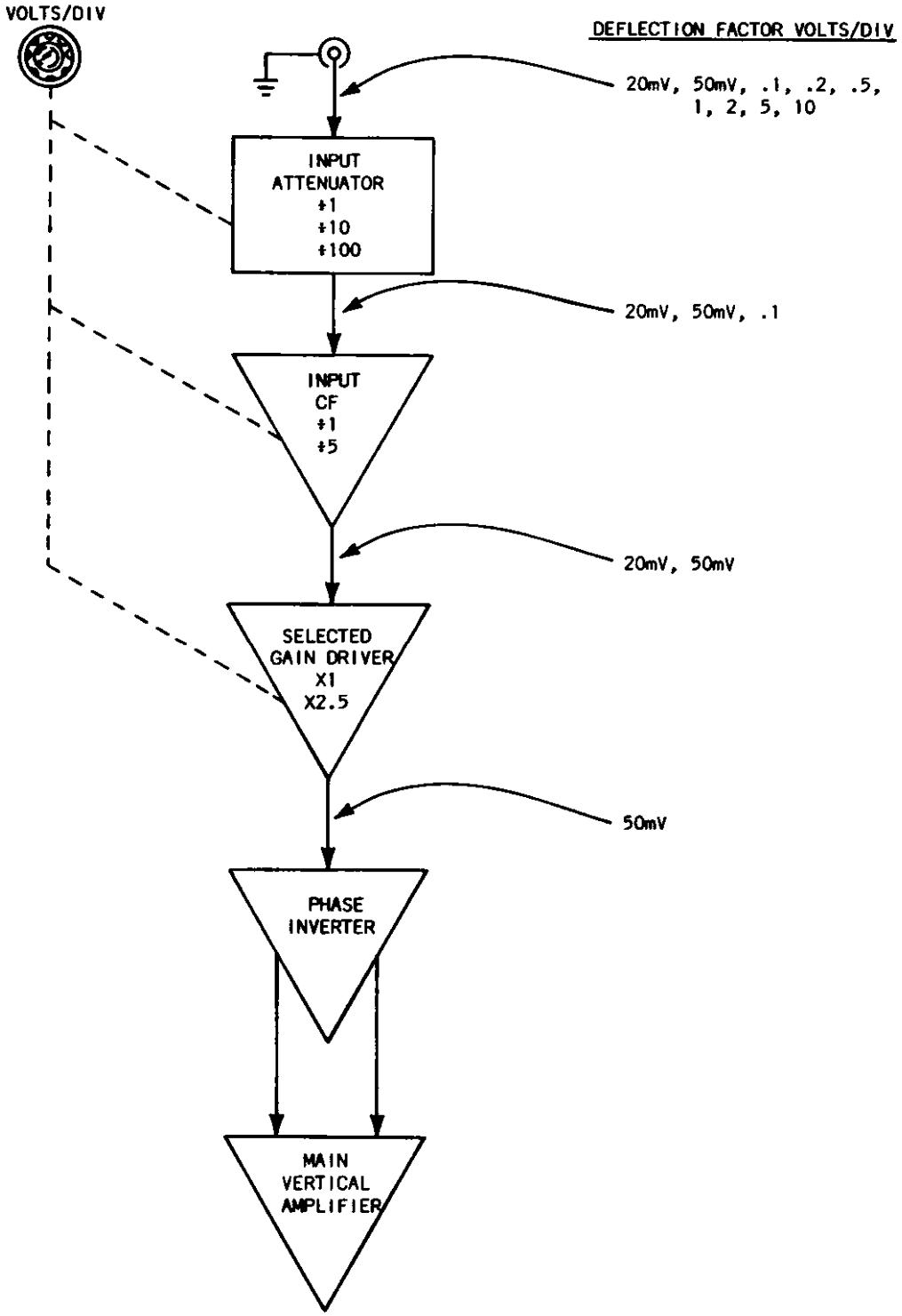


Fig. 3-41. Switched-gain amplifier.

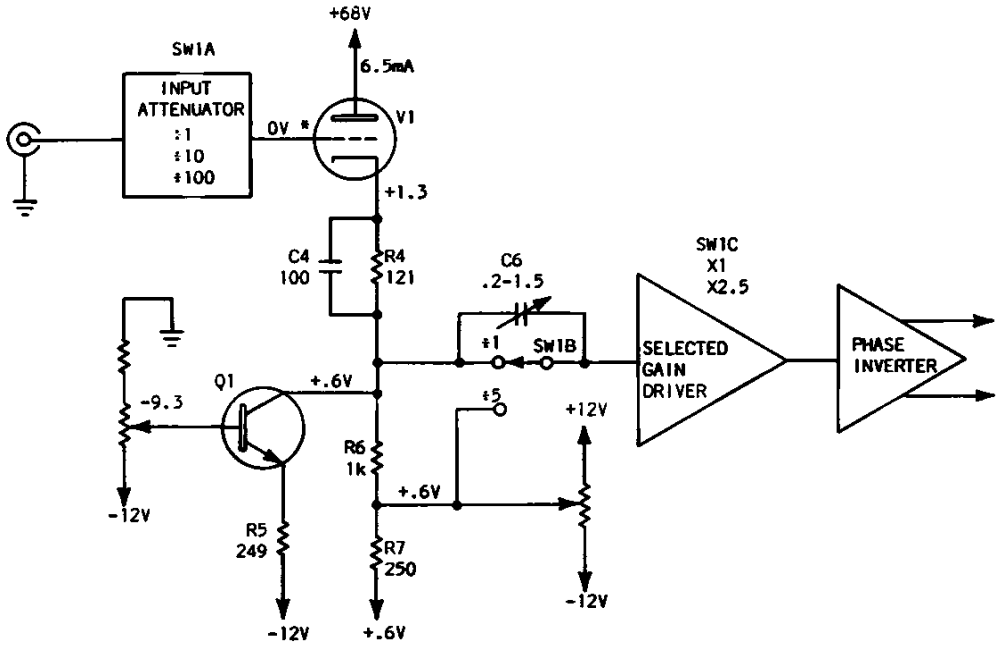


Fig. 3-42. A., IS input-amplifier cathode circuitry.

CF output either 20 or 50 mV/div

Assuming unity gain, deflection factor at Ql's collector equals the factor at V1's grid.* (Fig. 3-42).

Signal voltage at the top of R6 or R7 drives the selected-gain driver. With SW1B positioned as shown, a deflection factor of 20 mV or 50 mV exists at the collector of Q1. Selecting 100 mV/div at Q1's collector places SW1B in the down or 15 position. Since R6 and R7 is a 5:1 divider, drive to the selected-gain driver is 20 mV/div. Deflection factor out of the input cathode follower is either 20 or 50 millivolts.

*Unity gain provides convenient figures. A more realistic figure, considering actual CF gain and drop across R4, is 80% of V1 grid signal (Ay = 0.8 at collector Q1).

compensated voltage divider

C6 makes R6-R7 a compensated voltage divider. Distributed capacity shunts Q1 and R7. With SW1B positioned as shown, no additional capacitor is necessary -- C6 is shorted. With SW1B in the down or ÷5 position, C6 shunts R6 requiring an adjustment for proper capacitive voltage division.

setting quiescent voltages

No quiescent voltage difference should exist between the ÷1 and ÷5 positions of SW1B. With the input jack grounded, one switches the VOLTS/DIV selector through its range and should observe no vertical CRT deflection. If a quiescent voltage appears across R6, switching from ÷1 to ÷5 appears as a signal to the following stages. Amplified, it vertically deflects the CRT trace.

The quiescent levels result from V1 self-bias resistive values, and adjustable longtailing. V1 self-bias determines the voltage at the top of R4. Q1, controlling total cathode current, sets the voltage drop across R4. Q1 base-voltage adjustment sets the collector level to the proper operating point for following direct-coupled stages. Returning the junction of R6-R7 to a variable voltage allows one to adjust for no-voltage difference across R6. Voltage return for R7 approximates Q1 nominal collector level. At quiescence, with voltage levels adjusted, no discernible deflection results from actuating SW1B.

compensated voltage divider

C4 compensates R4. One must consider R4 as part of the resistive network across which an input signal develops. The capacitance across R4 compensates as in the other voltage-divider networks already discussed.

For a complete input amplifier, combine the components of Fig. 3-40 and 3-42.

Fig. 3-43 depicts the input stage of a broadband vertical preamplifier. A low-resistance network shunts the cathode resistor which reduces gain to 50%.

grid circuit

Begin circuit analysis with the grid circuit. Grid resistors R1 returns to an adjustable negative-voltage supply, consisting of R8, R9, R10 and the -15 volt supply. One adjusts R10 for a voltage equal to the drop across R1 which results from negative grid current (current created when the heated control grid emits electrons).

Grid limiting develops across R2. C2 bypasses R2, rapidly charging input tube capacitance.

negative R

R11, R12 and C12 compensate for negative-resistance input characteristics. R11 is a suppressor. Plate signals across R12 develop Miller-effect. C12 bypasses R12 to reduce degenerative feedback at high frequencies.

protection

B1 and D1 are protective devices. B1 ignites during signal overloads and D1 clamps negative excursions at about 0.2 volts below ground.

controls

Location of controls VARIABLE VOLTS/DIV (R6) and Gain (R5) in the cathode circuit of V1 complicates

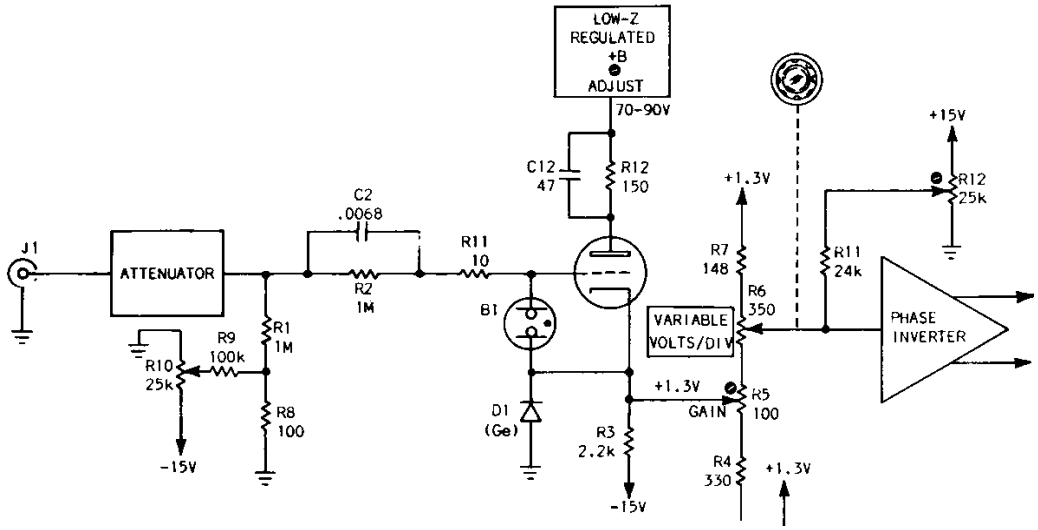


Fig. 3-43. Constant output impedance CF.

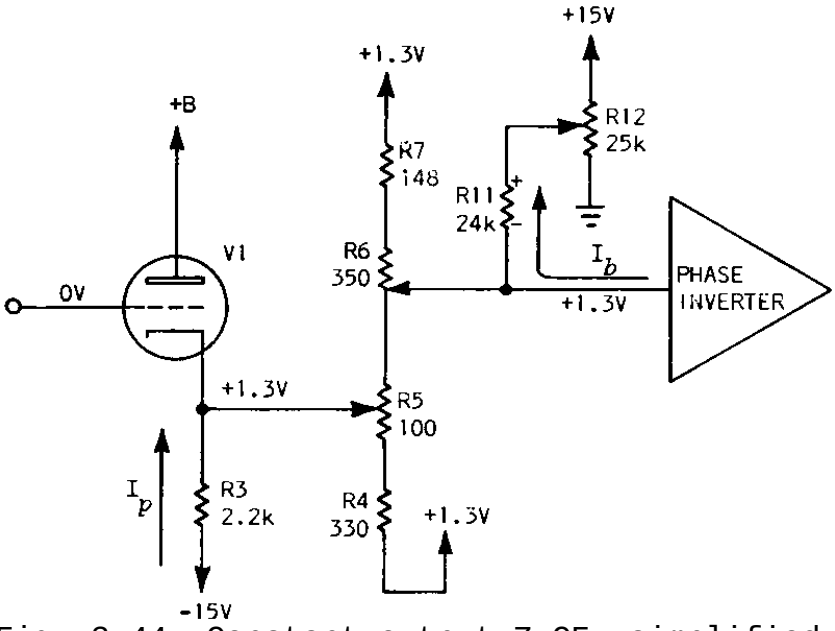


Fig. 3-44. Constant output Z CF, simplified.

this amplifier. These controls usually appear in one or more later amplifier stages, frequently the phase inverter. In this case, placing Gain and VARIABLE controls at the input amplifier improves overall vertical response.

R6 extends to the front panel providing the operator a continuously variable uncalibrated between-step deflection-factor control. Adjusting R5 Gain calibrates. One adjusts R5 with R6 set to the least resistance between the wiper of R6 and the connection with R5. (The lower extreme as shown in Fig. 3-43). For the variable (R6) to be most useful, no vertical deflection should occur when one moves R6 through its range.

no quiescent current flows in VARIABLE or Gain

Preventing quiescent current flow through resistive network R4, R5, R6 and R7 allows one to use the VARIABLE without deflecting the vertical display. When a current flows through R6, moving the wiper of R6 creates a voltage change at the phase-inverter input. Following stages amplify this voltage change, vertically deflecting the CRT. V1 plate supply, R4 return, R7 return and adjustment R12 set circuit conditions for zero current through network R4, R5, R6 and R7. Under no signal condition, one then varies R5 or R6 without causing vertical deflection.

Refer to Fig. 3-44, a simplification of Fig. 3-43. Applying equal voltage to the four terminals prevents

quiescent current flow through R4, R5, R6 and R7: Both R4 and R7 return to +1.3 volts. Wipers of R5 and R6 rest at 1.3 volts. Zero current is then demanded.
R4 and R7 return to a fixed supply. Self-bias of V1 sets R5 wiper potential. By adjusting V1 plate return, one changes V1 tube parameters forcing a self-bias equal to the return voltage for R4 and R7.

Current originating in the phase inverter develops a voltage across Rll and R12. This causes the same potential to appear at the wiper of R6 as at other terminals. Setting the wiper of R12 more than 1.3-volts positive demands all phase-inverter current flow through Rll and R12 rather than R4, R5, R6 and R7. R11 and R12 are high resistances to prevent signal shunting.

Rk = 200 Ω

External cathode resistance remains constant at all settings of R5 and R6. Total plate current flows through R3 under no-signal conditions. R3 functions as a longtail. However, signal voltages cause currents to flow through all cathode-circuit resistors. These shunt currents create a total R_k of approximately 200 ohms. Signal voltages develop across a divider consisting of r_k and R_k. Wideband stability depends upon this ratio remaining constant. The circuit configuration shown maintains R_k constant at all settings of Gain and VARIABLE controls.
100% of the CF signal develops at the wiper of R5. R5 setting establishes signal percentage across R6 and R7. Because of resisters Rll and R12, varying R6 affects no shunting. R5 is not so obvious. Set for maximum gain, the wiper of R5 rests at the R5 to R6 connection: R4 and R5, paralleled by R6 and R7, shunt R3. At nominal gain R5 is centered: One-half R5 appears in each parallel leg shunting R3. Minimum-gain setting causes R5, R6 and R7, paralleled by R4, to shunt R3. Total R_k does approximate 200 ohms over the total range of R5.

R_k 208 Ω at maximum gain

Fig. 3-45 develops equivalent circuit cathode resistance. Assume r_k is 200 ohms. Fig. 3-45A shows the desired equivalent circuit: Input signals, modified by μ, develop across divider R_k and r_k. Fig. 3-45B solves for maximum gain R_k: Resistive network R4, R5, R6 and R7 is an equivalent shunt resistance of 230 ohms which parallels R3.

R_k 204 Ω at mid gain

R_k 196 Ω at low gain

R_k resolves to 208 ohms. Nominal gain results in 204 ohms R_k (Fig. 3-45C). Lowest resistance R_k occurs at minimum gain: R_k = 196 ohms (Fig. 3-45D). Referred to nominal gain, R_k varies from 2% at maximum gain to 4% set at minimum.

small input R to the phase inverter varies

This CF circuit presents a low resistance to the phase inverter, as is required. The phase-inverter input resistance does, however, change with Gain and VARIABLE adjustments.

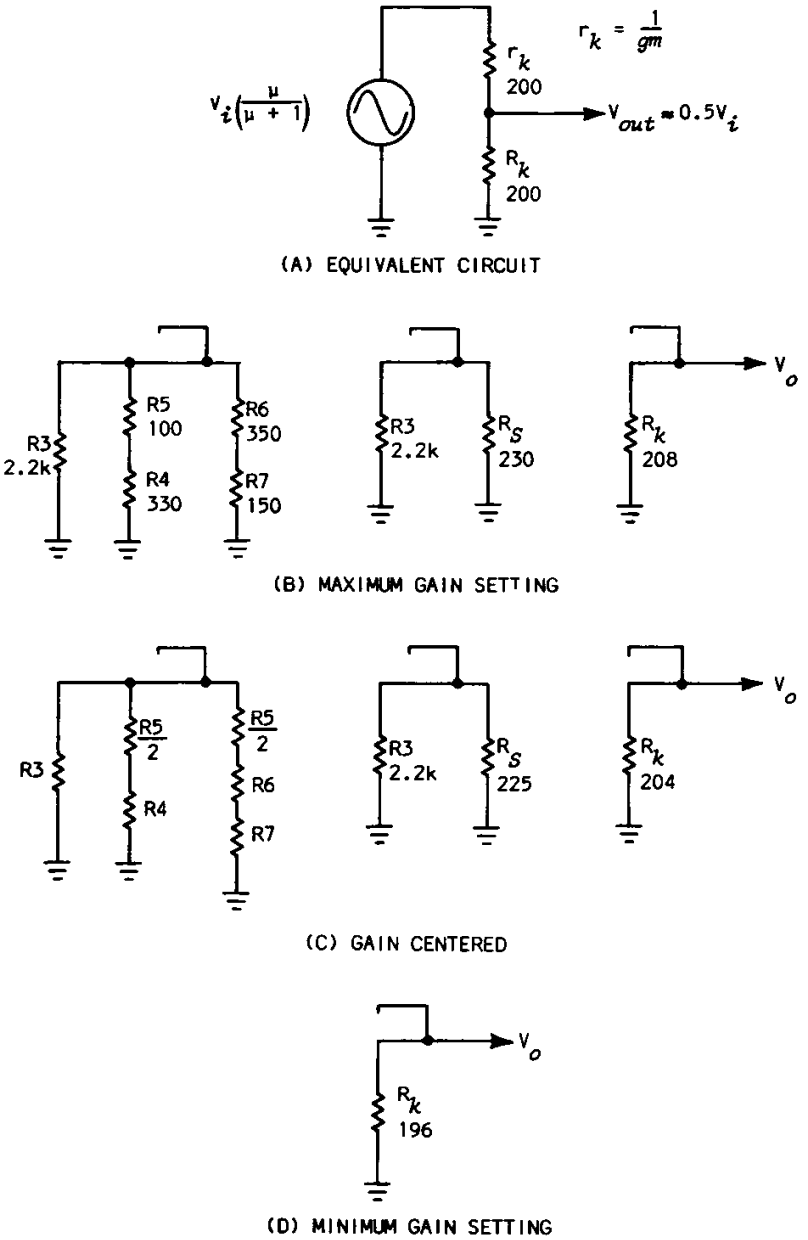


Fig. 3-45. Equivalizing cathode resistance.

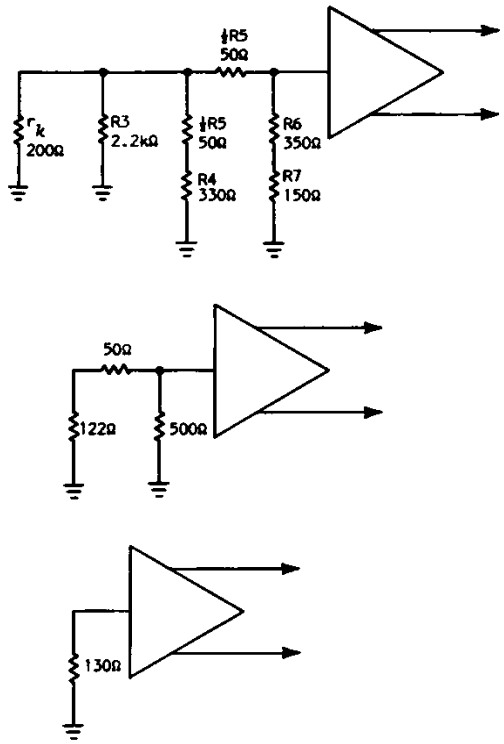


Fig. 3-46. Nominal-gain phase-inverter input resistance.

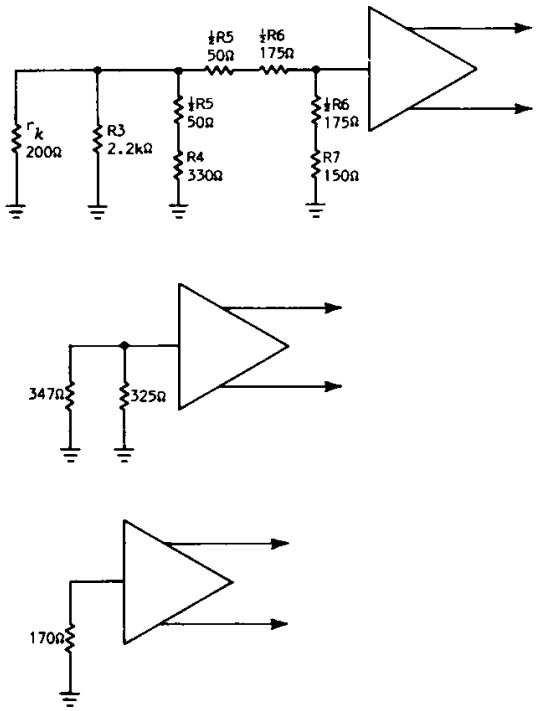


Fig. 3-47. Phase-inverter input resistance, variable centered.

gain changes R6 input R

Fig. 3-46 shows input resistance as 130 ohms, with in calibrated position and R5 centered. Input resistance changes with gain settings from a minimumof 100 ohms to a maximum of 150 ohms. 100 ohms represents high gain; 150 low gain.

VARIABLE changes input R

Assume nominal gain. Actuating the VARIABLE increases then decreases phase-inverter input resistance. Input resistance varies from 130 ohms through 170 ohms to 120 ohms. 170 ohms occurs with the VARIABLE centered (Fig. 3-47).

Many of the cathode-follower concepts are not peculiar to tube-type circuitry. Source or emitter followers exhibit similar characteristics modified by active-device peculiarities.

Emitter follower (EF) symbols and terms are those common to all followers: high input impedance, low output impedance, minimized Miller-effect capacitance, and longtailing to stabilize and emphasize all characteristics. Differences, however, exist.

input Z lower than CF or SF

Terms such as *low* and *high* can be misleading when they refer to impedance values. Impedances of an emitter follower when compared to source followers or cathode followers are of a different magnitude, much lower. For example, the input impedance of an EF is high compared only to other transistor configurations. Input impedance is neither high enough nor stable enough to meet input-amplifier requirements. The loading on an input-attenuator network would be too great. Cathode followers and source followers are for this reason the only followers used as preamplifier input amplifiers. Emitter followers may be used in all other circuits of a vertical amplifier.

EF never used as input amplifier

the tube and FET are *on* devices

Another difference appears during basic operating considerations. The electron tube and some field-effect transistors (FET) are normally *on* devices while a transistor is normally *off.* That is, with zero bias, plate or drain current flows. However, a transistor turns *off* with zero bias applied.

transistor is an *off* device

	FORWARD-BIASED JUNCTION			V_{CE} (SAT)
	ACTIVE	CUT-IN/CUT-OFF	SAT	
Si	0.6	0.5	0.6	0.2
Ge	0.2	0.1	0.2	0.1

Fig. 3-48. Semiconductor operating voltages.

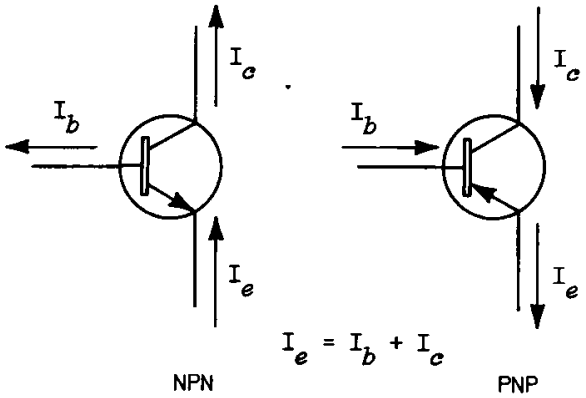


Fig. 3-49. Transistor current (electron) flow.

Consider the transistor as a device in one of three states: on, off, or saturated. Fig. 3-48 lists the active bias conditions assumed in this book for either silicon or germanium transistors. These are not absolute values but satisfy circuit analysis approximations.

forward bias

Applying forward bias to a transistor, 0.6 V for silicon (Si) or 0.2 V for germanium (Ge), causes emitter current flow. Fig. 3-49 indicates current distribution. Emitter current (Is) flows into the NPN transistor and divides, forming base current (I_b) and collector current (I_c), which flow in the external circuits. I_b and I_c flow into the PNP transistor and combine to form I_e. In either type transistor a percentage of I_e flows in the base circuit, establishing the input impedance of an emitter follower: I_b increases with I_e.

alpha beta

The percentage of I_e flowing in the base and collector circuits sets two transistor parameters, alpha (α) and beta (β). $\alpha \approx I_c/I_e$ and $\beta \approx I_c/I_b$ Since

terms are common, $\alpha = \beta/1+\beta$ and $\beta = \alpha/1-\alpha$. One sometimes sees α represented by *h* parameter, h_{fb}, and β by h_{fe}. This book will not use *h* parameters.

β indicates relative input Z

α and β tell a great deal about a transistor. A low β indicates a relatively large quantity of base current flow. Stated differently, a low β indicates a relatively low input impedance. Since I_b is a percentage of I_e then the I_b quantity depends upon I_e quantity. This implies emitter impedance affects base input impedance. It does. $R_{in} = \beta R_E$ where R_E is total emitter impedance. Conversely, external circuits which impede I_b reflect into the emitter

circuit $1/\beta$ times: 100-ohm base circuit load appears in the emitter as $100/\beta$ ohms.

a fairly constant

α remains a fairly constant parameter while a may change significantly. A large dynamic emitter current can cause α to change a few percent, but if α changes slightly β varies drastically: Assume 10-mA emitter-current change causes α to drop from 0.98 to 0.96. The difference between 9.8-mA and 9.6-mA I_c might go unnoticed. However, β changed from 49 to 28!

Initially:

$$\beta = \frac{\alpha}{1 - \alpha}$$

$$\beta = \frac{0.98}{1 - 0.98} = \frac{0.98}{0.02}$$

$$\beta = 49$$

Changed to:

$$\beta = \frac{\alpha}{1 - \alpha}$$

$$\beta = \frac{0.96}{1 - 0.96} = \frac{0.96}{0.04}$$

$$\beta = 28$$

β is only one factor determining output impedance (R_0) of an emitter follower. Additional terms used are:

R_b, base spreading resistance;
R_r, reflected base resistance;
r_e, dynamic emitter resistance;

R_t, transresistance resistance; and
R_E, external emitter resistance.

base spreading resistance

Base spreading resistance (R_b) exists in the transistor as a result of the manufacturing process. This resistance is a physical component which opposes the flow of base current. It takes a value between 1 Ω and 1 kΩ depending upon transistor type. Assuming 250 Ω gives a fair low-frequency approximation. I_b flows through R_b as a series component.

I_b represents only a portion of I_e, therefore only a portion of R_b opposes emitter current. The value of reflected resistance (R_r) is the quotient of R_b

reflected resistance

and β: $R_r = \frac{R_b}{\beta}$. If β were 50 and R_b were 250 Ω,

$$R_r = \frac{R_b}{\beta} = \frac{250}{50} = 5.$$

estimated R_r

One seldom knows the value of R_b. For purposes of circuit analysis, assume between zero Ω and 10 Ω as the value of R_b/β

Fig. 3-50 shows base spreading resistance as viewed from the base level. Viewed from the emitter this resistance appears as R_r as shown in Fig. 3-51.

dynamic emitter resistance

Dynamic emitter resistance (r_e) also appears as the remaining series portion of transresistance resistance (R_t).

Dynamic emitter resistance is *gm*-determined, as internal cathode impedance. However, a formula one should commit to memory makes r_e approximations simple: r_e - $\frac{26 \times 10\text{-}3}{I_e}$, where I_e is emitter current.

This formula, which applies to all transistors used as linear amplifiers, is derived from the general equation for current through a PN diode junction:

$$I = I_s \left(e^{\frac{V}{kT/q}} - 1 \right).$$

Where:

I = Quiescent or net diode current
I_s = Saturation current
e = Natural log base
V = Applied forward voltage

k = Bolzmann's constant = 1.38 x 10^{-16} erg/K
T = Absolute temperature, K
q = Electron charge = 1.602 x 10-19 coulomb

If V exceeds *k*T/q by 5, the equation simplifies to:

$$I \approx I_s \, {}_e^{V} \, \frac{}{kT/q}$$

(*k*T/q at room temperature is 26 mV).

Substituting the simplified formula into the forward-conductance formula yields r_e. Differentiating the original current equation for small increments of dynamic conductance results in conductance *gm.*

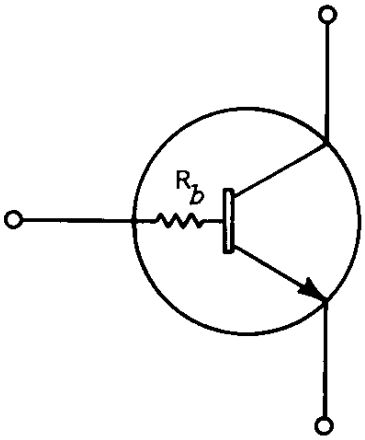


Fig. 3-50. Base spreading resistance.

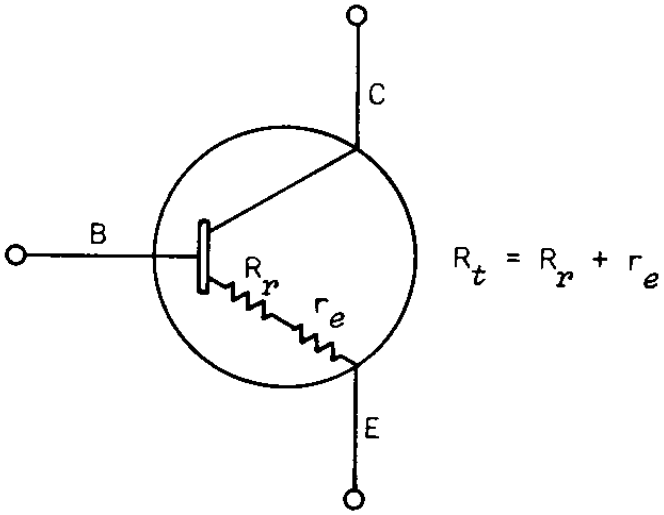


Fig. 3-51. Transresistance (R_t)

$$\frac{\Delta I}{\Delta V} \approx \frac{dI}{dV} = \frac{I_s \frac{V}{kT/q}}{e^{kT/q}} = gm = \frac{1}{r_e}$$

Now substituting:

$$gm = \frac{I}{kT/q}$$

$$r_e = \frac{kT/q}{I}$$

Since kT/q at room temperature is 26 mV.

$$r_e \approx \frac{26 \times 10^{-3}}{I_e}$$

All of which shows that R_t is predictable and small, developing for emitter followers high gain and low output impedance. To demonstrate this, assume $\beta = 50$, $R_b = 250\ \Omega$, and $I_e = 1$ mA.

$$R_t = R_r + r_e = \frac{R_b}{\beta} + \frac{26 \times 10^{-3}}{I_e}$$

$$R_t = \frac{250}{50} + \frac{26}{1} = 5 + 26 \approx 30\ \Omega.$$

R_t appears in series with external emitter resistance (R_E) for signal development, and in parallel with R_E to present output impedance. Fig. 3-52 shows the emitter-follower basic circuit, equivalent circuit, and formulas. Gain times the base signal develops across RE. Gain depends upon the resistance of R_E and R_t. When R_E exceeds R_t by 10 or more, gain approaches unity and R_t expresses output impedance. Further, R_t decreases with an increase in emitter current, indicating an advantage to longtailing.

longtailed emitter follower

Fig. 3-53 shows an NPN silicon transistor connected as a longtailed emitter follower. The collector returns to positive 10 volts and the base to ground. The emitter circuit contains turn-on voltage for the device. 39.4 volts across R_E demands approximately 4-mA emitter current. This is all the information needed for analysis:

$$A_V = \frac{V_{in}}{V_o} = \frac{R_E}{R_E + R_t}$$

$$R_o = \frac{R_E\ R_t}{R_E + R_t}$$

$$R_t = R_r + r_e$$

$$r_e = \frac{26 \times 10^{-3}}{4 \times 10^{-3}} = 6.5\ \Omega$$

Arbitrarily add 3.5 Ω for R_r, to round R_t to 10 Ω. In this case A_V = 1 and Ro = R_t = 10 Q. I_e is high enough and R_E large enough for unity gain and low output impedance. Assuming R_r, low is justified since the base driving circuits are unknown.

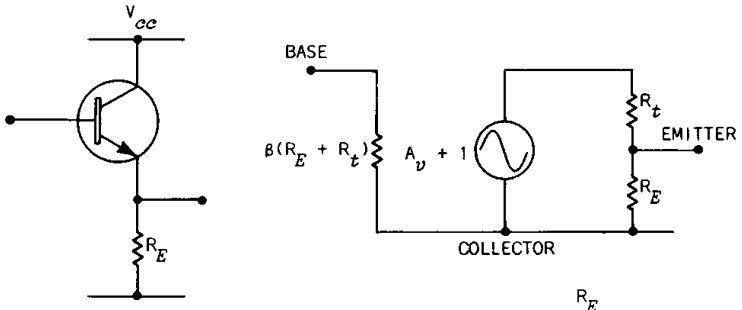


Fig. 3-52. Common collector.

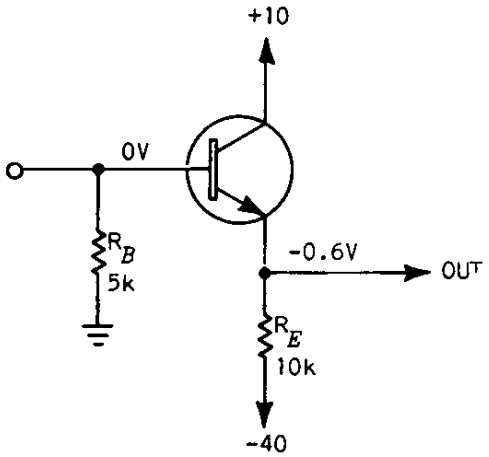


Fig. 3-53. Longtailed EF.

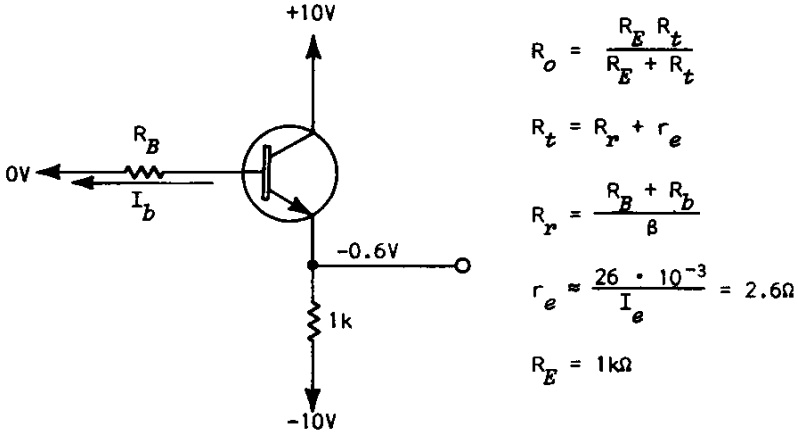


Fig. 3-54. Input components appear in the emitter output.

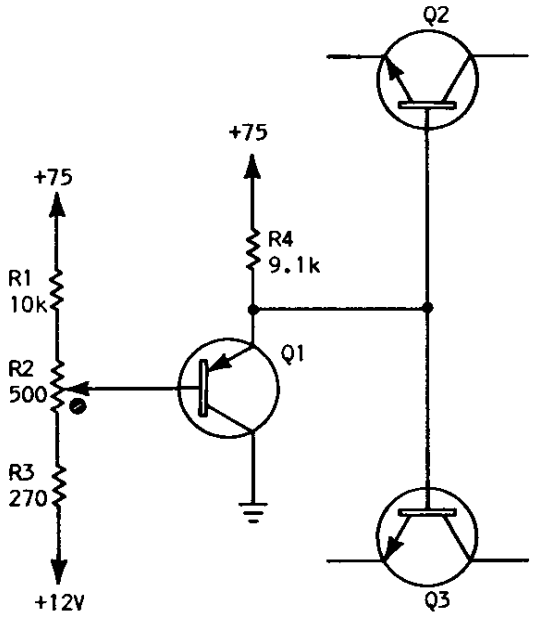


Fig. 3-55. Emitter follower providing low-impedance base supply.

input source impedance affects output impedance

Source impedance of base driving circuits can be important since this opposition to base current appears in series with R_b. Therefore, source impedance added to R_b and divided(by β constitutes R_r at the emitter. Should this raise R_t appreciably, both gain and output impedance are affected.

Fig. 3-54 shows an emitter follower with equivalent source impedance included in the base lead. About 9-mA I_e flows, resulting in less than 3 Ω r_e. R_t

now depends upon β and R_B. R_o and possibly gain will be a result of these factors. Assign S a value of 50. If R_B were 100 Ω, then R_r would increase by 2 Ω. This is hardly enough to worry about. One could safely assume an R_t between 5 and 10 Ω. However, were R_B 1 kΩ, R_t then appears as about 25 Ω. Gain is about 0.98 and Ro has increased appreciably.

determining emitter-follower action

To show how one determines emitter-follower action in an operating circuit, consider Fig. 3-55. Emitter follower Q1 functions as low-impedance voltage source, providing base voltage for grounded-base amplifiers Q2 and Q3. This circuit also provides thermal compensation.

impedance transformer

Q2 and Q3 as grounded-base amplifiers require a low-impedance base supply voltage. In this case the also require an adjustable return. Q1 reduces the value of voltage divider R1, R2 and R3 by β, keeping the initial R_B of Q2 and Q3 low and preventing large R_B variations during adjustment of base voltage.

temperature compensation

Temperature compensation results from all transistors being silicon and mounted near one another. Since the transistors share thermal environment, they experience equal base-emitter voltage changes. However, Q1 is a PNP transistor. Should I_e increase due to temperature, Q1 emitter voltage drops, decreasing the forward bias on Q2 and Q3 which counteracts temperature-induced current demand in Q1 and Q3.

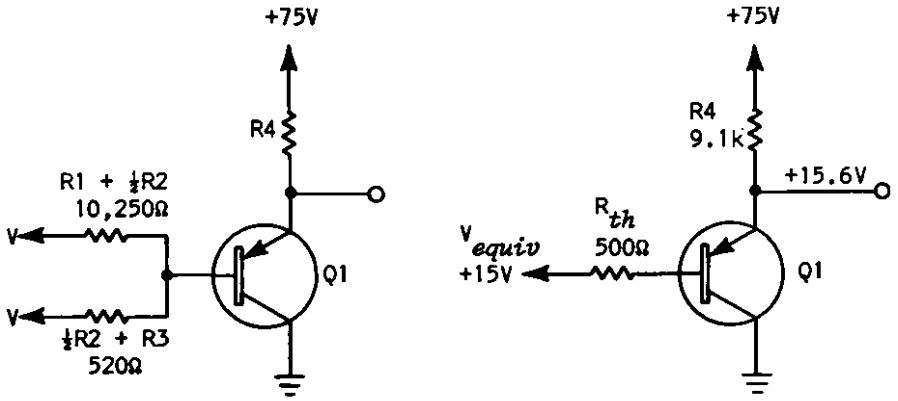
Q1 base circuit

One analyzes the circuit of Fig. 3-55 by first "Thevenizing" the base circuit of Ql. This gives an equivalent resistance returned to an equivalent voltage. The equivalent voltage is base voltage which, raised one diode junction (0.6 V for silicon), is Q1 emitter voltage. Q2 and Q3 base voltage is Q1 emitter voltage. And dropping this voltage one junction resolves Q2-Q3 emitter voltage. In other words, Q1 base voltage and Q2 or Q3 emitter voltage are equal.

Assuming R2 set to midrange, one breaks voltage divider R1, R2 and R3 as shown in Fig. 3-56: The base connects to the junction of a 10.25 kΩ and a 520 Ω resistor. Voltage at the resistive junction and the shunt value of the resistances give the Thevenin equivalent circuit. R_{th} is 500 Ω returned to +15 equivalent volts. Add 0.6 V to assign emitter voltage.

Now that the drop across R4 is known, solve for I_e and re. R_r consists of R_B and R_b divided by β. In this case R_{th} is R_B. Use a conservative β, say 50, and R_r is 16. The value R_b /ß is arbitrary. Any value between 1 Ω and 10 Ω may be used. 6 is chosen merely to give an even power of ten to the sum: $R_r + r_e$.

R_o is R_t. One might think the shunting of R4 should be considered. Don't waste the time! R4, 470 times larger than R_t, changes output resistance less than the R_r approximation error.



$$I_e = \frac{59.4V}{9.1 \cdot 10^3} = 6.65mA$$

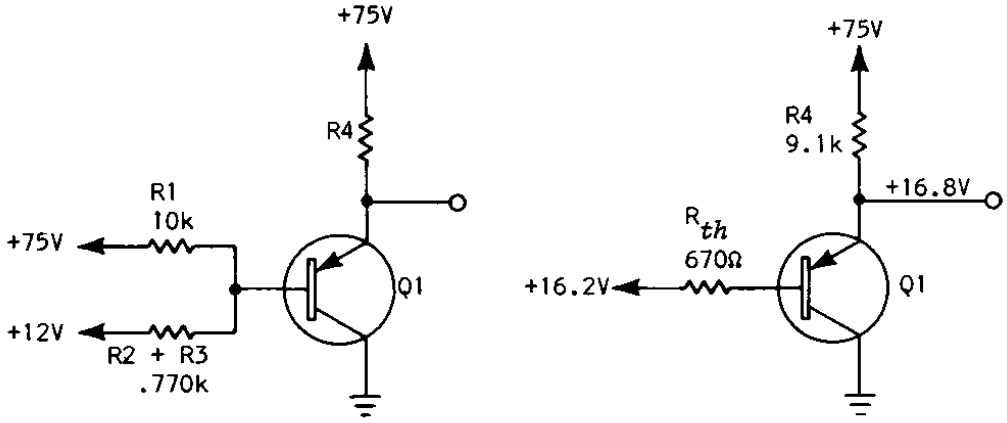
$$r_e = \frac{26 \cdot 10^{-3}}{6.65 \cdot 10^{-3}} \approx 4\Omega$$

$$\frac{R_{th}}{\beta} \approx 10\Omega$$

$$\frac{R_b}{\beta} \approx 6\Omega$$

$$R_t = 4 + 6 + 10 = 20\Omega = R_o$$

Fig. 3-56. Circuit equivalent with R2 centered.



$$I_e = \frac{59.2}{9.1 \cdot 10^3} = 6.65\text{mA}$$

$$r_e = \frac{26 \cdot 10^{-3}}{6.65 \cdot 10^{-3}} \approx 4\Omega$$

$$\frac{R_{th}}{\beta} = 13.4\Omega$$

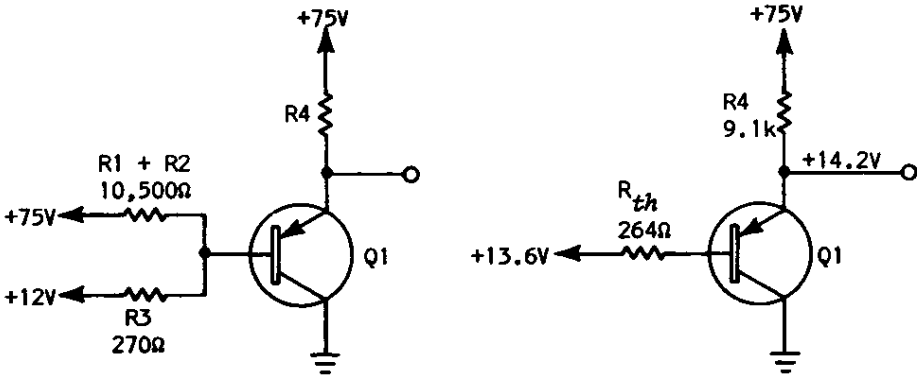
$$\frac{R_b}{\beta} = 6\Omega$$

$$R_t = 6\Omega + 13.4\Omega + 4\Omega = 23.4\Omega = R_o$$

Fig. 3-57. Circuit equivalent with R2 set to maximum.

maximum positive

For consistency, hold reflected base spreading resistance at 6 Ω for all settings of R2, and β at 50. Fig. 3-57 represents the equivalent circuit for maximum positive V_{BB}• R_{th} and the equivalent voltage to which it returns are larger values. Longtailing holds I_e and, therefore, r_e fairly constant. R_{th} (R_B) reflects a few additional ohms into the emitter, representing the increase in R_0 over the midsetting of R2.



$$I_e = \frac{60.8}{9.1 \cdot 10^3} = 6.7\text{mA}$$

$$r_e = \frac{26 \cdot 10^{-3}}{6.7 \cdot 10^{-3}} \approx 4\Omega$$

$$\frac{R_{th}}{\beta} = 5.3\Omega$$

$$\frac{R_b}{\beta} = 6\Omega$$

$$R_t = 6\Omega + 5.3\Omega + 4\Omega = 15.3\Omega = R_o$$

minimum
positive

Fig. 3-58. Circuit equivalent with R2 set to minimum.

Continuing the reasoning, Fig. 3-58 shows the circuit with R2 set to minimum. Here again, because of longtailing, R_B determines the change in R_0.

R_0 also represents R_B for Q2 and Q3. Keeping R_B small is a basic requirement for grounded-base amplifiers. Fig. 3-59 includes a formula which indicates R_B should be large. This is true if one ignores wanted signal degeneration. Temperature increases cause a decrease in emitter-to-base voltage -- an increase in forward bias. I_e, thus I_b, increases until the drop across R_B raises V_{EB} to the nominal bias level. Unfortunately, wanted signals suffer the same degeneration as thermal noise. This is the reason for the PNP-to-NPN configuration shown in Fig. 3-60.
Temperature increases cause V_{EB} of Q2 and Q3 to decrease, perhaps 2.5 mV/°C, which increases emitter-current demand. A signal is born! But, Q1 V_{EB} also decreases and the increased emitter current through R4 develops a more negative base voltage for Q2 and

Q3. Q2 and Q3 emitter currents return to quiescence. Desirable signals are not coupled into the feedback loop, therefore suffer no degeneration.

signal amplifier

Emitter followers also perform as impedance transformers in signal paths. This occurs in oscilloscope preamplifiers where the input amplifier is a cathode follower. Cathode followers have the required high input impedance and a relatively low

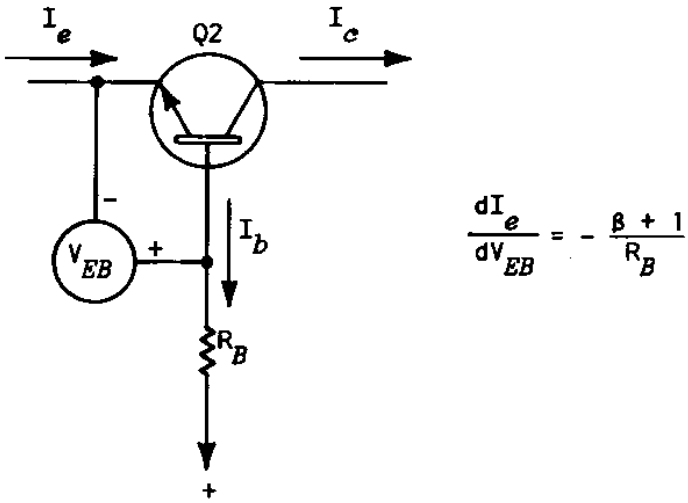


Fig. 3-59. A large R_B minimizes I_e changes, due to V_{BEB} variations.

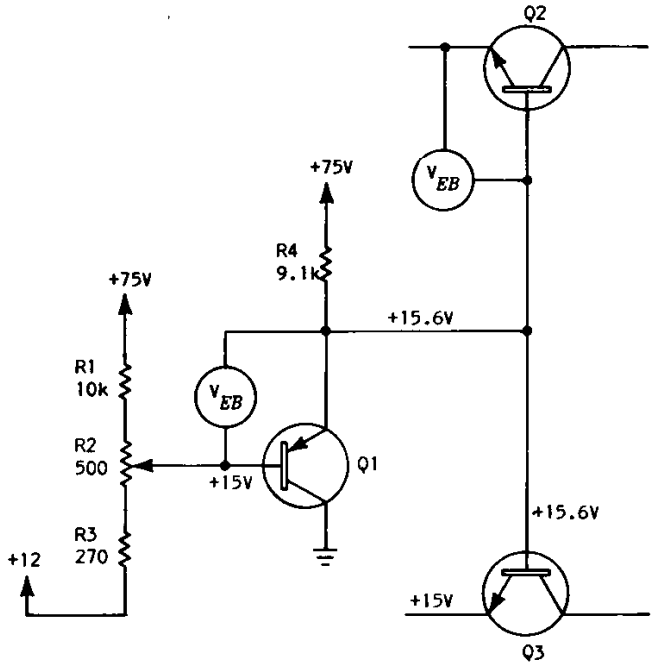


Fig. 3-60. Providing the thermal compensating effects with an emitter follower.

vacuum tube *gm* decreases with age

output impedance. Unfortunately a vacuum tube changes parameters during aging. Transconductance decreases at an unpredictable rate, increasing cathode follower output impedance. The increase in r_k could negligibly decrease CF gain and yet seriously decrease overall gain of a following transistor amplifier.

changing r_k changes R_t

In Fig. 3-61A the common-emitter amplifier receives V_{in} via the CF. V_0/V_{in} defines stage gain. With certain values a selected collector load resistance gives the gain desired. CF longtailed,

gm = 5000 μmho, β = 50, and $R_b/\beta + r_e = 6\ \Omega$

frequency gain remains at the desired level only so long as *gm* (r_k) remains constant. This is because r_k reflects into the emitter circuit, imposing degeneration as an unbypassed emitter resistor.

Refer to Fig. 3-61B. The CF voltage source applies base voltages through its internal impedance. R_B (1/*gm*) reflects into the emitter as a portion of R_t. R_t in this case constitutes total emitter degeneration of 10 Ω. During the operating life of the tube transconductance decreases. The longtailed CF appears a fairly constant voltage source whose internal impedance increases with age. After many operating hours, perhaps 1000 to 2000, r_k increases 5 or so times. The circuit then changes to that shown in Fig. 3-61C. R_t increases 2-1/2 times, reducing gain accordingly.

Using emitter-follower coupling (Fig. 3-62) affects a multiplication: Cathode follower r_k changes 500%, R_0 of the emitter follower changes 300%, however, R_t of the common-emitter amplifier changes but 1 Ω. And R_t values before and after aging are less than without the EF.

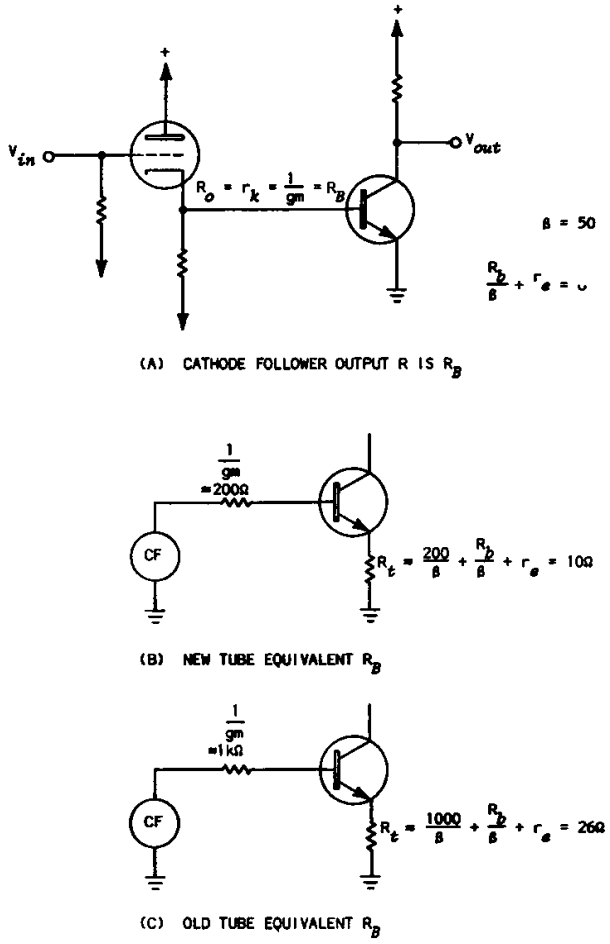


Fig. 3-61. Tube parameters increase R_B after many operating hours.

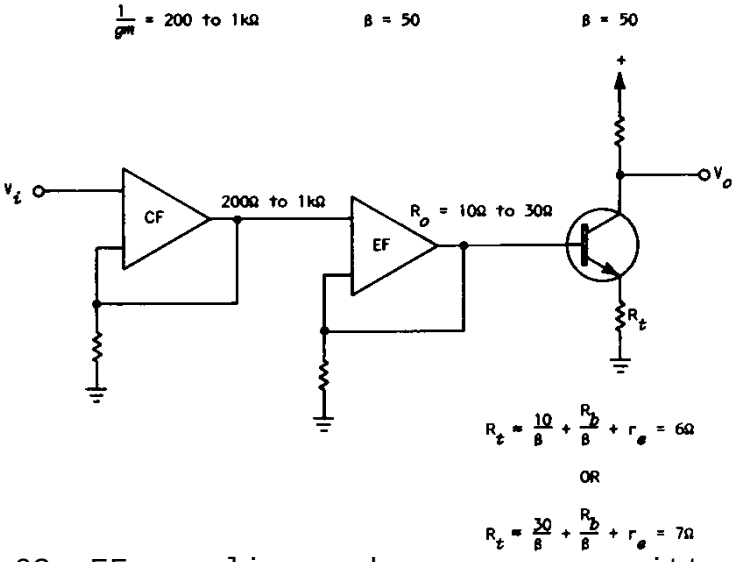


Fig. 3-62. EF coupling reduces common-emitter input impedance.

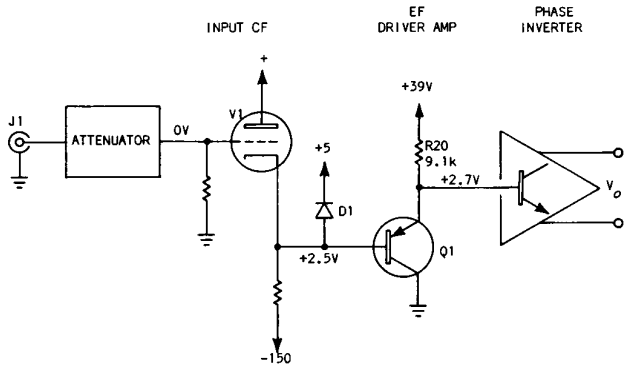


Fig. 3-63. An emitter follower used to reduce impedance and as a negative clamp.

Fig. 3-63 depicts an emitter follower used as described. Q1 also functions as a negative clamp.

V1, a longtailed cathode follower, applies input signals slightly attenuated to the base of Q1. Longtailed emitter follower Q1 functions as a very low-impedance signal source driving the phase inverter.

V1 self-bias, 2.5 volts, appears at the anode of D1 and base of Q1. Both are germanium. D1 clamps to prevent excessive positive excursions and Q1 clamps during excessive negative excursions. Cathode excursions which exceed +5 V turn D1 on. D1 then clamps the output at +5.2 volts to prevent reverse breakdown of Q1.

Reverse breakdown is not necessarily harmful. Drawing small current just puts the device in another mode of operation. However, most vertical circuits like the input cathode follower draw large current quantities. This increases the power dissipated by the junction beyond tolerable limits. Thus the clamp, which prevents reverse-breakdown.

Q1 conducts, collector-to-base, as a diode when base voltage drops 0.2 volts below ground. This most often happens during tube substitution. Removing V1 causes -150 volts to appear at the base of Q1. Ql base-collector diode turns on, dropping

Q1 clamping

the voltage across the CF longtail resistance. The Q1 clamp protects the phase inverter, an NPN,from reverse breakdown.

Interchassis connections create capacitance. Emitter followers are therefore frequently used as preamplifier output amplifiers. The push-pull amplifier of Fig. 3-64 drives the main vertical amplifier as a low-impedance source. Emitter current through R1 and R2 longtail Q1 and Q2.

balance

R3 and C1 carry the name High-Frequency Balance. Without R3 and C1, Q1 and Q2 operate as independent amplifiers. This is fine if both the input and output signals are truly push-pull. An unequal reactive load on either base or emitter lead, or for that matter in any stage from the phase-inverter to the CRT, causes an unequal phase shift. Cross coupling R3 and C1 balances the phase shift. One adjusts R3-C1 for minimum necessary phase shift --for best CRT step-function display.

negative input resistance character-istics

Emitter followers experience "negative-input-resistance characteristics." The conceptual effects of capacitances, impedances and transconductance are as explained for cathode followers. The same compensation concepts apply: suppressor resistor, shunt RC, and "Miller-effect" -- degenerative feedback from collector to base in a transistor.

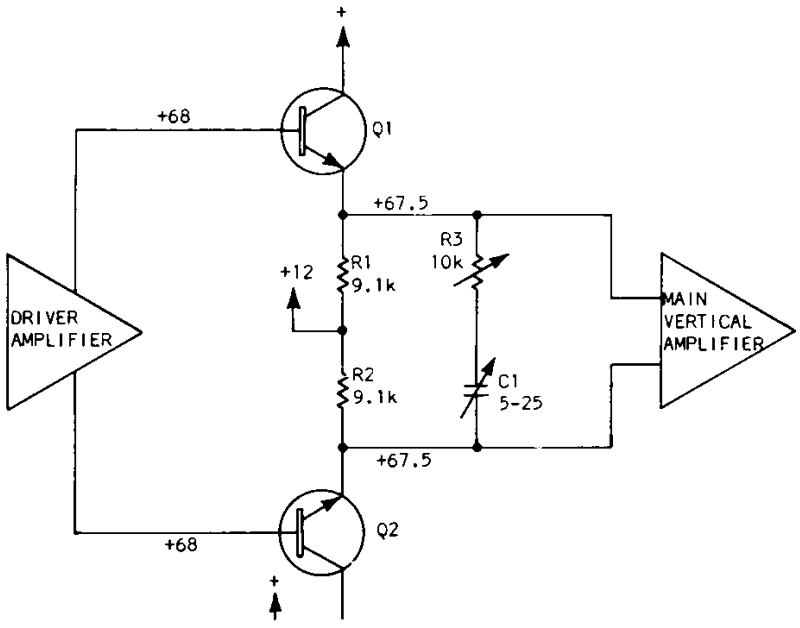


Fig. 3-64. Push-pull emitter followers.

step response

Longtailed emitter followers follow positive and negative steps at different rates. Cathode followers react more faithfully to positive voltage transitions than negative transitions. And this becomes more pronounced with longtailing. Emitter followers have similar reactions except the direction of current flow, thus reaction to positive and negative steps, depends upon transistor type.

NPN emitter followers, like cathode followers, follow positive step functions more faithfully than negative. PNP emitter followers react in opposite manner, reproducing negative step functions more faithfully than the positive step.

Capacitance charge time generally restricts the step response of any amplifier. Fig. 3-65 includes a simplified NPN emitter follower. The input signal consists of a positive step function followed sometime later by a negative step function. Refer to the positive transition as risetime (t_r) and the negative transition as falltime (t_f). Output t_r appears equal to the input. Output t_f, however, considerably exceeds input t_f. The output waveform effectively graphs C_0 charge rate. This is determined by components C_0, R_E and R_t.

C_0 represents total output capacitance which includes EF open-circuit output C, lead C, connector C and following-stage input C. R_E is the total external emitter-load resistance. R_t remains the active device transresistance.

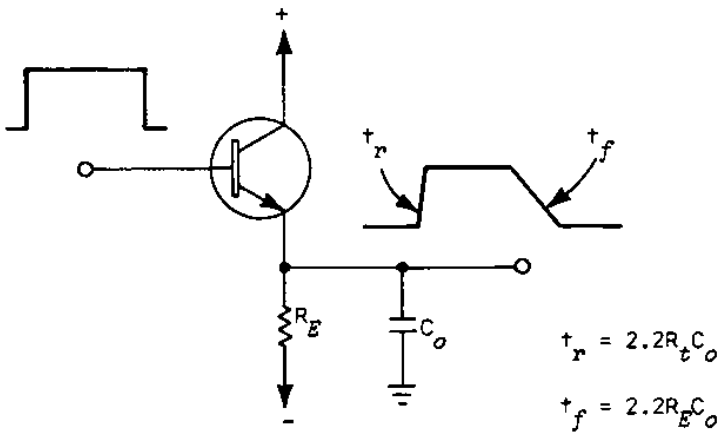


Fig. 3-65. NPN emitter followers react faster to rising steps than to falling steps.

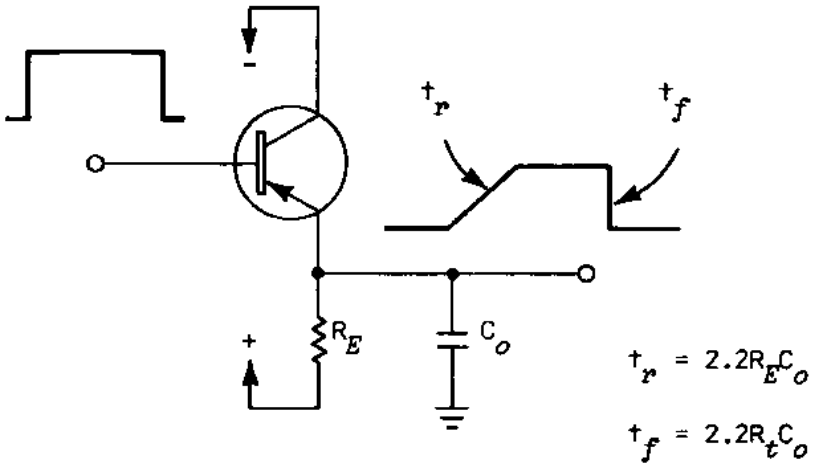


Fig. 3-66. PNP emitter followers react faster to falling steps than rising.

t_r = 2.2 RC defines response. C in the formula is C_0 for positive or negative step response. R changes: For positive steps put the value of R_t in the formula while R_E is the value for negative step response.

C_0 is not large, probably between 8 and 20 pF. During t_r charging current flows as emitter current. Only R_t limits charging current quantity. NPN emitter followers then increase risetime very little.

Current flows *into* the emitter of NPN transistors. Emitter current cannot contribute to the charge of C_0 during t_f. C_0 charges by drawing current from the negative supply through R_E. R_E, always a much larger resistance than R_t, accounts for the difference between t_r and t_f.

Longtailing establishes t_f. The total current available sets the charge rate of C_0. During t_f (NPN) the maximum current is that provided by the longtail. Circuit falltime will probably be linear (ramp-like) but longer than risetime.

C_0 charging rate also determines PNP step response (Fig. 3-66). However, emitter current flows out of the PNP causing opposite polarity response compared to NPN devices.

Positive step functions reduce emitter current forcing C_0 to charge toward the positive supply through R_E. This of course increases t_r.

t_f input and output appear equal. Emitter current charges C_0 negative, again only R_t opposes C_0 charge current.

push-pull

This unequal response is one reason that a vertical signal is converted to push-pull one or two stages after the input amplifier. If one views the single-ended output from an impedance standpoint, the difference in transit time indicates output impedance changes with step polarity. Push-pull amplifiers tend to maintain output impedance constant between terminals. However, push-pull circuits can create design problems for the inclusion of controls, particularly those that should return to the chassis.

An example of this is the switched-gain amplifier mechanically coupled to the input attenuator. Fig. 3-67 is the input amplifier driving the switched-gain amplifier. Q1B operates with zero emitter volts at quiescence, or center-screen. Therefore each attenuator position can return to chassis ground and switching causes no vertical CRT displacement. V1 and Q1A function as a longtailed input follower which sets and maintains Q1B emitter voltage at zero volts quiescent operation.

Analyze the voltage setting and temperature compensating of Q1A by first examining other input components.

R1A and R1B return V1 grid to ground and form a constant portion of the input attenuator.

R1A, R3, C3A and C3B oppose the negative input characteristics of CF Vl. R1A restricts the quantity of current drawn by the negative resistance of Vl. C3A and B form with R3 shunt compensation causing flat input capacitance to all frequencies and pulses. C3 results from circuit-board construction. R2 connects to conductor strips each of which is one capacitor plate. Circuit-board base material is the dielectric. Dielectric variations with frequency add to the input capacitance change. Including a connector near both

ends of R2 creates the second capacitor plate. Returning C3A and B to ground through R3 stabilizes the capacitance, and selecting resistance correctly, the network performs as shunt RC compensation for negative-resistance characteristics.

C2 bypasses grid-limiting resistor R2 to rapidly charge or discharge Vi input capacitance.

R4-C4 in the plate of V1 develop Miller-effect even though gain is low:

t_r (2.2 RC) is 66 microseconds or
$F_{C,}$ 1/(2 π Rc), is 5.3 kHz.

protective devices

Bl, D1 and D2 are protective devices: B1 protects V1 against input voltage overloads. Should grid-to-cathode voltage exceed ignition for neon tube B1, it fires. B1 regulates grid voltage until removal of the excessive input voltage. Assume B1 protects against grid-to-cathode arc due to negative voltage -- reasonable grid current through R2 limits positive grid voltage.

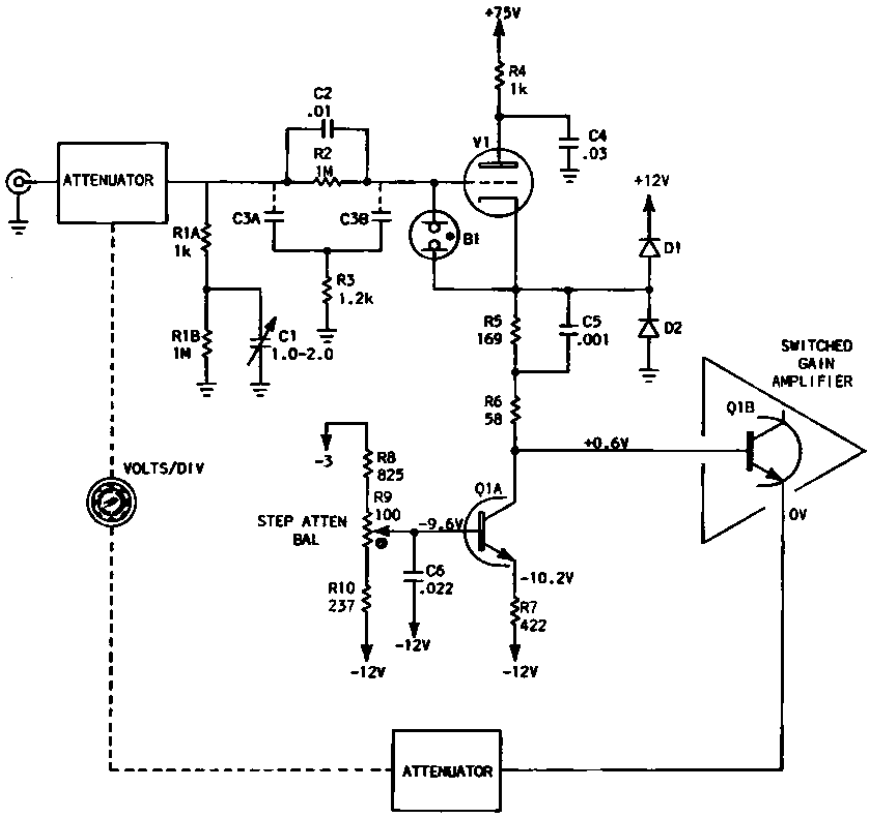


Fig. 3-67. Cathode follower with longtail providing temperature compensation to the following stage.

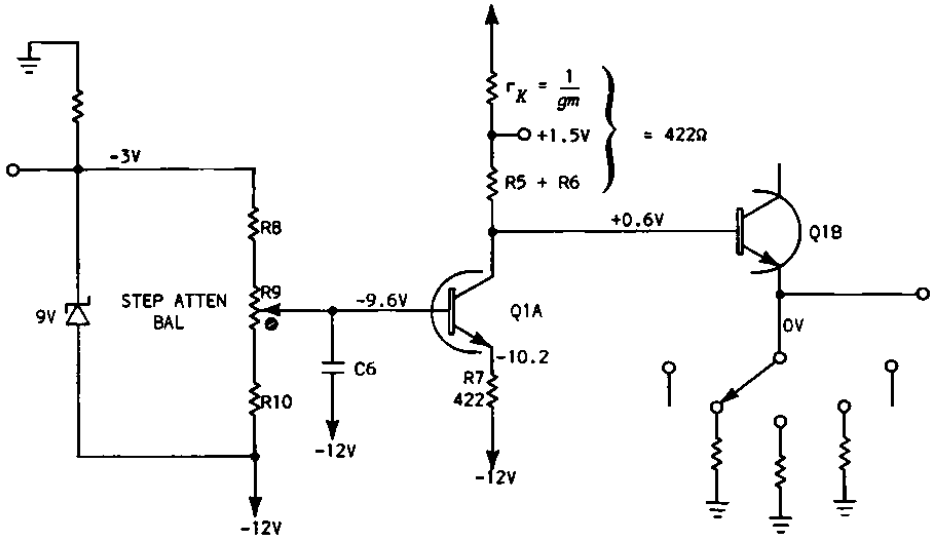


Fig. 3-68. Longtail temperature compensation.

D1 protects Q1A. Should cathode voltage exceed +12 volts D1 clamps. This prevents base-to-collector breakdown of Q1A.

D2 functions during warmup of V1. VI cathode must heat before V1 consumption equals the current delivered by Q1A. Q1A thus charges C5 toward the -12 volt supply. This causes the grid to appear more and more positive, demanding current from a cold cathode. D2 prevents this by turning on and clamping one diode junction below ground, holding positive bias at about 0.6 volts.

speedup capacitor

C5 bypasses R5 to "speedup" the development of fast-rise signals at the base of Q1B.

V1 self-bias, VI *gm,* R5, R6 and the conduction of Q1A set the base, thus emitter, operating level of Q1B. Further, due to the high impedance at the collector of Q1A compared to R5 and R6, almost the entire cathode voltage develops across Q1A. These truths permit the circuit simplification of Fig. 3-68. This figure includes partial Q1B emitter circuitry. The emitter connects to a switch which may be positioned to any one of several resistors.

Each resistor returns to ground and the emitter sets at zero volts. This is the desired quiescent condition: An operator actuating the switch causes no vertical deflection. A voltage at the emitter appears as a signal whose amplitude depends upon the emitter resistance selected. Following vertical circuits amplify this signal to deflect the CRT. Grounding the preamplifier input jack and vertically centering the CRT trace should develop zero volts at the emitter of Q1B.

Q1A collector current, through R5 and R6, sets Q1B operating point. The voltage at the top of R5-R6 results from the self-bias of V1. Q1A collector current drops a voltage across R5-R6 setting Q1B base voltage. One adjusts R9 in the base circuit of Q1A for proper base voltage. Since self-bias varies between tubes and with tube aging, this is an empirical adjustment. To check this adjustment switch through the range of the VOLTS/DIV selector. No vertical deflection should occur with the vertical input grounded and the CRT trace vertically centered.

Small power-supply variations do not change Q1A base voltage. This is because Q1A base and emitter components return to the same power supply and the drop across R8, R9 and R10 is regulated. Should the -12 volt supply change, the change occurs at the bottom of R7 and R10, and at the top of R8 due to the zener diode. Equal-voltage changes at both ends of the voltage divider demand an equal change at the base. Forward bias remains constant, thus collector current, thus the drop across R5-R6.

Capacitor C6 returns to -12 volts to prevent power supply fluctuations from appearing as signals at base of Q1A. Any -12 volt change also develops at the wiper of R9. C6, therefore, need not charge to a new level. If C6 returned to ground any voltage change at the wiper of R9 would depend upon C6 charging to the new level. This would develop a signal at Q1A collector, deflecting the CRT accordingly.

temperature compensation

The longtail-configuration temperature compensates Q1B. Q1A and Q1B share temperature environment -- the same case. Equal temperature-induced bias changes occur in Q1A and B. Q1A amplifies the temperature signal by -1, returning Q1B to the correct operating point.

Temperature compensation is necessary to maintain a stable display. A temperature-induced voltage, with Q1B uncompensated, develops at the emitter of Q1B causing a slow CRT display drift, up or down. In this case, an upward drift indicates a temperature increase and downward drift, a decrease.

In-phase equal-amplitude thermal signals appear at the base-emitter of Q1A and B. An out-of-phase thermal signal develops at the collector of Q1A. For this signal to cancel the thermally induced signal, Q1A must amplify by 1. This is the reason for equal Q1A collector and emitter loads.

Assume temperature increases to develop one-mV forward-bias increase. Center-screen voltage at Q1B emitter ascends from 0 to +1 mV. The same change develops at Q1A. To increase Q1A emitter voltage 1 mV, emitter current through R7 must increase

2.4 µA (I = E/R). If ß = 50, 2.35-µA collector

current flows. Collector current through R5, R6 and r_K drops an additional 1 mV; making Q1B base 1 mV more negative; which returns Q1B emitter to 0 V. One need not consider ß to determine collector current. Part tolerances impose sufficient error that one can consider emitter current and collector current equal.

R7 sets total emitter current, therefore determines the collector resistance needed for desired voltage gain. 2.4 µA through R7 develops 1 mV. The collector-voltage drop resulting from this current depends upon collector resistance. 422-ohms collector load gives the desired unity gain. R5,

R6 and r_K sum to 422 ohms. Include r_K ($1/gm$) since

total collector current flows as CF plate current. Don't consider the cathode as signal ground. A portion of the collector signal appears at the cathode whose amplitude is represented by r_K returned to virtual ground.

Single-ended control circuits, represented by the partial circuitry of Q1B, have been proven in thousands of Tektronix scopes. Q1A compensates for the major disadvantage, thermal drift. Keep this in mind while considering a seemingly unrelated development -- the **FET**.

field-effect transistors

Semiconductor manufacturers in the recent past developed field-effect transistors (FET) suitable for use in Tektronix instruments. Generally one considers these devices as direct substitutes for triodes. Numerous economies result: Initial cost, reliability, size, weight and heat. Heat savings here refer to elimination of tube filaments. FET displacement of tubes is very attractive for new design.

The FET source follower replaces the CF as an input amplifier. However, FET thermal reactions come into play. Current through the FET decreases as temperature increases. This is opposite to transistor temperature reaction.

A model of a source-follower input amplifier appears in Fig. 3-69. Q1 is the source follower longtailed by Q2. Q1 and Q2 are encapsulated in the same case so that Q2 temperature compensates the circuit. Setting R4 establishes total current initially through R2, Q2, R1 and Ql. Q1 self-bias develops the voltage at the top of Rl.

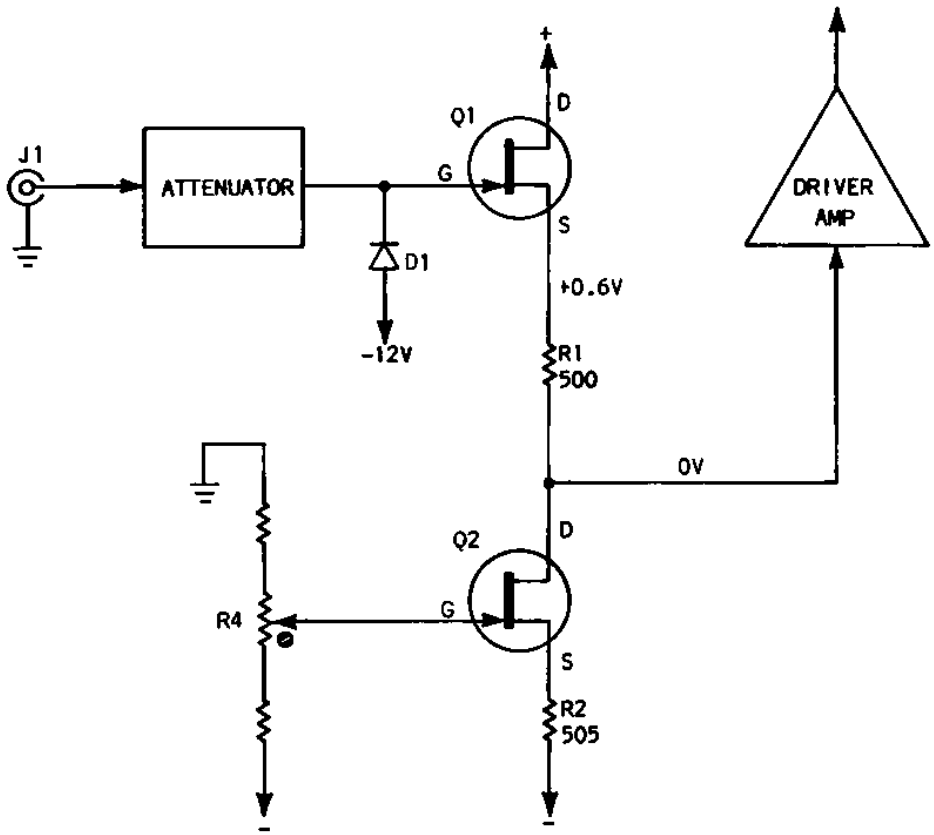


Fig. 3-69. Source-follower input amplifier.

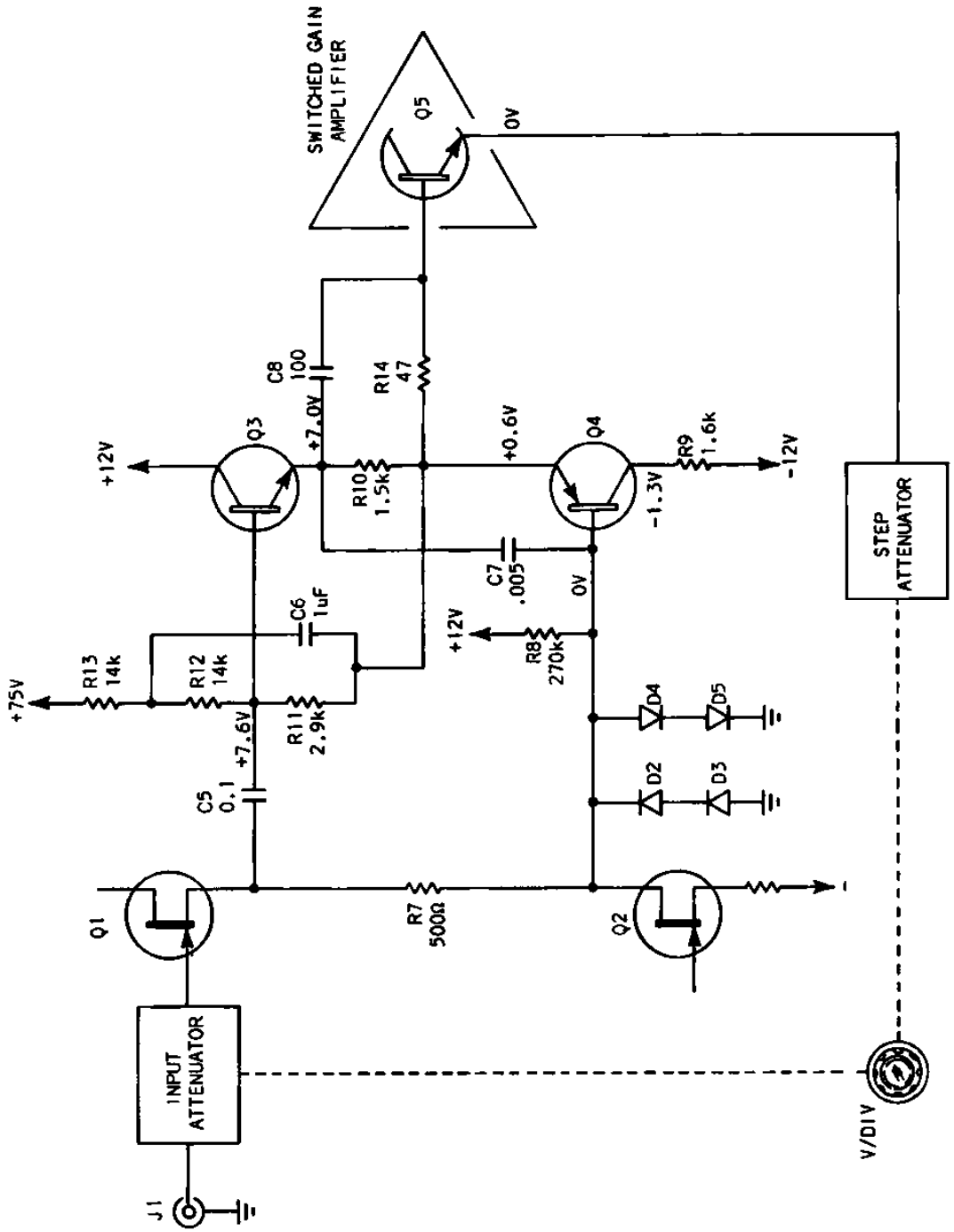


Fig. 3-70. Switched-gain driver amplifier.

Longtail current through R1 sets the output level, shown as zero volts. During temperature increases Q1 conduction decreases, decreasing self-bias. When the voltage at the top of R1 moves negative so should the output voltage. But, Q2 decreases conductivity with Q1, current through R1 decreases maintaining zero volts output.

Preventing output-voltage changes with temperature is good. It does not, however, allow direct connection of the single-ended transistor control amplifier, as the preceding example, since there is no temperature compensation of the control amplifier. Coupling the source follower to the advantageous single-ended control amplifier poses a problem. Fig. 3-70 illustrates one solution.

Emitter followers, Q3 and Q4, couple voltages to, and temperature compensate, the input transistor (Q5) of the switched-gain amplifier. Q3 and Q4 appear to have a complementary connection. They don't function as the classic complementary emitter follower and, therefore, will not carry the name.

Q4 performs several functions: Sets Q5 operating level, temperature compensates Q5, couples signals from DC to several Hz, and provides Q3 emitter current.

Q3 is a broadband emitter follower whose bandwidth exceeds 100 MHz.

Q2 sets the base voltage of Q4. Q4 elevates this voltage one silicon junction to establish the operating point for Q5. Fig. 3-70 shows center-screen nominal-temperature voltages. Q4 and Q5 share a heat sink. Q4 experiences the same temperature changes suffered by Q5. Thermal bias changes also equal. However, Q4 is a PNP device whose base voltage does not vary with temperature. Q4 emitter voltage then becomes more negative as temperature increases and more positive as temperature decreases. This action cancels Q5 thermal-bias reaction, holding the emitter to correct operating levels.

The selection of Q4 depends upon a PNP transistor whose temperature characteristics match those of NPN Q5. Everything has a price. The cost here

was frequency response. Emitter follower Q3 provides the circuit bandwidth. Cross coupling extends the low-frequency response of Q3 and stabilizes input capacitance at the base of Q4.

low-frequency consider-ations

First consider circuit reaction to signals from DC to 5 Hz, eliminating components of little consequence in this frequency range: D4, D5 and R8 protect Q4 against collector-to-base breakdown, maintains Q3-Q4 emitter current, and holds Q5 base and Q2 drain voltages at reasonable levels. Should Q1 and Q2 be removed from the circuit, R8 functions as the base return for Q4. Silicon diodes D4 and D5 clamp at +1.2 V thus preventing reverse breakdown of Q4. The clamping also prevents drastic circuit changes by containing Q3 and Q4 current changes to about 6% and holding Q5 emitter voltage at about +1.2 V. Effects upon temperature compensation and active-device power dissipation are negligible with Q2 in or out of the circuit. Further, the voltage across D4 and D5 represents a reasonable drain voltage for Q2 when it is replaced.

D2 and D3 clamp when signals exceed -1.2 volts to protect Q5 against reverse breakdown.

Diodes, connected as D2-D3 at the base of a PNP transistor, protect preceding or following devices but not the PNP. Imagine D2 and D3 open: Negative base signals cause positive collector signals moving the base-collector junction toward forward bias. An input signal of about -2.5 volts forward biases this junction and current flows from base-to-collector. This is merely normal forward biased diode action. Negative signals of this magnitude do represent reverse breakdown for the following NPN directly coupled to the emitter of Q4.

C5, C6, C7, C8 and R14 react at frequencies higher than those now considered. Using only the remaining components simplifies the initial circuit analysis. Refer to Fig. 3-71.

First determine quiescent conditions: Q3 and Q4 both have turn-on potential. Q4 elevates the zero-volts input one junction setting the voltage across R11, R12 and R13. 10% of the voltage develops across R11. One silicon junction below this base voltage is Q3 emitter voltage. These voltages create Q4-emitter-current demand. 2.4 mA must flow

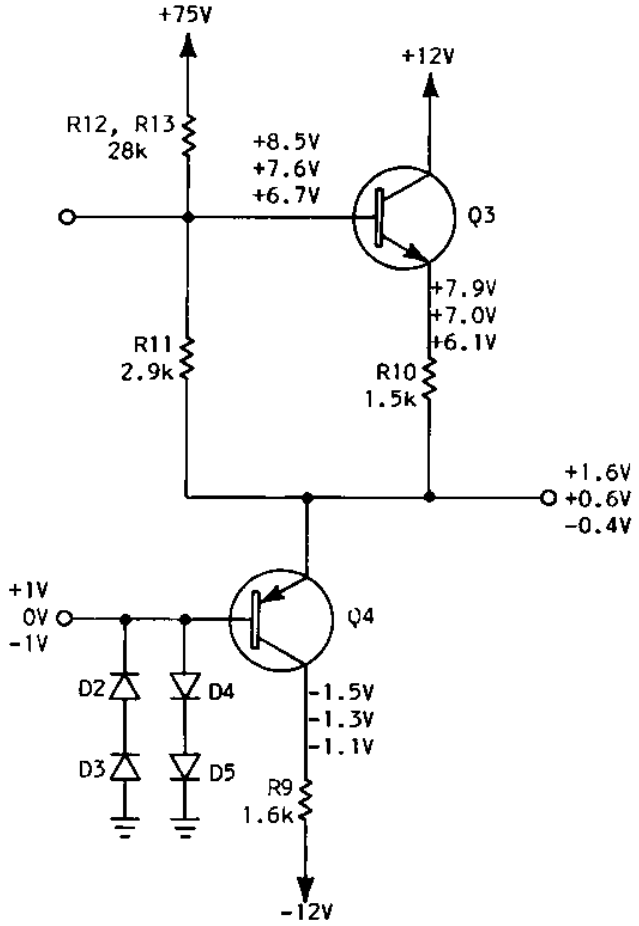


Fig. 3-71. Operating bias circuitry.

through R11 and 4.3 mA through R10. The current sum flows as Q4 emitter, thus collector current. 6.7 mA establishes Q4 collector voltage at -1.3 V. This current stabilizes Q3 and Q4 as longtail current by changing little during maximum signal-voltage variations.

The effects of voltage divider R11-R12-R13 cause Q4 collector-voltage change. A positive 1-volt signal reduces the voltage across R11-R12-R13, reducing current demand. This current change of about 0.03mA per volt adds to Q3 emitter-current change. The voltage divider develops 90% of Q4 emitter voltage at the base, therefore, emitter of Q3. Decreasing the voltage across R10 decreases Q3 emitter current 0.0667 mA. Summing Q3 and voltage-divider current changes, indicates Q4 collector current changes about 0.1 mA.

Negative signals increase Q4 collector current. The voltage divider draws more current and Q3 emitter current increases to drop an additional 0.1 volt across R10 for a -1 volt input.

Consider now the effects of the circuit configuration upon bandpass. Q4 alone couples signals from DC to a few Hz as a longtailed emitter follower, with R11, R12, R13, R10 and Q3 functioning as the longtail. Setting quiescent conditions establishes circuit reaction at the very low end of the bandpass. Due mostly to input capacitance, Q4 frequency response deteriorates at fairly low frequencies. Emitter follower Q3 functions at low frequencies to stabilize Q4 input capacitance.

capacitance stabili-zation

Fig. 3-72 includes circuit components necessary for capacitance stabilization at the base of Q4. The voltage source and its internal resistance (R_S) represent input circuitry. Signals above a few Hz couple through C5 to the base of Q3. Signal driving Q3 has two effects: Emitter current becomes constant, eliminating Q4 Miller-effect, and Q4 input capacitance discharges through C7.

Miller-effect results from Q4 collector-voltage changes. This adds to input capacitance. C5 couples a portion of the input signal to the base of Q3. Each signal increment reduces emitter-current *change*. As frequency increases, greater percentages

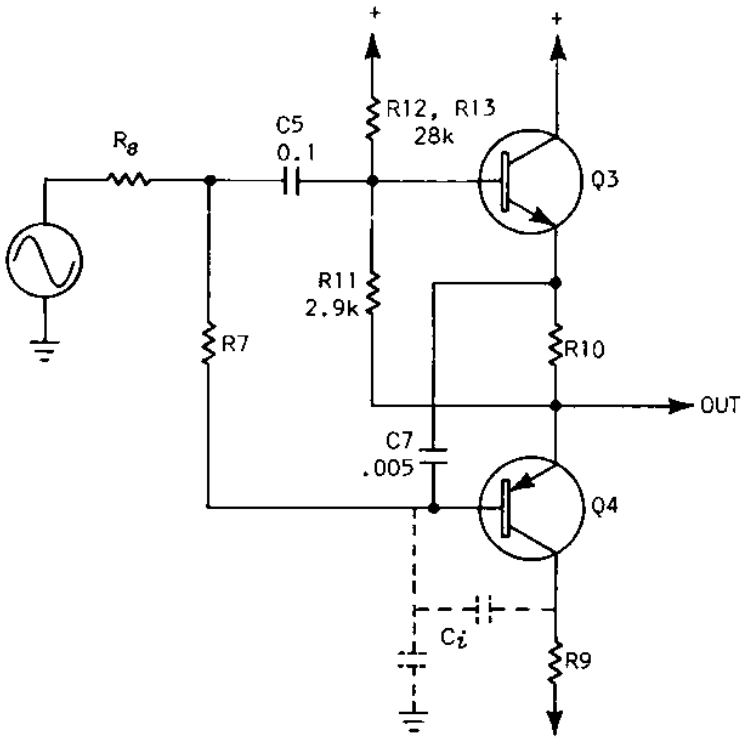


Fig. 3-72. Low-frequency signal circuit stabilizes input capacitance.

of the input voltage appear at Q3 until Q3 and Q4 emitters change equal amounts. When this occurs, emitter, thus collector, current is constant regardless of signal amplitude. Input capacitance is therefore no longer increased by Miller-effect.

Input capacitance yet exists at the base of Q4. This capacitance, however, quickly charges or discharges through C7 and the low emitter impedance of Q3. Cross coupling fails to eliminate input capacitance but does stabilize it to a constant value. C7, empirically selected, is listed at a nominal value.

Selection of C7 depends to a degree upon coupling-circuit time constant at the base of Q3. This time constant should be long to couple low frequencies. There is a problem: Physically or electrically large components contribute reactive shunts.

Returning R11 to the emitters increases the time constant by effectively increasing input R. Signals coupled through C5 develop across R12 and R13 paralleled by R11; an equivalent resistance of 2.8 kΩ. If R11 were returned to ground, the coupling RC time constant would be C5(2.8 kΩ) = 0.28 x 10-3 seconds.

$$F_c = \frac{1}{2\pi\ 0.28 \times 10^{-3}} = 0.57 \times 10^3 = 570 \text{ Hz.}$$

Returning Rll to the emitter increases R, thereby F_c, by 10. At low frequencies, 100% of input voltage develops at the base of Q4 and 90% at the base of Q3. C5 still drives 2.8-kΩ equivalent resistance but this resistance returns not to ground but to 90% of signal voltage. For one-volt signals C5 need couple but 0.1 volt -- or only 36-μA signal current need flow
through C5: 0.1V/2.8kΩ = 36 μA. Since 36 μA develops full signal voltage

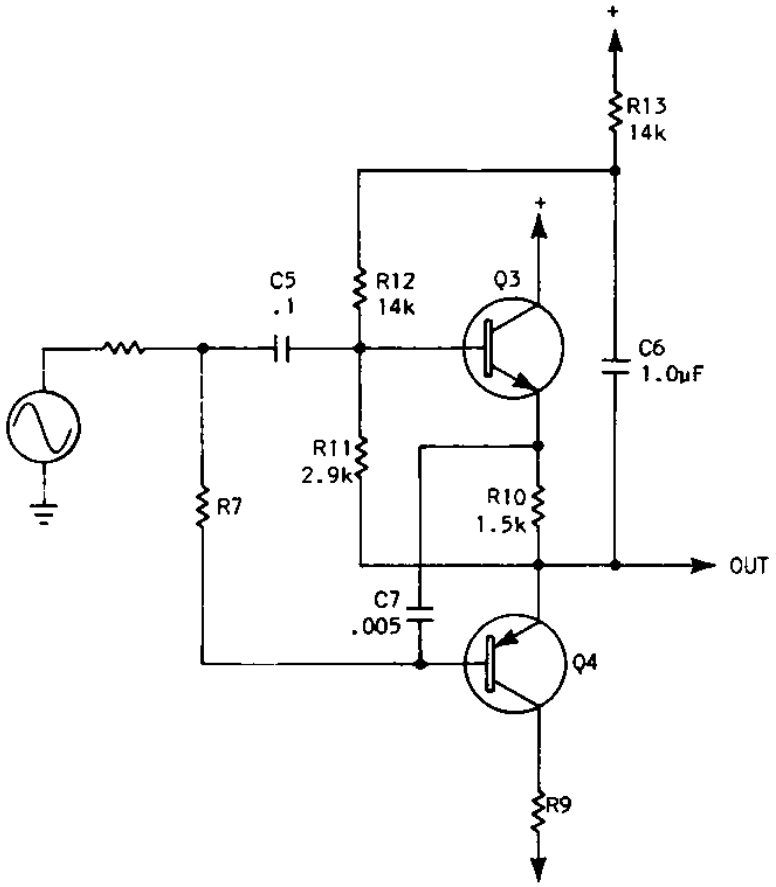


Fig. 3-73. C6 extends Q3 input time constant.

at the base of Q3, apparent input R is 28 kΩ:

$$R = \frac{E}{I} = \frac{1}{36 \times 10^{-6}} = 28 \times 10^{3}\ \Omega.$$

$$T = C5\ (28 \times 10^{-3})\ (2.8 \times 10^{-3})\ \text{seconds.}$$

$$F_c = \frac{1}{2\pi(2.8 \times 10^{-3})} = 0.57 \times 10^{2} = 57\ \text{Hz.}$$

To prevent low-frequency phasing problems Q3 should react to even lower frequencies. Extending low-frequency response must not include increasing the physical or electrical size of C5. This is the purpose of C6.

See Fig. 3-73. C6 shunts R11 and R12 of voltage divider R11-R12-R13. Q4-emitter signal voltages develop across the series circuit C6-R13. Therefore, C6 charge current adds to that demanded by R11-R12; and both currents are in phase with signal voltages. Signal voltages which develop across R13 via C6 increase apparent input resistance at the base, of Q3.

The -3 dB point for C6-R13 is 11.4 Hz. 70% of this input-signal voltage develops across R13, boosting the signal amplitude at the base of Q3. More of Q4 emitter voltage now develops at the base of Q3. Since Q3 equivalent base resistance returns to 97.2% of signal voltage, C5 need provide 10-μA signal current to develop 1-volt signals at the base

$$\text{of Q3: } I = \frac{0.028}{2.8\ k\Omega} = 10 \times 10^{-6}\ A$$

$$R_i \approx \frac{1}{10 \times 10^{-6}} \approx 100\ k\Omega$$

$$F_c = \frac{1}{2\pi\ C5\ R_{in}} \approx 16\ Hz.$$

All of which indicates that C5 couples signal energy to the base of Q3 at less than 20 Hz. Q3 then functions as signal-driven emitter follower maintaining Q4 input capacitance at a low value.

To this point Q4 coupled all signals to the switched-gain amplifier. When one increased input signal frequency and Q4 faltered, Q3 forced proper emitter-follower action. This "bootstrapping" by Q3 works for a portion of the bandpass until, at higher frequencies, Q4 becomes just another passive device.

Consider Q4 a passive device at frequencies above 1.5 MHz. At this frequency C5 couples full signal voltage, C6 is a short circuit and C7 continues to fix Q4 base capacitance. The last two components now come into play.

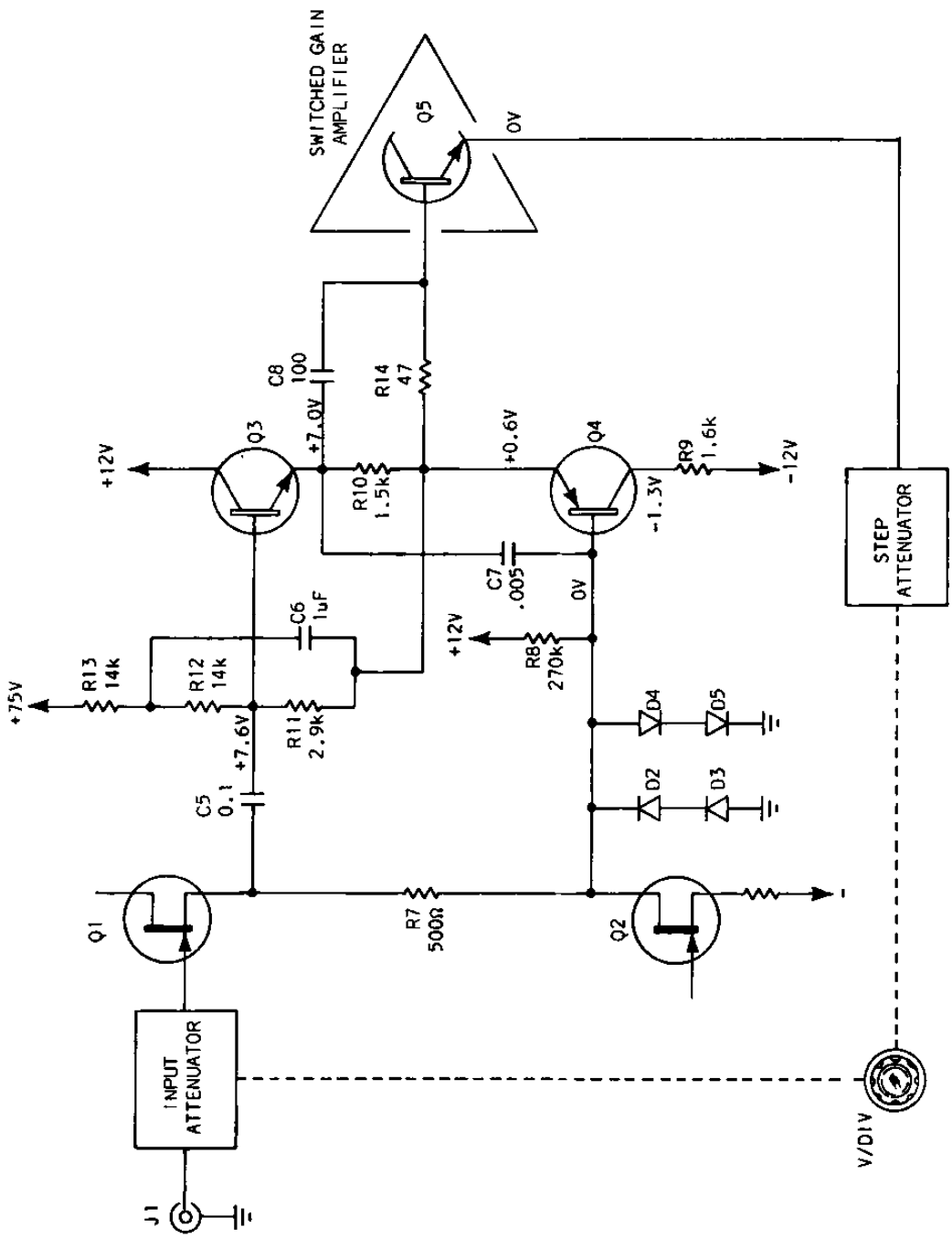


Fig. 3-74. Switched-gain driver amplifier.

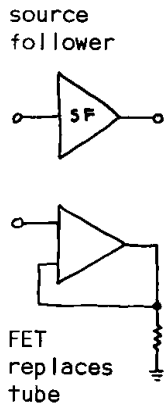
Fig. 3-74 is the complete schematic including C8 and R14.

C8 bypasses R10 providing a coupling path from Q3 emitter to the base of Q5. R14 attenuates signals little if any.

R14 emitter-loads to damp oscillations. As with conventional complementary emitter followers, high-amplitude fast-rise signals develop negative-input resistance characteristics of Q3-Q4. Since C8 bypasses R10, R14 represents total emitter-to-emitter impedance. R14 resistance is sufficient to damp oscillations yet small enough to have negligible effect upon desired signal amplitude.

Although of a different magnitude than cathode followers, emitter followers are high-input impedance, low-output impedance devices. They are found in any circuit of an oscilloscope vertical amplifier except the front end or preamplifier input stage.

A source-follower general description uses the old familiar phrases: High-input impedance and low-output impedance. These words describe any follower. Comparatively, source-follower (SF) input impedance exceeds that of the cathode follower or emitter follower. SF output impedance also exceeds that of the other followers.



Source-follower characteristics result from field-effect transistor parameters. These describe a high-input-impedance semiconductor. Oscilloscopes for years have been solid state except for those circuit points requiring high-input impedance. The FET then becomes attractive as a tube replacement. Some of the advantages are:

- High-input impedance
- Solid-state reliability
- No microphonics
- Excellent aging characteristics
- Small size
- Power-supply demand reduced.

Field-effect transistors fall into two general categories, junction (FET) and insulated gate (IGFET or MOSFET).

CHARACTERISTICS	TUBE	JUNCTION FET	INSULATED GATE FET
INPUT IMPEDANCE	HIGH	HIGH	VERY HIGH
NOISE	LOW	LOW	UNPREDICTABLE
WARM-UP TIME	LONG	SHORT	SHORT
SIZE	LARGE	SMALL	SMALL
POWER CONSUMPTION	LARGE	SMALL	SMALL
AGING	NOTICEABLE	NOT NOTICEABLE	NOTICEABLE
BIAS VOLTAGE TEMP COEFFICIENT	LOW, NOT PREDICTABLE	LOW, PREDICTABLE	HIGH, NOT PREDICTABLE
TYPICAL GATE/GRID CURRENT	≈1nA	≈.1nA	≈10pA
GATE/GRID CURRENT CHANGE WITH TEMP	HIGH, UNPREDICTABLE	MEDIUM, PREDICTABLE	LOW, UNPREDICTABLE
RELIABILITY	LOW	HIGH	HIGH
SENSITIVITY TO OVERLOAD	VERY GOOD	GOOD	POOR

Fig. 3-75. Electron tube vs field-effect transistor.

Only junction field-effect transistors, at this writing, appear in Tektronix vertical amplifiers.

Fig. 3-75 compares tube, FET and IGFET, characteristics. The FET matches or exceeds the tube in every category except one, overload sensitivity. Under IGFET the word *unpredictable* expresses today's FET preference.

conductivity voltage controlled

A FET is a resistance whose conductivity is voltage controlled. Majority carriers travel the *channel* which consists of "n" or "p" material. The majority carriers enter the channel at the *source* and exit at the *drain.*

n channel

source

drain

Fig. 3-76 is an "n" channel. Electrons, "n"-material majority carriers, flow from the negative voltage at the source through the channel to the positive voltage at the drain. Only voltage polarity determines which is the drain and which is the source end of the channel. Drain current (I_D) always flows from source to drain in "n" channels.

p channel

Majority carriers are holes in "p" channels. Therefore "p" channels function as described for "n" channels.

Just remember to reverse polarity: ID always flows from drain to source in a "p" channel.

channel voltage gradient

Fig. 3-77 illustrates a very simple but important point: A voltage gradient develops along the channel. The channel is nothing more than a resistance without polarity. But if one could reach into the device he would measure voltage differences along the channel, becoming more positive as he neared the drain ("n" channel). If drain current flows a voltage gradient must develop: E = IR.

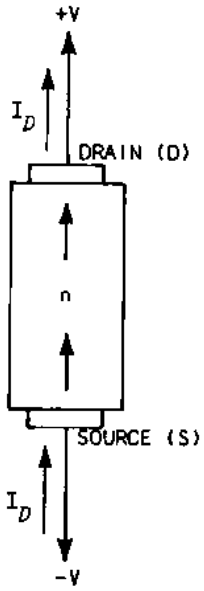


Fig. 3-76. FET channel.

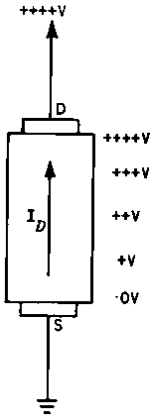


Fig. 3-77. Drain current develops voltage gradient across the channel.

Keep the voltage gradient in mind while completing the FET model. A *gate* is the final terminal needed.

gate

Picture the channel as a bar of "n" material with connectors at either end. Now join two smaller pieces of "p" material at either side of the bar, centered along its length. Add connectors and label the terminal *gate.* Fig. 3-78 is such a model.

depleted region

This figure shows an intrusion into the channel called a depleted region. When the "p" and "n" material join a change occurs at the junction. Free electrons in the channel fill "p"-region holes. Right at the junction a barrier forms preventing further combination of holes and electrons. Around the junction is a small area almost devoid of free carriers. Increasing the depleted area is the operating principle of an FET. This also explains why a junction FET is called a *depletion-mode* device.

Returning gate and source leads to ground and the drain lead to a low-impedance supply allows zero-bias analysis (Fig. 3-79). The emitter follower functions as a low-impedance drain-voltage supply. Setting emitter voltage slightly positive causes drain current to flow. Since the gate and source leads are shorted, gate-to-source voltage *(V_{GS})* is zero. I_D indicates drain current under this condition.

Initial drain-voltage (V_D) application caused "p"-material holes to move toward the gate terminals, but channel holes cannot cross the junction. Current flows only when carriers flow continuously through the entire circuit. This also applies to electrons. Channel electrons move away from the junction, but the gate (p) provides no free electrons to cross the junction.

channel resistance increased

Channel electrons pulled from the area near the gate leave this region completely free of carriers. The original small depleted area enlarges as shown. A depletion region conducts poorly. Enlarging this region then reduces the effective channel cross section, increasing channel resistance.

Notice that the depletion region skews toward the drain. Drain current develops a channel-voltage gradient creating this shape. I_D flows through a

length of "n" material, between the source connection and the nearest gate-junction edge. The resultant voltage drop, representing reverse bias, pulls the depletion region toward channel center. Reverse bias increases along the channel, pulling the depletion region further into the channel. Gate-to-drain voltage *(V_{GD})* of course represents maximum reverse bias.

pinch-off

Increasing drain voltage (V_D) increases I_D and the depleted area up to a point. Raising V_D above this point affects no I_D increase. This point carries the name *pinch-off* (V_V). The depletion region appears to reach into the channel and “pinch-off” any change in drain current.

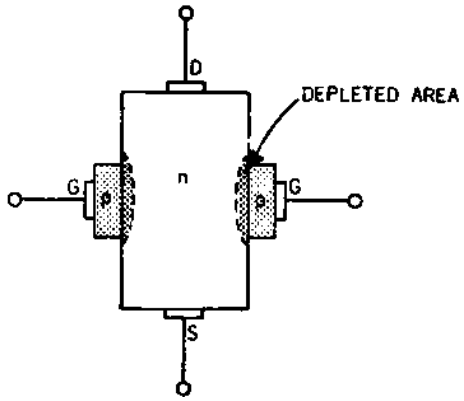


Fig. 3-78. Field-effect transistor model, n channel.

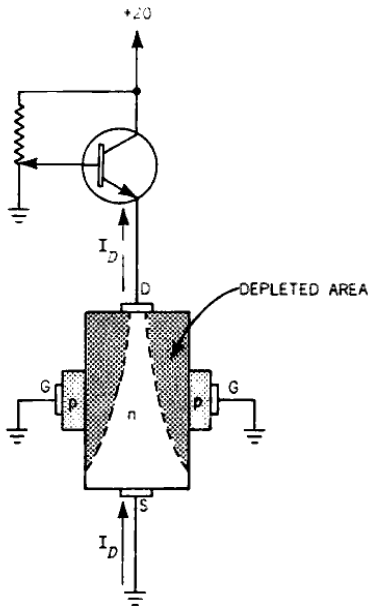


Fig. 3-79. Voltage gradient increases area depleted.

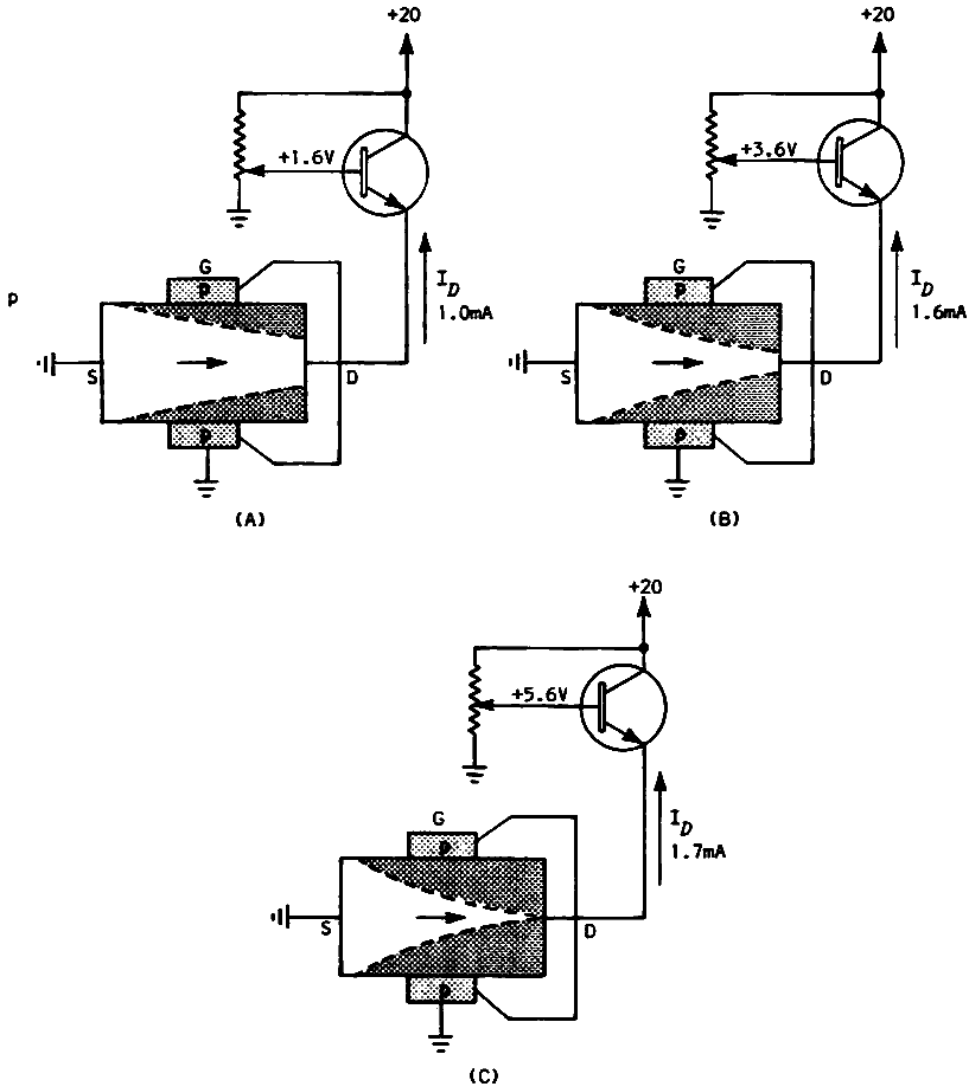


Fig. 3-80. ID increasing with V_D.

V_p

The FET models in Fig. 3-80 show the effects of increasing V_D. In (A) 1 volt at the drain draws 1-mA drain current, creating a depletion region enlarged at the drain end. Increasing V_D 2 volts (B) increases I_D by 0.6 mA and the depletion area extends further into the channel. Raising V_D another 2 volts to 5 increases I_D only 0.1 mA. The depletion regions almost touch. V_D increases, above 5 volts, draw no more than 1.7 mA through the channel. This then is pinch-off voltage (V_p).

Pinch-off occurs when the bias from *drain* to *gate* causes maximum depletion-region growth. Remember, V_p is a value of drain-to-gate voltage *(V_{DG}).*

A curve of this action appears as Fig. 3-81A. V_D increases, between 0 and 5 volts, increase I_D. Above 5 V_D, I_D changes little. When a voltage change across a device causes a current change in the device, the device has a predictable ohmic value. For this reason, call that portion of the curve below V_p the *ohmic region.* Above V_p, I_D remains constant with changes in V_D indicating infinite dynamic resistance.

ohmic region

IDSS

Drain-current nomenclature also changes above V_p. With gate and source shorted, I_D above V_p is considered saturated channel current: I_{Dss}.

drain-to-source resistance

Resistance in question appears as the FET drain-to-source resistance *(r_{ds}).* The r_{ds} curve, related to Fig. 3-81A, is plotted in Fig. 3-81B. Large r_{ds} values result from self-bias created by the voltage gradient between source and gate. FET curves thus resemble those of a triode with a large unbypassed cathode resistor.

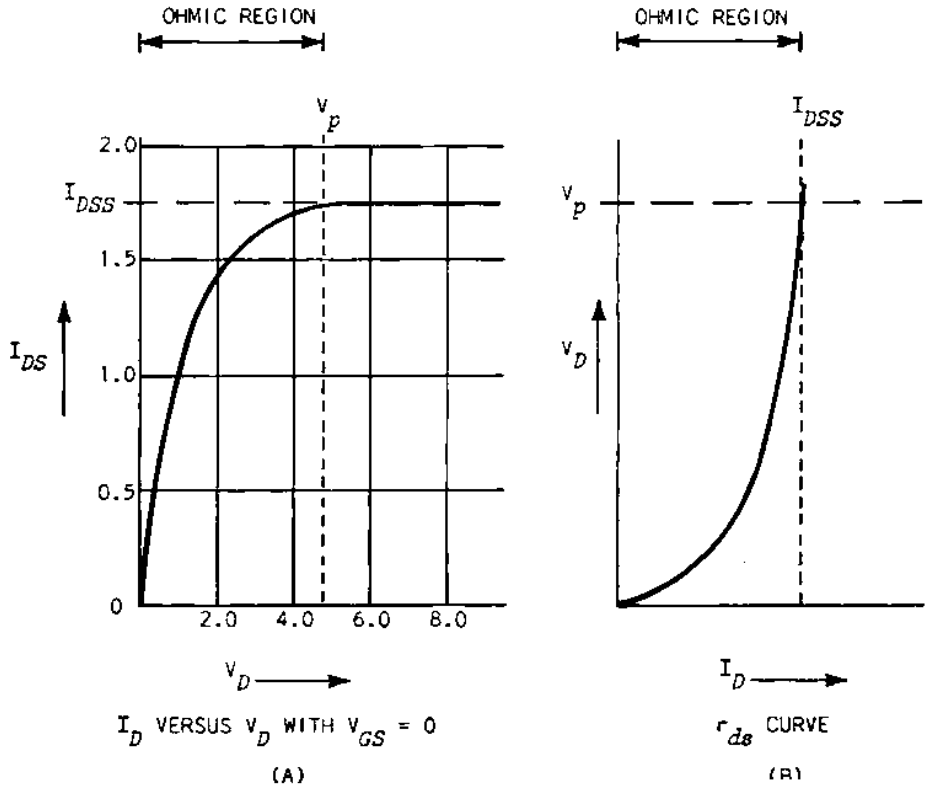


Fig. 3-81. Ohmic and pinch-off regions.

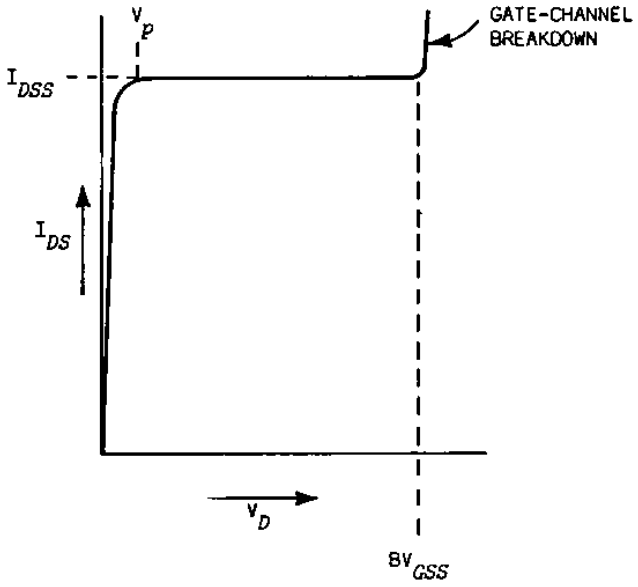


Fig. 3-82. Gate-to-channel breakdown, $V_{GS} = 0$.

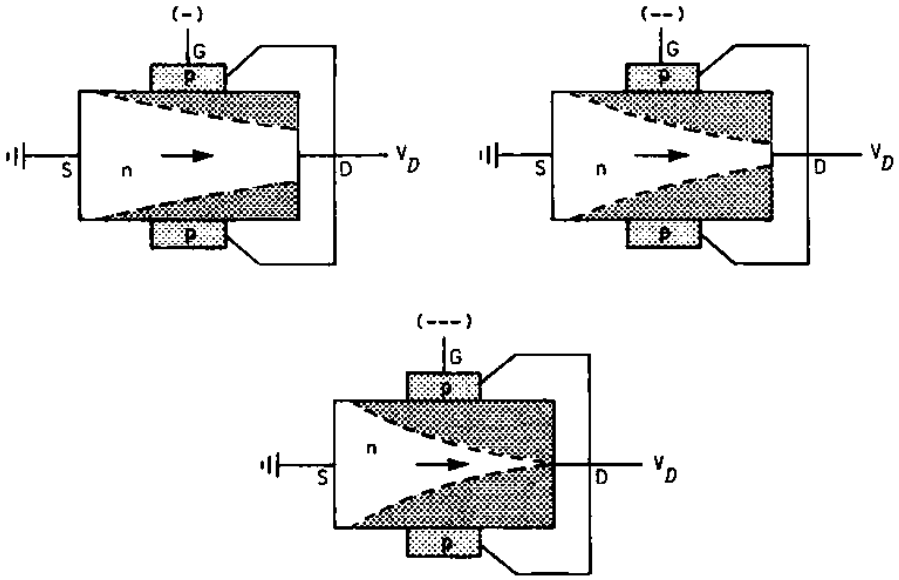


Fig. 3-83. Back-bias controlling-current flow in an n-channel FET.

gate-channel breakdown

Do not dismiss an FET as analogous to a tube, whether triode or pentode. This is a semiconductor. gate-to-For example, increasing V_D far above Vp causes to-channel breakdown. I_{DSS} of Fig. 3-82 remains constant as V_{DD} increases until reaching gate -to - channel breakdown voltage *(BVGSS)*• The I_D curve now ascends toward infinity. Operating an FET into *BVGSS* usually destroys the device.

Drain-to-gate *bias* (V_{DG}) controls channel cross-section area at the drain end of the channel. Gate-to-source bias *(V_{GS})* sets channel-current demand for a given V_D. Therefore small voltage changes at the gate cause relatively large I_D changes.

controlling conduction with *VGS*

The model of Fig. 3-83 controls I_D with V_{GS}. Here the source returns to ground, the drain to a set low-impedance voltage supply and gate voltage varies. Initial V_{GS} restricts I_D little. Applying greater negative voltage increases the depletion area, subtracts from channel area, thereby opposing I_D ' This continues until the device reaches pinch-off voltage. V_p occurs when *drain-to-gate* bias reaches the same value as with the 0- V_{GS} drain curve.

Since one most often measures voltage to ground or the source, V_p specifications list V_D and V_{GS} voltages at some small I_D flow. Many consider that driving the gate to V_p achieves cutoff. This for most practical measurements is true. A junction FET *cannot* be cut off or a voltage gradient across the channel would not develop. However, only nano-amperes or microamperes of I_D flow at V_p (cutoff).

Displacement current establishes basic input capacitance at the gate. Assume gate voltage, in the model of Fig. 3-83, swings from minimum negative to maximum negative then back to minimum negative. The depleted area swells then shrinks with gate-voltage changes. Depletion region carriers move with the region. This is displacement current. The name and effect are those of a capacitor dielectric.

drain characteristic curves

Plotting drain current versus drain voltage at various gate-voltage steps develops drain-characteristic curves. Fig. 3-84 drain characteristics resulted from a photograph of a Tektronix curve-tracer display. Pinch-off occurs at 6 volts. Only when *VGS* = 0, do V_p and V_{DS}, equal. However, V_p is always 6 V_{GD} for this particular device. Consider V_D values for V_{GS} settings other than zero:

At V_p, when V_{GS} = 0, V_D = +6
V_{GS} = -0.5, V_D = +5.5
V_{GS} = -1.0, V_D = +5.0
V_{GS} = -1.5, V_D = +4.5
V_{GS} = -2.0, V_D = +4.0.

Experimenters have difficulty pinpointing V_p and circuit analysts sometimes need to know *gm* of a given device. A transfer curve provides information for both.

Fig. 3-85 is such a curve. Determining I_{DSS} is simple and plotting other I_D points are easy enough until V_{GS} approaches V_p. I_D changes little near V_p, destroying confidence in the final V_p point. However, lay a straight edge at the I_{DSS} intercept

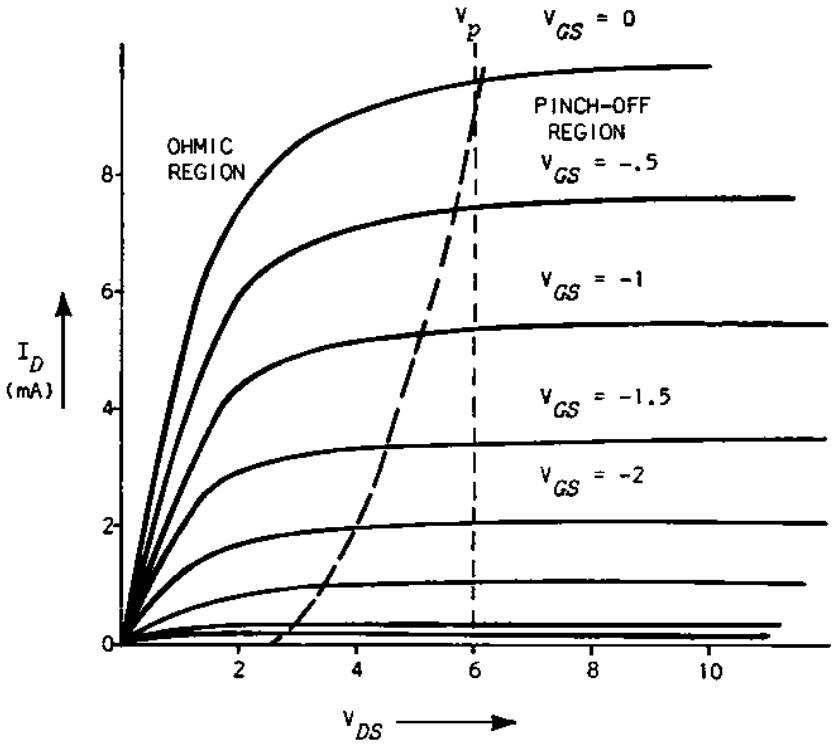


Fig. 3-84. Drain characteristics of FET.

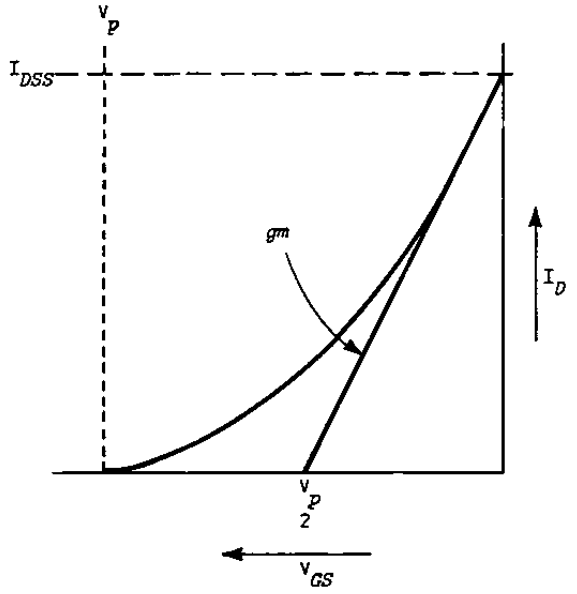


Fig. 3-85. Drawing a tangent to the transfer curve establishes *gm* and V_p.

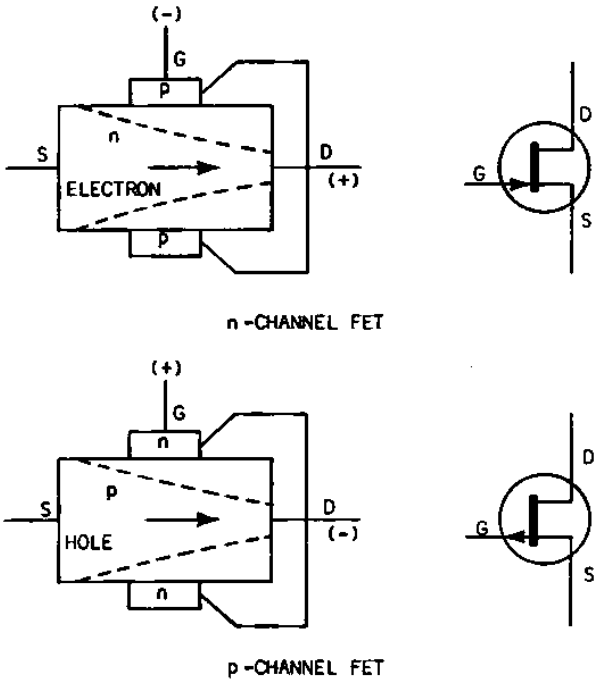


Fig. 3-86. Comparison of an n-channel FET and a p-channel FET.

plotting gm and Vp

and draw a line, tangent to the curve, to intercept V_{GS} The tangent intercepts at one-half V_p. The slope of the line is *gm*.

Fig. 3-86 compares "n"- and "p"-channel FET's. These FET's operate alike. They *are* "on" *devices* operated

toward cutoff. Stated differently: An FET, either "p" or "n" channel, performs when reverse-biased.

A forward-biased junction FET essentially ceases to be an FET. Input impedance falls and drain current bears no useful relation to input signals. This might well raise a question: Since the gate normally draws no current, and gate voltages control channel depletion electrostatically, what happens if an insulator be placed between gate and channel?

depletion mode IGFET

The answer: The device becomes an Insulated Gate FET (IGFET). Gate voltages deplete the channel as before with far lower gate leakage current (I_{GSS}). Now, however, ordinary metal serves as well as semiconductor for gate material. Call this device *a depletion-mode IGFET.*

MOSFET

The model of Fig. 3-87 is named MOSFET. This stands for Metal-Oxide-Silicon FET, one of several advertising names for IGFET's. MOSFET does describe IGFET construction. The silicon channel lays in substrate covered by insulation, a thin oxide layer thermally formed on the semiconductor surface. A layer of metal deposited on the oxide forms the gate. Holes in the oxide provide source and drain lead access to the channel.

surface effects

IGFET gate voltages create effects which take place near the semiconductor surface. The channel surface, oxide insulator and metal gate form a capacitor.

enhancement mode

Forward-biasing a properly designed IGFET enhances channel conductivity. Fig. 3-88 illustrates an IGFET which operates in the depletion *and* enhancement mode. The lightly doped channel, a moderate conductor, terminates in heavily doped regions at the drain and source. Negative gate voltages deplete the channel. Positive voltages enhance conductivity by inducing charges into the channel. Since the input is a capacitor, positive gate voltages cause equal negative charges on the surface of the channel.

A concentration of electrons forms this negative charge *enhancing* the channel.

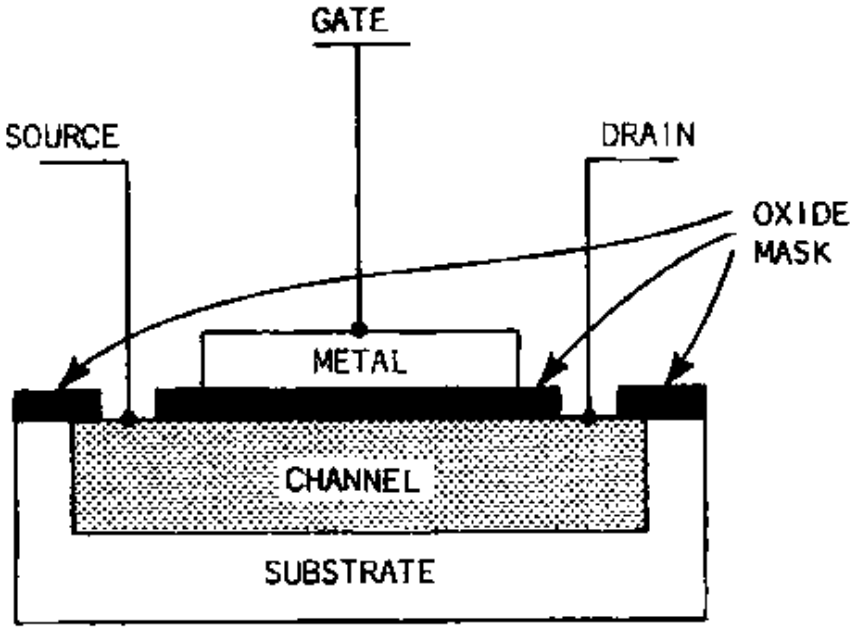


Fig. 3-87. Depletion-mode-only MOSFET construction

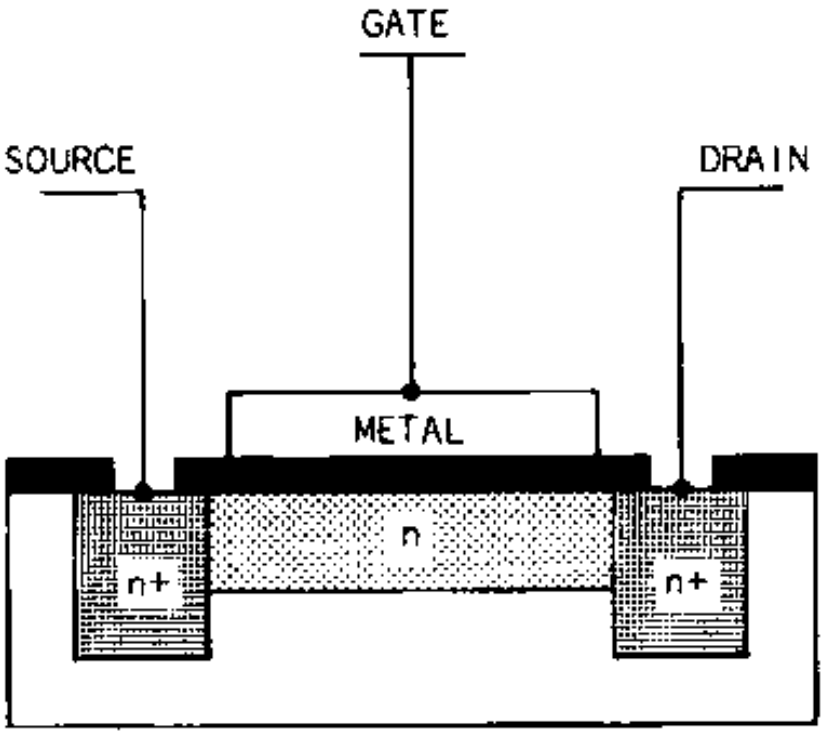


Fig. 3-88. Construction of an IGFET which operates in enhancement and depletion modes.

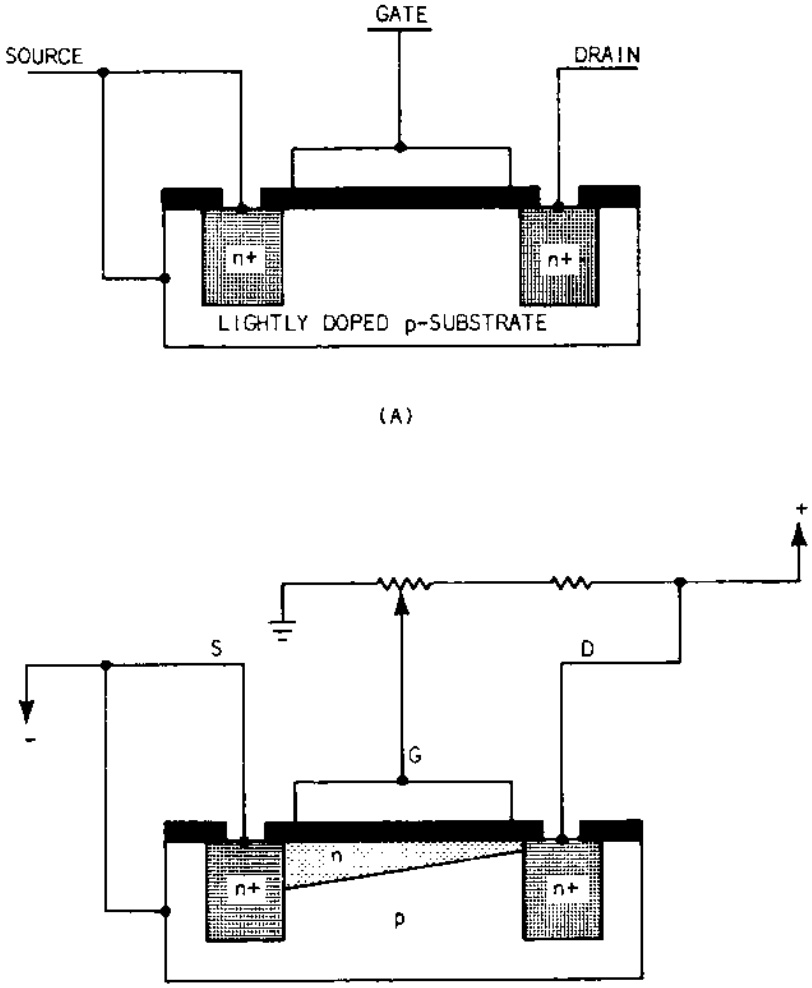


Fig. 3-89. Enhancement-mode-only IGFET.

The third type of IGFFT works in the enhancement mode only. Fig. 3-89A is a model of this type IGFET. Channel "p" material prevents current flow between the heavily doped "n" source and drain. In the absence of forward gate voltage no drain current flows. One of the channel "pn" junctions, with the gate open, is always reverse-biased regardless of voltage polarity across the channel.

Forward bias, as shown in Fig. 3-89B, causes channel conduction. Sufficient forward bias induces charges into the channel, bridging source and drain. This actually changes the "p"-channel surface into an "n" semiconductor.

transfer character-itics

IGFET transfer characteristics follow as the FET. Fig. 3-90 shows relative characteristics. Notice I_{DSS} relationships: lags is maximum I_D for depletion only devices and zero for enhancement-mode only IGFET's.

IGFET's do not at present appear in Tektronix vertical amplifiers. Whether IGFET's will appear in the future is pure conjecture. A number of companies devote considerable developmental activity to all types. Today junction FET's are cheaper and more predictable.

Schematic IGFET symbols appear in Fig. 3-91.

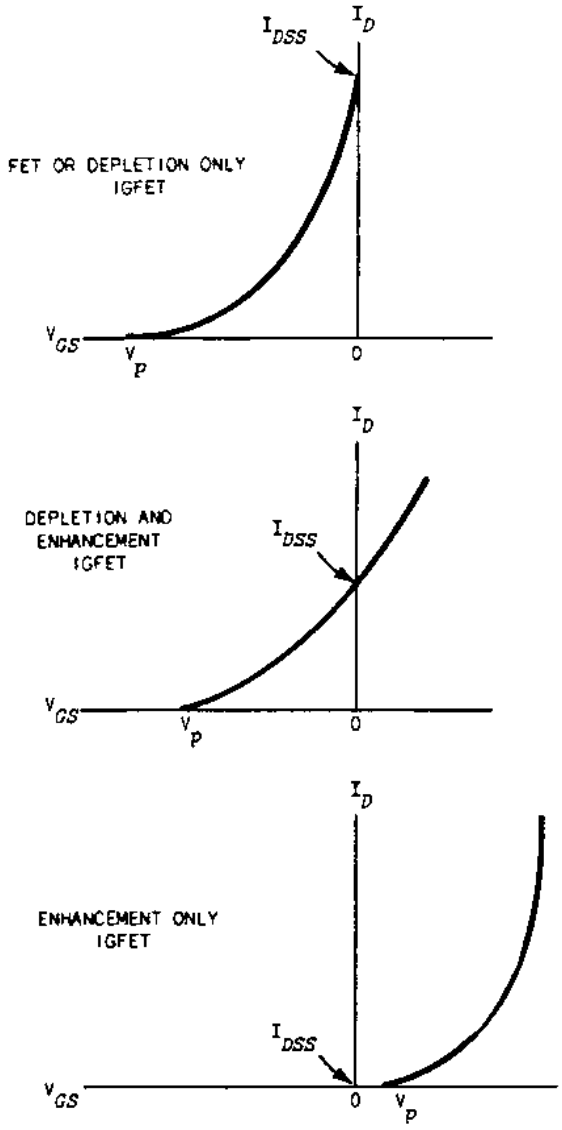


Fig. 3-90. Transfer characteristiccomparison.

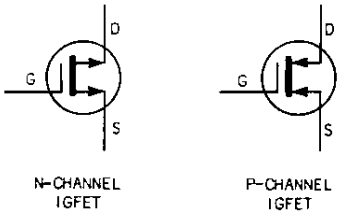


Fig. 3-91.

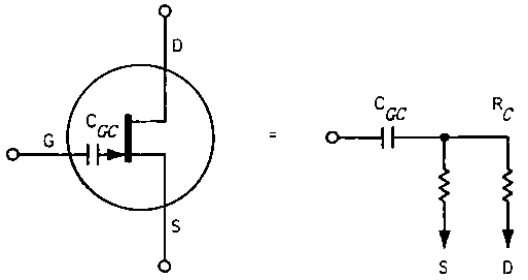


Fig. 3-92. The field-effect capacitance forms part of SF input capacitance.

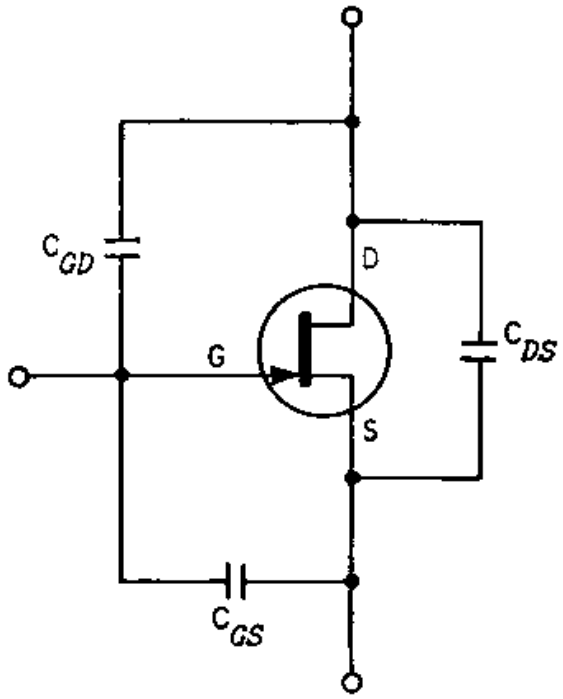


Fig. 3-93. Designating inter-element capacitance.

CGC

Source follower terms differ but effects parallel those of the other followers. Input impedance, Miller-effect, output impedance and voltage gain receive similar treatment. One component, however, differs from other three terminal devices, "gate-to-channel capacitance (C_{GC})." (Fig. 3-92.)

Field-effect is C_{GC}. Gate voltages cause displacement current within the semiconductor material which defines C_{GC}. Signals applied to the gate develop across CGC in series with a small resistance. This resistance is the parallel value of drain-to-gate and source-to-gate channel resistance. C_{GC} must then be small to prevent signal-source loading. Incidentally, this presents an FET design problem: High transconductance requires a large gate, but low input capacitance requires a small gate.

input capacitance

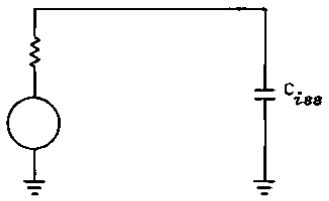
C_{GC} constitutes a portion of input capacitance (C_{iss}). Interelement capacitances combine to appear as C_{iss}. Fig. 3-93 labels these capacitances. C_{DS}, drain-to-source capacitance, adds to output capacitance rather than input. Gate-to-drain (C_{GD}) and gate-to-source (C_{GS}) capacitances shunt C_{GC} • The sum C_{GD}, C_{GS} and C_{GC} is C_{iss} with drain and source shorted.

Source-follower configuration changes C_{iss} somewhat. Returning the source to ground through a resistor and the drain to V_{DD} (apparent ground) slightly modifies C_{iss}. Stray capacitance and C_{DS} shunt the source resistor, thereby appearing in series with C_{GS}. This reduces C_{GS} apparent value from gate to ground, reducing input capacitance. C_{GD} remains constant since it returns to apparent ground at the drain.

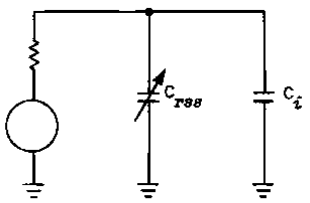
reverse capacitance

C_{GD} is the Miller-effect coupling capacitor. Adding a resistance between drain and V_{DD} causes C_{GD} to increase ($1 + A_V$) times. The effect carries the name reverse capacitance (C_{rss})• Listing C_{rss} with a specific value "ss" indicates source and gate shorted.

Fig. 3-94A shows the equivalent input circuit of a source follower whose drain returns to apparent ground. The signal generator works into a capacitive load equal to C_{iss}. On the other hand, loading the drain changes input C as indicated in



(A) COMMON DRAIN INPUT C



(B) COMMON SOURCE INPUT C

Fig. 3-94.

Fig. 3-94B. C_i consists of C_{iss} less C_{GD}. C_{rss}, which is C_{GD} varied by gain, shunts C_i as the generator load. Miller-effect occurs as in electron tubes and transistors. An FET merely has less capacitance to be affected.

follower gain similarities

Voltage gain is also similar. See Fig. 3-95. The source-follower reaction to an input step reproduces an output with slightly rounded corners and some signal loss. Rounded corners result from reactive components first presented. Signal loss indicates some form of voltage division.

voltage gain less than unity

The input step develops across external resistance R_S and internal channel resistance r_s in series. Voltage gain can never be more than the ratio of R_S to total resistance. However, a large R_S and a small r_s result in small signal losses. Assume 0.8 or better as longtailed-source-follower gain.

longtailing

Longtailing has the obvious advantage of providing large R_S values but there is another. An FFT is a square-law device. Operating in the ohmic region causes r_s to vary according to square-law. Current driving an FET by longtailing maintains operation in the pinch-off region which may not reduce but holds r_s constant.

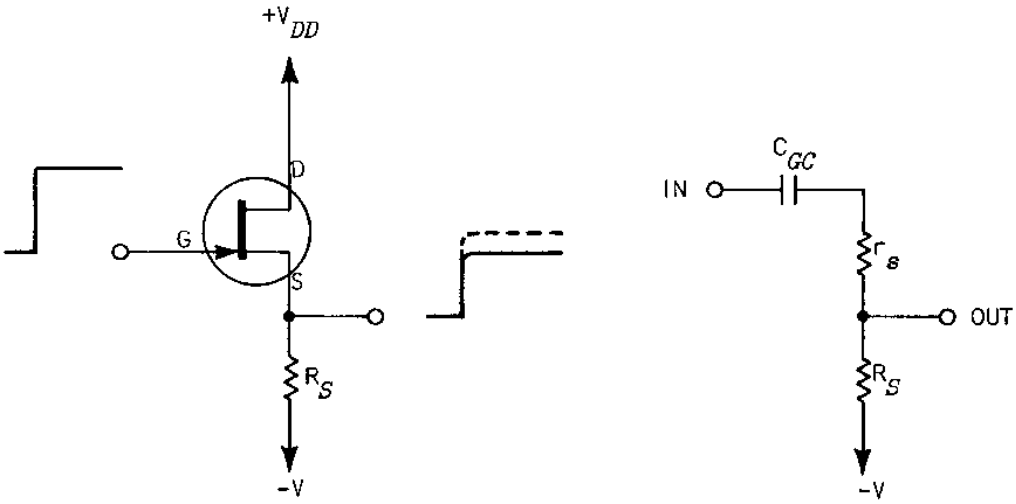
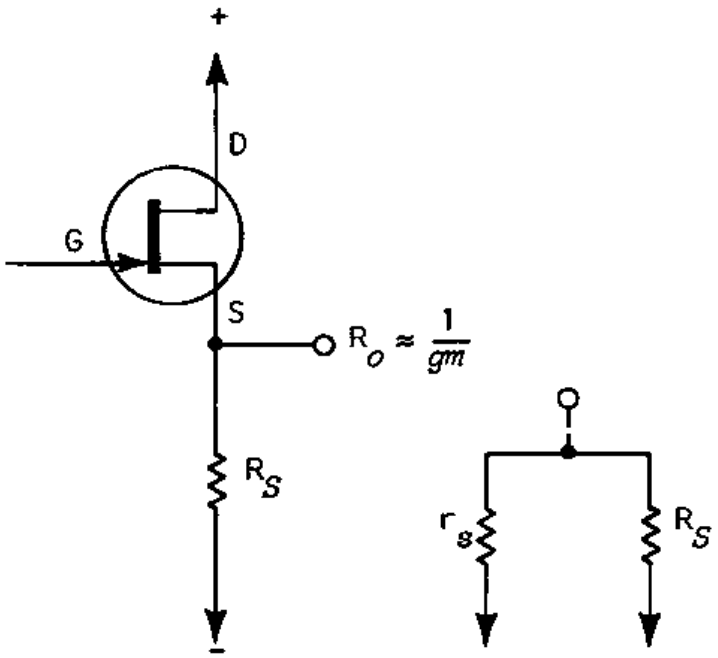


Fig. 3-95. $A_V \approx \frac{R_S}{r_s + R_S}$



$$R_o = \frac{R_S r_s}{R_S + r_s} \text{ IF } R_S >> r_s,\ R_o \approx r_s \text{ AND}$$

$$r_s \approx \frac{1}{gm} \text{ WHEN OPERATING ABOVE } V_p.$$

Fig. 3-96.

output impedance

R_S and r_S also determine output impedance. Like r_K inverting transconductance approximates r_S. And if

R_S be large, $R_0 \approx r_S \approx 1/gm$. Fig. 3-96 indicates

this. However, if R_S fails to exceed r_S by ten, R_0 must be considered the parallel value of R_S and r_S. An FET has fairly low *gm* (somewhere between 500 and 3000 µmhos). Higher-*gm* devices occur as design and manufacturing techniques improve. While considering FET circuit description in this book, assume 2000 µmhos, an r_S of 500 Ω.

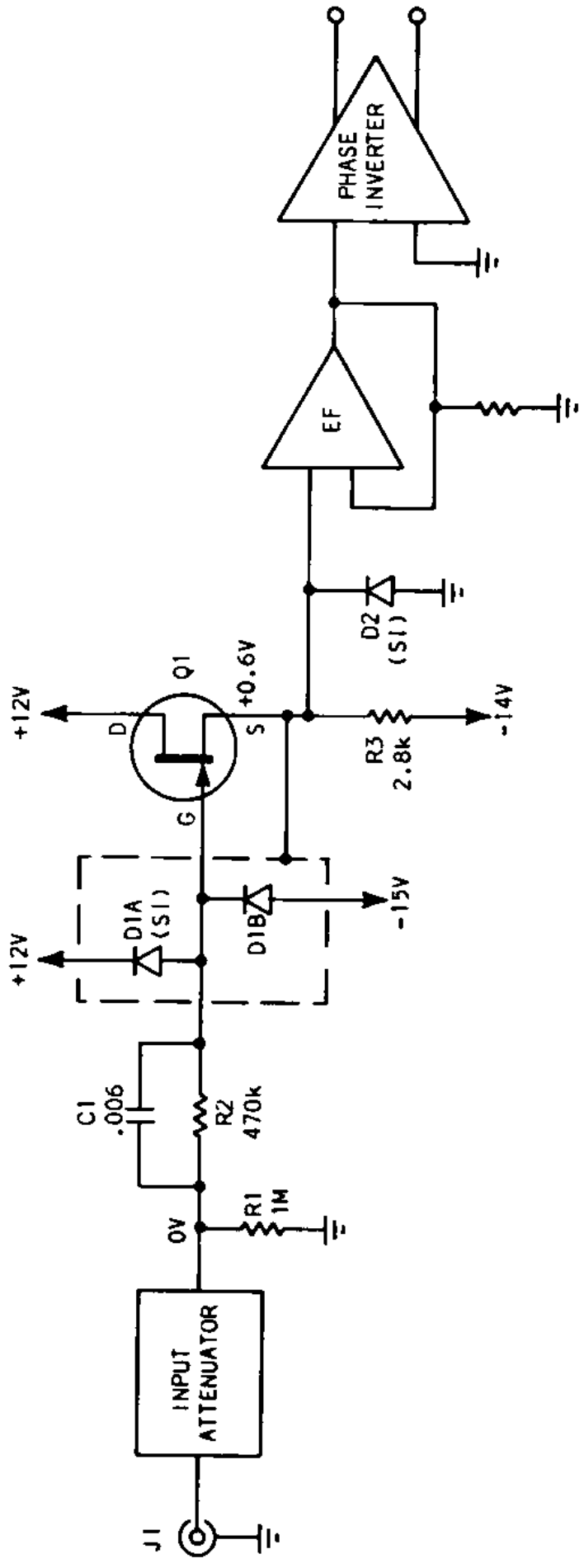


Fig. 3-97. Source-follower input amplifier.

input amplifier

Passive components of the SF input amplifier appear at first identical to those of a CF. As a case in point refer to the input amplifier of Fig. 3-97. R1, R2, R3, D2 and C2 appear in the same configuration here as in a CF input amplifier. R1, R3, D2 and C1 react in a similar fashion. R2, however, limits when D1A or D1B is on, rather than utilizing leakage current *(I_{gss}).*

R1 returns the gate to ground. And it forms a part of the input-attenuator voltage divider.

C1 serves as a current source which rapidly charges and discharges input capacitance. Input capacitance would otherwise charge through R2 slowing SF reaction to "fast" signals.

R2 prevents a low-resistance shunt of the circuit under test during conduction of D1A or B.

limiting

D1A serves as a current source which reduces Ql-gate-current demand. Applying a signal, +12.6 volts or more, to the gate of Q1 forward biases the gate-drain junction. This is not necessarily harmful to Q1. Current flows from drain to gate as in any semiconductor diode and is limited by R2. However, heavy current from drain-to-gate slows the recovery time of Q1. D1 has much less forward resistance than Q1 therefore excess positive inputs draw most of the current through D1A and very little through Q1. In the X1 attenuator position D1 in series with R2 shunts the circuit under test.

protection

D1B protects Q1. Positive voltages at the gate of Q1 can draw current from the drain or source or both. This does no damage, Q1 merely becomes a forward-biased "pn" junction. However, moderate current flow into the channel from the gate destroys an "n"-channel FFT! D1B turns on when input voltages exceed -15.6 volts, clamping V_G so that V_{DG} fails to reach BV_{SS}. The voltage "window" between clamps is as large as Q1 can handle since V_{DD} = +12 V and V_{SS} = -14 V.

reducing input capacitance

Tying the case of D1 to the source of Q1 reduces input capacitance. Stray capacitance associated with D1 must return to some reference for its effect to be predictable. Returning this capacitance to the source reduces the voltage across the capacitance, reducing effective gate capacitance.

clamping

R3 longtails and D2 clamps to protect the emitter follower. D2 prevents the voltage at the FF input from exceeding -0.6 V, resulting from signals or the removal of Q1.

reducing output impedance

The emitter follower functions as an impedance transformer. In this case the transistor phase inverter receives drive from 5 or 10 Ω rather than 500 Ω or more at the output of Q1.

balanced phase-inverter input impedance

Equal impedance at each phase-inverter input terminal is often as important as low-impedance drive at the active terminal. One terminal of the phase inverter is shown at ground. This is apparent ground. Both terminals return to an equal quiescent bias and, ideally, to equal input impedance. One method to accomplish this is to bias the undriven terminal of the phase inverter with circuits identical to the signal-drive chain. Fig. 3-98 is appropriate.

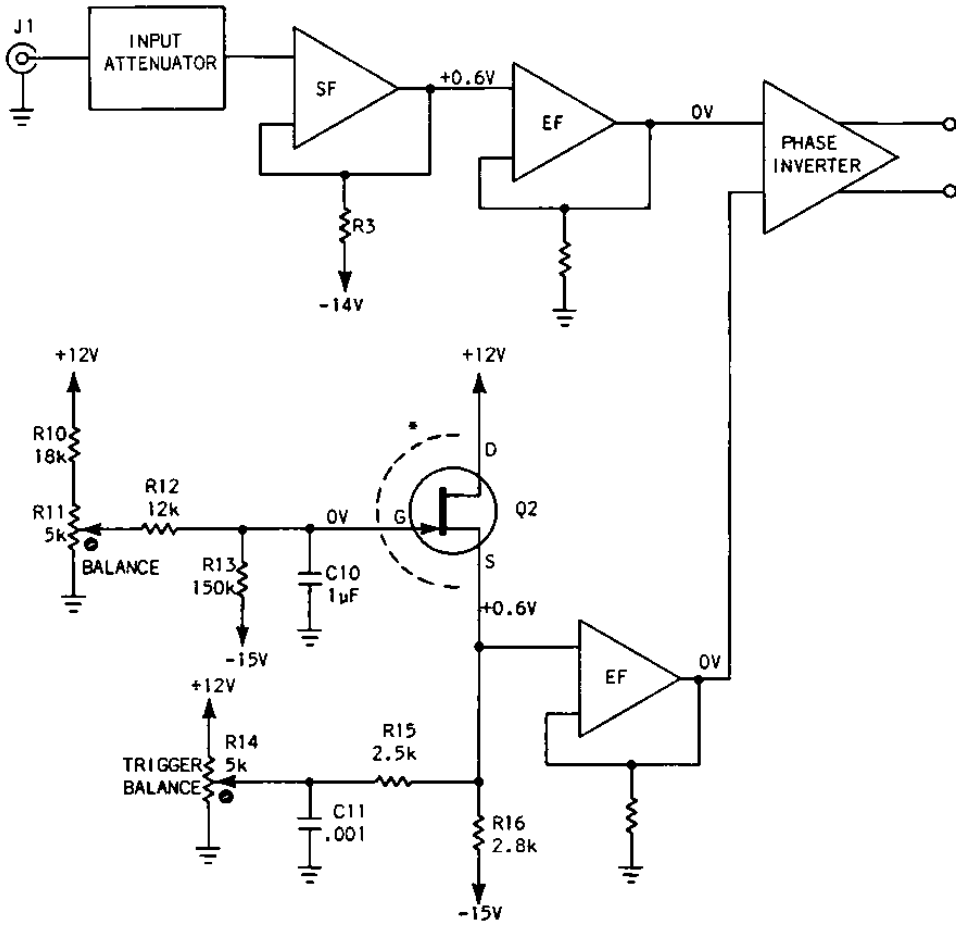


Fig. 3-98. Balancing the phase-inverter input terminals.

balanced phase-inverter bias

Of the same FET type, Q1 and Q2 share temperature environment. Identical emitter followers drive the phase inverter, therefore one sets Q2 gate voltage for a quiescent null across the phase-inverter input terminals. Now the phase inverter receives not only equal zero-signal voltages but equal low-impedance drive.

balancing adjustment

R10, R11, R12 and R13 in the gate circuit of Q2 sallow one to adjust Q2 gate voltage between -1.1 V and +7.0 V. This is sufficient range to compensate for any parameter differences between Q1 and Q2.

C10 filters any transients which might appear at the gate of Q2 and slows power-supply fluctuation effects All of which holds Q2 output constant so that the undriven terminal of the phase inverter represents apparent ground.

Longtail R16 is shunted by another balancing network. This network balances SF output resistance. Although R16 and R_S for the input SF (R3) equal, R16 returns to -15 V and R3 returns to approximately -14 V. A trigger pickoff circuit, not shown, develops v_{ss} for Q1. Trigger-pickoff part tolerances cause v_{cc} variation between units, and part replacements cause some variation. The result is an off-center zero-signal CRT display. With the signal input grounded, one adjusts R14 for a centered display.

Drain current controls *gm; **1/gm*** is r_S; r_S has the greatest control of R_0; and longtailing sets drain current.

To show how R14 adjustments balance R_0, keep the above facts in mind and assume three conditions for Q1 V_{SS}:

1. V_{SS} = -13 V
2. V_{SS} = -14 V
3. V_{SS} = -15 V.

Under condition 1, Q1 draws 4.6-mA I_D. Q2 source voltage, set equal to Ql, establishes the voltage drop across R16 creating a demand for 5.4 mA. Apparently, Q2 draws 0.8 mA more I_D than Ql.

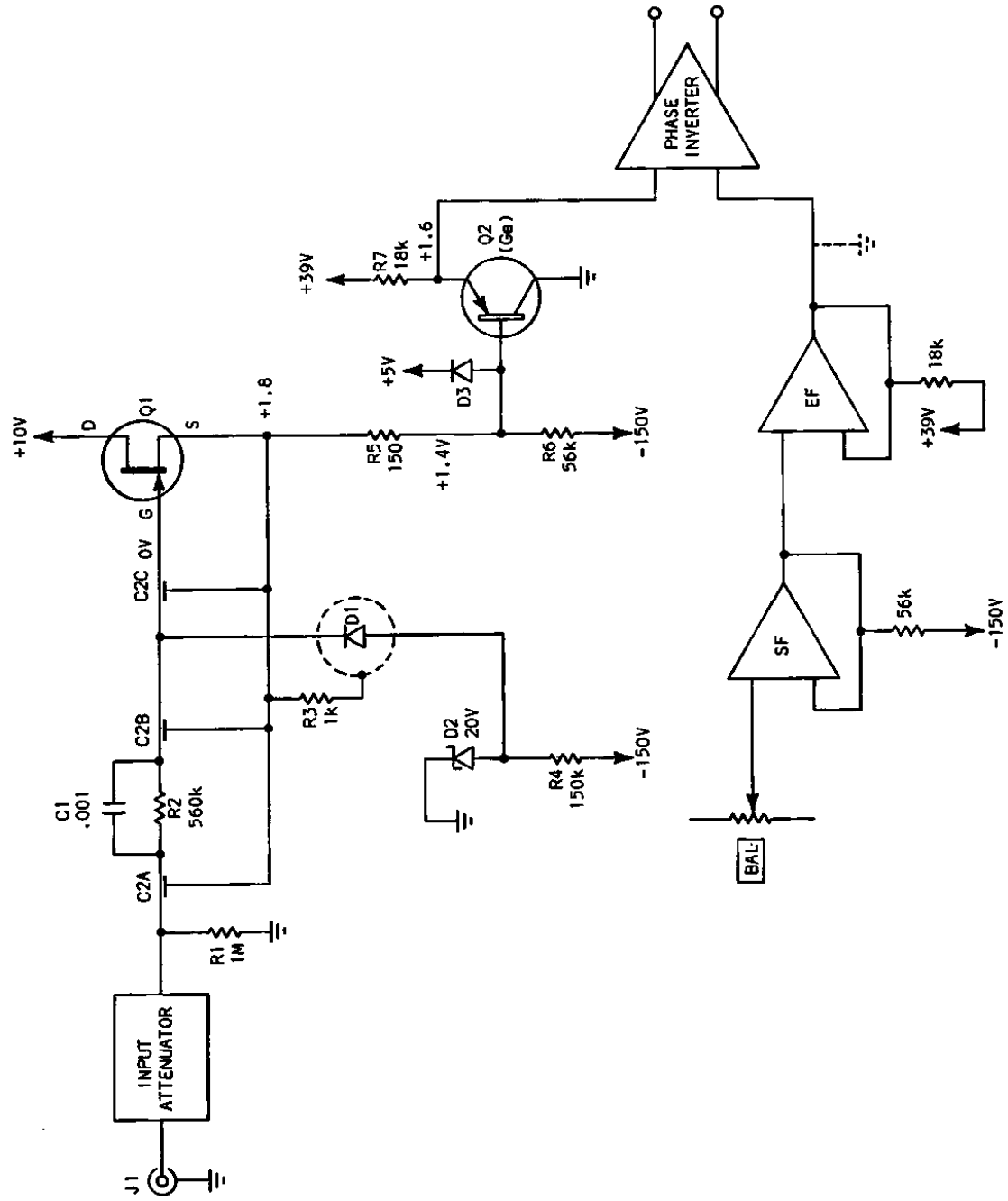


Fig. 3-99. Source follower replaces cathode follower as input amplifier.

Under condition 2, 5mA flow through R3 and R16 draws 5.4 mA.

Under condition 3, both resistors draw 5.4 mA.

If the current through R16 flowed as Q2 I_D, Q1 and Q2 R_0 would differ for conditions 1 and 2, but not 3. However, R14 and R15 shunt part of the longtail current so that Q2 I_D matches Q1 I_D.

4.5 mA is shunted with R14 set to +12 V, leaving about 1 mA to flow as Q2 I_D. Moving the wiper toward ground reduces shunt current which of course increases I_D for Q2. Zero-shunt-current demand occurs at some resistance value slightly above ground.

C11 with R15 decouple to prevent unwanted signals at the emitter-follower input.

input amp changed from CF to SF

Circuit complexity and high voltages usually identify amplifiers modified for source-follower instead of cathode-follower operation. This keepstotal amplifier modifications to a minimum. Fig. 3-99 is an example. Q1 and the BALANCE source follower replace cathode followers. Following circuits, including emitter-follower drive to the phase-inverter, remain unchanged.

R1 forms a portion of the input attenuator and returns the gate of Q1 to ground.

R2 is a limiting resistor, bypassed by Cl.

input capacitance stabilized and reduced

C2A, B and C are circuit-board strips circling connection terminals. This stabilizes the circuit-board dielectric, and returning C2 to the source, reduces input capacitance.

R3 ties the case of D1 to the source for the same reason -- stabilizes and reduces input capacitance. Capacitance from case to chip of D1 exists. Returning the case to a reference fixes the capacitance. And returning the case to the source reduces signal voltage across the device, thereby reducing capacitance.

protection

Protective circuit D1, D2 and R4 prevent gate-to-channel breakdown in Q1. Applying negative gate voltages which approach gate-to-drain breakdown (BV_{ss}) actuates this protective circuit. Zener diode D2 conducts through R4 to regulate the anode of D1 at -20 V. D1 clamps when gate voltage exceeds -20V.

Signal voltages develop across r_{ds}, R5 and R6. Because of resistive values most of the input voltage develops across R6 to appear at the base of Q2.

limiting

Positive voltage across R1, exceeding about 4 V, causes both gate-limiting and source-clamping. Clamping and limiting interact. Assume a fairly "slow" positive-going signal develops across R1: The signal appears at the gate and source of Q1. Q1 source follows the input ascension until the R5-R6 connection raises 3.2 volts above quiescence. D3 now turns on because of +5.6 anode volts and +5 cathode volts. D3 clamps the base of Q2 and the source of Q1. As Q1 gate voltage continues to rise, the gate-channel diode becomes forward-biased. Limiting current flows through D3, R5, the source-to-gate channel resistance, and R2. The drop across R2 limits gate current.

test-circuit loading

Notice that during excess voltage application input resistance decreases. The shunt across the circuit under test consists of R1 paralleled by R2, gate-source resistance, R5 and D3. For slow voltage changes R2 approximates the additional load.

balancing phase-inverter drive

The BALANCE source follower and emitter follower are the same type active devices, set to the same operating point as Q1 and Q2. Thus the phase-inverter drive is quiescently balanced. The input voltages and impedances equal at quiescence. Input signals appear at the phase-inverter terminal via Q2. The other phase-inverter terminal remains biased at the quiescent level; therefore is an *apparent* ground. There is an exception: Thermal (source-follower) signals appear at both input terminals. They are of equal amplitude and phase, therefore cancel. This is why active devices and circuit configurations match.

Fig. 3-100 shows the BALANCE circuit. Q4 longtailed by R8 divides Q3 output impedance β times, just as Q2 divides Q1 output impedance. R9 and R10 equal R5 and R6 in the source of Q1. These matched components allow one to adjust Q3 gate voltage for a quiescent center-screen display.

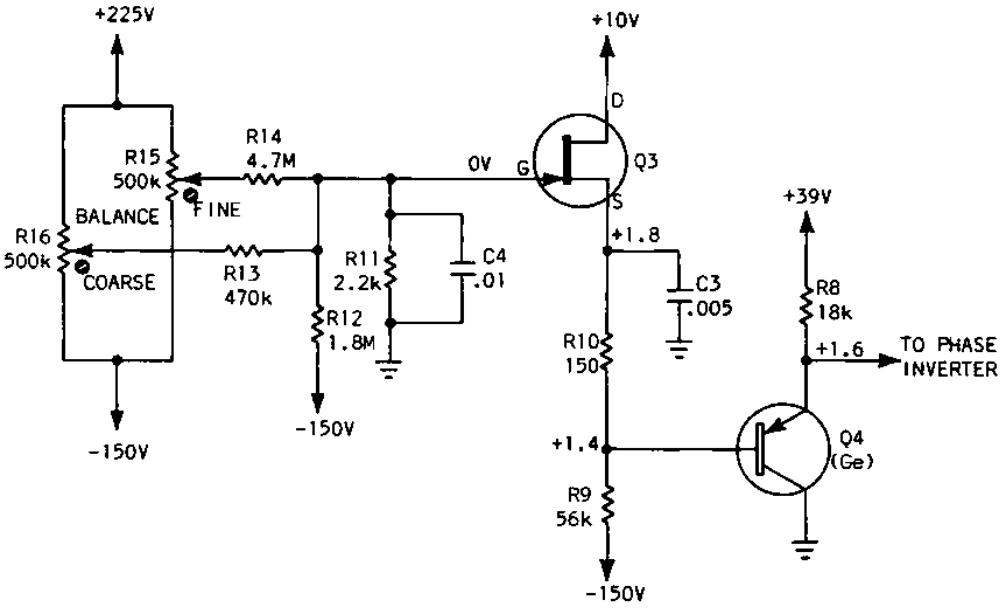


Fig. 3-100. Phase-inverter balance circuit.

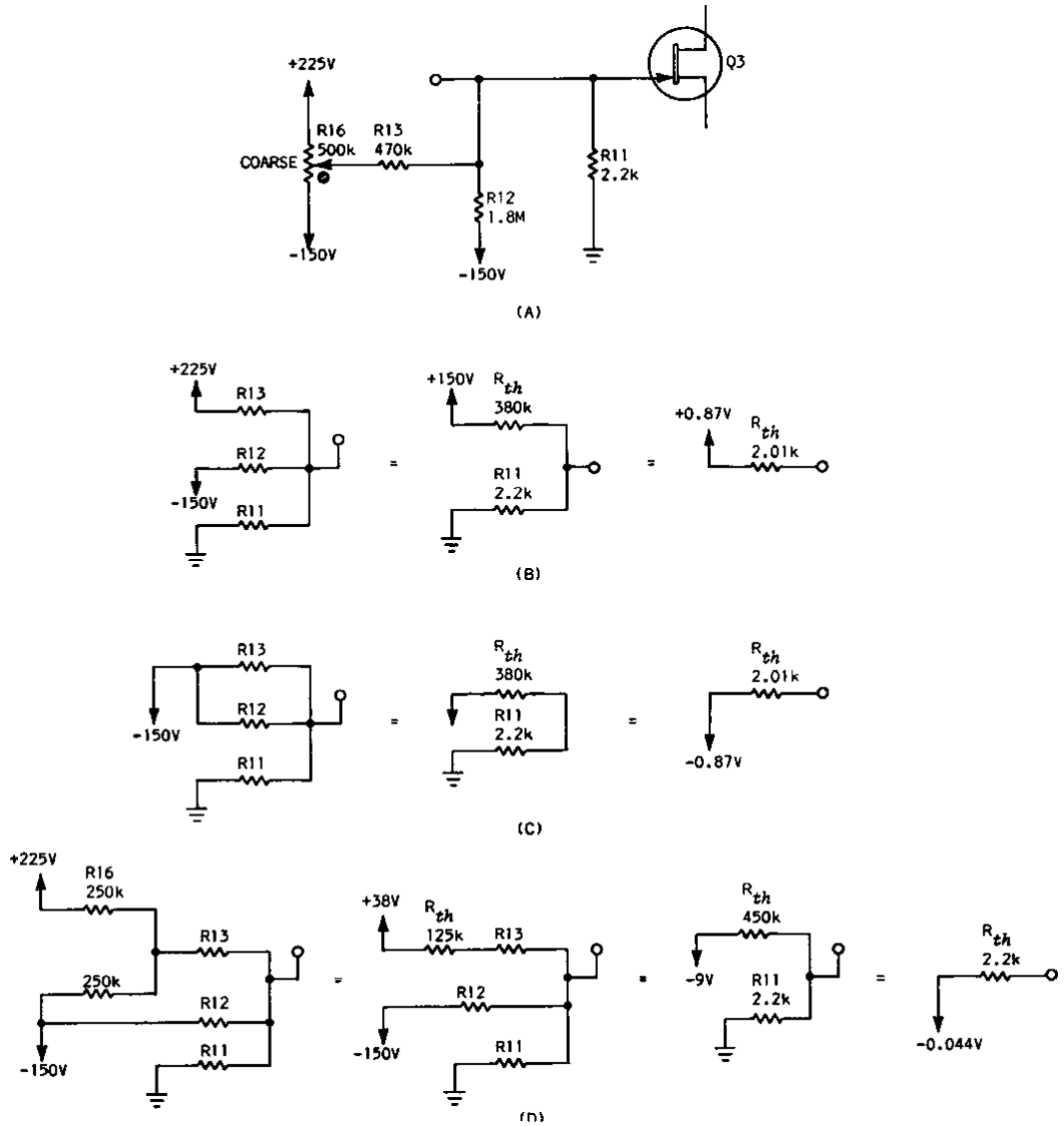


Fig. 3-101. Balance-adjust equivalent circuit.

C3 bypasses R_S to prevent switching transients from developing at the phase-inverter terminal. R11 and C4 filter transients in the gate circuit.

R11 in conjunction with R12, R13, R14, R15 and R16 establishes Q3 gate voltage. One sets this voltage for a "balanced" condition: A centered CRT vertical display at quiescence. To accomplish balancing, ground the vertical input jack, center the vertical POSITION control, and set R15 to mechanical center. Now adjust R16 for an approximately centered display; then set R15 for a display precisely centered.

Although gate supply voltages are quite high, adjusting R16 and R15 changes gate voltage in fairly small increments.

Fig. 3-101 develops the coarse BAL-adjust circuit equivalent including R11:

(A) is the circuit to be "Thevenized."

(B) shows that 2.01 kΩ returns to an equivalent +0.87 V with R16 set to +225 V.

(C) shows that setting R16 to -150 V develops an equivalent of 2.01 kΩ returned to -0.87 V.

(D) evolves the COARSE centered equivalent.

3-101A is the circuit to be "Thevenized."

3-101B shows that 2.01 kΩ returns to an equivalent +0.87 V with R16 set to +225 V.

3-101C shows that setting R16 to -150 V develops an equivalent of 2.01 kΩ returned to -0.87 V.

3-101D evolves the COARSE centered equivalent.

Now substitute the equivalent of Fig. 3-101D for R11 R12, R13 and R16 in the original circuit. This results in the Q3 gate circuit shown in Fig. 3-102A. Fig. 3-102B and C illustrate R15 extremes. Moving R15 from maximum positive to maximum negative changes Q3 gate voltage less than a volt. The fine BAL resistance is centered (Fig. 3-102D).

Centering both R15 and R16 creates the circuit shown in Fig. 3-102E. Gate voltage sets 2.5 millivolts below ground. Assume this is approximately zero volts, accounted for by part tolerances and computation errors. Further, small adjustments of R15 or R16, or both, zero the gate voltage.

input amplifier

The latter part of the emitter-follower section described an unusual emitter-follower configuration which resulted from a cathode follower to source-follower input-amplifier modification. Fig. 3-103 completes that input-amplifier schematic.

compensated voltage divider

Input DC voltages develop across R1, R2 and R3. C1 and C2 compensate this voltage divider for optimum pulse response. 98% of the input voltage develops at the gate of Q1A. R1 has negligible effect upon voltage division. It imposes losses between attenuator inductive components and C4 to prevent ringing.

limiting

C4 discharges stray capacitance, shunting R3, following gate limiting. R4 is the gate-limiting resistor. Because of such small gate current this circuit uses a large limiting resistance, R4.

test-circuit loading

Therefore, circuits under test which develop excessive voltages never work into a load greater than R3 paralleled by R4.

protection

D1 turns on, limiting negative voltages which exceed Q1A reverse-breakdown. When Q1A gate voltage becomes more than -12.6 volts, D1 turns on. D1 draws current through R1, R2, R4 and R6. This current added to that drawn by R3 loads the circuit under test.

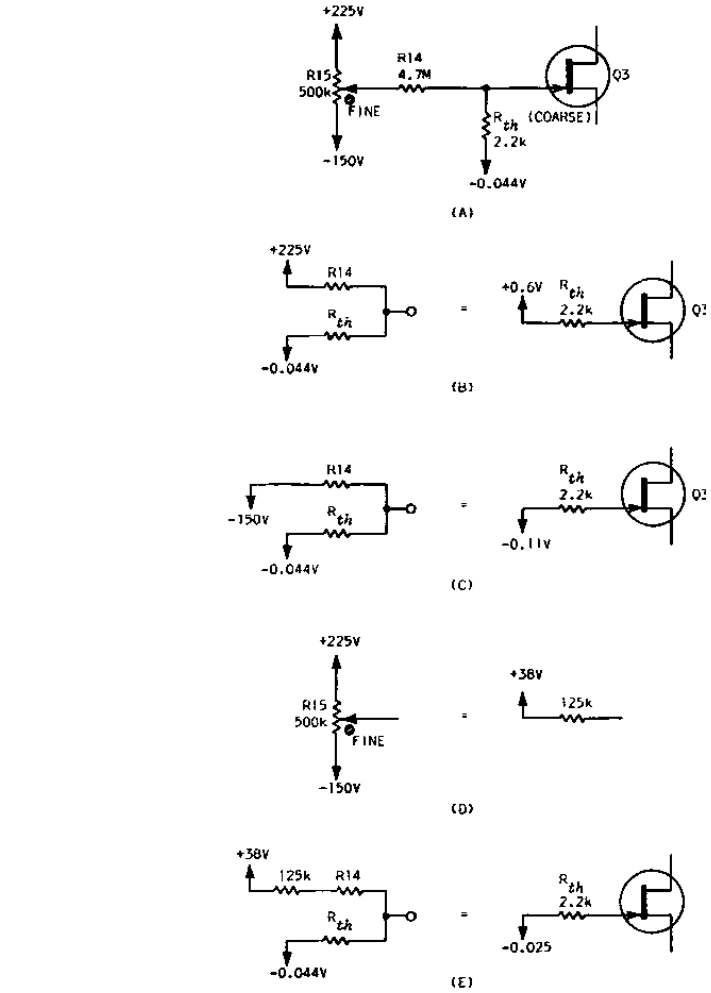


Fig. 3-102. Equivalent BALANCE circuits.

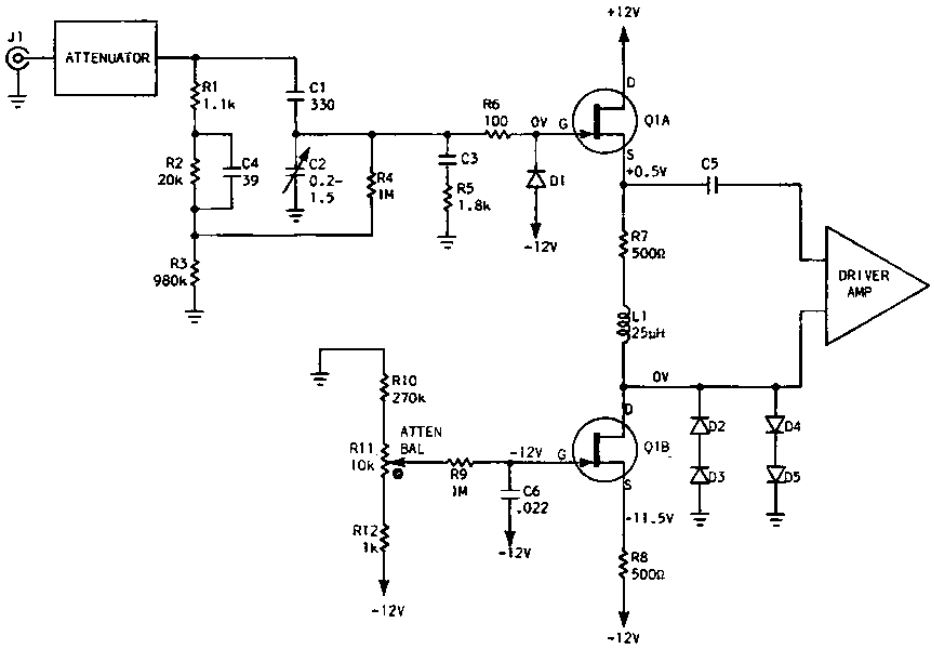


Fig. 3-103. Source-follower input-amplifier modification.

Positive-limiting initiates in the source of Q1A. When source voltage exceeds +1.2 V, D4 and D5 turn on, clamping the driver-amplifier input. Should Q1A gate voltage continue to ascend, the source-to-gate junction becomes forward-biased. Turning this diode on connects the input-limiting circuit to D4-D5 through R7.

L1 slows clamping action, either D4-D5 or D2-D3, during "fast" input voltages.

C1 discharges gate input capacitance upon removal of signal-voltage overloads, just as C4 discharges stray capacitance across R3.

C3 is circuit-board capacitance. Returning C3 to ground through R5 prevents "floating" capacitance. These components then provide negative-input-resistance compensation.

Negative-input-resistance characteristics receive two treatments: *Shunt RC* and a *suppressor.* R5-C3 shunt compensate and R6 is the suppressor.

thermal compensation

Q1 longtail configuration allows quiescent voltage to develop at the driver amplifier and Q1B connection, independent of temperature. One sets Q1B collector to zero quiescent volts. R8, Q1B, R7 and Q1A form a voltage divider between the -12 volt and the +12 volt supplies. If all divider impedances remain constant, Q1B drain voltage remains zero. This is the reason for using identical FET's in a common case: Q1 channel resistance changes with temperature. However, Q1B channel resistance always equals that of Q1A so voltage division remains constant.

Q1B drain voltage, or Q1A longtail current, results from the setting of ATTFN BAL, R11. R11 allows 0.5-volt adjustment at Q1B gate from about -12 to -11.5 volts.

Notice filter capacitor C6 returns to the -12 volt supply. This reduces the amplitude of any -12 volt power-supply fluctuations at the gate of Q1B. C6 also need have a small voltage rating since the source and gate return to the same supply.

Concepts presented in the follower series apply to amplifier concepts yet to be presented, and should be well understood before proceeding.

The following appendage is for those who work with Tektronix instruments and are unfamiliar with FET components.

Fig. 3-104 compares three-terminal active devices.

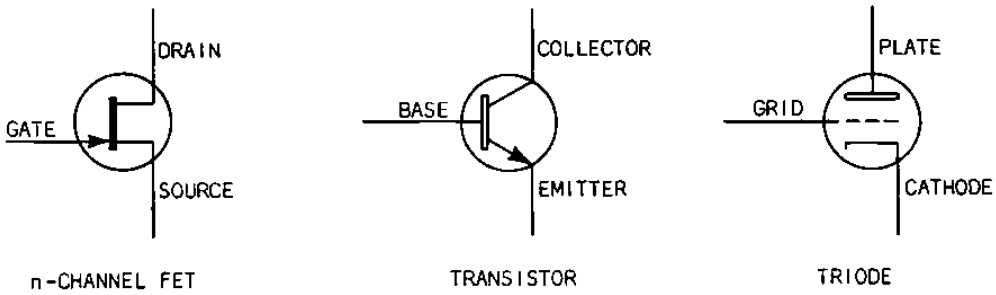


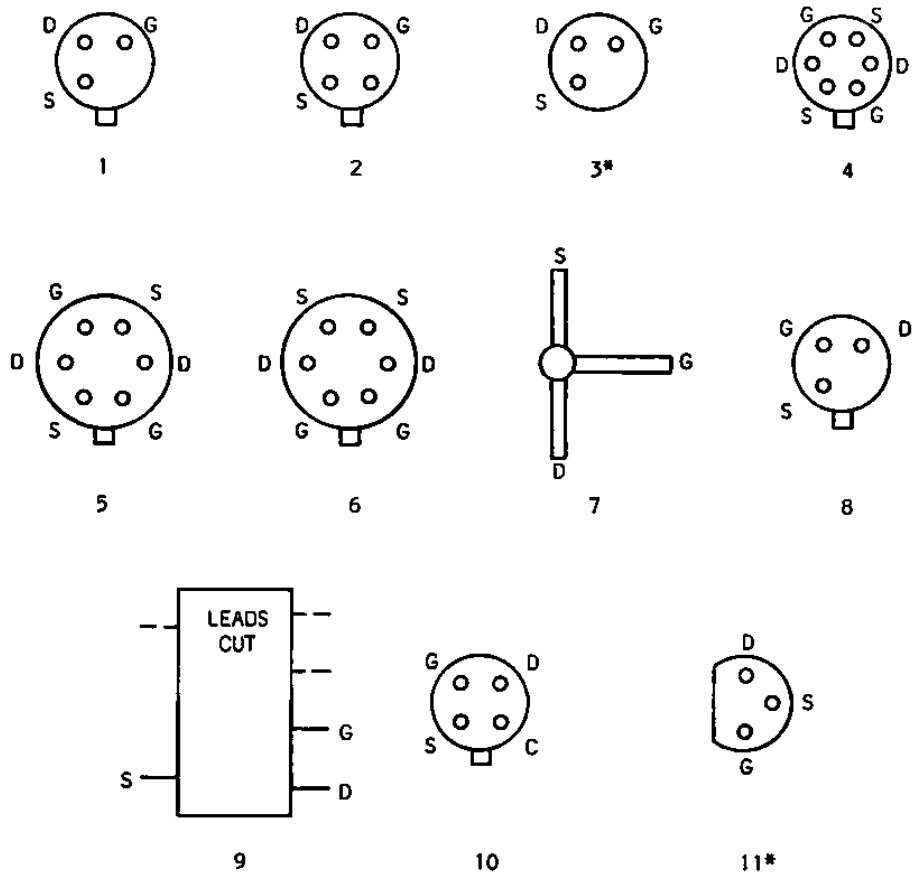
Fig. 3-104. Comparison of basic lead terminology of FET, transistor, and vacuum tube.

GROUP	TYPE	CHARACTERISTICS	HIGH-Z IN	LOW POWER CONSUMPTION	SMALL SIZE	LOW DRIFT	NOISE CHARACTERISTICS	SHORT WARM-UP TIME	SOLID-STATE RELIABILITY
PROBES	282	50Ω-TO-1MΩ ADAPTER	•	•	•	•			•
	P6045	DC-230MHz FET PROBE	•	•	•	•			•
	P6046	DC-100MHz FET DIFFERENTIAL PROBE	•	•	•	•			•
GENERAL PURPOSE PLUG-IN UNITS	1A1	DC-50MHz DUAL TRACE	•			•			•
	1A4	DC-50MHz FOUR TRACE	•			•			•
	1A5	DC-50MHz DIFFERENTIAL COMPARATOR	•			•			•
	1A7A	10μV/cm DIFFERENTIAL	•			•			•
	3A3	100μV/DIV DUAL DIFFERENTIAL	•			•			•
	81A	PLUG-IN ADAPTER	•						•
SPECTRUM ANALYZER PLUG-IN UNITS	1L5	50Hz-1MHz SPECTRUM ANALYZER	•			•			•
	3L5	50Hz-1MHz SPECTRUM ANALYZER	•			•			•
SAMPLING AND DIGITAL READOUT INSTRUMENTS	1S2	90ps TDR	•		•	•	•		•
	3S1	DUAL-TRACE SAMPLING	•		•	•	•		•
	3S2	DUAL-TRACE SAMPLING	•		•	•	•		•
	S1	350ps SAMPLING HEAD	•		•		•		•
	S2	50ps SAMPLING HEAD	•		•		•		•
	3S3	DUAL-TRACE SAMPLING PROBE	•		•	•	•		•
	3T2	RANDOM SAMPLING SWEEP	•		•	•	•		•
	230	DIGITAL READOUT	•						•
	568	READOUT OSCILLOSCOPE	•						•
PORTABLE INSTRUMENTS	323	DC-4MHz	•	•	•	•		•	•
	453	DUAL-TRACE 50MHz-SWEEP DELAY	•	•	•	•		•	•
MONITORS	410	PHYSIOLOGICAL MONITOR	•	•	•			•	•
TV INSTRUMENTS	520	VECTORSCOPE	•		•	•			•
DISPLAY UNITS	601	STORAGE DISPLAY UNIT	•						•
	602	DISPLAY UNIT	•						•
	611	STORAGE DISPLAY UNIT	•						•

Fig. 3-105. Tektronix FET utilization.

Fig. 3-105 lists major reasons for using FET circuits in production instruments.

Finally, Fig. 3-106 gives an FET basing diagram for Tektronix part-numbered FET's.



*PLASTIC
TO-18 -- 1,2,3,4,8,10,11
TO-5 -- 5,6
ALL DRAWINGS ARE BOTTOM VIEWS EXCEPT 9

TEKTRONIX PN	BASING NO	TEKTRONIX PN	BASING NO	TEKTRONIX PN	BASING NO
151-1001-00	9	151-1009-00	4	151-1018-00	10
151-1002-00	8	151-1010-00	4	151-1019-00	4
151-1003-00	4	151-1011-00	4	151-1020-00	4
151-1004-00	3	151-1012-00	2	151-1022-00	1
151-1005-00	3	151-1013-00	4	151-1024-00	10
151-1006-00	3	151-1015-00	2	151-1025-00	11
151-1007-00	4	151-1017-00	7	151-1026-00	3
151-1008-00	6				

Fig. 3-106. FET basing diagram.

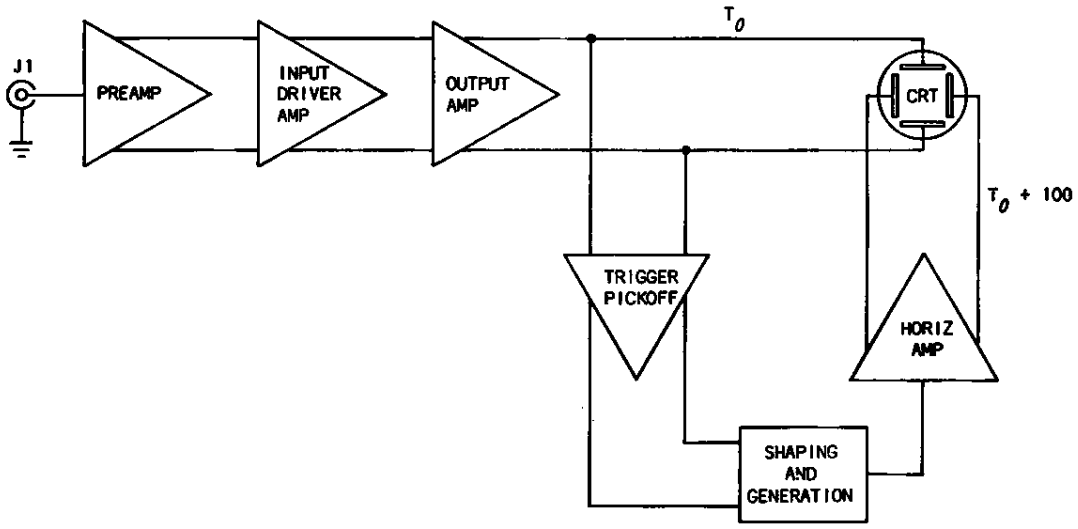


Fig. 4-1. Shaping and generation circuits add delay.

5 TRANSMISSION LINES

When one considers a transmission line as a means of conducting power between points, he may also consider any "black box" as a group of active devices cascaded with short transmission lines. This approach to electronics circuitry usually presents awkward problems for both writer and reader. On the other hand, a transmission-line approach gives the most direct and simple justification for some circuit components. Additionally, advantageous use of the transmission-line propagation velocity recurs again and again in vertical-amplifier design.

Power transits a transmission line at a rate determined by the type of line. This rate can be translated into time-per-unit length. Applying a signal simultaneously to short and long transmission lines of the same type, the signal out of the long line appears delayed in time from the signal out of the short line. Used in this fashion, the long transmission line is called a delay line.

delay line

THE USER MAY OBSERVE THE ENTIRE WAVEFORM THAT TRIGGERS THE HORIZONTAL SWEEP!

This is one function of vertical-amplifier delay lines.

delaying factors

A waveform will not travel from input jack to CRT in zero time. Each lead is a transmission line with a velocity factor and each amplifier requires time to act. Circuits that generate, shape or switch add the most delay.

See Fig. 4-1. Assume time zero occurs at the trigger pickoff point. At T_0 the vertical signal appears at the CRT and a portion of the signal feeds the trigger circuits. Switching, shaping, generation and amplification take place before the horizontal sweep begins. The first 80 nanoseconds of the waveform cannot be observed unless the user selects a horizontal sweep slow enough to display at least two waveforms.

Amplification takes time. Fig. 4-2 suggests an improvement by cutting the time differential. But the user still cannot observe the leading edge by selecting a sweep speed which displays only one waveform.

Inserting delay of the vertical signal between the trigger pickoff point and the CRT solves the problem. Fig. 4-3 shows vertical deflection occurring 100 nanoseconds *after* horizontal sweep start. A sweep speed may be selected that expands the presentation to include only the leading edge of the triggering waveform.

NOTE: 80-nanoseconds horizontal delay merely illustrates delay and may or may not be representative.

Delay lines appear most anywhere along the vertical signal path, but the *trigger pickoff* must *precede* the delay line.

Fig. 4-4 shows a line terminated at each end to minimize reflections. Oscilloscopes are voltage activated, so an advantage is sometimes gained by terminating only one end for maximum power transfer as in Fig. 4-5.

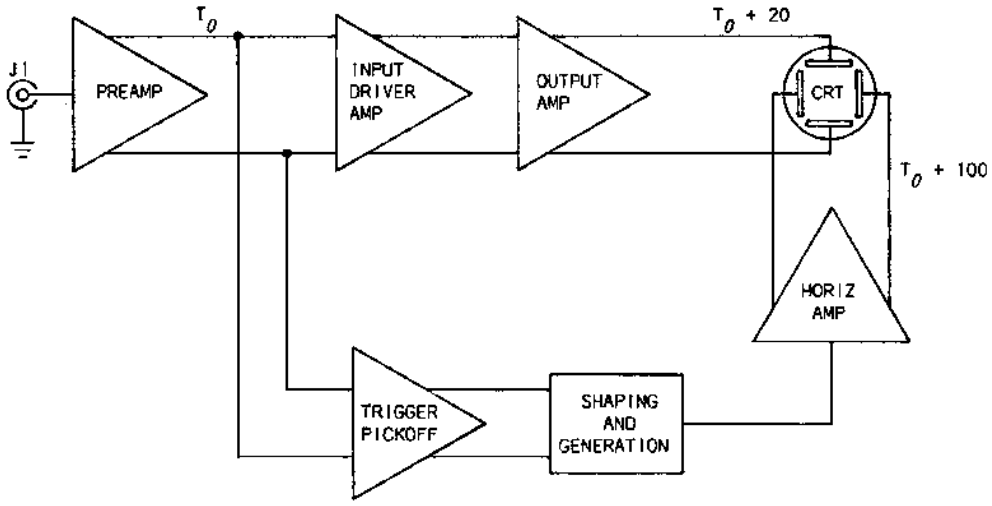


Fig. 4-2. Amplifiers impose less delay than shaping and generating circuits.

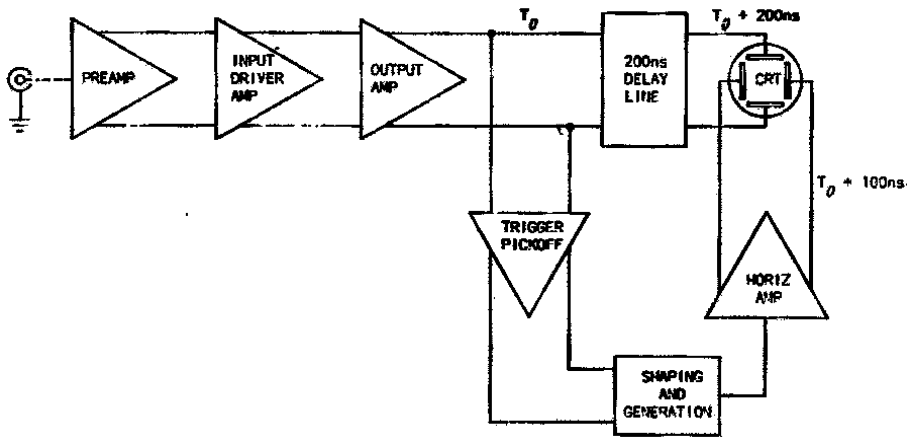


Fig. 4-3. Vertical signal delay allows horizontal sweep to initiate prior to vertical deflection.

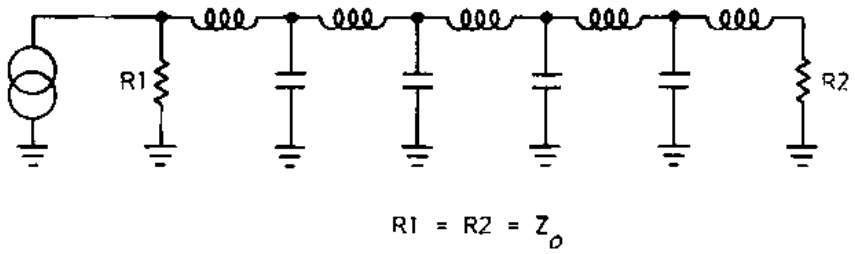


Fig. 4-4. Terminated transmission line.

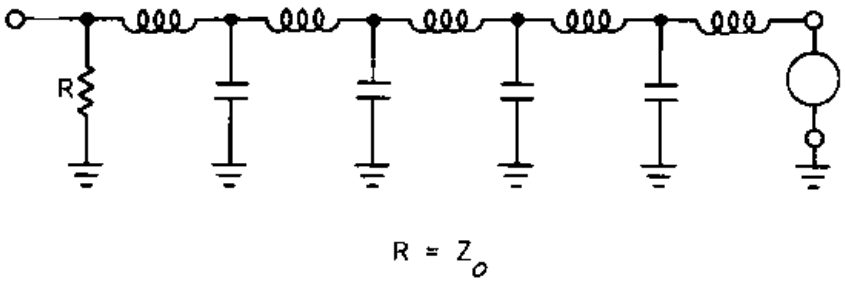


Fig. 4-5. Transmission line with single termination.

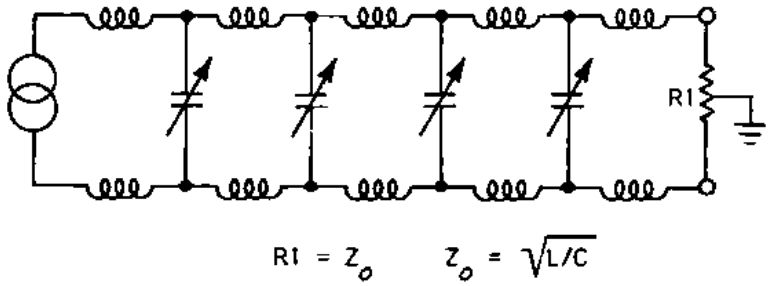


Fig. 4-6. An adjustable push-pull transmission line with single termination.

lumped-constant transmission lines

Delay lines are driven push-pull and lumped-constant transmission lines must have each section adjustable to be effective (Fig. 4-6). Lumped-constant transmission lines make delay lines of usable bulk which have high impedances (1000-2000Ω). This refers to the impedance across the line -- not from one side to ground.

There are disadvantages:

1. The time and skill necessary to adjust each section.
2. Lumped-parameter lines exhibit a bandpass which drops abruptly at F_c.

Not much can be done to reduce the adjustment chore. Optimum response requires precise proportioning of L, C and R components in each section. Further, the sections must match one another.

A lumped-parameter transmission line has a delay determined by values of L and C used. Changing either L or C changes line delay. For example: In both the horizontal and vertical amplifier of Fig. 4-7 a short lumped-parameter transmission line couples the driver-amplifier signal to the output amplifier. Capacitive components of both lines, made variable, gang for opposing effects. Maximizing C_V in the vertical, minimizes C_H in the horizontal. This gives a sort of teeter-totter time relationship between horizontal and vertical systems, allowing empirical phase adjustment. PHASING in this case is a front-panel control. The scope in Fig. 4-7 was designed for X-Y display. Transient response is not considered of primary importance and the line is short. This merely

illustrates the relationship of L and C in a basic lumped-parameter line.

The basic explanation of transmission-line components follows the premise that these networks simulate properly terminated smooth lines. This states that Z_0 remains constant over the frequency spectrum with no energy reflected. "Gaussian" response occurs only when velocity remains constant with frequency. Failure to maintain phase shift proportional to frequency ultimately distorts transient response. Transient response also suffers from any amplitude distortion as a function of frequency.

transient response distortion

Design of a lumped-parameter line represents the effort to make each section appear resistive over a broad frequency spectrum. The line-termination impedance should always match the Z_0 of the lines.

m-derived filters

Research in this area led to the development of m-derived filters. $\sqrt{\frac{1 - \omega_c^2}{\omega_\infty^2}}$ **establishes m where:**

$$\omega_c = 2\pi F_c = 1/\sqrt{LC}$$

$$\omega_\infty = 2\pi F_\infty$$

F_∞ = **angular frequency of peak attenuation.**

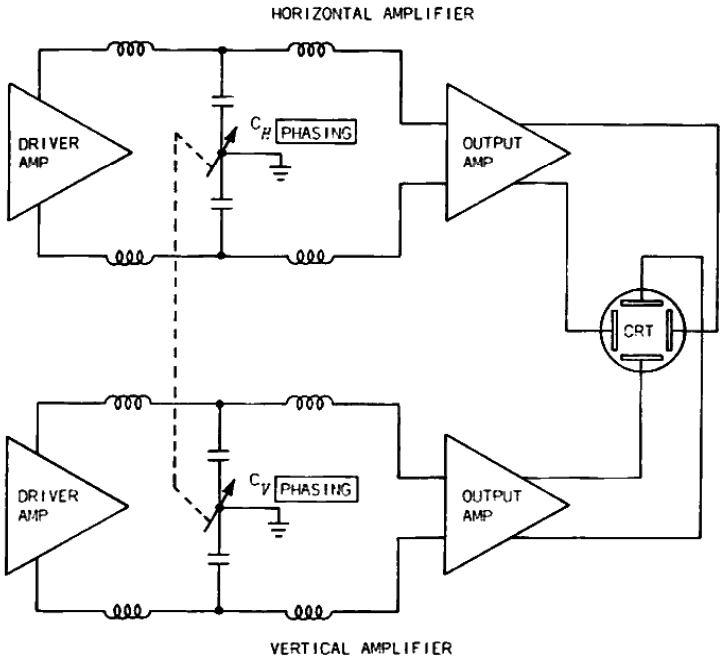


Fig. 4-7. X-Y phase adjustments.

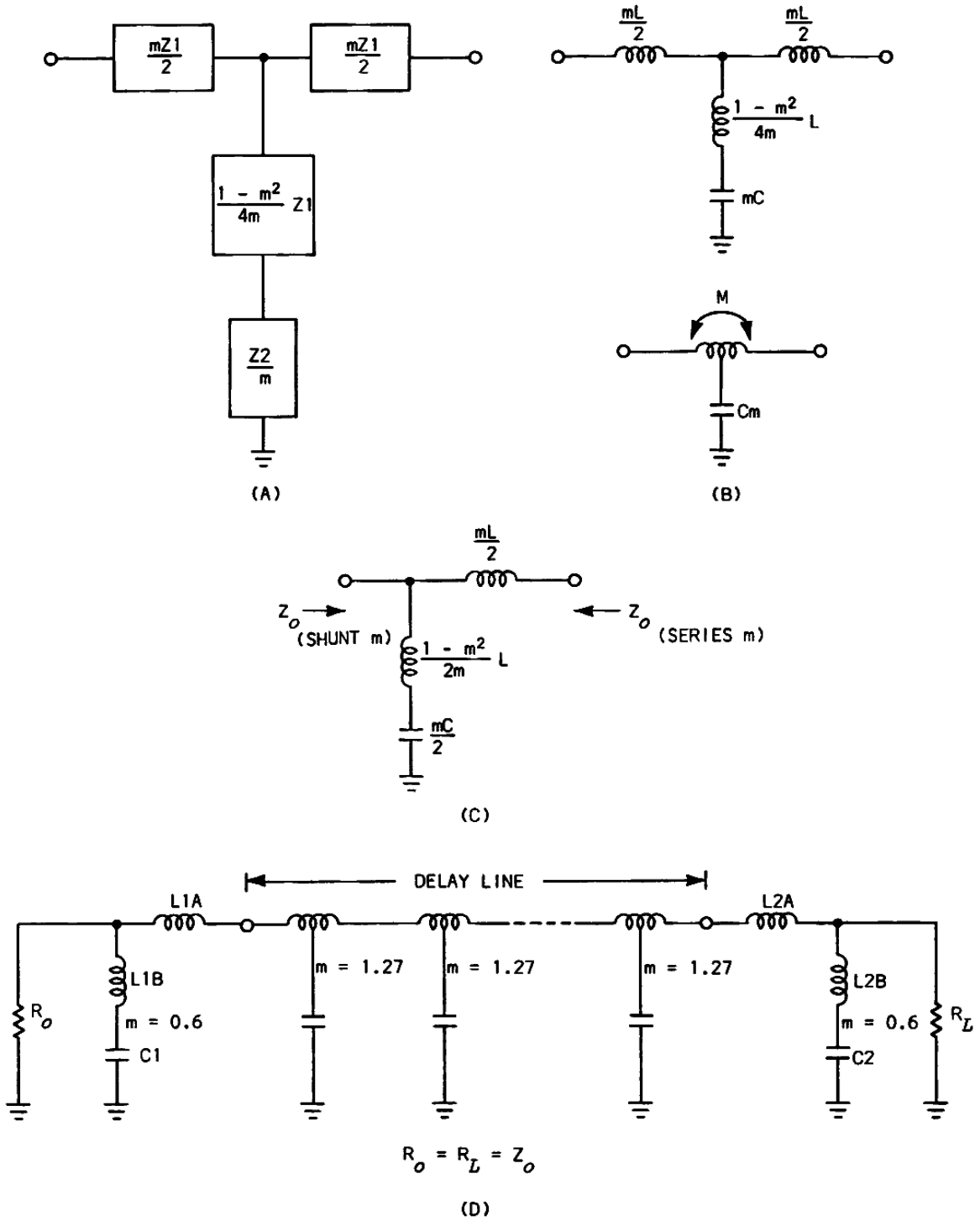


Fig. 4-8. Terminating a line consisting of m-derived sections with m-derived half sections.

reflections

Constructing lines from a chain or ladder of m-derived sections, terminated by an m-derived half section, virtually eliminates reflections as frequency varies. The sections may be constructed in either "T" or "π" configuration.

T-coil networks

Fig. 4-8 includes m-derived "T" models which receive treatment in a number of texts. Fig. 4-8A is the prototype model. The horizontal leg represents total series impedance and the vertical leg total shunt impedance. The counterpart appears in Fig. 4-8B. This circuit can be realized with a transformer having the proper amount of mutual inductance between series elements. Fig. 4-8B also contains the single-layer transformer which is the prototype equivalent. If one were to remove one-half of the series components and one-half of the shunt components, he would have an m-derived half section with exactly the characteristics of the original Fig. 4-8C.

Fig. 4-8D shows a delay line consisting of a ladder of m-derived sections terminated at either end by m-derived half sections. From a frequency standpoint, simple resistances, Ro and RL, complete the termination satisfactorily:

$$R^2 = (Z_{series\ m})(Z_{shunt\ m})$$

From either end, the line appears to consist of an infinite number of m-derived sections. This fails as a close approximation for transient response. Therefore, terminations include reactances. These elements must then be carefully adjusted for optimum observed step response.

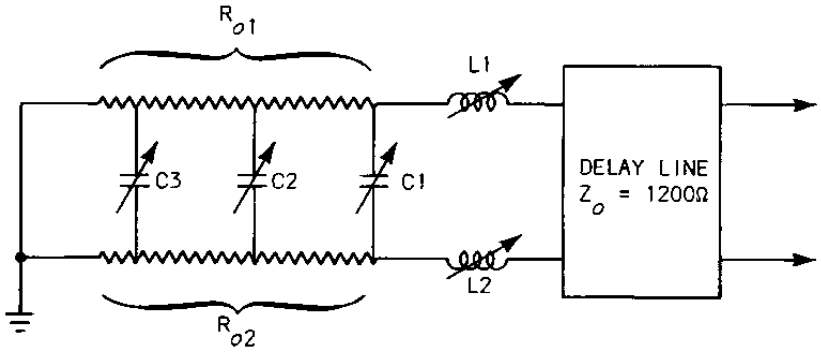


Fig. 4-9. Correcting for preshoot at the termination.

termination

When termination resistance (R_0) equals line surge impedance (Z_0), the line is properly terminated. Since Z_0 varies in a lumped-parameter line, R_0 must change with Z_0 to properly terminate. Fig. 4-9 shows such a termination. At the lowest frequency component of a step waveform, DC, the termination functions as a pure resistance equal to Z_0. AC waveforms cause the termination to become reactive. R_0 drops by the shunt value C2 and C3. Calibrating the reactances for optimum transient response creates an R_0 that varies with Z_0.

Ll, L2 and C1 represent m-derived half sections. One finds the m-derived structure used for delay lines, interstage coupling, and terminations. This is because the configuration offers a solution to the problem of delay variation with frequency. Proper selection of m creates the characteristic of constant group delay to quite high frequencies.

bridged T-coils

Bridged T-coils are an extension of m-derived sections. Under optimum conditions, a T-coil peaking network presents a constant resistance to an infinite number of frequencies. It also delays all frequencies linearly. A "perfect" transmission line presents a constant impedance to all frequencies. A T-coil peaking network is, therefore, one section of a lumped-parameter transmission line which simulates the smooth transmission line.

These circuits appear most frequently as amplifier output loads. This improves bandwidth over an RC-loaded amplifier developing the same gain. The formula. $1/2\pi RC$ represents RC-amplifier frequency

response. If input current remains constant, then output voltage varies with output *impedance.* Output voltage decreases to a 3-dB point when the output impedance decreases 30%. T-coil peaking extends the frequency at which the 3-dB point occurs.

T-coil peaking

With selected values a T-coil peaking circuit improves bandwidth by a factor of 2.74. Normally.

$$F_c = \frac{1}{2\pi RC}. \quad \text{With optimum T-coil peaking}$$
$$F_c = 2.74\left(\frac{1}{2\pi RC}\right) \text{ or } \frac{2.74}{2\pi RC}.$$

T-coils, as components, make up only a portion of a T-coil circuit. Selected values of capacitance and resistance, added to a basic T-coil, complete the circuit. See Fig. 4-10. Here a coil, wound for the proper amount of mutual coupling is tapped halfway down its inductive length. A number of electronic texts describe this coil under the title "m-Derived Filters." Adding load resistance and capacitance makes the circuit more complete (Fig. 4-11). R1 and C1 have a direct relationship to the total inductance of L1. Normally, R1 and C1 values are known before determination of L1 and one other dependent variable, a bridging capacitor. The bridging capacitance depends upon the value of C1 and the coupling coefficient of L1.

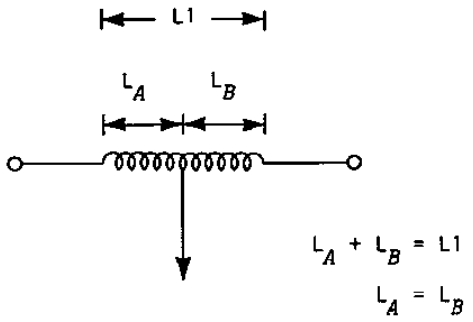


Fig. 4-10. Inductor tapped at electrical center.

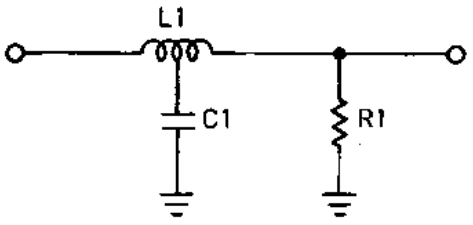


Fig. 4-11. Basic T-coil components.

Fig. 4-12 shows a completed T-coil circuit. With properly proportioned components, T-coil (L1), load capacitance (C1), load resistance (R1), and bridging capacitor (C2), the circuit defines an all-pass network. The impedance of the section equals R1 at all frequencies (ideal components).

series peaking

Useful bandwidth improvements between 2.6 and 2.8 result from application of T-coil techniques. Employing series peaking adds to the bandwidth improvement factor. See Fig. 4-13. Addition of L2-C3 improves bandwidth to a factor between 2.9 and 3.1. The LCR values must again properly proportion.

Circuit drive occurs at one of two points. Fig.4-13 shows input drive at the junction of L2-C3 and output voltage taken across C1. Fig. 4-14 illustrates the alternate method. Input drive at C1-L1 develops output voltage across C3.

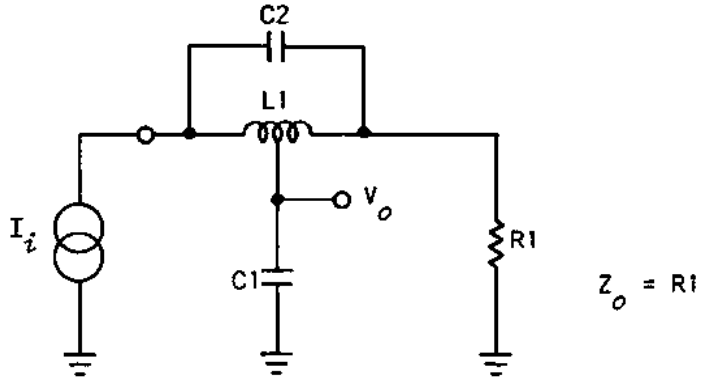


Fig. 4-12. T-coil circuit complete.

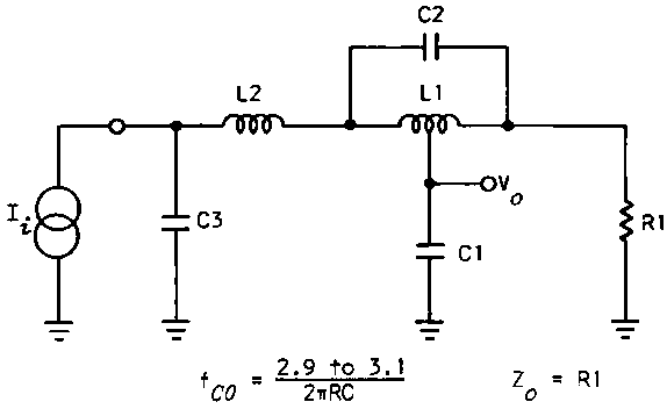


Fig. 4-13. T-coil with inductive peaking output taken across C1.

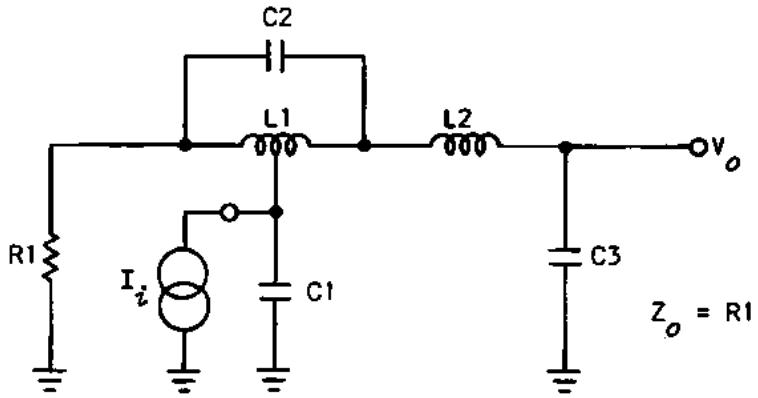


Fig. 4-14. T-coil with inductive peaking output taken across C3

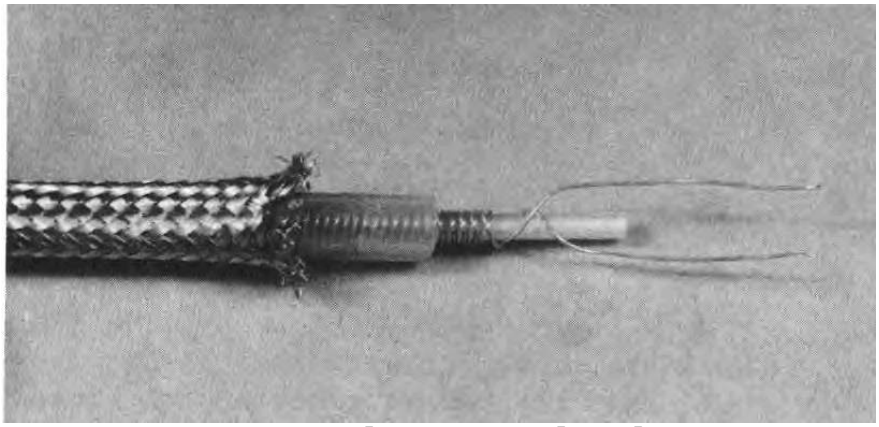


Fig. 4-15. Spiral-wound delay-line coax.

One encounters each of the circuits represented in Figs. 4-12, 4-13 and 4-14 in oscilloscope vertical amplifiers. The key to identification is coil configuration and resistance. Capacitances can be either components or distributed circuit capacitance. In any case, treat T-coil peaking as a transmission line terminated in its characteristic impedance.

coaxial delay lines

The transmission-line people didn't give up on coax delay lines. A superior delay line is manufactured using coaxial cable. The delay per foot has been increased by a factor of about 40, and the risetime characteristics improved. This cable is definitely ***not*** off-the-shelf or common coax.

The photo in Fig. 4-15 illustrates the method of spiral winding or braiding the two inner conductors in opposite directions about a common core.

Advantages include adjustment elimination, space and weight saving. Consider the following description: 140-nanosecond delay, 4.3-nanosecond risetime, 10-cubic-inch size and a fractional-pound weight! This is the package of Fig. 4-16.

Risetime does deteriorate with line length. Compare the approximate values listed below:

Delay Time	Risetime
140 ns	4.3 ns
170 ns	5.6 ns
195 ns	6.5 ns

Characteristic impedance is low, 93 Ω each side.

Oscilloscopes using vertical delay enable the operator to observe the leading edge of the waveform that triggers the horizontal sweep. Either a lumped-parameter or a fixed-tuned delay line may be used. If a fixed-tuned delay line is used it will be made of special coax and have a lower impedance than the lumped parameter.

Delay lines also function to establish phase coherence between parallel signal paths.

Unfortunately, no vertical-amplifier transmission line meets all requirements of impedance and phase. Several of the unfamiliar vertical circuits are attempts to optimize the balance between amplitude and phase distortion for better transient response. Applying a complex waveform of known dimension as an input signal and observing the waveform dimension at the output, evaluates a vertical system.

evaluating vertical systems

Fig. 4-17 illustrates the use of a step waveform for vertical evaluation. Fig. 4-17A shows the unobtainable perfect system. A "perfect" step input results in a "perfect" step output.

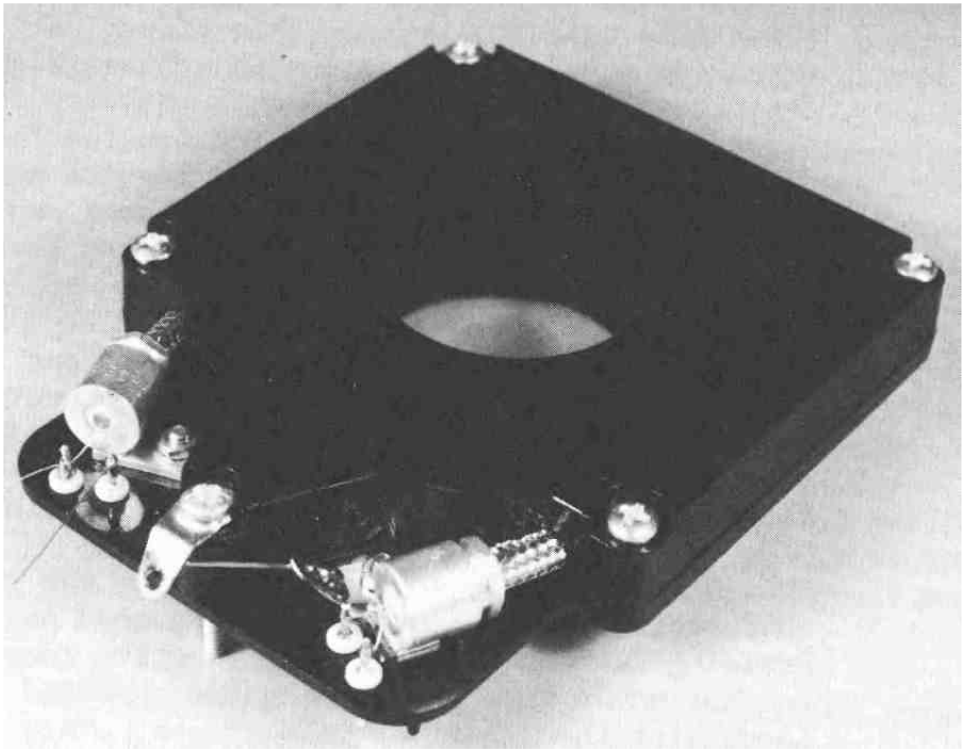


Fig. 4-16. Coax delay-line package.

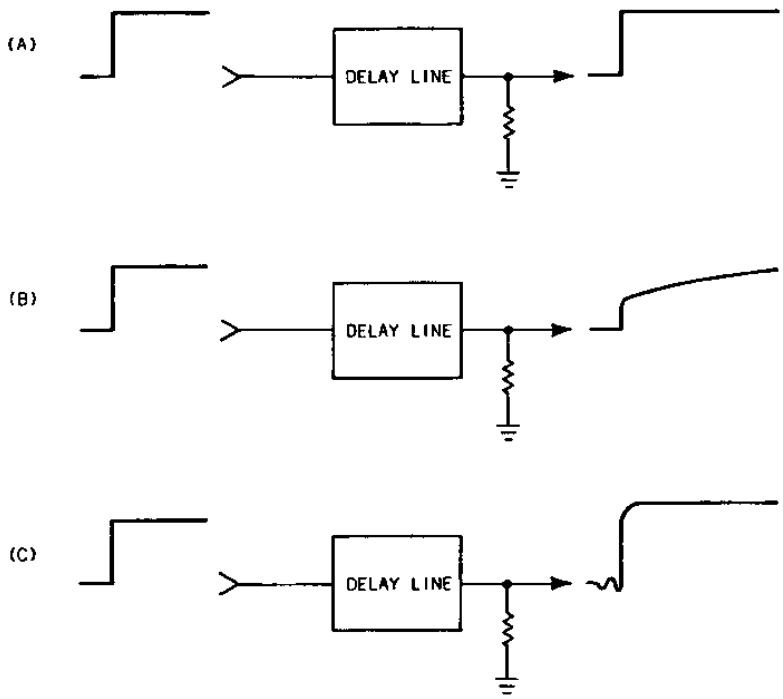


Fig. 4-17. Delay-line step response.

dribble-up

Fig. 4-17B represents a result known as "dribble-up." This is amplitude distortion. A "perfect" step drives the circuit. The resultant waveform steps a small amount then takes considerable time to reach full peak amplitude. Skin-effect, a transmission-line characteristic, causes high frequencies to be attenuated more than low frequencies. Rather than compensate at the termination for dribble-up, most vertical systems restore waveshape by following stage amplification. These amplifiers boost high frequencies and attenuate the lows to achieve overall system response.

Dribble-up is characteristic of coaxial and balanced shielded transmission lines. Naturally, the effect becomes more pronounced as line length increases. Therefore, delay lines constructed with either of these cable types impose dribble-up.

This does not apply to "special" coax, the inner conductors of which consist of a braided pair. Braiding introduces additional reactive components to what would have been a balanced shielded cable, increasing the delay per unit length. This "special" line imposes a velocity problem common to lumped-parameter transmission lines called

preshoot

"preshoot."

Fig. 4-17C presents this distortion. The name is derived from the illusion that the output circuit appears to anticipate energy arrival. Early arrival and algebraic summing of higher-frequency components cause preshoot. Higher-frequency components of the "perfect" step transit the line at a greater velocity than lower-frequency components.

The lumped-parameter line distorts because of sharp cutoff frequency (F_C), a characteristic smooth lines do not present. Networks constructed of L and C component sections in a chain or ladder pass frequencies below, but not above, F_C. F_C sets the point of abrupt change in phase velocity and Z_0. Variations of Z_0 start considerably below F_C. Equations for Z_0 and velocity appropriate for smooth lines also apply to lumped networks only at frequencies far below F_C.

T-coil use as delay-line termination helps eliminate preshoot. Fast-rise instruments which use the "special" coax delay lines develop preshoot as well as dribble-up. Amplifier boost or attenuation circuits correct dribble-up. Preshoot, however, results from unequal group delay which should be corrected as early as possible. Fig. 4-18 shows T-coil peaking applied to the line termination. Here three cascaded T-coil sections present an all-pass constant-resistance load. The 93-g terminating resistors are a part of the main vertical amplifier. None of the "T" networks attenuate an input signal. However, each section has an upper-frequency point, determined by part values, where signal delay occurs. Selection of component values causes section three to add delay to the lowest frequency component responsible for preshoot. Higher-frequency components encounter additional delay by sections two and three. All three sections delay the highest frequency components passed by the vertical delay line.

Inductors L1 through L4 and capacitors C1 through C6 correct for phase shift and cause the terminating impedance to equal Z_0 at all frequencies.

resolving terminations

Complex terminations are not difficult to identify because of proximity to the delay line. When analyzing a circuit consider these terminations as merely extensions of the delay transmission line. Resistors, equal in value to nominal Z_0, usually

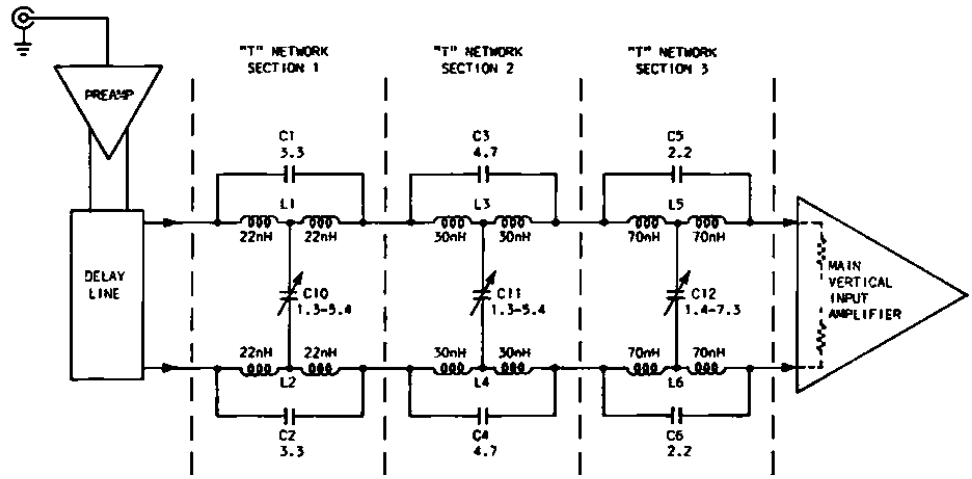


Fig. 4-18. Bridged T-coil compensation of the delay-line termination.

return the reactive termination to signal ground. Then Fig. 4-18 is a transmission line terminated in its characteristic impedance of 186 Ω (two 93-Ω resistors in the main vertical block).

Sometimes the resistive termination is not obvious. If one wishes to resolve the nominal termination impedance he still considers the DC resistance only. Fig. 4-19 illustrates a main vertical input amplifier driven, push-pull, by a preamplifier via the delay line. The main vertical input amplifier consists of an emitter follower with a complex input network for delay-line compensation and vertical-gain adjustment.

Typical push-pull drive is 100 millivolts per division. R11, common to push-pull current, functions as a bypassed resistor. 5 Ω approximates output impedance. R9-R10 are large compared to output impedance, so gain approaches unity.

Quite complex circuitry exists at the bases. All of the LCR network compensates and terminates the delay line. Termination for the delay line should match its characteristic impedance. Characteristic impedance for this delay line from one center conductor to the other is 186 Ω or from each center conductor to virtual ground, 93 Ω.

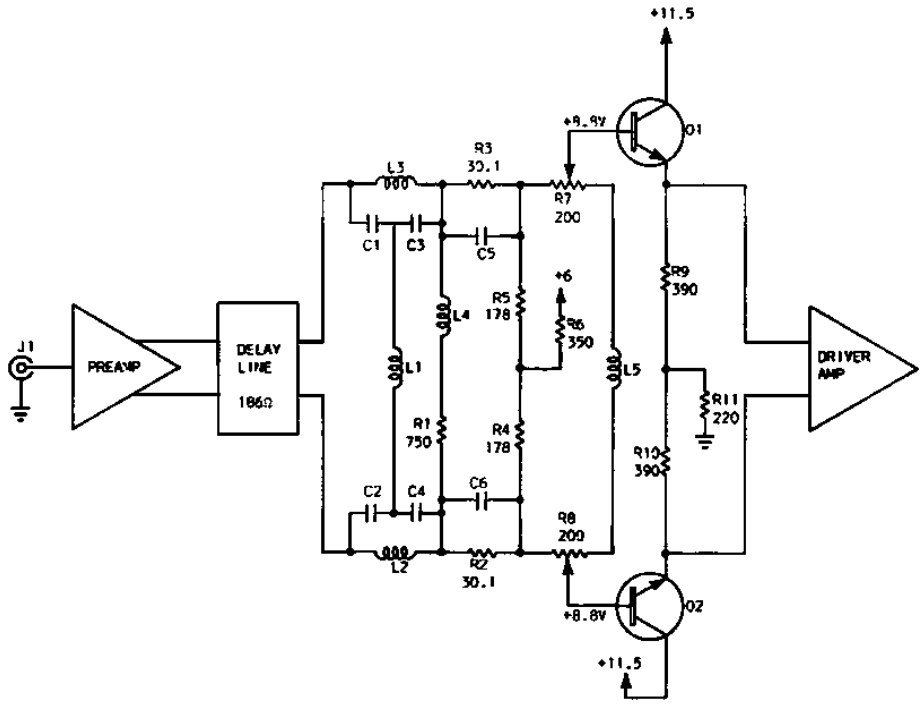


Fig. 4-19. Main vertical input amplifier.

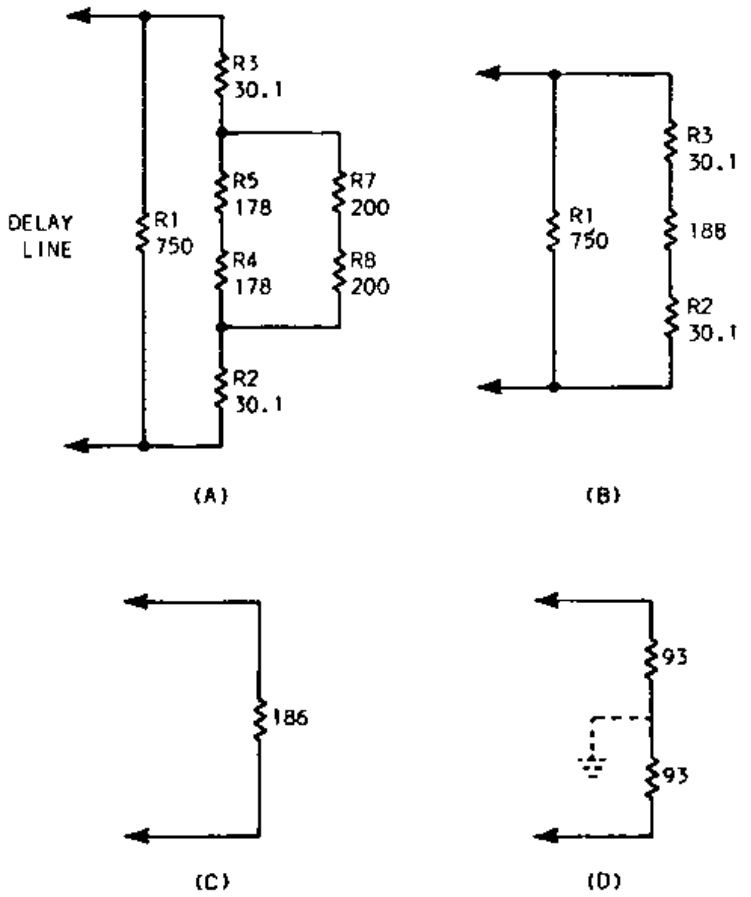


Fig. 4-20. Base circuit resistance of 4-19 equal to delay line Z_0.

R7 and R8, ganged, allow adjustment of vertical gain or deflection factor. Notice that these controls are not in the DC-current path. Adjustment at quiescence does not cause a vertical shift at the CRT.

R1 through R8, less R6, terminate resistively. R6 is a series dropping resistor for the preceding push-pull stage, thus the junction of R4-R5 becomes a common mode or virtual ground point. Fig. 4-20 step-by-step simplifies the resistive network. DC resistance matches the transmission-line surge impedance (Z_0).

interstage coupling T-coils

T-coils as interstage coupling networks should be treated as short sections of transmission line, terminated in Z_0.

Fig. 4-21 shows a series-peaked T-coil in the plate of V30. T-coil components consist of R35, L30, T31, L40 distributed and stray capacitance. Adjusting L30 proportions T-coil components.

The plate load for V30 is 1 kΩ. Assume the plate load consists of a transmission line terminated by a resistance (R35) equal to Z_0. Assume further that, with L30 properly set, Z_0 remains constant and resistive over the circuit bandwidth.

One adjusts L30 for optimum step response as seen on the CRT.

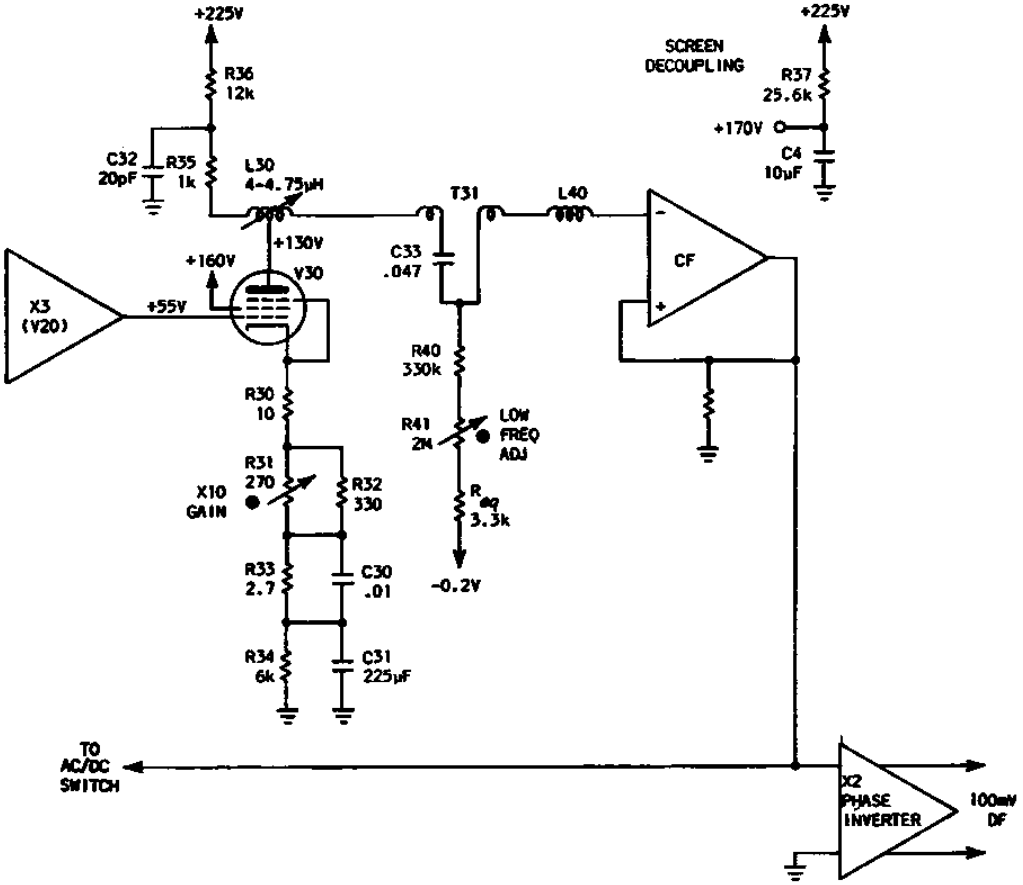


Fig. 4-21. Combination T-coil plate load.

T-coil drive occurs at one end of the coil as well as at the center tap. The impedance, Z_0, equals the terminator resistance. See Fig. 4-22. V2 drives a plate load of 1.2 kΩ (R2). Capacitances involved are V2 plate capacitance, shunt capacitance at the Driver input terminal, and L1 distributed capacitance. One empirically adjusts L1 for optimum LCR proportioning.

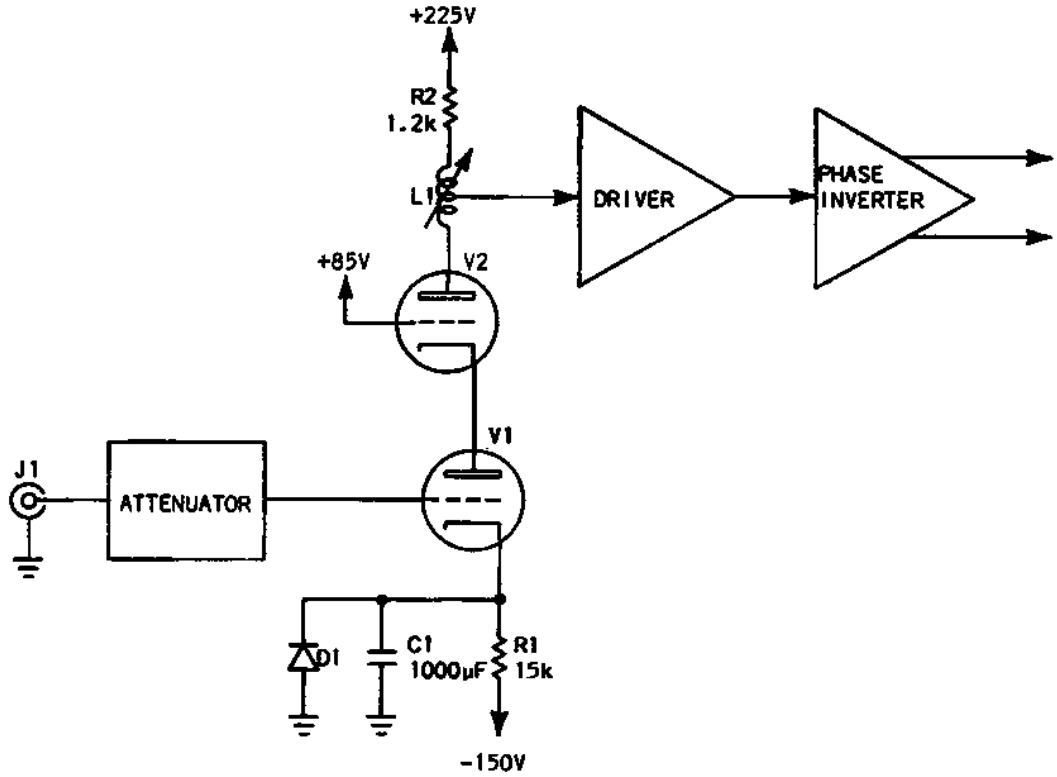


Fig. 4-22. Alternate T-coil connection.