

Integrated Circuits

Package Information

Tape and Reel Information

A separate 'Tape and Reel' document is also available from the CML website

Latest changes to this document - June 2011

Packages Q6 and Q7 added to packages portfolio.

CML Microcircuits Package Information

Legend

Cerdip

ceramic dual-in-line

CLCC

ceramic leaded chip carrier

DIL

dual-in-line

LQFP

low-profile quad flat pack

PDIP

plastic dual-in-line

PLCC

plastic leaded chip carrier

SSOP

shrunk small-outline package

SOIC

small-outline integrated circuit

TQFP

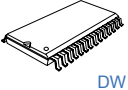

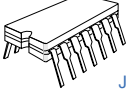
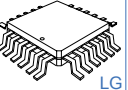
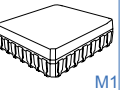
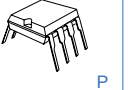
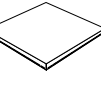
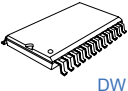
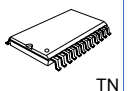
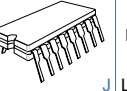


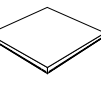
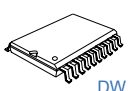
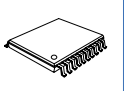



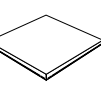
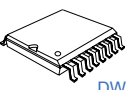
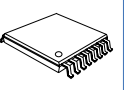
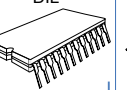
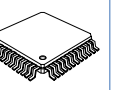

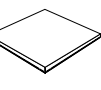
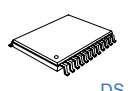
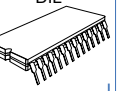
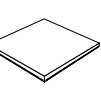
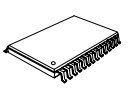

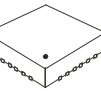
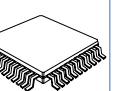
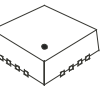
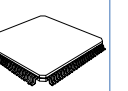

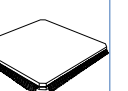
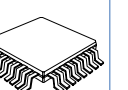
thin quad flat pack

TSSOP

thin shrunk small-outline package

VQFN

very-thin quad flat pack

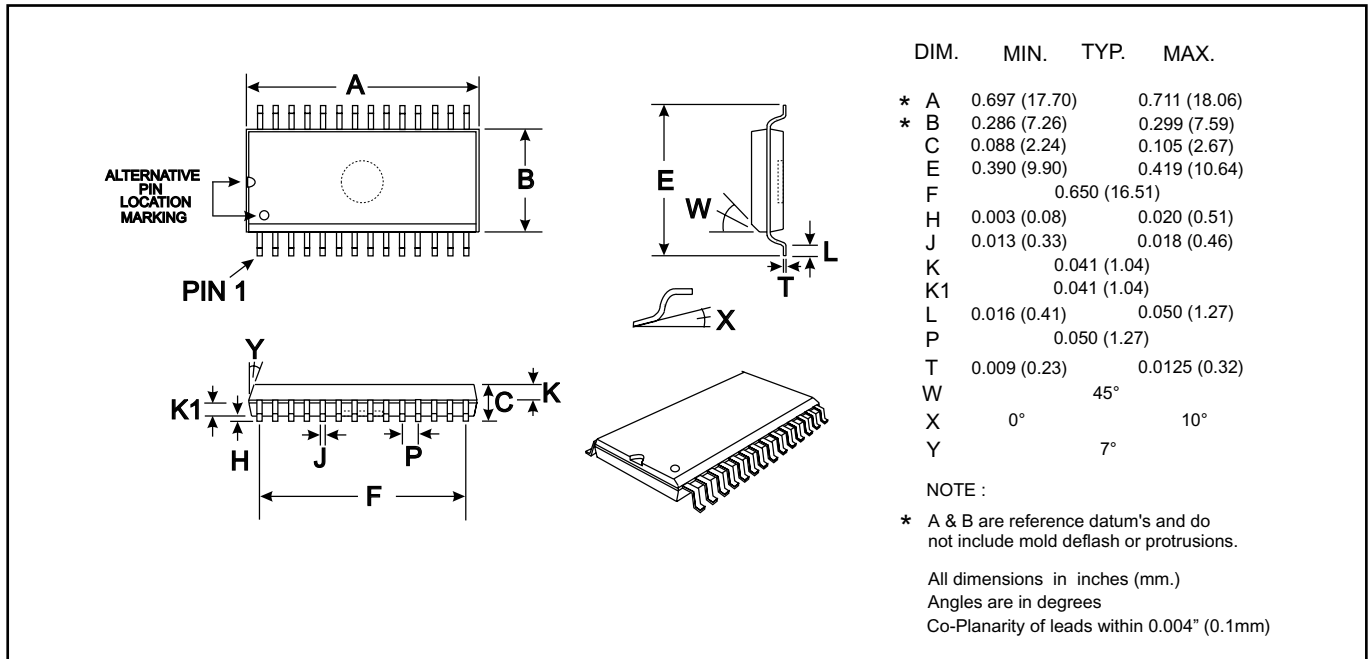
	D	E	J	L	M	P	Q
1	28-pin SOIC  DW	28-pin TSSOP 	14-pin cerdip DIL  J	24-pin PLCC  LG	28-pin ceramic CLCC  M1	8-pin PDIP  P	64-pin VQFN 
2	24-pin SOIC  DW	24-pin TSSOP  TN	16-pin cerdip DIL  J	24-pin PLCC  LH LS		14-pin PDIP  P	56-pin VQFN 
3	20-pin SOIC  DW	20-pin TSSOP 	22-pin cerdip DIL  J	28-pin PLCC  LH 8 LH		16-pin PDIP  P	48-pin VQFN 
4	16-pin SOIC  DW	16-pin TSSOP 	24-pin cerdip DIL  J	48-pin LQFP 		24-pin PDIP  P	40-pin VQFN 
5	24-pin SSOP  DS		28-pin cerdip DIL  J				32-pin VQFN 
6	28-pin SSOP 			44-pin PLCC 			24-pin VQFN 
7				44-pin LQFP 			16-pin VQFN 
8				100-pin LQFP 			
9				64-pin LQFP 			
10				144-pin LQFP 			
11				32-pin TQFP 			

Note: For the purposes of this document, the physical IC connection descriptions of 'lead', 'leadless' and 'pin', etc. are represented by the single term of 'pin'.

CML Microcircuits Package Information

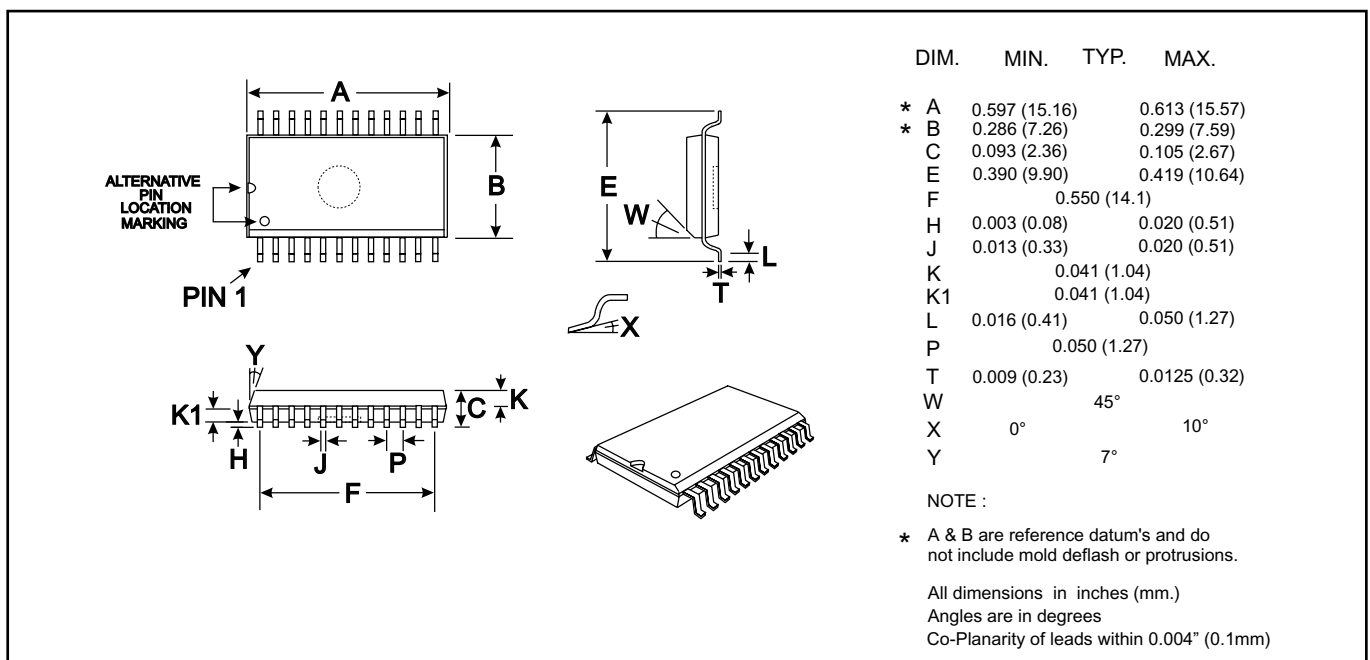
28-Pin SOIC, DW

(D1)



24-Pin SOIC, DW

(D2)



CML Microcircuits Package Information

20-Pin SOIC, DW

(D3)

DIM.	MIN.	TYP.	MAX.
* A	0.495 (12.57)		0.510 (12.95)
* B	0.286 (7.26)		0.299 (7.59)
C	0.088 (2.24)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
F		0.450 (11.43)	
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
K1		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X		0°	10°
Y		7°	

NOTE :

- * A & B are reference datum's and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
 Angles are in degrees
 Co-Planarity of leads within 0.004" (0.1mm)

16-Pin SOIC, DW

(D4)

DIM.	MIN.	TYP.	MAX.
* A	0.395 (10.03)		0.413 (10.49)
* B	0.286 (7.26)		0.299 (7.59)
C	0.088 (2.24)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
F		0.350 (8.89)	
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
K1		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X		0°	10°
Y		7°	

NOTE :

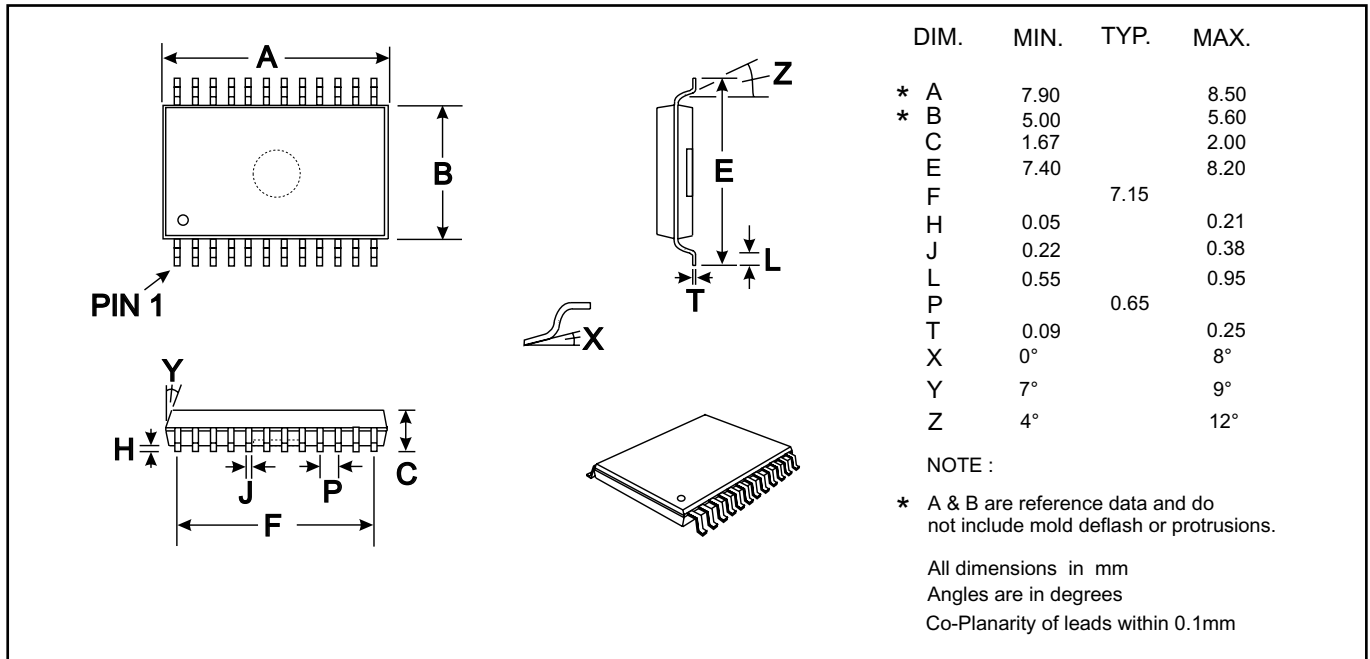
- * A & B are reference datum's and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
 Angles are in degrees
 Co-Planarity of leads within 0.004" (0.1mm)

CML Microcircuits Package Information

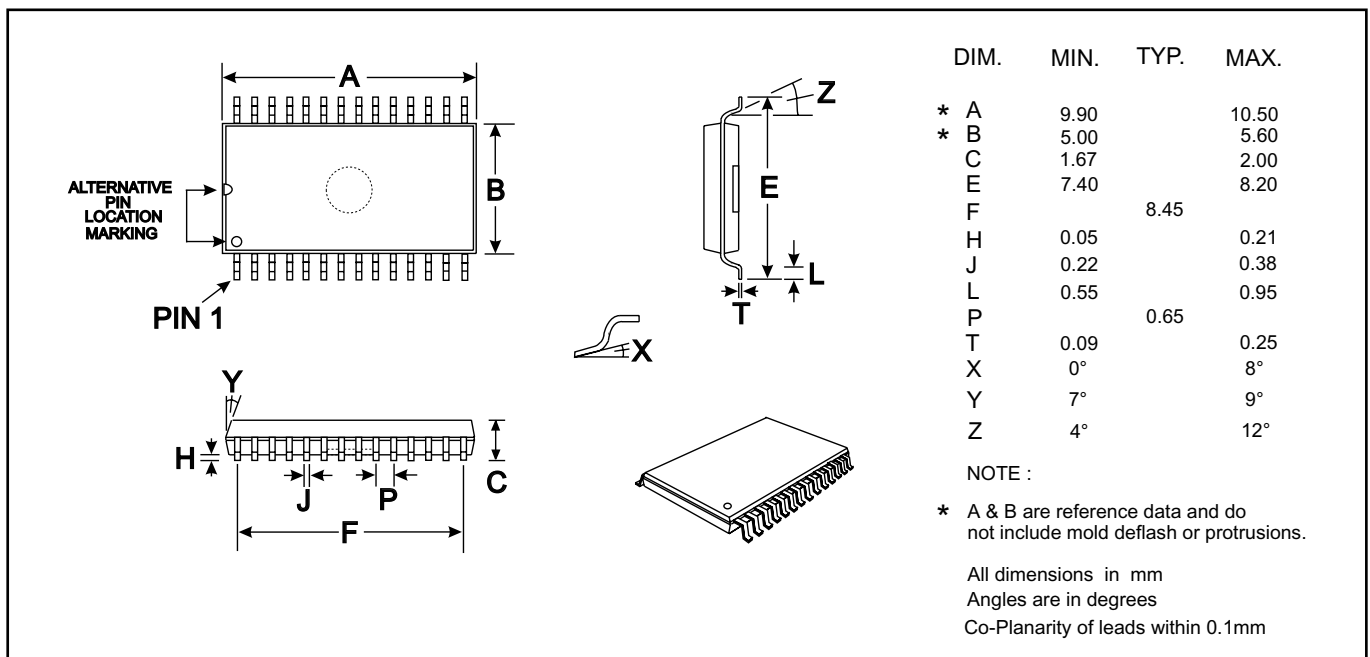
24-Pin SSOP (D5)

(D5)



28-Pin SSOP (D6)

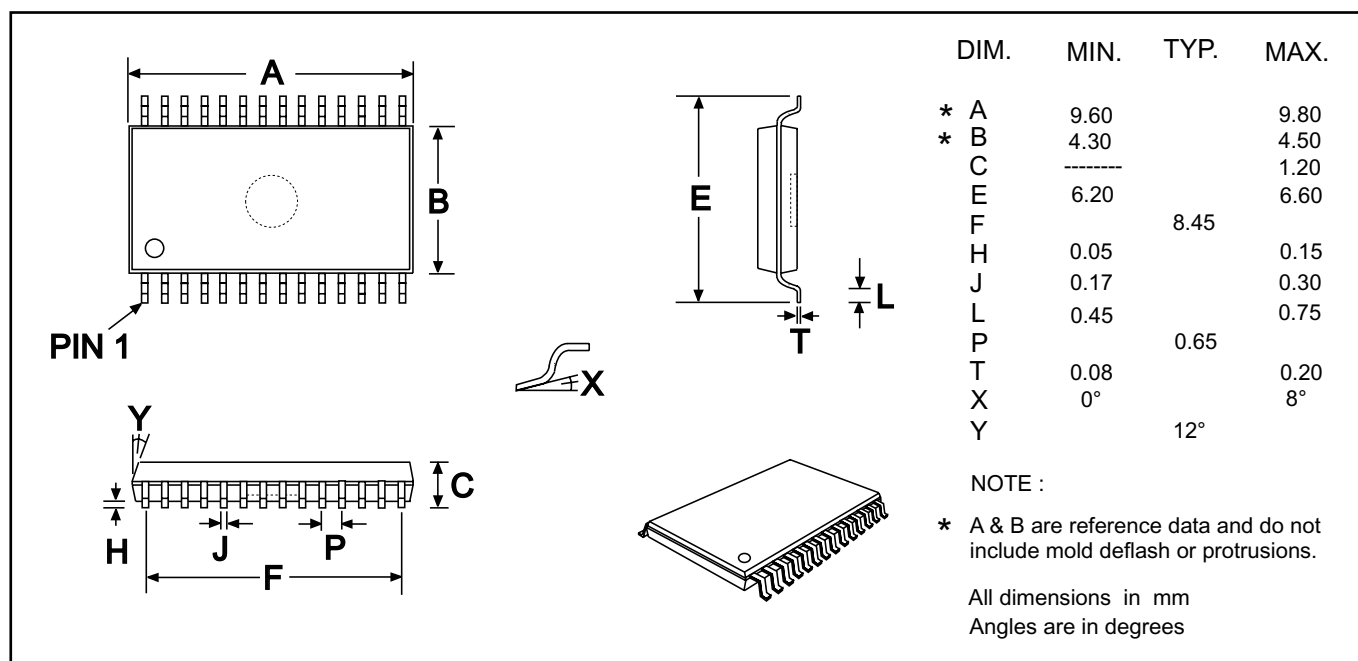
(D6)



CML Microcircuits Package Information

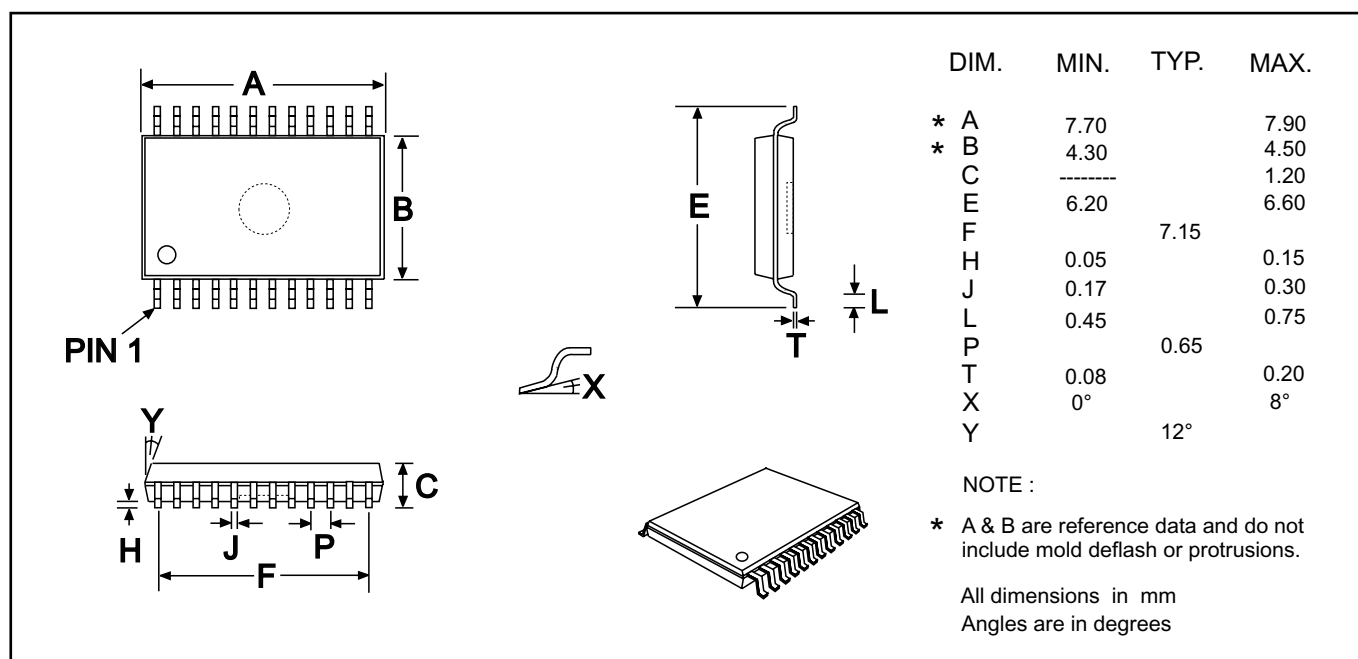
28-Pin TSSOP (E1)

(E1)



24-Pin TSSOP (E2)

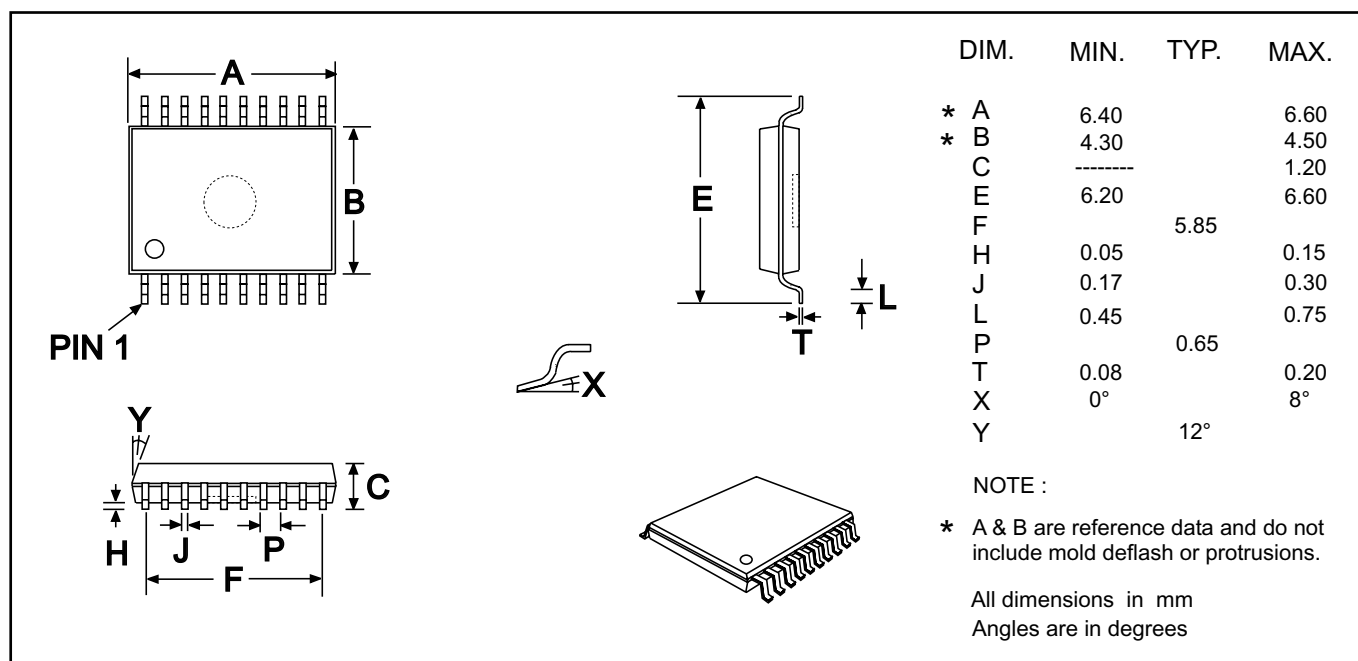
(E2)



CML Microcircuits Package Information

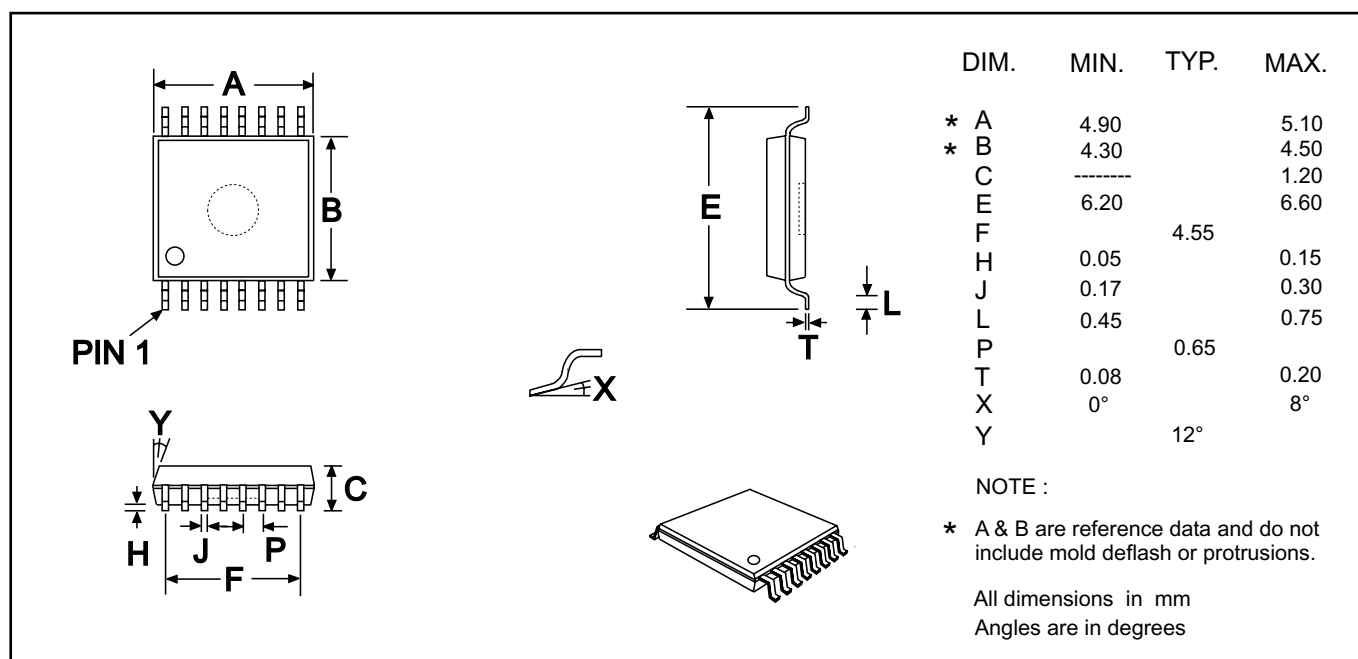
20-Pin TSSOP

(E3)



16-Pin TSSOP

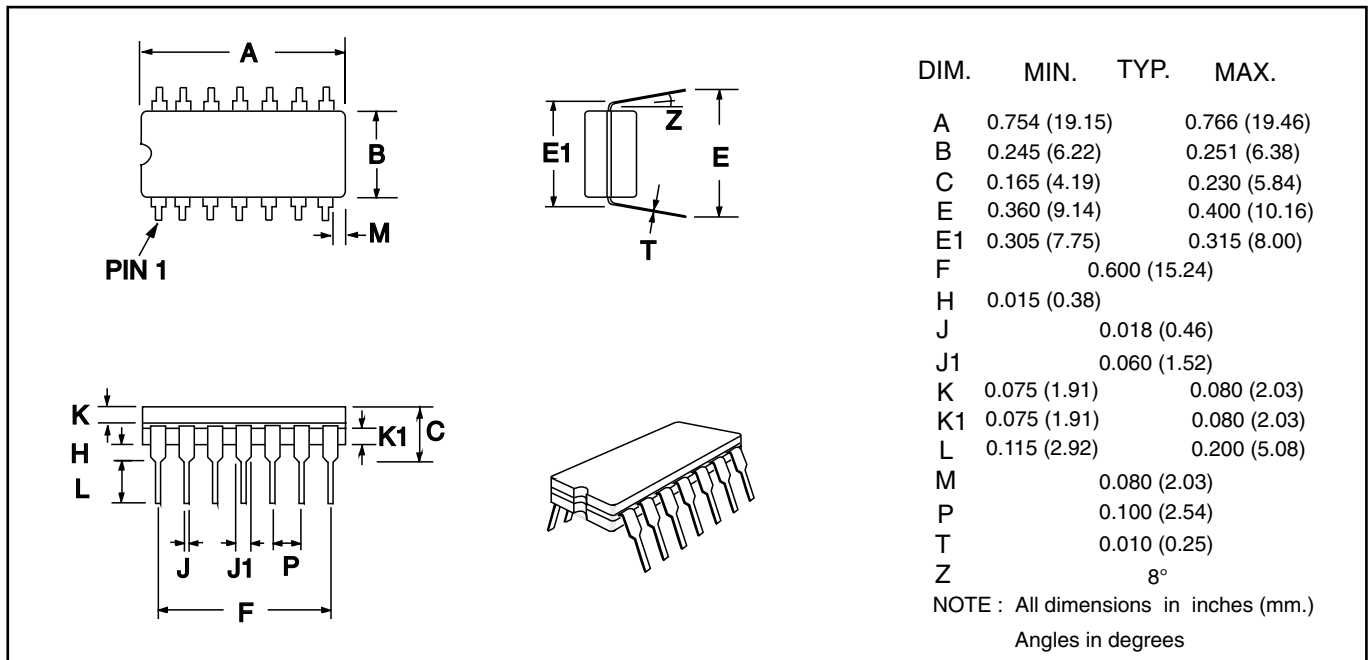
(E4)



CML Microcircuits Package Information

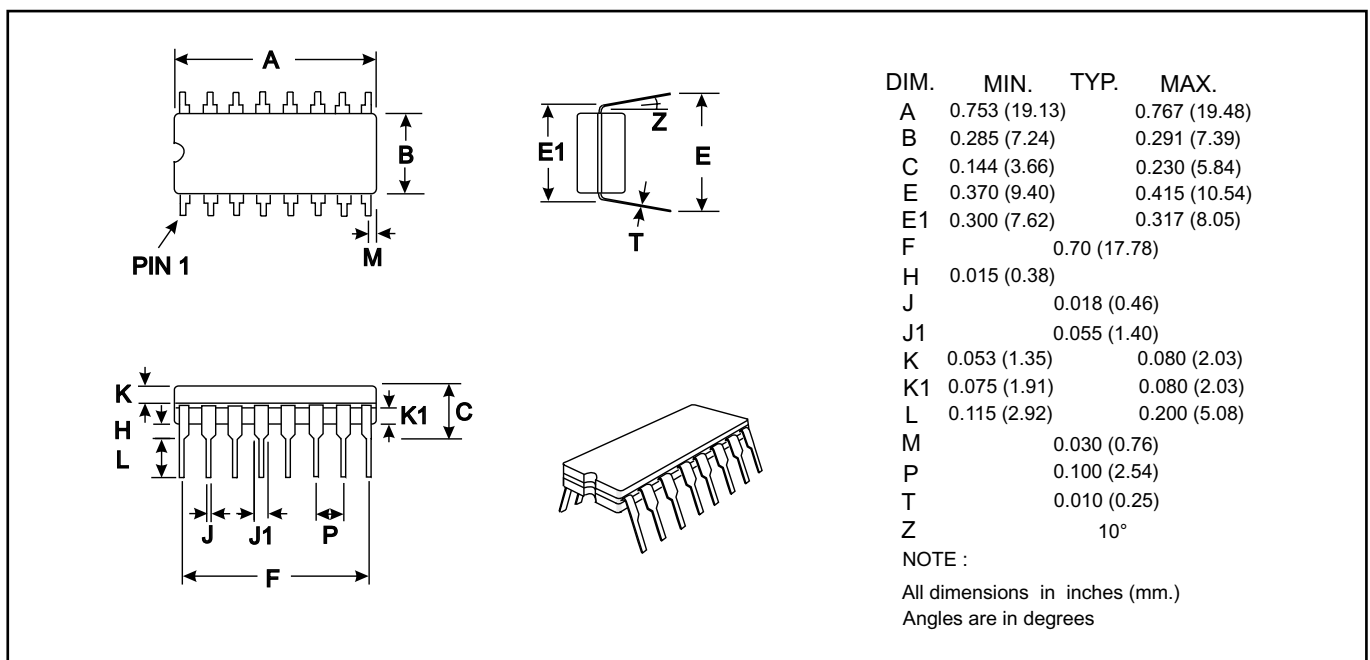
14-Pin Cerdip DIL; J

(J1)



16-Pin Cerdip DIL; J

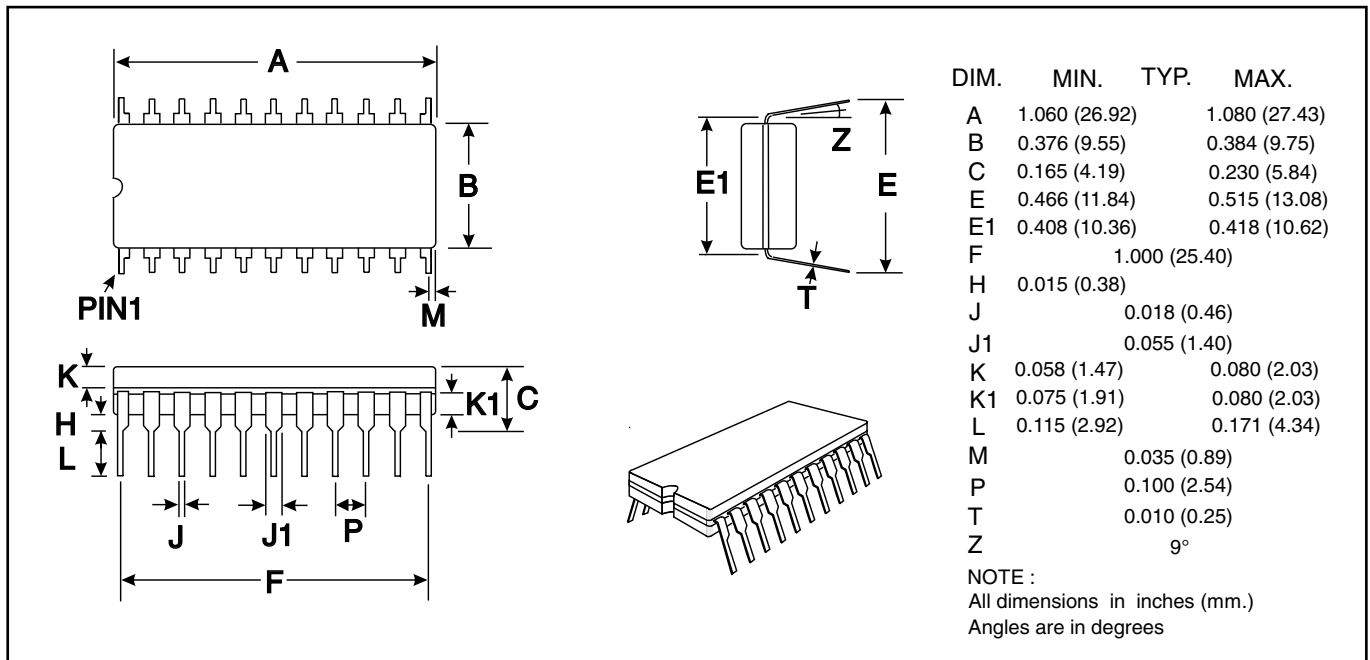
(J2)



CML Microcircuits Package Information

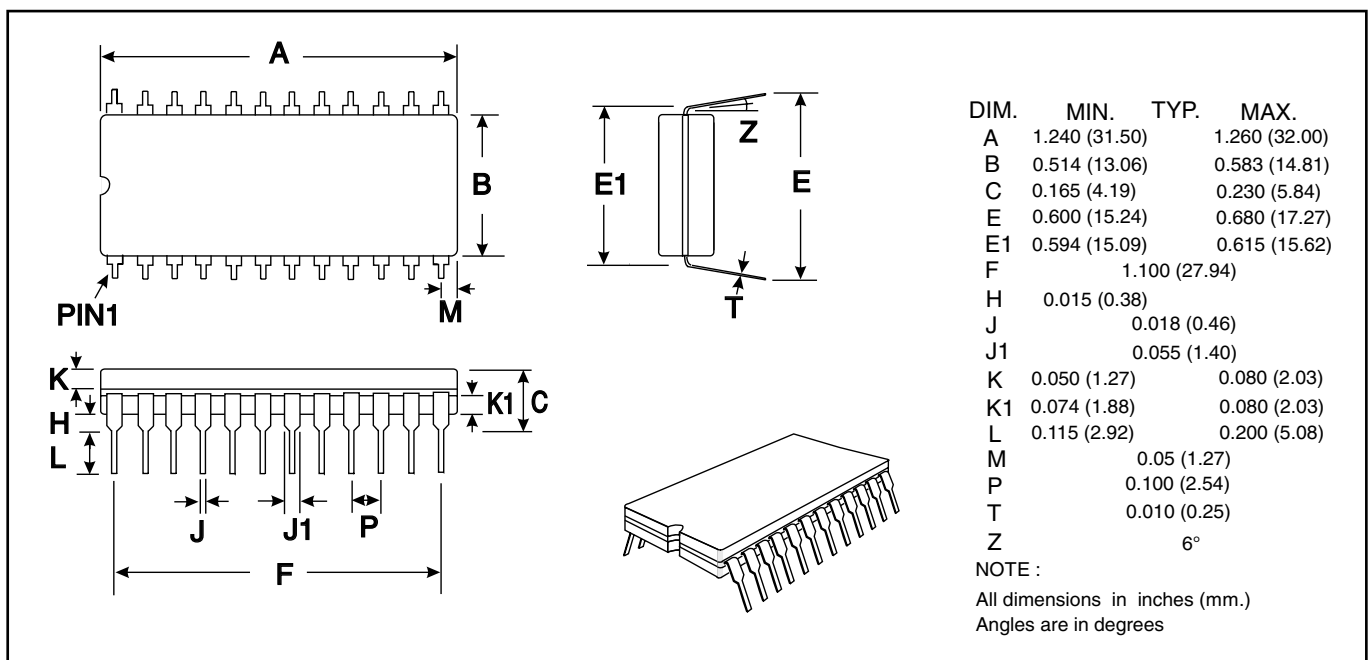
22-Pin Cerdip DIL; J

(J3)



24-Pin Cerdip DIL; J

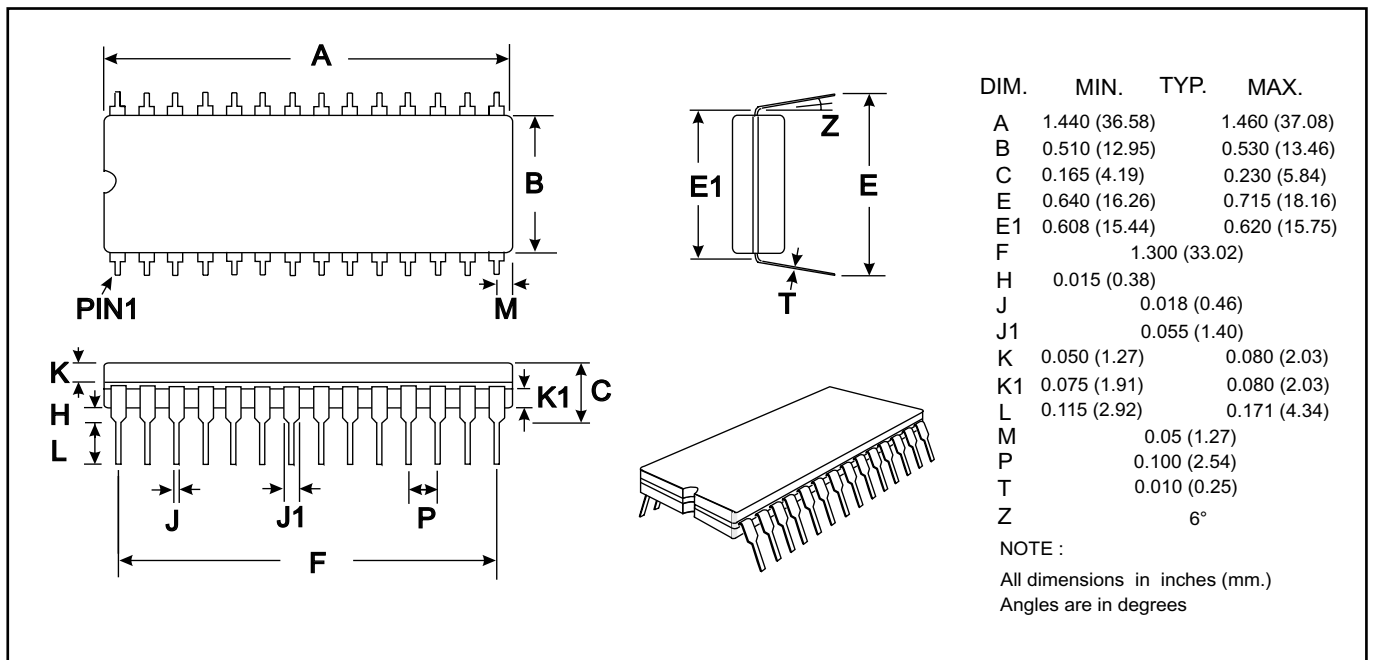
(J4)



CML Microcircuits Package Information

28-Pin Cerdip DIL; J

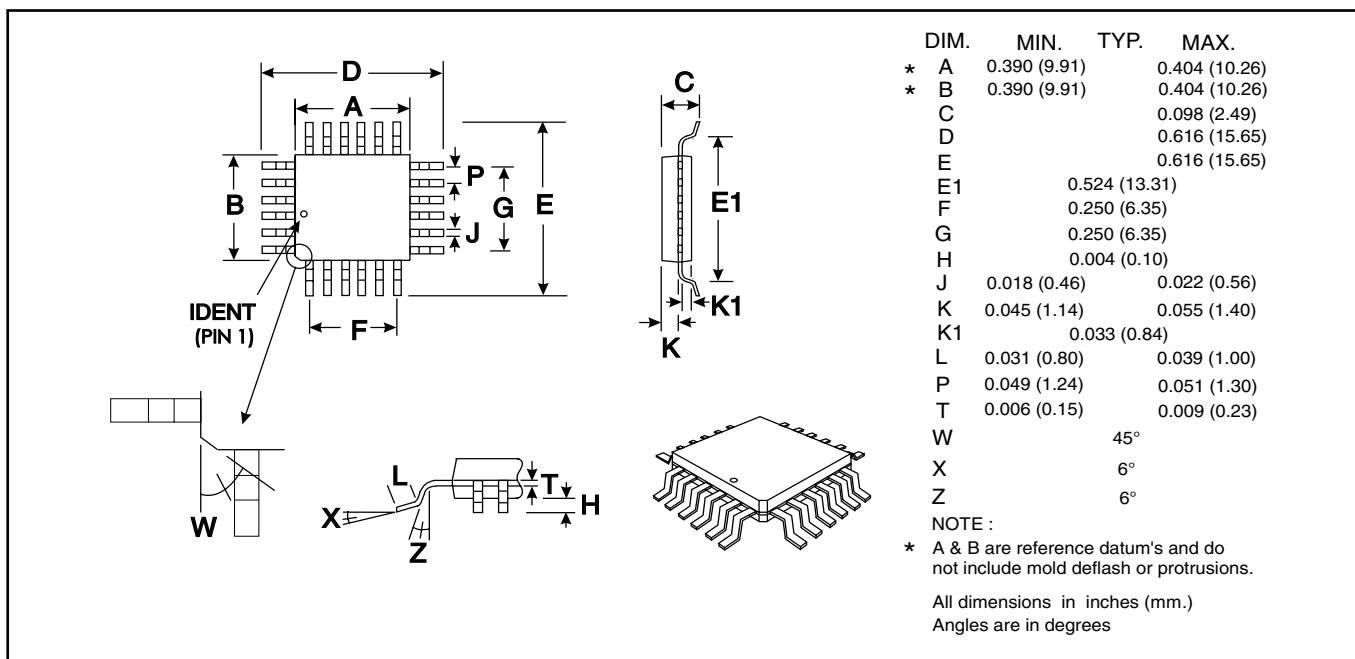
(J5)



CML Microcircuits Package Information

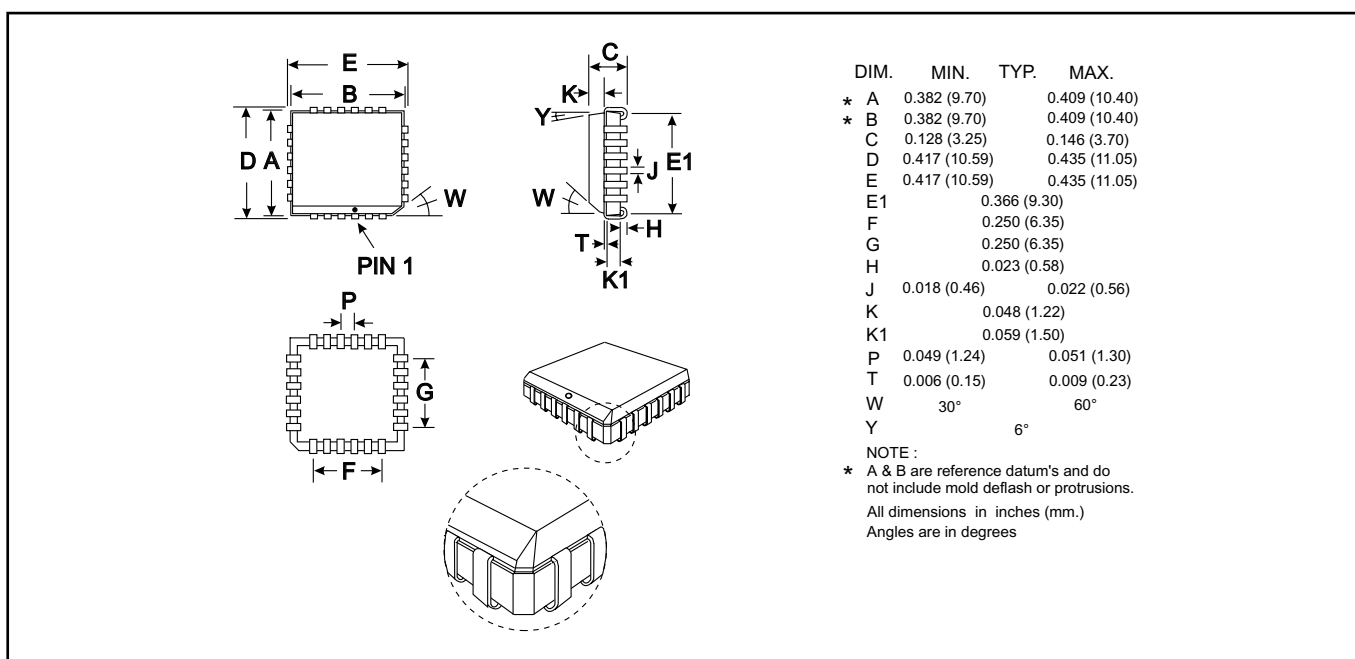
24-Pin PLCC; LG

(L1)



24-Pin PLCC; LS

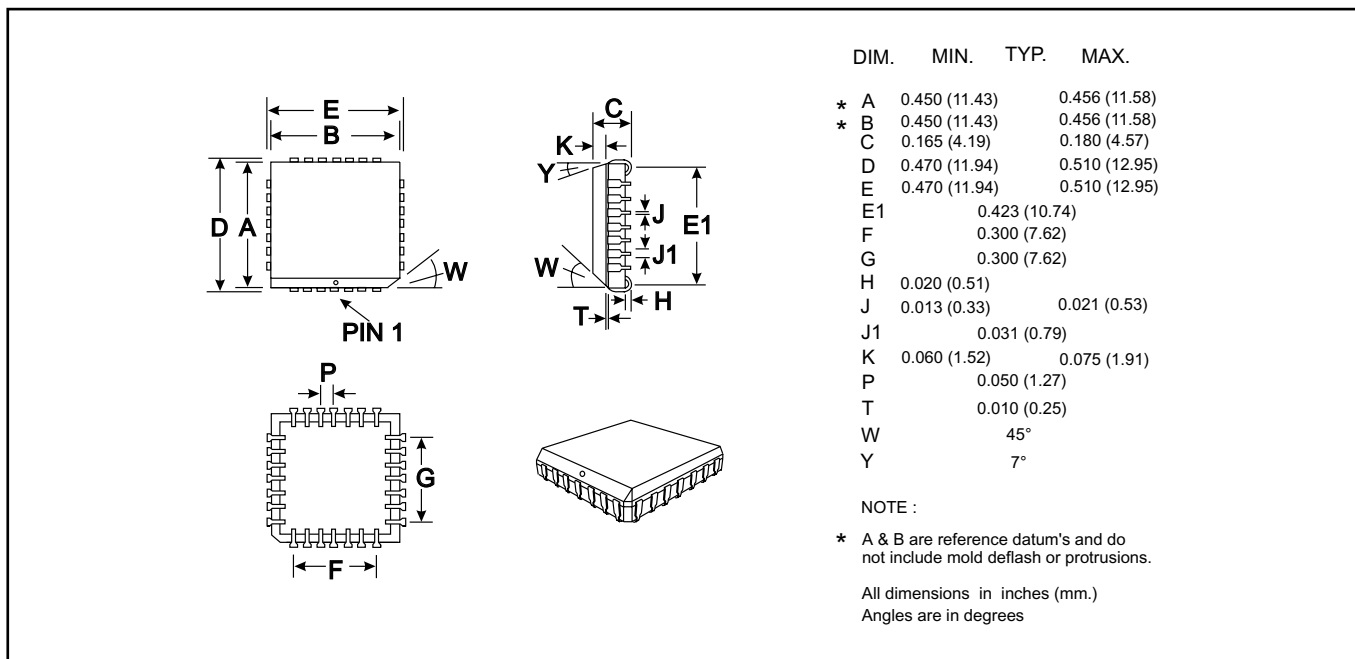
(L2)



CML Microcircuits Package Information

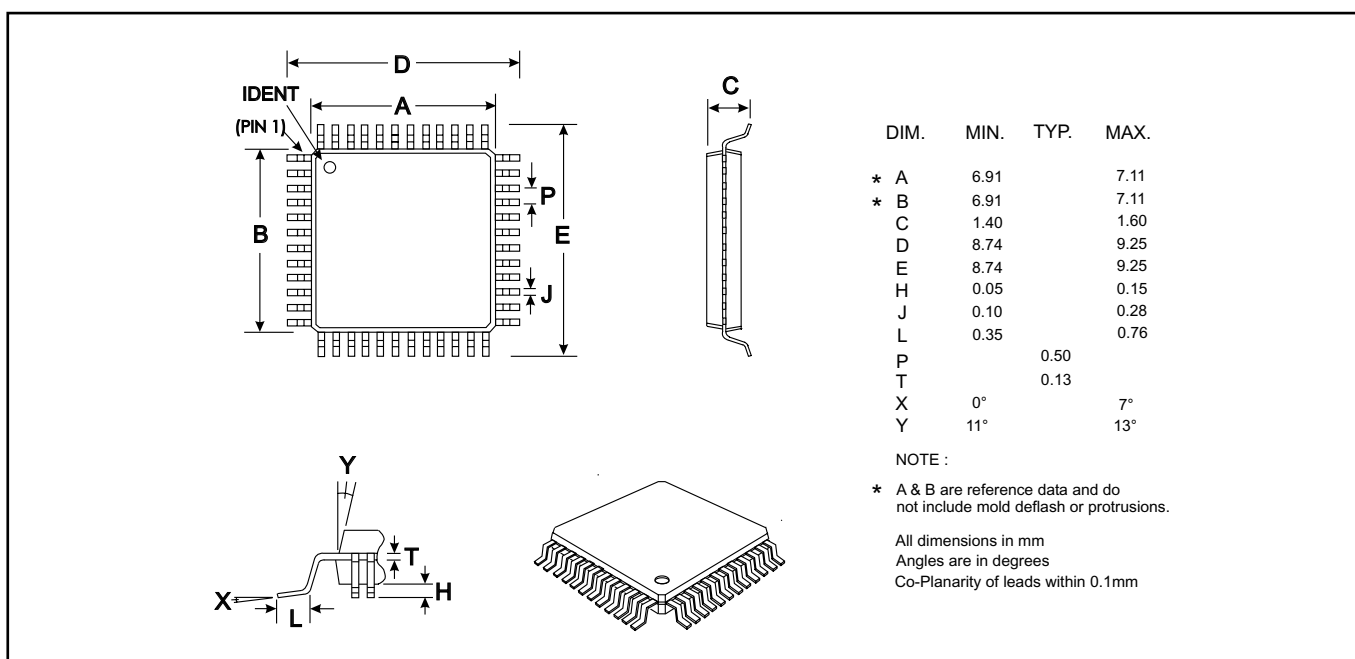
28-Pin PLCC; LH

(L3)



48-Pin LQFP

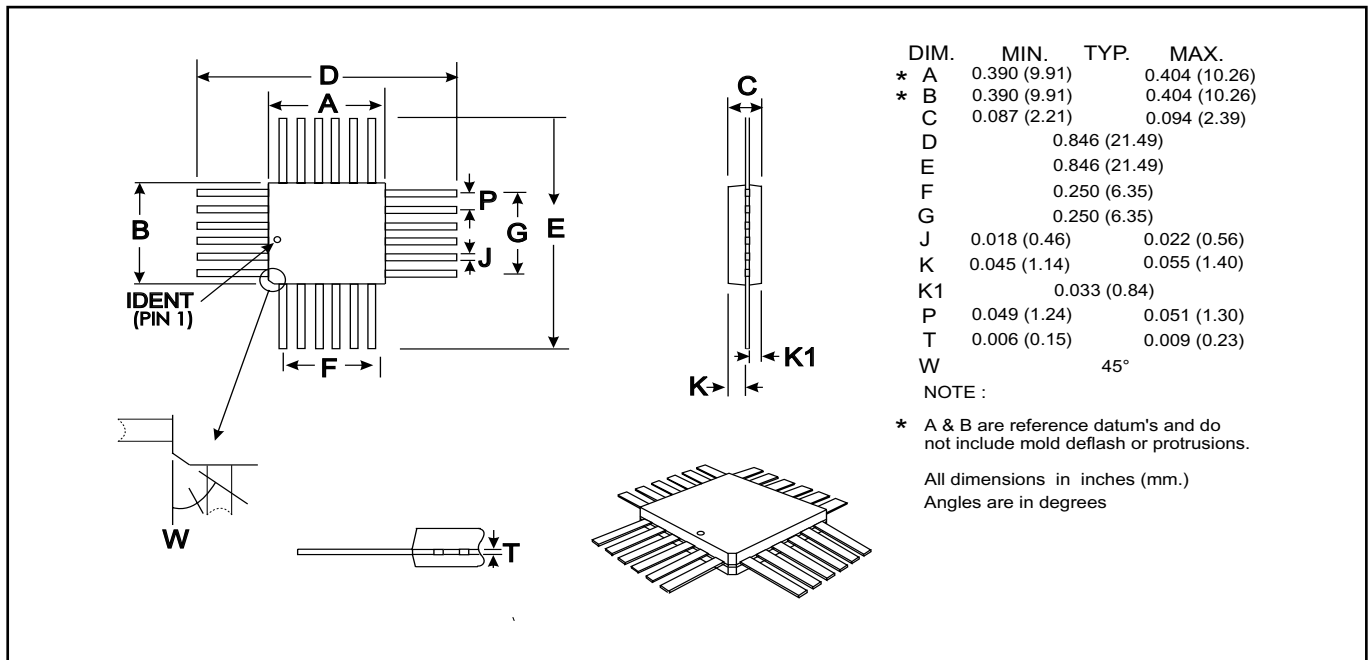
(L4)



CML Microcircuits Package Information

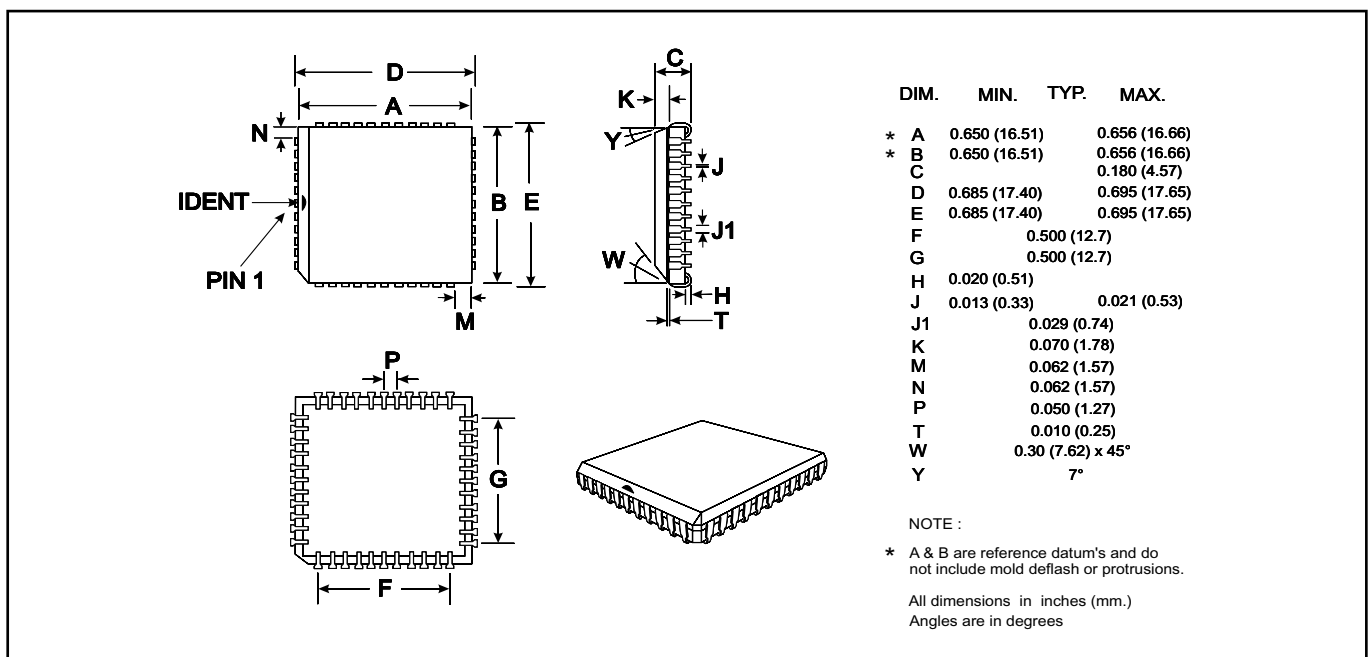
24-Pin PLCC; L

(L5)



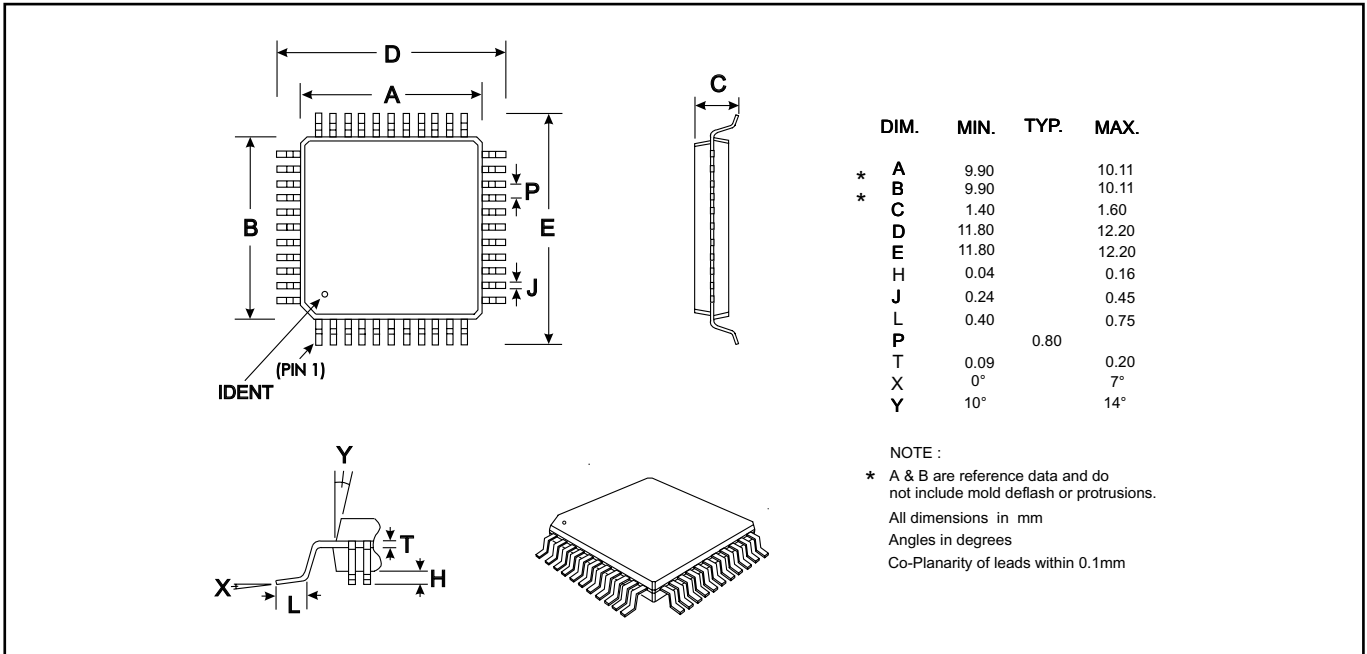
44-Pin PLCC; LH

(L6)

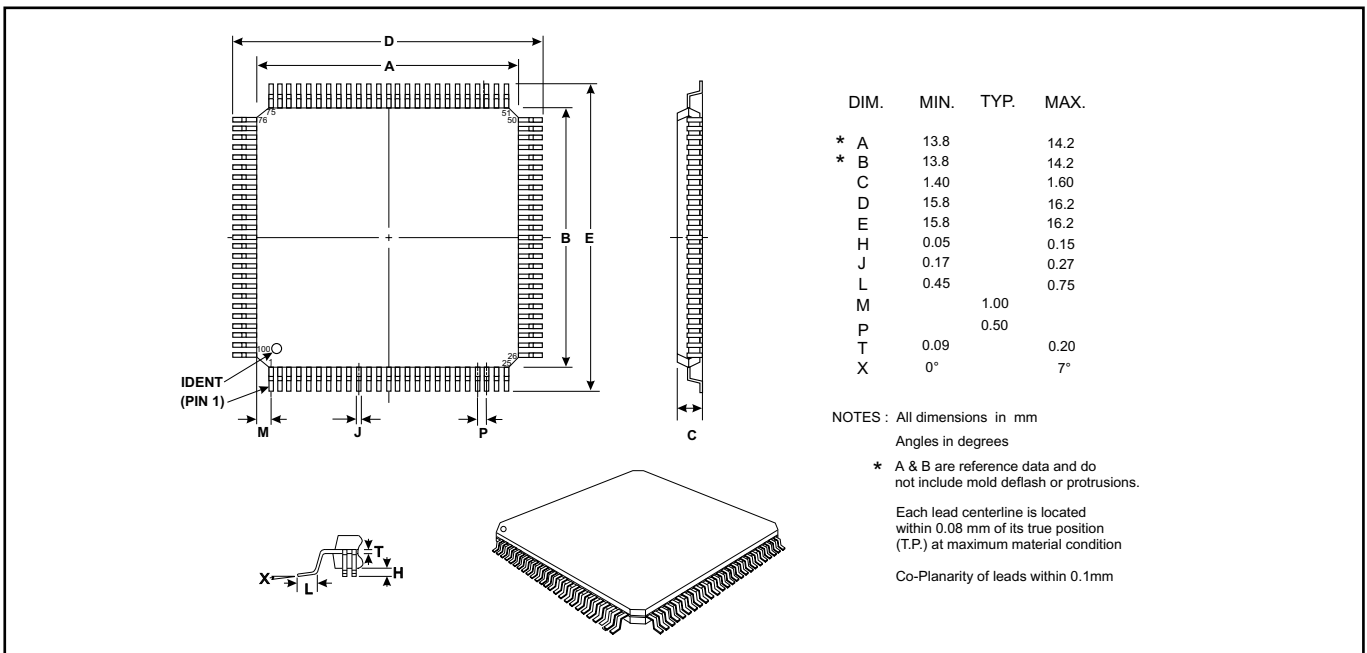


CML Microcircuits Package Information

44-Pin LQFP; L7

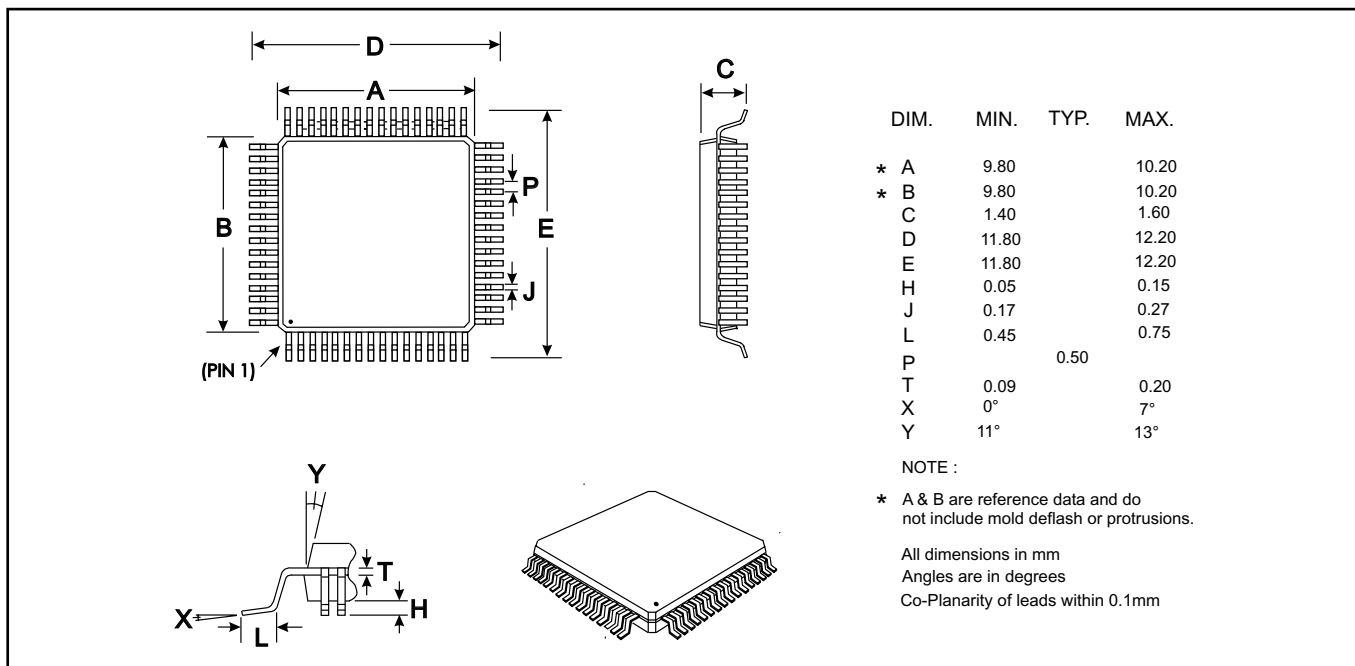


100-Pin LQFP; L8

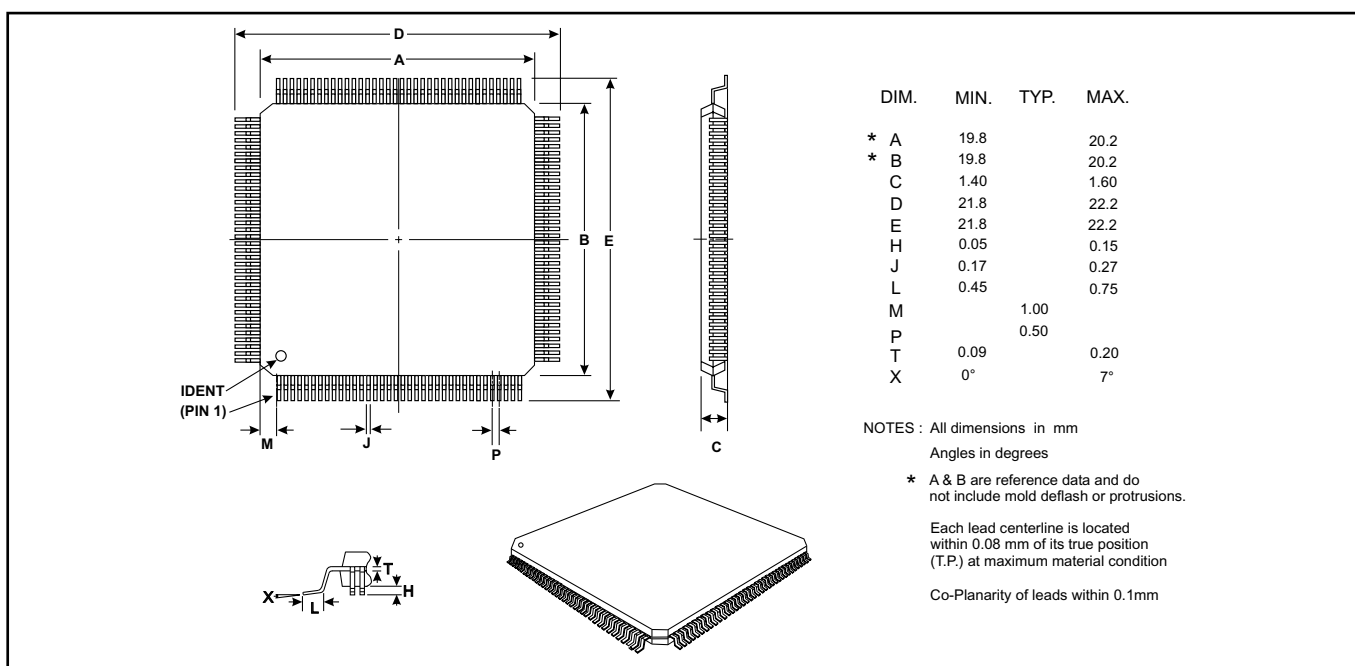


CML Microcircuits Package Information

64-Pin LQFP; L9

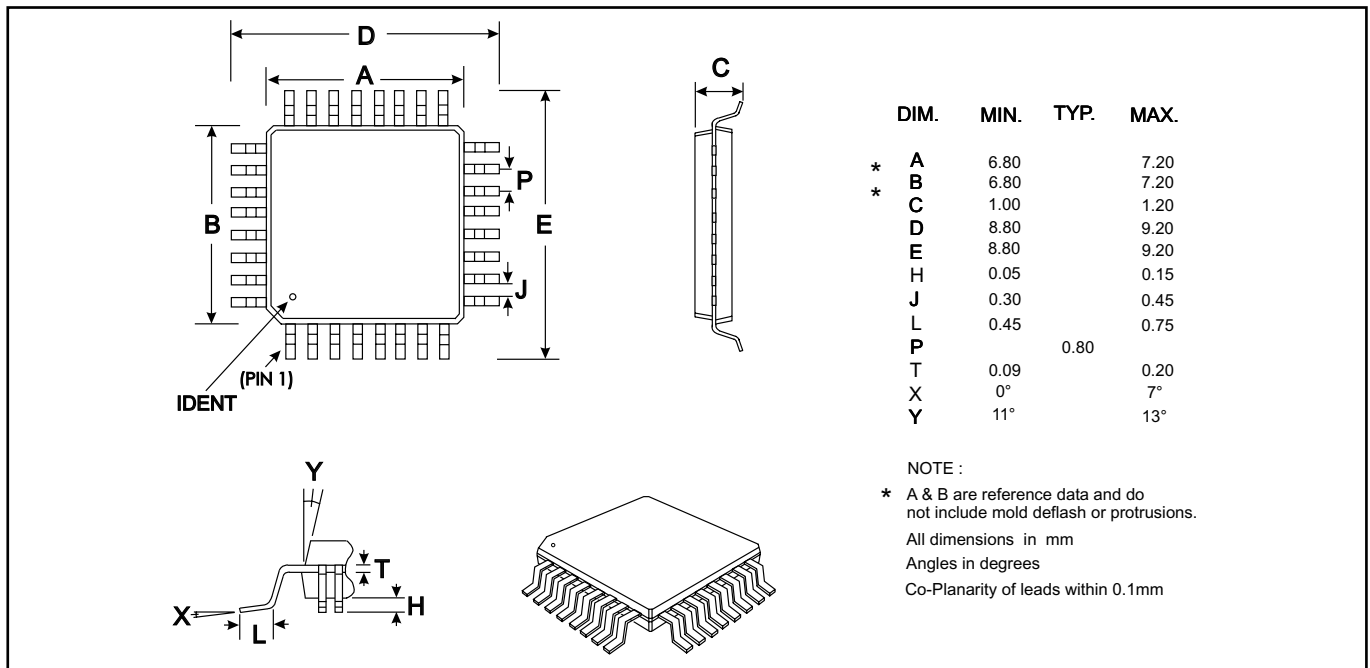


144-Pin LQFP; L10

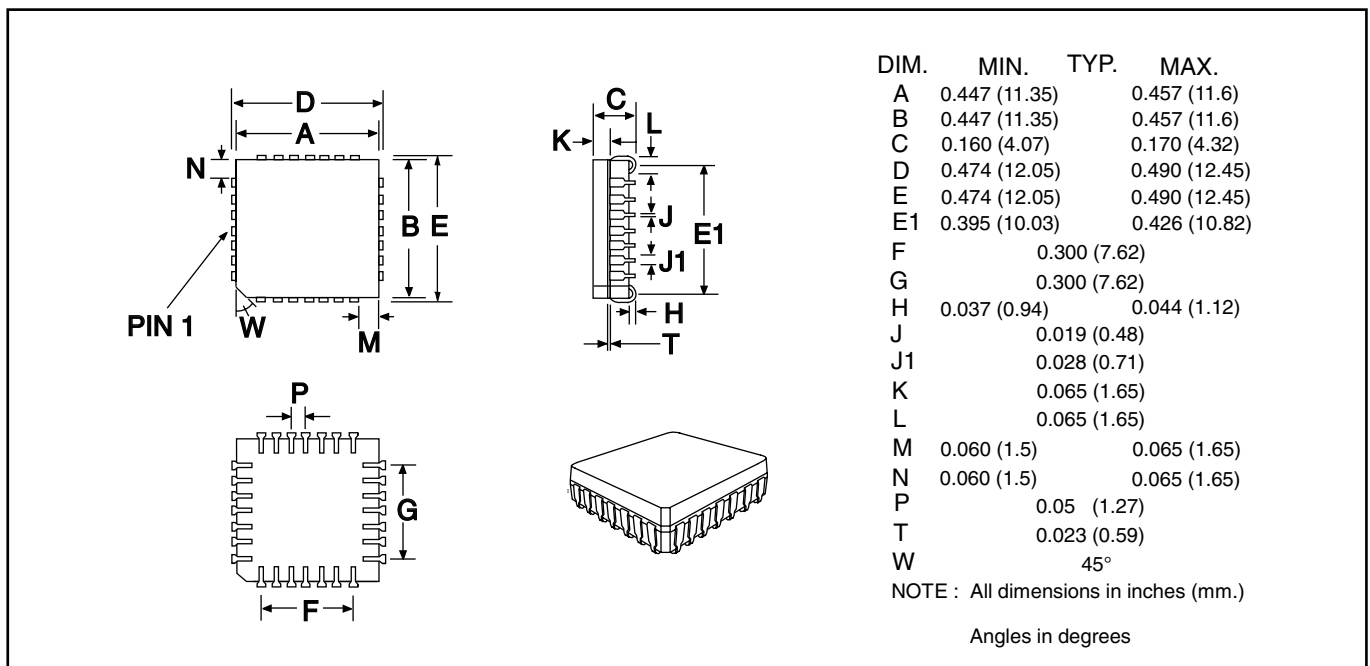


CML Microcircuits Package Information

32-Pin TQFP; L11



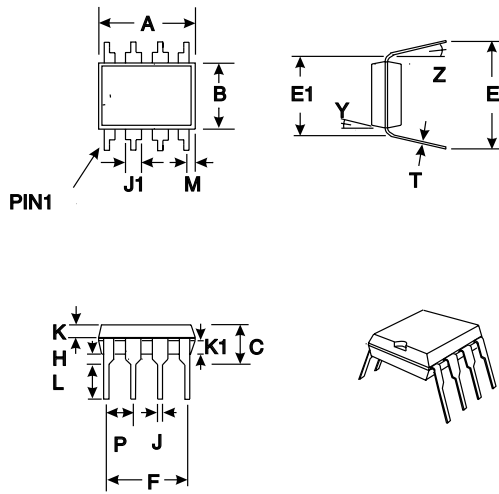
28-Pin Ceramic CLCC; M1



CML Microcircuits Package Information

8-Pin PDIP; P

(P1)

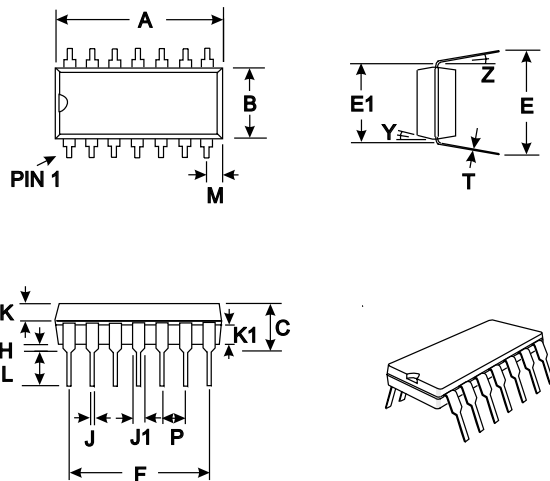


DIM.	MIN.	TYP.	MAX.
* A	0.346 (8.790)		0.400 (10.16)
* B	0.240 (6.10)		0.260 (6.60)
C	0.145 (3.68)		0.200 (5.08)
E	0.300 (7.62)		0.390 (9.91)
E1	0.290 (7.37)		0.325 (8.25)
F		0.30 (7.62)	
H		0.030 (0.76)	
J	0.015 (0.38)		0.023 (0.58)
J1	0.045 (1.14)		0.065 (1.65)
K		0.062 (1.58)	
K1		0.062 (1.58)	
L	0.121 (3.07)		0.150 (3.81)
M		0.029 (0.74)	
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	
Z		5°	

NOTE :
 * A & B are reference datum's and do not include mold deflash or protrusions.
 All dimensions in inches (mm.)
 Angles are in degrees

14-Pin PDIP; P

(P2)



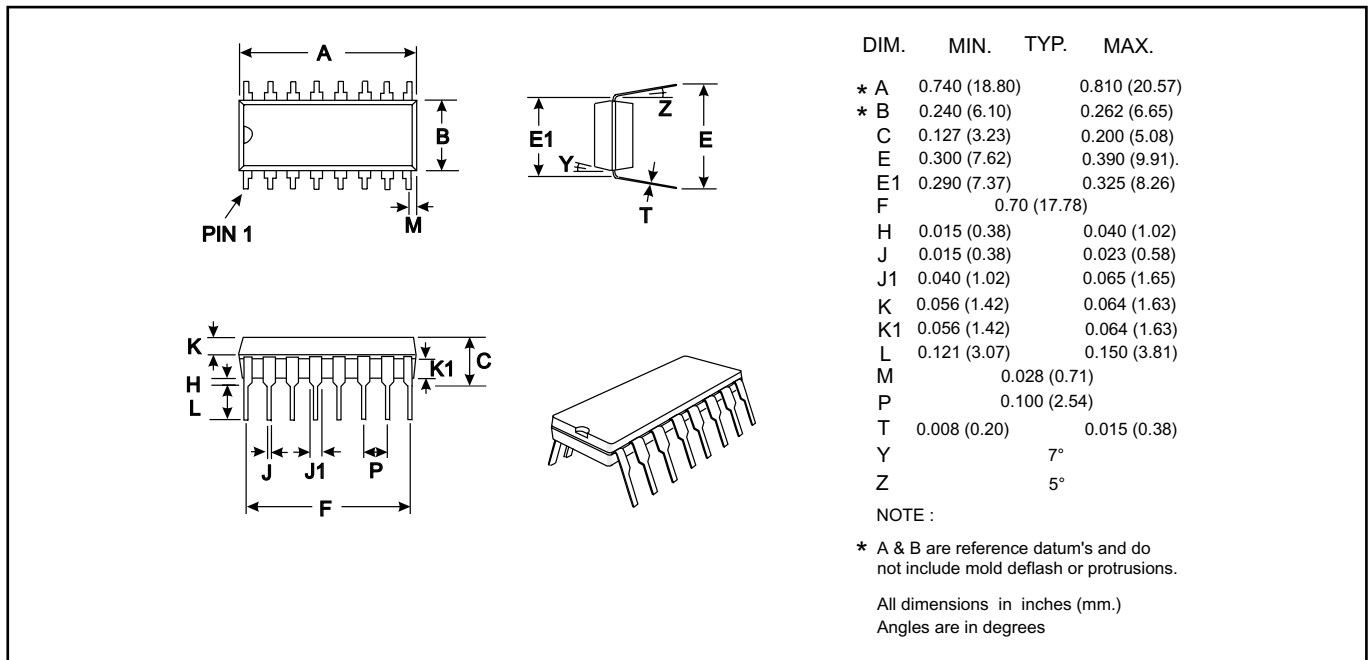
DIM.	MIN.	TYP.	MAX.
* A	0.740 (18.80)		0.810 (20.57)
* B	0.240 (6.10)		0.260 (6.60)
C	0.127 (3.23)		0.200 (5.08)
E	0.300 (7.62)		0.390 (9.91)
E1	0.290 (7.37)		0.325 (8.26)
F		0.60 (15.24)	
H	0.015 (0.38)		0.07 (1.78)
J	0.015 (0.38)		0.023 (0.58)
J1	0.045 (1.14)		0.065 (1.65)
K	0.056 (1.42)		0.064 (1.63)
K1	0.056 (1.42)		0.064 (1.63)
L	0.121 (3.07)		0.150 (3.81)
M		0.072 (1.83)	
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	
Z		5°	

NOTE :
 * A & B are reference datum's and do not include mold deflash or protrusions.
 All dimensions in inches (mm.)
 Angles are in degrees

CML Microcircuits Package Information

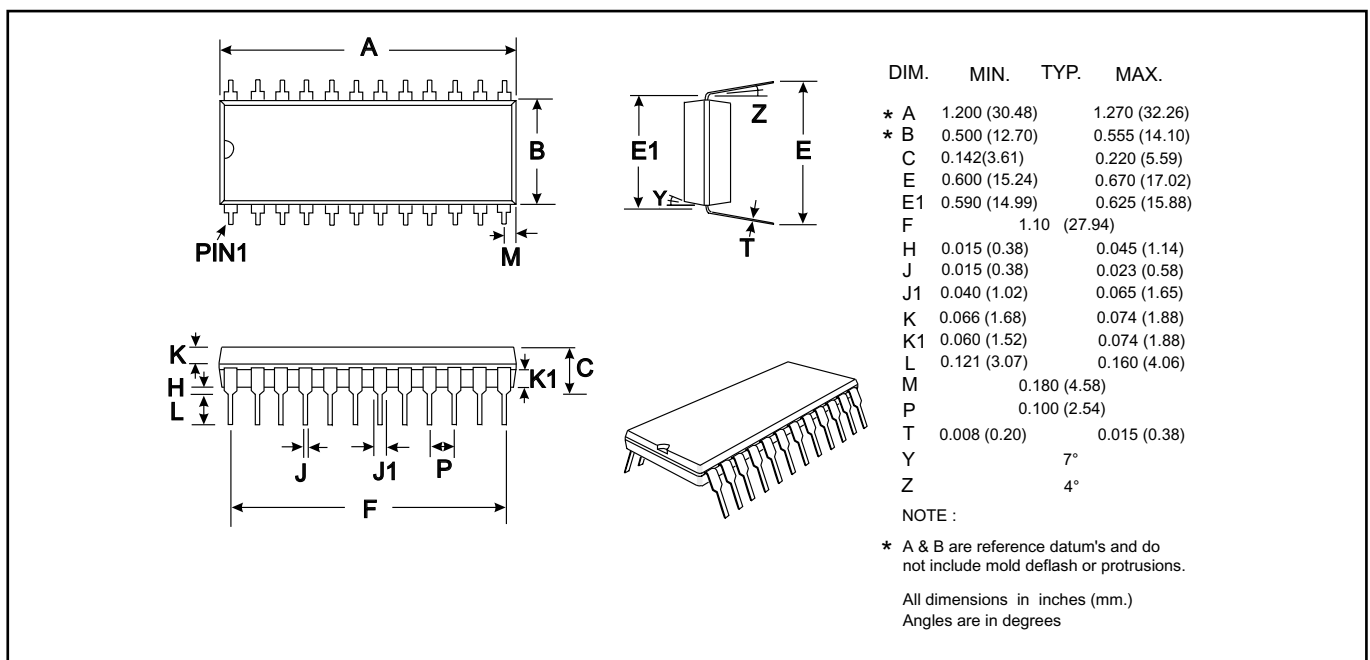
16-Pin PDIP; P

(P3)



24-Pin PDIP; P

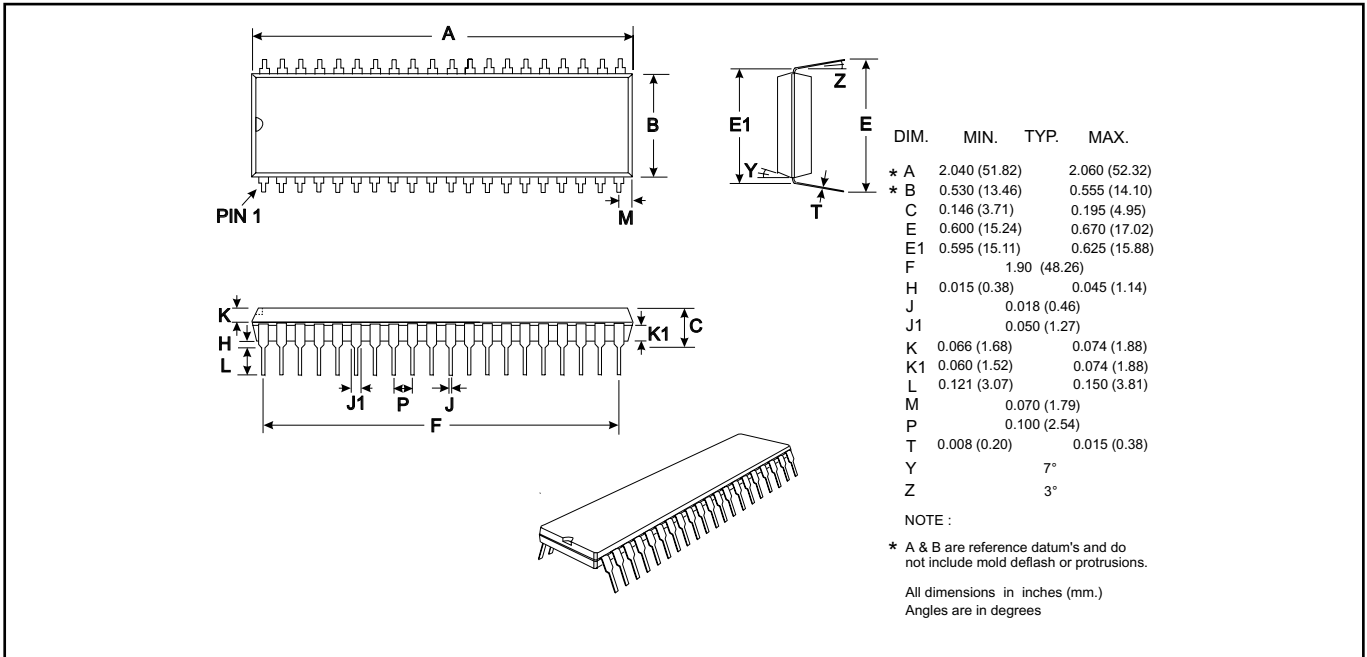
(P4)



CML Microcircuits Package Information

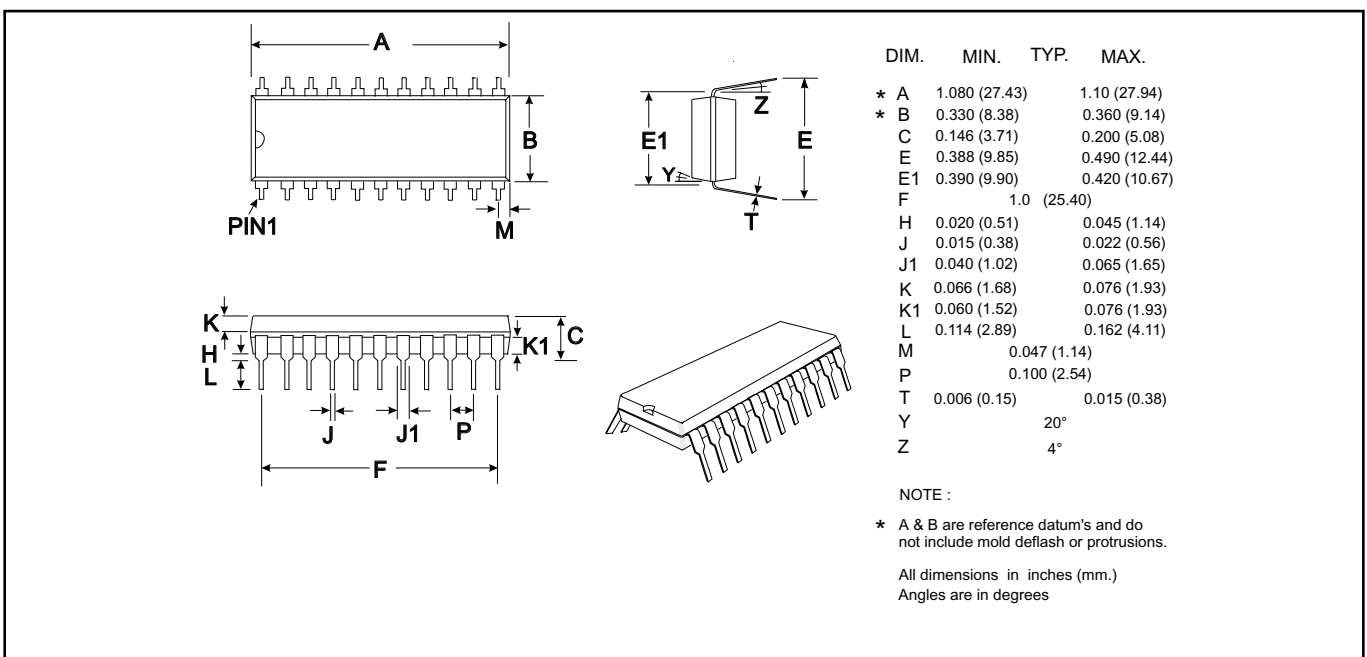
40-Pin PDIP; P

(P5)



22-Pin PDIP

(P6)



CML Microcircuits Package Information

64-Pin VQFN

(Q1)

DIM.	MIN.	TYP.	MAX.
* A		9.00 BSC	
* B		9.00 BSC	
C	0.80	0.90	1.00
F	7.00		7.80
G	7.00		7.80
H	0.00		0.05
J	0.18	0.25	0.30
K	0.20		
L	0.30	0.40	0.50
L1	0		0.15
P		0.50	
T		0.20	

NOTE :
 * A & B are reference data and do not include mold deflash or protrusions.
 All dimensions in mm
 Angles are in degrees

Index Area 1 Index Area 2

Dot Dot Chamfer

Index Area 1 is located directly above Index Area 2

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
 L minus L1 to be equal to, or greater than 0.3mm
 The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

56-Pin VQFN

(Q2)

DIM.	MIN.	TYP.	MAX.
* A		8.00 BSC	
* B		8.00 BSC	
C	0.80	0.90	1.00
F	4.25		6.25
G	4.25		6.25
H	0.00		0.05
J	0.18	0.25	0.30
K	0.20		
L	0.30	0.40	0.50
L1	0		0.15
P		0.50	
T		0.20	

NOTE :
 * A & B are reference data and do not include mold deflash or protrusions.
 All dimensions in mm
 Angles are in degrees

Index Area 1 Index Area 2

Dot Dot Chamfer

Index Area 1 is located directly above Index Area 2

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
 L minus L1 to be equal to, or greater than 0.3mm
 The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

CML Microcircuits Package Information

48-Pin VQFN

(Q3)

DIM.	MIN.	TYP.	MAX.
* A		7.00 BSC	
* B		7.00 BSC	
C	0.80	0.90	1.00
F	4.60		5.65
G	4.60		5.65
H	0.00		0.05
J	0.18	0.25	0.30
K	0.20		
L	0.30	0.40	0.50
L1	0		0.15
P		0.50	
T		0.20	

NOTE :

- * A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

Index Area 1 Index Area 2

Index Area 1 is located directly above Index Area 2

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

40-Pin VQFN

(Q4)

DIM.	MIN.	TYP.	MAX.
* A		6.00 BSC	
* B		6.00 BSC	
C	0.80	0.90	1.00
F	2.75		4.30
G	2.75		4.30
H	0.00		0.05
J	0.18	0.25	0.30
K	0.20		
L	0.30	0.40	0.50
L1	0		0.15
P		0.50	
T		0.20	

NOTE :

- * A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

Index Area 1 Index Area 2

Index Area 1 is located directly above Index Area 2

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

CML Microcircuits Package Information

32-Pin VQFN

(Q5)

DIM.	MIN.	TYP.	MAX.
* A		5.00 BSC	
* B		5.00 BSC	
C	0.80	0.90	1.00
F	3.00		3.80
G	3.00		3.80
H	0.00		0.05
J	0.18	0.25	0.30
K	0.20		
L	0.30		0.55
L1	0		0.15
P		0.50	
T		0.20	

NOTE :

- * A & B are reference data and do not include mold deflash or protrusions.
- All dimensions in mm
- Angles are in degrees

Index Area 1

Index Area 2

Dot

Index Area 1 is located directly above Index Area 2

Dot

Chamfer

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
 L minus L1 to be equal to, or greater than 0.3mm
 The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

24-Pin VQFN

(Q6)

DIM.	MIN.	TYP.	MAX.
* A		4.00 BSC	
* B		4.00 BSC	
C	0.80	0.90	1.00
F	2.55		2.80
G	2.55		2.80
H	0.00		0.05
J	0.18	0.25	0.30
K	0.20		
L	0.25		0.50
L1	0		0.15
P		0.50	
T		0.20	

NOTE :

- * A & B are reference data and do not include mold deflash or protrusions.
- All dimensions in mm
- Angles are in degrees

Index Area 1

Index Area 2

Dot

Index Area 1 is located directly above Index Area 2

Dot

Chamfer

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
 L minus L1 to be equal to, or greater than 0.3mm
 The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

CML Microcircuits Package Information

16-Pin VQFN

(Q7)

