FOR IMMEDIATE RELEASE

Pennsylvania Sept-13-2006 – Keystone Semiconductor, Inc. founded in 2005 by inventor Wen T. Lin in Spring House, Pennsylvania, announced today a huge breakthrough of electronic industry by introducing the new Arrival-time Locked Loop technology to replace the current Phase Locked Loop (PLL) technology.

The PLL technology was invented 80 years ago to produce a stable signal locally from a noisy signal received through the communication channel to help the world communicate. But due to its complexity, the popularity of PLL did not gain ground until the IC age arrived in the 70s. Since then, it has become the most popular technology to produce a stable clock signal from a reference signal source and is extensively used in electronics product today. Any electronic equipment that requires a stable clock signal has at least one of the PLL circuit inside, for example radio, stereo, TV, cable TV, cell phone, cordless phone, PCs, automobiles, satellite communications, GPS and including almost all electronic products today.

Despite its popularity and widespread use, the PLL is still very difficult to use today and causes a stability problem for the design engineer. This problem is commonly known as the dead-zone jittering problem. This problem occurs when the local signal is synchronized to the reference signal without phase offset. For years, engineers have battled with this nasty problem with many clever solutions, many of which are patented. It appears that this problem was finally under control when the IC industry advanced into submicron technology ten years ago. However, all the current solutions are still unable to lock the two signals together without phase offset and the phase detector always produces constant glitches to increase the noise level for the system, and worst of all, since nobody knows why the dead-zone jittering occurs in the first place, no one can guarantee that it won't happen again. This presents an immense threat to a system such as PC, a system that must be precisely clocked. A single jitter of clock can crash the whole system immediately. As the world is getting more precise in timing, the threat and cost of the dead-zone jittering is also getting higher.

The PLL's problem is very deep-rooted in two sources. The first problem is that the concept of phase locked is simply wrong. When a steady signal arrives at a steady rate but suddenly moves in time, there is really no way for the receiver to know what has been changed during the data transmission to cause the movement of signal. The movement of signal can be caused by the amplitude change, frequency change

or phase change. The only thing that the receiver knows for sure is that the arrival-time of the signal has been changed. However, the engineers have been taught all these years that the sudden movement of signal was only caused by the phase change and we needed a phase locked loop to solve the phase jittering problem. As can be imagined, everything we have been doing all these years is wrong. Although during the late 70's, a new breed of phase detector commonly known as "phase-frequency detector" (PFD) was born to greatly alleviate the phase locked problem. The PFD is simply a special kind of arrival-time detector that generates dead-zone jittering glitches. The introduction of PFD was a big step forward for the PLL technology and could have solved the phase locked loop problem forty years ago; however, lacking the concept of arrival-time, nobody had any clue what was missing until today.

The concept of arrival-time was invented about forty years later than the PLL, around 1960, when statistical physics and statistical communications were established as independent fields of study. The arrival-time of a signal is known as a stochastic process governed by the Poisson distribution. The nature of arrival-time is very difficult to analyze since it requires many tools from the theory of statistics. As a result, the concept of arrival-time is not popular among the electronic engineers today and most electronic engineers have never even heard of "arrival-time".

The second problem of the PLL is due to the current feedback control theory which provides the theoretical foundation for the current PLL. This technology is even older than the PLL and can be traced back to the ancient concept of servo control system. The feedback control theory has been improving the quality of life for all mankind since the industrial age began, but it could not help the engineers solving the dead-zone jittering problem because the current feedback control theory is poorly structured and not precise enough to guide the engineers to understand the nature of the feedback control loop.

For years before finishing their design of the feedback control loop, the engineers were taught to use a root locus plot or other tools to check the stability of the loop by varying the loop gain of the system from zero to infinity even though the loop gain of the system was usually a small fixed constant. The current feedback control theory was unable to explain why the root locus plot is needed and nobody seemed to care to find that out because the root locus plot had already helped the engineers to finish their job on time. Unfortunately, the same reason that the current feedback control loop theory failed to justify the need for the root locus plot turned out to be the same reason to explain why the dead-zone jittering problem was pro-

duced. The inability of the current feedback control theory to explain this simple fact indicates that there is a fundamental weakness with the current feedback control theory despite the fact that it was established for more than 150 years.

Wen T. Lin had experienced the dead-zone jittering problem many times in his career. The dead-zone jittering problem is the most frustrating and aggravating problem for electronic engineers because the better the engineers doing their job to balance the design, the more the dead-zone jitters. It is a brutal, confidence-shattering bug. Wen T. Lin was finally able to crack the dead-zone jittering problem in January of 2005 and he has filed numerous provisional patent applications for his findings since then. All his provisional patents are grouped into three formal PCT patent applications. The first installment of the arrival-time locked loop trilogy, PCT/US05/26842 entitled "A system and method of detecting a phase, a frequency and an arrival-time difference between two signals" was published by the patent authority for public review on August 10, 2006. The second installment entitled "Arrival-time Locked Loop" will be published in November of 2006. The last installment of the arrival-time locked loop will not be published until the summer of 2007.

The first patent asked many tough questions, provided the answers and solved many of the mysteries of the PLL and the crack of the PLL began to grow. The second patent built the theoretical foundation for the arrival-time locked loop from an entirely new concept and traced the problem of PLL back to the ancient feedback control theory. For the first time, engineers will know for sure what they are doing when designing a feedback control loop. No more guess work will be needed and they know exactly what to do and what to expect. The last patent will provide a surprise ending and show how the new technologies converge. These three patents provide a new foundation for the concept, theory, and circuits of the arrival-time locked loop. The concept and theory of new inventions, however, is not limited to the application of arrival-time locked loop. The new concept and theory can be applied to all the feedback control loop system as well. This new invention allows the design engineer to fully understand the nature of feedback control loop and guides engineers to a successful design every time.

Wen T. Lin was able to pin-point the sources of both problems in the current theories, fix them, and invent a new Arrival-time locked loop system that finally solves the dead-zone jittering problem once and for all so that the two signals can now be locked without phase offset. Since there is no phase offset, there is no

glitch output when the loop is locked and the phase noise of system is minimal. And since the source of the dead-zone jittering problem is completely fixed, the arrival-time locked loop is the only solution to guarantee the elimination of dead-zone jittering by design.

Wen T. Lin graduated with a BSEE from the National Taiwan University in 1978 and received an MSEE from Penn State University in 1984. His master thesis, entitled "Dead-time modified photocounting statistics for chaotic communications with arbitrary coherence time" was published by the Optical Society of America in 1984. It was a cutting edge study about the arrival-time of photons under the influence of random wideband noise.

Wen T. Lin's engineering career began as an analog design engineer for stereo equipment, color TV, video and cable TV equipments. He joined the O'Neill Communications, Inc. in 1988 as an RF engineer to develop the first spread spectrum radio for the PC network, Local Area Wireless Network (LAWN®). He started Omnispread Communications, Inc. in 1993 to continue the LAWN® business after O'Neill Communications, Inc. was closed. He then developed the new LAWNII® products for industrial customers in 1995 and has been producing LAWNII® products ever since.

The first installment of the arrival-time locked loop trilogy is now published by the PCT authority and can be downloaded from this address: http://www.wipo.int/pctdb by using the Publication No. WO/2006/083324. Due to the patenting process, the other two patent applications are still not available for public review; however, Keystone Semiconductor, Inc. will release the new inventions to the companies that wish to license the new technology from Keystone Semiconductor and sign a Non-Disclosure Agreement. For licensing information or if you have any questions, please contact Wen Lin at 215-654-9787 or by email wlin@keystonesemiconductor.com.

Keystone Semiconductor, Inc.
PO Box 248
809 N Bethlehem Pike #C6,
Spring House, PA 19477-0248
Phone: 215-654-9787
Fax: 215-654-9925