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Ring oscillators: Characteristics and applications

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The structure and operating principle of ring oscillators (RO) have been described. The expression for the frequency of oscillation of a complementary metal oxide semiconductor (CMOS) delay cell based conventional ring oscillator is presented and propagation delay of the delay stages is calculated. The limitations of a conventional RO have been studied and a few techniques to overcome these limitations have been mentioned. In this context, some modified structures of ring oscillators such as negative skewed delay RO, multi feedback RO, coupled RO are described for high frequency oscillation. The effect of noise sources on the output of ring oscillators has also been studied. Some potential applications of such ring oscillator based on its voltage tuning characteristics and multiphase outputs are also mentioned.

Keywords: Ring oscillator, CMOS inverter, Phase noise, Timing jitter

1 Introduction

Oscillatory behaviour is ubiquitous in all physical systems, especially in electronic and optical. In radio frequency and lightwave communication systems, oscillators are used for frequency translation of information signals and channel selection. Oscillators are also present in all digital electronic systems, which require a time reference, i.e., a clock signal, in order to synchronise operations. An ideal oscillator would provide a perfect time reference, i.e, a periodic signal. However all physical oscillators are corrupted by undesired perturbation/noise. Hence signals generated by practical oscillators are not perfectly periodic, since oscillator is a noisy physical system and it makes them unique in their response to perturbation/noise.

A variety of oscillators is available but the principle of operation, the frequency band of oscillation and the performance in noisy environment are different from one class of oscillators to the other. Recently[1], communication transceiver design in single IC demands monolithic oscillator with low cost and low power dissipation. In this system, the design of ring oscillator using delay stages inside the IC has created much more importance compared to other monolithic oscillators like relaxation oscillators. Generally, the performance of ring oscillator is better than relaxation oscillators although not as good as that of the sinusoidal oscillators. But the continuous efforts of the scientists and researchers have yielded in improving the performance of ring oscillators so as to attain a good level of satisfaction which can now be used successfully in the communication systems. The level of satisfaction has been achieved in both cases: speed of operation and noise performance.

2 Ring Oscillator and its Oscillation Frequency

Ring oscillator is cascaded combination of delay stages, connected in a close loop chain. The ring oscillators designed with a chain of delay stages have created great interest because of their numerous useful features. These attractive features are: (i) It can be easily designed with the state-of-art integrated circuit technology (CMOS, BiCMOS), (ii) It can achieve its oscillations at low voltage, (iii) It can provide high frequency oscillations with dissipating low power, (iv) It can be electrically tuned, (v) It can provide wide tuning range and (vi) It can provide multiphase outputs because of their basic structure. These outputs can be logically combined to realize multiphase clock signals, which have considerable use in a number of applications in communication systems. The oscillation frequency of an RO depends on the propagation delay τ_d per stage and the number of stages used in the ring structure. To achieve self-sustained oscillation, the ring must provide a phase shift of 2π and have unity voltage gain at the frequency of oscillation. In an m-stage ring oscillator, each stage provides a phase shift of π/m and dc inversion provides the remaining phase shift of π. Therefore, the oscillating signal must go through each of the m delay stages once to provide the first π phase

shift in a time of $m\,\tau_d$ and it must go each stage a second time to obtain the remaining π hase shift in a time period of $2m\,\tau_d$. Thus the frequency of oscillation is given by:

$$f_o = \frac{1}{2m\tau_d} \quad \ldots (1)$$

The oscillation frequency of an RO may be determined from the expression of τ_d which depends on the circuit parameters. But the main difficulty in obtaining the expression of τ_d arises due to the nonlinearities and parasitics of the circuit. The propagation delay of bipolar transistor based differential delay stage[2] and CMOS transistor based delay stage[3] are described by Alioto and Palumbo and Docking and Sachdev, respectively. Alioto and Palumbo[2] used a ramp input signal to calculate τ_d. But the only assumption made by Docking and Sachdev[3] is that the output voltage waveform of the RO is sinusoidal. From analytical and simulation results reported by Alioto and Palumbo[2] and Docking and Sachdev[3], one can note that the oscillation frequency is proportional to the tail current of the differential pairs. This property makes them useful in PLL as a VCO. Next, the oscillation frequency of a single ended inverter based RO is considered. Generally, single ended ring oscillators consist of CMOS delay cell comprising of a PMOS and an NMOS transistor with additional delay element at its output as shown in Fig. 1. When switching between on and off, the MOS transistor performs the operations in saturation, linear and cut off mode. The input of an inverter switches from low (v_{in}=0) to high (v_{in}=V_{DD}) is considered. In that time PMOS is in cut off region and capacitor C discharges through NMOS transistor and the discharge current is given by:

$$I_{DN} = -C\frac{dv_{out}}{dt}. \quad \ldots (2)$$

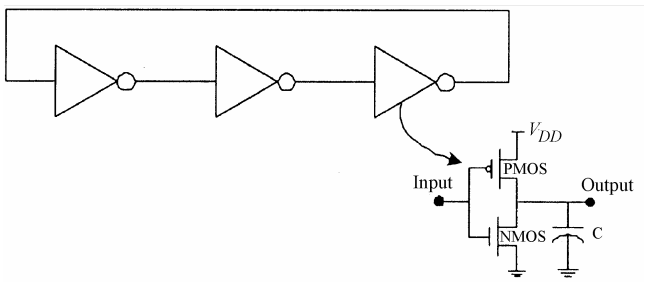

Fig. 1 — Hardware structure of single ended inverter based ring oscillator

The output propagation for high to low delay time (τ_{dhl}) is defined as the fall time of output voltage from V_{DD} to V_{DD}/2and it can be expressed as:

$$\tau_{dhl} = \int_{V_{DD}}^{V_{DD}/2} \frac{dv_{out}}{I_{DN}}. \quad \ldots (3)$$

where I_{DN} is the drain current of the n-channel metal oxide semiconductor (NMOS) transistor. The NMOS transistor changes from the saturation to linear mode of operation during the high to low transition at v_{out}=V_{DD}−v_{TN} while v_{in}=V_{DD} during this entire transition, where v_{TN} is the threshold voltage of the NMOS transistor. The above integral must be solved for each region of operation separately and thus the integral becomes:

$$\tau_{dhl} = -C\int_{V_{DD}}^{V_{DD}-v_{TN}} \frac{dv_{out}}{I_{DNS}} - C\int_{V_{DD}-v_{TN}}^{V_{DD}/2} \frac{dv_{out}}{I_{DNL}} \quad \ldots (4)$$

The drain current in saturation and linear mode of NMOS transistor can be expressed as I_{DNS}=$g_N(V_{DD}-v_{TN})^2/2$ and I_{DNL}=$g_N v_{out}[(V_{DD}-v_{TN})-v_{out}/2]$, respectively. Here g_N is transconductance parameter of the NMOS transistor. Thus evaluating the integration in Eq. (4), one gets:

$$\tau_{dhl} = \frac{C}{g_N(V_{DD}-v_{TN})}\left\{\frac{2v_{TN}}{(V_{DD}-v_{TN})} + \ln\left(\frac{3V_{DD}-4v_{TN}}{V_{DD}}\right)\right\}. \quad \ldots (5)$$

Now consider the output for low to high propagation delay time (τ_{dlh}), which is defined as the time delay to reach the output voltage at 50% of its maximum value V_{DD}. When the input of an inverter switches from high to low, the NMOS transistor goes into cutoff region. In that moment load capacitor C charges through PMOS transistor and the charging current is given by:

$$I_{DP} = C\frac{dv_{out}}{dt} \quad \ldots (6)$$

The PMOS transistor changes the mode of operation during the output from low to high transition. It changes from saturation to linear mode when v_{out} reaches $-v_{TP}$ while v_m=0 during this entire transition. Thus the propagation delay time can be expressed as:

$$\tau_{dlh} = C\int_{0}^{-v_{TP}} \frac{dv_{out}}{I_{DPS}} + C\int_{-v_{TP}}^{V_{DD}/2} \frac{dv_{out}}{I_{DPL}} \quad \ldots (7)$$

The drain current of PMOS transistor in saturation and linear mode can be expressed as:

$I_{DPS}=g_P(V_{DD}-v_{TP})^2/2$ and
$I_{DPL}=g_P(v_{DD}-v_{out})[(v_{DD}+v_{TP})-(v_{DD}-v_{out})/2]$

Thus evaluating the integration in Eq. (7) one gets:

$$\tau_{dlh}=-\frac{C}{g_P\left(V_{DD}+v_{TP}\right)}\left\{\frac{2v_{TP}}{\left(V_{DD}+v_{TP}\right)}+\ln\left(\frac{3V_{DD}+4v_{TP}}{V_{DD}}\right)\right\} \quad \ldots (8)$$

Therefore, total delay time in the decay and rise for m stage ring oscillator is $m(\tau_{dhl}+\tau_{dlh})$ and oscillation frequency is:

$$f_o=\frac{1}{m\left(\tau_{dhl}+\tau_{dlh}\right)}. \quad \ldots (9)$$

From the above discussion one may conclude that the number of inverter stages used in the ring structure and the propagation delay of the delay stages limit the oscillation frequency of the ring oscillator.

3 High Speed Ring Topology

The increase of oscillation frequency can be achieved in two ways: by reducing the propagation time delay of inverter stages or by decreasing the number of stages used in the ring structure. The delay of each stage depends on the circuit structure and process parameters. The reduction of the number of stages in the ring structure is attractive not only for the purpose of operational speed increment but also for the power consumption reduction and saving in the area for its implementation in ICs. But the number of available multiphase outputs reduces with the decrease of number of stages. To solve the conflict between oscillation speed and multiphase outputs several improved circuit structures have been reported earlier. Out of these, three popular high speed ring structures are: (i) negative skewed delay ring oscillator, (ii) multi-feedback ring oscillator and (iii) coupled ring oscillator. These are described in this paper. Besides having high frequencies, coupled ring oscillators are useful for producing quadrature outputs and coupled ring oscillator based array oscillators are useful for precise delay generation.

3.1 Negative skewed delay ring oscillator

A high speed ring oscillator for multiphase clock signal generation using negative skewed delay scheme has been reported by Lee *et al*[4]. This algorithm is valid for both odd and even number of inverter cells in the ring structure. The ring structure consists of CMOS inverter and a conceptual negative delay element inserted at one of the two transistor (PMOS/NMOS) inputs in the CMOS inverter. The input of the PMOS transistor is connected to the conceptual negative delay element; therefore the input signal to this transistor comes earlier than that of the NMOS transistor. But in conventional ring oscillator, the input signal of an inverter is simultaneously provided from the previous stage. In this scheme the input to the PMOS is one phase faster than that of the NMOS. This means that the PMOS input is derived from the (i-2)-th node while the NMOS input is derived from the i-th node. This scheme is also illustrated in Fig. 2 for five-stage ring oscillator. Simulation results as reported by Lee *et al.*[4] confirm the theoretical prediction that the oscillation frequency of negative skewed delay ring oscillator is 50% higher than that obtained from a conventional ring oscillator without reducing the number of available multiphase outputs. But the minimum number of stages required to maintain oscillation is five whereas in conventional ring oscillator two stages for differential inverter and three stages for single ended inverter are required to maintain oscillation. However, negative skewed delay ring structure with less than five stages in its loop may be oscillatory if differential delay stages with proper feedback mechanism are used. A three-stage four inputs differential delay cell based high speed self-regulating voltage controlled ring oscillator using negative skewed delay scheme has been reported by Yan *et al.*[5]. Here differential stages are used mainly for producing oscillation even when the number of stages in the ring structure is less than five and to obtain improved noise performance due to supply fluctuation. In this scheme, ring oscillator with even

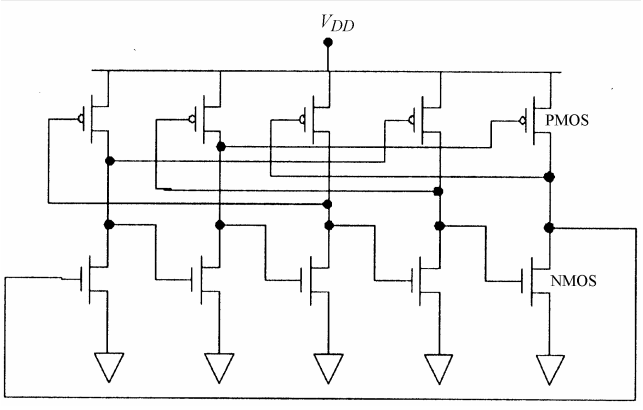

Fig. 2 — Five stages negative skewed delay ring oscillator

number of stages, if the PMOS input is derived from the (i-2)-th node and the NMOS input is derived from the i-th node, all the nodes of the ring oscillator have stable voltages set to either the power supply or ground, and the ring oscillator can not oscillate. The feedback mechanism of the ring oscillator with an even number of stages is different from that of a ring oscillator with an odd number of stages for its operation. For example, in case of ten-stage ring oscillator, the PMOS and NMOS transistor inputs should be derived from the (i-3)-th node and i-th node respectively to achieve self sustained oscillation. Negative skewed delay ring oscillator consumes almost double power than that of the conventional ring oscillator.

3.2 Multi-feedback ring oscillator

It is well known that there is an inverse relationship between oscillation speed and multiphase outputs in conventional single ended inverter based ring oscillator. The number of multiphase outputs is equal to the number of stages m used in the ring structure. The oscillation speed is also inversely proportional to the time delay τ_d per stage. Therefore, average time delay per stage should be reduced without decreasing the number of stages in the ring structure to achieve multiphase outputs as well as high speed operation. To solve the conflict between high speed and multiphase output several ring topologies are described earlier. Out of these, a general ring oscillator topology for multiphase outputs, has been reported by Sun and Kwasniewski[6]. The topology uses sub-feedback loops inside a long chain ring oscillator for both multiphase outputs and high speed operation. In each sub-feedback loop, there exists an optimum number of inverter stages that keeps the circuit reliably oscillating at a higher speed and at the same time it maintains a constant phase relationship among the inverter stages due to the symmetric structure of the loop. Thus reduced time delay per stage can be achieved due to the presence of sub-feedback loop. The feedback index i is an integer number, in the range $2 \le i < m$, which represents the number of inverter stages in each sub feedback loop. The sub feedback loop can contain an even (i = 2, 4, 6, …) or odd (i = 3, 5, 7, …) number of inverter stages. An odd number of inverters inside a sub feedback loop increases the oscillation frequency, while an even number of inverters in the sub feed back loop decreases the oscillation frequency because frequency increment or decrement depends on the phase difference between two adjacent node and feedback indexes. For a long chain ring oscillator, there exists an optimum feed back index i, which gives the highest oscillation frequency. Such ring topology is shown in Fig. 3.

3.3 Coupled ring oscillator

Coupled ring oscillators are not only attractive for high speed operation but also multiphase quadrature outputs. Specially designed single ended inverter based coupled ring oscillator can produce quadrature output, which is not a common feature of all conventional single ended inverter based ring oscillators but quadrature outputs are available in differential ring oscillator. Moreover, coupled oscillator may be useful in noisy environment because it has better phase noise and jitter performance for a given power dissipation and oscillation frequency than conventional ring oscillators. Different varieties of coupled oscillator are described below.

A three-stage coupled ring oscillator has been reported by Grozing *et al.*[7] to produce quardrature outputs and high speed oscillation. Here a simple linear model of the ring oscillator is used to predict the oscillation frequency of the coupled oscillator. Two three-stage conventional single ended ring oscillators are coupled together in such a way that the system can oscillate by producing three sets of

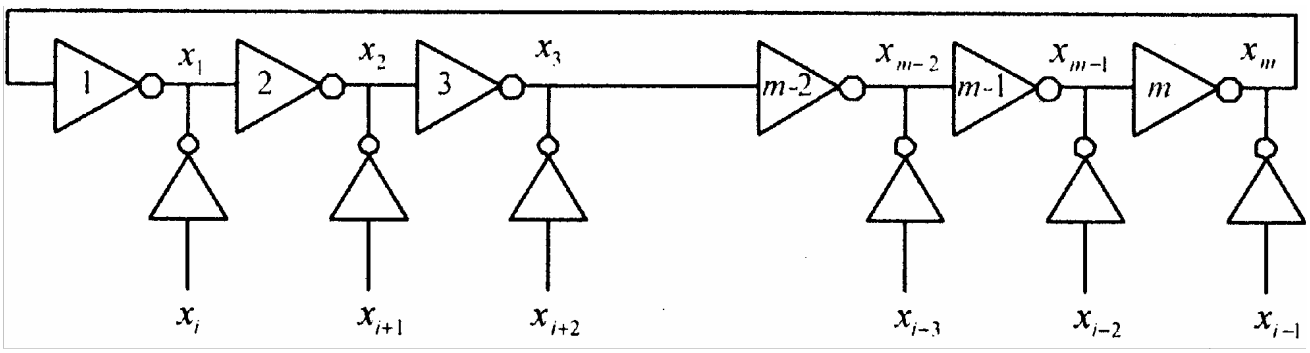

Fig. 3 — Multi-feedback ring oscillator based on single ended delay stages

quadrature outputs with 30° phase difference between the adjacent vertical nodes as shown in Fig. 4. Analytical study regarding the oscillation frequency of the coupled oscillator has been done by solving a matrix equation, which was derived from the transfer function and the previous output of the delay stage. Valid eigen function of the transfer matrix of the system shows that the oscillation frequency of the coupled oscillator is 1.57 times greater than that of the oscillation frequency of the conventional three-stage ring oscillator. This coupled ring oscillator occupies double chip area and dissipates almost twice as much power as conventional ring oscillator.

Three stage coupled ring oscillator, which is also capable of producing quadrature outputs have been reported by Mesgarzadeh and Alvandpour[8]. In this ring topology, two additional delay cells are used to couple two conventional single ended inverter based ring oscillators as shown in Fig. 5. The coupled system can produce two sets of quadrature outputs with 90° phase shift as indicated in the Fig. 5. The oscillation frequency of these coupled ring structures is equal to the oscillation frequency of the conventional single ended inverter based ring oscillator. These coupled oscillators have better phase noise performance compared to conventional ring oscillators.

Coupled ring oscillators are also used to generate precise delay. Maneatis and Horouitz[9] described a two- dimensional array oscillator (Fig. 6) based on coupled rings to generate precise delays with a resolution equal to an inverting buffer delay divided by the number of rings. The basic idea in this ring topology is to force several rings oscillating at the same frequency to be uniformly offset in phase by a precise fraction of a buffer delay. However, the oscillation frequency is determined primarily by the number of buffers per ring and is largely independent of the number of rings in the array. More output phases can be added, and the delay resolution can be increased simply by adding rings to the array. This type of array oscillator can be realized using both single ended or differential inverting buffer.

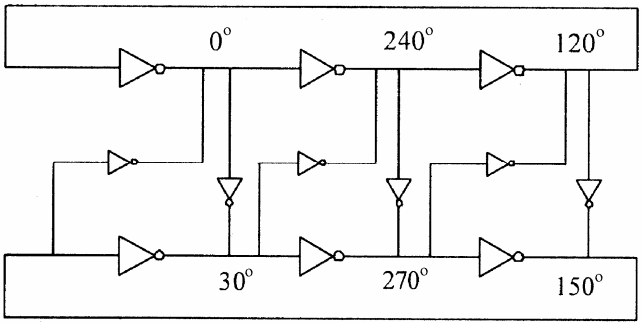

Fig. 4 — Three sets of quadrature output high speed coupled ring oscillator based on single ended delay stages

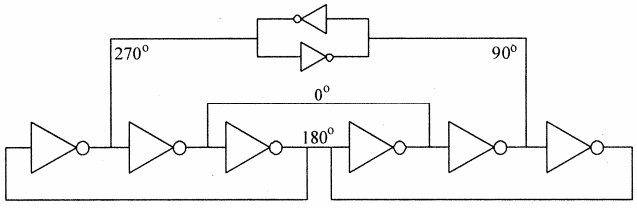

Fig. 5 — Two sets of quadrature output coupled ring oscillator based on single ended delay stages

4 Effect of Noise Sources on the Output of an Oscillator

Noise source changes the frequency spectrum and timing interval of transition of the oscillator dramatically. In general, such noise sources can be classified into two broad groups: (i) deterministic noise and (ii) random noise. There are four main sources of deterministic noise: (a) Crosstalk between adjacent signal traces, (b) EMI radiation on a sensitive signal path, (c) Noise from power layers of a multilayer substrate and (d) Simultaneous switching of multiple gates to the same logic state. Random noise sources include: (a) Thermal noise, which is associated with electron flow in conductors, (b) Shot noise, which normally occurs due to potential barrier in semiconductors. When the electrons and holes cross the barrier, shot noise is produced, (c) Flicker (1/*f*) noise, which is associated with crystal surface defects in semiconductors. It is often referred to as

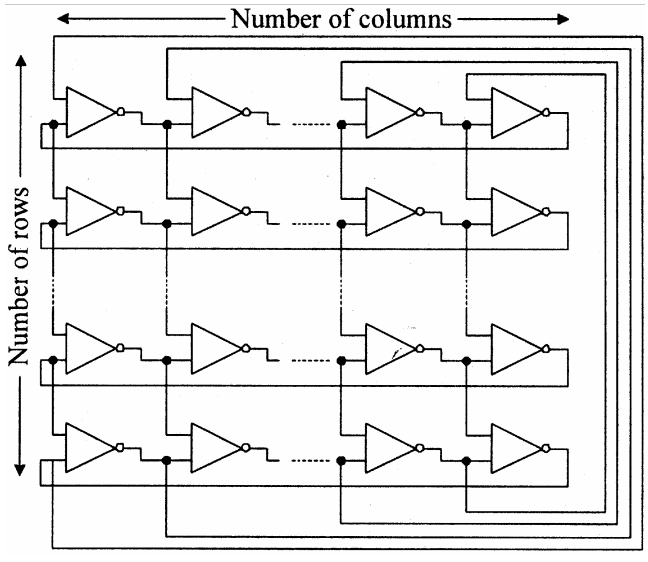

Fig. 6 — Two dimensional array oscillator based on dual input inverter stages ring oscillator

pink noise because most of the power is concentrated at the lower end of the frequency spectrum. These noise sources affect both amplitude and phase of all oscillators. In all practical stable oscillators, amplitude fluctuation can be ignored because the amplitude may be limited by an automatic gain control or by the intrinsic non-linearity of the oscillating systems. Therefore the amplitude fluctuation of any stable oscillator may be restored to the initial state but phase fluctuation persists indefinitely. The output of a practical oscillator may be expressed as:

$$v_{out}(t) = v_o\{1 + a(t)\}\, Sin\left[2\pi f_o t + \varphi(t)\right]. \quad \ldots (10)$$

where $a(t)$ and $\varphi(t)$ are function of time. The fluctuation presented by $a(t)$ and $\varphi(t)$ is an inherent problem of all physical oscillators. The popular techniques for characterizing these output fluctuation, i.e., spectral dispersion and timing uncertainty of practical oscillators are termed as phase noise and timing jitter respectively. Phase noise is a frequency-domain view of the noise spectrum around the oscillator signal, while jitter is a time-domain measure of the timing accuracy of the transition edge.

4.1 Phase noise

The power spectral density $S_\varphi(f_{off})$ of phase fluctuation $\varphi(t)$ is difficult to measure directly by spectrum analyzer. Generally, one measures the normalized single sideband noise spectral density defined by Hajimiri and Lee[1] and may be expressed as:

$$L(f_{off}) = \left[\frac{P_{sid}(f_o + f_{off},\ 1Hz)}{P_c}\right] \quad \ldots (11)$$

where $P_{sid}(f_o+f_{off}, 1\text{Hz})$ represents the single sideband power at a frequency offset f_{off} from the carrier in a measurement bandwidth of 1Hz as shown in Fig. 7. The P_c is the total power under the power spectrum. The unit of $L(f_{off})$ is decibel below the carrier per hertz (dBc/Hz). At frequencies where $S_\varphi(f_{off})$ is small, it is twice that of the single sideband (SSB) phase noise.

$$S_\varphi(f_{off}) = 2\,L(f_{off}) \quad \ldots (12)$$

If one considers only white noise source (thermal and shot noise) in the oscillating system, then Eq. (12) can be expressed as reported by Herzel & Razavi[10] as:

$$S_\varphi(f_{off}) = \frac{D_\varphi}{2\pi^2 f_{off}^2} \quad \ldots (13)$$

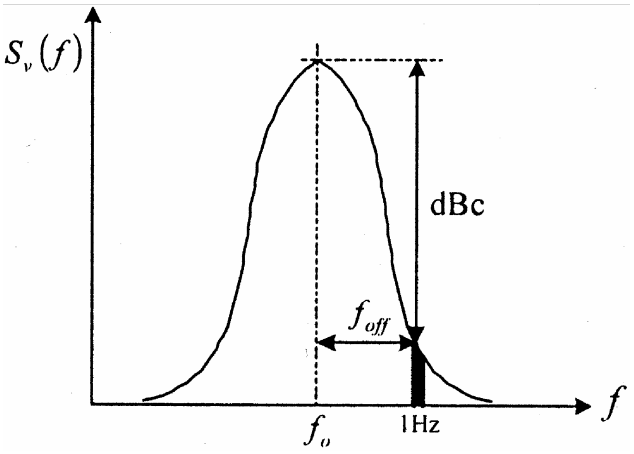

Fig. 7 — Illustration of phase noise per unit bandwidth

where D_φ is the phase diffusivity. Thus power spectral density (PSD) of noise is proportional to $1/f^2_{off}$ for white noise source. If flicker noise source are present in the oscillator circuit, then phase noise would be proportional to $1/f^3_{off}$ for small offset frequency f_{off}.

4.2 Timing jitter

In an ideal oscillator, the zero crossing of the rising edge happens after a fixed time interval, for example the rising edge of the n-th period takes place at nT, where T is the constant time period of the oscillator. However, in presence of noise, T becomes a function of n, denoted by T_n. This results in a time deviation of $\Delta T_n = T_n - \overline{T}$ from the mean period $\overline{T}$ at every cycle. This deviation (or jitter) ΔT_n can be expressed as absolute jitter or long-term jitter[10] [Fig. 8(a)] as:

$$\Delta T_{abs} = \sum_{n=1}^{N} \Delta T_n\ . \quad \ldots (14)$$

This value varies with the observation time ($t = NT_n$), and the variance of this measure diverges as t goes to infinity. This is not a very useful measure for free-running oscillators as it increases with time. This measure is more often used with phase locked loops (PLLs), because a PLL has a phase reference source that resets the jitter, which a free-running oscillator does not have. The root mean square cycle jitter measures the variance of each period to the average period and it is defined as:

$$\Delta T_c = \lim_{N\to\infty} \sqrt{\frac{1}{N}\sum_{n=1}^{N} \Delta T_n^2}\ . \quad \ldots (15)$$

The root mean square (rms) cycle-to-cycle jitter Fig. 8(b) measures the variance between successive periods. This is defined as:

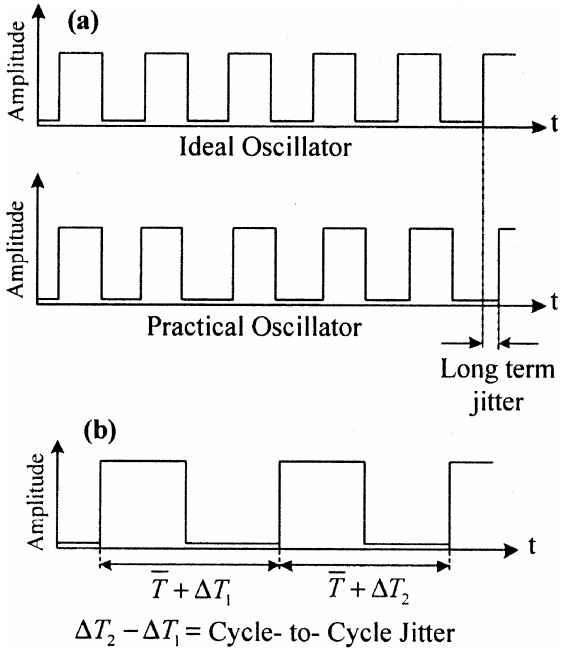

Fig. 8 — Illustration of jitter (a) long-term jitter and (b) cycle-to-cycle jitter

$$\Delta T_{cc}=\lim_{N\to\infty}\sqrt{\frac{1}{N}\sum_{n=1}^{N}\left(T_{n+1}-T_n\right)^2}\ . \qquad \ldots (16)$$

The measurement of rms cycle jitter and rms cycle-to-cycle jitter is more meaningful for a free running oscillator rather than an oscillator in PLL.

On the other hand jitter is a statistical measure of a noisy oscillation process. The statistics of the timing jitter depends on the correlations among the noise sources involved in the oscillating system. Generally, jitter is defined as the standard deviation ($\sigma_{\Delta T_{abs}}$) of the absolute jitter. In the case of independent noise sources (white noise), $\sigma_{\Delta T_{abs}}$ is proportional to the square root of the measurement interval ΔT[11] as:

$$\sigma_{\Delta T_{abs}}=\kappa\sqrt{\Delta T} \qquad \ldots (17)$$

where κ is a proportionality constant determined by the circuit parameters. If the noise sources (supply noise and substrate noise) are totally correlated with one another then the $\sigma_{\Delta T_{abs}}$ is proportional to the ΔT (Ref. 1),

$$\sigma_{\Delta T_{abs}}=\varsigma\,\Delta T \qquad \ldots (18)$$

where ς is another proportionality constant. In practical oscillating system both correlated and uncorrelated noise sources are present. Thus a log-log plot of $\sigma_{\Delta T_{abs}}$ verses ΔT for a free running oscillator shows two regions with a slope of 0.5 and 1 corresponding to κ and ς, as shown in Fig. 9.

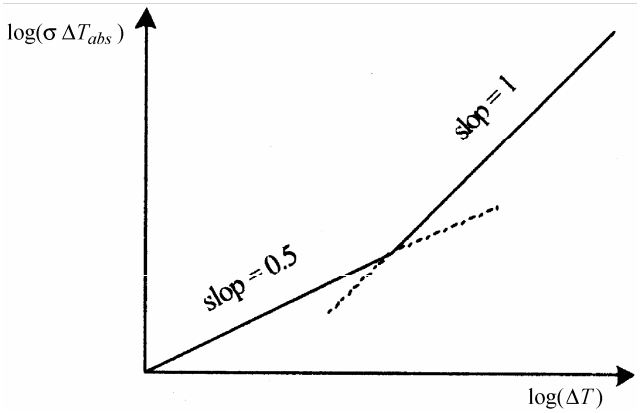

Fig. 9 — Variation of rms jitter with measurement time interval in log-log scale

4.3 Relationship between phase noise and timing jitter

Since phase noise and jitter characterize the same noisy oscillation process, the relationship between them is important to convert one to the other. In digital application, it is desirable that $\sigma_{\Delta T_{abs}}$ decreases with the same rate as that of the period T, with a view to keeping constant the ratio of the timing jitter to the period. Therefore phase jitter in terms of timing jitter is defined as reported by Hajimiri and Lee[1] as:

$$\sigma_{\Delta\varphi_{abs}}=2\pi\frac{\sigma_{\Delta T_{abs}}}{T}=2\pi f_o\sigma_{\Delta T_{abs}}\ . \qquad \ldots (19)$$

Next consider the relationship between cycle jitter/cycle-to-cycle jitter and power spectral density of phase noise. According to Herzel and Razavi[10] one can write the following expressions

$$\Delta T_c=\kappa\sqrt{\overline{T}}\ . \qquad \ldots (20)$$

$$\Delta T_{cc}=\sqrt{2}\,\Delta T_c\ . \qquad \ldots (21)$$

$$\kappa=\frac{\sqrt{2D_\varphi}}{2\pi f_o}\ . \qquad \ldots (22)$$

Combining Eqs (13), (17) and (22), one obtains

$$\sigma_{\Delta T_{abs}}=\frac{f_{off}}{f_o}\sqrt{S_\varphi\left(f_{off}\right)}\sqrt{\Delta T}\ . \qquad \ldots (23)$$

Combining Eqs (13), (20) and (22), one obtains

$$\Delta T_{\mathrm{c}} = \frac{f_{\mathrm{off}}}{f_{\mathrm{o}}} \sqrt{S_{\varphi}(f_{\mathrm{off}})} \sqrt{T} \; . \qquad \ldots (24)$$

Similarly,

$$\Delta T_{\mathrm{cc}} = \frac{f_{\mathrm{off}}}{f_{\mathrm{o}}} \sqrt{S_{\varphi}(f_{\mathrm{off}})} \sqrt{2} \sqrt{T} \; . \qquad \ldots (25)$$

Eqs (23) to (25) show the relationship between phase noise and jitter and at the same time also describe the interrelationship among the absolute jitter, cycle jitter and cycle-to-cycle jitter.

4.4 Phase noise and timing jitter in ring oscillator

The analysis of noise in ring oscillator is different from other oscillators like sinusoidal oscillators and relaxation oscillators. A harmonic oscillator is characterized by an equivalence to two energy storage elements, operating in resonance, to give a periodic output signal. The actual resonant element might be a LC tank or a quartz crystal. A relaxation (multivibrator) oscillator is characterized by an equivalence to one energy storage element, and relies on the additional circuitry that senses the element state and controls its excitation to give a periodic output signal. The ring oscillators have the advantage that they do not require any kind of resonator and have a large tuning range, but their frequency and phase characteristics are somewhat poorer than those of high *Q*-resonator based oscillators. Like the multivibrator, a ring oscillator is fully integrable in nature but the basic difference between them is the number of energy storage elements present in the oscillator circuit. The number of energy storage elements is not explicit in ring oscillator; in fact there are many energy storage elements since the ring is composed of multiple stages. However, relaxation oscillator is an integrated nature but ring oscillator does not fit well into the model of relaxation oscillator.

The effect of thermal noise on timing jitter in CMOS differential delay cell based ring oscillator was described by Weigandt *et al*[12]. This study established the following points: The timing jitter is inversely proportional to the total capacitive load at the output of each delay stage and inversely proportional to the gate-source bias voltage above threshold for the balanced state. Timing jitter and power consumption of a ring oscillator has an inverse relationship between them for fixed output period. The total jitter variance for one cycle of oscillation is proportional to *m* for *m*-stage ring oscillator provided noise sources are uncorrelated. The rms timing jitter[13] of ring oscillator based PLL is greater than the intrinsic jitter in the inverter chain.

Studies on phase noise and timing jitter of CMOS differential ring oscillator was reported by Herzel and Razavi[10]. The results obtained in this study are as follows: The nonlinearity of the delay stage and the unwanted fluctuation of tail current due to supply and substrate noise increases phase noise of the oscillator output. Jitter increases almost linearly with the increase of supply and substrate voltage noise frequency. The increase of transistor gate width of the CMOS inverter and the number of inverters in the ring structure increases jitter of the oscillator output. But the phase noise and jitter decreases with the increase of power consumption of the oscillator for fixed period oscillation as reported in earlier research works[12].

McNeill[11] described timing jitter due to circuit parameters and circuit level noise sources (thermal and shot noise) in ring oscillator composed of bipolar differential pair delay stages. Jitter due to collector resistance of the delay stage is proportional to the square root of the thermal energy divided by the power dissipation in the collector resistance. Therefore power dissipation in collector load reduces oscillator jitter. But thermal noise of the base resistance of the delay stage increases oscillator jitter. The fluctuation of tail current due to thermal and shot noise increases oscillator jitter but increase in tail current means delay stage dissipates more power, which leads to the improvement in jitter performance. Another important investigation of this article is that jitter does not depend on the number of stages of the ring oscillator. To understand this conclusion (verified through hardware experiment by the author of this paper) one must consider the jitter accumulation process around the ring. There is only one delay stage, which during the process of transition, affects jitter accumulation at a given instant and all other stages in the ring are inactive and do not contribute to jitter. Thus from the stand point of jitter accumulation, the key measure is the number of stage transitions, not the number of oscillator periods. Thus measure of total jitter variance normalized to the oscillator period are not independent of the number of stages as reported by Weigandt *et al*[12].

Phase noise and timing jitter of CMOS single-ended ring oscillators and differential ring oscillators were reported by Hajimiri and Lee[1]. From this analysis, one can conclude the following points:

Phase noise is inversely proportional to the power consumption of the single ended ring oscillator (SERO) and differential-pair ring oscillator (DRO) and it increases quadratically with the oscillation frequency. The timing jitter is inversely proportional to the square root of the power dissipation by the SERO and DRO. Phase noise and timing jitter depend on the number of stages of the DRO but they have no such dependency on the number of stages of the SERO. DRO has lower sensitivity to substrate and supply noise in comparison with SERO. DRO injects relatively low noise into the other circuit components on the same chip in comparison with SERO.

Study of phase noise in CMOS differential ring oscillator was described by Dai and Harjani[14]. From this analysis one can note that phase noise is proportional to $1/V^2_{pp}$ for linear operation and $1/V^3_{pp}$ when output voltage swing is clipped by the power supplies of the oscillator. Here V_{pp} is the peak-to-peak voltage swing of the oscillator output. Thermal noise and flicker noise of the biasing circuit of the differential delay stages increases phase noise at the oscillator output.

Recently, timing jitter and phase noise in CMOS ring oscillator have been studied and reported by Abidi[15] due to white noise and flicker noise. White noise in the differential pairs dominates the jitter and phase noise, whereas the phase noise due to flicker noise arises mainly from the tail current control circuit. The analysis shows that jitter and phase noise is independent of the number of stages due to white noise. But phase noise is proportional to f^2_{off} and f^3_{off} for white noise and flicker noise, respectively.

The analysis of phase noise and timing jitter in ring oscillator mainly from the viewpoint of circuit parameters and deterministic and random perturbations has been summarized. But the treatment of phase noise and timing jitter from the viewpoint of probability theory, stochastic theory and numerical methods are also reported[16].

5 Applications of Ring Oscillators

Wide voltage tuning range of ring oscillators are particularly attractive for PLL based frequency synthesis and clock signal generation required by many applications like frequency synthesizer and data clock recovery circuits for serial data communication. Sarkar and Mandal[17] reported a ring oscillator based indirect frequency synthesizer. A variable length ring oscillator with voltage tuning range of 1.2 to 5.6 MHz is used to synthesized different harmonics of the input reference signal of frequency 120 KHz. On the other hand, a variable length ring oscillator based PLL is also described by Mandal and Sarkar[18] to demodulate FM signal, whose carrier frequency can change with in the locked range from 1 to 6 MHz of the PLL. Kim *et al*.[19] described a high speed clock recovery circuit comprising of a CMOS ring oscillator based PLL, which is locked to the reference clock signal of 30 MHz for disk drive application. Enam and Abidi[20] used a NMOS ring oscillator based PLL, which is capable to reconstruct the clock signal of frequency near 1 GHz from the input nonreturn-to-zero (NRZ) data stream for optical fiber receiver. An architecture of high performance PLL based frequency and phase synthesis circuit is described by Mair and Xiu[21]. The voltage control oscillator used by them in the PLL is a 32-stages inverter based ring oscillator. This ring oscillator oscillates at a single frequency of 114.5454 MHz and additional logic circuit select one of the proper phase shifted output from 32 different phase shifted signal to synthesize required frequency and phase depending on the frequency and phase control data. Ring oscillators have not only wide voltage tuning range but also have multiphase outputs, which is an unique feature of ring oscillators. These outputs of ring oscillators have wide applications in frequency synthesis and in clock recovery circuits. Sarkar and Mandal[22] described a direct digital frequency synthesizer based on accumulator and phase register. The clock signal used in the phase register is taken from a 15-stages inverter based ring oscillator. A technique of time period modification of this clock signal is proposed here by selecting different phase shifted signal of the ring oscillator with the half of a multiplexer to synthesize fixed period signal. A charge pump phase locked loop (CP-PLL), comprising of a ring oscillator is described by Mandal and Sarkar[23] to extract continuous carrier signal from burst like input signal. In this techniques different phase shifted output of the ring oscillator are used to detect the time interval of transition missing of the input burst like signal and after detecting transition missing additional logic circuit will stop the operation of the CP-PLL instantaneously providing satisfactory output of the CP-PLL. A fully integrated PLL has been designed by Young *et al*.[24] for on-chip clock distribution in microprocessor. The voltage controlled oscillator used by them is a 5-stages differential inverter based ring oscillator, which is capable of producing the clock frequency range 5 to 110 MHz with a peak-to-peak jitter less than 0.3ns for a 50 MHz clock frequency. A novel technique of pulse width modulator design is also proposed by Sarkar & Mandal[25] by using a multiphase ring

oscillator and a multiplexer-based digitally controlled phase shifter (DCPS). Different phase shifted outputs of the ring oscillator are used to produce 0 to 100 % variation of the width of the pulse train, depending on the control word applied to DCPS. Beside these ring oscillators are important for low cost and low power consumption applications in integrated circuits and systems.

6 Discussion

The oscillation frequency of an RO depends on the propagation delay of the inverter stages. The smallest propagation delay time is determined by the structure of the inverter stage, process parameters and design technology and it can be increased by incorporating additional voltage control delay (may be capacitive or resistive-capacitive load) at the output of the inverter stage. This property makes them useful in PLL as a VCO. A few modified ring topologies are also described here. In those structures care has been taken to reduce the average propagation delay time of inverter stage to achieve high frequency oscillation as well as multiphase outputs. Some coupled ring topologies using single ended inverters are also described. These have been designed to generate quadrature outputs which are not the general features of SERO but it is available in DRO. Couple ring oscillator based array oscillator which is useful for producing precise delay has also been mentioned. This precise delay signal has potential applications in digital electronics for testing different ICs.

Further, phase noise and timing jitter which are very important parameters used to measure the output fluctuation of a noisy oscillator are also described in this paper. This output fluctuation arises due to the presence of unwanted noise sources in the oscillator circuit. The effect of noise sources on phase noise and timing jitter in ring oscillators which are designed using different technologies such as bipolar, CMOS are also summarized here. From this study one can note the following points: (i) Noise sources affect the phase and amplitude of the ring oscillator output; (ii) Phase noise and timing jitter decrease with the increase of power consumption of the oscillator circuit for fixed frequency oscillation; (iii) Phase noise and timing jitter[20] depend on the number of stages in DROs and there is no such dependency in case of SEROs; (iv) Supply and substrate noise have worse effect on SEROs and this effect is small in DROs because it has high common noise rejection; and (v) Timing jitter and phase noise is independent of the number of stages due to white noise. But phase noise is proportional to f^2_{ff} and f^3_{off} for white noise and flicker noise respectively.

Extensive study on ring oscillators reported here indicates that a good amount of work has been done in the recent past on ring oscillators for the following purposes: (i) To understand the physics of oscillation of a ring oscillator; (ii) To design improved performance ring oscillators having electrical tuning capability in the higher part of the EM spectrum; and (iii) To identify the causes of phase noise and jitter at the output of the ring oscillator.

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