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Ground Bounce in 8-Bit High-Speed Logic

Today's demand for higher speed systems is for increased performance, but with strong consideration for power usage. Traditionally, high-drive bus interface logic has been implemented in Bipolar technology, but recent years have witnessed strong demand for a CMOS counterpart series called FCT. In fact, FCT has evolved to deliver far greater performance (shorter propagation delays) than is available in Bipolar technology, thus becoming the only available avenue for very high-speed system designers. Maintaining the same high output drive capabilities as Bipolar products (64mA sink), FCT circuits from Pericom are available with propagation delays down to 3.6ns (maximum) for some functions. However, speed improvements and power reduction come with some penalties, i.e.,noise phenomena called "Ground Bounce."

Ground Bounce is the simultaneous switching noise of outputs during the logic HIGH to LOW transition and the resultant potential difference between the chip ground and the external ground plane. When several outputs switch simultaneously, the total build up of current in the common ground or V_{CC} lead inductance can be substantial. The noise becomes more pronounced as the output edge rate and the drive capability increase or as more current is switched through the ground lead.

Pericom Semiconductor's FCT products, designed to have low ground bounce are TTL compatible and limit the output swing to 3.4 volts instead of 5 volts. This reduces the discharge current through the ground lead and reduces maximum noise by 30 to 40 percent. To reduce ground bounce while achieving high speeds, specially optimized control circuits are designed to gradually turn-on the output driver. Optimized layout of the power and ground lines in the chip further reduces ground bounce.

Ground bounce and speed characterization were done on a special bench setup as shown in Figure 1. Ground bounce measurement was done with seven bits simultaneously driven from logic HIGH to logic LOW and the remaining bit tied to ground. The noise voltage waveform generated at the undriven bit (quiet bit) is measured and represents the worst case ground bounce noise. This is the standard setup and measurement in characterizing ground bounce. On system boards, with proper board design, the noise characteristics are usually much lower.

An FCT244 device in a plastic DIP package from Pericom Semiconductor and two other suppliers were characterized with the setup as shown in Figure 1. Figures 2 and 3 compare the waveforms of the output voltage transitions and the corresponding ground bounce as observed at the undriven LOW output. Table 1 summarizes the results. The results show that Pericom Semiconductor's FCT device has significantly lower ground bounce compared to the other suppliers.

Note:
Contact factory for double density 16-bit FCT ground bounce data.

Key to High Speed Low Noise Design
Because parasitic inductance cannot be totally removed from the package, ground bounce can be minimized or circumvented, but rarely eliminated. Figure 4 shows a simplified circuit model of several key factors critical for good ground bounce control design.

During the output HIGH to LOW transition, the sum of output load current and all switching current through the device flows through the ground lead and generates noise voltage. Several factors affect the amplitude of this voltage:

- **Number of outputs switching simultaneously.** The more outputs switching simultaneously, the more ground bounce.
- **Magnitude of lead inductance.** Higher lead inductance results in greater ground bounce. A package with less parasitic ground lead inductance gets better noise performance.
- **Output voltage swing.** A higher output voltage swing would result in higher ground bounce. Thus, a CMOS compatible output with 5 volts V_{OH} would inherently result in higher noise than a TTL compatible output with lower V_{OH} voltage.
- **Output edge rate.** Output edge rate determines how fast current discharges through the ground lead inductor. Since transient voltage across an inductor increases with current rate of change, the faster the rate, higher the noise. To get low noise performance, output edge rate must be controlled.
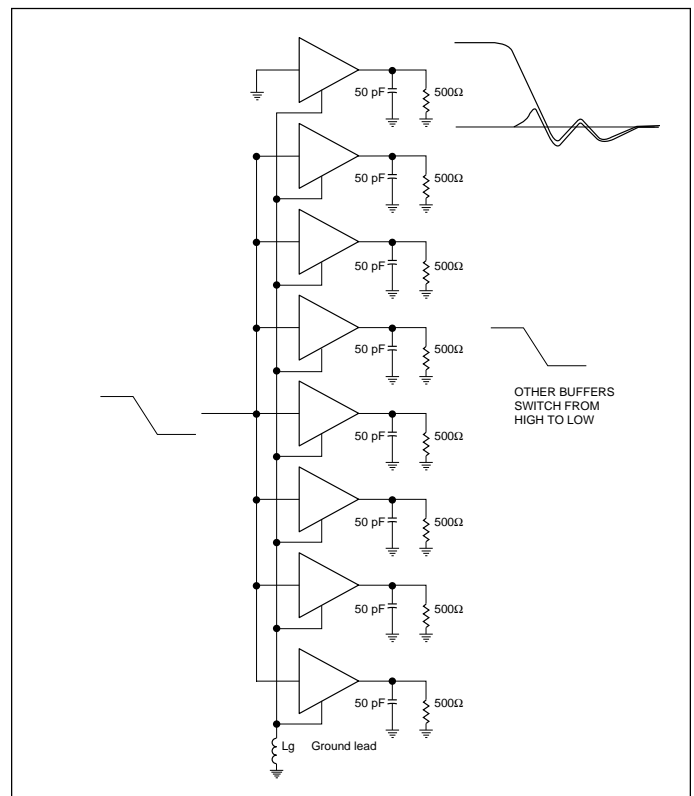

*Figure 1. Typical Ground Bounce Evaluation Setup.*

Pericom Semiconductor addresses these issues directly at the outset of the design. First, we design our FCT products to be TTL compatible. This limits the output swing to 3.4 volts instead of 5 volts, reducing the maximum noise as the maximum output swing is lowered. To control the output edge rate without compromising speed, a proprietary control circuit is designed to gradually turn on the output driver to optimize the speed performance and ground bounce characteristics. Also, alternative package choices complement the high-speed low-noise design. Plastic DIP packages have the highest lead inductance and hence, the worst ground bounce characteristics. Packages like SOIC and QSOP have much lower lead inductance and hence, much lower ground bounce. Table 2 shows a comparison of package inductance and estimated ground bounce. It is evident that the surface mount packages (SOIC, QSOP) offer system designers the advantages of reduced board space, higher speed performance and lower ground bounce.

Table 1. Ground Bounce Comparison at Room Temperature. Pericom Semiconductor vs. Competitors 1 and 2

Unit	Speed (ns)		Ground Bounce (V)	
	T$_{PHL}$	T$_{PLH}$	Pos.	Neg.
PSC, D Speed	2.84	2.88	1.52	1.28
Comp. 1, D Speed	2.92	3.08	2.04	1.88
PSC, C Speed	3.2	3.4	1.32	1.00
Comp. 2, C Speed	3.24	3.84	1.52	1.34
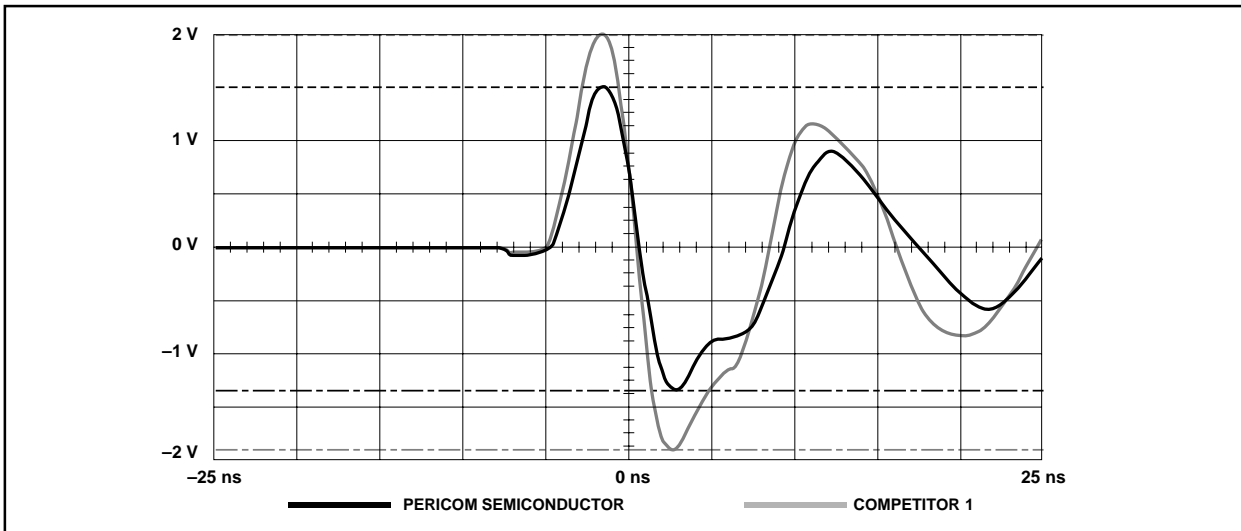
Figure 2. Ground Bounce Waveforms: Pericom Semiconductor vs. Competitor
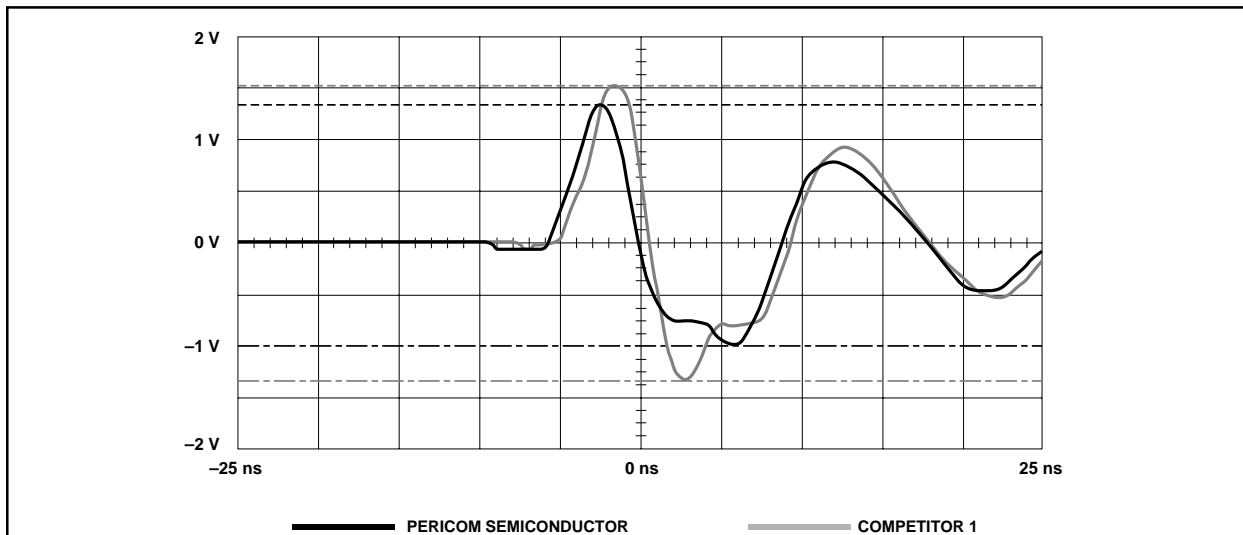
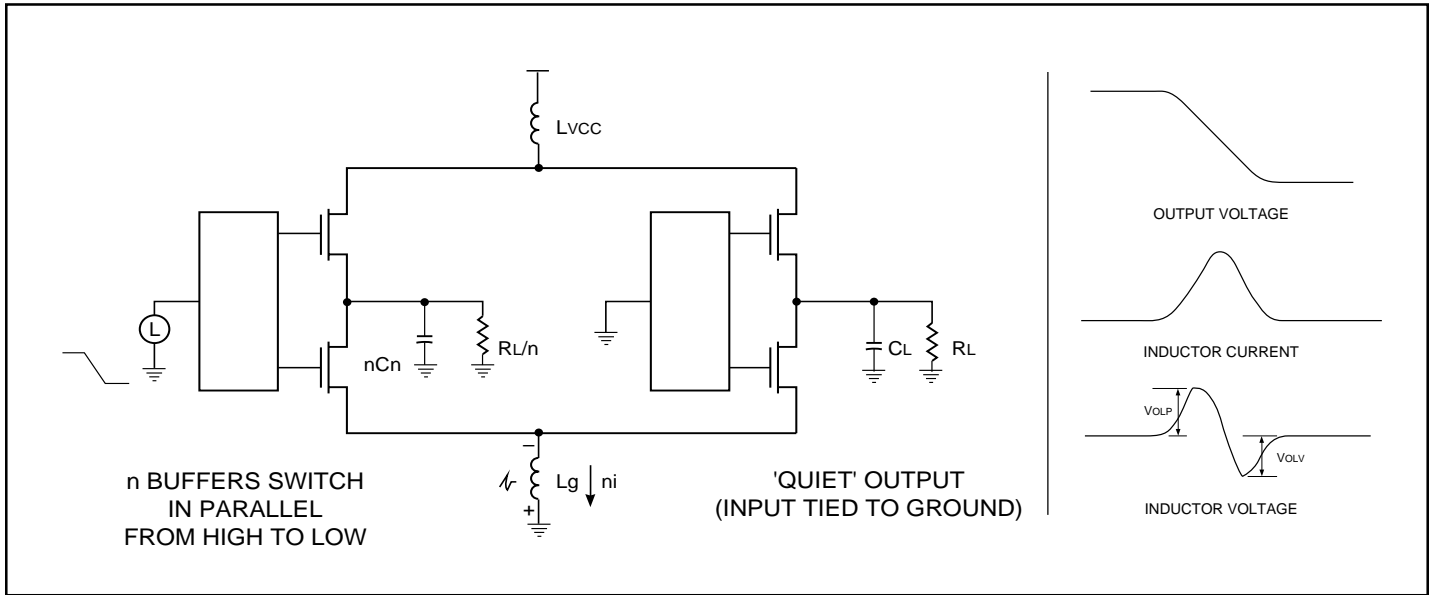*Figure 3. Ground Bounce Waveforms: Pericom Semiconductor vs. Competitor 2*

Figure 4. Simplified Circuit Model

Table 2. Ground Bounce Package Comparison

Ground Lead Package	Relative Inductance	Ground Bounce
PDIP	13.7nH	100%
SOIC	8.5nH	80%
QSOP	3.6nH	50%