SPARC T4 PROCESSOR

SPARC T4 KEY FEATURES

- Integrated and scalable enterprise server compute engine
- 8 SPARC V9 cores with full binary compatibility
- Private 128K Level 2 Cache per core and shared 4MB Level 3 Cache
- Supports up to 64 compute threads
- Dual, multithreaded, on-chip 10GbE ports
- Cryptographic Instruction Accelerators integrated in the pipeline
- Oracle Solaris guaranteed binary compatibility

KEY BENEFITS

- Five times increase in single-thread performance over previous generation
- Scales to cost-effectively meet needs of growing data center requirements
- Integrated cryptographic processing provides wire speed security capabilities without impact on primary workloads
- Built-in virtualization technology enables dynamic scaling, increased resource utilization, and simpler operations
- On-chip networking functionality supports high capacity, network-intensive content and eliminates storage bottlenecks

Oracle's SPARC T4 processor combines optimized performance on single-threaded and cryptographic workloads with high throughput performance, creating a scalable system-on-a-chip ideal for mission-critical applications.

Figure 1. The SPARC T4 processor features 8 cores and 64 threads with 5x the single thread performance of the previous generation

SPARC T4 Processor Overview

Oracle's SPARC T4 processor is a design breakthrough that delivers a five times increase in single-thread performance over the previous generation, while maintaining the high throughput performance that has historically distinguished the SPARC T-series. Featuring eight complex cores, deeper pipelines, out-of-order execution, instruction retry, sophisticated branch prediction, dedicated 128K L2 cache per core, 4MB shared L3 cache, and a higher frequency (2.85GHz or 3.0GHz) clock, the SPARC T4 delivers the horsepower demanded by next generation datacenter applications. The SPARC T-4 processor core pipeline is designed to automatically switch to single-thread mode when only a single thread is active – meaning all of the resources of the core are dedicated to that thread's execution. With faster single-threaded processing, the SPARC T4 enables shorter application boot times and rapid batch processing while maintaining stunning throughput performance, making it the ideal platform for consolidation and virtualization of legacy architectures.

The SPARC T4 processor was designed from the ground up with security as a focus and has Crypto Instruction Accelerators integrated directly into each processor core. These accelerators enable high-speed encryption for over a dozen industry standard ciphers including DES, 3DES, AES, SSL, and RSA. By integrating encryption capabilities directly inside the instruction pipeline the SPARC T4 processor eliminates the performance and cost barriers typically associated with secure computing.

The SPARC T4 processor was developed to be a true system-on-a-chip functionality. By

integrating system level features such as high speed 10 GbE networking directly on to the silicon, applications perform more efficiently while overall system reliability is improved due to reduced part count in the server. By leveraging the unique, no-cost capabilities of Solaris Containers and Oracle VM for SPARC, the SPARC T4 processor enables customers to run up to 64 domains on one processor - improving system utilization, reducing hardware acquisition costs, and minimizing operational complexity.

SPARC T4 Processor Features and Specifications

Processor Features
• 8 SPARC V9 cores • Die size 403 mm^2 • Frequency: 2.85 GHz and 3.0 GHz • 40nm process technology • Up to 64 threads per CPU • Up to 16 DDR3 DIMMs per T4 supporting DDR3 1066 MHz memory • Scalability up to 4 sockets with no additional silicon necessary • Cryptographic Instruction Accelerators directly accessible through direct non-privileged access crypto instructions • 128 KB Level 2 Cache per core • 4 MB, 8 banked, 16 way associative Level 3 Cache • Max power 240W • Dual 10 GbE XAUI Network Interface Units integrated on chip • Dual PCI Express Generation 2 x8 interfaces integrated in silicon • New on-chip Encryption Instruction Accelerators with direct non-privileged support for 16 industry-standard cryptographic algorithms plus random number generation in each of the eight cores: AES, Camellia, CRC32c, DES, 3DES, DH, DSA, ECC, Kasumi, MD5, RSA, SHA-1, SHA-224, SHA-256, SHA-384, SHA-512

T4 Core Specifications	
• 15.4 mm^2 core size • 8 threads • 2 out-of-order integer execution pipelines, one floating-point unit (FGU), and Cryptographic Instruction Accelerators integrated in the pipelines	• 16 KB data cache and 16 KB instruction cache • Sophisticated branch predictor • Hardware data prefetcher

Oracle Hardware Warranty

Visit http://www.oracle.com/us/support/policies/index.html for more information about Oracle's hardware warranty for the SPARC T4 processor.

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