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# Fine grain thermal modeling and experimental validation of 3D-ICs

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ABSTRACT

3D die stacking is a promising technique to allow miniaturization and performance enhancement of electronic systems. Key technologies for realizing 3D interconnect schemes are the realization of vertical connections, either through the Si die or through the multilayer interconnections. The complexity of these structures combined with reduced thermal spreading in the thinned dies complicate the thermal analysis of a stacked die structure. In this paper a methodology is presented to perform a detailed thermal analysis of stacked die packages including the complete back end of line structure (BEOL), interconnection between the dies and the complete electrical design layout of all the stacked dies. The calculations are performed by 3D numerical techniques and the approach allows importing the full electrical design of all the dies in the stack. The methodology is demonstrated on a 2 stacked die structure in a BGA package. For this case the influence of through-Si vias (TSVs) on the temperature distribution is studied. The modeling results are experimentally validated with a dedicated test vehicle. A thermal test chip with integrated heaters and diodes as thermals sensors is used to successfully validate the detailed temperature profile of the hot spots in the top die of the die stack.
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## 1. Introduction

General trends in microelectronics show increase in functionality and power dissipation combined with an ongoing miniaturization [1]. These trends lead to increasing power densities in the dies. As a result these elevate power densities might give rise to excessive operating temperatures, which influence the electrical performance and reliability of the device. 3D stacking of dies is an enabler for further miniaturization and increase of functionality [2]. Here the individual dies are thinned down aggressively – down to about 20 μm – and are glued on top of each other. In the case of such 3D stacks even more thermal issues appear [3]. The glue used to bond the dies together typically is poorly conductive. Furthermore the thinned dies will only allow a reduced thermal spreading effect compared with full thickness dies. Therefore the same dissipation will lead to higher temperatures in a stacked die package compared with a single die package. Other aspects to be considered are multiple localized areas of heat dissipation in the different dies, the complex interconnection schemes between and/or through the dies which allow multiple paths for the heat flow and the complicated back end of line (BEOL) structure metal and oxides. In the case of a full thickness die the thermal influence of the BEOL is limited on temperature distribution in the conductive silicon. However in the case of thinned dies the thickness of the BEOL can be of the same order as the thickness of the Si itself (up to 10 μm thickness for a 10 metal layer BEOL structure), and should be included in the thermal analysis.

Therefore there is a need to perform a thermal analysis including the structure of the BEOL and the location of all the power sources in the layout. Furthermore the thermal analysis should be included in the design loop to assess the thermal consequences of design iterations and verify the final design before sign-off. Turowski et al. [5] presented a multiscale analysis for a single die. [3, 6–8] present a compact model approach using transfer functions for a thermal analysis on a higher level of abstraction for a stacked die structure. In this paper a methodology is presented for a full detail analysis based for stacked dies on the design layout of all the stacked dies. In this approach Cadence Virtuoso™ is used for the layout design and the thermal simulator FireBolt™ [4] for the thermal analysis. At the different stages of the design flow, the requirements for the thermal analysis are different and a trade-off between the desired accuracy of the modeling approach and the required computational time should be made. In the initial stage of the design, many different configurations need to be explored in a path finding exercise and fast solving thermal simulation tools with acceptable accuracy are required. In this phase of the design, thermal compact models [14] could be used to assess the impact

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**Symbols and units**

$\mathbf{r} \equiv (x,y,z)$ Location (m)
$T$ Temperature (K)
$k$ Thermal conductivity (W/(mK))
$P_V$ Power density (W/m$^3$)
$S_i$ Area of face 'i' (m$^2$)
$h_i$ Heat transfer coefficient (W/(m$^2$K))
$c_i$ Thermal capacitance (J/K)
$\varphi$ Flux density (W/m$^2$)
3D-IC 3 dimensional (stacked) integrated circuit
BEOL Back End of Line structure
BGA Ball Grid Array
M2 Metal 2 layer of the BEOL structure
TSV Through-silicon via

of the several design choices. In later stages of the design loop, the number of design options is reduced and more modeling accuracy is desired. The very detailed modeling presented in this paper is aimed to be used at the final stage of the design process where is it used as a thermal verification of the complete design. For this final thermal check of the complete design with very high accuracy, a higher computational time is acceptable.

In Section 2 the general approach to perform the detailed simulations is explained. In Section 3, this approach is applied to a typical case of a two die stack with TSVs and integrated heaters and sensors. The results of these simulations are discussed in Section 4. In Section 5 the experimental validation is discussed. A dedicated thermal test vehicle and test chip are presented and the simulation results are compared with the experimental data.

## 2. Methodology

Fig. 1 shows an overview of the different steps in the methodology to perform a detailed thermal analysis including the full chip design. In the first step the main region of interest in the structure is selected. There is large difference in length scale in the thermal phenomena in the structure; from the heat generation at transistor level (submicron level) to the board level and ambient (cm-level). Therefore a partitioning is being made between the main region of interest, in which the full 3D thermal analysis will be performed numerically and the outside area which will be transformed to thermal boundary conditions for simulation in the internal part [9]. In this case the internal region, to be simulated in detail is the die stack and the interface layers and interconnections in between them.

The package (overmould, interposer,...), solder balls, PCB and ambient environment will be converted to a '*package model*' in a second step and will be used as boundary conditions for the

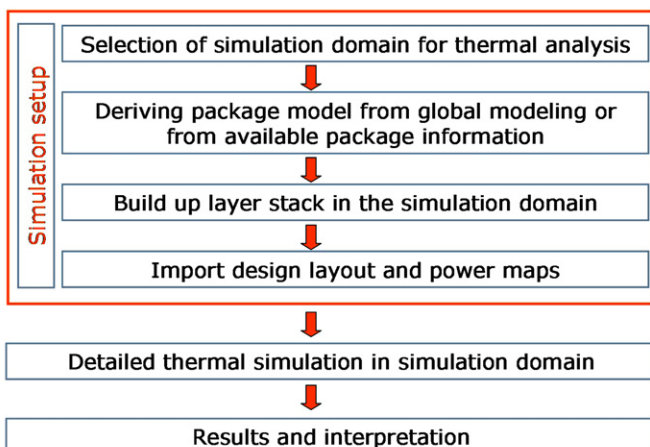


**Fig. 1.** Flow chart with the consequent step in the approach for detailed thermal modeling of a stacked die structure.

detailed simulation. This can be done using the thermal package properties in the data sheet or by extracting the information from a system (board) level simulation to estimate the heat flow through each of the sides. In this case steady state or transient boundary condition are extracted from the higher level simulation tool and represented as thermal RC networks to mimic the thermal behavior of the surrounding of the simulation domain. This RC representation is referred to as a '*package model*'. Depending on the structure of the package a more complex package model can be used to represent the external part of the structure to account for the local effect of wirebonds or solder balls.

The third step in the approach shown in Fig. 1 is the representation of the materials used in the die stack. Here all material properties, their temperature dependencies and the thickness of the respective layer are specified for the materials present in design layout files. This description of the layer stack links the design layout to the actual 3D simulation model. Fig. 2 shows a schematic representation of the preparation and transformation of the separate individual GDSII design files of all the dies in the stack to the representation of the 3D stacked structure. The process consists of several steps. After optional format conversion which translates data to the Cadence Virtuoso layout design tool, the layout is converted from a 2D to a 3D representation. This step brings back the stack hierarchy flattened in the post-layout design phase and opens space for possible thermal layout modifications (i.e. adding extra layers representing overmould). Next the inputs for the thermal simulator are added. These include the top level 3D description of the layout, the exact locations of the thermal sources and the monitors' location. The inputs are generated making use of automated Linux scripts. The rest of the input files which define the design layers, the material list, the thermal-layer list and the material-layer definition, are generated manually. When all information is assembled correctly the simulation domain is discretized using the thermal simulation tool FireBolt [4]. FireBolt [4] solves the heat diffusion equation [10], which in steady state, in Cartesian co-ordinates is

$$\nabla[k(\mathbf{r},T)\nabla T(\mathbf{r})]+P_V(\mathbf{r})=0 \quad (1)$$

where $\mathbf{r} \equiv (x,y,z)$ in (m), $T$ is the temperature (K), $k$ is the thermal conductivity (W/(mK)), and $P_V$ is the power density (W/m$^3$). Boundary conditions are expressed at the six die faces as described in "Package Model" Section 3.2. $P_V$ is considered invariant with temperature, assuming power values may be iteratively updated in an electro-thermal loop (not done in this case). Sub continuum heat-transport is modeled where required. FireBolt uses fast meshless methods for initial discretization of the 3D-IC, followed by refinement iterations in an adaptive, multi-level hierarchical modeler and solver. Simplification of the layout in a single die, or 3DIC, may result in significant errors in thermal simulation [11]. Even non-functional layout such as metal fill may significantly affect heat-transport in a chip. In FireBolt the 3DIC chip is modeled at the length-scales of its layout geometries, as needed to meet specified spatial and thermal error-tolerances.

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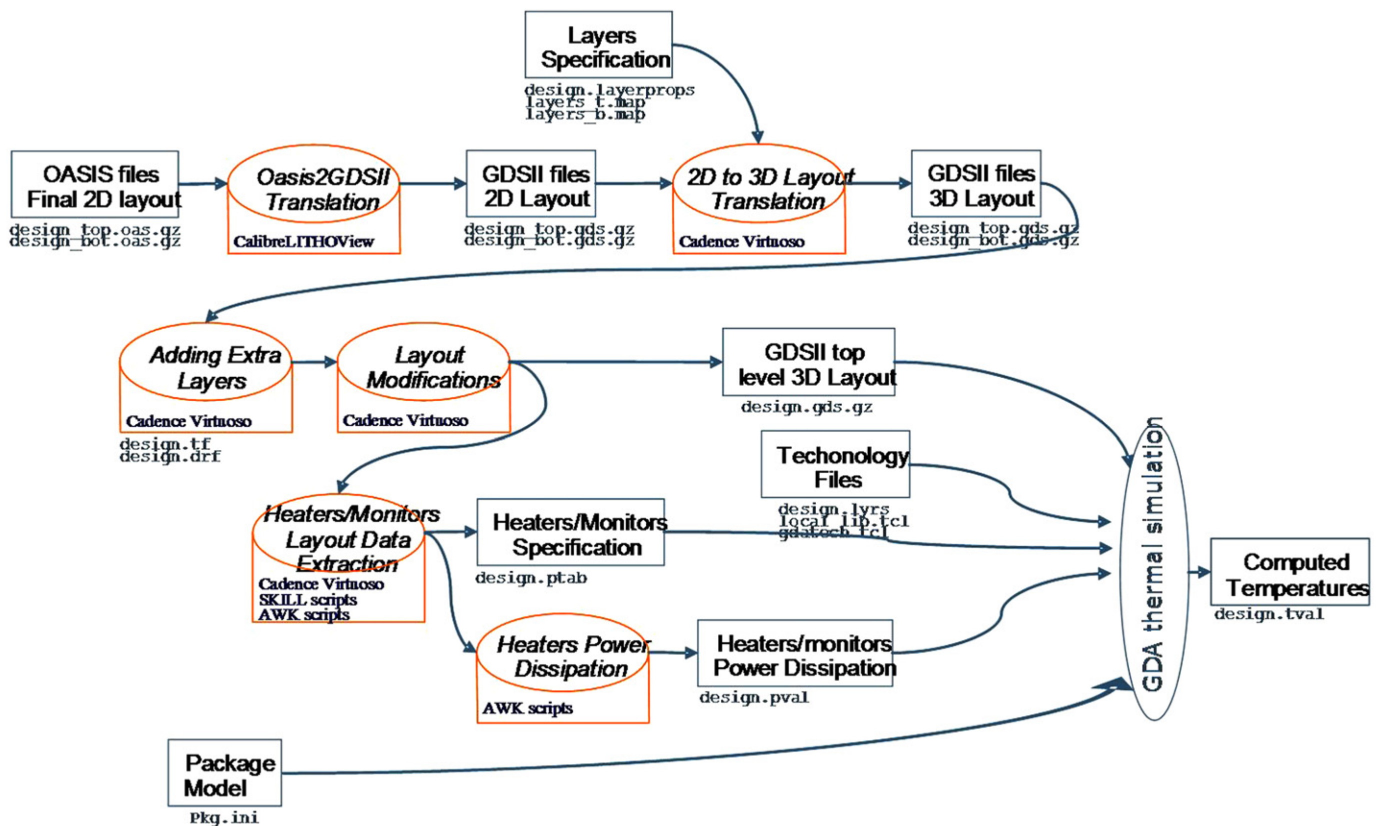


**Fig. 2.** Flow chart of the preparation procedure of the 3D layout design and material information to be used in the thermal simulation.

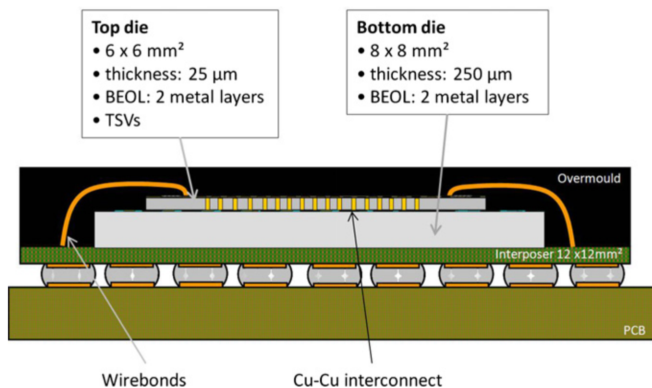


**Fig. 3.** Schematic of the test case of two stacked dies: a 25 μm thin top die $5 \times 5$ mm$^2$ with TSVs on top of a thicker 250 μm thick die $8 \times 8$ mm$^2$ in a BGA type package.

## 3. Case study: 2 stacked die structure

In this the section the general approach detailed thermal modeling presented in the previous section for is applied on specific 3D integrated structure. A schematic of the test case is shown in Fig. 3. The test case consists of a two die stacked structure in a BGA package. The BGA package in soldered to a PBC and the whole structure considered to be in an ambient environment of still air at 300 K. The top die is a 25 μm thick die, $5 \times 5$ mm$^2$ in size. The active region of the top die is connected to the bottom die by means of Cu through-Si vias (TSVs) through the top die [12]. These vias have a diameter of 5 μm. Several pitches of the TSVs are considered to study the effect of the TSV on the thermal behavior or the stack. The bottom die is an $8 \times 8$ mm$^2$ die with a thickness of 250 μm. The different steps of the procedure presented in Fig. 2 will now be dealt with in detail.

Thermal test structures are integrated in the top die of the stack. To dissipate heat meander resistor heaters in the metal 2 later of the BEOL of the top die are used. Diodes in both top and bottom die are used for the temperature measurements. The forward voltage drop over the diode is temperature dependent. If a constant current is applied through the diode the relation between voltage drop and temperature is linear and after calibration the diodes can be accurately used as thermometers. A constant diode current of 100 μA is used for the diode measurements since this dissipates a negligible power in the die, so that the die temperature is not affected. A lower current has a better '$V$–$T$' sensitivity, but the '$V$–$T$'-curves might become non-linear. Fig. 7 gives an overview of the location of the 6 heaters that are implemented on the top die. To study the thermal effect of the hot spot size, heater sizes of $50 \times 50$ and $100 \times 100$ μm$^2$ are used. Different TSV densities are used in the die locally below the heaters to characterize their ability to locally enhance the heat transfer: a reference structure without TSVs, an array of $7 \times 7$ TSVs (5%) and $12 \times 12$ TSVs (12%) are used. At each heater a set of set of 5 diodes at different distances (0, 60, 80, 120, 160 μm) from the hot spot center are added to capture the local temperature peak. This allows for characterization of the narrow temperature peak at the hot spot and the effect of hot spot size and interface layers on the peak shape. The position of diodes in the top die overlaps with diodes in the bottom to study the vertical heat conduction in the stack. This can be used to characterize the thermal properties of the polymer glue layer between the top and bottom die. With this set of diodes and heaters both the horizontal and vertical heat spreading in the stack can be accurately studied.

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### 3.1. Definition of the simulation domain

First the region of interest is selected in the structure. In this domain the detailed numerical simulation will be performed. In this test case the stack includes both Si die, the adhesive layer in between the dies. Also all the interconnections between the two dies and the complete back end of line structure (BEOL) of both dies are included in the model. To simplify the geometry of the simulation domain part of the overmould compound surrounding the top die is included in the model.

### 3.2. Package model

The region outside the simulation domain is converted to thermal boundaries conditions applied on the simulation domain. Inside FireBolt, the boundary conditions are formulated for each face $S_i$ with uniform heat transfer coefficient $h_i$ and thermal capacitance $c_i$ parameters as shown in the following equation where $\varphi$ is the flux density:

$$\varphi(\mathbf{r}_i) = h_i(T(\mathbf{r}_i) - T_A) + c_i \frac{dT(\mathbf{r}_i)}{dt} \text{ with } \mathbf{r}_i \in S_i \tag{2}$$

here the parameters of the package model are extracted from a full 3D finite element model of the package and PCB. For the finite element analysis the software tool Msc.Marc is used. From this thermal model the heat flow through each of the faces of the simulation domain can be obtained and converted to boundary conditions in the form of RC thermal networks, to be used in the detailed model.

The board level finite element of the structure can be seen in Fig. 4 (left). Fig. 4 (right) shows a schematic representation of RC networks as boundary conditions at the sides of the simulation domain. At the location of the wirebonds at the top the die stack and the solder balls at the bottom addition faces $S_i$ can be attributed with a local higher value of $h_i$, since the wirebonds and solder balls act as local heat sinks. Fig. 5 shows a bottom view of the distribution of the heat flow through the bottom of the considered simulation domain. Higher values of the heat flux at the bottom of the die stack can be observed at the locations corresponding with the placement of the solders balls.

### 3.3. Material layer stack information

In this step of the data preparation the information of the several materials and thickness of the respective material layers is included. Fig. 6 gives a schematic overview (not to scale) of the



**Fig. 5.** Distribution of the heat flux at one quarter of the bottom of the die stack extracted from the FE model of the package and PCB.



**Fig. 6.** Schematic representation of the materials in the die stack (not to scale), including the BEOL structure of the top and bottom die.



**Fig. 4.** Full 3D FE model of the package and PCB (left). Representation of the boundary conditions applied on the simulation domain (right).

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material layers and their respective thickness in the die stack. For both the top and the bottom die a BEOL structure with 2 metal layers is used.

The metal layers of the top die are connected to the metal layers of the bottom by TSVs (through-Si vias) through the thinned top die [12]. At the backside of the top die, the TSVs are connected to the metal 2 layer using thermo-compression Cu–Cu bonding.

### 3.4. Design layout and power sources location

The design layouts of both individual top dies are combined to a 3D design layout according to the procedure specified in Fig. 2. Fig. 7 shows the 3D design for this stack of a smaller die on top of a larger bottom die. In the figure the location of 6 heat sources in indicated. This heat sources are located in the 'metal 2' layer of the top die. In normal operation of logic dies the heat is generated in a region close to the top of the bulk of the Si. However in the thermal test chips available the metal meander resistors to dissipate the power are located in the 'metal 2' layer. To be able to validate the modeling experimentally the heat sources are therefore placed in the 'metal 2' layer in the model. In all heat sources a power of 10 mW is dissipated. This is a typical value of the power dissipation in structures in low power devices. For the 3 heat sources at the left side the area of the heat source is $100 \times 100\ \mu m^2$. At the right side of the top die, the same amount of heat is dissipated in areas of $50 \times 50\ \mu m^2$.

To study the influence of the TSV density on the temperature distribution different array densities of TSVs are placed right below the location of the heaters. The different densities are an array of $7 \times 7$, $11 \times 11$ and no TSVs in the area of $50 \times 50$ and $100 \times 100\ \mu m^2$ respectively. The locations of these TSVs areas are indicated on Fig. 7.

### 3.5. Thermal simulation

The 3D steady state heat equation is solved numerically in the simulation domain using the information of the package and environment as boundary conditions as shown in Fig. 4. A grid resolution matching the feature size in the design layout is used for the discretization. For this specific design a spatial resolution of 100 nm is used. Table 1 summarizes the numerical details of the simulations. 120 mW is dissipated in each of the heat sources in the metal 2 layer of the top die. The total power dissipated in the structure is $6 \times 120$ mW in the heat sources in the top die. The ambient temperature is considered to be 300 K.

Typical applications for 3D integration are stacks of memory and logic dies. For these applications, temperatures up to 85 °C can occur in the logic die. For these high power cases, the temperature dependence of the material properties should be considered. Due to this temperature dependence several iterations are required to meet the convergence criterion of 0.05 °C. For this case, with temperatures reaching 97 °C, two iterations are sufficient to meet this criterion. This amounts to a typical calculation time of 4 h 30 min. In the case of low power applications with operating temperatures below 50 °C, it is not necessary to include the temperature dependence of the thermal properties.

## 4. Discussion of simulation results

Fig. 8 shows the temperature distribution in the 'metal 2' layer of the top die. This is the layer where the power is dissipated. A sharp temperature peak can be observed at the location of the hot spots. As expected the temperature peak is higher in the smaller hot spots

**Table 1**
Simulation performance details.

| | |
|---|---|
| **Die size** | |
| *X* | 8.34 mm |
| *Y* | 8.34 mm |
| *Z* | 280.68 μm |
| **Power sources** | |
| Power level | 720 mW |
| No. of sources | 2100 |
| **Resolution** | |
| Thermal | 0.05 °C |
| Spatial | 100 nm |
| **Calculation** | |
| Runtime | ~4 h 30 min |
| Peak memory | ~5.8 Gb |

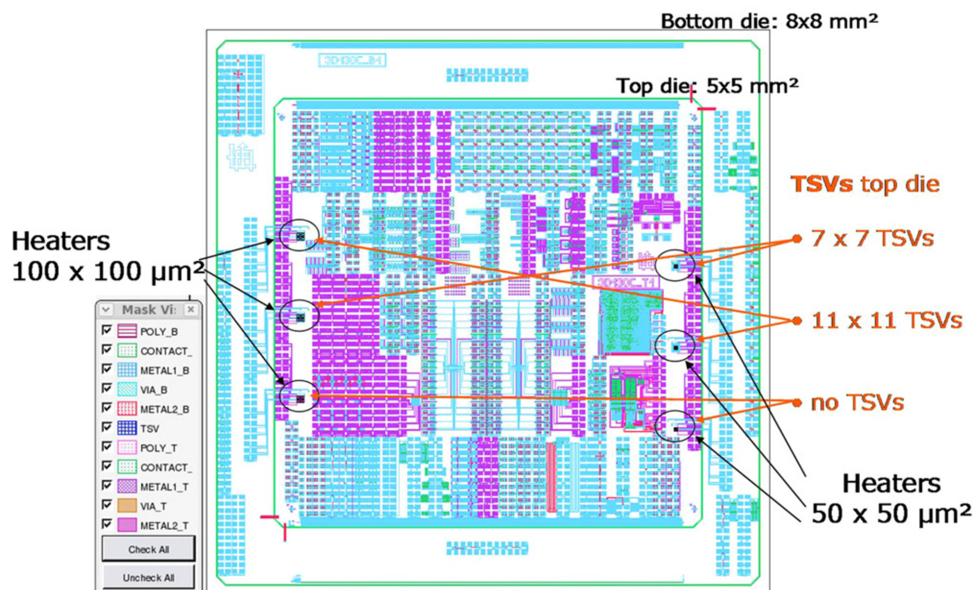


**Fig. 7.** Combined view of the layout of the top die on top of the bottom die including the heating structures and the TSVs through the top die.

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due to the higher power density. In this case with the power dissipation in the metal layer of the BEOL structure a very sharp peak is observed due to the poorly conductive oxide layers surrounding it. For normal operation with heat dissipation in the bulk of the Si a less pronounced peak is expected. The influence of the TSV density can be seen in Fig. 8: in the case without TSVs the maximum temperature increases above the 15 °C of the temperature chuck, amounts to 85.21 °C in the $50\times50\,\mu m^2$ hot spot. For the TSV density of $7\times7$ and $11\times11\,\mu m^2$ the temperature peak is 78.24 and 71.15 °C respectively. In the case of the $100\times100\,\mu m^2$ hot spots the effect of TSV density is less pronounced. Fig. 9 shows a surface plot of the heat flux in the bulk of the Si of the top die. At the top of the TSV an influx of heat can be seen. The heat is generated fairly uniform in the layers on top the Cu TSVs. The heat will flow down through the stack concentrated through the Cu TSVs.

## 5. Experimental validation of the thermal modeling

To have confidence in the modeling results and to improve the proposed approach of the detailed thermal modeling, the simulations need to be experimentally validated. Therefore a dedicated thermal test chip and a test vehicle have been developed to experimentally characterize the thermal effects in the stacked die structure and to validate the modeling approach

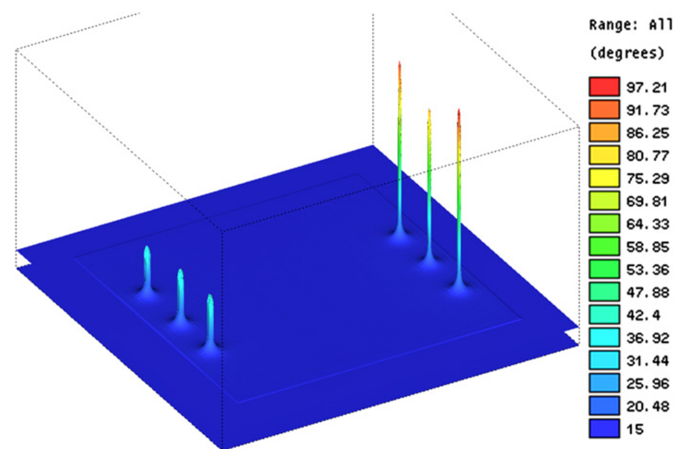


**Fig. 8.** Surface plot of the temperature distribution (°C) in the metal 2 layer of the top die for a power of 120 mW dissipated in the heat sources with an array of $100\times100\,\mu m^2$ on the left side and $50\times50\,\mu m^2$ on the right side.

[13]. For the measurements, the thermal structures on the test chip, described in Section 3 will be used. For a complete validation of the modeling approach, a transient analysis needs to be performed. The comparison between the steady state modeling and experimental results presented in this paper is the first step in the validation process. This comparison validates only the steady state modeling. The complete validation needs to be confirmed by a thorough transient analysis that can be performed using the thermal structure functions approach [6].

### 5.1. Experimental setup

To be able to evaluate the thermal modeling early in the development of the 3D integration including the TSVs a more simplified version of the packaged die stack is considered. In this case a packaging of the die stack is not necessary and the thermal measurements can be performed on a wafer level probe station. Fig. 10 shows a schematic representation of the experimental setup. A thinned top die (25 μm thickness) is bonded to a full thickness landing wafer (725 μm). The die stacked is mounted on a chuck and kept in place by vacuum. The temperature of this chuck can be controlled to provide an isothermal boundary to the bottom of the die stack. Probes assessing the bond pads of the top die are used to electrically connect to the heaters and diodes to dissipate heat in the meander heaters and measure the voltage of the diode for the constant current of 100 μA. The distance between bond pads and diode is sufficient not to interfere with the thermal measurements. If the bond pads and the probes are too close to the diodes they might

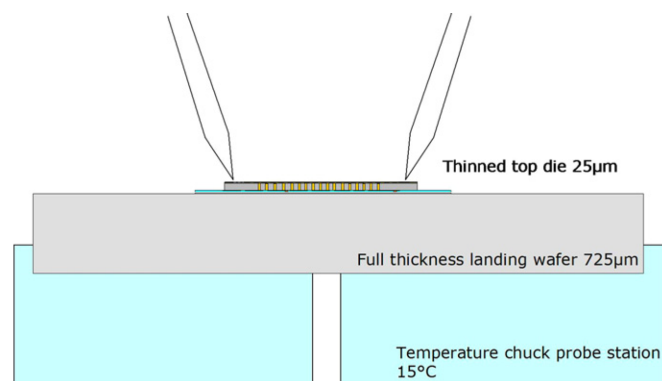


**Fig. 10.** Schematic representation of the experimental set up to validate the thermal modeling.

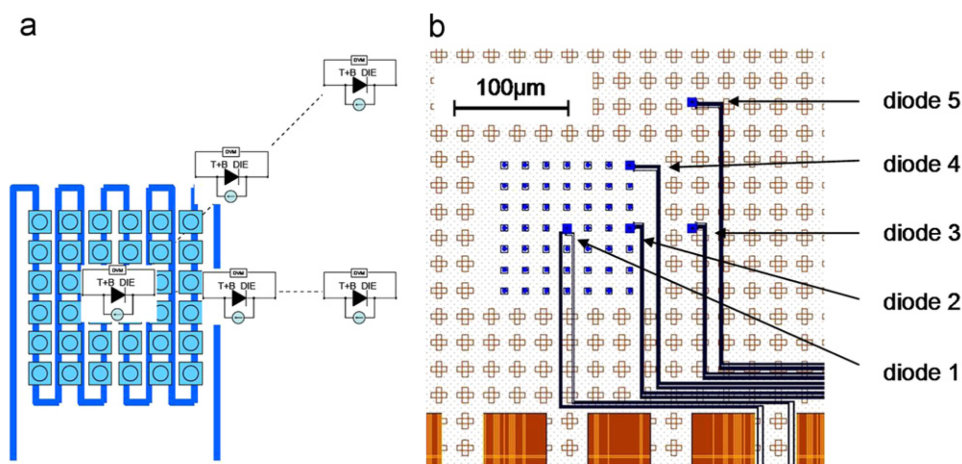


**Fig. 9.** Schematic representation (a) and detail of the design layout (b) to indicate the location of the diodes with respect to the meander heater and the TSV array.

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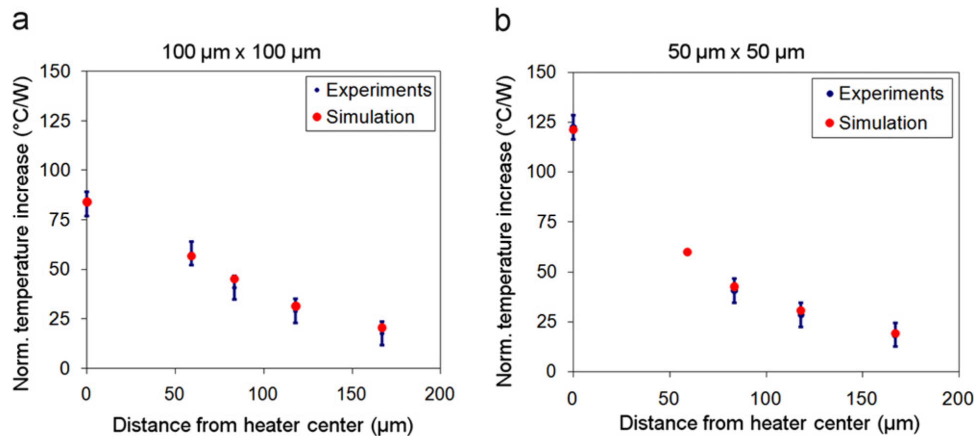


**Fig. 11.** Comparison of the simulation results (red dots) with the experimental temperature measurements (blue dots and error bars) corresponding to the diodes in the top die for a dissipated power of 120 mW for a $100 \times 100\ \mu m^2$ meander heater (a) and a $50 \times 50\ \mu m^2$ meander heater (b).

act as a local heat sink and influence measured temperatures. In this case the distance is more than 1 mm; therefore it can be considered that the probes will not have an influence on the local temperature profile close to the heater ($50 \times 50$ or $100 \times 100\ \mu m^2$).

### 5.2. Experimental validation of the detailed thermal modeling

The experimental results are used to validate the detailed fine grain thermal modeling performed on the same test vehicle. For the comparison and validation a power of 120 mW is dissipated in all the heaters while the temperature chuck is kept at a constant temperature of 15 °C. The experimental measurements of the 6 structures on the test die are performed for 10 different test chips. From these results the average temperature and a 95% confidence interval is calculated. Fig. 11 shows the results of the local temperature profile in the active layer of the Si just below the hot spot. The temperature is evaluated in the locations of the diodes allowing one to one comparison of the simulation with the experiments. The figures on the left hand side and right hand side show the temperature profiles for the large ($100 \times 100\ \mu m^2$) and small heater ($50 \times 50\ \mu m^2$), respectively. The agreement between the simulation and experimental results is very good. Not only the temperature peak is predicted very accurately by the modeling, but also the shape of the temperature profile matches nicely with the temperature measurements in the diodes. For the whole profile the modeling results are within the range of the 95% confidence interval of the experiments. The maximum differences between the modeling and the average value of the experiments are less than 5% for the temperature peaks and less than 10% in the tail.

## 6. Conclusions

In this paper a methodology to perform a detailed, fine grain thermal analysis of a stacked die structure is presented. This methodology allows including the complete detail of the design layout and the full description of the BEOL structure of all the dies in the stack. The approach is demonstrated on a test case of a stacked die structure of two dies BGA package. Both the complete design layout of the top and bottom die, including the interconnections, such as TSVs and solder balls, between both dies are combined to a 3D design. A detailed thermal simulation with a spatial resolution of 100 nm is performed based on the 3D layout specified in the GDSII file and the definition of the stack of materials. Using this approach the thermal influence of the proximity and array density of the below the heat sources TSVs in the top die is studied.

The detailed modeling is experimentally validated using a dedicated test vehicle. A dedicated thermal test chip with integrated heaters and diodes as thermal sensors is developed. The locations of the diodes on the die allow to accurately capture the temperature profile of the hot spot ($50 \times 50$ or $100 \times 100\ \mu m^2$). A very good agreement between the detailed modeling and the experimental measurements is found. The maximum error is less than 5% in the temperature peak and less than 10% in the tails of the temperature profile.

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