Cascaded Channel-Select Filter Array Architecture Using High-K Transducers for Spectrum Analysis

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***Abstract*—This work presents a novel cascaded filter array architecture for large-scale MEMS filter arrays that overcomes the limitations associated with the large shunt capacitance to efficiently scale the number of filters in the array. The proposed architecture effectively reduces the capacitive loading at the input by utilizing a series connection of the filters, resulting in improvement in the return loss and stopband rejection for large arrays. This work demonstrates the feasibility of large-scale filter arrays without the need for additional costly isolation strategies for real-time spectrum monitoring applications.**

I. Introduction

On-going research and development of high quality factor (Q) RF MEMS resonators and filters has allowed their use in a number of RF applications, such as timing references and front end band-select filters [1-4]. Many of these devices have been designed to fit the specifications of current communication system architectures as direct replacement components for quartz or SAW devices with notable success. Currently, most radio architectures use the concept of band-select filtering followed by heterodyning to a lower intermediate frequency, where further signal processing and channel-select filtering is performed. This architecture has been established as the standard for most radio front ends since its invention by Armstrong [5]. It, however, involves a number of tradeoffs between various performance metrics, including linearity, power consumption, and noise, which have been unavoidable largely due to the lack of extremely narrowband filtering capability at RF frequencies using conventional resonator technologies. RF MEMS resonators may be able to relax some of these tradeoffs due to their ability to realize extremely high Q exceeding 10,000 on chip, providing the potential for extremely narrowband filters even at VHF and UHF frequencies. Furthermore, this capability may even enable new types of communication standards and radio architectures for specific applications. One such application is cognitive radio, systems that are able to scan the spectrum and setup a communication link on relatively unused channels or identify and filter blocker signals before they saturate other sensitive electronics [6,7]. Large scale RF MEMS filter arrays have emerged as a key technology which may enable cognitive radio for mobile applications due to the unique ability of this technology to provide both channel-select filtering and lithographical definition of resonant frequency on an integrated platform. However, the number of filters necessary for such applications is on the order of hundreds to thousands.

Recent work has demonstrated arrays each with two and ten separate filters [8,9]. In both cases, the filters were connected in the conventional parallel configuration that is normally envisioned for such an array. While these works demonstrated arrays with multiple filters, they left unanswered questions about how the performance of such arrays would scale as the number of filters is increased. This is a problem due to the shunt capacitance present at the input of any RF MEMS resonator or filter, regardless of the transducer used. As the size of the array increases, the input loading from these shunt capacitors will increase in proportion to the number of filters in the array, significantly degrading performance. The first example [8] shown above was able to circumvent these negative effects by using a differential architecture and a

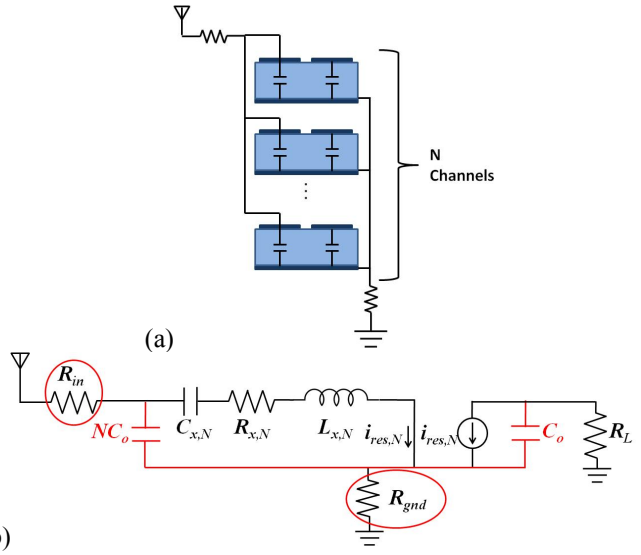

Figure 1. (a) Simplified schematic of the conventional parallel filter array architecture. (b) Equivalent circuit model used for analysis with feedthrough path highlighted in red and important parasitic resistances circled.

parallel inductor to resonate with the shunt capacitance. The utility of such methods, however, are severely limited when it comes to scaling to hundreds of filters. On the other hand, the second example [9] used an AlN transducer, which is known to be a very efficient transducer, and thus is relatively unaffected by the shunt capacitance at such low frequencies and small array sizes. However, as the filter array increases in size and is designed to operate at higher frequency, it will also suffer from the input loading presented by the shunt capacitance. Others have suggested alternative methods of alleviating this problem by added isolation using integrated switches [10] but mechanical switches have yet to be successfully integrated into radio systems or cellular phones, making their use difficult in large scale arrays.

While the problem of shunt capacitance has been raised as an issue potentially limiting the use of MEMS filter arrays, to the authors' knowledge, a rigorous analysis of its effects on filter array performance for arbitrarily large array sizes has not yet been reported. In this paper, we present an analysis based on Butterworth-Van Dyke (BVD) equivalent circuit models with relevant parasitic elements and find that these parasitics combined with the large shunt capacitance severely limit filter performance when using a simple parallel array architecture. We then propose a novel series cascaded filter array architecture that provides a means of alleviating the increasingly negative effects of the shunt capacitance as the array increases in size. Experimental results will then be presented to verify our analysis and we will conclude with a summary and implications of this work.

II. Conventional Parallel Architecture and Effects of Shunt Capacitance

While the MEMS community has been focusing much of its energy on trying to interface directly to a 50 Ω environment (i.e., obtaining motional resistance of 50 Ω), in many cases this has been achieved naively by increasing the transduction area, which also increases the shunt capacitance. In general though, unless the filter array interfaces directly to a 50 Ω distributed system (e.g., antenna), this is not a necessary requirement. In fact, for a given motional resistance, it is always possible in the ideal case (i.e., no parasitic shunt capacitance) to terminate the filter with an optimal impedance which will result in nearly ideal filter characteristics, as long as the Q of the resonators is sufficiently high (i.e., $Q_{res} >> Q_{filter}$). Systems terminated with impedances on the order of 1 kΩ or lower have been demonstrated with low insertion loss and suitable shape factor, indicating that this is not the fundamental limitation [9]. The main problem in the context of large scale filter arrays then is not the motional impedance but the loading of the shunt capacitance. Even the work in [9] achieves its well-behaved filter response only after using the methods previously discussed to mitigate the negative effects of the shunt capacitance. Some of the well-known effects include large insertion loss and passband return loss due to a large impedance mismatch with the source that increases with array size. There are, however, other seldom considered effects – particularly in the stopband response – that arise due to parasitic routing resistances that become increasingly important as array size increases. As a starting point for analyzing these effects, we use a model based on the illustration in Fig. 1(a). An equivalent circuit model is shown in Fig. 1(b). Here, N represents the number of channels in the filter array (i.e., array size), R_{in} models any parasitic interconnect losses, and R_{gnd} models imperfect grounding that results from interconnect losses in the ground plane. The input is loaded by the parallel combination of the shunt capacitances of N filters. We will discuss in this section specifically how a number of important filter metrics – return loss, stopband rejection, and insertion loss – are affected by the shunt capacitance loading and parasitic resistances.

Before discussing the simulation results, note that the following simulations are based on data collected from individual 20 MHz PZT-on-Si filters fabricated at the U.S. Army Research Laboratory. The transduction area of these devices is scaled to achieve 50 Ω motional impedance. These devices are used specifically because the extremely high dielectric constant of PZT makes the loading effects significant at relatively low frequencies and small values of N. This significantly reduces the burden on fabrication and measurement setup for experimental demonstration. This does not, however, restrict the generality of this analysis. While these loading effects in other strongly coupled transducers may become significant at higher frequencies or larger N, this problem cannot be avoided by simply choosing a different transducer, especially when the goal is to design a large scale

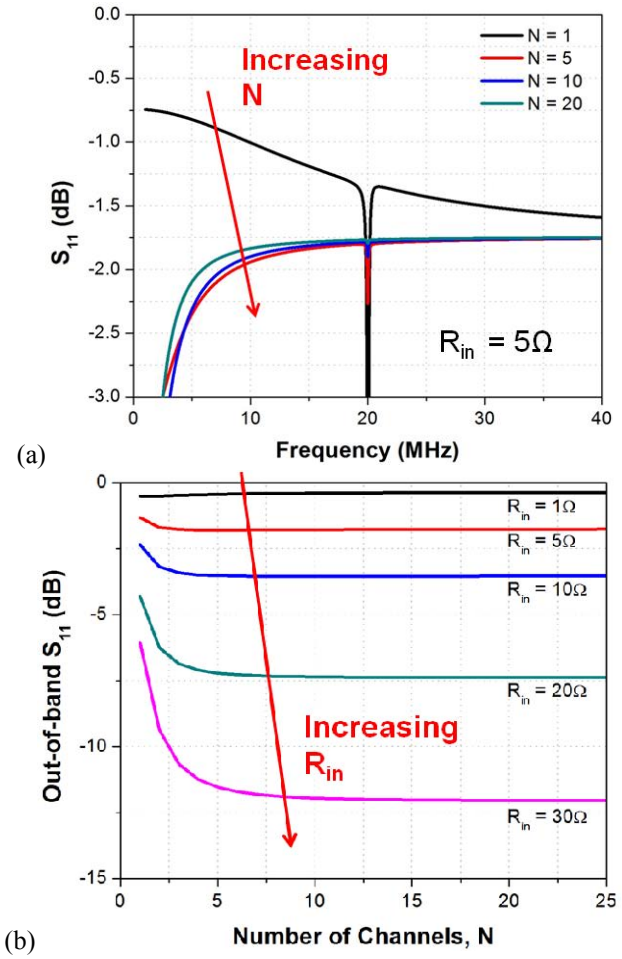

Figure 3. Return loss simulation results (a) as a function of frequency for R_{in} = 5Ω and varying N and (b) stopband return loss as a function of N at 20 MHz.

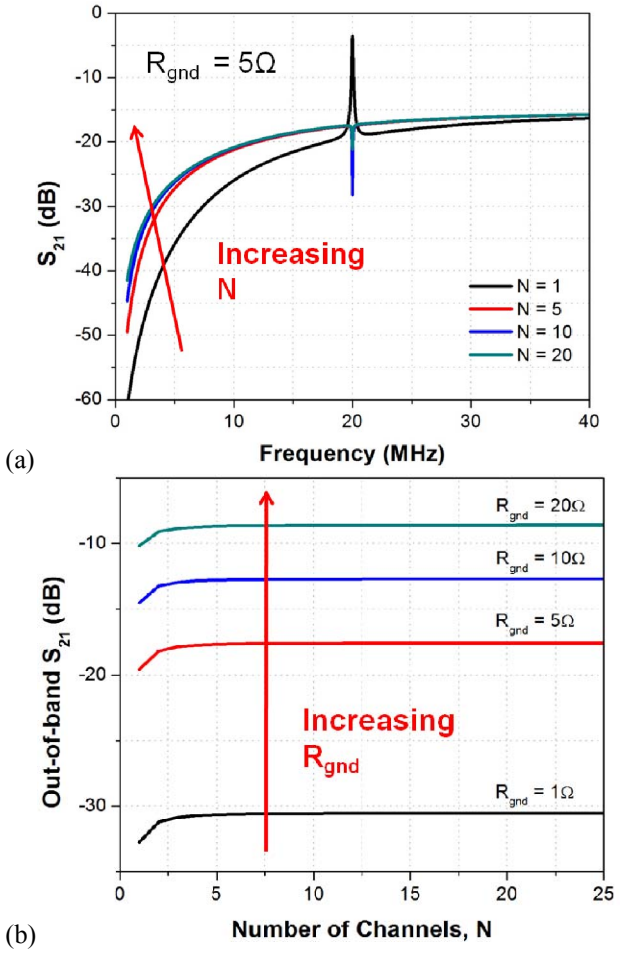

Figure 4. Transmission simulation results (a) versus frequency for R_{gnd} = 5Ω and varying N and (b) feedthrough signal as a function of N at 20 MHz.

filter array with hundreds or thousands of filters.

A. Return Loss

For filters, a large value of return loss in the stopband and a small value in the passband are typically desired. While the need for small passband return loss is well known, it is also important that the stopband return loss be large, a fact often overlooked by designers of MEMS filters. This requirement ensures that energy at these frequencies is not intercepted and wasted in the filter array – even -1 dB of return loss in the stopband means 20% of the incident power is absorbed. Also, nonlinearities may cause interference to appear in the filter passband if strong signals interact with one another. To see how this parameter is affected as the array size increases, we simulate the frequency response of the return loss for a fixed value of R_{in} = 5 Ω and various values of N (Fig. 3(a)). We see that as N increases, the stopband return loss converges to a certain value. This is due to the decreasing impedance of the effective shunt capacitance with increasing N, which virtually terminates the parasitic resistance R_{in} to ground. This provides a path for stopband energy to be absorbed by the filter array and dissipated in R_{in}, in contrast to the case when R_{in} = 0 where this energy was completely reflected. This is also illustrated in Fig. 3(b), which plots the stopband return loss as a function of N for different values of R_{in} at 20 MHz and shows that the stopband return loss converges to a value for large N that is highly dependent on R_{in}. Interestingly, Fig. 3(a) also indicates that the notch depth in the passband decreases as N increases. This indicates that as N increases, less passband energy is absorbed in the filter and any energy that is absorbed is dissipated in the parasitic resistances.

B. Stopband Rejection

Another common problem for RF MEMS filters is the feedthrough signal which limits the stopband rejection. This is often the result of imperfect grounding of the device. The path though which this signal may flow is highlighted in red in Fig. 1(b) and includes the shunt capacitance. Thus, we expect that this feedthrough signal will also be affected as the filter array increases in size. The simulated transmission results for R_{gnd} = 5 Ω and different values of N shown in Fig. 4(a) confirm that the feedthrough signal increases with N, and for certain values of R_{gnd} and N, the feedthrough may even exceed the insertion loss, eliminating the filter response. As in the case for the stopband return loss, the feedthrough converges to a value which is highly dependent on the parasitic resistance R_{gnd}, as shown in Fig. 4(b). This, again, is due to the decreasing impedance of the effective shunt capacitance as N increases, making the feedthrough signal a very strong function of R_{gnd}.

C. Insertion Loss

As previously mentioned, the main reason why insertion loss increases with N is because of impedance mismatch – energy is reflected away rather than flowing into the filters in the array. When these parasitic resistances are now added to the analysis, it is evident that energy dissipation through them – which was also found to impact stopband return loss – is an additional mechanism that prevents energy from reaching the filters. As the previous simulation results show, this dissipation increases with N for given values of the parasitic resistances R_{in} and R_{gnd}, and as already discussed, beyond a threshold value for N depending on R_{in} and R_{gnd} the filter response is practically lost. Again, this behavior is highly sensitive to these parasitic components for large N, setting a limit to the achievable array size. Of course, it is always desirable to minimize these parasitics through good fabrication. However, there may be certain limits to how low they can be made in practical systems. For increased robustness and insensitivity to process variations, it would therefore be desirable to also employ architectural methods of reducing the sensitivity of the filter array to these parasitic components. We see, however, that because of the large capacitive loading at the input, the parallel filter architecture does not provide any robustness to these parasitic resistances, especially as the size of the array increases.

III. Series Cascaded Filter Array Architecture

The analysis in the previous section indicates that the main issue limiting the performance of large scale MEMS filter arrays using the parallel architecture is the large effective shunt capacitance at the input. This combination of N shunt capacitances results in an impedance that decreases with

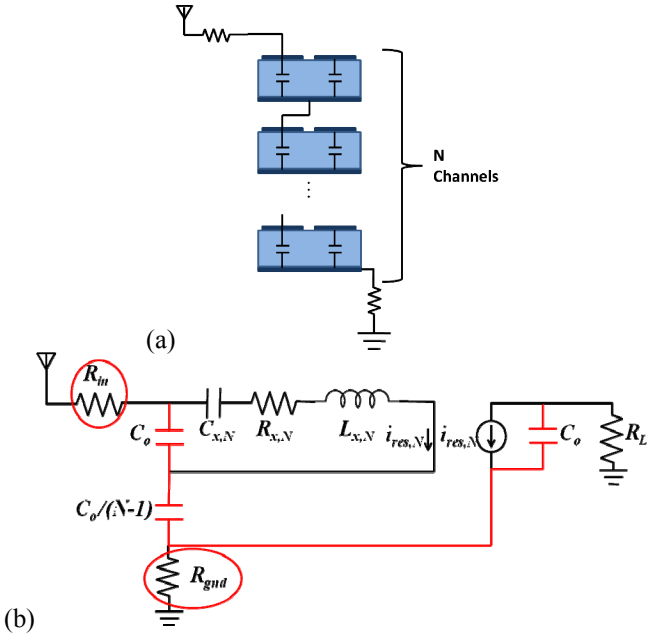

Figure 5. (a) Simplified schematic of proposed series cascaded filter array architecture. (b) Equivalent circuit model used for analysis with feedthrough path highlighted in red and important parasitic resistances circled.

increasing N, leading to a large feedthrough signal and allows the wasteful dissipation of energy through parasitic resistances. Furthermore, the filter response for large N becomes very sensitive to these parasitic resistances, which is undesirable. To avoid this problem, we propose an array architecture where the filters in the array are connected such that a series connection of their shunt capacitance is realized. This will be referred to as the series cascaded filter array architecture and Fig. 5 shows a simplified illustration of this architecture with its equivalent circuit model. For this architecture, since the filters are now connected in series, we expect the effective shunt capacitance to be inversely proportional to N, which results in an impedance that actually increases with array size. It is then expected that both the stopband return loss and feedthrough signal should improve as the array size increases.

We verify the improvement in stopband return loss, by simulating the return loss as a function of frequency for a constant value of R_{in} = 5 Ω and for different values of N (Fig. 6(a)). The results show that the stopband return loss approaches 0 dB as N increases, as expected. More significantly, Fig. 6(b) shows that this is true regardless of the value of R_{in}, as opposed to the parallel filter array architecture in which this parasitic resistance determines the value of return loss for large N. This indicates that the high impedance of the series cascaded array architecture effectively prevents stopband energy from being dissipated in R_{in} and allows it to be reflected back to the source.

Next, the transmission behavior of the series cascaded architecture is simulated as shown in Fig. 7 to verify the improvement in the stopband rejection and feedthrough signal. Fig. 7(a) shows the filter transmission as a function of frequency for R_{in} = 5 Ω and different values of N. This graph shows that as N increases, the feedthrough signal decreases as expected. Fig. 7(b) also confirms that the relationship is

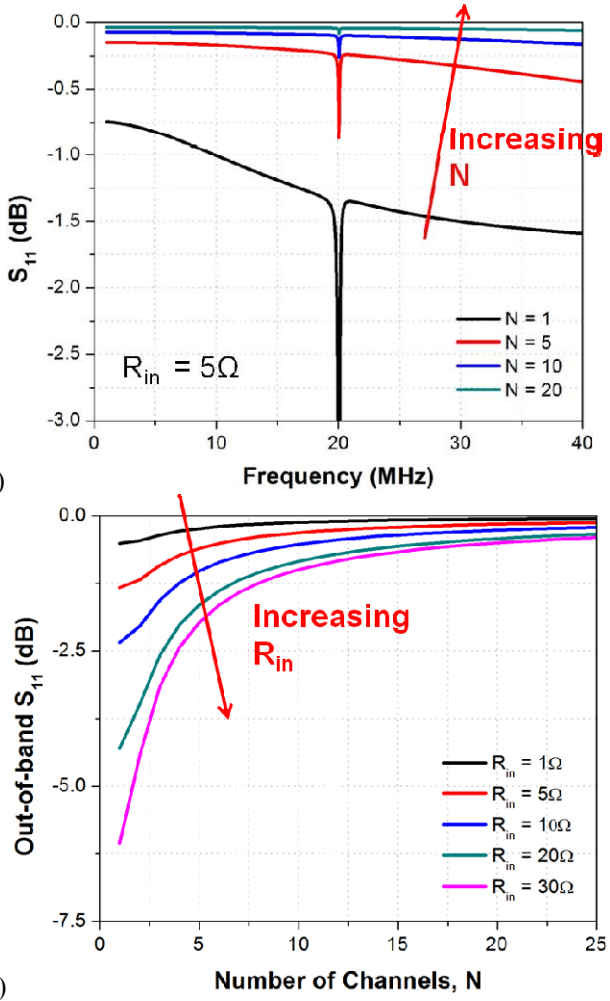

Figure 6. Return loss simulation results (a) as a function of frequency for R_{in} = 5Ω and varying N and (b) stopband return loss as a function of N at 20 MHz.

inversely linear with N, in contrast to the case of the parallel array architecture, where the feedthrough signal increases to some constant level for large N. Since the insertion loss also increases with N due to the voltage division occurring from the series connection of the N filters in the array, the result is a stopband rejection that is relatively insensitive to the array size and, more importantly, a transmission response that does not lose its filter behavior beyond a certain value of N. These simulation results all indicate that the series cascaded array architecture significantly improves the stopband return loss and filter transmission characteristics over its parallel counterpart for large arrays.

IV. Experimental Setup and Results

In order to demonstrate the performance enhancement that results from the use of the series cascaded filter array architecture, two 9-channel arrays of PZT-on-Si filters – one using the parallel architecture, the other using the series cascaded architecture – designed for center frequencies around 20 MHz with channel spacing of 30 kHz were fabricated in the process described in [11]. As previously mentioned, this technology was chosen due to the high dielectric constant of

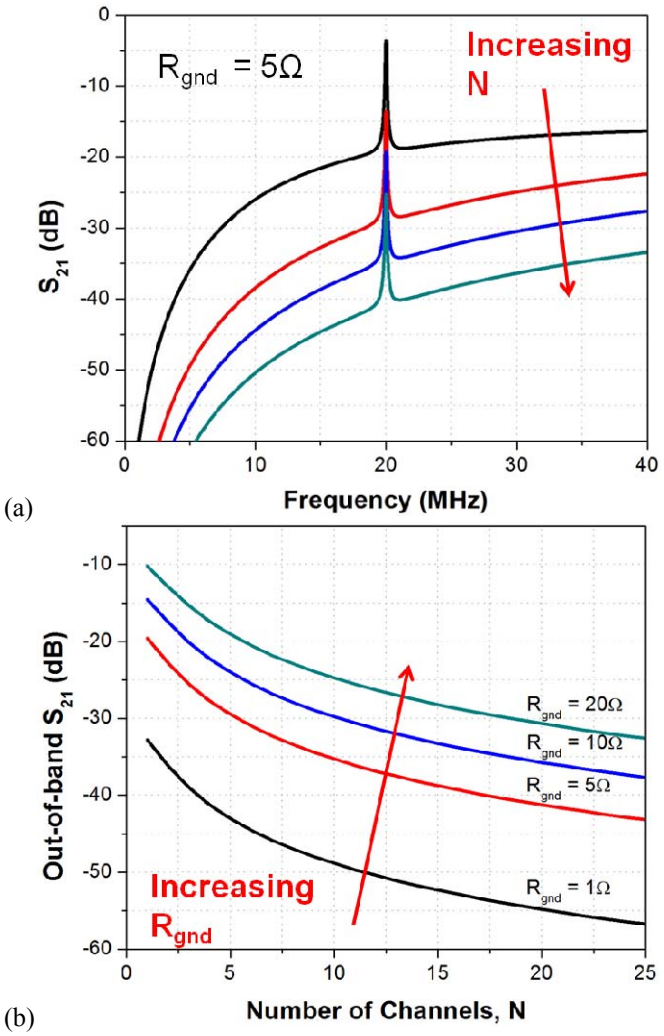

Figure 7. Transmission simulation results (a) versus frequency for R_{gnd} = 5Ω and varying N and (b) feedthrough signal as a function of N at 20 MHz.

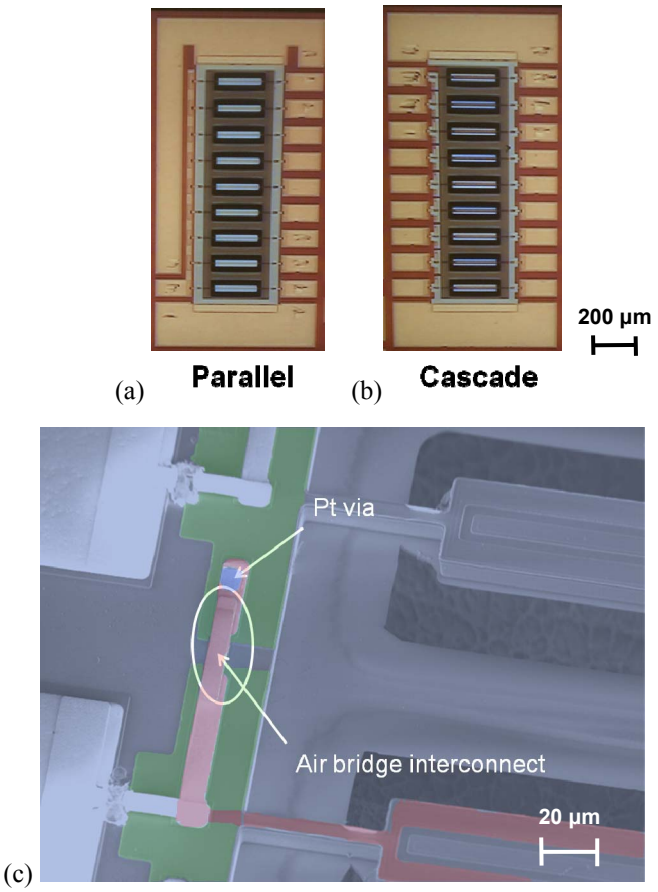

Figure 8. Chip micrograph of 9-channel filter array centered around 20 MHz implemented with (a) conventional parallel architecture and (b) series cascaded architecture using PZT-on-Si filter technology presented in [11]. (c) SEM image showing the routing between filters in the series cascaded architecture.

PZT enabling this work to demonstrate the capacitive loading effects at lower frequency using fewer filters, reducing the burden on fabrication and testing. Micrographs of these arrays are shown in Fig. 8(a) and (b). The SEM image in Fig. 8(c) shows how the series connections are implemented. The area shaded in green indicates the bottom electrode layer of the top filter underneath the PZT layer. A via, shaded blue, is opened to route to the gold air-bridge, which is then connected to the top electrode of the next filter, all of which is shaded in red. This connection is repeated for all filters except the last one in the chain, whose bottom electrode is connected to ground.

Fig. 9 shows the details of the two-port testing setup used to characterize these filter arrays. Port 1 of the vector network analyzer is connected to the GSG probe on the left and provides the input stimulus to the array. The outputs are probed using a 9-point probe structure whose connections are routed to a switching matrix. This matrix selects one filter output to be connected to port 2 of the network analyzer while all others are terminated with 50 Ω impedances. Typical two-port measurements are then repeated to characterize the response of each filter in the array.

Experimental results for the return loss and transmission are shown in Fig. 10(a) and (b), respectively. First, in Fig. 10(a), we see that the parallel filter array has a stopband return loss of roughly -3.5 dB while the notch depth is only about 0.1 dB, indicating that a majority of the absorbed energy is dissipated in parasitic resistances rather than passing through the filters. On the other hand, the series cascaded array shows a larger stopband return loss of roughly -0.7 dB with a notch depth of 0.4 dB, indicating a larger portion of passband energy is reaching the filters. In total, the stopband return loss is improved by roughly 2.9 dB.

Fig. 10(b) shows the results of transmission measurements again confirming the benefits of the series cascaded architecture. The parallel filter array has filters with only 7 dB stopband rejection compared with a roughly 23 dB rejection and 20 dB lower transmission floor for the series cascaded array. The insertion losses are also similar between the two arrays, which is expected. The series cascaded filter array has somewhat higher insertion loss, but this may be due to lower quality factors and non-zero routing resistance between filters. These have been noted and will be improved in future designs. In general, while these filter characteristics have room for improvement, they do indicate that the series cascaded filter array is favorable in terms of both return loss and transmission response of large scale filter arrays.

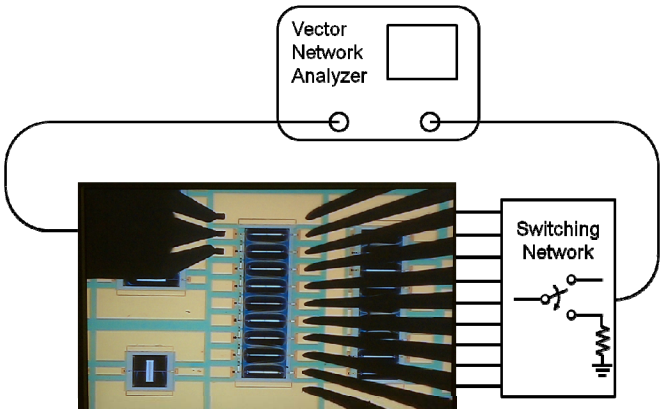

Fig. 9. Two-port measurement setup with switching network used for characterization of the two filter arrays.

V. Conclusions

In summary, this paper presents a detailed analysis of how the performance of the conventional parallel filter array architecture scales with array size using BVD equivalent circuit models. Through this analysis, the large effective shunt capacitance which increases with array size for the parallel array architecture was found to be the main factor limiting the performance of the array, specifically the stopband return loss, stopband rejection, and insertion loss. In addition, it was found that the filter performance was also extremely sensitive to parasitic routing resistances. While it is always desired to minimize these parasitic losses, some might be unavoidable, especially when targeting the design of very large scale filter arrays. Thus, any architectural changes that may reduce this sensitivity would be very beneficial. In response, the series cascaded filter array architecture was proposed to improve the scaling of filter performance with array size by making the effective shunt capacitance now inversely proportional to array size. Simulated results also indicate that this architecture reduces the sensitivity of the filter array to parasitics. This performance improvement was experimentally verified using 9-channel filter arrays with PZT-on-Si filters around a frequency of 20 MHz. While this technology was chosen to demonstrate this concept without the excessive burden of fabricating and testing much larger arrays, the validity of this analysis and architecture is not limited by the type of transducer. This problem of capacitive loading for the parallel array will become an issue even for more efficient transducers when frequency and/or array size is increased. The proposed architecture presents a system-level solution to one of the inherent device limitations of RF MEMS filters, thus opening up the potential for realizing chip-scale spectrum analysis for cognitive radio applications.

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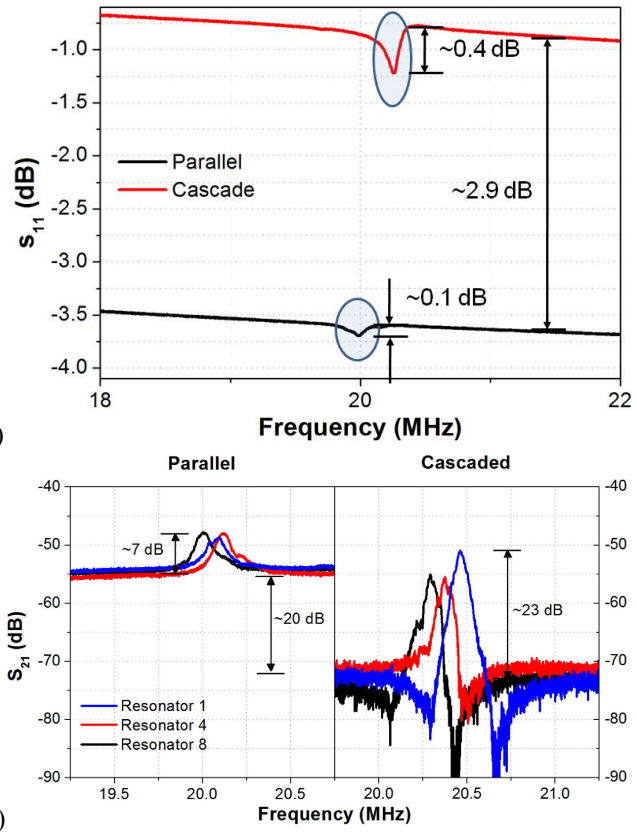

Fig. 10. Experimental results showing the (a) return loss and (b) transmission response for both parallel and series cascaded 9-channel filter arrays.

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