Intel® X79 Express Chipset

Specification Update

November 2011

Contents

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Revision History

	Description	Date
001	• Initial Release	November 2011

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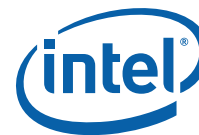
Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	CDI / IBP Number
Intel ® X79 Express Chipset Datasheet	326200-001

Nomenclature

Errata are design defects or errors. Errata may cause the behavior of the PCH to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present in all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

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Summary Tables of Changes

The following tables indicate the errata, specification changes, specification clarifications, or documentation changes which apply to the product. Intel may fix some of the errata in a future stepping of the component and account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations:

Codes Used in Summary Tables

Stepping

X: Erratum exists in the stepping indicated. Specification Change that applies to the stepping indicated.

(No mark)
or (Blank box):   This erratum is fixed or not applicable in listed stepping or Specification Change does not apply to listed stepping.

Status

Doc: Document change or update will be implemented.

Plan Fix: This erratum may be fixed in a future stepping of the product.

Fixed: This erratum has been previously fixed.

No Fix: There are no plans to fix this erratum.

Row

Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

Erratum Number	Stepping C0	Status	ERRATA
1	X	No Fix	USB Full-Speed / Low-Speed Device Removal Issue
2	X	No Fix	SATA Signal Voltage Level Violation
3	X	No Fix	USB Full-Speed Isochronous Traffic May be Lost
4	X	No Fix	Incorrect data for LS or FS USB Periodic IN Transaction
5	X	No Fix	USB FS/LS Incorrect Number of Retries
6	X	No Fix	USB PLL Control FSM not Getting Reset on Global Reset
7	X	No Fix	USB Babble Detected with SW Overscheduling
8	X	No Fix	USB Low-Speed/Full-Speed EOP Issue
9	X	No Fix	Asynchronous Retries Prioritized Over Periodic Transfers
10	X	No Fix	USB Delayed Periodic Traffic Timeout Issue
11	X	No Fix	Occasional SCU SAS/SATA Port performance degradation
12	X	No Fix	SATA Differential Return Loss Violations
13	X	No Fix	USB VHSOH Maximum Violation

Specification Changes

Spec Change Number	Stepping C0	SPECIFICATION CHANGES
N/A	N/A X	None

Specification Clarifications

No.	Document Revision	SPECIFICATION CLARIFICATIONS
N/A	N/A	None

Documentation Changes

No.	Document Revision	DOCUMENTATION CHANGES
N/A	N/A	None
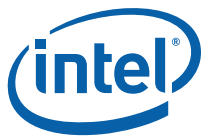
Identification Information

Markings

PCH Stepping	S-Spec	Top Marking	Notes
C0	SLJHW	918407	

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PCH Device and Revision Identification

The PCH implements two types of revision identification: Revision Identification (RID) and Compatible Revision ID (CRID).

The Revision ID (RID) is traditionally an 8-bit register located at offset 08h in the PCI header of every PCI device and function. The assigned value is based on the product's stepping.

The Compatible Revision ID (CRID) is an 8-bit hardwired value that is normally identical to the RID value of a previous stepping of the product with which the new product is deemed "compatible." Multiple CRID values are possible, and can be independently and uniquely selected to manage separate stable software images when desired.

Note: CRID is not an addressable PCI register. The CRID value is simply reflected through the RID register when appropriately selected.

Following reset, the RID value can be read from the RID registers of all devices and functions. To select the CRID value, BIOS must write an assigned CRID select key to D31:F0:Offset 08h. If a correct key is written to a RID register then reads to the RID registers of all devices and functions will return the CRID.

The RID register at D31:F0:Offset 08h is a "write-once" register and gets locked after the first write. If any value other than the key is written to the RID register a system reset must occur before writing the correct value.

Table 1.   PCH CRID Table

CRID Select Keys	PCH Stepping	Rev ID	CRID Value	Notes
1Dh	C0	04h	05h	Enable CRID by writing 1Dh to D31:F0:Offset 08h

The RID register will not retain its value during suspend states. To prevent undesirable enumeration events, the system BIOS must re-select the CRID during resume events from ACPI S3 or S4 states.

PCH Device and Revision ID Table (Sheet 1 of 2)

Device Function	Description	PCH Dev ID	PCH C0 Rev ID	Comments
D31:F0	LPC	0x1D40	05h	PCH
		0x1D41	05h	PCH Production
D31:F2	SATA[1,2]	0x1D00	05h	Non-AHCI and Non-RAID Mode
		0x1D02	05h	AHCI (Ports 0-5)
		0x1D04	05h	RAID: 0/1/5/10
D31:F5	SATA[1,2,3]	0x1D08	05h	Non-AHCI and Non-RAID Mode (Ports 4 and 5)
D31:F3	SMBus	0x1D22	05h	
D31:F6	Thermal	0x1D24	05h	
D22:F0	MEI #1	0x1D3A	05h	
D30:F0	DMI to PCI Bridge	0x1D25h	05h	When D30:F0:4Ch:bit 29 = 1
		0x244Eh	05h	When D30:F0:4Ch:bit 29 = 0
D29:F0 or D29:F7	USB EHCI #1	0x1D26	05h	
D26:F0 or D26:F7	USB EHCI #2	0x1D2D	05h	
D27:F0	Intel HD Audio	0x1D20	05h	
D28:F0	PCI Express Port 1	0x1D10 or 0x1D11	05h	When D28:F0/F1/F2/F3/F4/F5/F6/F7:ECh:bit 1 = 0
		0x244Eh[10]	05h	When D28:F0/F1/F2/F3/F4/F5/F6/F7:ECh:bit 1 = 1
D28:F1	PCI Express Port 2	0X1D12 or 0x1D13	05h	When D28:F0/F1/F2/F3/F4/F5/F6/F7:ECh:bit 1 = 0
		0x244Eh[10]	05h	When D28:F0/F1/F2/F3/F4/F5/F6/F7:ECh:bit 1 = 1
D28:F2	PCI Express Port 3	0X1D14 or 0x1D15	05h	When D28:F0/F1/F2/F3/F4/F5/F6/F7:ECh:bit 1 = 0
		0x244Eh[10]	05h	When D28:F0/F1/F2/F3/F4/F5/F6/F7:ECh:bit 1 = 1
D28:F3	PCI Express Port 4	0X1D16 or 0x1D17	05h	When D28:F0/F1/F2/F3/F4/F5/F6/F7:ECh:bit 1 = 0
		0x244Eh[10]	05h	When D28:F0/F1/F2/F3/F4/F5/F6/F7:ECh:bit 1 = 1

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PCH Device and Revision ID Table (Sheet 2 of 2)

Device Function	Description	PCH Dev ID	PCH C0 Rev ID	Comments
D28:F4	PCI Express Port 5	0X1D18 or 0x1D19	05h	When D28:F0/F1/F2/F3/F4/F5/F6/F7: ECh:bit 1 = 0
		0x244Eh[10]	05h	When D28:F0/F1/F2/F3/F4/F5/F6/F7: ECh:bit 1 = 1
D28:F5	PCI Express Port 6	0X1D1A or 0x1D1B	05h	When D28:F0/F1/F2/F3/F4/F5/F6/F7: ECh:bit 1 = 0
		0x244Eh[10]	05h	When D28:F0/F1/F2/F3/F4/F5/F6/F7: ECh:bit 1 = 1
D28:F6	PCI Express Port 7	0X1D1C or 0x1D1D	05h	When D28:F0/F1/F2/F3/F4/F5/F6/F7: ECh:bit 1 = 0
		0x244Eh[10]	05h	When D28:F0/F1/F2/F3/F4/F5/F6/F7: ECh:bit 1 = 1
D28:F7	PCI Express Port 8	0X1D1E or 0x1D1F	05h	When D28:F0/F1/F2/F3/F4/F5/F6/F7: ECh:bit 1 = 0
		0x244Eh[10]	05h	When D28:F0/F1/F2/F3/F4/F5/F6/F7: ECh:bit 1 = 1
D25:F0	LAN[4]	0X1D33	05h	
D22:F0	MEI #1	0x1D3A	05h	
D22:F1	MEI #2	0x1D3B	05h	
D22:F3	KT	0x1D3D	05h	
Bx[5]:D0:F0	SCU0	varies[6]	05h	
Bx:D0:F3	SMB 0	0x1D70	05h	

Notes:
1. PCH contains two SATA devices. The SATA Device ID is dependant upon which SATA mode is selected by BIOS and what RAID capabilities exist in the SKU.
2. The SATA RAID Controller Device ID may reflect a different value based on Bit 7 of D31:F2:Offset 9Ch.
3. SATA Controller 2 (D31:F5) is only visible when D31:F2 CC.SCC = 01h
4. LAN Device ID is loaded from EEPROM. If EEPROM contains either 0000h FFFFh in the Device ID location, then 1C33 is used. Refer to the appropriate Intel GbE physical layer Transceiver (PHY) datasheet for LAN Device IDs.
5. Bus number n and x is assigned by the BIOS, x is a number larger than n+1.
6. SCU device ID is based on RAID capabilities. See Table 3 for details.
7. This table shows the default PCI Express Function Number-to-Root Port mapping. Function numbers for a given root port are assignable through the "Root Port Function Number and Hide for PCI Express Root Ports" register (RCBA+0404h).
8. SCU1 will not appear as a separate PCI function on B0 or later steppings.
9. Virtual Root Port can not exist at the same times as Virtual Switch Port (Bn+1:D8:F0).
10. There can only be one PCI Express* port with Device ID 244Eh in the system.

Table 3. PCH SCU Device ID Based on Port Configuration and RAID Features

Port Configuration	Intel® RSTe RAID 5	Third Party Device Driver	SCU Device ID (Physical Functions)	SCU Device ID (Virtual Functions)	Hard SKU or Equivalent
4 ports SATA	No	No	1D69h	1D59h	-B
4 ports SATA	Yes	No	1D65h	1D55h	-B

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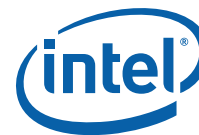
Errata

1.   USB Full-Speed / Low-Speed Device Removal Issue

Problem: If two or more USB Full-Speed / Low-Speed devices are connected to the same USB controller, the devices are not suspended, and one device is removed, then one or more of the devices remaining in the system may be affected by the disconnect.

Implication: The implication is device dependant. A device may experience a delayed transaction, stall and be recovered via software, or stall and require a reset such as a hot plug to resume normal functionality.

Workaround: None.

Status: For the steppings affected, see the Summary Tables of Changes.

2.   SATA Signal Voltage Level Violation

Problem: SATA transmit buffers have been designed to maximize performance and robustness over a variety of routing scenarios. As a result, the SATA transmit signaling voltage levels may exceed the maximum motherboard TX connector and device RX connector voltage specifications as defined in section 7.2.1 of the Serial ATA spec, rev 3.0. This issue applies to Gen 1 (1.5 Gb/s) and Gen2 (3.0 Gb/s).

Implication: None Known.

Workaround: None.

Status: For the steppings affected, see the Summary Tables of Changes.

3.   USB Full-Speed Isochronous Traffic May be Lost

Problem: If a USB Full-Speed inbound ischronous transaction with a packet length 190 bytes or greater is started near the end of a micro-fame the PCH may occasionally see more than 189 bytes for the next micro-frame.

Implication: If the PCH sees more than 189 bytes for a micro-frame an error will be sent to software and the isochronous transfer will be lost. If a single packet is lost no perceptible impact for the end user is expected.

Note: Intel has only observed the issue in a synthetic test environment where precise control of packet scheduling is available, and has not observed this failure in its compatibility validation testing.

— • Isochronous traffic is periodic and cannot be retried thus it is considered good practice for software to schedule isochronous transactions to start at the beginning of a micro-frame. Known software solutions follow this practice.

— • To sensitize the system to the issue additional traffic such as other isochronous transactions or retries of asynchronous transactions would be required to push the inbound isochronous transaction to the end of the micro-frame.

Workaround: None.

Status: For the steppings affected, see the Summary Tables of Changes.

4. Incorrect data for LS or FS USB Periodic IN Transaction

Problem: The Periodic Frame list entry in DRAM for a USB Low-Speed or Full-Speed Periodic IN transaction may incorrectly get some of its data from a prior Periodic IN transaction which was initiated very late into the preceding Micro-frame.

It is considered good practice for software to schedule Periodic Transactions at the start of a Micro-frame. However Periodic transactions may occur late into a Micro-frame due to the following cases outlined below:

- Asynchronous transaction starting near the end of the proceeding Micro-frame gets Asynchronously retried.

- Two Periodic transactions are scheduled by software to occur in the same Microframe and the first needs to push the second Periodic IN transaction to the end of the Micro-frame boundary.

Note: Transactions getting Asynchronous retried would only occur for ill behaved USB device or USB port with a signal integrity issue.

Implication: The implication will be device, driver or operating system specific.

Note: This issue has only been observed in a synthetic test environment.

Workaround: None.

Status: For the steppings affected, see the Summary Tables of Changes.

5. USB FS/LS Incorrect Number of Retries

Problem: A USB Low-Speed Transaction may be retried more than three times, and a USB Full-Speed transaction may be retried less than three times if all of the following conditions are met:

- A USB Low-Speed transaction with errors, or the first retry of the transaction occurs near the end of a micro-frame, and there is not enough time to complete another retry of the Low-Speed transaction in the same micro-frame.

- There is pending USB Full-Speed traffic and there is enough time left in the microframe to complete one or more attempts of the Full-Speed transaction.

- Both the Low-Speed and Full-Speed transactions must be asynchronous (Bulk/Control) and must have the same direction either in or out.

Note: Per the USB EHCI Specification a transaction with errors should be attempted a maximum of 3 times if it continues to fail.

Implication:

— For Low-Speed transactions, the extra retry(s) allow a transaction additiona

— l chance(s) to recover regardless of if the Full-Speed transaction has errors or not. If the Full- Speed transactions also has errors, the PCH may retry the transaction fewer times than required, stalling the device prematurely. Once stalled, the implication is software dependant, but the device may be reset by software.

Workaround: None.

Status: For the steppings affected, see the Summary Tables of Changes.

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6. USB PLL Control FSM not Getting Reset on Global Reset

Problem: The PCH USB PLL may not lock if a Global Reset occurs early during a cold boot sequence.

Implication: USB interface would not be functional an additional cold boot would be necessary to recover.

Workaround: None.

Status: For the steppings affected, see the Summary Tables of Changes.

7. USB Babble Detected with SW Overscheduling

Problem: If software violates USB periodic scheduling rules for Full-Speed isochronous traffic by overscheduling, the RMH may not handle the error condition properly and return a completion split with more data than the length expected.

Implication: If the RMH returns more data than expected, the endpoint will detect packet babble for that transaction and the packet will be dropped. Since overscheduling occurred to create the error condition, the packet would be dropped regardless of RMH behavior. If a single isochronous data packet is lost, no perceptible impact to the end user is expected.

Note: USB software overscheduling occurs when the amount of data scheduled for a microframe exceeds the maximum budget. This is an error condition that violates the USB periodic scheduling rule.

Note: This failure has only been recreated synthetically with USB software intentionally overscheduling traffic to hit the error condition.

Workaround: None.

Status: For the steppings affected, see the Summary Tables of Changes.

8. USB Low-Speed/Full-Speed EOP Issue

Problem: If the EOP of the last packet in a USB Isochronous split transaction (transaction >189 bytes) is dropped or delayed 3 ms or longer the following may occur:

- If there are no other pending Low-Speed or Full-Speed transactions the RMH will not send SOF, or Keep-Alive. Devices connected to the RMH will interpret this condition as idle and will enter suspend.

- If there is other pending Low-Speed or Full-Speed transactions, the RMH will drop the isochronous transaction and resume normal operation.

Implication:

- If there are no other transactions pending, the RMH is unaware a device entered suspend and may start sending a transaction without waking the device. The implication is device dependant, but a device may stall and require a reset to resume functionality.

- If there are other transactions present, only the initial isochronous transaction may be lost. The loss of a single isochronous transaction may not result in end user perceptible impact.

Note: Intel has only observed this failure when using software that does not comply with the USB specification and violates the hardware isochronous scheduling threshold by terminating transactions that are already in progress.

Workaround: None.

Status: For the steppings affected, see the Summary Tables of Changes.

9. Asynchronous Retries Prioritized Over Periodic Transfers

Problem: The integrated USB RMH incorrectly prioritizes Full-Speed and Low-Speed asynchronous retries over dispatchable periodic transfers.

Implication: Periodic transfers may be delayed or aborted. If the asynchronous retry latency causes the periodic transfer to be aborted, the impact varies depending on the nature of periodic transfer:

- If a periodic interrupt transfer is aborted, the data may be recovered by the next instance of the interrupt or the data could be dropped.

- If a periodic isochronous transfer is aborted, the data will be dropped. A single dropped periodic transaction should not be noticeable by end user.

Note: This issue has only been seen in a synthetic environment. The USB spec does not consider the occasional loss of periodic traffic a violation.

Workaround: None.

Status: For the steppings affected, see the Summary Tables of Changes.

10. USB Delayed Periodic Traffic Timeout Issue

Problem: If a periodic interrupt transaction is pushed out to the x+4 micro-frame boundary, the RMH may not wait for the transaction to timeout before starting the next transaction.

Implication: If the next Full-Speed or Low-Speed transaction is intended for the same device targeted by the periodic interrupt, the successful completion of that transaction is device dependent and cannot be guaranteed. The implication may differ depending on the nature of the transaction:

- If the transaction is asynchronous and the device does not respond, it will eventually be retried with no impact.

- If the transaction is periodic and the device does not respond, the transfer may be dropped. A single dropped periodic transaction should not be noticeable by end user.

Note: This issue has only been seen in a synthetic environment.

Workaround: None

Status: For the steppings affected, see the Summary Tables of Changes.

11. Occasional SCU SAS/SATA Port performance degradation

Problem: Intel has observed the x79 SCU SAS/SATA controller may exhibit one or more random ports with unreliable I/O performance. This phenomenon has been noted on a simple, direct-attached 1m configuration.

Implication: Under various temperature/voltage operating conditions, bit-error rates in excess of spec-defined limits may be seen.

Workaround: SCU must not be used on the X79 Express Chipset

Status: No Fix Planned for the X79 Express Chipset (SSPEC# SLJHW)

12. SATA Differential Return Loss Violations

Problem: The Intel x79 Express Chipset SATA buffer capacitance may be higher than expected.

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Implication: There are no known functional failures. This may cause a violation of the SATA-IO compliance test for Receiver or Transmitter Differential Return Loss.

Workaround: None.

Note: Intel plans to obtain a waiver for the SATA-IO building block status.

Status: For the steppings affected, see the Summary Tables of Changes

13.   USB VHSOH Maximum Violation

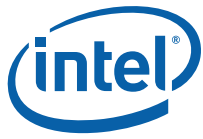Problem: Intel x79 Express Chipset High-Speed USB 2.0 VHSOH may exceed the USB 2.0 specification.

Note: The maximum expected VHSOH is 440 mV.

Implication: There are no known functional failures.

Note: This issue has only been seen in a synthetic environment.

Workaround: None

Status: For the steppings affected, see the Summary Tables of Changes
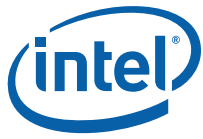
Specification Changes

There are no Specification Changes in this Specification Update Revision.

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Specification Clarifications

There are no Specification Clarifications in this Specification Update Revision.

Documentation Change

There are no Documentation Changes in this Specification Update Revision.

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