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Active Matrix OLED Using 150°C a-Si TFT Backplane Built on Flexible Plastic Substrate

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ABSTRACT

Flexible displays fabricated using plastic substrates have a potential for being very thin, light weight, highly rugged with greatly minimized propensity for breakage, roll-to-roll manufacturing and lower cost. The emerging OLED display media offers the advantage of being a solid state and rugged structure for flexible displays in addition to the many potential advantages of an AM OLED over the currently dominant AM LCD. The current high level of interest in flexible displays is facilitating the development of the required enabling technologies which include development of plastic substrates, low temperature active matrix device and backplane fabrication, and display packaging. In the following we will first discuss our development efforts in the PEN based plastic substrates, active matrix backplane technology, low temperature (150°C) a-Si TFT devices and an AM OLED test chip used for evaluating various candidate designs. We will then describe the design, fabrication and successful evaluation and demonstration of a 64x64 pixel AM OLED test display using a-Si TFT backplane fabricated at 150°C on the flexible plastic substrate.

Key Words: Flexible Display, AM OLED, Plastic Substrate, 150°C a-Si TFT, Plastic Display, Flexible AM OLED, Flexible Active Matrix OLED, Organic Light Emitting Diode, Plastic Dimensional Stability, Flexible TFT-OLED

1. INTRODUCTION

Recently there has been a lot of interest in developing displays fabricated using flexible and plastic substrates [1]. Displays fabricated using plastic substrates would have the potential advantages of being highly rugged and not prone to breakage, light weight, thinner, amenable to roll-to-roll manufacturing, and lower cost compared to glass substrate based displays. AM OLED technology is a potential candidate display media for flexible displays. Currently AM OLED is being developed as the next generation display technology capable of challenging the AM LCD technology in many of its current applications. Compared to AM LCD, the advantages of AM OLED include superior image quality, wide viewing angle, fast response time, being lighter, thinner, all solid state and more rugged, and potentially lower power consuming and lower cost. Currently, glass substrate based AM OLED is being developed aggressively to compete with well entrenched back lit AM LCD (on glass) technology in applications ranging from small to large displays. Small size AM OLEDs on glass are already on the market in consumer products such as mobile phones and digital cameras. Large AM OLEDs (on glass) with sizes over 20" diag. have been successfully fabricated to demonstrate the technical feasibility [2]. Also, the AM OLED attributes have generated interest in the consideration of these displays for the demanding avionic applications [3].

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The development of AM OLED on a plastic (flexible) substrate enables many unique applications. In addition to enabling a wide range of consumer applications, flexible displays provide unique advantages for many military systems requiring displays that are highly rugged, conformable and flexible, and enable new applications such as displays for active camouflage.

However, for the flexible AM OLED technology to become a reality, a number of enabling technologies must be developed and refined. These enablers include technologies for flexible/ plastic substrates, barrier films, low-temperature active matrix device/ backplane fabrication [4], OLED materials and devices, display encapsulation and packaging. In the following we will discuss the results of our flexible display development effort. We will first discuss the plastic substrate development, followed by active matrix backplane technology, and AM OLED test chip development. We will discuss the design, fabrication and demonstration of the world's first AM OLED display built on a plastic substrate using 150^{o} C a-Si TFT backplane on a transparent 125 μm thick flexible plastic substrate.

2. PLASTIC / FLEXIBLE SUBSTRATE DEVELOPMENT

Polyester films are well-known substrates for a wide range of electronic applications such as membrane touch switches and flexible circuitry [5]. New developments in polyester film substrates are contributing to the successful development of plastic substrates for use in passive matrix OLED applications and potentially for use with the active matrix a-Si TFT developments on plastic. In this section we will discuss the development of polyethylene naphthalate (PEN) films (Teonex® brand) [6]. These PEN based substrates offer a unique combination of excellent dimensional stability, low moisture pickup, good solvent resistance, high clarity and very good surface smoothness. This combination of attributes makes PEN a promising substrate for subsequent vacuum and other coating processes for potential use in flexible active matrix backplane fabrication.

The technical challenges in this development are, however, extremely demanding. The plastic substrates need to offer glass-like properties and must therefore have high clarity, smoothness of surface, and excellent dimensional and thermal stability coupled with excellent oxygen and moisture barrier.

2. 1. Optical Properties

Good optical properties can be achieved with PEN films by close control of the polymer recipe. Typically PEN has a total light transmission (TLT) of 87% over 400-700nm coupled with a haze of less than 0.7%. The substrate is optically clear and colorless. Figure 1 shows the transmission spectra of a 125 μm thick PEN substrate in the visible range.

2.2. Surface Quality

Surface smoothness and cleanliness are both essential to prevent pinpricks in subsequent barrier coatings and to ensure that the defects from the substrate do not deleteriously affect the TFT active matrix manufacturing yield. Through control of recipe and film process, very good initial smoothness can be achieved. This is demonstrated in Figures 2a-c. Figure 2a shows a 2.5 millimeter square area of industrial grade PEN, as examined using a conventional non-contacting, white-light, phase-shifting interferometry techniques (using a Wyko NT3300 surface profiler). As shown in Figure 2a, the industrial grade PEN contains over ten peaks greater than 100 nm in height and numerous peaks over 50 nm. In comparison optical grade PEN shows only five peaks greater than 50 nm in the same measured area (Figure 2b), indicating how the surface quality can be controlled by recipe and process optimization. The surface defects which remain in the PEN however are still detrimental to the performance of thin overlying layers. Removing these entirely requires the application of a coating layer, typically comprised of a scratch resistant material. This coating layer acts to smooth over all the underlying PEN surface defects and additionally helps to prevent surface scratches during the subsequent substrate handling operations. Figure 2c shows the surface topography of a surface-tailored PEN over a 1.2 millimeter square area and illustrates how all the surface defects are removed by the application of a coating layer.

2.3. Dimensional Stability

Dimensional stability during TFT array processing (involving temperature cycles between room temperature and the process temperatures) is extremely critical to ensure that the features in each layer of the TFT device structure align properly with the corresponding features in the previous layers. Plastic films undergo a variable and undesirable change in dimensions at the Tg, due to both molecular relaxation events associated with the increased mobility of the polymer chains and shrinkage or expansion associated with the relaxation of residual strain within the oriented parts of the film structure. This is an artifact of the film manufacturing conditions [7]. PEN has an inherent advantage over polyethylene Terephthalate (PET) with a Tg of 120^{o}C versus approximately 80 ^{o}C. In addition, the dimensional stability of PEN can be enhanced further by a heat stabilization process where the internal strain in the film is relaxed by exposure to high temperature whilst under minimum line tension. Shrinkage at a given temperature is measured by placing the sample in a heated oven for a given period of time. The % shrinkage is calculated as the % change of dimension of the film in a given direction before and after heating. Heat-stabilized films exhibit shrinkage of the order of < 0.1 % and typically < 0.05% when exposed to temperatures of up to 180^{o}C for 5 minutes. In addition, once heat stabilized, the Tg effects described above are essentially negated and PEN remains a dimensionally reproducible substrate up to 200^{o}C. Figure 3 shows the results of the thermo mechanical analysis (Using Perkin Elmer Thermomechanical Analyzer PE-TMA-7) from heat stabilized PEN. For comparison purpose similar results are shown for non-heat-stabilized PEN in the Figure. The non-heat-stabilized PEN and heat-stabilized PEN films are sequentially ramped from 140^{o}C to 200^{o}C and the change in dimensions on cooling back to room temperature before the next heating cycle are recorded in the y axis. The change in the expansion of heat stabilized PEN is fairly linear as the sample is heated through the Tg and to higher temperatures and then cooled. Its improved thermal resistance provides a dimensionally reproducible substrate over this temperature range and permits a continuous use temperature of 160°C.

An advantage that PEN films exhibit over the high Tg amorphous resins is that being crystalline they have a significantly lower moisture uptake, typically 1500ppm at equilibrium compared to approximately 2% for some amorphous resins. High moisture uptake can lead to unpredictable dimensional reproducibility with some amorphous high Tg resins.

2.4. Solvent Resistance

The PEN film has excellent solvent resistance to most acids and organic solvents and will typically withstand the solvents used in AM OLED display fabrication. Indeed no specific issues of significance are seen using the PEN substrate during the fabrication of the AM OLED test displays during this development program.

2. 5. Barrier Layers

The inherent barrier properties of PEN films are typically of the order of ca 1 g/m^2/day for water vapor transmission rate and an equivalent ca of 3 mL/m^2/day for oxygen transmission rates. This is still a long way from the levels required for the protection of OLED displays, which require water vapor transmission rates of $<10^{-6}$ g/m^2/day and oxygen transmission rates of $<10^{-5}$ mL/m^2/day. No polymer substrate meets all these requirements, and the plastic substrates currently being developed need to use barrier layers to withstand moisture and oxygen penetration. Various barrier strategies are being explored by a number of companies. One approach involves multi-layer structures of inorganic barrier coatings coupled with planarizing organic coatings to minimize the detrimental effects of pinholes and diffusion at grain boundaries in the barrier layers [8]. PEN film with its excellent surface smoothness offers an ideal base film for depositing subsequent barrier coatings to provide flexible substrates for AM OLED fabrication.

Based on the above results and considerations, heat-stabilized PEN has been selected as a flexible substrate for active matrix OLED development for this program using a maximum TFT backplane process temperature of 150^{o}C.

3. ACTIVE MATRIX BACKPLANE TECHNOLOGY

3.1. TFT Technology

For the present flexible display development program the thin film transistor (TFT) technologies that we considered include low temperature poly-silicon (LTPS), amorphous silicon (a-Si), and organic semiconductor (OTFT). The suitability of these options for the current application are considered in light of the process temperature constraint of 150^{o}C imposed by the use of the selected PEN plastic substrate. While it is possible to transfer high performance

polysilicon or single crystal silicon TFT devices processed at a high temperature on a glass, quartz, or silicon substrates on to a flexible plastic substrate [9,10], this approach is not deemed appropriate for our application because of low-cost considerations, and hence will not be discussed further.

The conventional LTPS process [11] used in the current AM LCDs uses a typical process temperature in the range of 450-600^{o}C using polysilicon film produced by Excimer laser recrystallization of an a-Si film. Due to the high process temperature requirement, the conventional LTPS TFT approach obviously cannot be used with plastic substrates with 150^{o}C process temperature limitation. To overcome this problem ultra low-temperature polysilicon (ULTPS) TFT processes are currently being developed using a process temperatures of about 100^{o}C [12]. Good progress has been made in producing TFTs with high mobility and satisfactory threshold voltages for the n- and p-channel devices. However, the leakage currents need to be reduced further for fabricating high quality active matrix displays. The ULTPS technology continues to be developed to reduce the leakage currents and to further enhance maturity and increase process yield.

Amorphous silicon TFT is currently the workhorse of the well-established AM LCD technology. The conventional a-Si TFTs used in the current AM LCDs are fabricated at a typical process temperature of 300^{o}C. Again for the obvious reason of high process temperature requirement, the conventional a-Si TFT process could not be used with candidate plastic substrate with a process temperature limitation of 150^{o}C. However, in recent years significant advances have been made in the process temperature reduction, and a-Si TFTs have been successfully fabricated using a process temperature of 150^{o}C [13], with a performance comparable to the 300^{o}C process with respect to mobility, threshold voltage and leakage current. However, a-Si TFT is available only in the n-channel mode which restricts the choice of pixel addressing circuitry that could be utilized. We will discuss this further under the next section on pixel drive electronics. In addition, a-Si TFTs are known to have threshold voltage, V_t, shifts under prolonged positive gate bias, particularly under higher operating temperature conditions. One approach for increasing the a-Si TFT stability, and decreasing the propensity for V_t shift is to reduce the display operating voltages and pixel current drive requirements. The recent progress in OLED materials towards lower drive voltages and pixel current requirements is very encouraging.

In recent years there has been a lot of interest in the development of organic electronics, and TFTs fabricated using organic semiconductors. OTFTs have the advantage of very low process temperature, and they could be processed using low-cost solution casting methods (e.g. spin coating, ink jet printing, etc.) instead of the more expensive thin film deposition methods. To date OTFTs fabricated using Pentacene as the organic semiconductor have shown the best performance [14] with a field effect mobility of over 3 cm^2/V.Sec, near zero V_t, and "on"- "off" current ratio of over 10^8. These characteristics are better than the typical characteristics from a-SI TFT. One major advantage of OTFTs with compete solution processing (e.g. ink-jet printing) is that it is easier to compensate for dimensional instability of the plastic substrate [15] during backplane processing. However, the OTFT is at an early stage of development, and the TFT stability issues remain to be thoroughly investigated, and much technology development is required for it to reach the maturity level of the current a-Si TFT technology.

Based on the relative status of these TFT technologies, we have selected 150^{o}C a-Si TFT approach for fabrication of backplanes on plastic substrates for demonstration of the plastic AM OLED displays.

3.2. Pixel Circuit Design Options Using a-Si Technology

OLED must be driven by a constant current to control its luminance (graylevel), unlike the LCD, which is voltage driven. Figure 4 shows the basic current driven pixel circuit for an AM OLED. This circuit consists of a select transistor T1, a drive transistor (current source element), T2, and a storage capacitor Cs. During the row select period, select transistor T1 turns on and transfers the voltage (data) signal from the column electrode to the gate of the drive transistor T2. After the addressing period, T1 is switched-off, and the programmed voltage (data) is held on the gate of T2 for the rest of the frame time. The storage capacitor, Cs prevents discharge of the T2 gate node (by leakage through T1) to any appreciable degree. Thus Cs allows continuous driving of the OLED by T2 while the other rows in the display are addressed sequentially. When T2 is biased in saturation ($|V_d| > |V_{gs}- V_t|$), it behaves as a constant current source, with the current, I_{sd}, given by:

$$I_{sd} = K . \mu_{fe} . (V_{gs}-V_t)^2$$

Where K is a constant based on the transistor size and the gate capacitance, μ_{fe} is the field effect mobility V_{gs} is the gate-source voltage and V_t is the threshold voltage. This ensures that the OLED pixel is driven by a constant current provided by T2 operating in the saturation regime with the programmed gate (data) voltage. This addressing scheme works well when the TFT performance is uniform across the display surface. Because the pixel current (current through T2) is proportional to $(V_{gs}-V_t)^2$ and μ_{fe}, any non-uniformities in the threshold voltage and mobility will result in pixel luminance variations.

Generally, a PMOS transistor is used for the AM OLED pixel driving, using a bottom emission structure with the light emission through ITO anode at the bottom. Connecting the OLED to the drain side of the TFT ensures that the gate-source (V_{DD} bus) bias across the drive TFT is held constant to achieve a constant current drive. However when using the n-channel a-Si TFT, the power supply (V_{DD}) bus will be connected to the TFT drain, and the OLED will be on the source side the TFT. With this configuration, the drive TFT gate voltage is divided between the TFT gate-source voltage, V_{gs}, and the OLED (V_{OLED}). Any variations in the OLED devices across the display will result in variation in V_{gs} and thus variations in the drive current and the luminance. Thus an n-channel TFT cannot provide a constant current, when the OLED properties vary across the display surface. The basic voltage programmed current source design (Figure 4) could provide adequate uniformity in small size displays. However, large-sized displays may require current programmed pixel circuit designs that compensate for some level of TFT and OLED variations to achieve the required display uniformity.

There are many current programmed pixel drive circuits reported in the literature. While the basic operating principle in all these circuits is similar, the detailed architectures are different. In current programmed pixel drive circuits, the data signal is provided as a current rather than a voltage. During the pixel addressing period, the pixel circuit comprising multiple (typically 4 to 5) TFTs facilitates biasing the pixel drive TFT to conduct the selected data current and serves to compensate for the variations in the TFT and OLED at the pixel. For the present effort we selected the simple 2 TFT per pixel voltage drive mode for demonstrating the flexible AM OLED.

4.0. AM OLED TEST CHIP

4.1. Test Chip Design and a-Si TFT

In conventional a-Si:H TFT fabrication for AMLCDs, the highest temperature step in the entire process is in the range of 300-350^{o}C, which has historically been needed to insure high mobility and low gate leakage. For the plastic substrate selected, the circuit fabrication processes must not exceed 150^{o}C. For compatibility with this substrate, we have developed an a-Si:H TFT process with 150^{o}C maximum temperature. Using plasma-enhanced chemical vapor deposition (PECVD), high quality TFTs with low gate leakage and high mobility have been fabricated at this low temperature of 150^{o}C [13]. To further develop the 150^{o}C process, and to verify active matrix pixel circuits for polymer LEDs, we designed and fabricated a test chip using both glass and plastic substrates.

Figure 5 shows a schematic cross section of the integrated TFT/PLED structure used in the test chip. The fabrication process starts with ITO deposition and patterning, so that conventional ITO suppliers (supplying ITO on bare substrates) can be used. Then a chromium (Cr) layer is deposited by thermal evaporation and patterned as the bottom gate electrodes of the TFT's. SiN_x, intrinsic a-Si, n^+ a-Si layers are then deposited by PECVD, followed by another Cr layer as the source/drain metal contacts. After patterning of the n^+ a-Si layer to define the channel and patterning of the intrinsic a-Si to define the TFT island, contact holes are etched through SiN_x for contacts between interconnect metal and gate metal. Then aluminum is deposited and patterned as the interconnect metal. Finally, a thick SiN_x layer is deposited as the passivation layer and a window is etched to expose the ITO for the PLED. After cleaning, the polymer layers for the PLED are then deposited, the cathode is deposited and the active area is sealed for environmental stability. Figure 6 shows a picture of the finished test chip.

4.2. TFT Performance

The TFT performance on glass and plastic substrates is found to be similar. Figure 7 shows the typical transfer characteristics of TFT's on glass (a) and plastic (b) substrates. We can see that high quality gate dielectric SiN_x is achieved at 150°C based on the gate leakage current being comparable to that from standard 300-350°C TFT's. The threshold voltage is low (2 V for glass, and 2.4 V for plastic) and comparable to conventional TFT's fabricated in the range of at T_{MAX} = 300-350°C. Also, the mobility at 150°C is comparable to the conventional high temperature a-Si TFT mobility. The 150°C TFT on glass (Figure 7A) shows a mobility of 0.67 $cm^2/V{\cdot}S$, and the TFT on plastic in Figure 7B shows a mobility of 0.7 $cm^2/V{\cdot}S$. This mobility is sufficient for providing the current drive necessary for driving a PLED display using the selected PLED materials.

4.3. AM OLED pixel circuit performance:

Several candidate pixel drive circuits were implemented in the test chip. In this section we will discuss the performance of a 2 TFT/Pixel test drive circuit (Figure 4). In this circuit, the switching transistor T1 is implemented as two TFT's of W/L= 20um/5um in series to achieve a low leakage current. The driving transistor T2 has a W/L = 80um/5um, and its source connected to the anode of the PLED. The storage capacitor C is ~2 pF. Figure 8 shows the picture of a 5x5 test pixel array in the test chip being driven with a QVGA timing, with a data voltage of 10 V. (Note that one row contact is missing, and hence only 4 rows are seen in the figure).

Figure 9 shows the pixel drive current vs. programming data voltage applied to the pixel on a glass substrate. For an average pixel brightness of 100 cd/m^2, only 6V of data voltage input is required to achieve the target current of 1.8μA. The data voltage at which the pixel current saturates depends on the select voltage, because this determines the cutoff of T1. Pulsed operation under different timings shows that leakage current in T1 is very small (< 10^{-11}A), and the data is accurately latched in the pixel for the entire frame time. Similar results are achieved on plastic substrates. These results from the test chip show that low temperature (150°C) a-Si TFT's on plastic or glass substrates can provide adequate drive current for driving AM PLEDs at low (< 10V) driving voltages and have the necessary low leakage current for active matrix operation.

5.0. DEVELOPMENT AND DEMONSTRATION OF AM OLED-ON-PLASTIC SUBSTRATE

To develop the complete TFT backplane processes and to test and verify the feasibility of fabricating AM OLEDs on flexible plastic substrates we selected a 64 x 64 pixel test display vehicle. In the following we will discuss the design of this test display, backplane process development and fabrication using 150°C a-Si TFTs, AM OLED fabrication on plastic substrates, drive electronics development, and display test and demonstration.

5.1. Backplane Design and Fabrication

This developed test display has a resolution of 80 dpi (monochrome), with a pixel pitch of 300 x 300 microns. Backplanes for three such displays are fabricated on a 4" dia. PEN plastic wafer (substrate). Figure 10A shows a picture of the processed plastic wafer with three 64x64 pixel backplanes and test structures and process control monitors. We have also demonstrated the feasibility of fabricating larger and higher resolution backplanes as shown in Figure 10B with 160(x3) x160 array for an 80 dpi color AM OLED. However, in the following we will focus on the 64x64 pixel monochrome AM OLED fabricated on PEN flexible plastic substrate. As the current focus of the development is demonstrating the general feasibility of AM OLEDs built on plastic substrates using 150°C a-Si TFT process, we selected the simple 2 TFT per pixel circuit shown in Figure 4, for the 64x64 pixel test display. We developed a 7-mask a-Si TFT backplane processes using a channel passivated type inverted staggered a-Si TFT structure. The backplane process starts with the deposition of a 3000Å thick PECVD SiN_x layer, followed by a-Si TFT array fabrication, ITO pixel electrode (anode for the bottom emitting OLED structure) fabrication, and ends with an overcoat layer with a window etched at the pixel region.

We have demonstrated the feasibility of fabricating 150°C a-Si TFTs with high mobility and low-leakage current with adequate "on" current (~5μA) and low "off" current (~ 1 pA) for driving an AM OLED pixel using glass substrates. We fabricated AM OLEDs using the 64x64 pixel 150°C a-Si TFT backplanes on glass substrates, and verified the mask and display designs by verifying the functionality of the displays fabricated. However, translating the developed glass substrate based process on to a flexible plastic substrate was a major challenge. The challenges we encountered in the

fabrication of plastic backplanes included management of issues related to: a) shrinkage (lack of dimensional stability) of the plastic substrate at the 150°C process temperature, b) differential thermal expansion coefficients (TCE) between the plastic substrate and the thin films used in the TFT backplane structure, c) handling the 125 μm thick flexible substrate in the process equipment designed for use with rigid glass substrates of about 0.7 mm thickness, and d) surface imperfections (scratches, embedded particles etc.,).

The need for dimensional stability of the plastic substrate can be illustrated when we consider the typical design rules used in the TFT backplane fabrication. For a typical 3 μm design rule used (for a contact via, as an example), a shrinkage (mis-alignment of) more than 1.5μm is problematic. The as received heat stabilized PEN shrinks by about 0.05 % during TFT backplane processing. This translates to a mis-alignment of 300 μm over a span of 60 mm (the region over which three 64x64 pixel backplanes are fabricated in the 4" dia. plastic wafer). Clearly, this level of shrinkage (dimensional in-stability) is not acceptable. We have successfully increased the dimensional stability of these substrates by pre-annealing (pre-shrinking) the substrates prior to the TFT backplane fabrication. With the developed pre-stabilization process, we reduced the shrinkage during TFT backplane processing to 1.5 μm over a 60 mm span (~ 25 ppm or 0.0025 %). This has allowed successful fabrication of the three 64x64 pixel backplanes using the mask set that we designed for use with 4" dia. wafers.

The problems due to CTE mismatch are addressed by proper choice of thin film materials used in the TFT array fabrication, and optimization of the TFT array fabrication process. Similarly, appropriate changes have been made to some process tools to handle flexible plastic substrates. Figure 11 shows a photograph of a pixel in a fabricated 64x64 pixel backplane. These backplanes are characterized for the a-Si TFT performance and its uniformity, and the plastic substrate / process induced defects such as pixel defects and line defects, and then used for the AM OLED fabrication.

5.2. OLED Display Fabrication

The fabricated backplanes were used to assemble AM OLEDs by integrating them with OLED devices and interconnected to the display drive electronics. The AM OLED fabrication process consisted of first depositing a PDOT layer. After drying the PDOT layer, Super Yellow emissive polymer (a poly(phenelene vinylene)-type polymer from Covion) was deposited and dried. Finally, the cathode was deposited, and the entire structure was then encapsulated with a glass lid. (Note that our future vision is to protect the AM OLED structure using another flexible plastic substrate with adequate oxygen and moisture barrier properties). The row and column bond pads on the display are then connected to the display drive electronics using flex cables with a heat seal connection scheme.

For exercising the 64 x 64 pixel AM OLEDs fabricated for test and evaluation, we designed a versatile drive electronics system. Figure 12 shows the architecture of the developed drive electronics system. The 2-TFT-pixel circuit used in the 64x64 AM OLED display requires a voltage-drive for pixel data. The display is driven with voltages representing gray-scale pixel data on the column (data) lines, an enable pulse on the row (scan) lines and a DC voltage for pixel drive. Since no suitable commercial gray-scale driver was available for a display of only 64 columns, a simple 64-channel sample and hold (S/H) circuit was devised for the column driver. Analog VGA data is amplified and level-shifted such that it corresponds with the optimal operating range of the display under test. A 1:64 multiplexer switches the pixel data to the appropriate hold amplifier; one for each column of the display. Use of high-impedance amplifiers reduces voltage sag on each column throughout the select line time.

A COTS driver IC was selected for the row driver. This IC is capable of driving 80 output channels with a voltage swing of up to 20v. The driver IC consists of a bidirectional shift register (1 in, 80 out) and two banks of 80 analog switches – each bank connected to two different supply voltages, thus allowing independent adjustment of select and deselect pulse voltages. The desired bank of switches is selected using the polarity inversion signal, POL. Although the polarity inversion feature is not used with an OLED display, it is utilized here as a method of driving a backplane using either n or p-channel TFTs. At the heart of the drive electronics is the timing generator. A programmable logic device utilizes VGA (640x480x60p) synchronization signals and an on board clock to generate all the necessary control signals for the column and row drivers. Since the display of concern is 64 pixels by 64 rows, the VGA signal is mapped to the display via pixel decimation. The pixel clock for the sample-and-hold is 1/10 frequency of the VGA clock and the row shift clock is 1/7.5 of the VGA horizontal sync frequency. To allow for maximum flexibility, all display drive voltages are made adjustable.

Figure 13 shows the photograph of a first 64x64 pixel AM OLED fabricated on a plastic backplane using 150°C a-Si TFTs, and displaying text image "DARPA" in a dark and bright background. While this display had several pixel defects and some artifacts related to the drive electronics used, it was found to be generally functional and capable of displaying grayscale images. The surface quality of the plastic substrate was found to be an important variable on the quality of the backplane with respect to defects. Displays made using plastic substrates with improved substrate surface quality were found to result in backplanes and displays with fewer defects as illustrated in Figure 14 showing "test images" in a 64 x 64 AM OLED.

7.0 SUMMARY

We have developed 150°C a-Si TFTs with a mobility and leakage current comparable conventional high temperature (~300°C) a-Si TFT processes, for fabrication of flexible AM OLEDs using plastic substrates. PEN based substrates with a thickness of 125 microns that are suitable for backplane processing have been developed. Also, we developed the backplane processes using the PEN substrate and 150°C a-Si TFT process. Using these enabling developments we designed, fabricated and demonstrated a world's first AM OLED on a flexible plastic substrate using 150°C a-Si TFT technology. This technology shows a promise for fulfilling the future flexible display application requirements.

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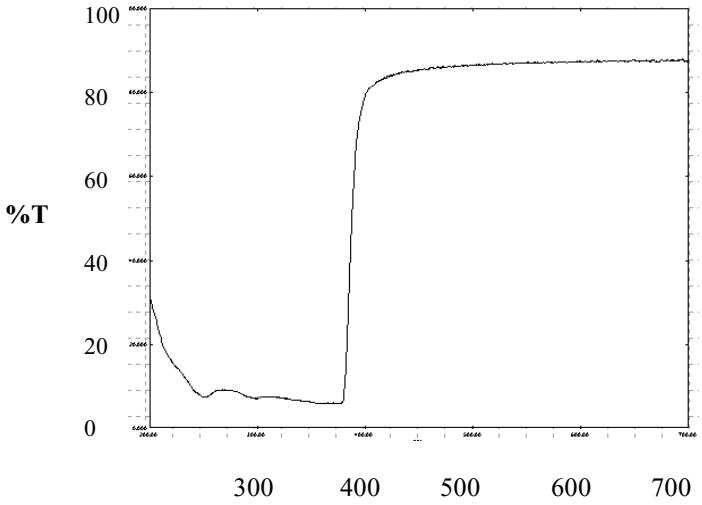

Figure 1: Transmission Curve for PEN Substrate

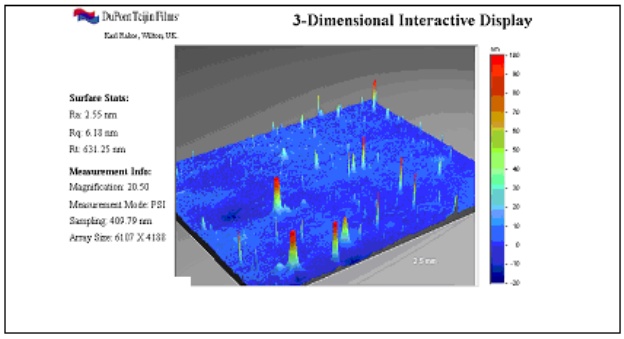

Figure 2A. Surface Smoothness of industrial Grade PEN

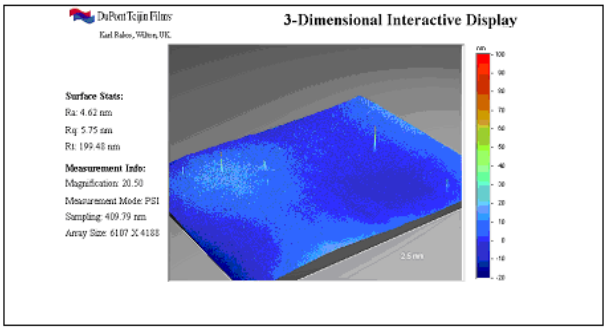

Figure 2B. Surface Smoothness of Untreated Teonex® Q65

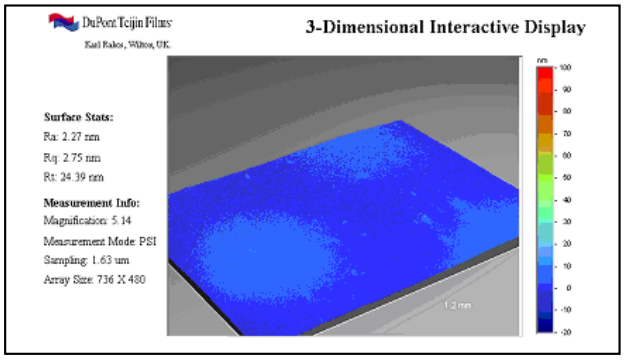

Figure 2C. Surface Smoothness of Surface Tailored Teonex® Q65

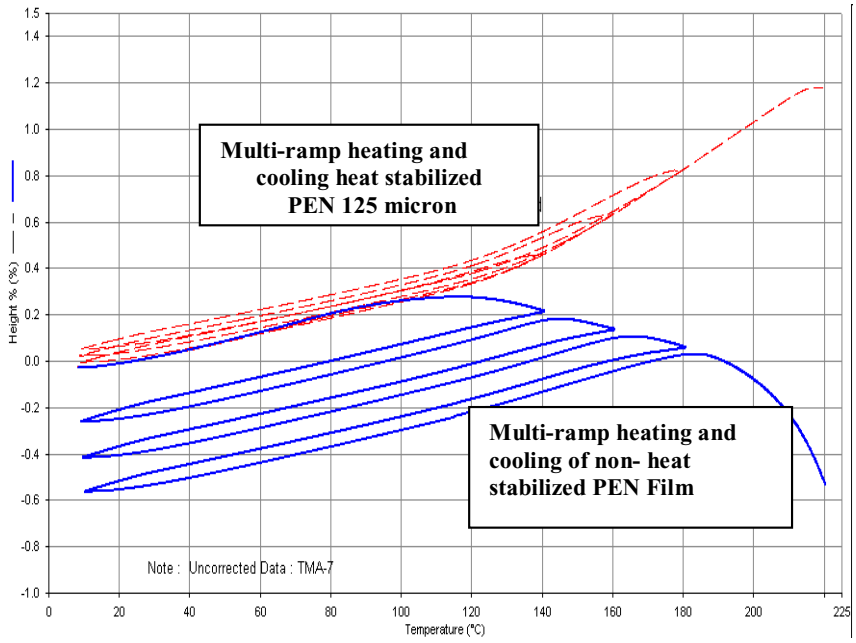

Figure 3. Thermal Mechanical Analysis of Heat Stabilized and non-Heat Stabilized PEN Film

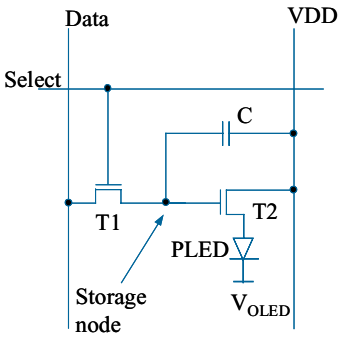

Figure 4. 2TFT / Pixel AM OLED Pixel Drive Circuit

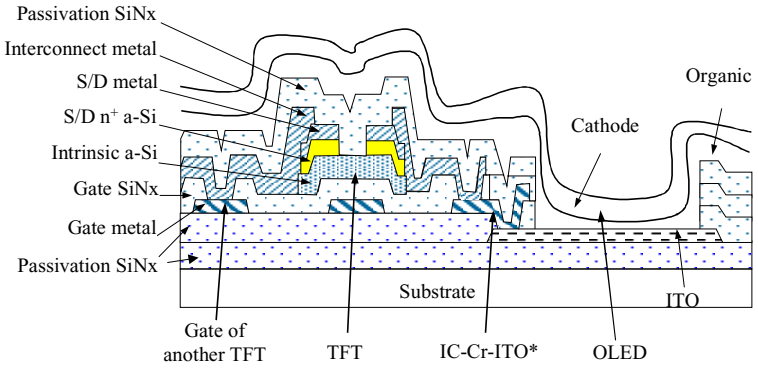

Figure 5. Cross section of integrated TFT/PLED structure

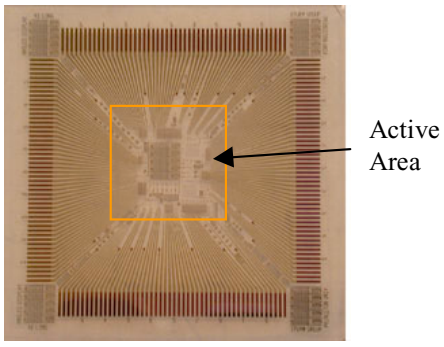

Figure 6. Picture of AMPLED test chip (75 x 75 mm^2)

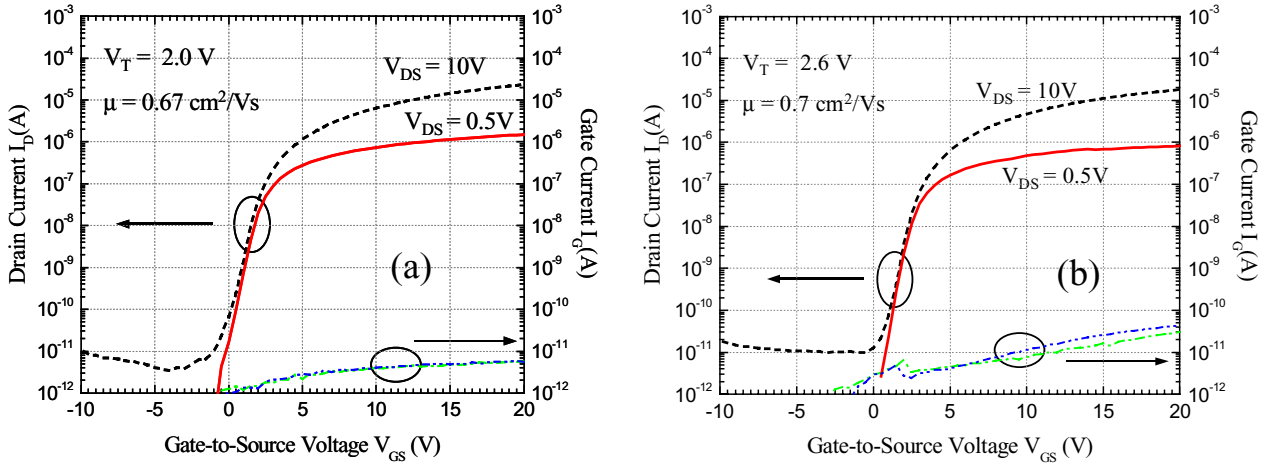

Figure7 Transfer characteristics of TFT's on (a) glass (b) plastic substrates

Fig. 8. 5 x 5 AMPLED test array on glass (one row contact missing) with V_{DATA} = 10V.

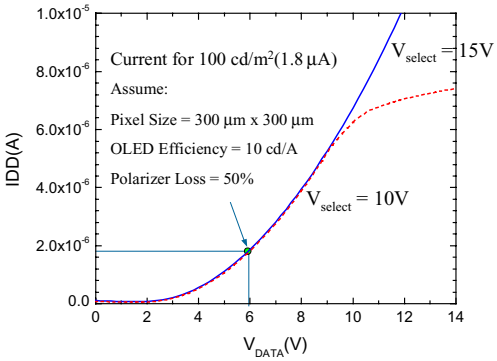

Fig. 9. PLED drive current through T2 versus programming voltage for pixel circuit on glass.

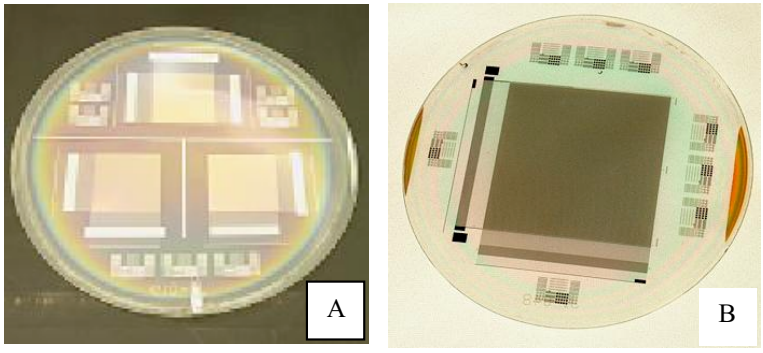

Figure 10: Photographs of a-Si TFT backplanes processed on a 4" diameter Teonex® Q65 flexible plastic backplanes: A) Substrate with three 64x64 pixel arrays , B) Substrate with one 160(x3)x 160 pixel array

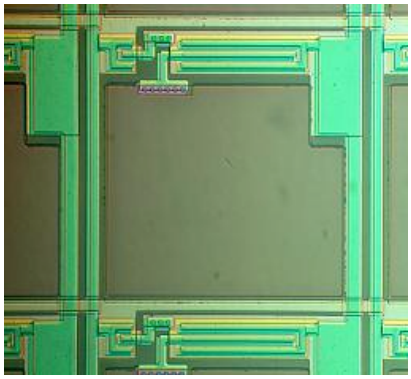

Figure 11: Photograph of an AM OLED pixel in the processed backplane

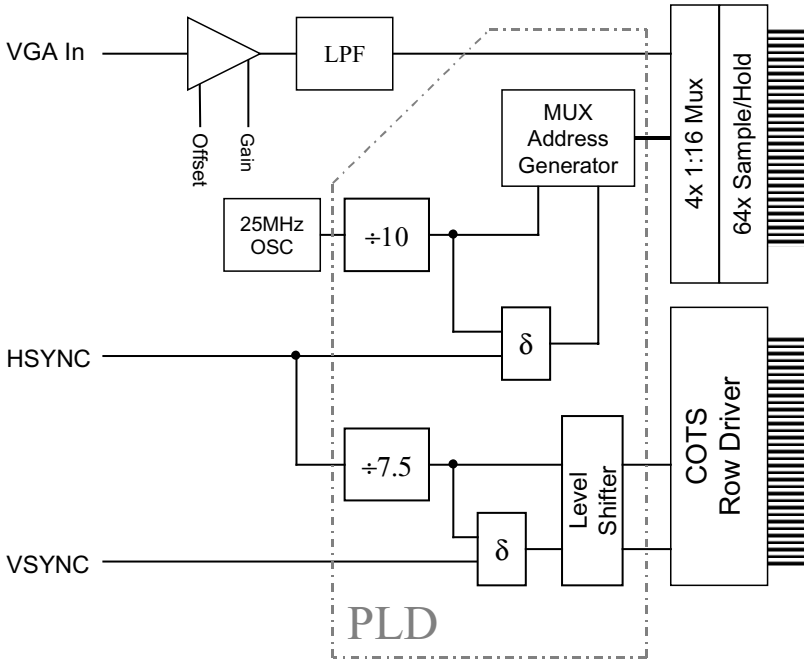

Figure 12: Display drive electronics used for driving the 64 x 64 pixel arrays

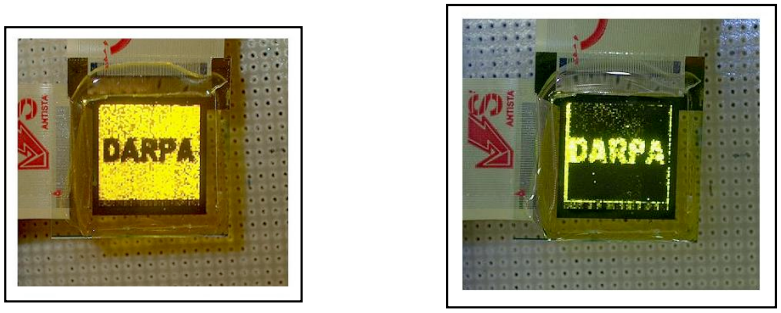

Figure 13: Test images on a first 64 x 64 pixel AM OLEDs fabricated on a flexible substrate

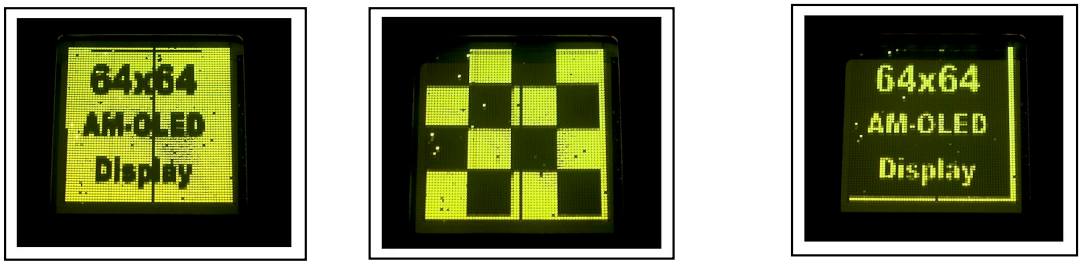

Figure 14: Test images on a 64 x 64 pixel AM OLED fabricated using a flexible substrate with improved surface quality