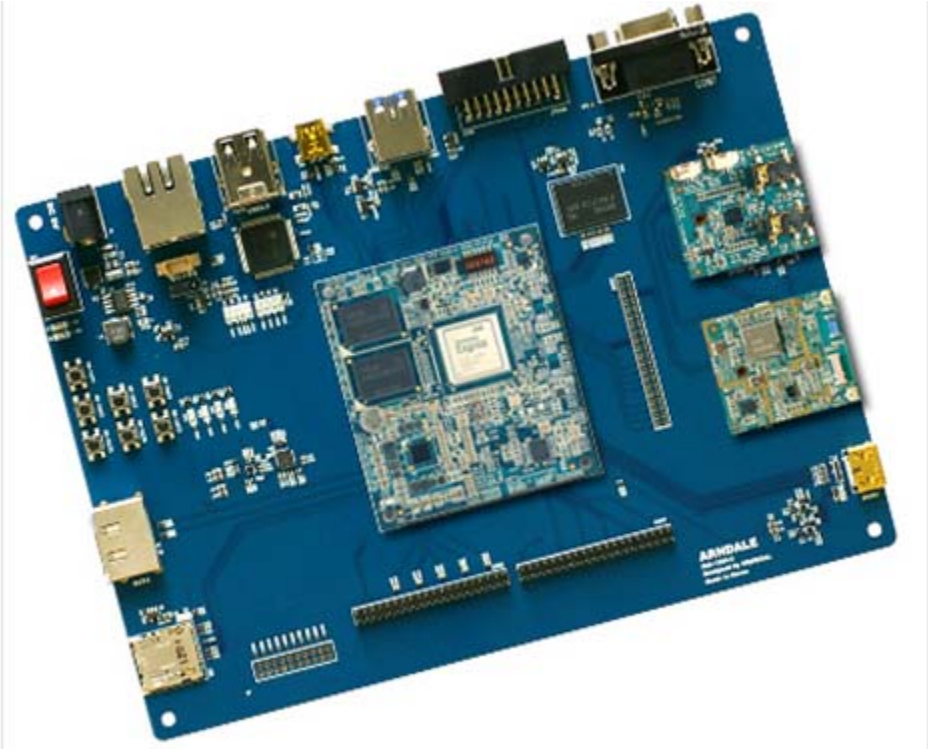
ARNDALE 5 Base Board
System Reference Manual

(Version 1.0)



InSignal

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1. Revision History

날짜	내용	Rev No.	작성자
2012/08/01	Preliminary Release	0.1	FELIX
2012/11/01	Re-release after initial feedback	1.0	FELIX

2. Overview

ARNDALE Board, a new community development board designed around its Exynos 5 Dual system-on-chip (SoC) offers World 1st Cortex-A15 dual core CPU speed, remarkable 3D GPU performance (72GFLOPS) with OpenGL/ES and OpenCL and World's highest resolution support (24bit 2560X1600@60fps).

The Exynos 5 Dual features the implementation of both the world's first dual-core ARM® Cortex™-A15 MPCore™ processor and the world's first quad-core ARM Mali™-T604 GPU based on 32nm High-K Metal Gate (HKMG) process technology.

The Newest board offers the open source developer community a rich environment for producing the highest caliber of mobile applications, including in the areas of Tablet, gaming, security, multimedia, and user interface on multiple operating systems.

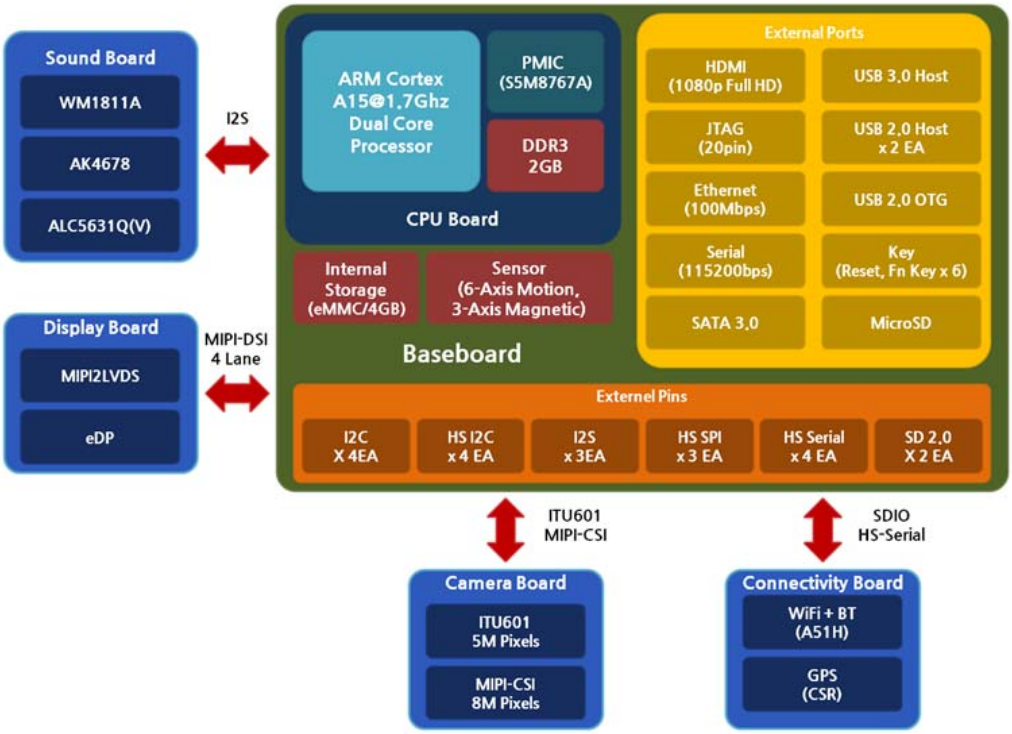
3. Characteristics of Product

- Support ARNDALE 5 DUAL CPU BOARD
  - 1.7 GHz Cortex-A15 dual core subsystem with 64/128 bit SIMD NEON
  - 32KB(instruction)/32KB(DATA)L1 Cache and 1MB l2 Cache
  - 32-bit 800 MHz LPDDR3/LPDDR2 2GB

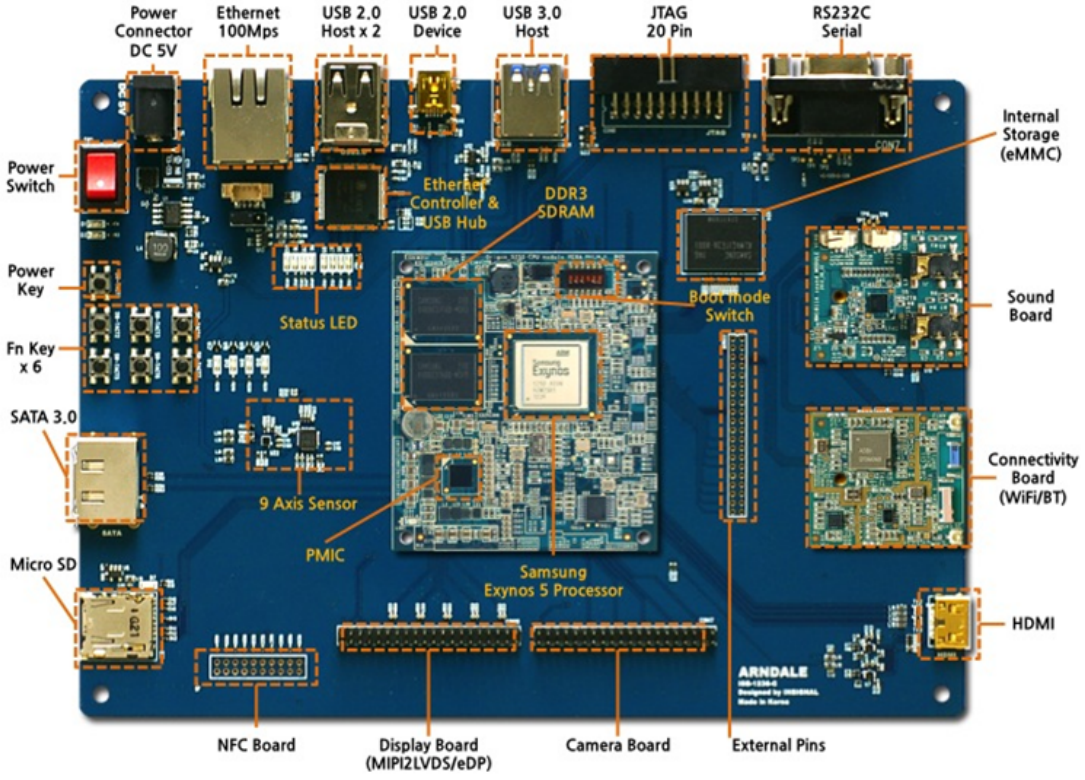
- Support ITU 601 camera Interface
- Support HDMI 1.4 interfaces with on-chip PHY
- Support MIPI DSI Standard Specification V1.01r11
- Support MIPI CSI standard specification V1.0 Tow ports
- Support USB3.0 Host 1-channel that supports SS(5Gbps) with on-chip PHY
- Support USB2.0 Device 1-channel that supports LS/FS/HS with on-chip PHY
- Support USB2.0 Host 2-channel that supports LS/FS/HS with on-chip PHY
- Support USB HSIC 1-channel that supports 480Mbps with on-chip PHY
- Support 10/100Mbps Ethernet One Port
- Support SATA 1.0/2.0/3.0 interface
- Support One channel eMMC 4.41 DDR in 8bit 4GB
- Support One channel SDIO 3.0
- Support One channel SD2.0
- Support Four channel high-speed UART(up to 3Mbps data rate for Bluetooth 2.0 EDR and IrDA 1.0SIR)
- Support Three channel high-speed SPI
- Support Three channel 24-bit I2S audio interface
- Support Four channel I2C interface support , up 400kbps
- Support Four channel HS-I2C up to 3.1Mps
- Support Configurable GPIOs
- Support 6EA Configurable Button
- Support 4EA Configurable LED
- 1EA Power on Button
- Hold currents up to 2.3A
- INPUT POWER DC5V

4. BLOCK DIAGRAM

4.1 H/W BLOCK DIAGRAM



4.2 BASE BOARD SYSTEM BLOCK DIAGRAM



5. Specification

5.1 H/W Specification

	Item	Features	Reference
System	**CPU**	Cortex-A15 Dual CPU MODULE	
Interface	**Serial Port**	UART 2 Baud Rate : 115200bps	Debug
	JTAG Port	JTAG 20Pin Box header	Debug
	USB 3.0 HOST	USB HOST 3.0 1port	Up to 500mA
	USB 2.0 HOST	USB HOST2.0 2ports	Up to 500mA
	USB 2.0 Device	USB Device2.0 2port	
	SD/SDIO	SD/SDIO CARD Version2.0	
	eMMC	eMMC4.41 DDR in 8bit	
	HDMI	HDMI1.4a 1080p 60Hz	
	TFT-LCD	7” 1024 x 600 LVDS	
	MIPI DSI	MIPI DSI Standard Specification V1.01r11	
	MIPI CSI	MIPI CSI standard specification V1.0	
	HSIC	USB 2.0 HSIC	
I/O	**POWER SW**	1 X Push Button	
	Function SW	6 X Push Button	
	LED	4 X GPIO	
Network	**1 LAN Port**	1 x 10/100Mbps Auto detection	WAN/LAN
Power	**INPUT POWER**	5V / 3A	
	Power Consumption	Min : 5V / 160mA (Client sleep mode) Normal : 5V / 750mA	

5.2 H/W Environmental

	Item	Features	Reference
Power	**INPUT POWER**	5V / 3A	
	Power Consumption	Normal : 5V / 750mA	
Environmental	**Temperature**	Operation : -0℃~ 50℃ Storage : -10℃~80℃	
	Humidity	Operation : 10% to 80%, Non-Condensing Storage : 5% to 90%, Non-Condensing	
Mechanical	**Dimension**	140mm X 195mm	
	Weight		

6. ARNDALE 5 BaseBoard System Architecture and Design

6.1 Input Power

The 5VDC input power is supplied from the input DC jack at J1

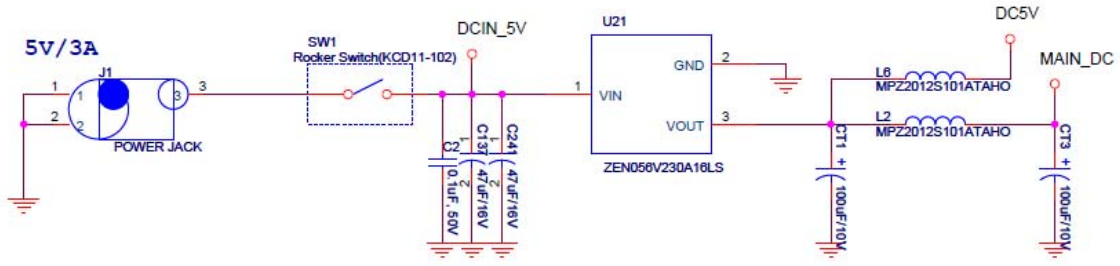


Figure 1 – ARNDALE BaseBoard Input Power Section.

CAUTION: only use a 5VDC regulated power supply to power the ARNDALE BaseBoard. Connecting a supply with an output higher than +5VDC could cause possible board damage.

6.2 Debug UART Interface

A single RS-232 port is provided on the ARNDALE BaseBoard via 9-pin D-SUB female connector at location CON7.
It provides access to the UART2 interface of the ARNDALE CPU BOARD.
See Figure 2 for the implementation of the RS232 port.

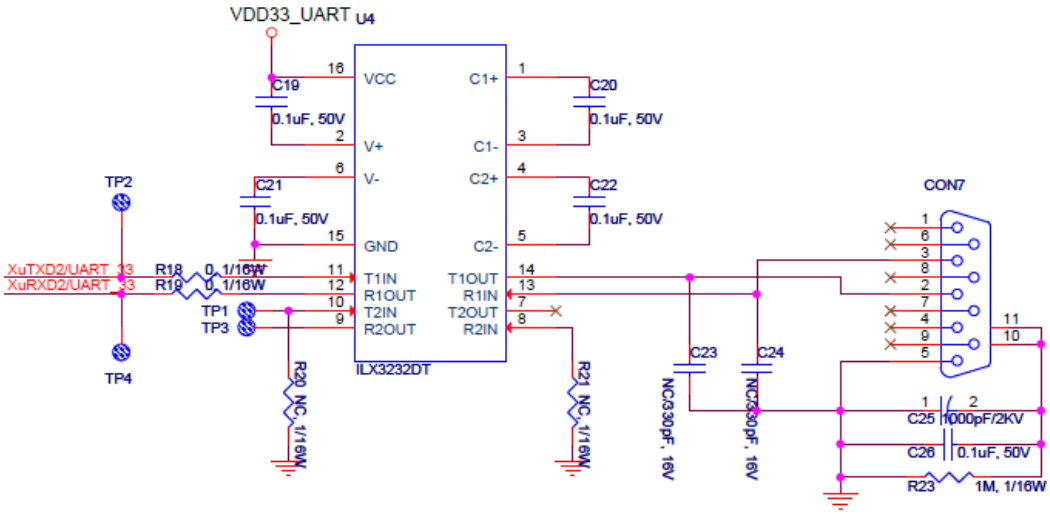


Figure 2 – ARNDALE BaseBoard UART2/RS-232 Section

6.3 Debug JTAG Interface

A JTAG header is provided to allow for advanced debugging on the BaseBoard by using a JTAG based debugger. The JTAG interface uses a 20 pin connector. ARM 2×10 pin used by almost all ARM based systems.

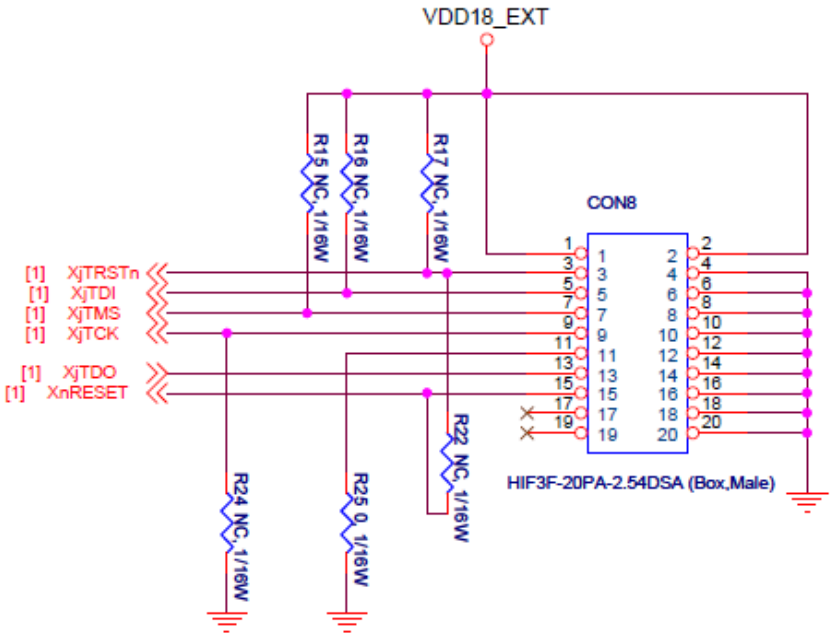


Figure 3 – ARNDALE BaseBoard JTAG Section.

6.4 Micro SD Card Socket

The ARNDALE Baseboard supports removable memory storage via onboard Micro SD card Socket. It is an four-bit card Socket that supports 1.8V cards.

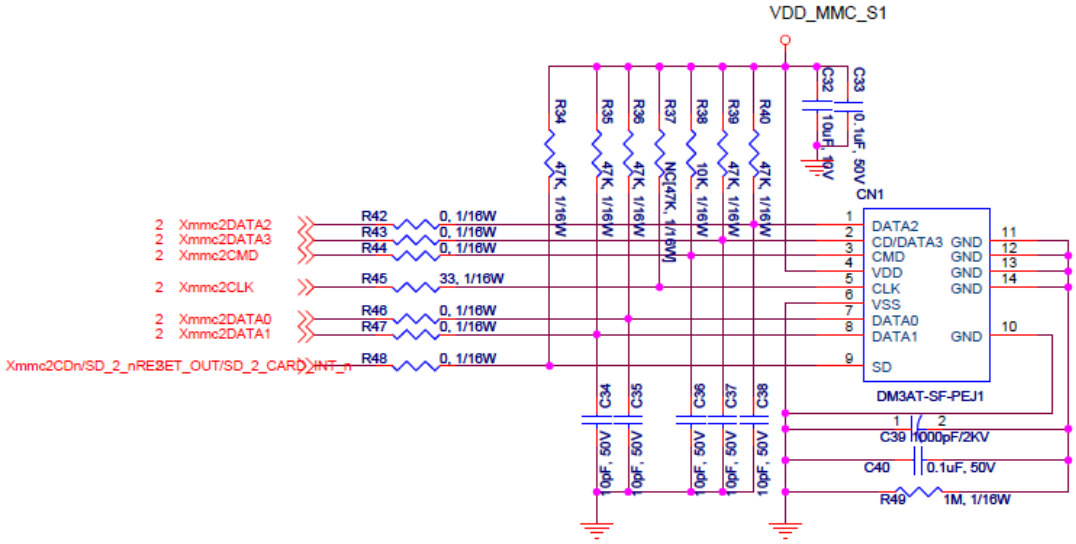


Figure 4 – ARNDALE Baseboard Micro SD Section.

6.5 USB 2.0 Device Connector

The ARNDALE Baseboard uses the USB OTG transceiver within the ARNDALE CPU that is connected to an industry standard mini-AB connector (CON9) as shown in Figure 5.
The default setting of ARNDALE Baseboard supports USB Device.

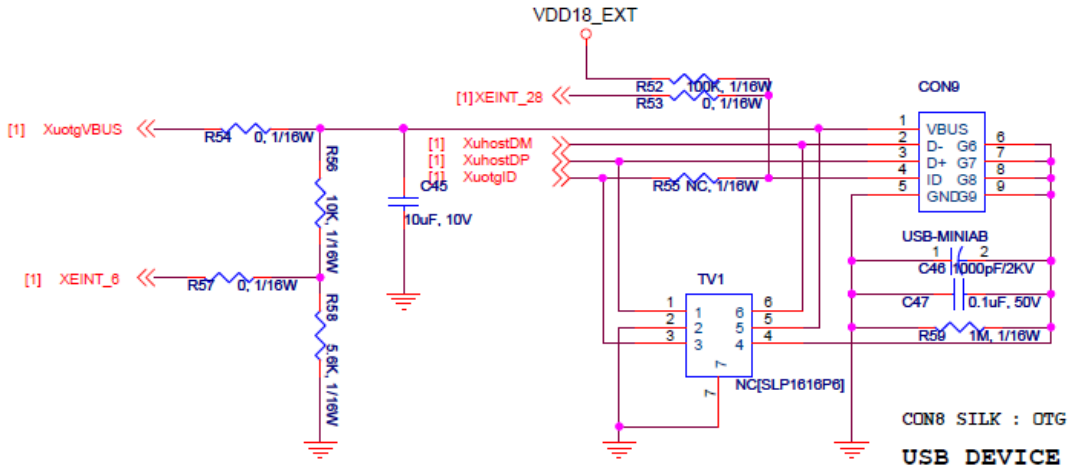


Figure 5 – ARNDALE Baseboard USB 2.0 Device Section.

6.6 USB HOST 3.0 Connector

The ARNDALE Baseboard supports USB HOST3.0 via onboard USB3.0 Standard-A plug.
It supports super-speed (5 Gbps) and high-speed (480 Mbps) and full-speed (12Mbps).
See Figure 6 for the implementation of the USB3.0 A port.

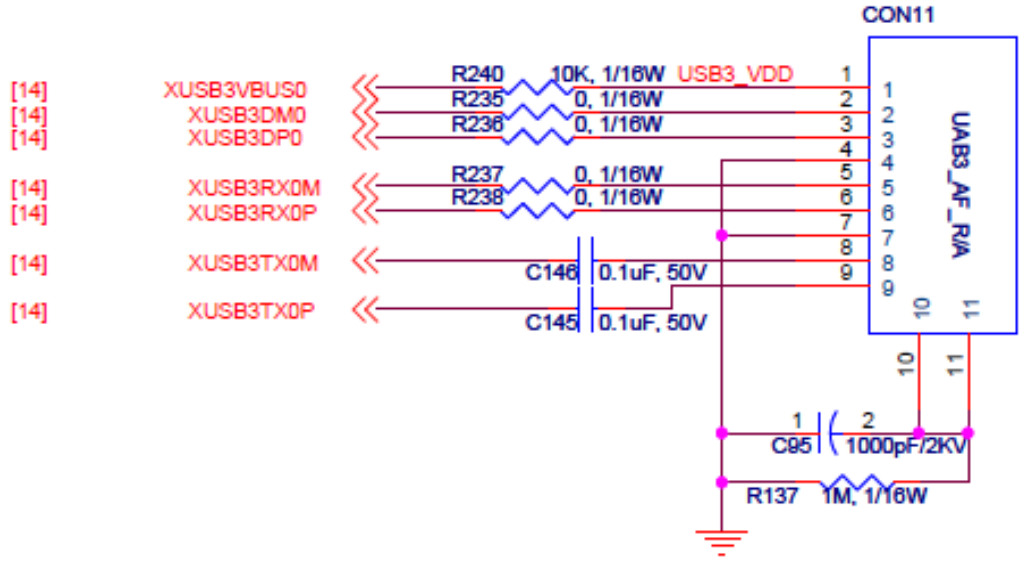


Figure 6 – ARNDALE BaseBoard USB 3.0 HOST Section

6.7 HDMI Interface

The ARNDALE BaseBoard supports a High-Definition Multimedia Interface (HDMI)1.4 compliant (with 3D) via an industry standard Type C connector at location J2.

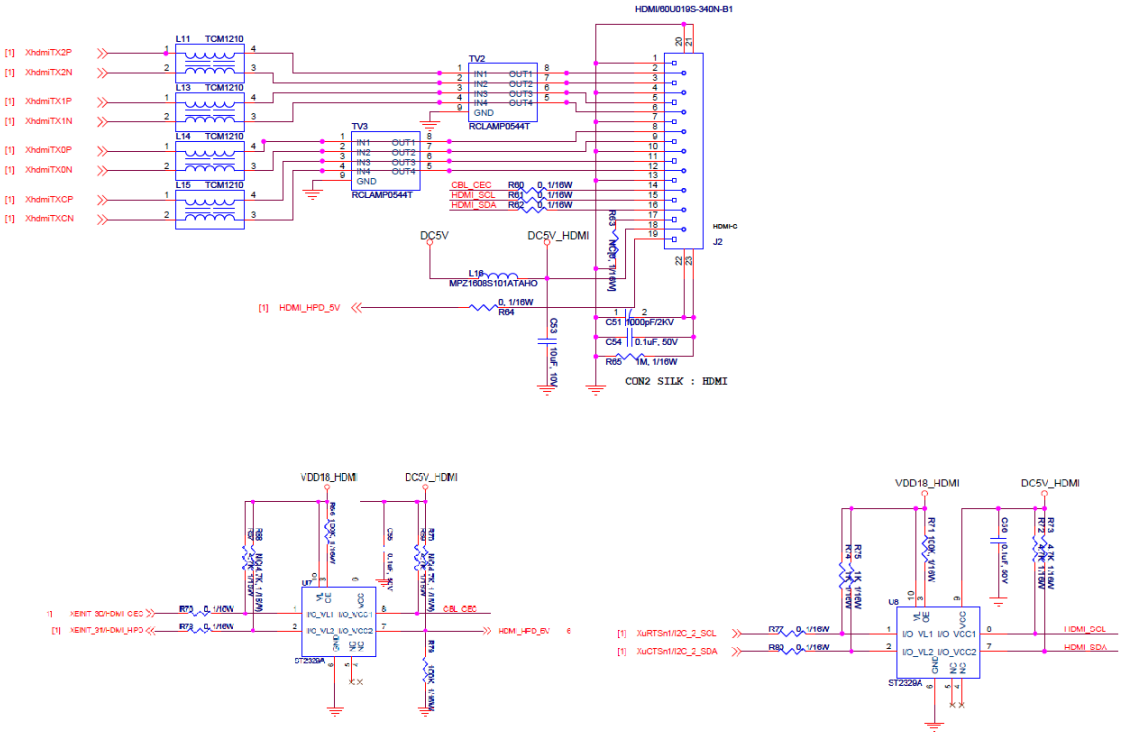


Figure 7 – ARNDALE Baseboard HDMI Section.

Table 1. ARNDALE HDMI Signals

Signal Name	Description	Type	CPU PIN Name
Xhdmi TX2P	HDMI DATA TX2P	I/O	Xhdmi TX2P
Xhdmi TX2N	HDMI DATA TX2N	I/O	Xhdmi TX2N
Xhdmi TX1P	HDMI DATA TX1P	I/O	Xhdmi TX1P
Xhdmi TX1N	HDMI DATA TX1N	I/O	Xhdmi TX1N
Xhdmi TX0P	HDMI DATA TX0P	I/O	Xhdmi TX0P
Xhdmi TX0N	HDMI DATA TX0N	I/O	Xhdmi TX0N
Xhdmi TXCP	HDMI CLK P	I/O	Xhdmi TXCP
Xhdmi TXCN	HDMI CLK N	I/O	Xhdmi TXCN
HDMI_CEC	HDMI Consumer Electronic Control	I/O	GPX3_6
HDMI_HPD	HDMI Hot Plug Detect	O	GPX3_7
HDMI_SCL	I2C clock line	I/O	GPA0_7 / I2C_2_SCL
HDMI_SDA	I2C data line	I/O	GPA0_6 / I2C_2_SDA

6.8 USB HOST 2.0 and Ethernet 10/100 Interface

The ARNDALE BaseBoard used as the upstream USB interface to the AX88760 USB/Ethernet Hub IC.
The Hub IC provides three downstream Host USB ports, and an Ethernet Interface.
Two of the USB host Ports are available via the combo connector CON10.
The Ethernet interface is available via a RJ-45 connector at J7

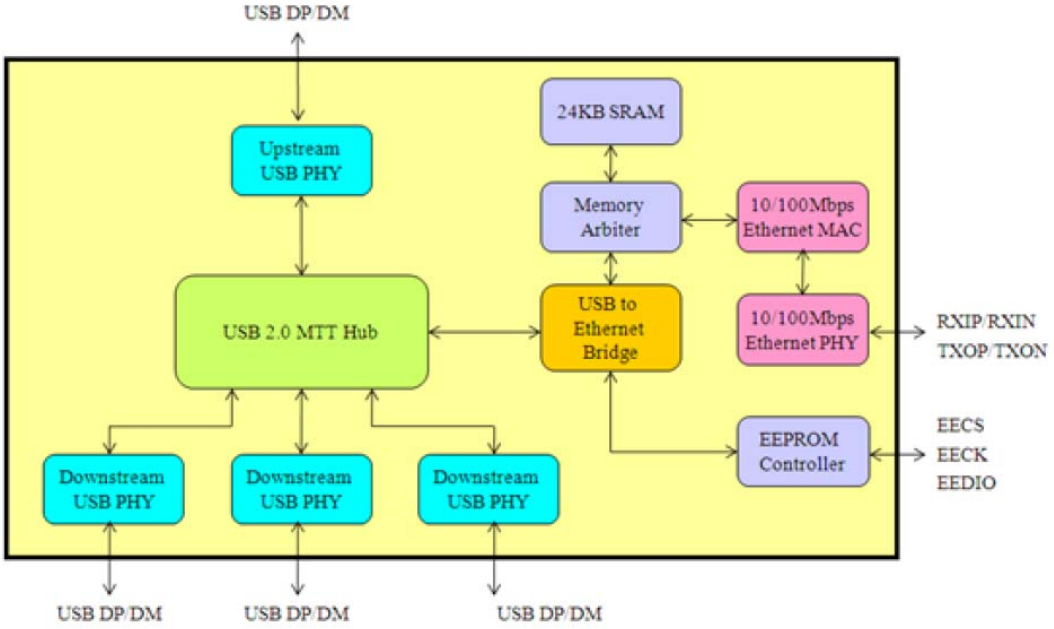


Figure 8 – AX88760 Block Diagram

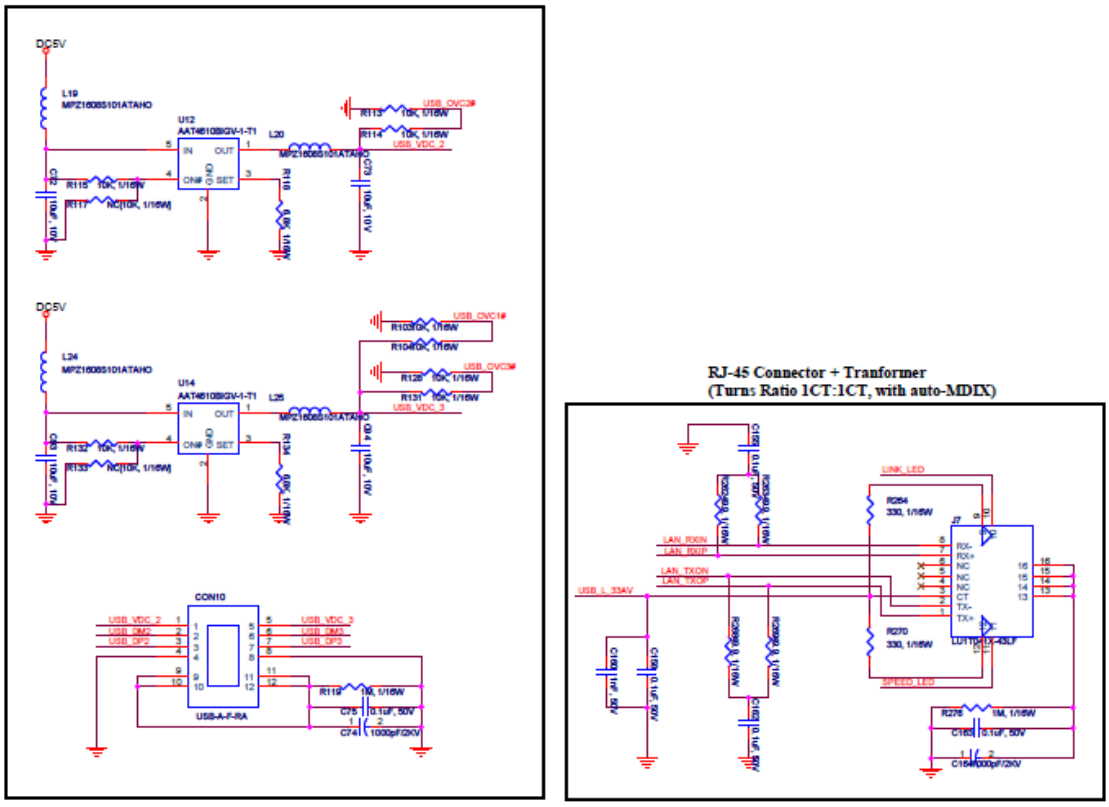


Figure 9 – ARNDALE Basebaord USB HOST 2.0 X2 , Ethernet 10/100 Section

6.9 SATA Interface

The ARNDALE BaseBoard support the Serial Advanced Technology Attachment storage interface via an industry standard Type E-SATA connector J8.
It supports SATA 1.5 Gb/s, SATA 3.0 Ggb/s, SATA 6.0 Gb/s speeds.
It's compliant with SATA Specification 3.0, and AHCI Revision 1.3 specifications.
The SATA interface is available via J8.

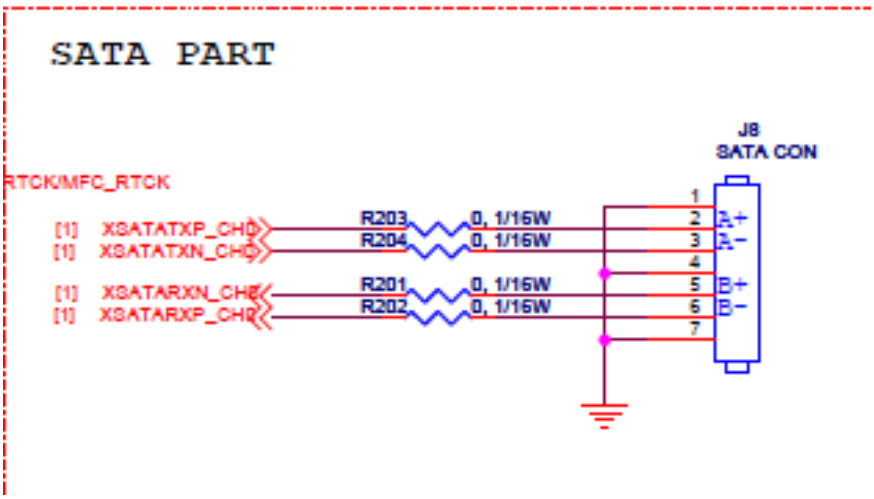


Figure 10 – ARNDALE Baseboard SATA 3.0 Section

6.10 9-AXIS SENSOR

The ARNDALE BaseBoard provide an onboard 9-AXIS Sensor.
See Figure 11 for the implementation of the Sensor section.

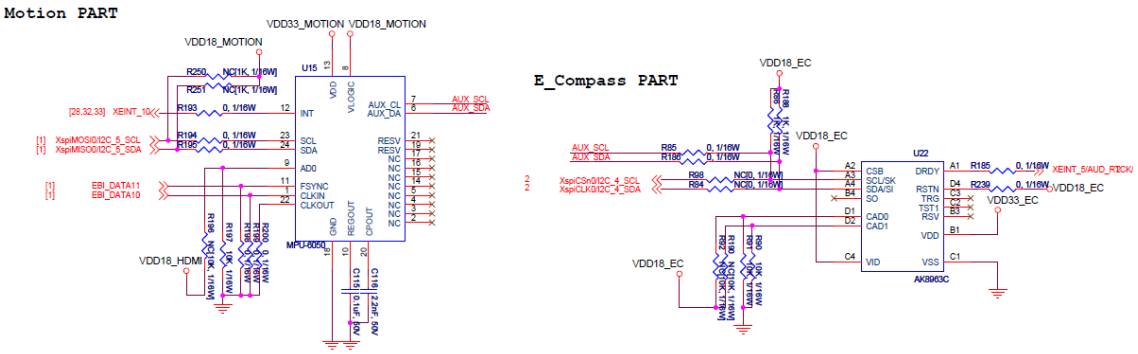


Figure 11 – ARNDALE BaseBoard 9-AXIS Sensor.

Table 2. ARNDALE 9-AXIS Signals

Signal Name	Description	Type	CPU PIN Name
XEINT_10	GPX1[2]/INT1[2]	I/O	XEINT_10
I2C_5_SCL	I2C_5 Serial Clock	I/O	XSPIMOSI_0
I2C_5_SDA	I2C_5 Serial Data	I/O	XSPIMISO_0
EBI_DATA11	GPY6[3]/EBI_DATA[11]	I/O	XSRAMDATA_11
EBI_DATA10	GPY6[2]/EBI_DATA[10]		XSRAMDATA_10
XEINT_5	GPX0[5]/INT0[5]		XEINT_5
AUX_SCL	I2C_Serial Clock to MPU6020		
AUX_SDA	I2C_5 Serial Data to MPU6020		

6.11 eMMC

The ARNDALE Baseboard supports 4GB One channel 8-bit eMMC storage.
It supports MultiMediaCard System Specification Ver. 4.41 compatible.

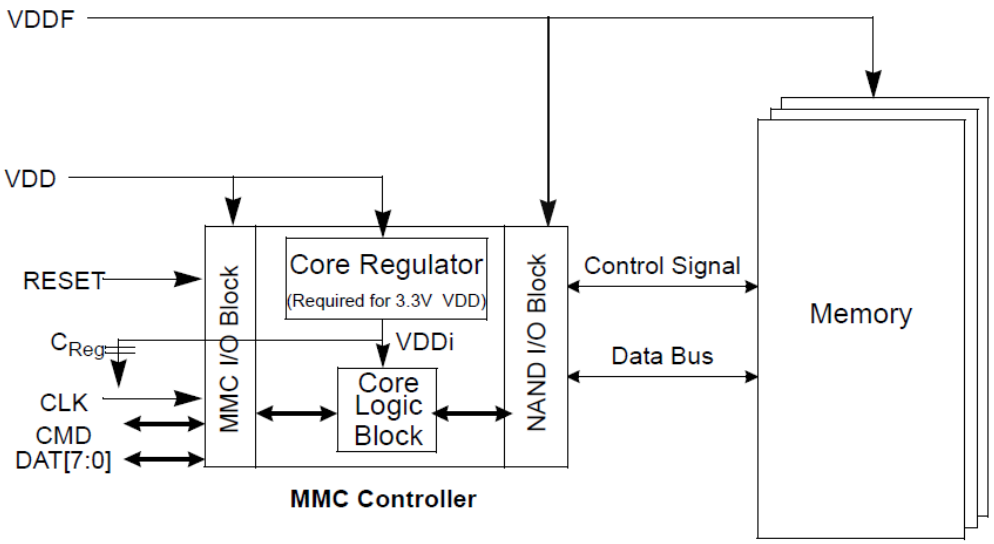


Figure 12 eMMC Block Diagram

Table 3. ARNDALE eMMC Signals

Signal Name	Description	Type	CPU PIN Name
Xmmc0DATA0	Data0 for SDMMC0	I/O	SD_0_DATA[0]
Xmmc0DATA1	Data1 for SDMMC0	I/O	SD_0_DATA[1]
Xmmc0DATA2	Data2 for SDMMC0	I/O	SD_0_DATA[2]
Xmmc0DATA3	Data3 for SDMMC0	I/O	SD_0_DATA[3]
Xmmc0DATA4	Data4 for SDMMC0	I/O	SD_0_DATA[4]
Xmmc0DATA5	Data5 for SDMMC0	I/O	SD_0_DATA[5]
Xmmc0DATA6	Data6 for SDMMC0	I/O	SD_0_DATA[6]
Xmmc0DATA7	Data7 for SDMMC0	I/O	SD_0_DATA[7]
Xmmc0CLK	Clock for SDMMC0	O	SD_0_CLK
Xmmc0CMD	Command for SDMMC0	I/O	SD_0_CMD
Xmmc0CDn	SDMMC0 control signal of VCC/VCCQ	I/O	SD_0_CDn

6.12 User Indicators

There are four user LEDs that can be driven directly from a GPIO pin on the ARNDALE CPU BOARD.
Transistor PDTC114YE is used to drive the LEDs from the DC3V3_MAIN.
A logic level of 1 will turn the LED ON.

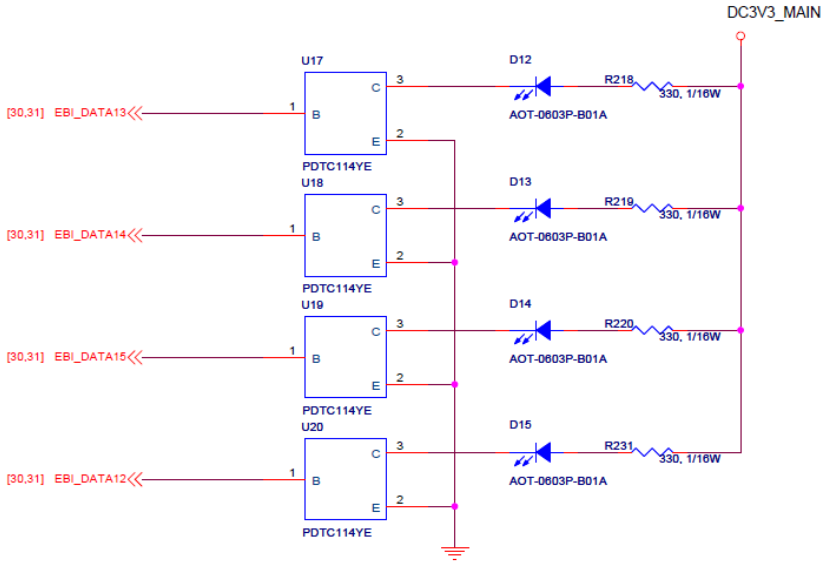


Figure 13 User Indicators

Table 4. ARNDALE eMMC Signals

Signal Name	Description	Type	CPU PIN Name
EBI_DATA12	GPY6[4] / EBI_DATA[12]	I/O	XSRAMDATA_12
EBI_DATA13	GPY6[5] / EBI_DATA[13]	I/O	XSRAMDATA_13
EBI_DATA14	GPY6[6] / EBI_DATA[14]	I/O	XSRAMDATA_14
EBI_DATA15	GPY6[7] / EBI_DATA[15]	I/O	XSRAMDATA_15

6.13 Boot Push Button

SW-TACT1 is a push-button switch that may be depressed to initiate a Power-ON reset of the ARNDALE BaseBoard.

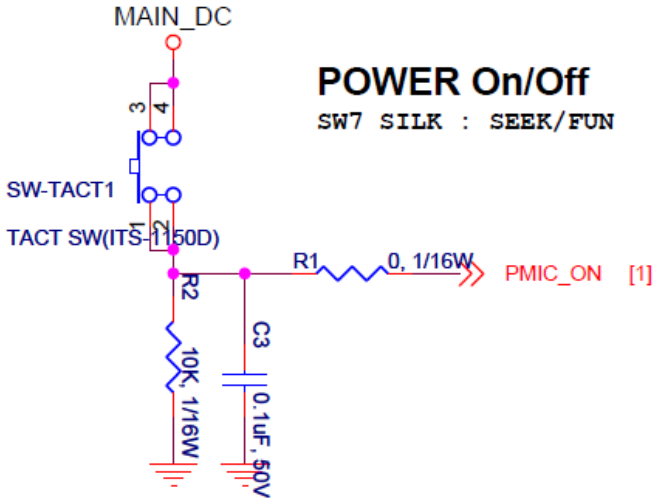


Figure 14 Boot Push Buttons

6.14 User Push Buttons

There are six user Buttons that can be driven directly from a GPIO pin on the ARNDALE CPU BOARD.

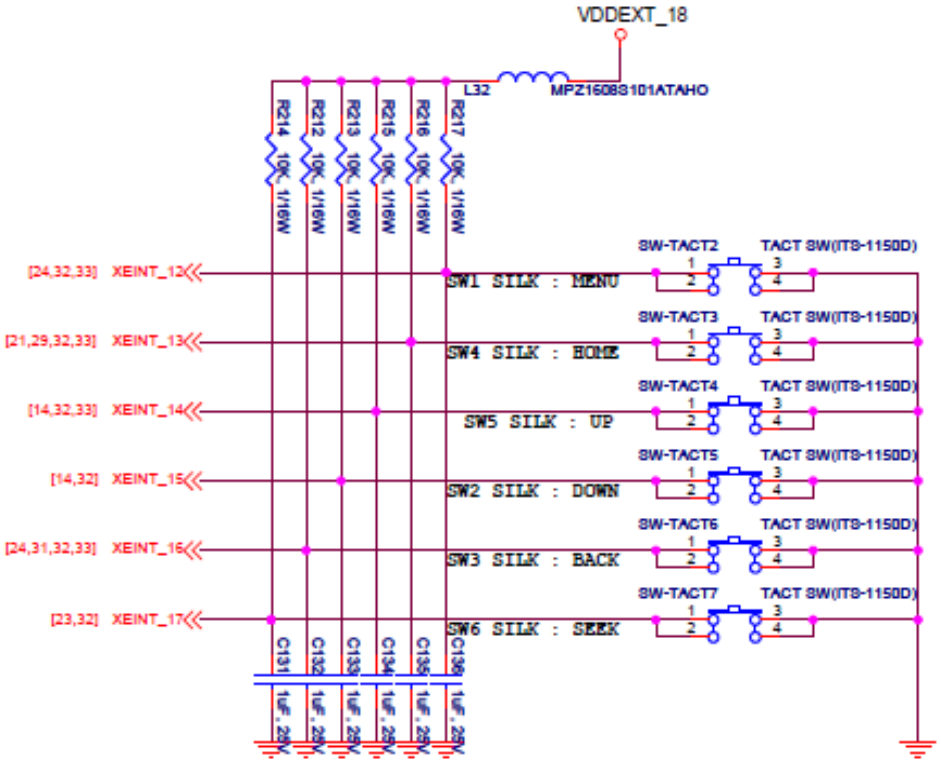


Figure 15 User Push Buttons

Table 5. ARNDALE eMMC Signals

Signal Name	Description	Type	CPU PIN Name
XEINT_12	GPX1[4]/WAKEUP_INT1[4]/ALV_DBG[8]	I/O	XEINT_12
XEINT_13	GPX1[5]/WAKEUP_INT1[5]/ALV_DBG[9]	I/O	XEINT_13
XEINT_14	GPX1[6]/WAKEUP_INT1[6]/ALV_DBG[10]	I/O	XEINT_14
XEINT_15	GPX1[7]/WAKEUP_INT1[7]/ALV_DBG[11]	I/O	XEINT_15
XEINT_16	GPX2[0]/WAKEUP_INT1[0]/ALV_DBG[12]	I/O	XEINT_16
XEINT_17	GPX1[1]/WAKEUP_INT1[1]/ALV_DBG[13]	I/O	XEINT_17

7. Expansion Connectors Placement

7.1 CONNECTIVITY Connectors (CON12 & CON13)

The ARNDALE BaseBoard provides locations for two 30-pin B2B expansion connectors, CON12 and CON13 to support CONNECTIVITY platform expansion.

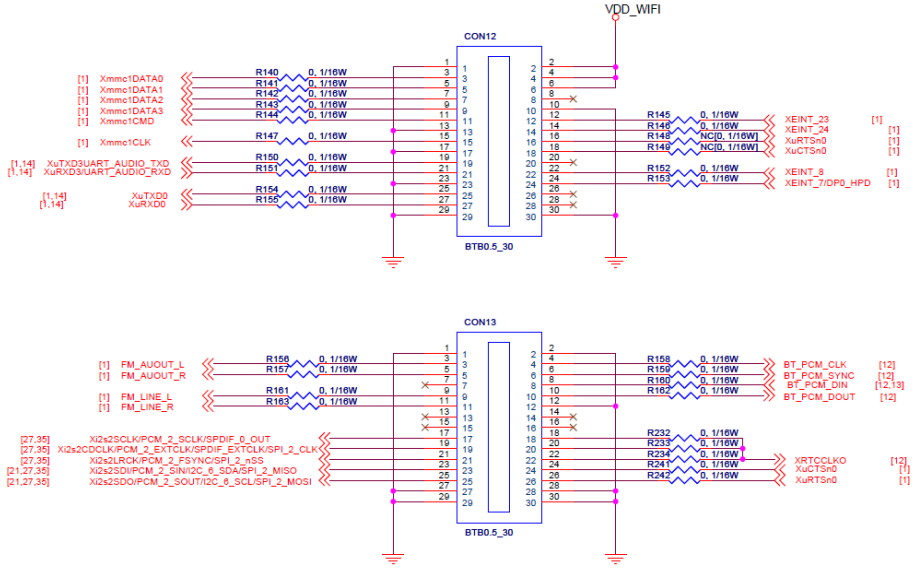


Figure 16 Connectivity Connectors Section

Table 6. ARNDALE Connectivity Connector Signals (CON12)

Signal Name	Description	P/N		Signal Name	Description	P/N
GND	Digital Ground	1		VDD_WIFI	5V DC POWER	2
Xmmc1DATA0	SD_1_DATA0/GPC2[3]	3		VDD_WIFI	5V DC POWER	4
Xmmc1DATA1	SD_1_DATA1/GPC2[4]	5		VDD_WIFI	5V DC POWER	6
Xmmc1DATA2	SD_1_DATA2/GPC2[5]	7		NC	-	8
Xmmc1DATA3	SD_1_DATA3/GPC2[6]	9		GND	Digital Ground	10
Xmmc1CMD	SD_1_CMD/GPC2[1]	11		XEINT_23	GPX2[7]/INT2[7]	12
GND	Digital Ground	13		XEINT_24	GPX3[0]/INT3[0]	14
Xmmc1CLK	SD_1_CLK/GPC2[0]	15		XuRTSn0	UART0 request	16
GND	Digital Ground	17		XuCTSn0	UART0 clear	18
XuTXD3	UART3 Transmit Data	19		NC	-	20
XuRXD3	UART3 Receive Data	21		XEINT_8	GPX1[0]/INT1[0]	22
GND	Digital Ground	23		XEINT_7	GPX0[7]/INT0[7]	24
XuTXD0	UART0 Transmit Data	25		NC	-	26
XuRXD0	UART0 Receive Data	27		NC	-	28
GND	Digital Ground	29		GND	Digital Ground	30

Table 7. ARNDALE Connectivity Connector Signals (CON13)

Signal Name	Description	P/N		Signal Name	Description	P/N
GND	Digital Ground	1		GND	Digital Ground	2
FM_AUOUT_L	FM Radio/LINE IN L	3		BT_PCM_CLK	Serial Data Clock	4
FM_AUOUT_R	FM Radio/LINE IN R	5		BT_PCM_SYNC	Sync Signal	6
NC	-	7		BT_PCM_DIN	Serial Data Input	8
FM_LINE_L	FM Radio/LINE OUT L	9		BT_PCM_DOUT	Serial Data Output	10
FM_LINE_R	FM Radio/LINE OUT R	11		GND	Digital Ground	12
NC	-	13		NC	-	14
NC	-	15		NC	-	16
Xi2s2SCLK	GPB1[0]	17		XRTCCLKO	RTC_CLKOUT/ETC6[3]	18
Xi2s2CDCLK	GPB1[1]	19		XRTCCLKO	RTC_CLKOUT/ETC6[3]	20
Xi2s2LRCK	GPB1[2]	21		XRTCCLKO	RTC_CLKOUT/ETC6[3]	22
Xi2s2SDI	GPB1[3]	23		XuCTSn0	UART0 clear	24
Xi2s2SDO	GPB1[4]	25		XuRTSn0	UART0 request	26
GND	Digital Ground	27		GND	Digital Ground	28
GND	Digital Ground	29		GND	Digital Ground	30

7.2 AUDIO Connectors (CON14 & CON15)

The ARNDALE BaseBoard provides locations for two 30-pin B2B expansion connectors, CON14 and CON15 to support AUDIO platform expansion.

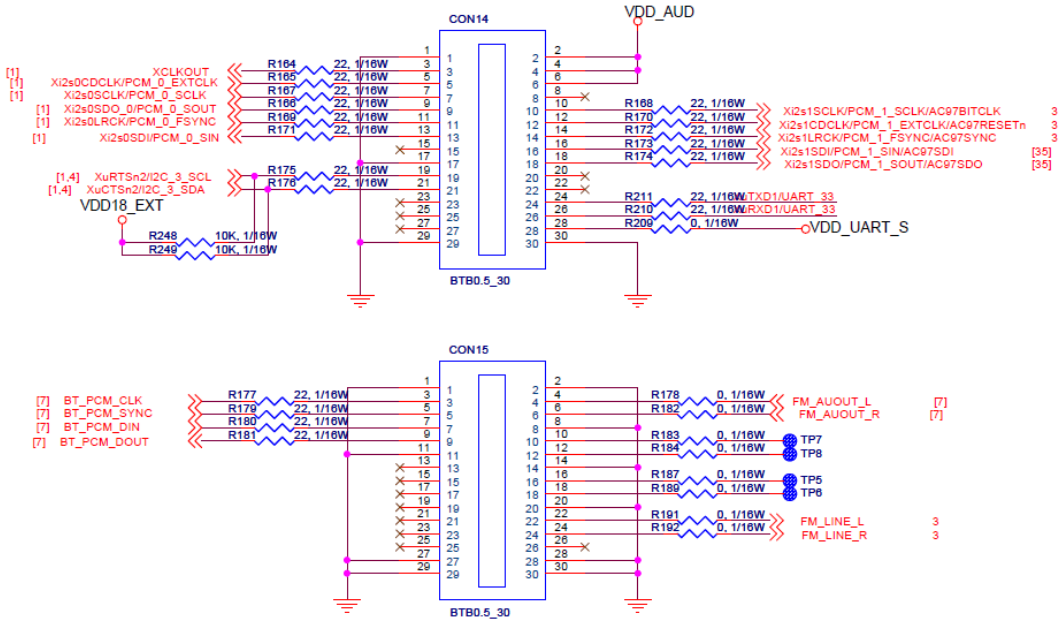


Figure 17 AUDIO Connectors Section

Table 8. ARNDALE AUDIO Connector Signals (CON14)

Signal Name	Description	P/N		Signal Name	Description	P/N
GND	Digital Ground	1		VDD_AUD	5V DC POWER	2
XCLKOUT	External Master Clock	3		VDD_AUD	5V DC POWER	4
Xi2s0CDCLK	I2S_0_CDCLK/GPZ[1]	5		VDD_AUD	5V DC POWER	6
Xi2s0SCLK	I2S_0_SCLK/GPZ[0]	7		NC	-	8
Xi2s0SDO	I2S_0_SDO/GPZ[4]	9		PCM_1_SCLK	PCM1 bit clock	10
Xi2s0LRCK	I2S_0_LRCK/GPZ[2]	11		PCM_1_EXTCLK	PCM1 Codec clock	12
Xi2s0SDI	I2S_0_SDI/GPZ[3]	13		PCM_1_FSYNC	PCM1 channel clock	14
NC	-	15		PCM_1_SIN	PCM1 serial data input	16
GND	Digital Ground	17		PCM_1_SOUT	PCM1 serial data out	18
I2C_3_SCL	I2C3 Clock/GPA0[3]	19		NC	-	20
I2C_3_SDA	I2C3 Data/GPA0[2]	21		NC	-	22
NC	-	23		XuTXD1	AUDIO Ext Serial TXD	24
NC	-	25		XuRXD1	AUDIO Ext Serial TXD	26
NC	-	27		VDD_UART_S	AUDIO Ext Power	28
GND	Digital Ground	29		GND	Digital Ground	30

Table 9. ARNDALE AUDIO Connector Signals (CON15)

Signal Name	Description	P/N		Signal Name	Description	P/N
GND	Digital Ground	1		GND	Digital Ground	2
BT_PCM_CLK	Serial Data Clock	3		FM_AUOUT_L	FM Radio, LINE OUT	4
BT_PCM_SYNC	Sync Signal	5		FM_AUOUT_R	FM Radio, LINE OUT	6
BT_PCM_DIN	Serial Data Input	7		GND	Digital Ground	8
BT_PCM_DOUT	Serial Data Output	9		TP		10
GND	Digital Ground	11		TP		12
NC	-	13		GND	Digital Ground	14
NC	-	15		TP		16
NC	-	17		TP		18
NC	-	19		GND	Digital Ground	20
NC	-	21		FM_LINE_L	FM Radio, LINE IN	22
NC	-	23		FM_LINE_R	FM Radio, LINE IN	24
NC	-	25		NC		26
NC	-	27		GND	Digital Ground	28
GND	Digital Ground	29		GND	Digital Ground	30

7.3 Expansion Header CON16

The expansion header is provided to allow a limited number of functions to be added to the ARNDALE BaseBoard via the addition of a daughterboard.

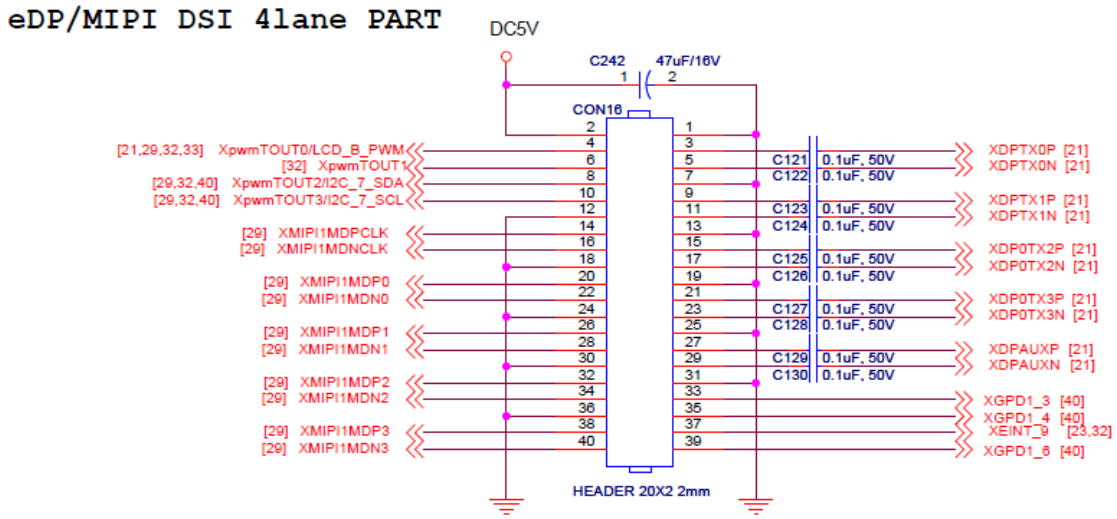


Figure 18 Expansion Header CON16

Table 10. ARNDALE Expansion Header Connector Signals (CON16)

Signal Name	Description	P/N		Signal Name	Description	P/N
DC5V	5V DC POWER	2		GND	Digital Ground	1
XpwmTOUT0	GPB2[0]/TOUT_0	4		XDPTX0P	XdpTX0P	3
XpwmTOUT1	GPB2[1]/TOUT_1	6		XDPTX0N	XdpTX0N	5
XpwmTOUT2	GPB2[2]/I2C7_SDA	8		GND	Digital Ground	7
XpwmTOUT3	GPB2[3]/I2C7_SDA	10		XDPTX1P	XdpTX1P	9
GND	Digital Ground	12		XDPTX1N	XdpTX1N	11
XMIPI1MDPCLK	MIPI-DPHY Master clock DP	14		GND	Digital Ground	13
XMIPI1MDNCLK	MIPI-DPHY Master clock DN	16		XDPTX2P	XdpTX2P	15
GND	Digital Ground	18		XDPTX2N	XdpTX2N	17
XMIPI1MDP0	MIPI-DPHY Master DP0	20		GND	Digital Ground	19
XMIPI1MDN0	MIPI-DPHY Master DN0	22		XDPTX3P	XdpTX3P	21
GND	Digital Ground	24		XDPTX3N	XdpTX3N	23
XMIPI1MDP1	MIPI-DPHY Master DP1	26		GND	Digital Ground	25
XMIPI1MDN1	MIPI-DPHY Master DN1	28		XDPAUXP	XdpAUXP	27
GND	Digital Ground	30		XDPAUXN	XdpAUXN	29
XMIPI1MDP2	MIPI-DPHY Master DP2	32		GND	Digital Ground	31
XMIPI1MDN2	MIPI-DPHY Master DN2	34		XGPD1_3	GPD1[3]	33
GND	Digital Ground	36		XGPD1_4	GPD1[4]	35
XMIPI1MDP3	MIPI-DPHY Master DP3	38		XEINT_9	GPX1[1]/INT1[1]	37
XMIPI1MDN3	MIPI-DPHY Master DN3	40		XGPD1_6	GPD1[6]	39

7.4 Expansion Header CON17

The expansion header is provided to allow a limited number of functions to be added to the ARNDALE BaseBoard via the addition of a daughterboard.

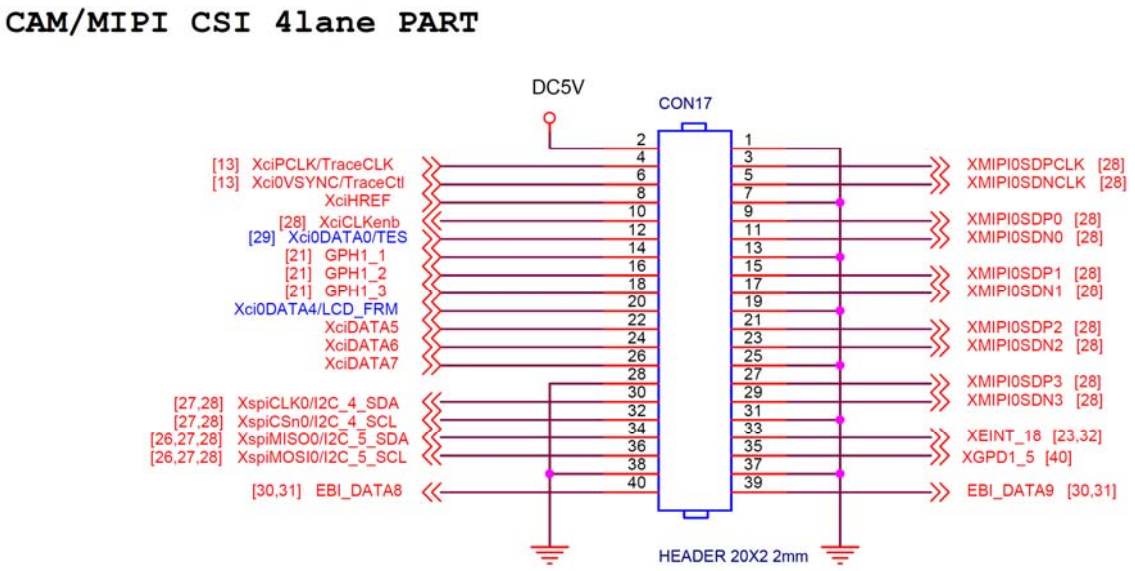


Figure 19 Expansion Header CON17

Table 11. ARNDALE Expansion Header Connector Signals (CON17)

Signal Name	Description	P/N		Signal Name	Description	P/N
DC5V	5V DC POWER	2		GND	Digital Ground	1
XciPCLK	GPH0[0]/CAM_A_PCLK	4		XMIPI0SDPCLK	MIPI-DPHY0 slave DP clock	3
Xci0VSYNC	GPH0[1]/CAM_A_VSYNC	6		XMIPI0SDNCLK	MIPI-DPHY0 slave DN clock	5
XciHREF	GPH0[2]/CAM_A_HREF	8		GND	Digital Ground	7
XciXLKenb	GPH0[3]/CAM_A_CLKOUT	10		XMIPI0SDP0	MIPI-DPHY0 slave DP data0	9
Xci0DATA0	GPH1[0]/CAM_A_DATA0	12		XMIPI0SDN0	MIPI-DPHY0 slave DN data0	11
GPH1_1	GPH1[1]/CAM_A_DATA1	14		GND	Digital Ground	13
GPH1_2	GPH1[2]/CAM_A_DATA2	16		XMIPI0SDP1	MIPI-DPHY0 slave DP data1	15
GPH1_3	GPH1[3]/CAM_A_DATA3	18		XMIPI0SDN1	MIPI-DPHY0 slave DN data1	17
Xci0DATA4	GPH1[4]/CAM_A_DATA4	20		GND	Digital Ground	19
XciDATA5	GPH1[5]/CAM_A_DATA5	22		XMIPI0SDP2	MIPI-DPHY0 slave DP data2	21
XciDATA6	GPH1[6]/CAM_A_DATA6	24		XMIPI0SDN2	MIPI-DPHY0 slave DN data2	23
XciDATA7	GPH1[7]/CAM_A_DATA7	26		GND	Digital Ground	25
GND	Digital Ground	28		XMIPI0SDP3	MIPI-DPHY0 slave DP data3	27
XspiCLK0	SPI0_CLK/I2C_4_data	30		XMIPI0SDN3	MIPI-DPHY0 slave DN data3	29
XspiCSn0	SPI0_Nss/I2C_4_clock	32		GND	Digital Ground	31
XspiMISO0	SPI0_MISO/I2C_5_data	34		XEINT_18	GPX2[2]/INT2[2]	33
XspiMOSI0	SPI0_MOSI/I2C_5_clock	36		XGPD1_5	GPD1[5]	35
GND	Digital Ground	38		GND	Digital Ground	37
EBI_DATA8	GPY6[0]/EBI_DATA[8]	40		EBI_DATA9	GPY6[1]/EBI_DATA[9]	39

7.5 Expansion Header CON18

The ARNDALE BaseBoard provides location for 40-pin through-hole expansion connector, CON17, to support platform expansion.
The connector is not mounted on the current ARNDALE BaseBoard.

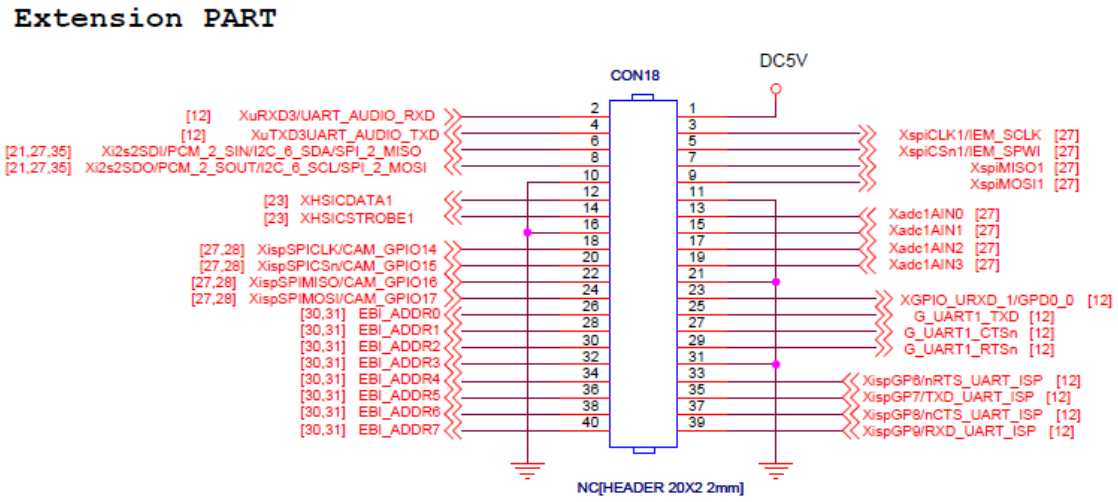


Figure 20 Expansion Header CON18

Table 12. ARNDALE Expansion Header Connector Signals (CON18)

Signal Name	Description	P/N		Signal Name	Description	P/N
XuRXD3	UART_3_RXD/GPA1[4]	2		DC5V	5V DC POWER	1
XuTXD3	UART_3_TXD/GPA1[5]	4		XspiCLK1	GPA2[4]/SPI_1_CLK	3
I2C_6_SDA	I2C_6_data/GPB1[2]	6		XspiCSn1	GPA2[5]/SPI_1_nSS	5
I2C_6_SCL	I2C_6_clock/GPB1[1]	8		XspiMISO1	GPA2[6]/SPI_1_MISO	7
GND	Digital Ground	10		XspiMOSI1	GPA2[7]/SPI_1_MOSI	9
XHSICDATA1	HSIC_1 USB bi-directional	12		GND	Digital Ground	11
XHSICSTROBE1	HSIC_1 USB STROBE	14		Xadc1AIN0	Xadc1AION[0]	13
GND	Digital Ground	16		Xadc1AIN1	Xadc1AION[1]	15
XispSPICLK	CAM_SPI_CLK/GPF1[14]	18		Xadc1AIN2	Xadc1AION[2]	17
XispSPICSn	CAM_SPI_nSS/GPF1[15]	20		Xadc1AIN3	Xadc1AION[3]	19
XispSPICMISO	CAM_SPI_MISO/GPF1[16]	22		GND	Digital Ground	21
XispSPIMOSI	CAM_SPI_MOSI/GPF1[17]	24		XGPIO_URXD_1	RXD for UART1	23
EBI_ADDR0	GPY3[0]/EBI_ADDR[0]	26		G_UART1_TXD	TXD for UART1	25
EBI_ADDR1	GPY3[1]/EBI_ADDR[1]	28		G_UART1_CTSn	CTS for UART1	27
EBI_ADDR2	GPY3[2]/EBI_ADDR[2]	30		G_UART1_RTSn	RTS for UART1	29
EBI_ADDR3	GPY3[3]/EBI_ADDR[3]	32		GND	Digital Ground	31
EBI_ADDR4	GPY3[4]/EBI_ADDR[4]	34		XispGP6	GPE0[6]	33
EBI_ADDR5	GPY3[5]/EBI_ADDR[5]	36		XispGP7	GPE0[7]	35
EBI_ADDR6	GPY3[6]/EBI_ADDR[6]	38		XispGP8	GPE0[8]	37
EBI_ADDR7	GPY3[7]/EBI_ADDR[7]	40		XispGP9	GPE0[9]	39

8. MECHANICAL DESIGN