Application Information for Sharp's LS013B7DH01 Memory LCD
Sharp Microelectronics of the Americas

INTRODUCTION

This Application Note provides additional design assistance for Sharp's LS013B7DH01 Memory LCD. This module is a transflective, monolithic active-matrix liquid crystal module utilizing Sharp's CG-silicon thin-film transistor process. It offers high performance and power efficiency for compact display applications, with a zebra-type connector for simple integration.

Subjects covered will be:

- Mechanical Specifications, including dimension drawings and connector specifications
- Absolute Maximum Ratings
- Optical Specifications, including view angles, reflectivity, contrast, and risetime
- Electrical Characteristics, including interfacing and signal timing information
- Design Notes
- Manufacturing Information, including handling and storage
- Reliability Information

This Note is based on Sharp's document number LCP-2110042A and is designed to provide supplementary information for the Specifications for these parts.

Always refer to the latest Specifications when designing with these devices.

FEATURES

- Transflective monochrome panel; accepts a back-light for extreme low-light ambients
- 120° concentric viewing cone with 30 ms response
- 20:1 contrast with 14.5% reflectivity and 0.45% transmissivity
- 1.26-inch screen with 144 × 168 resolution in a 24192-pixel stripe array)
- Serial interface for display control
- Screen data is arbitrarily renewable by line
- Built-in, 1-bit internal memory for data storage
- Thin and light, compact module incorporating mono-lithic technology
- Super low power consumption TFT panel
- Zebra connector
- RoHS compliant

MECHANICAL SPECIFICATIONS

PARAMETER	SPECIFICATION	UNIT
Screen Size	1.26 (3.2)	Inch (mm)
Viewing Area	20.88 (H) × 24.36 (V)	mm
Dot Configuration (Square panel)	144 (H) × 168 (V)	Dot
Dot Pitch	0.145 (H) × 0.145 (V)	mm
Pixel Array	Stripe Array	
External Dimensions	24.88 (W) × 33.0 (H) × 1.64 (D)	mm
Mass	3.0 (TYP)	g
Surface Hardness	3H	Pencil hardness

External Dimensions

NOTES:
1. Units: mm
2. ( ): Reference dimensions

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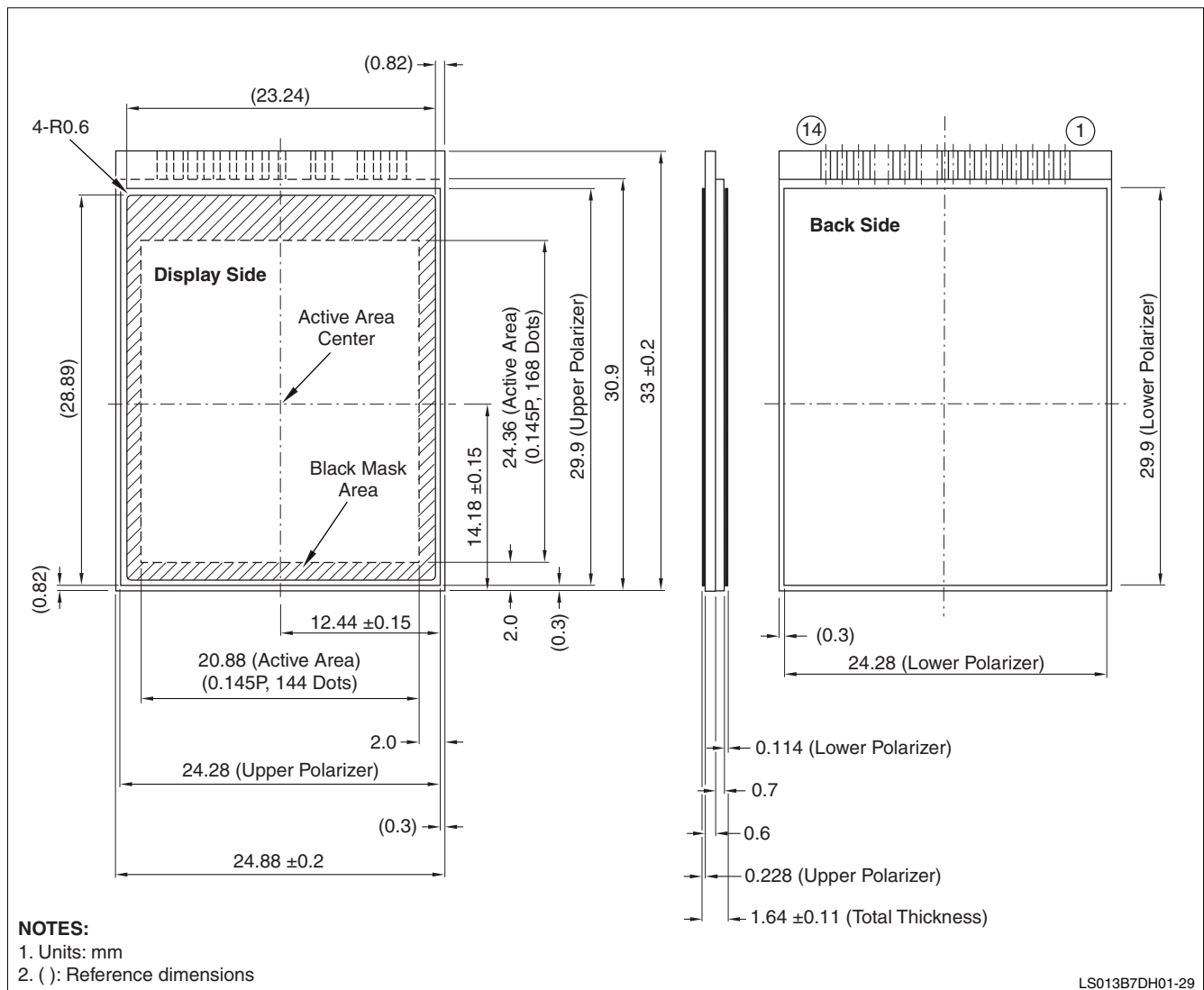
Connector Specifications

Table 1. Input Terminals and Functions

TERMINAL	SYMBOL	I/O	FUNCTION	NOTES
1	TEST1	///	Test terminal	1
2	TEST2	///	Test terminal	1
3	SCLK	INPUT	Serial clock signal	
4	SI	INPUT	Serial Data input signal	
5	SCS	INPUT	Chip select signal	
6	EXTCOMIN	INPUT	External COM inversion signal input (H: enable)	2
7	DISP	INPUT	Display ON/OFF signal	3
8	VDDA	POWER	Power supply (Analog)	
9	VDD	POWER	Power supply (Digital)	
10	EXTMODE	INPUT	COM inversion select terminal	4
11	VSS	GND	GND (Digital)	
12	VSSA	GND	GND (Analog)	
13	TEST3	///	Test terminal	1
14	TEST4	///	Test terminal	1

NOTES:
1. TEST terminal: No connect. Do not tie HIGH or LOW.
2. EXTCOMIN is HIGH enabled. When LOW, the serial input flag is enabled. See Figure 15 and Figure 17 for recommended circuits.
3. DISP enables/disables the display. All pixels will revert to Normal mode (reflective) when LOW. When DISP = H, data in the pixel memories displays normally.
4. EXTMODE pin must be connected to VDD for HIGH, and to VSS for LOW. See Figure 15 and Figure 17 in Interfacing and Signals.
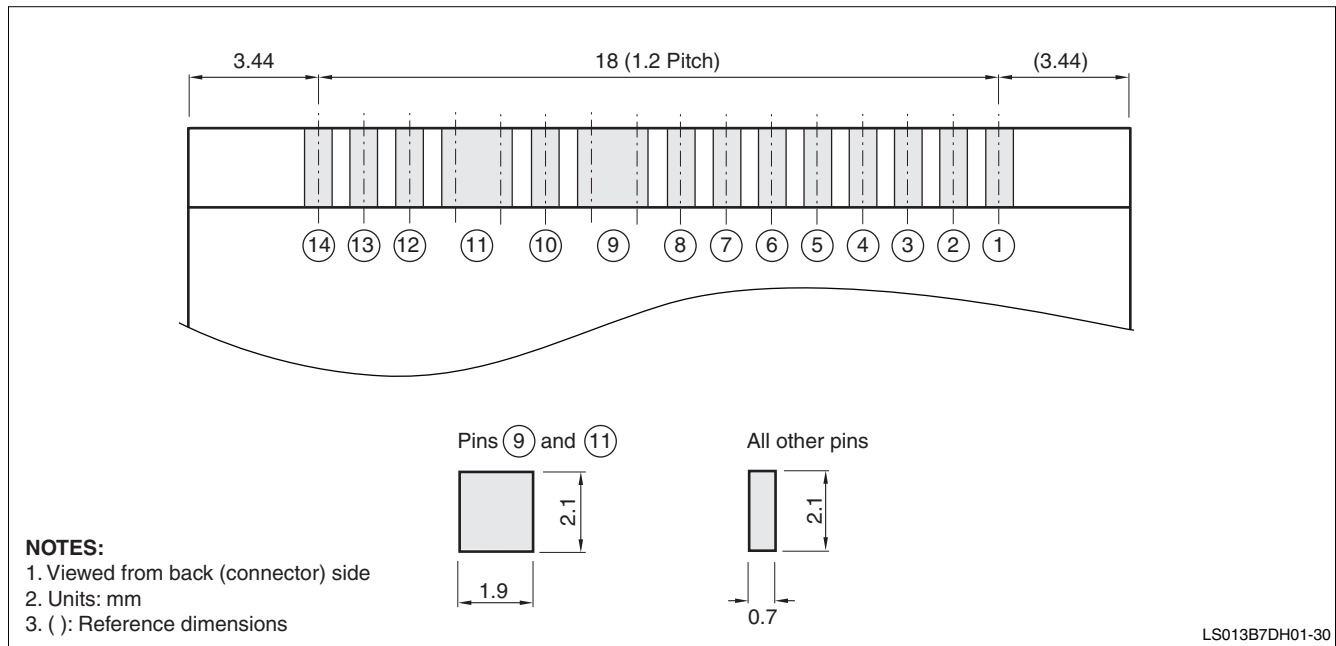

NOTES:
1. Viewed from back (connector) side
2. Units: mm
3. ( ): Reference dimensions

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Figure 1. Panel Connector Mechanical Specifications

Zebra Connector Specifications

Contact resistance is <20 Ω

RECOMMENDED CONNECTORS
- Shin-Etsu Polymer: SX type
  - Recommended Size: L: 27.7 ±0.2 mm, W: 1.5 ±.01 mm, H: 2.0 ±0.1 mm, P: 0.3 mm
  - Recommended compression ratio: 15 ±8%

See Figure 2 for placement position specifications.

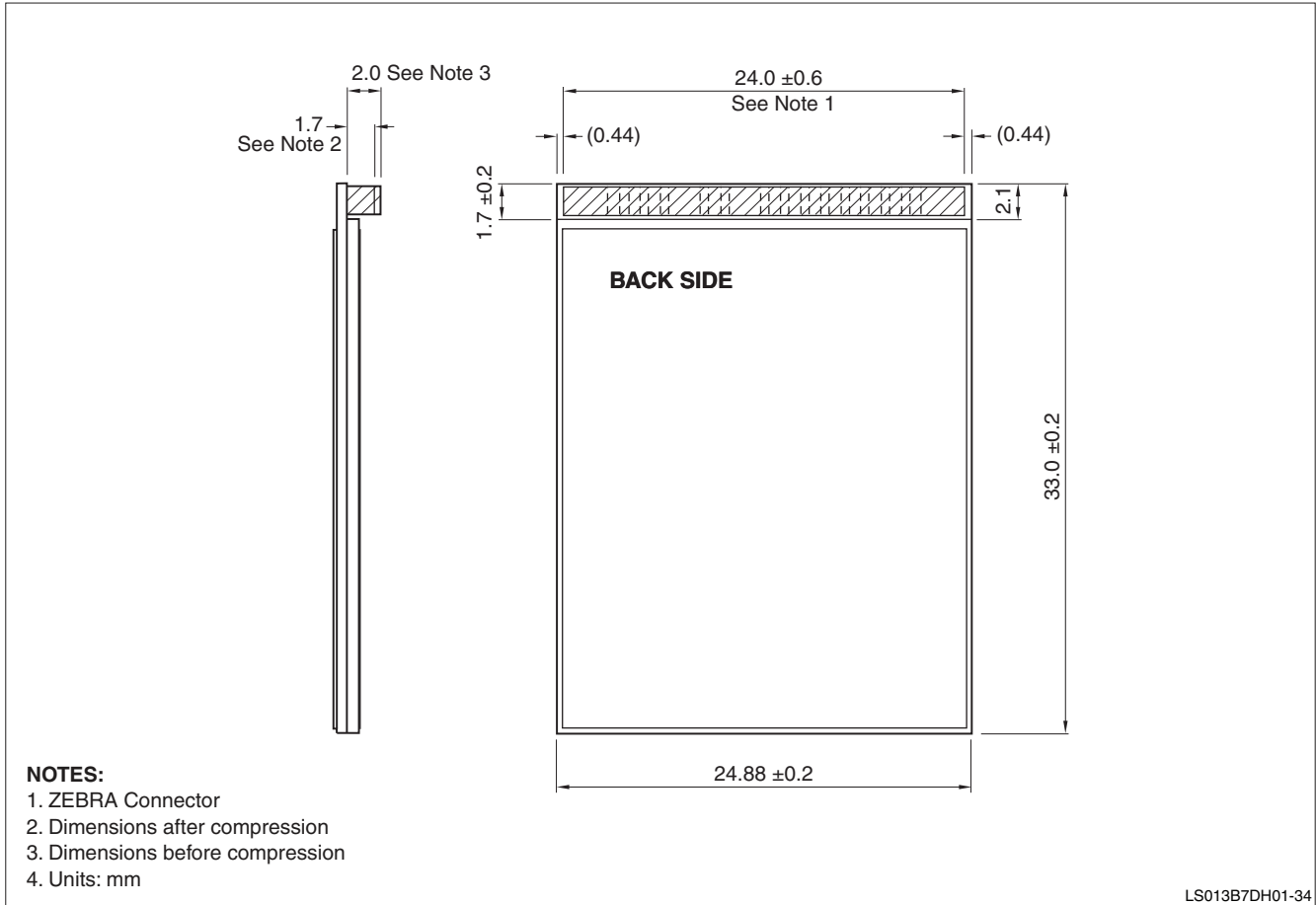**NOTES:**
1. ZEBRA Connector
2. Dimensions after compression
3. Dimensions before compression
4. Units: mm

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Figure 2. Zebra Connector Specifications

Absolute Maximum Ratings

PARAMETER		SYMBOL	MIN.	MAX.	UNIT	NOTES
Power Supply Voltage	Analog	VDDA	-0.3	+5.8	V	
	Logic	VDD	-0.3	+5.8	V	1
Input Signal Voltage (HIGH)				VDD	V	2
Input Signal Voltage (LOW)			-0.3		V	
Storage Temperature		Tstg	-30	+80	°C	3
Operation Temperature (at panel surface)		Topr1	-20	+70	°C	4

NOTES:
1. Applies to EXTMODE.
2. Applies to SCLK, SI, SCS, DISP, EXTCOMIN.
3. Do not exceed this temperature in any part of the module.
4. Maximum wet bulb temperature is 57°C or lower. No condensation is allowed. Condensation will
   cause electrical leakage and may cause the module to fail to meet its Specifications.
5. Operating Temperature is the guaranteed temperature limits for operation.
6. For contrast, response time, and other display quality determination, use Ta = +25°C.

OPTICAL SPECIFICATIONS

Ta = 25°C

PARAMETER		SYMBOL	MIN.	TYP.	UNIT	NOTES
Viewing Angle CR ≥ 5	H	$\theta 21, \theta 22$	40	60	Degrees	1
	V	$\theta 11$	40	60	Degrees	1
		$\theta 12$	40	60	Degrees	1
Contrast Ratio		CR	12	20		2
Reflectivity Ratio		R	11	14.5	%	2
Transmissivity Ratio		T		0.45	%	
Response Time	Rise	tR		10	ms	3
	Fall	tF		20	ms	3
Chromaticity	White	x		0.307		2
		y		0.330		2

NOTES:
1. Viewing Angle is described as clock positions:
   $\theta 12$ = 12 o'clock, $\theta 11$ = 6 o'clock, $\theta 21$ = 3 o'clock, $\theta 22$ = 9 o'clock. See Figure 3.
2. Contrast Ratio, Reflectivity Ratio, and Chromaticity are measured through the use of an integrating sphere. See Figure 4.
3. Response Time is measured by the change interval in an optical receiver when the test panel's signal is transitioned from white to black to white. See Figure 5 for the measurement setup and Figure 6 for the output waveshape.
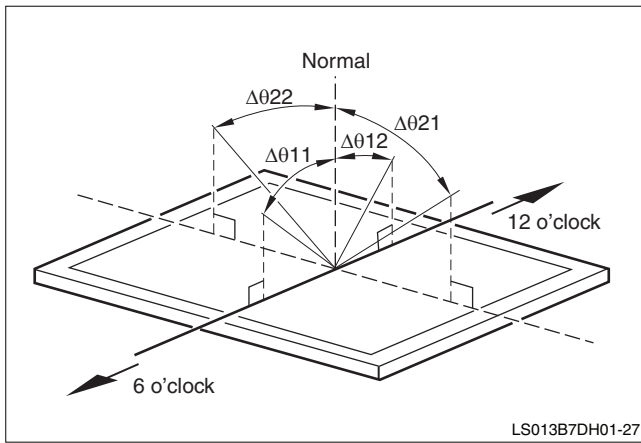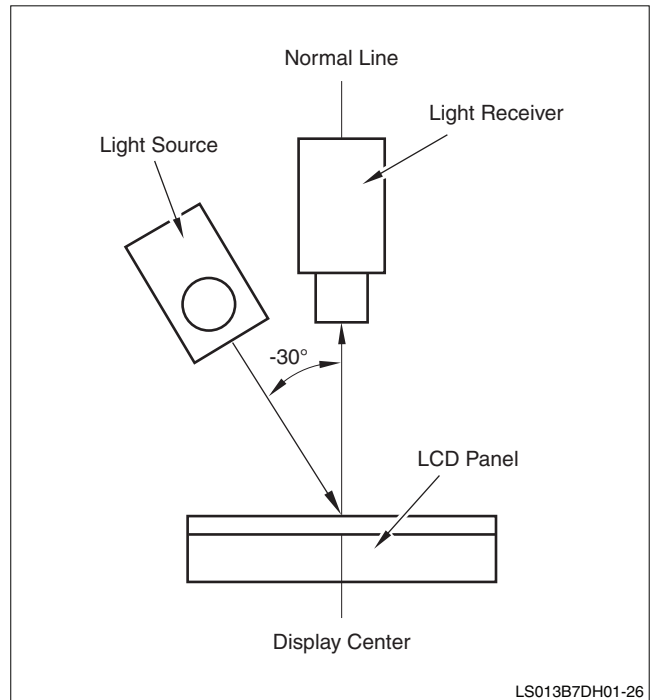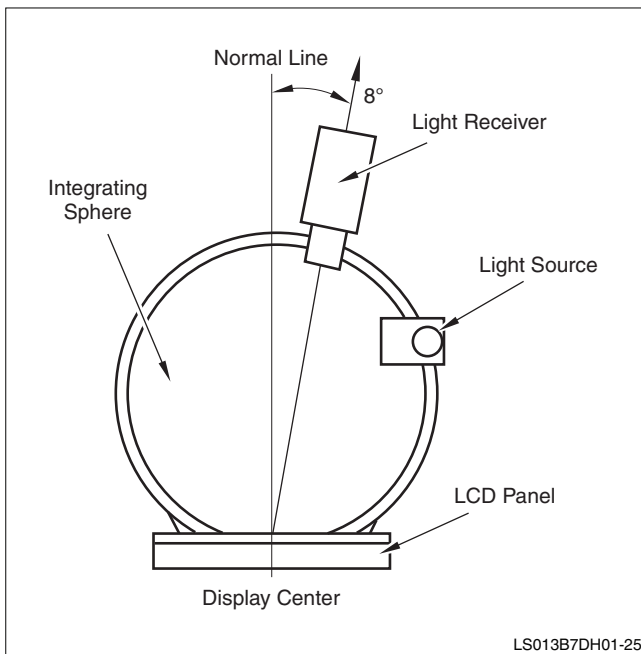
Figure 3. Viewing Angle

Figure 4. Setup for Contrast, Reflection Ratio,
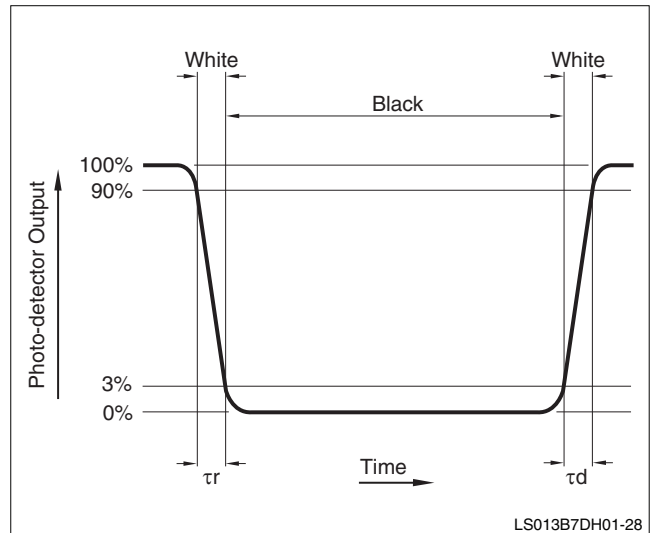and Chromaticity

Figure 5. Setup for Response Time

Figure 6. Response Time

ELECTRICAL SPECIFICATIONS

Here are the Recommended Operating Conditions for this module, with VSS (GND) = 0V and Ta = 25°C.

Power Consumption

This module has the ability to shut down most of its logic circuits when it is in Static mode (not being updated). It has two levels of power consumption: Static and Dynamic Display. Table 3 shows examples of differing levels of power consumption in the different modes.

Table 2. Electrical Specifications

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Power supply	Analog	VDDA	+4.8	+5.0	+5.5	V	
	Logic	VDD	+4.8	+5.0	+5.5	V	1
Input signal voltage	HIGH	VIH	+2.70	+3.0	<VDD	V	2
	LOW	VIL	VSS	VSS	VSS + 0.15	V	

NOTES:
1. 3 V or less is recommended; never exceed VDD.
2. EXTMODE = H
3. VI = 3 V; applies to SCLK, SI, SCS, DISP, EXTCOMIN
4. VI = 0 V; applies to SCLK, SI, SCS, DISP, EXTCOMIN

Table 3. Power Consumption Levels

LC Inversion Frequency	MIN.	TYP.	MAX.	UNIT	Condition
1 Hz		15	60	µW	Static Mode; no display update
		- 50	100	µW	Dynamic Mode; display update rate: 1 frame/sec (SCLK = 1 MHz)
60 Hz		50	100	µW	Static Mode; no display update
		90	150	µW	Dynamic Mode; display update rate: 1 frame/sec (SCLK = 2 MHz)

NOTE:
1. Ta = 25°C, SCS, SCLK, Si, DISP, and EXTCOMIN = 3 V, VDD = 5 V, VDDA = 5 V
2. Test pattern: full black (non-reflective) to full white (reflective).
3. These numbers represent average power, not peak power usage when driving VCOM.
   Always allow for a margin in power supply design.
4. The LC Inversion Frequency given here is the maximum and minimum values specified for this device.
   It is derived from fCOM (see Table 4).

Decoupling Capacitors

Use of a decoupling capacitor on VDD and VDDA is recommended, even when the two supplies are tied together. See Figure 7.

Values for these capacitors:

C1: DISP to VSS: rank B, 0.1 µF Ceramic

C2: VDDA to VSS: rank B, 1 µF Ceramic

C3: VDD to VSS: rank B, 1 µF Ceramic

These are recommended values; actual values should be determined by the final design. Always place the decoupling capacitors as close as possible to the part as the impedance of the VDD and VSS lines is low when the module is operating.
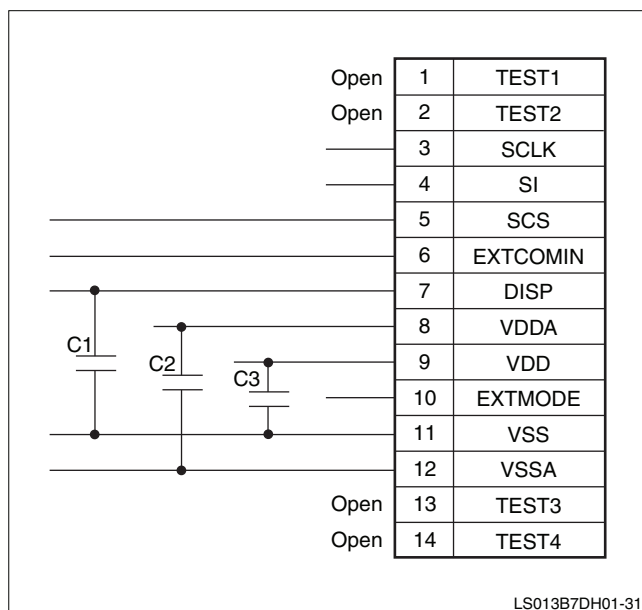

Open	1	TEST1
Open	2	TEST2
	3	SCLK
	4	SI
	5	SCS
	6	EXTCOMIN
	7	DISP
	8	VDDA
	9	VDD
	10	EXTMODE
	11	VSS
	12	VSSA
Open	13	TEST3
Open	14	TEST4

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Figure 7. Decoupling Capacitors

Power Supply Sequencing

This device requires proper supply sequencing on both startup and shutdown to prevent latching of the logic circuits. Refer to Figure 8.

POWER-UP

VDD and VDDA must rise together or VDD must rise faster than VDDA.

1. 5V rises to nominal
2. Initialize pixel memory: send D2 CLEAR ALL flag or set the display to all-white (requires >1 V)
3. Latch cancellation for TCOM; requires a period to cancel the COM latch circuit by DISP = HIGH (requires > 30 µs)
4. TCOM polarity initialization by EXTCOMIN (requires > 30 µs)

POWER-DOWN

VDD and VDDA must fall together or VDDA must fall faster than VDD.

1. Initialize pixel memory (requires >1 V)
2. Initialize VA, VB, and VCOM (requires >1 V)
3. 5V falls
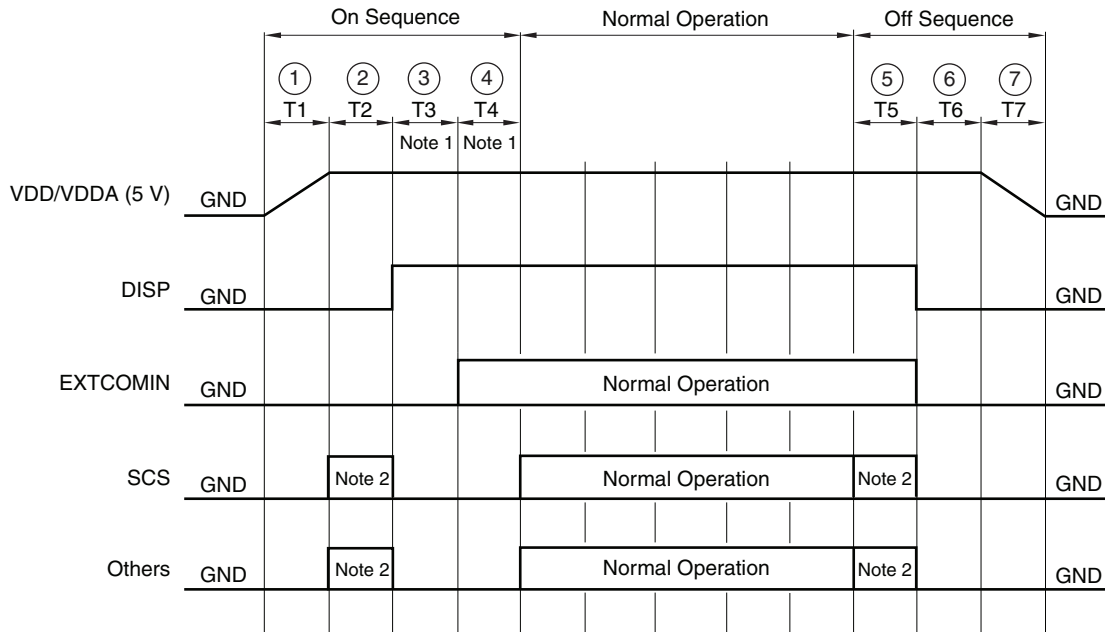
Figure 8. Power Supply Sequencing

SIGNAL DESCRIPTIONS

Input signal characteristics are given in Table 4 and Table 5.

All measurements are at VDDA = +5.0 V, VDD = +5.0 V, GND = 0 V, Ta = 25°C.

Table 4. Signal Frequencies

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
fSCS	Frame frequency	1		60	Hz
fSCLK	Clock frequency		1	2	MHz
tV	Vertical Interval	16.66		1000	ms
fCOM	COM Frequency	0.5		30	Hz

Table 5. Signal Transition Times

PARAMETER	DESCRIPTION	MIN.	TYP.	MAX.	UNIT	NOTES
trSCS	SCS Risetime			50	ns	
tfSCS	SCS Falltime			50	ns	
twSCSH	SCS HIGH Duration	92			µs	2
		12			µs	3
twSCSL	SCS LOW Duration	1			µs	
tsSCS	SCS setup time	3			µs	
thSCS	SCS hold time	1			µs	
fSI	SI frequency		0.5	1	MHz	
trSI	SI Risetime			50	ns	
tfSI	SI Falltime			50	ns	
tsSI	SI setup time	(120)			ns	
thSI	SI hold time	(125)			ns	
trSCLK	SCLK Risetime			50	ns	
tfSCLK	SCLK Falltime			50	ns	
twSCLKH	SCLK HIGH duration	200	450		ns	
twSCLKL	SCLK LOW duration	200	450		ns	
fEXTCOMIN	EXTCOMIN frequency		1	60	Hz	4
trEXTCOMIN	EXTCOMIN Risetime			50	ns	
tfEXTCOMIN	EXTCOMIN Falltime			50	ns	
thlEXTCOMIN	EXTCOMIN HIGH duration	1			µs	
trDISP	DISP Risetime			50	ns	
tfDISP	DISP Falltime			50	ns	

NOTES:
1. Parenthesis indicate preliminary values.
2. Dynamic Mode (continuously updating display)
3. Static Mode (no display updating)
4. fEXTCOMIN must always be less than fSCS (Table 4)

Timing Diagram

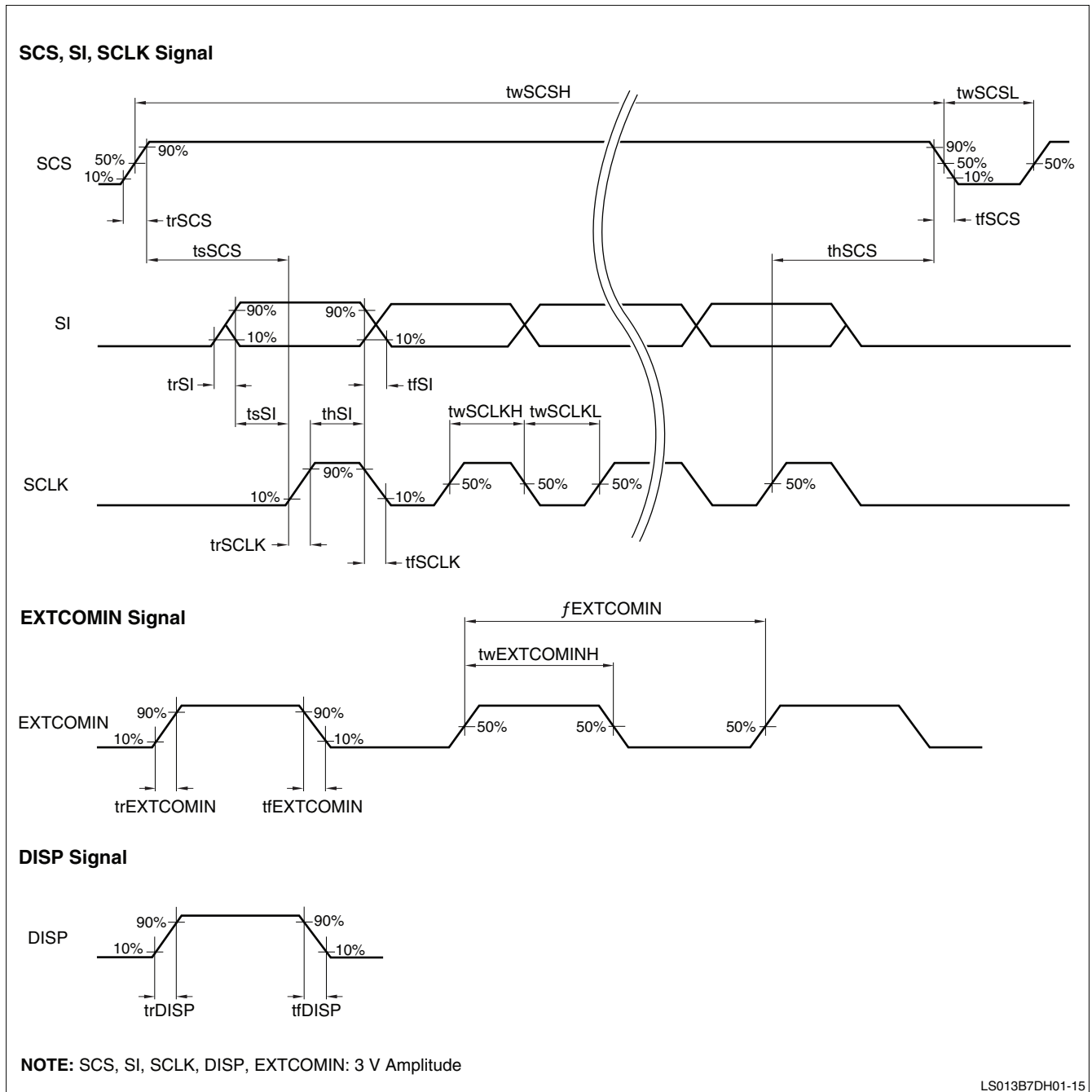This diagram depicts input signal timing for Table 5.

Figure 9. SCS, SI, SCLK, EXTCOMIN, and DISP Signals

PROGRAMMING

For software commands, see the Application Note, Programming Sharp's Memory LCDs, by Ken Green.

In all the following diagrams and descriptions, these conventions are used:

- M0: MODE
  When M0 is 'H', the module enters Dynamic Mode, where pixel data will be updated.
  When M0 is 'L' the module remains in Static Mode, where pixel data is retained.

- M1: VCOM
  This polarity-inversion flag enables a periodic polarity inversion on the panel to keep a latent charge from building up within the Liquid Crystal cells. When M1 is 'H' then VCOM = 'H' is output. If M1 is 'L' then VCOM = 'L' is output.
  When EXTMODE = 'H', M1 value = XX (don't care). See COM Inversion and Signal Selection.

- M2: CLEAR ALL
  When M2 is 'L' then all flags are cleared. When a full display clearing is required, refer to CLEAR ALL.

- D1 - D144: Display data
  Setting D(n) = 'L' sets that pixel to black. Conversely, Setting D(n) = 'H' sets that pixel to white.

- DUMMY DATA: Dummy data
  Dummy data is typically 'XX (don't care); however Sharp recommends setting bits to 'L'.

Data Addressing and Positions

This module uses mixed addressing for columns and lines. Columns (X direction) are addressed using a 7-bit binary scheme, and lines (Y direction) are addressed directly as 96 bits. One line is the minimum addressable unit in the display; even if only one pixel in the line is to be updated, the entire line must be sent.
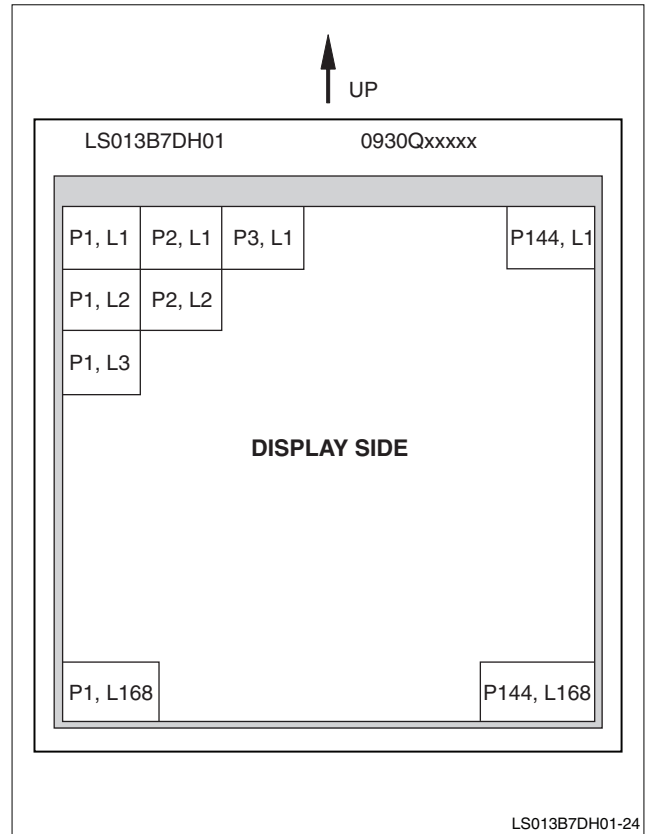

Figure 10. Display Data Position

Table 6. Column (X direction) Addressing

Line Address	Column Address							
	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7
L1	H	L	L	L	L	L	L	L
L2	L	H	L	L	L	L	L	L
L3	H	H	L	L	L	L	L	L
:	:	:	:	:	:	:	:	
L165	H	L	H	L	L	H	L	H
L166	L	H	H	L	L	H	L	H
L167	H	H	H	L	L	H	L	H
L168	L	L	L	H	L	H	L	H

Dynamic Mode

For software commands, see Sharp's Application Note, Programming Sharp's Memory LCDs, by Ken Green.

MULTIPLE LINE WRITE

Dynamic Mode assumes the updating of at least one line in the display. During the Data Write period, data is stored in the panel's binary latch. During Data Transfer, the data from the latch is written to the panel memory, line-by-line. During the write to panel memory, data for the next line is latched.

Dynamic Mode is entered by sending M0 = H and M2 = L.

Figure 11 shows an example of writing multiple lines.
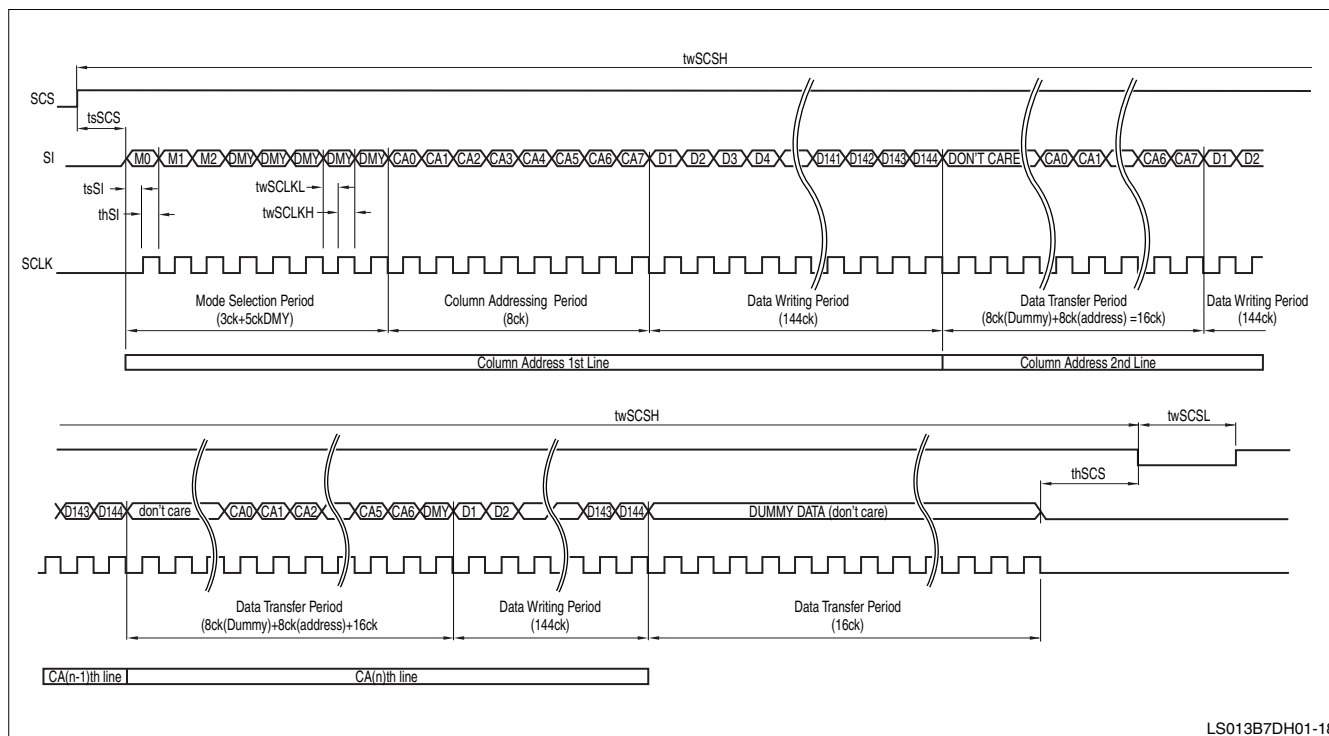
Figure 11. Dynamic Mode Timing Diagram, Writing Multiple Lines

SINGLE LINE WRITE

Writing a single line of data is much the same as writing multiple lines. During the Data Write period, data is stored in the panel's binary latch. During Data Transfer, the data from the latch is written to the panel memory, line-by-line. During the write to panel memory, data for the next line is latched.

Dynamic Mode is entered the same way, by sending M0 = H and M2 = L.

Figure 12 shows an example of writing a single line.

Static Mode

Static Mode is the module's lowest-power mode, with data latches and other circuitry powered down. Static Mode can be held indefinitely; as long as the panel has power and VCOM is toggled periodically. Sharp recommends keeping maximum time between VCOM toggles to no more than one second.

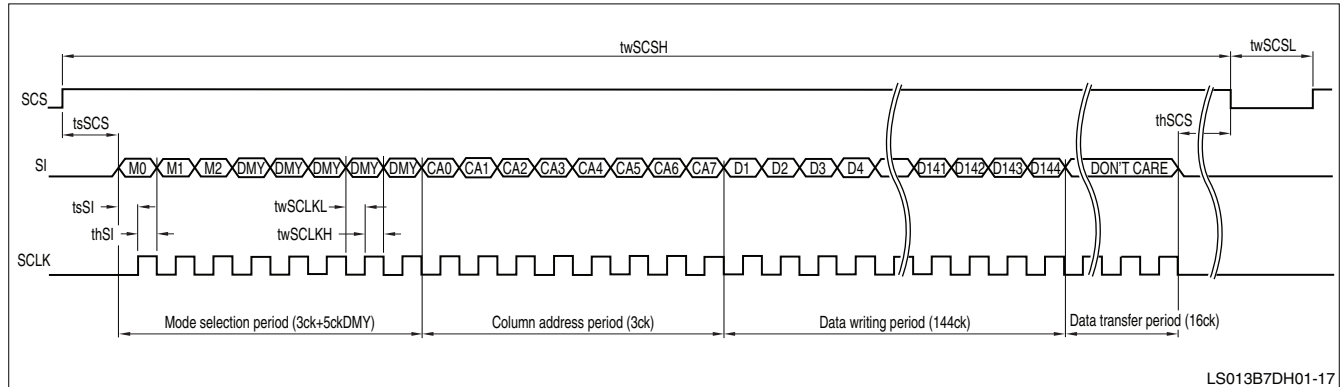Static Mode is entered by sending M0 = L and M2 = L.

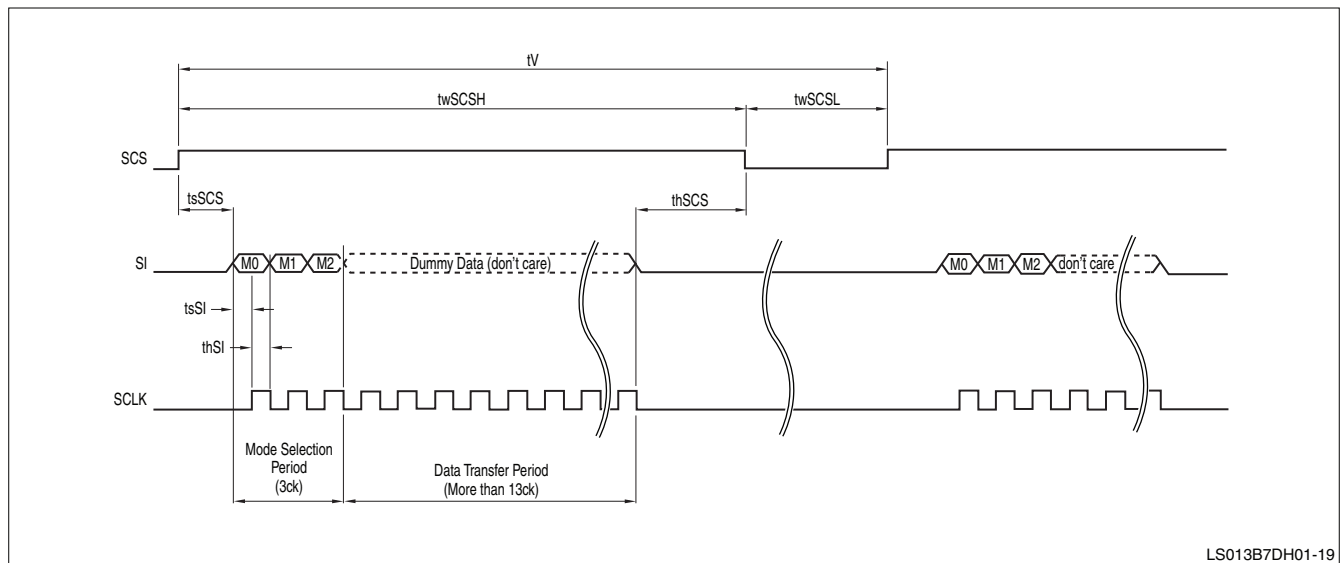Figure 12. Dynamic Mode Timing Diagram, Writing a Single Line

Figure 13. Static Mode Timing Diagram

CLEAR ALL

CLEAR ALL will clear all data from pixel memories and the display will revert to its normal white color.

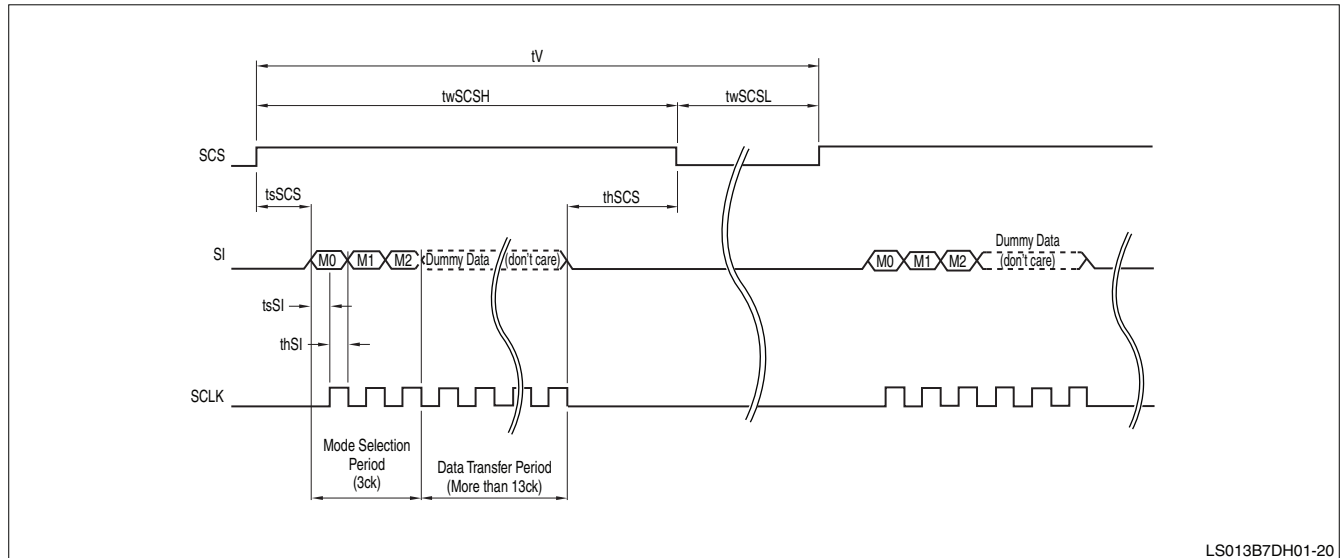CLEAR ALL is invoked by sending M0 = L and M2 = H.

Figure 14. CLEAR ALL Timing Diagram

VCOM Inversion

This Module utilizes a signal called EXTCOMIN which most developers know by the name of VCOM.

Periodic VCOM inversion impresses a polarity inversion across the panel to keep a latent charge from building up within the Liquid Crystal cell. It can be implemented either through software or through hardware. In either implementation, the positive and negative inversion intervals should be kept as equal as possible, and intervals should not exceed one second.

Provisions in the design must be made for periodic VCOM inversion; it can be accomplished either through software or hardware. Tying EXTMODE to either VDD or VSS selects the input mode. See Figure 15 and Figure 17.

For both software and hardware toggles the panel generates an internal version of VCOM, called COM. The internal COM signal is the one which accomplishes the polarity inversion on the panel.

SOFTWARE VCOM TOGGLE

The panel electronics generate an internal version of the VCOM serial input signal, called COM. The internal COM signal is the one which accomplishes the polarity inversion on the panel. Figure 16 shows the internal signal interactions during software VCOM toggling.

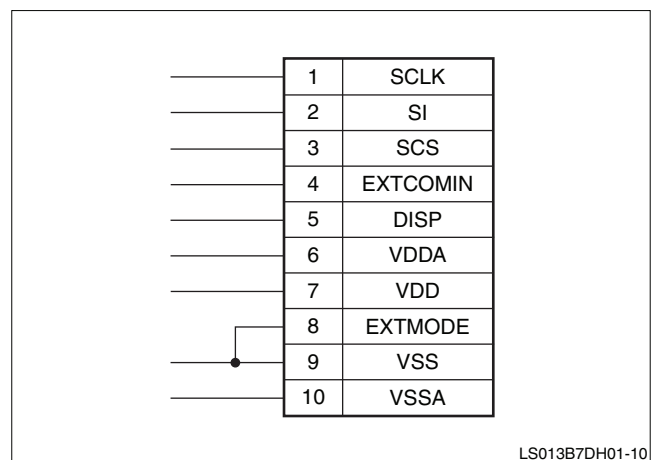To implement VCOM inversion in software, the M1 bit

Figure 15. VCOM Software Input

is periodically toggled. When M1 is 'H' then VCOM = 'H' is output to the panel. If M1 is 'L' then VCOM = 'L' is output to the panel. The COM signal is set after the M1 flag is read. Note that the M1 flag must periodically change state to cause VCOM to toggle.

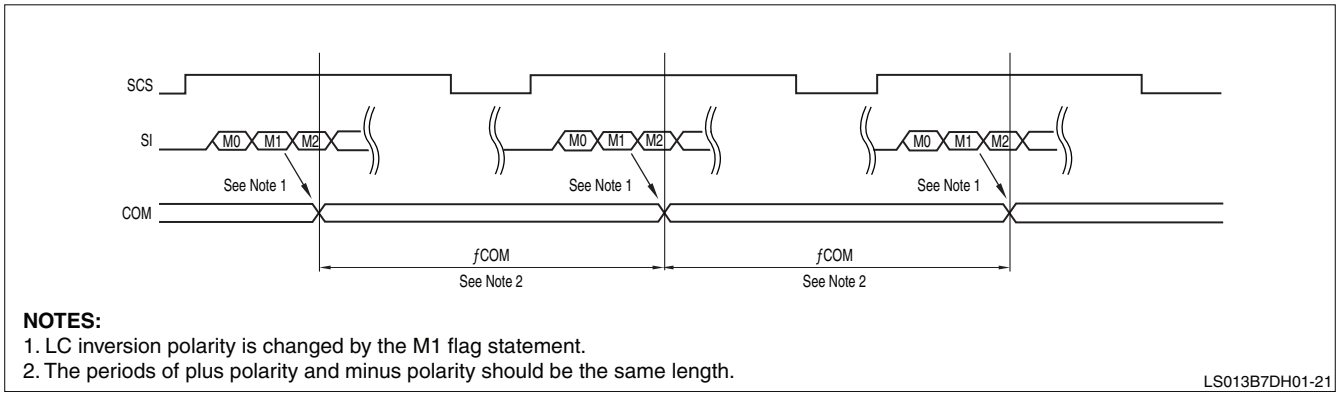Always keep the VCOM duty cycle at 50%, and cycles no more than 1 second apart.

NOTES:
1. LC inversion polarity is changed by the M1 flag statement.
2. The periods of plus polarity and minus polarity should be the same length.

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Figure 16. EXTMODE = L, Software VCOM Toggle

HARDWARE VCOM TOGGLE

When implementing a VCOM toggle through hardware, EXTMODE is set to 'H', and the M1 value becomes XX (don't care). Hardware then toggles EXTCOMIN, and the timing between toggles of this line sets the VCOM inversion interval. Therefore, it's important not to allow the toggling interval of EXTCOMIN to exceed one second. To set the panel for software toggling of M1, tie EXTMODE to VDD as shown in Figure 17.

VCOM inversion has two different conditions when using a hardware toggle, and both depend upon the condition of the SCS signal.

When SCS is HIGH, The LC cell inversion polarity toggle is armed when EXTCOMIN rises. When SCS goes LOW, VCOM will toggle. Do not toggle EXTCOMIN more than once while SCS is HIGH.

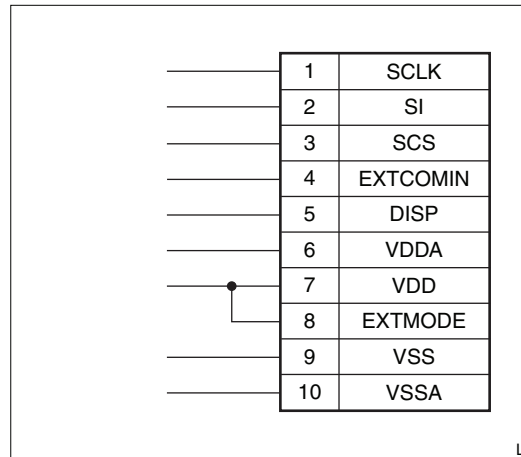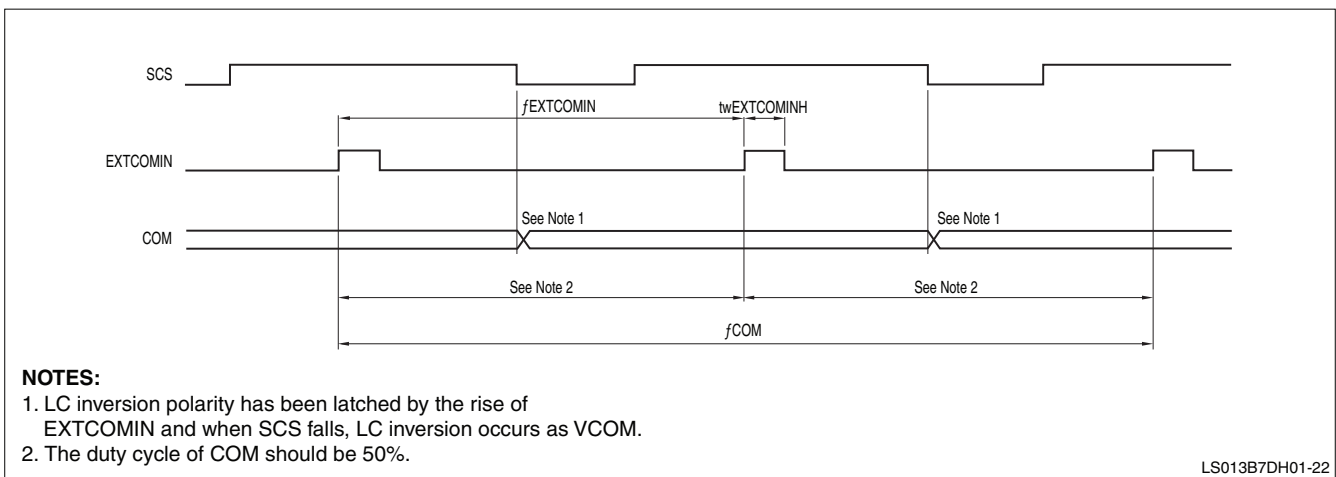When SCS is LOW, VCOM will toggle immediately upon the rise of EXTCOMIN.

1	SCLK
2	SI
3	SCS
4	EXTCOMIN
5	DISP
6	VDDA
7	VDD
8	EXTMODE
9	VSS
10	VSSA

Figure 17. VCOM Hardware Input

NOTES:
1. LC inversion polarity has been latched by the rise of EXTCOMIN and when SCS falls, LC inversion occurs as VCOM.
2. The duty cycle of COM should be 50%.

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Figure 18. EXTMODE = H, Hardware VCOM Toggle; Behavior When SCS = H

NOTES:
1. LC inversion polarity has been latched by the rise of EXTCOMIN internally as COMZ, and because SCS is LOW, LC inversion occurs immediately.
2. The duty cycle of EXTCOMIN should be 50%.
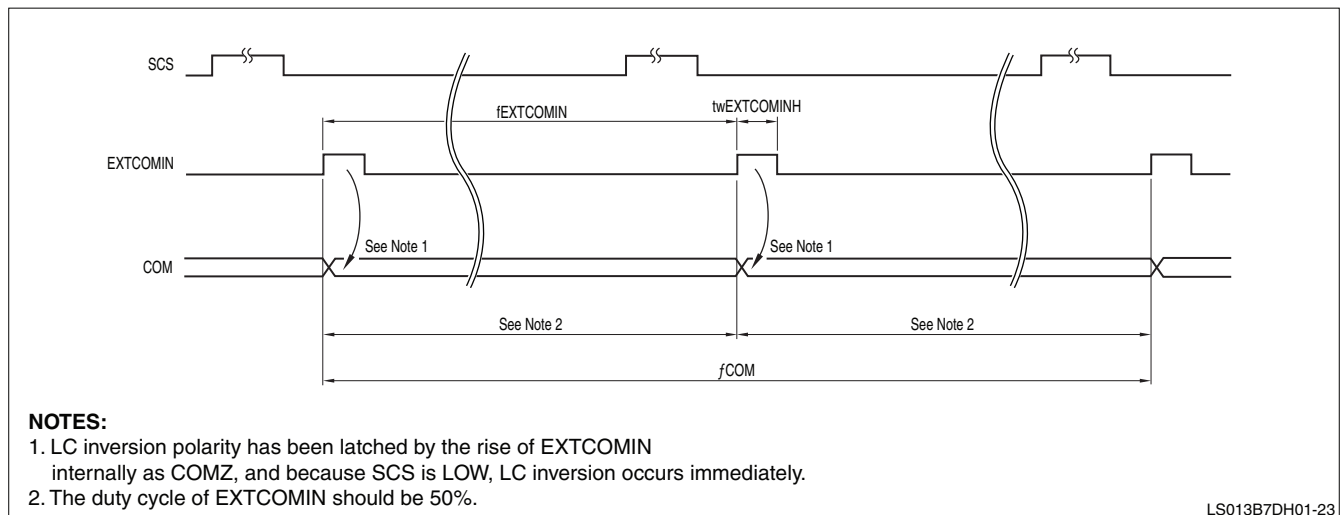
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Figure 19. EXTMODE = H, Hardware VCOM Toggle; Behavior When SCS = L

Further illustration of the SCS-to-EXTCOMIN relationship is shown in Figure 20 and Figure 21. When writing data frequently to the panel, make sure to keep EXTCOMIN at either the same frame frequency or lower.

When holding a static image, make sure SCS stays LOW, to allow the EXTCOMIN signal to toggle VCOM.
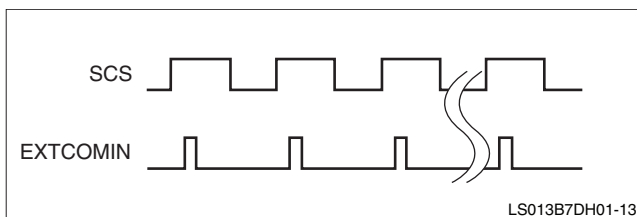

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Figure 20. EXTCOMIN Relationship to SCS: Higher Data Rates
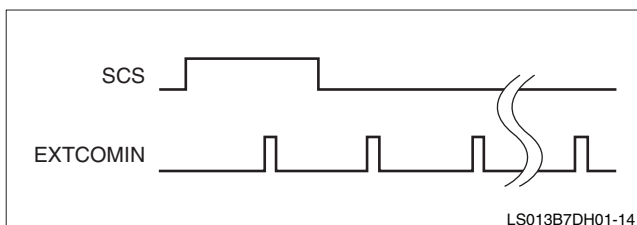

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Figure 21. EXTCOMIN Relationship to SCS: Static Image

DESIGN NOTES

1. This device is static sensitive. Handle it only in a static-safe environment.

2. Do not press on the surface of the module, and do not stack modules in such a way that pressure will be applied to the surfaces or to the connector area. The safest place for temporary storage of modules is in their shipping tray.

3. This part is susceptible to mechanical stress and such stress may affect its display qualities. Keep the part properly supported in the final design and avoid twisting or bending forces upon it.

4. The connector on this module is designed for a limited number of insertions. Do not attempt to solder directly to the connector.

5. The Specifications for this part give definite environmental, electrical, and signal drive conditions for the operation of this module. Operating it outside of these given limits can reduce image quality, shorten its life, or cause it to fail altogether.

6. When displaying static images, Sharp recommends refreshing the image data every two hours to prevent stuck pixels.

7. Recommended storage is in a dark place. Keep it from long periods of exposure to direct sunlight or other sources of ultraviolet light.

8. The liquid crystal material in this module will solidify if stored below the rated temperature, and will become an isotropic liquid if stored above the rated storage temperatures. After such storage, the material may not return to its original properties.

9. Areas external to the display area on this part are light sensitive. Do not allow the gate driver area (the circuit areas outside of the LC glass) to be exposed to light in the final design. Shield these areas.

10. Support for the module should be designed to avoid stress exceeding the maximums given in the Specifications.

11. Do not put a seal or adhesive materials on the glass surface. Picture uniformity defects can result.

12. Do not use chloroprene rubber in the design as it generates chlorine gas and can affect the reliability of the LCD module's connector areas.

13. This part is shipped with a protective film over the polarizer, to prevent scratches or other damage. Remove this film before use. Do not attempt to reapply this film once it has been removed. If the film is reapplied and the LCD module is stored in this condition, the polarizer may be affected enough to cause a picture quality failure.

14. Materials used in setting or epoxy resins (anime hardening agents) and silicon adhesives (dealco-holized or oxime) all release a gas which can affect the quality of the polarizer. Always confirm compatibility with these materials.

15. It is neither a failure nor a defect condition to have a slight change in black level in a black area of an image visible under varying luminance levels and source angles.

16. Use of decoupling capacitors is recommended. See Electrical Specifications.

17. This device can be powered from a 3 V system with these power supply ICs. See Power Supply Reference Circuits for more information.
    – SII: S-8821 Charge Pump Power Supply IC
    – National Semiconductor: LM2750 Charge Pump Power Supply IC

Table 18. Electrical Specifications for 3 V Step-up Power Supply ICs

PART NUMBER	VIN (V)		VOUT (V)			I OUT (mA)
	MIN.	MAX.	MIN.	TYP.	MAX.	
S-8821	2.8	5.0	4.9	5.0	5.1	0.04
LM2750	2.7	5.6	4.8	5.0	5.2	0.04

NOTES:
1. Refer to each manufacturer's specifications for more information.
2. This information is for reference. Evaluate the parts in actual use.
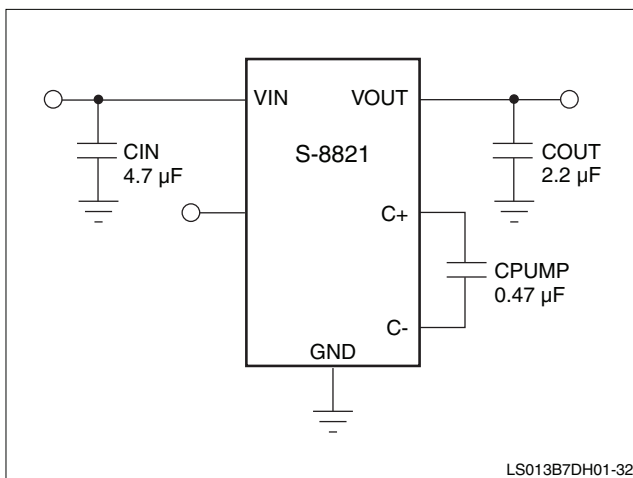
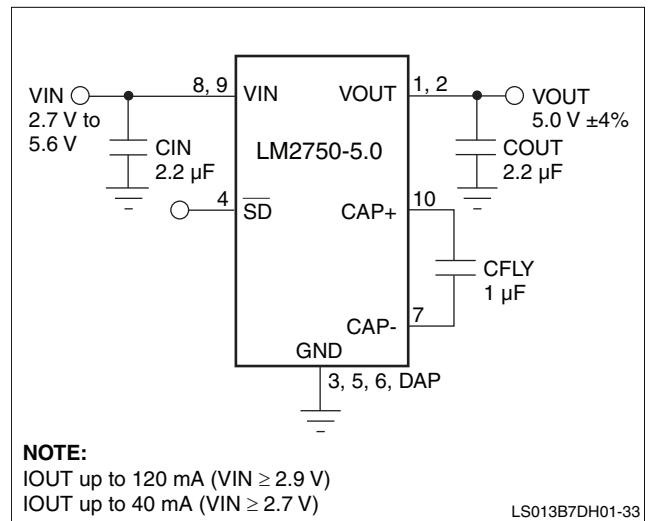POWER SUPPLY REFERENCE CIRCUITS

Figure 22. S-8821 Reference Circuit

Figure 23. LM2750 Reference Circuit

HANDLING, STORAGE, AND PACKAGING

1. This module is not made to be disassembled. Doing so may cause permanent damage.

2. The liquid crystal material in this module is injurious to humans. Do not allow it to get into the eyes or mouth. If any liquid crystal material gets on skin or clothing, immediately wash it out with soap and water.

3. This module is RoHS compliant, and does not use any ODS (1,1,1-Trichloroethane, CCL4) in its materials or in its production processes.

4. When discarding this module, dispose of it as glass waste. This LCD module contains no harmful substances. The liquid crystal panel contains no dangerous or harmful substances. The liquid crystal cell contains an extremely small amount of liquid crystal (approx.100 mg) and therefore will not leak; even if the panel should break.

5. The material used in this panel has a median lethal dose (LD50) of greater than 2,000 mg/kg and tests negative (Aims test) for mutagenic properties.

6. When storing this module, keep it from long periods of exposure to direct sunlight or other sources of ultraviolet light. Recommended storage is in a dark place.

7. The liquid crystal material in this module will solidify if stored below the rated temperature, and will become an isotropic liquid if stored above the rated storage temperatures. After such storage, the material may not return to its original properties.

8. Storing this part in high humidity will damage the polarizer. Keep humidity controlled when in storage.

9. These parts are static sensitive. Handle and store them in a static-controlled area.

10. These parts are glass and as such are fragile. As with any glass, they may also contain sharp edges, and are susceptible to damage through mishandling or abuse.

11. The handling area must be free of any corrosive elements such as salt air and acid or base gases, to keep end reliability high.

Cleaning

1. Water drops on the polarizer must be wiped off immediately as they may cause color changes or other defects if allowed to remain.

2. To clean these parts, wipe their surface with a soft cloth.

3. If further cleaning is needed, use IPA (isopropyl alcohol) and a light touch on the surface. Do not use organic solvents as they may damage the terminal area - which uses organic materials.

4. When cleaning the terminal area is required, wipe with a soft cloth or cotton swab.

5. Do not touch these parts with bare fingers. Fingerprints may leave an indelible mark on the polarizer, and fingerprints may degrade the terminal area, causing future circuit failures.

Storage

1. Store these devices at a temperature range between 0°C and 40°C, at 60% RH or less.

2. Use within 3 months.

3. Open the package within an area that has proper static control precautions, and less than 50% RH.

4. When storing this module, keep it from long periods of exposure to direct sunlight or other sources of ultraviolet light. Recommended storage is in a dark place.

Packaging

Figure 24 shows the serial number schema. Figure 25 shows the location where the serial number is printed.
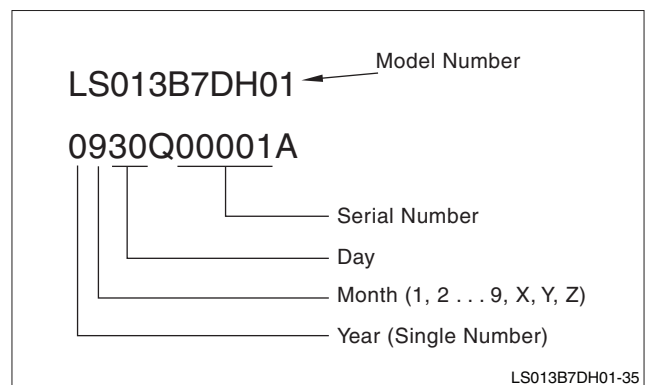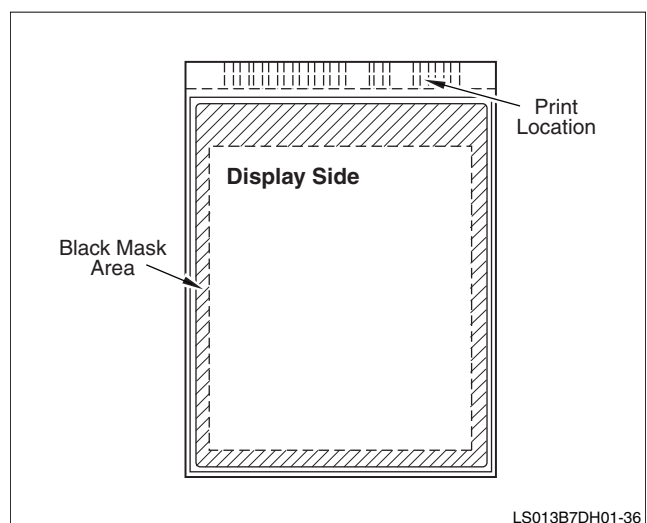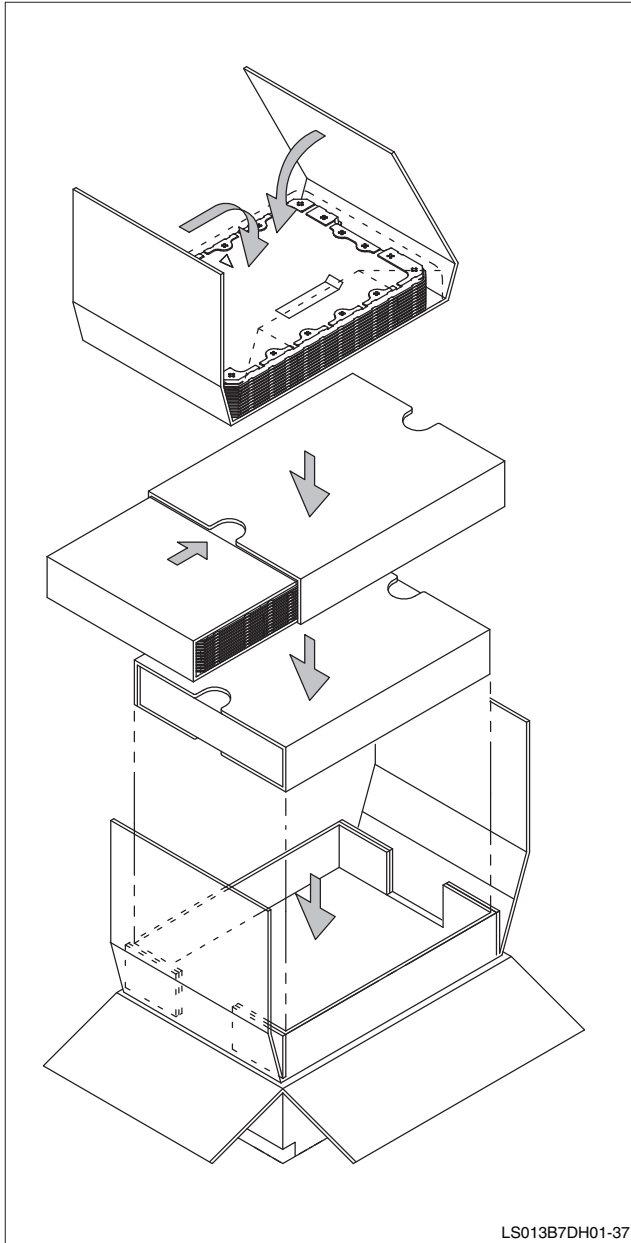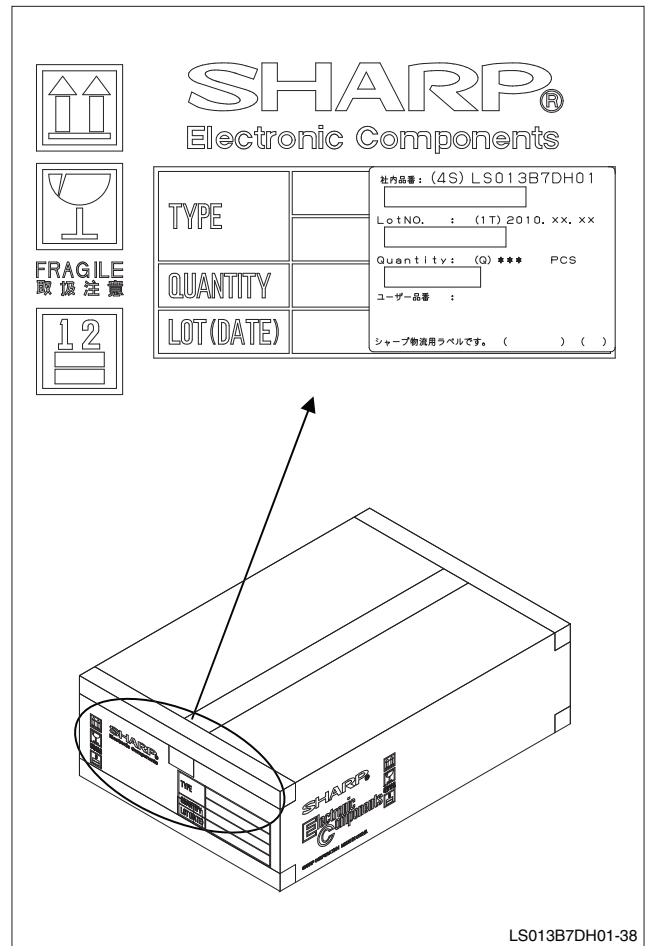

Figure 24. Serial Numbering

Figure 25. Serial Number Location

Packaging Diagrams

Figure 26. Packaging Format

Figure 27. Package Labeling

RELIABILITY
Environmental Reliability

Table 5. Test Item Reliability

NO.	TEST ITEM	TEST CONDITION
1	High temperature storage test	Ta = 80°C, 240h
2	Low temperature storage test	Ta = 30°C, 240h
3	High temperature and high humidity operating test	Tp = 40°C/95% RH, 240h
4	High temperature operating test	Tp = 70°C, 240h
5	Low temperature operating test	Tp = -20°C, 240h
6	Shock test	Ta = -30°C (1h) to +80°C (1h) / 5 cycles
7	Electrostatic discharge test	±200 V, 200 pF (0 Ω) once per terminal

NOTES:
1. Ta = ambient temperature, Tp = panel temperature
2. Check for any items which impair display function

Physical Reliability
• The Panel surface stress specification parameter is the stress force [N] before image failure.

• Load test: Minimum 120[N]; on an LCD panel with polarizer, fixed to a test stage.

• Pressure point is the center of the panel, with a φ10 mm column, at 1 mm/minute.

• Full pressure is held for 5 seconds after achievement, then released.

• Panel must survive this test without any image failures.

SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE.

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