VERY HIGH SPEED INTEGRATED CIRCUITS

- VHSIC -

FINAL PROGRAM REPORT

1980 - 1990

VHSIC PROGRAM OFFICE

OFFICE OF THE UNDER SECRETARY OF DEFENSE FOR ACQUISITION
DEPUTY DIRECTOR, DEFENSE RESEARCH AND ENGINEERING
FOR RESEARCH AND ADVANCED TECHNOLOGY

SEPTEMBER 30, 1990

FOREWORD

This report presents a description and final account of the VHSIC program during its ten years of successfully developing advanced integrated circuit technologies and products for military systems. The new technologies and the products that VHSIC has produced have steadily found their way not only into defense systems but also into the commercial industrial base. They provide the reservoir from which new system capabilities are emerging and a foundation upon which continual further advances are being made.

Over the course of the past decade, the VHSIC program has been active in the development of new materials, new circuit design concepts, advanced fabrication processes, new manufacturing equipment, higher levels of radiation hardening, new data interface standards and specifications, and improved techniques for built-in-test and maintainability. The VHSIC Hardware Description Language and other design automation tools have broken through major integrated circuit complexity barriers and will decrease the cost and the development time of modern electronic systems. The resulting achievements have helped to produce a new level of system design and fabrication --- one that approaches an integrated "concept-to-system" capability.

The broad scope of technology that VHSIC activities included and the almost universal application of IC technology in military systems required an unusual structure and management strategy for the program. Although most of the technology work was in the "research and development" category, the identified goals and near term objectives were to insert the technology products into systems as soon as possible --- either as updates to then-current systems or as enhancements to systems in the design and development phase. In addition, the applicability of almost all of the technical achievements of the program to commercial IC production meant a continuing high interest on the part of the entire semiconductor industry in the progress of the program. A corresponding responsibility was required on the part of the VHSIC program managers to consult with the industry leaders and be aware of their concerns. Finally, since the technology was (and is) broadly applicable to the electronic system requirements of all the military Services, an integrated Department of Defense management was adopted which involved the participation of technical and contract managers at the Services' headquarters and technical specialists from many of the Service laboratories.

The results of the VHSIC program will continue to be absorbed into industrial practice and DoD procurement for many years as new IC production capabilities are achieved and new systems designs are placed into operation. Continuing developments in integrated system design techniques will allow a design, simulation, and re-design process that ensures optimum performance at low development costs. The evolution of the Qualified Manufacturing Line procedure will make it possible to produce highly complex ICs as military qualified parts without incurring excessive qualification costs.

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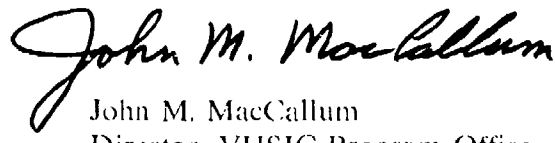
The legacy of the VHSIC program is a broad spectrum of technological advances, the enhanced military capabilities, and the maintenance of U.S. leadership in an area of technology that is vital to our national well being.

In carrying out its activities the VHSIC program involved a major portion of the U.S. semiconductor industry and a considerable number of technical managers and specialists in the Department of Defense. The success and achievements of the program would not have been possible without their leadership initiatives and dedicated, enthusiastic efforts.



John M. MacCallum
Director, VHSIC Program Office
ODDDRE/R&AT

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CHAPTER 1

EXECUTIVE SUMMARY

In March 1980, the Department of Defense began the Very High Speed Integrated Circuits (VHSIC) program to develop advanced silicon integrated circuits. In September 1990, the VHSIC program officially came to an end in terms of starting new activities. During the intervening decade, with funding of approximately $918M, VHSIC organized the efforts of hundreds of engineers, scientists, and managers, and scores of companies in a highly technical and complex enterprise. For much of that time VHSIC was considered one of the highest priority technology programs in the DoD and of vital importance to sustaining the military superiority of the United States. This Final Report is an update to and summary of the Annual Reports for 1986, 1987, and 1988 (References 2.27-2.29). Together, these four reports provide an overall documentation of the VHSIC program.

This report presents the rationale and objectives of the program, the organization and structure through which it directed its efforts, the results that were achieved from its many activities, and independent assessments of the impact that it has had on integrated circuit technology and its use in military systems. Such an assessment by one of the primary initiators of the VHSIC Program is included at the end of this Executive Summary.

"VHSIC is our highest priority technology and we will continue to provide strong management emphasis in order to achieve the increased military capability expected from its results."

- Richard D. DeLauer, Under Secretary of Defense for Research and Engineering. Statement to the 98th Congress, First Session, March 1983.

Background And Program Objectives – (Chapter 2)

Prior to 1980, the DoD had spent several years carefully assessing its needs and deficiencies in integrated circuit technology. The major deficiency perceived was that the DoD deployment of military products incorporating state of the art microelectronic technology was running ten or more years behind the appearance of that technology in the commercial market. Worse still, the delay was increasing with time. However, the need for ready access to this technology had become increasingly vital to the U.S. defense posture as the weapon systems being deployed became more and more dependent on electronic subsystems for their effectiveness, for their speed of response, and for their adaptability in rapidly changing battle environments.

The goal of the VHSIC program was to correct that deficiency by giving system developers and acquisition managers a military qualified microelectronics technology that was on par with or better than the technology available commercially.

Program Structure – (Chapter 2)

VHSIC presented the DoD with an unusual program concept to define and manage. The technology of integrated circuits was (and is) broadly applicable to a wide and rapidly growing variety of uses which were dominated by commercial activity. The application of integrated circuits in military equipment was also pervasive throughout the Services, on all platforms, and in most weapon systems. The program would therefore have to face the problems of developing new generations of complex integrated circuits in cooperation with the leaders of the semiconductor industry and then finding effective ways to make them readily available to the military systems community. The core of VHSIC was the development of a new level of "high tech" electronics design and manufacturing which, it was realized even then, would have strong implications for changes in other indispensable system acquisition activities such as military qualification procedures. The management and structure of the VHSIC program therefore had to integrate all of these elements into a compatible set of comprehensive and interactive activities.

To define and organize the tasks that would have to be carried out, a VHSIC Program Office (VPO) was established in the Office of the Under Secretary of Defense for Research and Engineering (later to become OUSD for Acquisition) for overall management and direction of the program. The Army, Navy, and Air Force each set up corresponding offices to award and administer the contracts. They also provided the detailed, day-to-day technical management of the program, the technical teams required for program reviews, and the in-house skills and facilities for testing the VHSIC products.

Under the coordination of the VHSIC Program Office, a high degree of tri-Service cooperation and task sharing was achieved. The formulation of programs and the evaluation of proposals were carried out jointly. Representatives from all the Services and other DoD components attended the program reviews and provided technical evaluations to the program managers. This cooperative environment permitted the administrative tasks of letting and monitoring contracts to be distributed among the Services while the technical tasks were handled by the DoD VHSIC community as an organic whole, each Service contributing the expertise of its internal technical staffs and sharing the information gained as the contractors made progress.

The program was divided into the following distinct activities.

Phase 0: a one year concept definition effort to prepare a detailed development plan to accomplish the technical objectives set out by the VHSIC program office. Emphasis

was put on 1.25 micron minimum feature size and 25 megahertz clock speed. Nine companies participated in Phase 0, starting in March 1980.

Phase 1: a primary effort, based on the approaches defined in Phase 0, to develop and produce silicon chips with 1.25 micron minimum feature sizes and 25 MHz clock speed, and to demonstrate them in subsystem brassboards. Phase 1 contracts were awarded to Honeywell, Hughes, IBM, Texas Instruments, TRW, and Westinghouse in May 1981.

This phase was later expanded to include a yield enhancement program to increase the yield or producibility of the VHSIC chips.

Manufacturing Technology: the development of better manufacturing tools and techniques that were needed to make the VHSIC chips producible and affordable. These projects were defined and funded jointly with the manufacturing technology programs in the Services.

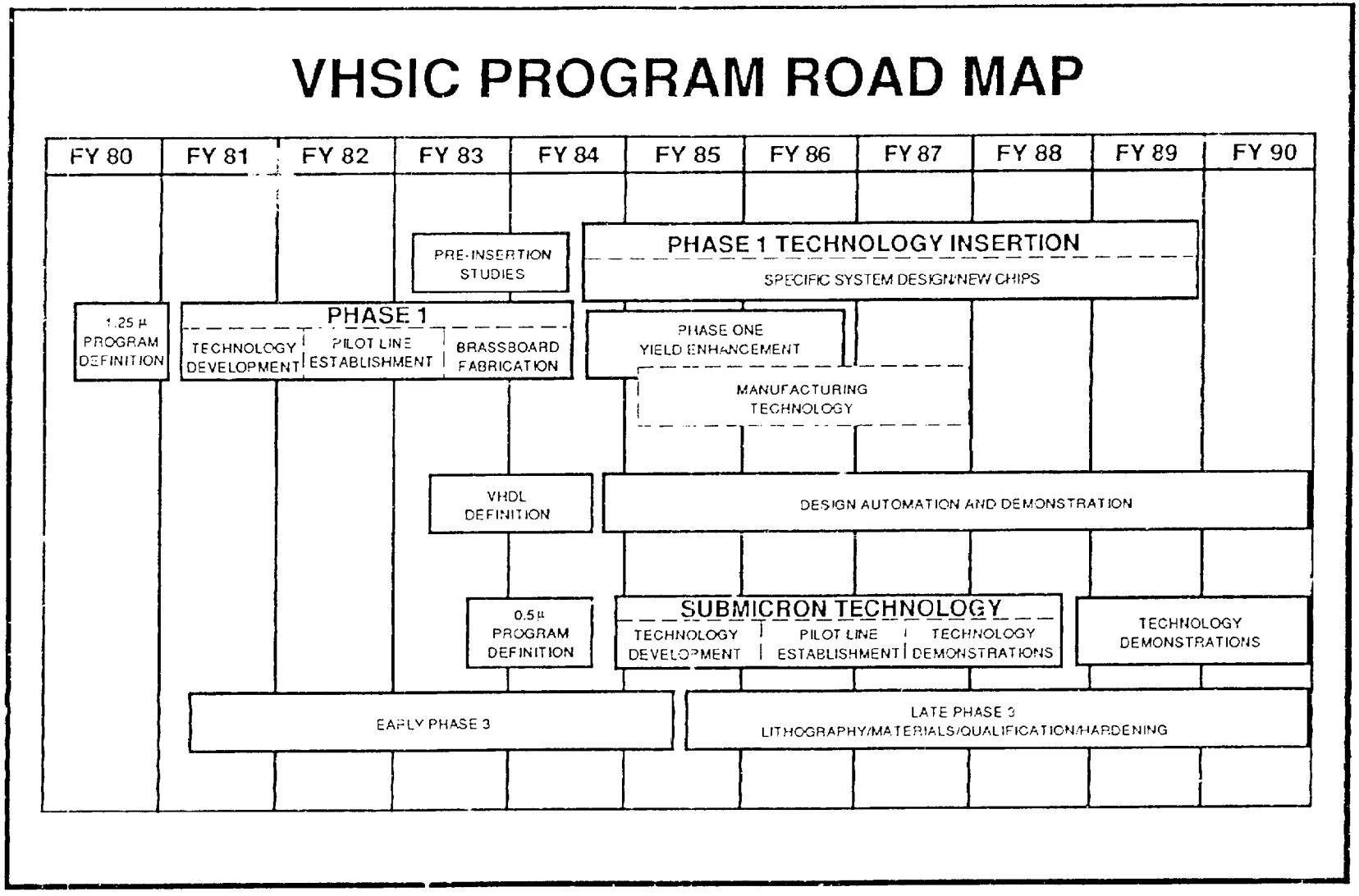
Design Automation: the development of the design tools, standards, software, and hardware needed to make the design of large, complex VHSIC chips more effective and affordable.

Technology Insertion: the demonstration of VHSIC Phase 1 chips and technology by inserting them into a broad variety of military systems, both existing systems and others still in development. In cooperation with the system program offices, VHSIC co-funded both feasibility studies and demonstrations of hardware in operating systems.

Phase 2: a primary effort to develop and produce (on a pilot line basis) silicon chips with 0.5 micron minimum feature size and 100 megahertz clock speed. This phase was started after it became clear that development of the 1.25 micron technology and its transition into manufacturable products could, in fact, be accomplished. The contractors selected to undertake the submicron development tasks were Honeywell, IBM, and TRW. Contracts were awarded and work began in November 1984.

Phase 3: a broadly based collection of separately funded contracts conducted concurrently with Phases 1 and 2. These supporting technologies were found necessary to meet the program objectives. Specific efforts were undertaken to deal with technology applications, materials requirements, lithography and fabrication tools, design software development, packaging, chip qualification, and radiation hardness.

A "roadmap" of these program activities and the overall program funding profile from 1980 to 1990 are shown in Figures 1.1 and 1.2.



VHSIC

Figure 1.1 VHSIC Program Roadmap

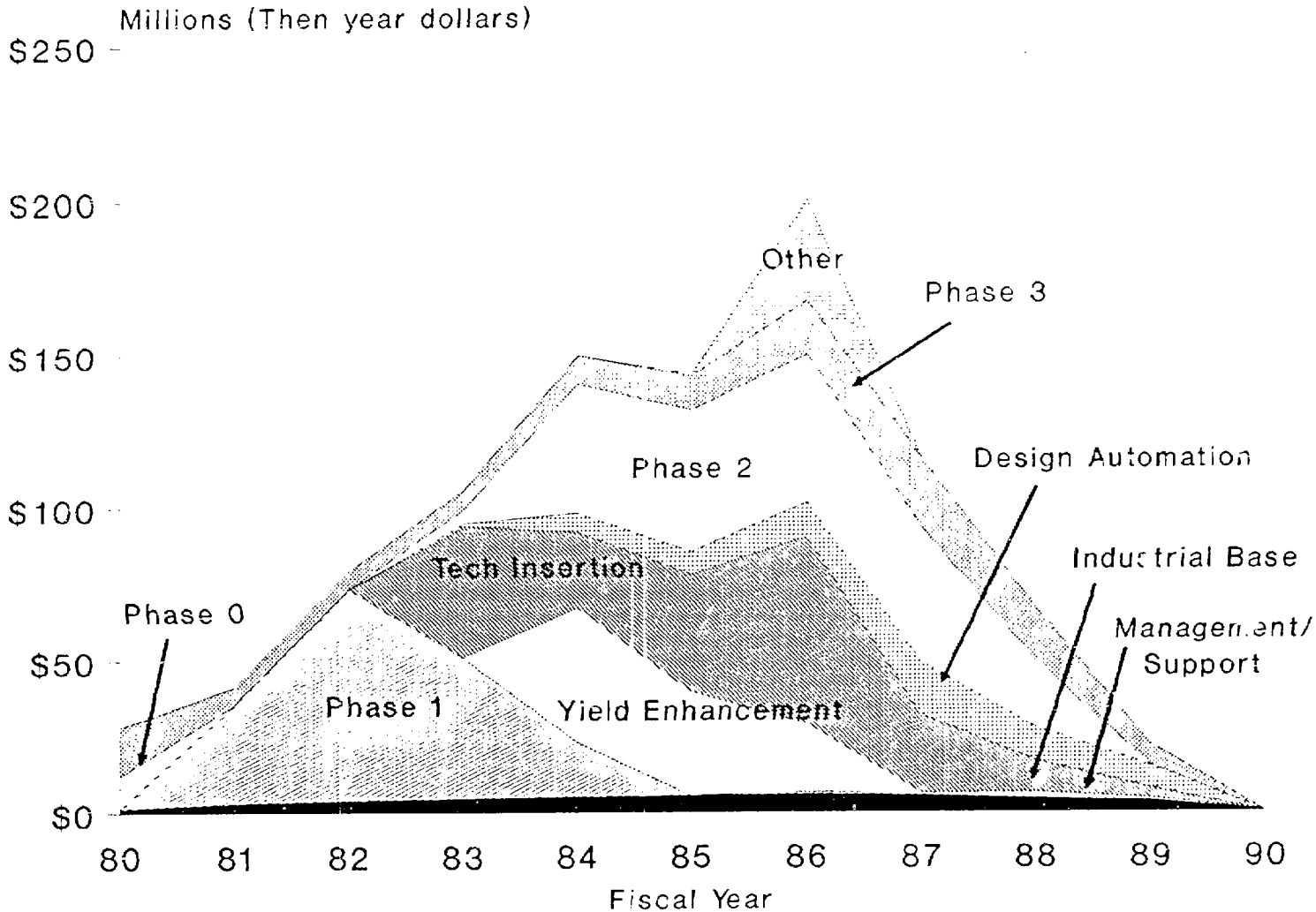


Figure 1.2 VHSIC Funding Profile

Security

The House and Senate Conference Report for the 1980 Defense budget, which authorized the initial funding for the VHSIC program, included the following statement:

> *"The export of the technology developed in this (VHSIC) program would be controlled where applicable by the ITAR until the state-of-the-art for such technology progresses to the point where national security permits its transfer to other controls for export".*

This statement represented a departure from the existing administrative controls on microelectronics. Only those devices specifically designed for military application had previously been controlled by the ITAR. All dual-use or general purpose devices, even those built to military specifications, were controlled under the Export Administration Regulations (EAR) of the Department of Commerce.

As the Defense VHSIC Program officially came to an end, the VPO no longer considered it necessary or appropriate to single out "VHSIC" devices for special control. The terms of the Congressional mandate for release from ITAR control were met by the diffusion of the technology throughout the industry and the subsequent availability of comparable technology in Europe and the western Pacific.

The VPO also supported authorizing the use of devices developed under this program in commercial applications. Such devices would be properly identified as "dual-use" and would then be subject to the same EAR control as other commercial integrated circuit devices.

Program Results

The results of the decade of work conducted by the VHSIC program are summarized in the remainder of this Executive Summary. A chronology of some of the more significant events that occurred during the course of the program are listed in Table 1.1 at the end of this chapter. More details are described in Chapters 2 through 7 of this report. The most complete technical accounts and the fullest documentation of results will be found in the references that are listed in Appendix A. Included at appropriate places throughout this report are individual assessments of the VHSIC program which have been contributed by people who have been mostly outside of the VHSIC program offices but who have participated in VHSIC activities in various positions. Each contribution provides an evaluation, from the author's personal perspective, of the impact that VHSIC has had either on a company position with respect to IC technology, on DoD applications of IC technology, or on particular areas of IC technology.

Table 1.2 VHSIC Chips Demonstrated in Phase 1 and Phase 2

Chip Name	Equivalent Logic Gates (x1000)	Size (Mils)	I/O Pins
Phase 1 Chips			
Honeywell: Pipeline Par Proc	28	311x309	180
Sequencer	27	300x300	180
Arithmetic Unit	18	300x300	180
Hughes: Multiple Channel Correlator	18	368x315	148
Single Channel Correlator	20	397x367	148
Signal Tracking Subystem	14	360x360	148
IBM: Complex Multiplier/Adder	37	320x320	240
T.I.: Data Processing Unit	16	350x350	84
Vector Arithm Logic Unit	17	353x365	164
Vector Address Generator	12	301x312	84
Array Controller/Sequencer	10	301x312	84
Device Interface Unit	16	350x350	84
Multipath Switch	4	250x265	84
General Buffer Unit	10	341x312	84
Static RAM		240x264	32
TRW: Window Addressable Memory	11	310x290	132
Content Addressable Memory	12	314x272	132
Register Arithm Logic Unit	6	337x330	132
Multiply/Accumulate	8	320x298	132
Address Generator	10	336x285	132
Microcontroller	6	346x306	132
Matrix Switch	2	200x200	132
Four Port Memory	13	290x313	132
Westinghouse: Static RAM	30	190x310	42
Pipeline Arithmetic Unit	33	340x350	224
Extended Arithmetic Unit	26	340x350	224
Extended Arithmetic Unit Mult	23	340x350	224
General Purpose Controller	20	340x350	224
10K Gate Array	10	280x304	224
Phase 2 Chips			
Honeywell: Array Processor Unit *	32	370x370	270
Array Processor Controller *	27	370x370	270
Bus Interface Unit **	19	280x280	180
IBM: Systolic Processor	33	215x215	180
Configurable Static RAM	9	215x215	180
Address Generator	24	215x215	180
Bus Interface Unit	15	215x215	180
Signal Processing Element	10	151x151	180
TRW: CPUAX Superchip ***	4100/1700	1500x1600	275

* Personalization of a 70K configurable gate array
** Personalization of a 35K configurable gate array
*** Total transistors on chip/number needed to operate fully

The direct activities of VHSIC were concentrated in four broad areas --- design and design automation, fabrication and manufacturing technology for VHSIC chips, insertion of VHSIC products into systems, and the transfer of the technology into the broader industrial community involved in military system development.

Design and Design Automation: (Chapter 3, Sections 3.1 and 3.2)

Twenty-nine chips for Phase 1 and nine chips for Phase 2 were designed, produced, and demonstrated during the VHSIC program. They constituted very complete and powerful chip sets which were capable of performing the wide variety of signal processing functions needed by military weapon systems and were used experimentally to explore specific system applications. These chips are listed in Table 1.2.

In order to design chips of such functional complexity and large physical size, the VHSIC program needed advanced design automation tools. Design standards were also needed to make sure that the resulting chips would operate successfully in real system environments. The VHSIC efforts in this very dynamic and rapidly growing field of technology have had a strong influence on many of the directions taken in design tool development. The most visible influence has been the development of the VHSIC Hardware Description Language (VHDL) which was adopted as a international commercial standard by the IEEE in December 1988.

The VHDL provides a powerful computer language by which both the hardware structure and the electrical behavior of any IC can be described. The VHDL description can be used in the design process to simulate the performance of the chip and make sure that it will operate as desired. It can also be used to generate the computer programs for testing the chip after manufacture, to transfer the design data from one company to another for second source production, and to provide archival documentation of the chip design in case it needs to be remanufactured in the future. As a result of its usefulness in the acquisition and maintenance of electronic systems, VHDL has been adopted as a DoD requirement for microcircuit documentation.

"ASIC documentation in VHDL. Digital Application-Specific Integrated Circuits (ASICs) designed after 30 September 1988 shall be documented by means of structural and behavioral VHSIC Hardware Description Language (VHDL) descriptions in accordance with IEEE 1076. Behavioral VHDL descriptions shall describe the input/output behavior at a sufficiently detailed level to permit the behavioral description to be used within a larger VHDL model for test generation and fault grading of the containing model.

> *Fault coverage. Fault coverage shall be reported for the manufacturing-level logic tests for all digital microcircuits designed after 30 September 1988. Fault coverage shall be based on the equivalence classes of single, permanent, stuck-at-zero and stuck-at-one faults on all lines of a TISSS-compatible structural VHDL model, where the structural model is expressed in terms of gate-level primitives or simple atomic functions (such as flip-flops)."*
>
> *DOD MIL-STD-454L, Requirement 64 (Microelectronic Devices)*
> *September 20, 1988*

VHSIC also emphasized the need for system level design tools. The increasing functional complexity of VHSIC chips was bringing the concept of an "electronic system on a chip" much closer to realization and so the design of individual chips was no longer isolated from the design of the overall system. The Architectural Design and Assessment System which was developed under a Phase 3 contract has found widespread use in the design of optimal system architectures. The development efforts begun by VHSIC have been continued in many cases under separate Service sponsorship.

VHSIC required that testing capabilities be built into the chips so that they could provide self-generated data on their readiness to operate. This requirement resulted in the development of very sophisticated built-in test design methodologies that are now in use.

Four standards were developed to provide for the interoperability of VHSIC chips with each other and with the other system components. The standards include an electrical specification for direct interfacing of all VHSIC chips, a parallel interface bus for message and data communication on a system backplane, a serial test and maintenance bus for sending and receiving test data signals on the system backplane, and a serial element test and maintenance bus for test data communication with individual chips on the same circuit board. These standards are part of a group of data bus and interface standards that were developed and transferred to the larger industrial (and international) electronic community for use in the controlled exchange of data.

Fabrication and Manufacturing Technology: (Chapter 3, Section 3.3)

The VHSIC contractors developed technologies for fabricating the complex, large area, signal processing chips first with 1.25 micron and then with 0.5 micron feature sizes. They accomplished this on time schedules which, in both cases, produced manufacturing prototype chips ahead of the time schedules for the production of equivalent commercial chips. Twenty

nine different 1.25 micron chips and nine 0.5 micron chips were designed, fabricated, and demonstrated. Many new and difficult fabrication problems had to be solved, especially in the areas of silicon substrate material, fine-line lithography, multi-layer metalization, and packaging.

"...most experts agree that without VHSIC, semiconductor development in the U.S. wouldn't have progressed so quickly toward submicron geometries, even in the commercial world."

"Among the technical breakthroughs spawned by VHSIC is the use of multiple layers of metal in advanced semiconductors, now a routine design feature in high-density ICs."

"What Did We Get From VHSIC", Electronics, June 1989, p. 97

The first VHSIC chip with 1.25 micron technology was produced in February 1983. Since that time, the technology has evolved into a full production capability at a large number of industrial manufacturing lines. A representative list of such companies with their VHSIC manufacturing capabilities is included in Chapter 7.

The culmination of the manufacturing technology developed in the VHSIC program was the successful fabrication and operation by the Phase 2 contractors of highly complex, capable, 100 megahertz, 0.5 micron chips. IBM demonstrated a set of four signal processing chips in an acoustic beamformer brassboard in December 1988, TRW demonstrated an operating VHSIC "superchip" in December 1989, and Honeywell is scheduled to demonstrate a set of three customized gate array chips in a cruise missile guidance application in September 1990. The TRW "superchip", for example, measures 1.5 inch by 1.6 inch and contains over 4 million transistors. More than one half of the transistors are used as redundant elements that are automatically switched into operation, if needed, to ensure that the chip is functioning properly before it leaves the manufacturing line. This design characteristic also guarantees that the chip will have an extraordinarily extended lifetime in satellite applications or other unattended operations.

After an intensive effort on manufacturing yield enhancement, the various Phase 1 chip types were produced on pilot production lines at yields that ranged from under 10%, which is marginal for production, to over 70% which is high enough to enter confidently into full scale production.

One of the major requirements of VHSIC was that the chips be operable in severe radiation environments. In coordination with the Defense Nuclear Agency, the VHSIC program developed fabrication technologies which could, by the end of Phase 2, produce chips that were fully capable of meeting military radiation hard specifications at very little, if any, extra cost.

System Insertion: (Chapter 5)

A very substantial portion of the VHSIC management efforts and funding went into approximately twenty-seven system demonstration projects in which VHSIC chips and boards were integrated into system hardware so that the benefits and advantages could be realistically evaluated in a variety of applications. An even larger number of system insertion demonstrations were undertaken independently by system program offices, using the design and manufacturing capabilities developed by VHSIC program contractors. The technology insertion demonstrations, many of which continued beyond the formal close of the VHSIC program, have shown that VHSIC is highly effective in benefiting the performance, weight, space, power, and reliability of systems. Some platform systems in development, such as the LHX helicopter and the ATF fighter, are using electronic subsystems which would be impossible to design and build within the constraints of weight and space imposed by the platforms without the technology made available by the VHSIC program.

"When the helicopter-borne version of the AT&T-built AN/USY-2 enhanced modular signal processor enters fleet service in 1995, it will give anti-submarine forces 18 times the power of existing units at half the weight."

Defense Science, April 1990, p. 50

Two examples of the successful early insertion of VHSIC technology into systems that have passed the full scale development stage and are scheduled for production are the AN/APG-68 airborne radar signal processor by Westinghouse for the F-16 aircraft (scheduled for 1991 production) and the AN/AYK-14(V) airborne computer by Control Data Corporation (scheduled for 1990 production). These are described in Sections 5.3.4 and 5.2.2 respectively. In particular, the AN/AYK(V) insertion proved that the benefits expected of VHSIC could in fact be achieved in real systems, as the following table shows.

	Previous Version	VHSIC Version
Number of chips	13	5
Complexity per chip	4000 gates	35,000 gates
Chips fabricated	51	5
Cost per chip	$50,000	$130,000
Total chip cost	$2,550,000	$650,000
PCB Iterations	4	1
Check out time	15 months	4 months
Design to brassboard	42 months	30 months

Another important aspect of the technology insertion effort involved the use of VHSIC design and fabrication technology to alleviate the "obsolete parts" problem. Many of the integrated circuit chips used in military equipments go out of production as time progresses. This creates a difficult and expensive maintenance or resupply problem. The Air Logistics Command Center at Sacramento used the VHSIC technology to design circuit boards that were "form, fit, and function" replacements for equipment in the F-111 aircraft. The result was much less expensive than procurement of exact replacement parts, an improvement in reliability, and a much faster design cycle. Although the VHSIC program was neither designed nor expected to solve the broader aspects of system acquisition problems, it developed a technology that was available not only for designing and building new, advanced systems but also was very useful in solving some otherwise intractable problems of resupply and retrofit for older electronic subsystems.

Technology Transfer: (Chapters 6 and 7)

VHSIC has carried out the task of transferring the technology developed in the contract programs to the people and organizations that could use it most effectively, in three direct ways.

First, the contract programs were conducted on a highly interactive, tri-Service basis, led by a Steering Committee composed of the DoD Program Director and the three Service Program Directors. The Steering Committee set policy, initiated programs, and evaluated progress. Formal, semi-annual (sometimes quarterly) technical reviews of each Phase 1 and Phase 2 contract were attended by technical evaluators from each of the Services. Technical committees in such areas as lithography, packaging, CAD, and qualification were formed, with representatives from each of the Services. These committees interacted closely with the contractors, helped to solve technical and programmatic difficulties, served as advisors to the Program Offices, and provided liaison with system program managers. The result of this management structure was a high level of communication, coordination, and cooperation within VHSIC and between VHSIC and potential system users.

Second, in order to increase the flow of information to potential users, the Program Office set up a series of VHSIC Application Workshops to describe the products being developed and the ways in which they could be applied in systems. Workshops for specialists in technical areas such as CAD, packaging, and qualification were organized and held at which information was exchanged, problems defined, and various approaches charted. More than forty such workshops were conducted in all sections of the U.S.

Third, a number of major conferences were organized, the most prominent of which were Annual VHSIC Conferences, held from 1982 to 1989. At these, the status of the total program was presented to a wide spectrum of technical and management attendees from Government and industry. Two VHSIC Tech Fairs were held at which the wares of most of the VHSIC contractors were displayed and demonstrated. Technical VHSIC sessions were organized at the Government Microelectronic Conference (GOMAC) for the years 1978 through 1989.

An important indirect mode of technology transfer activity also took place. The very existence of the VHSIC program and the visible results of its contract efforts spurred other companies to initiate independent IC technology development programs with the intention of remaining current and competitive. Several companies (including Raytheon in Phase 1 and Harris in Phase 2) even entered into no-cost contracts with the Government in order mutually to share information during their development activities. By the end of the VHSIC program the list of companies that had gained a VHSIC capability included most of the major IC fabrication and/or design houses in the United States.

There were other indirect processes, such as the wide distribution of technical reports and the development of DoD requirements documents, by which VHSIC technology diffused into the electronics industry and into the procedures for the procurement of military equipment.

The Impact of VHSIC

VHSIC pursued certain specific goals in carrying out its program. ICs with fixed specifications and electronic brassboards configured for particular weapon systems were required to be demonstrated. On the other hand, because of the broad utility of IC technology, the impact of VHSIC activities and results could be equally broad and, therefore, difficult to measure. In order to assess the impact correctly one must, therefore, have a clear understanding of what VHSIC was expected to produce.

The fabrication goals of 1.25 and 0.5 micron feature sizes and the FTR goals of $5x10^{11}$ and $1x10^{13}$ gate-Hz/cm^2 were expected to be within the boundaries of the then-current development programs of the leading semiconductor companies. In fact, those were the

conditions under which the development contracts were let. The expectation was that these goals would accelerate the emergence of technology that was already under active commercial development and hasten its application to military designs. In many cases these VHSIC goals required the contractors to operate at the leading edge of their development efforts. For example, increased chip functionality required larger chip sizes which in turn required advances in optical lithography, multilevel chip interconnects, and packaging technology. The reduction in feature size to 0.5 micron in particular put a heavy emphasis on the development of high resolution lithography using both electron beams and light optics.

Therefore, the specific chips that were developed during Phases 1 and 2 and used in application brassboards were primarily intended to demonstrate that a comprehensive mastery of the technology which met the stringent VHSIC requirements could indeed be achieved. It was also hoped that derivatives of these chips would find wide spread system application and, therefore, be required in increasingly large numbers. They would also be quickly absorbed into the DoD acquisition process. This indeed did happen in some cases. In other cases the technology has evolved and diffused more indirectly so that the impact of VHSIC must be looked for beyond the bounds of the VHSIC hardware itself.

Chapters 2, 3, 5, and 7 of this report include articles on VHSIC that have been contributed by people who were participants in the program or who have closely followed the program activity in a particular field of technology. The papers they have written are their personal views of the impact VHSIC has had and include some descriptions of company-specific case histories by managers involved in VHSIC contracts. The contributed papers also emphasize that many of the applications of VHSIC, especially in the design automation area, are ongoing and even accelerating. Therefore the impact of VHSIC in some areas will increase in time.

This Executive Summary concludes with one such assessment by the initial architect of the VHSIC program in his role as a former Director for Electronic and Physical Sciences in the Office of the Under Secretary of Defense for Research and Engineering.

The Impact of VHSIC

Leonard R. Weisberg
Vice President, Corporate Research and Engineering
Honeywell, Inc.

The VHSIC program has had a profound impact on Honeywell's and other companies' technology and business strategies, and thus on the United States defense capabilities. Besides greatly accelerating the use of new technology ICs in

our military systems, VHSIC provided additional significant advantages including the VHDL language, high—speed multi—chip packaging, and interoperability standards. Furthermore, the VHSIC program established, at Honeywell, a source of highly advanced radiation hard ICs for critical space and strategic applications.

Impact on DoD Systems

In order to maintain the U.S. technology lead, the use of new technology ICs in military systems had to be accelerated. Highly advanced ICs had to be available for military use at the same time they became available for the commercial market, or even earlier. Even though the military portion of the IC market had shrunk to 7%, industry's attention had to be refocused onto military needs.

To accomplish this, a very different kind of program was needed. VHSIC was established with strong DoD policy support and unprecedented funding levels for a broad technology research and development program. VHSIC focused attention not only on advancing the IC technology, but also on special military system requirements including ultra—high speed processors for which the commercial demand is limited.

The VHSIC program galvanized the semiconductor IC industry into action. Several of the largest IC manufacturers became contractors or subcontractors in the VHSIC program including IBM, Motorola, TI, and National; it is noteworthy that the last three are presently among the top five producers of military ICs. Similarly, VHSIC became the focal point of attention among the top military contractors for electronic systems and subsystems, with Westinghouse, Hughes, TRW, and Honeywell as main contractors in VHSIC.

The VHSIC technology goals were symbolized by the numbers 1.25 micron ("near—micron") and 0.5 micron ("submicron"). These numbers set new, demanding goals for the production of military ICs at both merchant IC manufacturers and system developers. Achieving submicron dimensions was no longer a distant goal, oriented mostly to commercial memory requirements. Instead, it became a real target whose achievement would ensure a leading business position for those companies that reached it.

As a result, the VHSIC contractors built up their IC capabilities with investments estimated at double (or more) the VHSIC funding. For example, Honeywell invested about $300 million, nearly triple its total VHSIC contract funding. Even companies that did not have VHSIC contracts felt that they had to remain competitive and therefore also significantly increased the investment in their military IC capabilities.

It is our estimate that near—micron and submicron military ICs have become available to the designers of military systems three to five years earlier than would have happened without the VHSIC program. Military systems and equipment are now in development with these advanced ICs, or their direct derivatives, which give unprecedented performance, size, weight, power and reliability that could not have been achieved without VHSIC.

There are now over 40 programs in which VHSIC has been or is being designed into future products. In Honeywell alone, these include the Enhanced

Modular Signal Processor (the new Navy standard processor), the MK–50 Advanced Lightweight Torpedo, the Advanced Spaceborne Computer Module, the Multipurpose Space Computer, and upgrades to Milstar.

Impact on Technology

Besides meeting the main VHSIC goal of accelerating military IC capabilities by three to five years, other important capabilities emerged from the VHSIC program of significant importance to industry.

VHSIC Hardware Description Language (VHDL)

The development of VHDL is particularly notable. The VHDL portion of the VHSIC program was a far–sighted endeavor with an outstanding payoff. It is now possible to start an IC design at a functional system–level description, proceed into more and more detailed design levels and end up with a fully documented and well validated circuit layout ready for fabrication. This is all done under the control of a computer aided design (CAD) system. It significantly reduces the time and cost of the design by virtually eliminating the need for major redesign.

VHDL has been established by the IEEE and accepted by industry as a standard language for the description of ICs. It will reduce the cost of IC procurement by providing better documentation of design specifications. It will make second sourcing much easier, allow designers to mix and match ICs from different vendors in their designs, and alleviate the perennial problem of replacement of obsolete IC parts.

Multi–Chip Packaging

It has long been recognized that shrinking the feature sizes on the IC chip is not a complete solution to the need for increased electronic functionality. The IC chips themselves need to be more densely packaged in order to increase the speed of interchip data exchange and achieve further reductions in size and weight. The development of thin film multi–layer (TFML) multi–chip IC packaging under the VHSIC program was again a far–sighted development.

Interoperability Standards

The VHSIC program has helped in the establishment of standards for interfaces between chips on a board and between boards, and for test and maintenance buses. As these standards become broadly established and used in new designs, the circuits developed by different contractors will be able to operate together compatibly and built–in or self test becomes more practical and cost

effective. The VHSIC standards form the basic foundation of the common module developments which have become increasingly important in the design of military avionics systems.

Impact on Honeywell

The impact of VHSIC on Honeywell is probably similar to those of the other VHSIC contractors and can be viewed as a typical case history.

By 1980, Honeywell had established a major IC capability oriented mostly to internal needs. This was not unusual for companies with a major computer business. Special ICs were required and, before the advent of silicon foundry companies, total dependence on independent vendors for the development and delivery of the needed ICs was considered to be too risky. Some very specialized products were also needed and these could most easily be held as proprietary products with an internal facility. However, maintenance of such internal facilities were (and are) expensive and becoming more so as the IC technology rapidly changed.

When the VHSIC program was first announced, it was recognized that participation in the program would require a major change in the company's business strategy for ICs. Winning a VHSIC contract would mean operating under DoD specifications and restrictions and losing some proprietary advantage. On the other hand, it would accelerate the technology advances already under way in the company and would potentially provide a stronger and more responsive capability for its military business.

To respond to the VHSIC challenge, Honeywell formed a new program organization and a new plan for technology development was put in place. For example, a program on CAD (computer aided design) underway in one of the computer divisions was accelerated by nearly two years to meet the VHSIC program needs. Major corporate investments were made for both new equipment and facilities. People at all levels worked long and hard on the VHSIC program to make it a success.

One particular result was that Honeywell combined its new VHSIC technology with ongoing efforts on radiation hard ICs. This provided a new generation of radiation hard memories, gate arrays, and processors with outstanding performance, size, power, and reliability for space and strategic applications.

This, VHSIC created in Honeywell both a major new technology capability and a major new source of supply for military ICs. Without the VHSIC program, this capability would not exist.

Conclusions

The VHSIC program has had profound effects on military ICs, changing the industry and advancing the technology and product availability by several years. The full impact of the VHSIC program may not be seen for a few more years

during which the many systems now in development are deployed. The VHSIC program has had a positive and decisive role in making these systems possible.

Table 1.1 - Major Events, Milestones, and Highlights

1978
- o DoD letter of instruction to the three Services culminating the period of program concept discussions in DoD (July 19)
- o Program "kick-off" meeting in DoD, chaired by Mr. L. R. Weisberg; formation of Overview Committee and technical working committees for lithography, fabrication, and DAST (Design, Automation, Software, Test) (August 9)
- o Extensive organizational, policy, and technical meetings within the Government and with industry to define the program in detail (August 1978 - April 1979)

1979
- o Mr. L. W. Sumney appointed first VHSIC Program Director
- o New line items for $12M per Service established in FY80 budget (January)
- o Formulation of procurement procedures (February - March)
- o Commerce Business Daily Announcement #117, describing the VHSIC program (April 15)
- o RFP for Phase 0 - Program Definition issued (June 22)
- o RFP for Phase 3 issued (November)

1980
- o Phase 0 awards (9 contracts, $10.5M): (March)
  - Hughes, Rockwell, GE (Army)
  - TRW, IBM, Westinghouse (Navy)
  - T.I., Honeywell, Raytheon (Air Force)
- o Phase 3 contract awards (April - October)
- o Phase 1 RFP issued (September 10)
- o Phase 0 completed (December)

1981
- o Phase 1 contracts ($167M) started (May 1)
  - Hughes, T.I. (Army)
  - IBM, TRW (Navy)
  - Honeywell, Westinghouse (Air Force)
- o First Annual VHSIC Review and program kick-off meeting (June)

1982
- o Mr. E. D. Maynard, Jr. appointed VHSIC Program Director
- o Technology Insertion studies begun

1983
- o Fifteen weapon systems selected for Technology Insertion
- o First fully functional VHSIC chip - TRW Matrix Switch (February)
- o Nine contracts awarded for Submicron Program Definition
- o Yield Enhancement program defined
- o Manufacturing Technology program defined
- o VHSIC Hardware Description Language (VHDL) development began with one year program definition phase (July)

1984
- o Yield Enhancement modifications to Phase 1 contracts executed
- o Acoustic signal processor using VHSIC chip demonstrated by IBM (May)
- o Integrated Design Automation System procurement started
- o VHDL information released from ITAR control (January)
- o Phase 2 contract awards (November) to :
  - IBM (Army)
  - TRW (Navy)
  - Honeywell (Air Force)
- o Additional Technology Insertion candidates selected

1985
- o Yield Enhancement and Manufacturing Technology programs started
- o Information on Bus Interface Unit released from ITAR control (August)
- o Electrooptic Signal Processor brassboard demonstrated by Honeywell (September)
- o VHDL Support Environment information released from ITAR control (October)

1986
- o VHSIC TISSS information released from ITAR control (June)
- o First system demonstration of VHSIC technology: AN/ALQ-131 electronic warfare pod with TRW Phase 1 chips flight tested at Eglin AFB (July)
- o MIL-STD-1750A computer brassboard using VHSIC chips demonstrated by Texas Instruments (July)
- o Navy flight demonstration of IBM VHSIC Signal Conditioner for the AN/UYS-1 in a P-3 aircraft. (September)
- o AEBLE-150 electron beam lithography machine delivered to Motorola for use in the Phase 2 (October)
- o Demonstration of VHSIC chip set in the Enhanced Position Location and Reporting System by Hughes (December)
- o Twenty nine fully functional VHSIC chip types fabricated with total production of VHSIC chips over 100,000 (December)
- o Phase 2 contractors establish chip interoperability specification

1987
- o VHSIC version of the F-111 Digital Signal Transfer Unit demonstrated in flight
- o VHSIC chip packaging information released from ITAR control (March)
- o Navy AN/SRS-1 Combat D/F system with VHSIC chips demonstrated by Sanders Associates (September)
- o VHSIC circuit boards with Honeywell chips demonstrated in Navy AN/UYS-2 Enhanced Modular Signal Processor (September)
- o VHSIC automatic target tracking system with Hughes chips for the M1A1 tank demonstrated (December)
- o VHSIC Hardware Description Language (VHDL) adopted for industry wide design language as IEEE Standard 1076 (December 10)

1988
- o Dr. J. M. MacCallum appointed VHSIC Program Director
- o ADAS information released from ITAR control (March)
- o VHDL documentation mandated by DoD for all new systems (September)
- o Complex vector processor module for Advanced Tactical Fighter demonstrated by Westinghouse (November)
- o Demonstration of Phase 2 radiation hard 0.5 micron chips in an anti-submarine warfare beamformer brassboard by IBM (December)
- o Insertion of Phase 2 VHSIC technology into cruise missile advanced guidance unit begun by Honeywell and General Dynamics

1989
- o Demonstration of a fully functional CPUAX superchip designed by TRW and fabricated by Motorola; running at 12 MHz (December)

1990
- o General Dynamics demonstration of Honeywell Phase 2 chips in brassboard of cruise missile advanced guidance unit (scheduled for September)

CHAPTER 2 - THE VHSIC PROGRAM HISTORY, STRUCTURE, AND POLICIES

CHAPTER 2

THE VHSIC PROGRAM - HISTORY, STRUCTURE, AND POLICIES

Very High Speed Integrated Circuits (VHSIC) is the name of the program which the Department of Defense program conducted over a period of more than ten years beginning in March 1980. Over this period of time, the objective of the program was to develop two new generations of the silicon integrated circuits for use in DoD weapon systems.

This final report on VHSIC summarizes the background and origins of the program, its structure, and the contract efforts undertaken to accomplish the program objectives. It also covers the accomplishments made during this period, the activities of DoD laboratories in support of the contract efforts, and an assessment of the impact that VHSIC has had on the technology of the integrated circuit and its use in military equipments.

2.1 Program Origins and Objectives

The defense posture of the United States has been increasingly based upon the concept of a military force that is technologically superior to any potential adversary. We use advanced technology, particularly electronic technology, wherever possible to ensure our ability to defend against numerically greater forces. In any modern electronic system the silicon integrated circuit is the basic device for processing signals and it has become indispensable in the design of modern military weapons. The technology for making the device is a very demanding one. Complex and expensive equipments are required to produce it, advanced skills and knowledge are required to use it, and large continuing investments are required to keep it up-to-date.

During the 1960s, the DoD was the leading world force behind the development of integrated circuits (ICs). It supplied much of the research and development investment and accounted for over 70% of the user market in the United States. It was, therefore, able to maintain a comfortable lead in the military applications of ICs. During the 1970s, the commercial exploitations of this new technology grew very rapidly and resulted in a large expansion of commercial sales. By 1978, even though the DoD use of microcircuits had itself grown substantially, commercial applications represented more than 90% of the total integrated circuit market sales.

As a result, the IC manufacturers became oriented toward the large commercial market and less interested in supporting military requirements. Through law, regulation, and policy, the DoD's limited buying power was further diluted by fragmented purchasing patterns across the industry. The "comfortable lead" of the U.S. in the military applications of ICs began to erode.

The DoD, concerned about this change, spent several years carefully assessing its needs and deficiencies in this area of technology. The major deficiency perceived was that too often military microelectronic products did not incorporate the state of the art technology used in

commercial products. Advances in the semiconductor industry were not focused on military applications and most chips had to be separately qualified on low volume manufacturing lines to meet military specifications after their qualification for the commercial market. A gap resulted between the commercial introduction of advanced technologies and their use in military systems. Worse still, the delay was increasing with time. By 1980, this time lag had grown to 10 years or more for many DoD systems.

Using commercial products could not solve the problem because their performance did not generally meet military system needs, especially in the environmental areas of temperature and radiation. Compounding the problem was the fact that weapon systems were becoming increasingly dependent on electronic subsystems for their effectiveness, speed of response and adaptability to changing battle environments. There was also increasing evidence that Soviet weapons systems were beginning to use sophisticated integrated circuits.

Based on these considerations, the DoD decided to correct the deficiency by giving system developers and acquisition managers a military qualified microelectronics technology that was on par with the technology available commercially. It established the program called VHSIC, with the objective of being able to design, manufacture, and use silicon ICs in military systems with state-of-the-art fabrication technology, i.e. concurrently with commercial products.

After a number of discussions between Government and industry representatives, the technical goals of one-half micron feature size and 100 megahertz clocking frequency were chosen to quantify the desired product. IC chips combining these two characteristics would imply the ability to process electronic signal much more effectively than the technology current at that time. A figure of merit called the functional throughput rate (FTR) with units of gate-hertz/cm^2 was devised, which incorporated chip area, clock speed, and complexity (as measured by the number of electronic logic gates) into a set of desired attributes. One could thus characterize the suitability of IC chips for various applications.

At the same time, it was realized that these ambitious goals could only be reached after prolonged development efforts. Therefore, an additional "mid-term" goal of 1.25 micron feature size and 25 megahertz clock speed was chosen. This goal would be less difficult to meet but would still represent a significant advance in technical capability. It would also lessen the risk of the program and, if necessary, provide a decision point midway through the program on whether to proceed or not.

During the preparation of the VHSIC program plans, it was evident that many of the detailed technologies involved in IC design, fabrication, and use were sufficiently new that a supporting research and development effort in these areas was needed in order to reduce the risk of reaching the end goals. This supporting effort should also be separate and independent of the main line of development.

It was also clear from the start of the planning that the wide spectrum of capability in the U.S. semiconductor industry, and the equally wide technical approaches possible toward achieving the program goals, would make it impossible for the Government by itself to define the detailed tasks necessary to initiate a full scale development program. The DoD would need close interaction with industry in putting the program into action. It decided to do this by means of a concept definition phase in which many contractors would be funded to study

the problems posed by the VHSIC goals and to describe in detail their approach to solving them.

The following assessment of the impact that VHSIC has had on the semiconductor industry and the technologies used in it, has been contributed by the first Director of the DoD VHSIC Program Office. As such he had the initial responsibility for formulating and carrying out the plans for getting the program started.

The Legacy of VHSIC

Larry W. Sumney
President, Semiconductor Research Corporation
(Former Director, DoD VHSIC Program Office)

Introduction

Eight years have passed since my association with the VHSIC program. In these years, I have continued to work closely with the semiconductor industry of the U.S. but in an environment not dominated by the strictures of government. This permits easier decisions, more rapid implementation, and greater cooperation than is possible in Government programs such as VHSIC, and provides an excellent technology and management perspective for evaluation of the impacts, products, and lessons that constitute the legacy of VHSIC.

Quoting from an earlier description of the VHSIC program,[1]

"... the purpose of VHSIC is to apply a constructive bias to the direction of the defense technical establishment and to the semiconductor community so as to prepare them for a radically altered future, and to increase both the ability and desire of the industry to respond to the Nation's defense needs. In the process of achieving this larger goal, and in order to achieve it, specific VLSI chips will be made, demonstrated, and applied in current vital defense systems. In addition, DoD management innovations are being tested that will permit more productivity for generic research and technology investments."

By this goal, VHSIC can only be viewed as a success. Defense technology has been converted to the VLSI age and semiconductor manufacturers are very responsive to defense needs. Complex chips have been made and demonstrated, and management innovations have been applied successfully. As with most major

[1] Sumney, L.W., "VHSIC: A Status Report", IEEE Spectrum, pp. 34-39, December 1982

programs, the objectives were defined in different ways by different people. VHSIC certainly did not succeed in meeting every objective defined for it. It has even been criticized for not meeting objectives that were never defined. But for those objectives defined either contractually or in policy statements, the return on DoD's investment of funds and hard work has been gratifying and substantial. I will illustrate with some of the more important ones.

Industry Teaming

At the 1987 VHSIC Tech Fair, Dr. William Perry, a former Undersecretary of Defense for Research and Engineering, expressed disappointment that VHSIC had only partially succeeded in integrating the efforts of merchant semiconductor companies and defense system contractors. I take an opposite view. Inhibited by competition, the usual adversarial habits of U.S. companies, or perhaps by the legacy of anti–trust actions, U.S. companies have, for many years, had difficulty in identifying ways to work together constructively. The team building established as a requirement of VHSIC at first was forced but, under the severe demands of the program, developed into strong cooperative relationships. The demonstration that such cooperation can work in this country has made it easier to implement the cooperative endeavors required for U.S. industry to effectively compete in international markets and has provided the pattern for future teaming arrangements that are now very common. Of course, not every teaming relationship worked and perhaps not as many were even proposed as we would have liked, but even for those that did not work, I believe that better understandings developed and overall benefits have accrued.

VHDL

In 1980, as VHSIC was beginning, the cost of designing a silicon chip was between $100 and $200 per gate. The design of a 20,000 gate chip could entail an investment of over $2 million and require over 2 calendar years. These costs were prohibitive for the broad system applications contemplated by VHSIC planners. It was even suggested [2] that complexity was advancing to the point that design might become impossible and that design tools for VLSI did not exist. The reduction and simplification of complex chip design through the invention of automatic design tools became a major focus of the VHSIC contractors.

The VHSIC hardware description language (VHDL) is a major output of this design effort. It provides a common computer language which is applicable at various levels of design as well as in testing, specification, procurement, and logistics functions. VHDL has become an official IEEE standard (IEEE 1076) and is now a widely used standard for design.

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2 Robinson, A.L., "Are VLSI Microcircuits Too Hard To Design?", Science, Vol. 209, p. 258, 1980.

VHDL is just one of many advances in the design area that resulted from the VHSIC program. Today, design automation has advanced to where the cost per gate for some designs is under $1, a two order of magnitude reduction in cost making VHSIC chip design affordable. A significant portion, but by no means all, of this improvement is attributable directly to VHSIC. A major contribution to the U.S. microelectronics industry was made. Computer aided design remains one of the few strong assets of this vital U.S. industry.

Chips

Many chips were developed by the VHSIC contractors and probably just as many by companies who chose to develop their own VHSIC capabilities. Some of these are now being tested, applied, and integrated into systems. Others have not found application. Many VHSIC chips were developed by companies not funded by the program but who were spurred by VHSIC to develop their own competitive technologies. The results are a large standardized set of VLSI chips designed and available for application in military systems. Their actual insertion into military systems has not been rapid due to the endemic system development cycle for defense systems that takes ten years and is difficult to change. This is a larger challenge than the VHSIC program was designed to address.

To cite one example of an outstanding VHSIC chip, the "superchip" developed by TRW and Motorola in Phase 2 of the program was demonstrated in December 1989, as a proof of concept device at the very state of the art in either defense or commercial technology. It contains 4 million devices, is capable of 200 million 32–bit floating point operations per second, consists of 142 macrocells (each one as complex as a normal chip) that can be externally reconfigured, uses 0.5 micron CMOS technology, and is designed for use in advanced signal processing applications. The superchip is the first of the new generation of complex chips that will set the leading edge of the technology for the next generation of VLSI. It has created a challenge to which others will respond. It is a direct product of the VHSIC program.

Computers

At the 1989 IEEE Workstation Symposium, a desktop supercomputer was demonstrated by the Johns Hopkins Applied Physics Laboratory. Designed for applications in computer visualization and capable of over 1 million computations per second, it uses low cost chips in a parallel processing architecture and represents the current state of the art in workstation technology. It was developed using VHSIC technology almost exclusively and represents one of the first commercial applications of VHSIC technology.

Lithography

Lithography, the process by which microcircuit patterns are transferred from the design station to the silicon wafer, is perhaps the most critical of all semiconductor technologies because of its key role as the pacing technology. VHSIC led in the development of the vital electron—beam machine that writes the patterns on a mask and assisted in the development of the next generation optical steppers and X—ray machines that transfer the mask patterns onto the wafers. These tool development efforts have resulted in the continued availability of critical tools from U.S. manufacturers even as the U.S. industry's share of the world market for lithography tools has deteriorated badly. Each of these areas are now being addressed by SEMATECH. Without the VHSIC activities in lithography, there would most likely be no industrial base in this technology area for SEMATECH to support.

Commercial VLSI Technology

One of the principal reasons VHSIC was initiated was to leverage the significant advances of the U.S. commercial industry for military applications. During VHSIC's lifetime, however, our commercial industry stumbled as it faced international competition. So, although the impact of VHSIC on U.S. commercial integrated circuit manufacturers has been discounted because this was neither the intent nor the thrust of VHSIC, in fact, significant VHSIC resources were directed to merchant semiconductor manufacturers who found that the VHSIC goals reached beyond their commercial objectives. It caused them to accelerate the pace of their technology development. Several years before the VHSIC program started, it was widely believed that half—micron semiconductor technology would not become available before the turn of the century. Now, at least partially as a result of the acceleration of technology development by VHSIC and of the clear annunciation of VHSIC technology goals, the half—micron technology is on the verge of broad commercialization.

Conclusions

From the perspective I have, VHSIC is an outstanding success for which the DoD should take great credit. It has advanced both the defense and commercial technologies in the U.S. semiconductor industry, made design and fabrication tools available that would not have otherwise existed at this time, and accelerated IC developments in the U.S. industry. That it has not solved the major defense system development cycle challenge nor the competitiveness problems of the U.S. commercial semiconductor industry is not surprising. It was neither intended, directed, nor funded to do either. In the context of the actual intentions and goals of the DoD VHSIC Program, it has been an outstanding success.

2.2 Program Structure

The program structure that evolved from all of the technical and administrative factors that had to be considered initially included four major phases. At various later times, certain areas of activity in these phases became separately identified. The final resulting program structure is described below. Each program phase was carried out by contracts awarded competitively. For each contract, Appendix B lists the contractor, the contract title and number, and a reference to the final report if available.

The VHSIC program was structured to address the following general technical issues.

- ICs with greater functionality and higher speed would require a longer, more complex, and more costly design cycle.
- Greater functionality would require either larger area chips or smaller feature sizes (or both) in order to accommodate a larger number of transistors. This would result in longer chip development time and higher manufacturing costs.
- Military ICs had to meet stringent requirements for radiation hardness, low power consumption, and high reliability over a wide temperature range. As the complexity and size of the chips increased so did the difficulty in meeting these environmental conditions.
- High reliability, in turn, required the development and use of fault tolerant designs and built-in self-test (BIST) circuits in addition to a well disciplined design and manufacturing technology.

2.2.1 Phase 0 - Concept Definition

Phase 0 began in March 1980 as a nine month effort during which the contractors conducted intensive preliminary technical studies and then defined a detailed development program to accomplish the technical objectives set out by the VHSIC program office. The nine companies that participated in Phase 0 were General Electric, Honeywell, Hughes, IBM, Raytheon, Rockwell, Texas Instruments, TRW, and Westinghouse.

As guidance during the Phase 0 studies, the VHSIC Program Office required that the first phase of VHSIC technology meet certain minimum specifications which were chosen to be a reasonable compromise between the ultimately desired chip performance and the difficulties that were expected in developing the necessary technology. The desired performance was expressed as goals for the contractors to aim at. The specifications are shown in the table on the following page.

Phase 1 Chip Requirements

Functional throughput rate	$5x10^{11}$ gate-Hz/cm^2
Minimum feature size	1.25 microns
On-chip clock rate	25 MHz
Operating temperature	-55°C to +85° C, with operation from -55°C to +125°C as the goal
Radiation environment	10^4 rads(Si) total dose with $5x10^4$ rads(Si) as the goal, plus other radiation requirements recommended by the Defense Nuclear Agency
Failure rate	0.006%/1000 hour (goal)

Each of the Phase 0 contractors was required to provide information in the following areas.

- electronic subsystem candidates for possible implementation as VHSIC brassboards,
- identification of broadly applicable VHSIC chips required by the subsystem candidates,
- architecture of the required VHSIC chips and approaches to their design,
- chip fabrication technology and processing techniques needed to make VHSIC chips with 1.25 micron and submicron minimum features,
- definition of a packaging approach for both 1.25 micron and submicron chips,
- computer aided design (CAD) requirements,
- lithographic requirements for the fabrication of 1.25 micron and submicron devices,
- key processing equipment that needed to be developed,
- existing and/or any proposed facilities necessary to meet VHSIC design and fabrication requirements,

- o support environment, such as a higher order language for use in DoD systems, which would simplify the use of VHSIC,
- o approaches to providing increased reliability and testability of VHSIC devices,
- o procedure for making VHSIC products available for sale to all other DoD contractors and government laboratories,
- o procedure for making major equipment developed available to other DoD contractors and government laboratories, and
- o corporate strategy for rapidly introducing VHSIC into DoD systems.

The study programs were completed in December 1980. Based on the work during the Phase 0 contracts, each company submitted a proposal to the Government for Phase 1, emphasizing the development of 1.25 micron technology and a brassboard which would demonstrate the advantages of its application in systems. Final technical reports for each of the Phase 0 contracts are listed as References 2.1-2.9.

2.2.2 Phase 1

In May 1981, Phase 1 started with major emphasis on the development and pilot production of silicon chips with 1.25 micron minimum feature sizes, their demonstration in subsystem brassboards, and a minor exploratory effort on submicron technology. The two technical development efforts were separately designated as Phase 1a for the 1.25 micron technology development, and Phase 1b for the submicron technology feasibility study. The Phase 1 contracts were awarded to six major companies, or teams, with expertise in weapon systems development and semiconductor manufacturing. The contractors were Honeywell, Hughes Aircraft, IBM, Texas Instruments, TRW, and Westinghouse. The detailed contract requirements are given in Reference 2.10 and the final reports are References 2.11-2.15.

Phase 1a

The goal of Phase 1a was to develop the necessary processes, tools, and design environments for the production of 1.25 micron signal processing chip sets that would perform reliably in severe military environments, be affordable, and be usable in a wide variety of applications. This goal supported the key DoD objective of significantly reducing the delay in getting advanced semiconductor technology into fielded military systems. The technical requirements for the IC chips developed in Phase 1 were the same as those listed above for Phase 0 (Concept Definition).

Phase 1b

The goal of Phase 1b was to develop a 0.5 micron VHSIC technology and to fabricate test chips which demonstrated that the design and manufacture of VHSIC chips on a pilot production basis would be feasible during Phase 2. In attempting to meet 0.5 micron goals, all critical problems were to be identified and specific methods of approach for their solution were to be addressed. The technology developments needed in order to meet the VHSIC end goals of 10^{13} gate-Hz/cm^2 FTR with a minimum on-chip clock rate of 100 MHz were to be accomplished in Phase 1b.

In order to overcome the increasing limitations of conventional optical lithography of pattern features in the submicron range, a separate additional contract was awarded to Hughes Aircraft for the development of an electron beam lithography machine capable of patterning 0.5 micron circuits suitable for use in large scale manufacturing operations.

The specific tasks to which all of the Phase 1 contractors were committed were grouped into four principal areas and summarized as follows.

Chip technology and fabrication

- Develop a 1.25 micron baseline process to fabricate VHSIC circuits.
- Establish a pilot production line to supply the projected number of VHSIC chips needed.
- Supply chip packages which meet the military environmental conditions, as well as the performance requirements such as speed, input/output connections, and power dissipation.

Design, architecture, software, and test

- Develop an architectural approach and design methodology which supports the VHSIC performance requirements.
- Provide software development systems at a high order language level, preferably using Ada.
- Include provisions for on-chip self test and fault tolerance at the chip or module level.

- o Define the CAD tools needed to support the full spectrum of the design process from architectural specification to physical chip interconnection and layout.

- o Develop a simulation methodology to validate circuit, chip, and subsystem designs and to project performance accurately before fabrication.

Chip and subsystem design

- o Carry out a detailed system analysis to define the VHSIC subsystem design requirements.

- o Develop specifications for the VHSIC modules, chips, and functional macrocells.

- o Design and layout the VHSIC chips and modules needed for the brassboard, including provision for testability and fault tolerance.

- o Demonstrate the completed brassboard in simulated operational conditions.

Technology transfer

- o Provide an effective plan for making chips, design services, equipment, and software available to other DoD contractors.

- o Establish a plan for developing a second source of supply for chips.

- o Prepare a plan for insertion of the VHSIC technology into DoD systems.

2.2.3 Phase 1 Yield Enhancement

In order to demonstrate the advantages of VHSIC technology in technology insertion projects a substantial supply of chips was needed. Because new fabrication techniques were used in the VHSIC pilot lines, the chips initially produced on the lines were sufficiently expensive to discourage large scale use. The goal of the yield enhancement (YE) program was to ensure the supply and affordability of the VHSIC chips by increasing the pilot line production yield and by establishing a more disciplined production environment. The causes of low yield needed to be identified and corrected.

Industrial experience shows that the chip yield for a given process increases as the amount of product processed through the line increases. This is the "learning curve" phenomenon normally encountered in all production line systems. Therefore, a substantial amount of wafer processing was one of the requirements of the YE program. Progress in

achieving improved yield was measured by periodically starting the fabrication of three consecutive lots of wafers that were collectively called a Yield Verification Run (YVR). Each contractor had a goal for yield which the pilot line should achieve by the end of the program.

2.2.4 Phase 1 Technology Insertion

"Technology Insertion" is the term used to describe the application of the products developed under the VHSIC program to the design and acquisition of systems. Technology insertion constituted one of the basic goals of the VHSIC program. Since hardware insertion necessarily involves the linking of "high tech" with operational military systems, it was also one of the more difficult problems that confronted the VHSIC program managers.

The VHSIC program approach for meeting this challenge was to support a substantial number of system hardware insertion projects. The projects supported the use of VHSIC chips in both existing, fielded systems and others still under development. In cooperation with system program offices VHSIC co-funded both feasibility studies and hardware insertion into operating systems to demonstrate that VHSIC worked and that its use was beneficial. The benefits became manifest in different ways depending on the application --- increased performance, increased reliability, enhanced maintainability, reduced acquisition costs, less weight and space, or reduced life cycle costs. At least twenty-seven major system insertion efforts were undertaken in which the use of VHSIC technology demonstrated the potential for improved system performance. In some cases such as the Army's Firefinder radars and the joint Navy/Air Force HF/EHF communications terminal, the projected saving in system life cycle costs approached the total cost of the VHSIC program.

There were also a number of independent insertion programs in the systems applications area. They used the advanced VHSIC microelectronic hardware in system developments but, since they were not directly funded by the VHSIC Program Office, they are not described in this report.

Collectively, these VHSIC technology insertion efforts reflected the growing activity by DoD contractors and by the commercial electronics industry in introducing VHSIC products and technology into military systems.

2.2.5 Phase 2 Submicrometer Technology Development

The Phase 2 submicron goal was to develop a second generation of silicon chips characterized by 0.5 micron feature sizes and a clock frequency of 100 MHz. Phase 2 was preceded by another program definition study (Phase 0') similar to Phase 0, in which detailed approaches to the 0.5 micron goal were developed and proposed by nine contractor teams headed by Harris, Honeywell, Hughes, IBM, RCA, Texas Instruments, TRW, Westinghouse, and Western Electric.

The nine Phase 0' contractors finished their study programs in January 1984 and submitted proposals in response to the RFP issued for Phase 2. The final reports for Phase

0' are listed as References 2.16-2.24. The Phase 2 contracts were awarded in October 1984 to Honeywell, IBM, and TRW to begin the technology development and demonstration of the second VHSIC generation. This IC technology had to meet, among other requirements, the following specifications.

Feature size	0.5 micron
Functional throughput rate	10^{13} gate-Hz/cm^2
On-chip clock rate	100 MHz
Failure rate	0.006%/1000 hours
Radiation (total dose)	$5x10^4$ rad(Si)
Electromagnetic pulse	
Rise time	0.27 microseconds
Width	7.1 microseconds
Fall time	7.1 microseconds
Amplitude	500 volts
Source impedance	100 ohms
Built-in fault detection	>95% coverage single "stuck-at" faults
	>75% coverage CMOS "stuck-open" faults
Interoperability	PI bus and TM or ETM bus
	Electrical Interface Specification

The specific developments to which the contractors were committed in Phase 2 were grouped into five major task areas:

Process Technology

- o Process development
- o Materials
- o Lithography and resists
- o Modeling, scaling, simulation
- o Process test chips and test structures
- o Intermediate test vehicle
- o VHSIC chip fabrication
- o Pilot line
- o Chip manufacturing techniques

Packaging

- o Single chip
- o Multichip

- o Board/module packages

Design

- o Hierarchical design system
- o Design simulation and verification
- o Design methodology
- o Testability
- o Chip design and layout

Applications

- o Major brassboard
- o Chip definitions and brassboard module architecture
- o VHSIC chip design
- o Software development
- o Life cycle cost factors
- o Brassboard module fabrication

Technology transfer/business strategy

- o Interoperability standards
- o Availability
- o Second source
- o External demonstration

2.2.6 Phase 3 and Other Supporting Technologies

In addition to the primary chip development efforts in Phase 1 and Phase 2, the VHSIC program included other funded contracts for the development of supporting technologies. In contrast to Phases 1 and 2, which were large, comprehensive, multi-technology programs, these projects were more sharply focused on the areas of key technologies, equipment, and design tools needed to transform VHSIC technology into a readily usable industrial capability. These activities were collectively called Phase 3 of the VHSIC program.

The initial Phase 3 program consisted of 59 projects or tasks (early Phase 3), most of which began in 1980. They were carried out by 50 performing organizations which included both large and small industrial contractors, universities, research institutes, and three government laboratories. Additional contracts were awarded during the period 1982-1988 (late Phase 3). The technical categories covered by the projects included (1) architecture studies (devices and systems), (2) high resolution lithography, (3) design automation, (4) materials preparation and characterization, (5) device technology, (6) advanced packaging technology, (7) reliability, (8) radiation hardening, (9) testing, and (10) standardization. The more

significant results achieved in the Phase 3 projects are discussed in the pertinent sections of Chapter 3. Technical summaries of most of the early projects can be found in the VHSIC Briefs (Phase 3 Projects), References 2.25 and 2.26. Appendix B also lists separately the project titles, performing organizations, contract numbers and DTIC numbers of final reports for the early projects.

2.2.7 Design Automation

Because of the great complexity of the IC designs that were to be fabricated, it was realized in planning for the VHSIC program that design automation would be a critical element in its success. This indeed turned out to be an accurate forecast of the needs of the semiconductor industry. Accordingly, the Phase 1 tasks included varying efforts in the development and application of design automation tools. It was hoped that these tools would be used not only by the contractors that developed them but that the entire DoD community would begin to make use of these software packages. For several reasons, this did not happen. Chief among them were (1) the VHSIC tools for the most part did not comprise a complete set in themselves but rather were used in conjunction with other proprietary and commercial packages in each company, a mix that was changing continually and (2) users began to demand software of commercial quality that was adequately supported, maintained, and updated.

Prior to Phase 2, the Government planned the development of an integrated design automation system (IDAS) that would overcome the problems mentioned above. A Request For Proposals was issued and proposals were received and evaluated. However, during the evaluation phase it became increasingly evident that a program to develop a comprehensive set of design tools that would be useful at the many necessary levels of design, and to provide the sophisticated data bases and user interfaces that would be required, was not feasible at that time. The projected cost of such a program was beyond the funds available and the probability of developing the technology within the VHSIC program time schedule was very low. Furthermore, industrial activity in design automation was in a dynamic state and growing rapidly in response to diverse commercial design needs and to the rapid advances in the fabrication of large complex chips. It appeared very likely that commercial developments in the design automation area would be able to meet most of the needs of the entire chip design community, DoD as well as commercial.

A reassessment of the entire design automation area indicated that the VHSIC program would be better advised to focus attention on efforts that would meet specific DoD needs and which could be leveraged on commercial developments for maximum effectiveness. A Phase 1 subcontract from TRW with the Sperry Corporation to develop a multi-level design simulator had shown the feasibility of such a tool and gave renewed emphasis to the importance of a specific common language in which to express designs. Previously, a VHSIC-sponsored workshop in the summer of 1981 had produced a prototype specification for such a hardware description language (HDL). In July 1983, a contract was awarded to Intermetrics, with IBM and Texas Instruments as team members, to develop a VHSIC HDL language which became known as VHDL, plus a simulator and other associated tools. This activity, now

successfully concluded, has enabled the Government to exert enormous leverage by having VHDL established as an industry standard by the IEEE. After the development of VHDL was underway and its importance and utility recognized, other contracts were also funded to make use of it for efficient design, documentation and management of VHSIC hardware and software.

"VHSIC helped bring on the computer-aided design revolution, [and] accelerate the emergence of surface-mounted package technology and on-chip testability ..."

"What Did We Get From VHSIC", Electronics, June 1989, p.97

A second fruitful effort was the development of design automation at the systems level, an area in which there was practically nothing available at the start of the VHSIC program and in which DoD had critical needs. A number of contracts of this type were funded. One of the most successful was the Architectural Design and Assessment System (ADAS) developed by the Research Triangle Institute. This software system can be used to assess various hardware/software tradeoffs very early in the design stage of a data system and thus ensure greater responsiveness of a proposed design to system requirements. ADAS, along with several other VHSIC-sponsored system design developments have become fully supported commercial products.

2.2.8 VHSIC Manufacturing Technology Program - Joseph A. Key, Army LABCOM

The VHSIC manufacturing technology program (VHSIC-MT) was undertaken as a bridge between the Phase 1 and Phase 3 development programs and the production of chips and circuits to be used in military systems. It was intended to serve both those systems identified through the VHSIC Technology Insertion program and, subsequently, all systems utilizing VHSIC-like circuitry. The other major effort aimed at production capabilities was the Yield Enhancement Program described earlier. Both programs evolved from two joint Industry/DoD workshops on manufacturing technology problems conducted in 1981 and 1982, that identified and defined the improvements required to enable production of affordable chips and circuits in the quantities required for early utilization. One of the recommendations from the workshops was that the production program be divided into two parts: one concerning solution of specific problems being experienced on the pilot lines of the six Phase 1 contractors (Yield Enhancement), and the other concerning generic problems likely to be encountered by any manufacturer involved in VHSIC production (Manufacturing Technology).

The VHSIC-MT program was divided into the following four major technology categories or thrust areas and was supported mostly with funding external to the VHSIC budget.

Production and testing
Lithography
Materials and processes
Packaging

The manufacturing technology program was developed and coordinated as a VHSIC program with each Service taking responsibility for technologies in which it had particular expertise and interest. In the packaging area, the Army assumed responsibility for most of the first level interconnect and package production efforts; the Air Force established programs on production processes concerning second level packaging and attendant issues (packaged chip to printed wiring board); and the Navy developed third level interconnection technologies (printed wiring board or module to system), in addition to addressing some first level approaches not covered by the Army.

Most of the contractual programs began in 1985, for a nominal three year time period. The Air Force developed an integrated, comprehensive packaging effort which was started in 1986 and was composed of three concurrent technology tasks followed by an integration task.

2.3 Program Management

The DoD recognized that the VHSIC program had to address both technical and management problems. The primary technical task would be to develop the technology to design and manufacture military specific ICs. At the same time, there were problems involving the management of the requirements of each of the Services, the transition from development of the technology to its insertion in systems, and providing a level of data security and control that would prevent compromise of the program and its goals. In 1978, the DoD adopted a management plan which would:

- establish the VHSIC Program Office within the Office of the Secretary of Defense supported by similar offices in the Army, Navy, and Air Force,

- develop an industrial contracting program for two new generations of advanced integrated circuits specifically designed to meet military system needs and provide the capability to support long term use of the circuits,

- o initiate an aggressive program to insert this technology into systems in such a way that it would minimize the financial and schedule risks to the weapon system developer,

- o provide leadership and guidance for the semiconductor industry to develop a VHSIC production capability that would continue to meet specific military needs while complementing the commercial goals of semiconductor manufacturers,

- o operate the program under the International Traffic in Arms Regulations (ITAR) to ensure adequate security control.

The VHSIC Program Office was established in the Office of the Under Secretary of Defense for Research and Engineering whose functions have since become part of the Office of the Under Secretary of Defense for Acquisition. In order to ensure the widest possible dissemination to the three Services of information and data about the technology as it was being developed by the contractors and to promote the early insertion of the technology into the various weapons systems of the Services, it was decided from the outset to make VHSIC a truly joint Tri-service program. Accordingly, the VHSIC Program Director was assisted by Program Directors from each of the Services. All the development contracts were let through the Services and each of the Service Program Directors was directly responsible for the administrative and technical management of the contracts in that Service.

Under the management of the VHSIC Program Office, current information about the program was made readily available to the entire DoD community. This was done by conducting frequent, periodic tri-Service reviews of each major development contract. Each of the Services sent technical managers and specialists to these reviews which were attended by as many as 75 DoD representatives. Annual VHSIC Conferences were held in the years 1982-1989. At these conferences, all of the VHSIC program activities and results were presented to industry and Government representatives, with emphasis directed toward system application of VHSIC technology. The VHSIC Program Office also published, for unlimited public distribution, Annual Reports of the VHSIC Program in 1986, 1987, and 1988 (References 2.27-2.29). Technical specialists held workshops on specific topics, and over 35 advanced training sessions on how to use VHSIC technology were conducted over the period 1984 through 1988. Joint Service committees were established to develop standards in appropriate areas. In the case of VHDL (the VHSIC Hardware Description Language), VHSIC program personnel supported and finally secured its adoption as a world wide IEEE standard. (See, e.g., Sections 3.1.3, 6.2, and 6.3.)

A steady transfer of VHSIC information and products took place to weapon system developers and to the IC industry at large. In response to the technical impetus established by the VHSIC contract programs and to the needs of the DoD of which VHSIC made them aware, many companies outside of the VHSIC funded efforts have developed design and manufacturing facilities for the production of VHSIC chips. (see Chapter 7).

During the course of the program, various policy directives were issued by OUSD as well as the Service Secretaries to encourage the adoption of VHSIC technology, to modify existing MIL-STDs and to promulgate new ones as required. See References 2.30 and 2.31.

2.4 Funding

A roadmap of the relation between the various portions of the VHSIC program and the funding allocated to each of the various parts is shown in Figure 2.1 and Table 2.1. A chart of the funding profiles over the ten year program period is shown in Chapter 1, Figure 1.2.

2.5 Security - James J. Hower: Eagle Research Group, Inc.

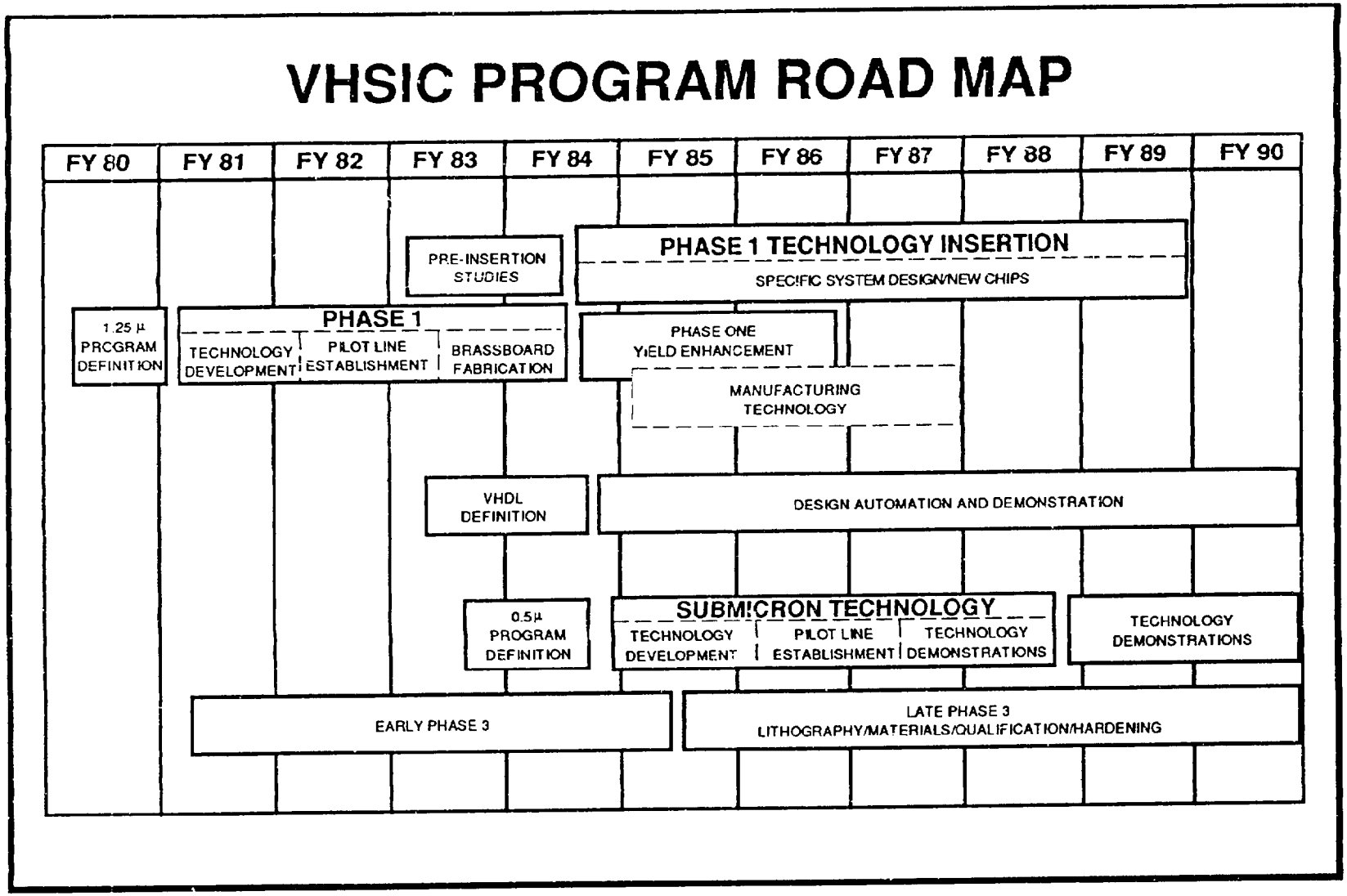
2.5.1 History of VHSIC Security Measures

In the late 1970s and early 1980s, when the VHSIC program was first formulated, intelligence reports were warning of the erosion of the U.S. technological lead over the Soviets. One of the primary reasons given for the erosion of our technological advantage was the "hemorrhaging of U.S. technology" to the Soviet Union via both legal and illegal means. Congress was in the process of passing a new Export Administration Act which would mandate the development of the Military Critical Technologies List (MCTL), because members of the Congress and the Defense Department considered the licensing system of the Department of Commerce Export Administration Regulations (EAR) to be inadequate for properly protecting critical technology. It was thought that critical technology could better be controlled by the State Department under the International Traffic in Arms Regulations (ITAR).

As a result of these considerations, the House and Senate Conference Report for the 1980 Defense budget, which authorized the initial funding for the VHSIC program, stated:

> *"The export of the technology developed in this (VHSIC) program would be controlled where applicable by the ITAR until the state-of-the-art for such technology progresses to the point where national security permits its transfer to other controls for export".*

This statement was significant not just because it was the first time that the control structure for a technology development was specifically mandated by Congress, but more importantly because it represented a departure from the existing control structure for microelectronics in general. Only those devices specifically designed for military application had previously been controlled by the ITAR. All dual-use or general purpose devices, even those built to military specifications, were controlled under the EAR. Moreover, all



VHSIC

Figure 2.1 VHSIC Program Roadmap

Table 2.1 - VHSIC Funding

	FY80	FY81	FY82	FY83	FY84	FY85	FY86	FY87	FY88	FY89	FY90	TOTAL
Phase 0	10.51											10.51
Phase 1		32.50	69.60	46.60	18.07							166.77
Yield Enhance					44.15	34.00	22.70					100.85
Techn. Insert				4.30	24.77	38.89	61.34	26.12	10.60	3.34		169.36
Design Automat				1.10	6.36	7.25	11.26	17.13	10.96	7.41		61.47
Phase 2-Def'n.				3.00	8.23							11.23
Phase 2-Submicron					1.39	33.73	46.44	48.14	43.76	21.66		195.12
Phase 3-Early	16.40	6.00	6.00	6.10	1.52	0.27	0.04					36.33
Phase 3-Later				0.40	8.12	10.96	18.00	23.14	17.76	7.14		85.52
Indust. Base							0.70	0.65	2.00	1.00		4.35
Manage/Support	1.50	3.00	4.00	4.50	5.18	5.55	5.90	5.57	4.46	3.58		43.24
Other						0.73	32.77					33.50
TOTAL	28.41	41.50	79.60	66.00	117.79	131.38	199.15	120.75	89.54	44.13		918.25

production equipment for dual-use and military devices was, and still is, subject to EAR control.

One of the first actions of the VHSIC Program Office (VPO) to comply with the Congressional mandate was to draft a change to the ITAR that would bring VHSIC devices under ITAR control. The proposed entry, which was to be added to Category XI, was forwarded to the Department of State by the Under Secretary of Defense for Policy (referred to hereafter as Policy) in December 1981. This entry read as follows:

> *"(d) Very High Speed Integrated Circuit (VHSIC) semi-conductor devices that are specifically designed for military applications and which have a high-speed signal and image processing capability with an operational parameter greater than 10^{11} gate-hertz/cm^2 for an individual semiconductor device."*

This entry was officially included in the revision of the ITAR which was published in December of 1984.

In 1984, there was a disagreement within the DoD over how to implement the Congressional mandate regarding the security controls for VHSIC. The technical side represented by the Under Secretary of Defense for Research and Engineering (R&E) generally favored minimum controls in order to foster technology transfer within the U.S. and with close allies, while Policy recommended that the appropriate response to the Congressional mandate was to classify the entire VHSIC program. While this action would ensure program security, R&E felt that it would create serious problems for the program managers in both the DoD and industry, as well as drive the program costs up sharply. For these reasons the VHSIC Program Office (VPO) considered it to be unacceptable. This classification issue therefore became an area of major disagreement within the OSD.

Efforts to reach agreement on the classification issue and other VHSIC security measures continued within Defense without a consensus. As the discussions became protracted over an excessive period of time, Policy submitted its position to the Secretary of Defense for approval. By this time, the Secretary of Defense had given primary responsibility for all export control and technology transfer issues to Policy. The Secretary approved the Policy position, and promulgated VHSIC security guidelines. While Policy set about to implement the guidelines, R&E and some industry representatives advised the Secretary of the negative impact of these security guidelines. In an effort to make this more workable, the VPO prepared and submitted a VHSIC Classification Instruction (DODI 5210.75). Under this Instruction, a VHSIC device would derive its classification from the system in which it was used. The combination of this guideline coupled with industry pressure from the highest levels finally convinced Policy to agree to investigate and consider the use of industrial practices to protect VHSIC technology.

While a VHSIC contractor panel was established to develop alternatives to classification, Policy and R&E drafted a joint memorandum initiating a certification

requirement for VHSIC-related contractors. The International Technology Transfer (IT^2) subpanel was directed to further evaluate VHSIC controls.

In an unrelated action, DOD Directive 5230.25, "Withholding of Unclassified Technical Data From Public Disclosure", went into effect. This Directive is based on 10 USC Section 140c, as added by P.L. 98-94, "Department of Defense Authorization Act, 1984", which allows unclassified technical data under the control of a Defense element to be withheld from release to the public if it contains critical technology related to military or space applications. Certification procedures for contractors were included.

A second Directive, DODD 5230.24, "Distribution Statements on Technical Documents", went into effect at approximately the same time. This Directive provided guidance regarding the marking of documents restricted from public release under DODD 5230.25. The VHSIC Program Office directed that all VHSIC documents restricted by DODD 5230.25 would be marked with Distribution Statement X in order to ensure maximum possible availability to Defense contractors.

During the ensuing months, the VPO and its Policy counterparts in Defense Technology Security Administration (DTSA) attempted to reach agreement on a VHSIC Technology Security Instruction. DTSA had submitted the proposed alternative of the industry panel for review by the Industrial Security Office within Defense. The industry document was rewritten by the Industrial Security Office into appropriate control language. The resulting Instruction, DODI 5230.26, "Very High Speed Integrated Circuit (VHSIC) Technology Security Program", imposed controls on unclassified information that were parallel to those required to protect classified information. A far more sophisticated certification procedure than was required by 5230.25 was also included. In spite of numerous negative comments, this Instruction, dated March 17, 1986, was officially released in April 1986.

The VPO directed the VHSIC Program Managers to comply with this Instruction and took the necessary action to have the requirements of this Instruction included as an interim rule in the DFAR. Nonetheless, few Defense contracts involving VHSIC were written or modified in accordance with this Instruction.

With the Security Instruction in place, attention was turned to the development of a VHSIC export policy. The VPO prepared and submitted a series of release matrices emphasizing sharing with our allies for Policy consideration. In June of 1986, agreement was reached and Policy drafted the export policy, based on the release matrix. DTSA forwarded the first draft to the VPO in October 1986. A final coordinated VHSIC export policy was issued on October 13, 1987.

A related security problem during the latter part of 1988 was the development of an export policy for radiation hardened devices. The VPO was instrumental in quickly developing a policy on such devices that was acceptable to both industry and Government. This policy document was promulgated by DTSA in April 1989.

During 1989 and 1990, the VPO worked with DTSA toward the cancellation of DODI 5230.26, subject to modification of DODD 5230.25 to include specific reference to VHSIC technology.

2.5.2 Additional Security Decisions

VHSIC was not just a program restricted to a few Defense contractors. It was the hope and intent of the Congress and the VPO to recognize and encourage industry-wide participation. Products from every company that was able to design and produce devices that met VHSIC specifications were in fact tested, verified, and subsequently qualified for VHSIC insertion initiatives.

In the course of the program, it was periodically necessary for the VPO to provide specific policy on security regarding some element of the overall program. A summary of the key determinations regarding VHSIC technology are listed below.

Date	Subject or Action
February 1981	Briefing of all program participants on ITAR controls
January 23, 1984	Release from ITAR control of VHSIC Hardware Description Language (VHDL) information
March 8, 1984	Release from ITAR control of VHSIC chip packaging information
August 5, 1985	Release from ITAR control of BIU data
October 15, 1985	Release from ITAR control of VHDL support environment information
June 15, 1986	Release from ITAR control of VHSIC TISSS information
June 21, 1987	Definition of what constitutes a VHSIC device
December 8, 1987	Release from ITAR control of VHSIC chip packaging information
March 10, 1988	Public release of ADAS information

By the end of the program the VPO no longer considered it necessary or appropriate to single out "VHSIC" devices for special control. The diffusion of the technology throughout the industry and the availability of comparable technology in Europe and the western Pacific had met the terms of the Congressional mandate for release from ITAR control. Consideration was given to generalizing the ITAR entry to read "electronic devices specifically

designed for military application" and deleting the gate-hertz/cm^2 performance parameter referenced in the ITAR. The VPO supported the authorization of devices developed under VHSIC for use in commercial applications. Under this situation the result would be that a "VHSIC" device used commercially would be properly identified as a "dual-use" device and then be subject to the same EAR control as any other commercial VLSI device.

CHAPTER 3 - DEVELOPMENT TASKS

CHAPTER 3

DEVELOPMENT TASKS

The goals for VHSIC chip production were symbolized by the values of their minimum feature size --- 1.25 micron for Phase 1 and 0.5 micron for Phase 2. However, the complete specifications for VHSIC chips set limits for many other parameters such as functional throughput rate, radiation hardness, reliability, and temperature environment (see Chapter 2 for Phase 1 and Phase 2 requirements). In addition, the program called for a variety of important but less well defined requirements. Interoperability of VHSIC chips was needed between themselves and with other chips and electronic subsystems. Design methodologies were desired which were more fully automated and which included built-in (i.e. on-chip) testing. Packages for chips of these sizes, speed, and I/O count did not exist. New procedures would have to be devised for testing and qualifying the chips for military use. If procurement for production systems was expected, then second sources had to be developed.

Work in all of these areas of hardware and software technology became the development tasks that occupied the VHSIC contractors and the VHSIC Program Office for the duration of the program.

This chapter describes in considerable detail the activities and the results of the development efforts down to the level of individual contracts. Further details are provided in the references that are listed in each section. For readers not needing this level of detail, the introductory paragraphs at the beginning of each numbered section provide a summary or discussion of the relevant issues.

3.1 Design

Although it was evident at the start of VHSIC that chip design and fabrication capability were equally important to the final success of the program, it was not clear which particular design activities should be supported by the Government. Obviously, the functional design had to be included, but were there generic features critical for DoD applications that had to be part of all designs? Were there design standards that should be implemented in order to ensure manufacturability at reasonable cost, reliability, and adequate life cycle support? Were existing design tools capable of doing the job?

The direction of the design effort evolved during the course of the program. During Phase 1, stress was placed on design-for-test to ensure that fabricated chips worked reliably and that they performed the functions for which they had been designed. In addition, design tool development was supported.

In the Phase 2 period, it was realized that Government supported standards development (rather than tool improvement) were activities that could have great industry-wide impact while at the same time meeting specific DoD needs. In the case of a hardware description language, the VHSIC program not only created a standard (VHDL) but also demonstrated its use with a simulator and associated tools. Similarly, standards for the

interoperability of the Phase 2 chips were developed and used in their design. Greater emphasis was also placed on the interactions between the design of individual chips and the overall system specification and operation.

The following assessment of the impact of VHSIC on the procedures and tools for system level design has been included because it emphasizes the significant conceptual changes in approach that VHSIC promoted in its design automation developments.

The Impact of VHSIC on System Level Design

Robert M. Rolfe
Institute for Defense Analyses

Introduction

The advent of the VHSIC program focused attention on the concept of "a system on a chip" and thereby brought to the forefront the following problems that until then had not been adequately addressed by chip designers.

- Making full use of the tremendous number of transistors (or gates) available to the designer in a VHSIC microcircuit can lead to lengthy design time and very high design cost.
- The high cost of large, complex, application specific chips makes any incremental change to older systems expensive and therefore discouraging unless significant needed system capabilities are added.
- Quality assurance and testing of the chip are no longer independent of the system integration process but must now involve system level specifications.
- System design requirements for software, maintenance, and life cycle reliability must also now be considered at the chip level.

These problems argue that the design of the chip architecture must incorporate the necessary test strategy to remove latent manufacturing defects as well as a test strategy for design verification to remove latent design defects. One can ask how one provides a design that is capable of identifying manufacturing defects in a structure containing millions of interconnects and active elements through an interface with only a few hundred electrical signal ports (namely, the chip periphery pads).

The VHSIC Hardware Description Language (VHDL), described in detail in Section 3.1.3, is the hub around which many specific tools have been created to address these problems. It supports model–based specifications which can be used for simulation and other analyses.

A comprehensive implementation of the IC design process must consider a host of specific issues if it is to be effective in meeting functional and physical requirements that will surely get even more complex and more difficult in the future. Several of the most important are discussed below.

Design Methodology

Hardware/Software Trade–Off Analyses

One of the first issues that must be resolved in a complex system design is the allocation of various system functions between hardware and software. Premature binding of the system architecture to a specific solution may decrease system performance, adaptability, and maintainability. Incorrect allocation of system functions to hardware or software will delay system development and age the design solution unnecessarily. Under the VHSIC program several software tools were developed to support analyses of proposed allocations. ADAS (the Architectural Design and Assessment System) and the JRS Automated VHDL/ Microcode Compiler, described in Section 3.1.4 address these issues. ADAS provides a capability not only to analyze but also to refine the system architecture while the JRS tool provides a path to reusable macrocells of a silicon compiler leading to actual layout of the chip. The latter capabilities can greatly increase design efficiency and quality since the silicon compiler macrocells will have been prechecked for functional accuracy.

Information Reuse

The VHSIC software products enable reuse of engineering information reuse during and after the process of designing the system. These products include VHDL and its descriptions of standard component models and test program sets. Engineering information reuse in a controlled process enhances concurrency of the system design process which shortens the design time while providing higher quality. VHSIC has also developed a specification framework for engineering information systems (EIS) to support access to shared information for tools and users. EIS is discussed below.

Product and Process Qualification

Using qualification or acceptance tests of a product chip after the manufacturing process to provide quality assurance ignores the tremendous impact of early engineering design decisions on the product quality and maintainability that is ultimately achievable. Qualification of the design as well as the manufacturing process reduces qualification costs when amortized over a quantity of products and product types produced through the qualified processes and, at the same time, it increases the product quality. The VHSIC program focused on development and

manufacturing process qualification with the Qualified Manufacturing Lines (QML) concept (Section 3.2.3). This concept has the potential for not only reducing "red tape" but also for ultimately improving product quality by not constraining design and manufacturing process solutions. It shifts the focus to pre–assured design and manufacturing quality versus "tested–in" quality.

Built–in Test and Maintenance

System test and maintenance have become one of the most important issues when designing highly complex systems comprised of highly complex chips. In contrast to other issues where the correct design methodology allows many different possible implementations, test and maintenance require standardization by specification at the hardware interface level to permit chips designed by different organizations and at different times to be used together in systems. The VHSIC program has developed a number of new system architectural features to facilitate the integration of complex chips into systems and to provide for their test and maintenance. (For details see Sections 3.1.1)

The standard for a powerful, general purpose backplane bus, the PI bus, has been developed by VHSIC for data communications across local backplanes. This standard is being used for the most recent tactical aircraft avionics programs.

Built–in test technology was mandated as part of the original VHSIC requirements, and the contractors have developed a number of enhanced techniques to accomplish it. Examples include level sensitive scan design (LSSD) and other scan design techniques to fully automate detail tests of the chip structure used in manufacturing and maintenance.

The architecture and specification for a test and maintenance (TM) bus were developed by VHSIC to support built–in test (BIT) for electronic subsystems. The BIT architecture integrates the built–in element test and maintenance (ETM) bus of a single VHSIC microcircuit with the subsystem TM bus. VHSIC–based electronic subsystems which use these integrated test buses can be expected to be self–diagnosing for most of the anticipated fault modes. This self–diagnosis includes identification to the faulty component even in a two level maintenance strategy.

Computer Aided Test

The VHSIC program has developed an approach to a methodology for testing VHSIC class microcircuits. The essential element of this approach is to develop and validate a language which allows the capture of the product and test specifications which, in turn, are linked to a set of standard test methods (e.g. MIL–STD–883) for VHSIC class microcircuits. By separating product and test specifications from the implementation of test programs, VHSIC developed test standards that enable innovative computer aided test tools and extensive reuse of product descriptions over the product life cycle.

This capability was demonstrated in the VHSIC Tester Independent Support Software System (TISSS) discussed in Section 3.2.2. An extension to the TISSS, the Line Replaceable Module (LRM), is currently being developed for the Advanced Tactical Fighter (ATF) and the Joint Integrated Avionics Working Group (JIAWG). The JIAWG goal is to use simulatable product and test specifications for common modules across DoD weapons platforms.

Engineering Information Management

Any design as complex as a VHSIC based microcircuit system requires large design teams with concurrent access to product description information over the development cycle. The VHSIC Engineering Information System (EIS) has addressed this need by defining a generic set of standards for computer aided engineering and design environments (Section 3.1.4). The basic EIS provides life cycle support of any well described product and has demonstrated this for design and layout information modeling.

Standards and Practices

The VHSIC program has had a strong impact on commercial electrical product standards activities within the IEEE and the Electronics Industry Association (EIA). VHSIC provided strawman standards for the Design Automation Standards Subcommittee of the IEEE including IEEE 1076 VHDL and IEEE WAVES (Waveform and Vector Exchange Specification). The VHSIC Phase 2 test and measurement bus (TM bus) was provided to the IEEE test bus standards committee. The EIA has drafted standards to use the IEEE VHDL for the specification of digital products and set out to develop guidelines for use of VHDL for the specification of standard industrial components. If approved, this guideline will become EIA 567.

The IEEE 1076 VHDL standard has been accepted for use in the commercial CAD industry even faster than in DoD (see the contributed paper in Section 7.2). Major commercial system developers have adopted it, and the marketplace now has a growing base of available computer aided engineering vendors supplying IEEE 1076 VHDL products.

The VHSIC program advanced the concept of virtual test of products based on simulatable specifications and designs. This fact not only shortens design intervals, but effectively removes a large category of latent design defects before prototype or breadboard fabrication. The feasibility shown by the VHDL simulator built as part of the VHDL contract with Intermetrics encouraged the CAE industry to develop system level and design phase simulators. Today, many commercial simulators are available for the VHSIC developed VHDL. Some of these simulators will even allow detailed VHDL descriptions of complete processing systems to host software development before the physical prototype is available. This capability enables design teams to practice concurrent engineering for software on custom hardware platforms.

The following are some specific activities in standards and practices that have taken place both in industry and in the Department of Defense.

- The Design Automation Standards Subcommittee of the IEEE has recently indicated it will develop a product and test specification language standard with strawman input initially derived from the VHSIC TISSS. Use of this strawman language already has demonstrated large engineering productivity improvements in the development of VHSIC qualification test programs.

- The Computer Aided Acquisition and Logistics System (CALS) specification references the IEEE 1076 VHDL for digital electronic products behavior description in MIL–STD–1840. IEEE 1076 VHDL is the only standard language for hardware behavior functionality. CALS delivery of VHDL electronic product descriptions that emulate product behavior and interface specifications will be exploited for many decades.

- The VHSIC program has developed a standard data item description (DID) by which procurement contracts in the DoD can define the electronic media delivery of hardware descriptions. MIL–STD–454 was extended to include VHDL and TISSS descriptions for microcircuits that must conform to DoD Requirement 64.

- The VHSIC TISSS product and test specification model is to be extended by the ATF program to support the full scale development (FSD) acquisition statement of work (SOW) by specifying requirements for delivery of simulatable specifications. The USAF Modular Avionics Support Architecture (MASA) plans to adopt tailored versions of the JIAWG simulatable specification requirements.

- Specifications of digital subsystems for reprocurement should be greatly improved by the VHSIC developed product and test specification and hardware description standards. Reprocurement is a critical issue in the DoD for long lived, routinely operated, space systems and complex weapons platforms.

- The ASCM (Advanced Spaceborne Computer Module) follow–on to the GVSC (Generic VHSIC Spaceborne Computer) is to be a standard module, consisting of many subassemblies, for spaceborne processing. The GVSC program beta tested the VHSIC TISSS standards for product and test specification standards.

Long Term Systems Design Issues

The VHSIC program has identified opportunities to improve design of systems in the future. In particular, the EIS has identified the need to develop

better information modeling concepts, methods, and tools. Although the integration of product data across the organization has been addressed for well cooperating engineering information systems, weakly coupled systems under autonomous control still pose an important challenge; most of our existing operational and maintenance support systems operate in this manner.

The VHSIC program has made great strides in built—in test (BIT) for digital microcircuits and tightly coupled subsystems, yet much effort must be made to fully integrate test architecture across systems. Accurate BIT remains a problem because VHSIC BIT solves the problem for only a small spectrum of electronic and mechanical systems.

Powerful BIT architectures create the need for significantly advanced automatic test pattern generation (ATPG) tools for manufacturing and product support. The ATPG tools have hardly kept pace with system design tool progress. VHSIC has attempted to address this with standard test architectures, test interfaces, and product description languages. Yet, much work remains in developing product description models that allow system designers to describe test architecture for the full spectrum of electronic and mechanical technologies used in a modern weapon system.

3.1.1 Built-In Test/ Built-In Self Test (BIT/BIST)

Complex digital systems consist of a hierarchy of chips, cards, and racks. At each level, tests must be performed to ensure that components work reliably in accordance with their design specifications and are free of any logic errors and timing problems. In addition to tests of this structural organization, tests must also be performed at different times during the life cycle of the various components: after manufacturing, at system start-up, and during on-line or off-line operation.

In order to meet these diverse testing requirements, special hardware must be incorporated into chip and card designs to render the components testable down to levels at which faults can be isolated (Built-In Test). For a chip, this is the gate level. The techniques for producing such testable designs requires a comprehensive implementation methodology usually referred to as design-for-test (DFT). While Built-In Test requires external test vectors, components with Built-In Self Test capability can generate their own test vectors and report their status to the outside world. Such capability is important for quick response, on-line operation testing, or to decide whether redundant elements are needed to be activated in fault tolerant designs.

During Phase 1, design techniques were developed, documented, and demonstrated which provided increased reliability and testability of chip performance through the inclusion of on-chip testing and fault tolerant designs. The details are to be found in References 2.11-2.15. Phase 2 extended this work to encompass standards for chip-to-chip and card-to-card communication (Section 3.1.2). TRW used BIST to improve fabrication yield on its

"superchip" to acceptable levels by connecting enough working macrocells together to form a functional chip. The Phase 2 work is described below.

Honeywell

The Honeywell approach to BIT/BIST was to include presettable sequential "flip-flops" (FFs) in all chip designs in such a way that all combinational logic and sequential element portions of the circuit would be testable. Loading a value to one FF causes the propagation of that value to another FF where the value can be captured and scanned out. This technique is very similar to IBM's level sensitive scan design (LSSD) technique and became the basis of Honeywell's standard design-for-test procedure.

To ensure defect free components and boards, Honeywell included both internal and boundary scan in its Phase 2 chips. With internal scan, all of the normal functional flip-flops within the design are replaced with scannable registers, i.e. registers whose setting can be sensed. Serial access to the internal registers, combined with computer generated test patterns, gave greater than 98% coverage of single stuck-at faults within the components. To implement boundary scan, scannable flip-flops were placed at each I/O pin to allow direct serial access to the chip I/O. This boundary scan approach, visible only during board test, provided thorough testing of interchip connections at the board level.

To meet the need for high coverage self-test, Honeywell implemented two approaches to pseudo-random self-test. The primary approach was to replace all registers in the design with registers known as Built-In Logic Block Observers (BILBOs) which support normal functional mode, test reset, test serial shift, parallel pseudo-random test pattern generation, and parallel signature analysis. By using BILBO registers throughout the design, parallel test patterns can be applied to the chip at full chip speed. In addition to this parallel approach, serially loaded pseudo-random test patterns are also supported to allow a cost/coverage comparison of these two approaches.

Honeywell chips included the element test and maintenance (ETM) bus (the chip level test bus) as the standard interface to the BIT circuitry to allow either pseudo-random pattern generation on the chip or deterministic patterns to be scanned in. Pseudo-random techniques allow high fault coverage testing of the internal circuitry of an IC.

A hierarchical maintenance system was designed with two levels of test interface, a chip level interface (ETM-bus) and a backplane or board level test maintenance interface (TM-Bus). Individual Honeywell chips include an ETM interface. They can be connected to a Honeywell Test Interface Unit (TIU) for communication of chip test information to a system test controller. The TIU device was fabricated, packaged, tested, and documented in VHDL. An applications board will be developed as a VHSIC add-on task. The TIUs connected to the TM-Bus can provide the system test controller with diagnostic information.

IBM

The IBM design methodology for built-in test was to use level sensitive scan design (LSSD) coupled to the standard ETM bus interface. LSSD ensures that all sequential elements can be set to arbitrary values from an external interface. This allows the complexity of the test generation to be reduced to that for a combinational circuit. The LSSD latches can be set to known values with external test vectors or by using internal linear feedback shift registers to generate pseudo-random patterns for built-in self-test. Pseudo-random patterns generated on chip can transfer data to the LSSD latches at a much higher rate than patterns externally scanned in. BIST stuck-at fault coverage was 59.4% for the AC chip, 90% for the CSR chip, 54.6% for the SP chip, and 78% for the VBIU chip. For IBM, BIST can test only that logic bounded on both sides by an LSSD latch so that the logic between the LSSD latches and the I/O pins remains untested. This is tested by a "boundary scan" procedure that supplements the BIST. These two test procedures used together produced a combined fault coverage of greater than 97% for all chip types.

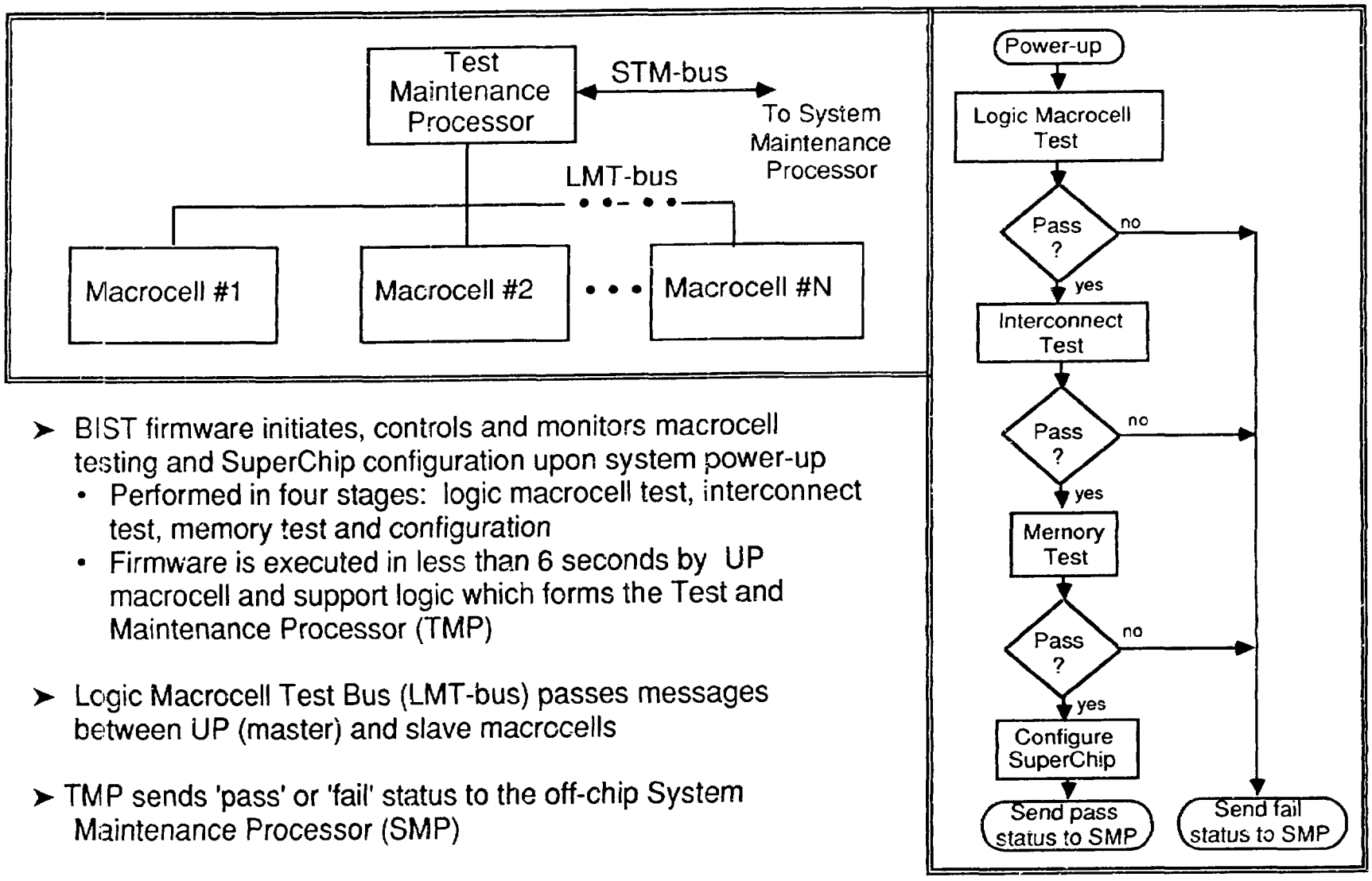
The system level BIST design used a hierarchical test bus architecture in which all chips contain ETM Bus interfaces. These chips are connected to a diagnostic maintenance device (DXMD) that contains the interface to the module level TM Bus. The DXMD was not fabricated for the VHSIC Phase 2 program. The TM-Bus can connect to IBM's "availability management system" for system level diagnostics and testing.

TRW

TRW's BIST approach was to partition a superchip into three sections: logic macrocells, interconnections between logic macrocells, and RAM arrays. The BIST system first tests the logic macrocells, then uses working macrocells to test interconnections between macrocells, and finally uses the working logic macrocells and interconnections to test the memory arrays. A serial test bus, the Logic Macrocell Test Bus (LMT Bus), provides communication between the central test processor and the local test hardware resident in the macrocells and supports testing at full chip speed.

Figure 3.1 illustrates the BIST system. The superchip BIST system minimizes the hardware located in the test node of macrocells under test and the size of the test bus. Test pattern generation and timing control hardware are located in the central test controller. The LMT Bus consists of four multiple-drop lines with pipelined repeaters. This test bus supports at-speed logic macrocell, interconnect, and memory test with a simple protocol, thus minimizing bus interface hardware in the macrocell test node, the Logic Macrocell Test Slave (LMTS). All bus transactions are controlled by the Logic Macrocell Test Master (LMTM) in the central test controller.

The LMT master provides the capability to generate the LMT Bus packets necessary to control LMT slaves for macrocell verification, configuration, and maintenance. A variety of control and data streams, including pseudo-random patterns, walking 1's and 0's, and solid



- BIST firmware initiates, controls and monitors macrocell testing and SuperChip configuration upon system power-up
  - Performed in four stages: logic macrocell test, interconnect test, memory test and configuration
  - Firmware is executed in less than 6 seconds by UP macrocell and support logic which forms the Test and Maintenance Processor (TMP)
- Logic Macrocell Test Bus (LMT-bus) passes messages between UP (master) and slave macrocells
- TMP sends 'pass' or 'fail' status to the off-chip System Maintenance Processor (SMP)

VHSIC10/89-1.13

Figure 3.1 Built-In Self-Test Features (TRW Superchip)

0's and 1's, can be generated with minimal external control. The LMT master can control many other test busses including the ETM Bus and commercial scan registers.

The LMT slave responds to LMT Bus commands in order to exercise real-time control over macrocell operation and perform at-speed compression of test results into an accessible signature. It also provides half rate and quarter rate clocks for the macrocell. Each logic macrocell contains an LMT slave.

3.1.2 Interoperability Standards

Although several projects used Phase 1 chips from different vendors on the same board, it was realized that the interoperability between new VHSIC chips (both 1.25 and 0.5 micron) from different vendors would be greatly enhanced if standards were established to specify their electrical, data path, and test bus interfaces.

Accordingly, the VHSIC Phase 2 Statement of Work, issued in 1984, stated the following requirements for interoperability:

"INTEROPERABILITY STANDARDS:

Interface/Interoperability Standards shall be established by agreement among all VHSIC Phase 2 Submicron contractors and the Government COTRs to assure that all chips developed under the VHSIC Phase 2 Submicron Program are interoperable, both electrically and physically. Standard voltage level(s) shall be established and utilized for all chips and input/output levels shall be equivalent for all chip interfaces, whether contained in a single or multi-chip package. A VHSIC half-micron Bus Interface Unit (BIU) chip shall be developed to facilitate module interoperability with a Standard Interconnect System Bus. The BIU and any other VHSIC chips developed under this Phase 2 VHSIC Submicron Program shall interface directly to a Standard System Maintenance Bus to be defined by agreement among all the VHSIC Phase 2 Submicron contractors and the Government COTRs. All these Standards shall be documented and delivered."

In accordance with this paragraph, a tri-Service Interoperability Committee negotiated four standards with the Phase 2 contractors (Reference 3.1). These were (1) electrical interface standards, (2) the parallel interface bus (PI-Bus), (3) the test and maintenance bus (TM-Bus), and (4) the element test and maintenance bus (ETM-Bus). The standards exist as copyrighted documents to prevent the propagation or publication of unauthorized changes, but they may be copied without modification. They are "open" standards, and may be used by anyone. The following is a description of each and its current status.

Electrical Interface Specification (Version 2.4, January 1988)

This standard provides interoperability between all Phase 2 chips, new Phase 1 chips, and standard TTL-I/O chips. Its purpose is to ensure the operation of VHSIC Phase 2 ICs from various vendors on the same board.

To permit the use of the Phase 1 chips and Phase 2 chips on the same board, new Phase 1 chips should comply with the Electrical Interface Specification, except that they will utilize a maximum 25 MHz for the SYSCLK signal frequency, and the DFNCLK signal will be operated at 1/4 of the SYSCLK frequency. Since both Phase 1 and Phase 2 chips operate at a maximum 25 MHz chip I/O at the package edge, this will provide direct interfacing. Redesign of original Phase 1 chips are expected to meet this specification also. It will ensure that chips which use the name "VHSIC" will enhance rather than detract from the "-ilities" of future DoD systems.

For existing printed circuit boards, the maximum I/O rate presently supported is 25 MHz. This limit is imposed by the physics of the board level interconnects. In the future, if impedance matched lines are used, higher I/O rates will be feasible. Both Honeywell and IBM have demonstrated that 50 MHz communications are achievable between ICs with impedance controlled lines on a multichip carrier. In addition, the Laser Pantography effort at Lawrence Livermore National Laboratory has constructed "Silicon PC Boards" with propagation velocities of 23 cm/ns as part of its VHSIC Phase 3 effort (Section 3.3.4).

Parallel Interface Bus (Version 2.2, March 15 1988)

The PI-Bus standard specifies the backplane parallel interconnection between VHSIC-based subsystem boards. Unlike microcomputer busses such as the VME, MultiBus, or FutureBus, the PI-Bus has no separate set of lines for addresses. This bus is meant to be a communications medium for systems to exchange messages or buffers of information, and not for CPUs to retrieve individual words from a memory. The bus provides a choice of 16- or 32-bit wide data paths, in either an "error detection" or a "single error correct, double error detect (SECDED) mode". All three VHSIC Phase 2 contractors have chosen to implement a 16-bit, error detection version of the BIU as a PI-Bus interface for their demonstration modules. IBM has over 1200 fully tested chips available. Honeywell has at least one fully functional part, and has packaged parts undergoing life testing, while TRW/Motorola has about 2700 functional BIUs which passed wafer probe. The bipolar drivers for the backplane are now available on the commercial market from Signetics. The PI-Bus is a standard interface on the Air Force Common Signal Processor (CSP) and called out in SDI technology programs such as the Advanced Spaceborne Computer Module (ASCM). It has been chosen by the Joint Integrated Avionics Working Group (JIAWG) as the backplane control bus for the ATA/ATF/ATH common avionics package. They will use a 16 bit error correcting version in a dual bus configuration, along with a dual TM-Bus, a MIL-STD-1553B serial bus, and a High Speed Data Bus. The Air Force ATF and the Army ATH (or LHX) are each in the

Demonstration/Validation phase with two competing contractor teams. By the ATF/ATA/LHX Commonality Memorandum of Agreement between the Services, the Navy is committed to a P^3I program to use the JIAWG specifications, and all three Services are committed to using the JIAWG avionics specifications/standards in deliveries after 1997. It also should be noted that the SAE-9 HINT committee, which was tasked to define a new parallel backplane bus, has selected the PI-Bus as the candidate for a new standard.

Test and Maintenance Bus (Version 3.0, November 1987)

The TM-Bus provides a serial backplane interconnection for the same 32 module set serviced by the PI-Bus by using four interconnect lines: Clock, Master Data, Control, and Slave Data. The TM-Bus is used by the Phase 2 VHSIC contractors on their demonstration brassboards. In addition, it is being quoted as the maintenance interface for several VHSIC contractors insertion efforts, and will be used by the ATA/ATF/ATH as explained in the PI-Bus section. The TM-Bus is being incorporated into draft standard IEEE 1149.5.

Element Test and Maintenance Bus (Version 3.0, November 1987)

The ETM-Bus standard provides the electrical and protocol definitions for a synchronous serial bus. This standard allows the designer to use chips from various VHSIC manufacturers on the same board and connect them to a common maintenance controller, which in turn receives its control and instructions via a backplane TM-Bus. A single controller can thus be used to test a board in both field and depot maintenance operations.

Because of interaction between the VHSIC ETM Bus group and the Joint Test Action (JTAG) working group, the proposed IEEE P1149.1 standard IC test bus proposed by JTAG came to be quite similar to the VHSIC ETM Bus. Honeywell has even designed a bus controller chip which will work with either bus although some differences remain between the two busses. The likelihood of wide acceptance of the P1149.1 bus in the commercial market makes it reasonable to expect it to supersede the ETM-Bus, even for military systems.

Maintenance of the VHSIC Bus Standards

Soon after the VHSIC bus standards were first proposed, a group at the Naval Ocean Systems Center encoded the PI- and TM-Busses in SIMSCRIPT and simulated them for different message types and load conditions. Several inconsistencies in the protocols, as well as ambiguities in the specification documents were discovered and corrected.

In 1988, when VHDL had become an IEEE standard, the VHSIC Interoperability Committee decided that the bus standards should be rewritten as VHDL descriptions to allow tests of the standards to be made in the widely available VHDL environment. In addition, it would also allow a designer to actually use a simulation model for a VHSIC bus with the

simulation of his system in order to evaluate which busses (16-bit, 32-bit, etc.) best fit the design requirements.

A team at the Science Applications International Corporation was contracted to write the bus specifications and test environment for both the PI- and TM-Busses in VHDL. The project was successfully completed in May 1990, and the entire system was demonstrated at the Naval Research Laboratory.

Copies of the VHDL PI- and TM-Bus specifications are available for computer downloading from the Naval Research Laboratory, Code 5305. A modified version that agrees with the Joint Integrated Avionics Working Group backplane specifications is expected to be available in the future.

3.1.3 VHSIC Hardware Design Language (VHDL)

Like many programs, the VHSIC Hardware Description Language (VHDL) was born out of necessity. By 1978, at the inception of the VHSIC program, DoD was already experiencing an unmanageable situation with parts obsolescence. Early VHSIC studies forecast that by 1990 about 80% of non-memory components in DoD systems would be Application Specific Integrated Circuits (ASICs). Additionally, the average lifetime of a semiconductor fabrication process was projected to be shortened to about two years. With the average system development cycle for DoD systems being 7-10 years, DoD was assured of parts obsolescence before a system was fielded.

The use of a Hardware Description Language (HDL) was viewed as the solution to the problem. By capturing the function of the device, as well as its hierarchical structure, a technology independent documentation would be created that could be used as a procurement specification to build new devices that performed the same function as the old one, but would be constructed in the prevailing technology. In addition, the HDL would produce a simulation model of the device that could be used to simulate at board, subsystem, and system levels. Thus for the first time DoD could also have the benefit of accurately knowing the performance of systems before construction.

While the obvious solution to the problem was the use of an HDL, in late 1979 and 1980 there were no commercial HDLs available. HDLs were in use in universities and custom computer aided design environments within large corporations.

DoD VHSIC program personnel believed that an industry standard hardware description language (HDL) was needed. In late 1979 through 1980, surveys of HDL technology were made. The conclusion was that while there were many HDLs in existence, all were either too limited in scope or proprietary. Thus, in the summer of 1981, the VHSIC office sponsored a workshop at Woods Hole, MA, gathering together language experts from industry, academia, and government, to define the requirements for a hardware description language. This workshop produced documentation that was used to generate a specification for an HDL.

In July 1983, a contract was awarded to Intermetrics, teamed with IBM and Texas Instruments, to develop a VHSIC hardware description language, simulator, and other

associated tools (Reference 3.2). The resulting VHDL version 7.2 was released in August 1985.

In December 1985, VHDL 7.2 was submitted to the IEEE as a candidate hardware description language standard. As a result, the IEEE created the VHDL Analysis and Standardization Group to standardize the language. The VHSIC Hardware Description Language (VHDL) became IEEE Standard 1076 in December 1987 and ANSI/IEEE 1076 in October 1988.

Since that time, the VHDL technology has been successfully transitioned to industry, academia, and government. About 50 Computer Aided Engineering tool suppliers have VHDL oriented products either on the market or in development. The IEEE and Electronic Industries Association are developing additional standards and practices based on VHDL. It is in production use within many companies and it is currently estimated that there are upwards of 1000 sites with VHDL capability.

In 1988, a VHDL Users Group was established first as an independent organization and, since June 1989, as a Technical Users Group under the IEEE Computer Society. There are currently about 800 members of the users group. More than 50 universities have VHDL activities ranging from research in areas such as design synthesis and formal verification, to using the language as a teaching aid in the design classes at junior level and above.

The Government has a wide variety of VHDL activities underway. VHDL was added as required documentation under MIL STD 454 Requirement 64 as of September 1988. A Data Item Description to cover VHDL documentation under contract, was developed by a tri-Service working group and became effective as DI-EGDS-80811 in May 1989. In cooperation with industry, the government has agreed to establish validation procedures and certification processes for VHDL models. This capability is expected to be on line by October 1990. Additionally, work is currently underway to place VHDL documentation requirements into MIL STD 1840 and usage guidelines into MIL Handbook 59 under the Computer Aided Acquisition and Logistics System (CALS) and to certify VHDL as a Federal Information Processing Standard (FIPS) in conjunction with the National Institute of Standards and Technology. The FIPS requirement covers systems through components, and extends the requirement to all government agencies.

Internationally, significant efforts with VHDL are underway in many countries, including Canada, England, France, Germany, Israel, Italy, Japan, Korea, and Sweden.

VHDL Language Definition and Development

The definition and development of VHDL was the cornerstone of the VHSIC design automation program, and was carried out under a contract with Intermetrics, Inc. Implementation of software started in August 1984, and continued into 1988. The software tool set developed included an analyzer, design library manager, reverse analyzer, and simulator. In September 1987, a VHDL language version for IEEE standardization was released, and, on December 10, 1987, the VHDL was approved as IEEE Standard 1076. Adoption of VHDL as an IEEE standard was a major VHSIC milestone, a step that ensures

that VHSIC designs documented in the VHDL will be readily transportable throughout the commercial and military IC design communities. The VHDL IEEE 1076 software (analyzer, design library manager, and fully interactive simulator) was delivered during 1988. Software is now production quality and resident on VAX/VMS and Berkeley UNIX on Sun workstations. An EDIF interface was added in 1990.

A VHDL newsletter is available from Intermetrics which regularly publishes information related to VHDL.

VHDL Independent Validation and Verification (IV&V)

The purpose of the IV&V effort was to test the VHDL software in actual use in the field. The primary contract for this effort was awarded to the United Technologies Microelectronics Center in August 1985. The work was divided into two parts. The contractor performed an initial test of the VHDL software and then acted as a focal point for secondary testing at "beta" sites. User comments from the beta test sites were incorporated into the IEEE 1076 version of the VHDL software. The contract was completed during 1988 and this part of the program concluded successfully with VHDL as a production tool.

Joint U.S./Canadian Rehost

Under the Joint U.S./Canadian program started in July 1987, the VHDL tools were adapted for use with high performance workstations. The U.S. provided the VHDL software, graphics interface, EDIF interface, validation tests, and technical consultation. The Canadian contractor, Bell Northern Research (BNR), installed the VHDL software on various high-end workstations and integrated some of its own design tools into that VHDL environment. The tools were ported to an APOLLO 4500 series platform and beta testing began in March 1990 for commercial release in June 1990. A DEC PMAX port was completed in May 1990, and beta testing began in July. Significant improvements to simulation efficiency were made by BNR. By using a different algorithm for event que management, a simulation speed improvement of 50 to 100% was achieved from the version 1.5 to version 2.1 of the Intermetrics tool set. BNR has also developed an EMACS based editor for VHDL that is available through the Canadian University Network. Additionally, work is progressing to integrate the VHDL system into the Cadence framework. The joint program is due to be completed in 1992.

3.1.4 Design Tools

At the very conception of the VHSIC program it was realized that in order to design chips of the required functional complexity, it would be necessary to employ computer aided design to a much greater extent than was current at the time. Furthermore, the high cost and

lengthy turn-around time of chip fabrication made it almost a necessity that designs be correct the first time.

In 1980, chip design was a compartmentalized process performed by separate individuals (or groups) using mostly manual methods. An integrated design methodology was needed which would utilize a set of automated design tools that would work together. At that time, among the six Phase 1 contractors, only IBM possessed an adequate CAD capability.

During Phase 1, the contractors were tasked to develop integrated CAD systems with which to design VHSIC chips. However, as described in Section 2.2.7, this approach was not practical and subsequently, much more focused goals for the VHSIC design tools program were formulated. They were three-fold:

- o to provide advanced design tools to support the designer using the VHDL,
- o to develop system level advanced design tools, and
- o to develop a comprehensive framework in which the design tools and design data could operate.

VHDL Insertion Tools

Workstations/Interfaces: The purpose of this effort was to develop terminals with interfaces which assist the designer using VHDL.

Gould (via subcontractor Vista Technologies) developed a prototype generic workstation interface for VHDL using a SUN 3 workstation, which automated the generation of VHDL code and checked for internal consistency. The work was completed successfully, and the final software was delivered in December 1987 to the Army at Ft. Monmouth and the Navy at the Naval Research Laboratory for evaluation. The new VHDL workbench allows a designer to input schematic diagrams and have VHDL structural descriptions compiled in real time. If functional descriptions are desired, the system provides "hand holding" by means of a syntax directed editor. The user can create VHDL code even with limited knowledge of the language. This system is a designer's entry into VHDL. The technology embodied in this program is being commercialized by Vista Technologies, and Vista is under subcontract to Intermetrics on the Canadian Rehost contract (Section 3.1.3) to provide a graphics interface to the Intermetrics tool set.

Integration of VHDL and ADAS: The goal of this contract was to integrate the Architectural Design and Assessment System (ADAS), developed by the Research Triangle Institute, with VHDL in such a way that system designs may be captured (hierarchically) with ADAS and archived in VHDL, thereby enhancing the ADAS tool set. To support this effort, extensive modifications to the ADAS graph editor, data base, and simulator were carried out. The net result was an integrated design system which took advantage of the modeling and simulation capabilities of both ADAS and

VHDL. Using these tools, designers can capture and simulate their designs at several levels of abstraction.

During 1988, implementation of the modifications to ADAS to support the VHDL interface was completed. The original interface was built around VHDL Version 7.2. After VHDL was standardized by the IEEE in December 1987, the interface was modified to support the new VHDL standard.

The ADAS simulator was also extensively modified under this contract. The modifications reduced the need to use functional simulation to model complex systems. The contract was completed in September 1988, and the results of the contract work were delivered to the Government. See References 3.3 and 3.4 for further details.

Synthesis Tools: The purpose of these efforts was to develop software techniques which would derive chip design data automatically from a VHDL behavioral description.

Honeywell developed a tool called V-Synth which determines a useful chip architecture from input that is algorithmic in nature and contains an implied structure. The output is an architectural description of a microprogrammed device in VHDL and the microcode to drive the device. Honeywell delivered a prototype of the software in June 1987 and the final version in November 1987. In 1988, Honeywell upgraded the VHDL Synthesis System under the VHSIC Phase 2 contract to be compatible with the IEEE Standard VHDL. The register transfer level VHDL behavioral description of the Phase 2 BIU chip design was synthesized using V-Synth. The generated microcode required 31 words of 40 bits each. The contract was completed in September 1989 and the software and final technical report were delivered. See Reference 3.5 for further details.

JRS Research developed an Automated VHDL/Microcode Compiler Synthesis and Design System (AMSDS) which synthesizes a microprogrammed processor architecture from an Ada program and a VHDL description of chips. Output from the program is a VHDL description of the processor and optimized microcode for the processor.

Sperry (now Unisys) was under contract to interface the VHDL analyzer to the MIXSIM interactive simulator. The contract was completed in May 1987 and the VHDL interactive simulator was delivered to Government laboratories for test.

Silicon Compiler Interfaces: Research Triangle Institute, Silicon Compiler Systems, and E-Systems completed the development and demonstration of the VHSIC Silicon Compiler (VSC). This effort involved the integration of ADAS, GENESIL and VHDL. Using the VSC, engineers can capture and model designs from the system to the transistor level. Designers can then use GENESIL as a fabrication mechanism for new integrated circuits identified during the design process. Information is transmitted among the tolls in the VSC with special purpose interfaces which provide the desired capabilities. Major capabilities include:

- o the representation of GENESIL objects in ADAS such that designers can evaluate the performance and functionality of a proposed chip design in the context of the overall system,

- o the ability to partition a hardware hierarchy based on its estimated area and power dissipation, and

- o the generation of VHDL functional models from GENESIL which can be incorporated into the hierarchical VHDL models produced by ADAS.

As part of the contract, E-Systems used the VSC tools to develop and simulate an image processing system. Part of the system included the development of a special purpose ASIC which performed the core calculations required for the imaging application. The simulation was done in VHDL Version 7.2.

The initial version of the VSC used VHDL Version 7.2. After the IEEE standardized VDHL, the VSC tools were converted to the 1076 standard. The contract was completed in September 1988 and the results were delivered to the Government.

The CMOS interface effort by National Semiconductor complemented this by making it possible to produce the chip designed with the GENESIL compiler on the National Semiconductor CMOS VHSIC pilot line. This provided an experimental demonstration that the hardware output corresponds with the input design specifications. See References 3.6 through 3.11 for further details.

VHDL Models: As part of its effort in the development of systems design tools reported above, JRS improved the comprehensiveness of VHDL modeling to include complex behavioral models, detailed physical attributes, and a greater variety of devices. JRS produced, analyzed, and simulated VHDL 1076 models of the TRW, TI, and Honeywell Phase 1 VHSIC chips.

System Design Tools

Under this program, advanced design tools were developed aimed at making the higher (system) level of the design process more automated and more efficient. The efforts in this area provided a variety of tools in fields such as design verification, design for test, advanced system synthesis, and life cycle cost modeling. Several contracts were awarded to universities in order to develop advanced concepts in this subject area and, at the same time, introduce VHDL into the academic community. Work on this part of the program began in September 1986. All work has been completed.

VHDL Annotation Language (VAL) (Stanford University: The VHDL Annotation Language (VAL) is a language extension of VHDL which allows designs to be specified as annotations to VHDL. Hardware behavior is defined by simple abstract

specifications and the behavior is related to more detailed architectural descriptions in VHDL. VAL augments VHDL by supporting powerful constructs for timing and abstraction, and simpler constructs for parallelism. It also provides some basic constructs for expressing correspondence between VAL specifications and VHDL architectures. VAL annotations are used to check consistency between VAL specifications and VHDL architectures during simulation. The contract was completed, and the VAL preprocessor is available through Stanford University. For further details see References 3.12-3.14.

Automated VHDL Microcode Computer Synthesis and Design System (JRS Research Laboratories): The project goals were to provide an integrated set of high level design automation/CAD tools for hardware/software design of high performance embedded computers for DoD applications. Included in the tool set are (1) an Ada to microcode compilation system that is automatically retargetable from VHDL, (2) an automated system that synthesizes designs described in VHDL from specifications written in Ada, and (3) links to external tools including silicon compilers.

JRS has been actively pursuing the development of this technology for the past nine years, including its association with the VHSIC Program since 1984. Versions of Ada to microcode compilers for four VHSIC Phase 1 processors were developed along with VHDL models of the chips. A functional prototype of the AMSDS was delivered to the VHSIC program offices of the three Services in June 1987, with additional releases through March 1990.

Highlights of the program are automatic compiler generation from a VHDL model of a processor, processor synthesis from application programs in Ada and C to a VHDL processor model, and a VHDL interface to the Seattle Silicon compiler. See References 3.15 and 3.16 for further details.

Advanced Design AutoMation (ADAM) System (University of Southern California): Prototype design tools were developed to allow a designer to specify requirements for a design in VHDL and produce a register transfer level description. A user interface was designed to provide the capability of entering design information into ADAM by writing descriptions in either VHDL or a natural language (i.e. English-like). A synthesis subsystem takes a behavior specification of the design and creates a register transfer level data path and a schedule of operations to be performed so that the data flow can be pipelined. An object oriented database manages the information for the system. License agreements from the University of Southern California have been obtained for distribution of the software to universities and industrial research laboratories within the United States, for research purposes only. All tasks were completed in the spring of 1990. For details see References 3.17 through 3.23.

Hierarchical Design for Testability (Research Triangle Institute): Utilization of the Test Engineer's Assistant (TEA) system methodology and computer-aided design (CAD) tools enables design and test of digital hardware to occur in parallel with system

functional design and results in systems that are maintainable at a lower life cycle cost. TEA provides a methodology and a supporting CAD system that allows the system designer to meet testability requirements. This is accomplished by supporting design for testability and built-in test (BIT) techniques at all levels of design abstraction. TEA interfaces directly to ADAS tools and through ADAS to VHDL.

RTI developed five tools in 1988. The Design for Testability Guideline Checker identifies untestable structures and recommends alternatives that are more testable. BIT Recommendation divides a board into ambiguity groups (AGs) for fault isolation testing and recommends a class of BIT techniques for each AG. BIT Overhead Summary calculates the approximate hardware overhead (i.e., test points, BIT support modules, and additional I/O) associated with the implementation of a particular board level BIT technique. BIT Placement Recommendation generates a new schematic of the board with a sample implementation of the given technique. System Summary itemizes the incremental hardware overhead attributable to added testability. The contract was completed in December 1988. See References 3.24-3.29 for further details.

Analog Design with VHDL (Dartmouth University): This effort explored the use of the VHDL linkage port to escape to other styles of design. An object oriented system based on Prolog was constructed, and rules to allow the design of different filter types were generated. The contract was completed in 1989 and prototype software and technical report were delivered to the government. See Reference 3.30 for further details.

Object Oriented Chip Design Using VHDL (Rensselaer Polytechnic Institute): An advanced design tool was developed that uses a novel way of producing a design. The designer has available a set of components, or building blocks, in a library from which he can build a chip. These blocks are keyed like jigsaw puzzle pieces so that the design process is analogous to putting a jigsaw puzzle together. As the design progresses, the VHDL description and the chip physical layout are produced automatically. The research was completed in 1989.

Artificial Intelligence for VHSIC Systems Design (AIVD) (RTI / OCTY): An advanced design tool was developed that uses a novel way of producing a design by working at the systems level. The designer has available a set of components, or building blocks from which he can build a chip, or in the general case, an electronic system. The user interacts with the system through an object oriented interface which permits access to components in an object oriented data base (the ROSE database developed at RPI). The system consists of an editor, the design library, a search engine, and a tool for insertion and extraction of designs expressed in VHDL. As the design progresses, the VHDL description is produced automatically. The contract was completed in 1989. See References 3.31 and 3.32 for further details.

Engineering Information System (EIS)

Requirements and Goals: An engineering automation system requires a framework within which hardware and software information can be managed from the inception of a design through its complete life cycle. The EIS allows data to reside in a heterogeneous hardware environment while presenting a homogeneous view of the data to the designer. The EIS program is being executed against a requirements document compiled by the Institute for Defense Analyses based on a series of industry, government, and academic workshops held in the mid-1980s. The prime contractor, Honeywell, began work in June 1987 and is due to finish in January 1991.

The main goal of the EIS program is to develop a set of specifications as strawman standards for tool and data interoperability. These candidate standards are being introduced into the commercial standardization process with the intent that a broad base of support will carry them into general use. Secondary goals of the EIS program are to demonstrate the feasibility and usefulness of these framework standards via prototypes and engineering demonstrations.

EIS will significantly enhance the payoff of prior VHSIC successes by increasing the utility of the VHSIC computer aided design and test tools and by lowering the cost of designing and inserting VHSIC chips. In addition, EIS is highly synergistic with the VHDL and TISSS programs (Sections 3.1.3 and 3.2.2).

Approach: In order to supply the necessary functionality, a broad set of services is necessary. The specifications for these services were determined by:

- adopting an existing standard for a necessary service when one was available.
- extending an existing standard to provide necessary services when the need could be met in such a way, and
- developing a new candidate standard in areas where no standardization has occurred, or where an existing standard clearly was not meeting the needs of the EIS community.

The implemented approach for developing new standards is responsive to the EIS objectives to permit the maximum use of existing technology and to preserve migration paths for vendors of products in related areas to meet the EIS specifications. EIS allows users to incorporate existing tools and databases so that the value of previous investments is retained.

Figure 3.2 shows the resulting conceptual nature of the EIS, wherein there is a set of general purpose framework services which operate against domain specific models. The basic paradigm is object-oriented, which allows the data management

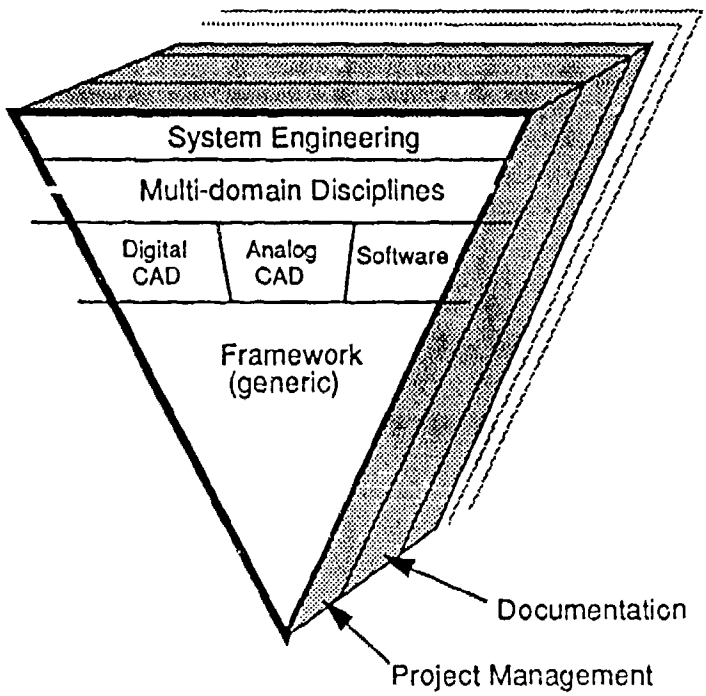


Figure 3.2 Relationship Of Frameworks To Application Domains

services to access other data organizations easily. The EIS has developed one domain specific model for digital IC design.

Results, Accomplishments, and Conclusions: The specification phase resulted in a three-volume document (Reference 3.33) which compiled the feature approaches, language-independent service interfaces, and the information model to support digital IC design. This material was widely reviewed throughout industry and received positive evaluations. Incremental builds of these specifications have shown their feasibility and usefulness. EIS is the only comprehensive specification of a general purpose engineering framework available today.

The EIS program has had a substantial impact on the development of standards in the CAD community. Within a year of the program outset, the CAD Framework Initiative (CFI) was formed. CFI is a consortium of over 50 companies addressing the same basic scope as the EIS specifications.

The EIS program has supported the CFI in providing strawman candidate standards and in defining CAD interoperability. To date, the CFI has adopted several EIS positions and used other EIS specifications as baselines for CFI subcommittees.

The EIS prototyping phase began in October 1989. The purpose of the prototypes is to establish validity of the specifications, determine feasibility of implementation, demonstrate that EIS can be built on existing software and adapt to existing tools, and to provide a vehicle for application demonstrations (EIS in actual use).

Build One of the prototypes, which has been completed, implements the high level object management services suitable for supporting CAD tool attachment and data interoperability on a local network. In addition, Build One validated the basic object/function invocation model. A user manual for the prototypes will be available in January 1991 from Honeywell (Reference 3.34).

The EIS Program held a series of open workshops, the most recent being in November 1989. The next open workshop is scheduled for early in FY1991. A newsletter is published monthly and distributed to a mailing list of 2500 individuals in the US and abroad.

3.2 Test and Life Cycle Support

This section brings together the various VHSIC activities relating to the very important areas of test and evaluation of the performance and radiation hardness of VHSIC chips, the qualification procedures to insure reliability, and new maintenance concepts needed for VHSIC.

3.2.1 Test and Evaluation

In-House Test and Evaluation of VHSIC Chip Performance

Army (ETDL): The Reliability, Testability, and Quality Assurance Branch of the LABCOM ETDL tested and evaluated the following VHSIC chips. The characteristics of each chip are described in Section 3.4.

Correlator (Hughes) - Parametric measurements were verified on both the correlator wafer test structures and a packaged device. Functional tests were not performed due to device tester limitations. All work was performed between May 1984 and December 1985.

Static Random Access Memory (SRAM) (Texas Instruments) - Electrical performance verification tests of the SRAM in a DIP package were performed using a non-pipelined mode in a joint effort by ETDL and the Rome Air Development Center (RADC). Results of dc tests were in agreement with TI test data. Ac test data, however, showed failures in access time and functional operation at elevated temperature. ETDL performed essential electrical characterization on 105 SRAM samples in the LCC package including dc and ac parametric tests in both non-pipeline and pipeline modes. Of these, 95 devices were shipped with test data to Hughes for use in the VHSIC Firefinder upgrade program. ETDL coordinated preparation of a detailed specification in Military Drawing Format by TI for the SRAM device. All work was performed between September 1984 and October 1987.

Multiport Switch (MPS) (Texas Instruments) - Electrical performance tests were performed at ETDL and TI. ETDL coordinated preparation of a detailed specification in Military Drawing Format by TI for the MPS device. All work was performed between December 1984 and July 1987.

Static Random Access Memory (SRAM) (Westinghouse) - The chip set was produced jointly by Westinghouse and National Semiconductor. Electrical performance verification tests were performed at ETDL over the full range of military temperature. Functional and parametric test data were in good agreement with

manufacturer's test data. All work was performed between August 1985 and November 1985.

Arithmetic Element Controller (AEC) (Hughes) - The AEC device was designed by Hughes and manufactured by LSI Logic for use in the VHSIC Signal Processor (VSP) module in the VHSIC/Firefinder upgrade. Electrical performance verification, functional, and parametric tests were performed at ETDL over the full military temperature range. Test results showed satisfactory performance and maximum data rates of 33 MHz at 25°C, 34 MHz at -55°C, and 26 MHz at 125°C. All work was performed between February 1984 and March 1989.

Signal Processing Element (SPE) (IBM) - Electrical performance verification tests at ETDL showed functional failure at -55°C, and maximum data rates of 22 MHz at 25°C and 26 MHz at 125°C. Failure at low temperature was due to the presence of electrical noise in the PGA package that increased as temperature decreased. Improved functional performance in the PGA package can be obtained with careful test fixturing and installation. In tests performed at ETDL and IBM, the SPE device in the PGA package did not function successfully at specified frequency and threshold voltage. However, IBM did achieve satisfactory performance of the SPE chip when used in a comparatively noise free multichip package. Other problems included a static power supply current (IDD) that exceeded the design specification, and a design problem in the on-chip-monitor (OCM) alleviated by use of a reset sequence in the data input at start-up to release the data bus. IBM reviewed all of these problems to determine corrective action. All work was performed between June 1988 and December 1989.

Bus Interface Unit (VBIU) (IBM) - Performance tests at ETDL included parametric and functional. Functional verification at the 50 MHz data rate was not achieved due to a noisy test fixture. Tests were performed at data rates of 36 MHz at -55°C, 34 MHz at 25°C, and 33 MHz at 125°C. All work was performed between December 1988 and September 1989.

Air Force (RADC): Over the duration of the VHSIC program the Microelectronics Reliability Division at the Rome Air Development Center performed detailed tests and evaluations of several VHSIC devices. The RADC test facility houses the enhanced VHSIC automated microcircuit electrical test system, the Tester Independent Support Software System (TISSS) central host computer, and VLSI design workstations. A brief chronology of the electrical testing performed by RADC is described in the following paragraphs.

During FY87, RADC developed test programs and performed characterization testing on four VHSIC device types: the Honeywell Sequencer, the Texas Instruments 72k SRAM, Westinghouse/National 16k and 64k SRAMs, and the IBM SPE chip.

Results of the memory device characterizations were documented in a joint AF/Army report (RADC-TM-86-5) and were also presented in a technical paper at the 1985 Government Microcircuit Applications Conference (GOMAC). See Reference 3.35. Several device performance deficiencies were noted during the testing and were reported directly to the manufacturers to facilitate corrective actions. All device testing was documented in report form and forwarded to the Army, Navy, and Air Force VHSIC program offices.

In FY88, test program development and device characterization focused on the Intel VHSIC-like static RAM, MIL-M-38510/613. This was the first VHSIC or VHSIC-like device to receive military qualification status. The characterization included all ac, dc, and functional tests included in the specification along with plots of various operating characteristics and a mini-life test on a sample device. The testing performed on the samples obtained by RADC indicated that the devices were able to meet all specification limits by wide margins and show good long term reliability potential. Results of the characterization were reported in RADC-TM-89-18.

RADC also investigated samples of TRW's CMOS 1028-bit Dual Static Shift Register. This device was fabricated using TRW's VHSIC CMOS process. Testing at TRW indicated that the device exhibited high supply currents when certain bits were stored in the shift register. This was confirmed by testing at RADC, and corrective actions were suggested to TRW in order to eliminate the problem.

Navy (NOSC and NRL): In 1986, functional tests were performed at the Naval Ocean Systems Center (NOSC) on Phase 1 CMAC and SPE chips from IBM, CAM and WAM chips from TRW, a 16k SRAM from National Semiconductor, and an FPMAK chip from Raytheon. The IBM, National, and Raytheon parts passed the functional tests over the frequency range 1-25 MHz at room temperature. The TRW parts were functional at 1 MHz, but defects in the tester adapter board prevented testing at higher clock speeds.

NOSC also performed parametric tests on Phase 1 test chips from IBM, TRW, Motorola, and Honeywell. Measurements included transistor parameters, contact resistance, and resistivity.

In 1987, the Naval Research Laboratory desinged a sidelobe canceller that incorporated TRW's MAC chip and two personalizations of the Motorola V6000 gate array. The system ran as designed at speeds up to 19 MHz with simulated data.

In-House Test of VHDL Phase 2 Chip Descriptions

Navy (NRL): As part of the acceptance procedure for deliverables, the Naval Research Laboratory (Code 5305) was tasked to test and accept the VHDL chip descriptions delivered on the Phase 2 contracts.

The descriptions delivered by IBM contained non-standard, VHDL ANSI/IEEE-1076 code; therefore, simulations were not run.

VHDL descriptions of the TRW macros were found to be in error after testing a packaged 1PRAM for functionality on a Daisy PMX system. NRL corrected the Intermetrics VHDL model of the 1PRAM and also wrote a correct set of test vectors. The model and the actual part were then found to give identical results when running the same set of test vectors.

Electromagnetic Effects (EME)

Electromagnetic Effects (EME) include upset and damage from radiated and conducted sources such as electromagnetic pulse (EMP), electromagnetic interference (EMI), radio frequency interference (RFI), high power microwaves (HPM), electrostatic discharge (ESD), and lightning. The EME Subcommittee of the VHSIC Qualification Committee investigated the problems associated with establishing standards for testing and accepting VHSIC devices for military systems. Results were presented in the EME Subcommittee report, Reference 3.36.

IBM Work on Electromagnetic Effects (EME): The IBM VHSIC Phase 2 Final Technical Report (Reference 3.45) states that (a) protection against electromagnetic pulse (EMP) is a system problem and cannot be resolved at the chip level, and (b) IBM has demonstrated electrostatic discharge (ESD) protection exceeding 800 V (human body mode) on packaged VHSIC chips. After Phase 2, work continued on ESD protection. New IBM designs were manufactured and evaluated using the VHSIC Phase 2 process. These new designs offered negligible performance degradation and provided protection level capability of up to 4000 volts.

Test and Evaluation of VHSIC Chip Radiation Hardness

VHSIC chips are required to operate in environments which subject them to nuclear and space radiation threats: total dose (TD) effects; neutron damage; ionizing rate for upset and latchup (LU); ionizing level for survivability; and single event upset (SEU) produced by alpha particles, protons, and heavy ions. In Section 3.3.2 (IBM) and Section 3.3.3, several of the process improvements to enhance radiation hardness are described. The present section gives the results of the radiation hardness tests on Phase 1 chips. Details of the test procedures are given in the 1987 VHSIC Annual Report (Reference 2.28, Section V.4.1). The results of the radiation tests for IBM Phase 2 chips are given in Section 3.3.2.

The test chips that were used to demonstrate the radiation hardening achieved in the DNA VHSIC Extension-To-Space program are listed in the following table

Contractor	Technology	Test Chip	Radiation Test *
Westinghouse/NSC	CMOS	10k gate array/64k SRAM	All
Motorola	CMOS	Discrete transistors	TD
IBM	NMOS - CMOS	Macro II test chip	TD/SEU
Hughes	CMOS/SOS	Test structures	TD,SEU
Harris/GE/RCA	CMOS/SOS	64k SRAM	All
Honeywell	Bipolar	SEU test chip	SEU
TI	STL	ACS chip	LU
TRW	Bipolar	Macrocell test chip	LU

* TD = total dose; SEU = single event upset; LU = latchup

Westinghouse: The SAFE implant used by Westinghouse in hardening its gate arrays was also used with the 64k SRAM, but the recessed n^+ change was not implemented initially due to the magnitude of the layout changes that would have been required. A scheme to incorporate the recessed n^+ design into the SRAM was developed by National Semiconductor Corporation in a subsequent IRAD program. Without the fully recessed n^+, the SRAM demonstrated a total dose hardness capability between 100 and 200 kilorads. With the recessed n^+ implemented, the 64k SRAM was hard to 1 megarad. The 10k gate array fabricated at Westinghouse was also hard to 1 megarad.

The use of p^- on p^+ epitaxial substrates eliminated dose rate induced latch up and led to an improvement in the dose rate upset threshold from $1x10^8$ rads/s to between $7x10^8$ and $1x10^9$ rads/s. Heavy ion SEU tests showed that the SRAM's projected error rate was reduced from $1x10^{-5}$ to $5x10^{-6}$ upsets/bit-day by the epitaxial substrate, and then to less than $5x10^{-9}$ upsets/bit-day by incorporating cross-coupled resistors in the SRAM memory cell. These values are based on room temperature operation at 3.0 volts. At 5.0 volts, the SRAM improved to less than $1x10^{-10}$ upsets/bit-day, while the gate array with no SEU hardening was characterized by an error rate of $5x10^{-7}$ upsets/bit-day.

IBM: Following the VHSIC Phase 1 program, IBM transitioned their radiation hardening activities to a 1.25 micron bulk CMOS process. This technology had been installed as part of their strategy to produce submicron CMOS under VHSIC Phase 2. CMOS also became the IBM 1.25 micron technology and has benefited from the radiation hardening activities during the VHSIC Phase 2 and GVSC programs. The IBM Phase 1 CMOS technology is hard to 1 megarad total dose and $1x10^9$ rads/s dose rate upset threshold; less than $1x10^{-10}$ upsets/bit-day SEU is available; and it has no latchup. IBM has produced 64k SRAMs with this technology and is developing a 256k SRAM.

Hughes Aircraft Corporation: CMOS/SOS correlator chips produced by Hughes during the regular Phase 1 program met or exceeded space hardness levels, especially in the areas of dose rate upset and latchup, where the use of SOS offers intrinsic advantages. In total dose testing, the correlator remained functional up to doses of 2 to 3 megarads, but leakage currents became significant at several hundred kilorads.

Harris/GE/RCA: Total dose tests have shown that the CMOS/SOS 64k SRAM functionality is maintained to several tens of megarads. However, further work is needed to reduce standby current which becomes significant and saturates after approximately 100 krads. Dose rate upset hardness has been demonstrated to more than $2x10^{11}$ rads/s, while SEU testing with heavy ions under normal bias conditions produced no upsets at effective linear energy transfers up to 250 MeV/(mg/cm^2), which makes it effectively immune to cosmic ray upset.

At the present time, Harris is fabricating the 64k SRAM along with 1.25 micron gate arrays and custom chips in the CMOS/SOS process. Thus, a spectrum of radiation hard SOS chips is currently available.

TRW: Content Addressable Memory (CAM) chips were processed along with a test chip containing about 200 special structures for studying latchup effects. Process lots included standard bulk, 7 micron, 10 micron, and 15 micron epitaxial starting wafers. CAMs manufactured on 7 micron epitaxial substrates exhibited no latchup responses at dose rates up to $2x10^{10}$ rads/s with supply voltages as high as 7 volts. PISCES modeling, coupled with bench characterization of the test structures, revealed that the 7 micron thickness was optimum for preventing latchup in TRW's triple diffused bipolar process. These substrates eliminated latchup without decreasing manufacturing yield or performance.

3.2.2 Test Technology

The Tester Independent Support Software System (TISSS)

The TISSS is a system for the automated generation and maintenance of electrical specifications and test programs for digital microcircuits. The use of the TISSS requires the chip designer to address, at a very early stage in the design, the question of how the desired functionality captured in the design is to be tested. The lack of coordination between the functional specifications and the specifications for test was becoming a serious problem with the advent of increasing chip complexity. Furthermore, the preparation of test vectors was requiring a large effort and had to be targeted to a particular tester.

The system includes a database-centered software support system that is independent of both the computer aided design and test environments and information representation languages for test vector/waveform data and test specification information to accomplish its

automation goals. These languages are currently undergoing standardization within the IEEE design and test communities.

The capability provided by TISSS enables the user to develop and maintain complex, device design and test information in a standardized, transportable computer-accessible format that can be used to automatically generate test vectors for the device into the data format appropriate to the tester being used. The Government use of TISSS significantly reduces the time required to insert advanced technology microelectronics into operational systems. In addition, the device data stored in the database can be used for reprocurement of devices no longer being manufactured.

Full scale development of TISSS was begun by the Harris Corporation in September 1985 and software development and initial application to the Generic VHSIC Spaceborne Computer (GVSC) microcircuits was completed during 1989-1990. This initial use of TISSS was for the generation of electrical test specifications and test programs for the GVSC microcircuits developed by the Air Force Space Technology Center (AFSTC). During this demonstration and application, the GVSC contractors, Honeywell and IBM, utilized TISSS software installed at their sites for the generation and capture of electrical test specifications for their respective GVSC microcircuits. They also translated test vector information to the TISSS Vector Language (TVL) for submission to the TISSS data base. After this information was generated and captured, it was then sent to the Rome Air Development Center for audit using the TISSS located there. After auditing, the information was used to automatically generate test programs for all of the GVSC microcircuits. The use of TISSS reduced the time needed to generate these complex GVSC test programs from an estimated one man-year to two man-weeks. The test programs were generated using the newly completed TISSS Teradyne J953 postprocessor.

Following the successful demonstration and application of TISSS in the GVSC Program, AFSTC required that the TISSS methodology be used in microcircuit development work to be performed by the Advanced Spaceborne Computer Module (ASCM) Program. Under this program, TISSS will also be applied to support design and test information capture and automatic test program generation for digital boards developed by the ASCM Program.

In 1990, the TISSS program will complete the development of a generic postprocessor that will greatly enhance industry acceptance of the TISSS data standards and practices. The generic postprocessor will reduce the time and cost associated with customizing the TISSS postprocessor to work with new target microcircuit and printed circuit board testers. The TISSS generic postprocessor, like the rest of the TISSS software, is coded entirely in Ada.

In addition to the TISSS applications to digital microcircuits, TISSS is currently undergoing extensions to support digital line replaceable modules (LRMs) targeted for next generation aircraft platforms, such as the Advanced Tactical Fighter (ATF). The TISSS extension development is currently supported by the ATF Program Office. The TISSS will be demonstrated during the summer of 1990 with applications to LRMs targeted for the ATF. The demonstration will consist of the capture of design and test information for Integrated Communication Navigation Identification Avionics (ICNIA) LRMs and auditing of the information using TISSS. After automatic auditing by TISSS, the information will be used to automatically generate test programs for two target testers, one located at RADC and the

other at the Sacramento Air Logistics Center. This demonstration will show the functionality of TISSS as applied to digital LRMs and also the feasibility of the capture and use of design and test information for LRM production, integration, certification, and life cycle support.

The TISSS information standards used are the VHSIC Hardware Description Language, discussed in Section 3.1.3 of this report, the TISSS Vector Language (TVL), and the Test Description Language (TDL). VHDL was standardized by the IEEE as ANSI/IEEE 1076-1987. The TISSS TVL is currently undergoing IEEE standardization and will be called the Waveform and Vector Exchange Specification (WAVES). The Test Description Language (TDL) is beginning IEEE standardization and will be called the Test Specification Language (TSL). The successful standardization of these representations will fulfill the VHSIC goal of defining the information languages for representing and easily interchanging for use all information necessary for microcircuit design, manufacture, test, insertion, and life cycle support. See References 3.37-3.41 for additional information on TISSS.

Microcircuit Testers

The Rome Air Development Center (RADC) is the lead organization responsible for the generation of specifications for qualification testing of integrated circuits used by DoD. Accordingly, they have been concerned with the capability of available testers for testing VHSIC-class devices.

At the start of the VHSIC program it was clear that existing microcircuit testers would not be capable of adequately assessing the quality of Phase 1 VHSIC chips. For example, a good portion of the earliest electrical testing on VHSIC Phase 1 memory devices was performed on a Tektronix S-3270 automated tester. The S-3270 had the capability of testing devices with up to 64 I/O pins at speeds up to 20 MHz. However, it did not have the performance necessary to test the majority of VHSIC devices. Electrical testing was therefore transitioned to a GenRad GR-18 capable of testing devices with up to 288 pins and clock rates up to 40 MHz with patterns of up to 256k test vectors.

RADC surveyed the tester manufacturers and it was apparent that even next generation test equipment would not have the necessary performance for characterizing Phase 2 VHSIC devices. Therefore, a contract was initiated with GenRad to develop a VHSIC-class microcircuit tester in 1984.

However, GenRad decided not to continue in the tester business. In fulfillment of their contract, however, they did deliver and install at RADC a Teradyne J953 tester which met RADC's requirements that it be capable of testing 100% of VHSIC Phase 1 devices and approximately 85% of VHSIC Phase 2 devices. It is capable of uncompromised testing of devices with up to 256 I/O pins at data rates up to 50 MHz. By multiplexing adjacent pins, the J953 can test devices with clock rates up to 100 MHz. The J953 can place timing edges with an accuracy of 500 ps and apply patterns to the device of up to 4M vectors. The test head has very low capacitance (30 pF) which lends itself to accurate waveform reproduction.

Of equal importance with the hardware, is the capability of the software that can be used with any test system. A TISSS postprocessor for the J953 makes it possible to generate

entire test programs for complex devices in a few weeks instead of the several months that had been required in the past.

3.2.3 Reliability and Qualification

Introduction

The reliability of integrated circuits has always been a serious issue for the semiconductor industry. Military requirements have further necessitated the establishment of qualifying procedures and standards, in order for parts to be used in DoD systems. However, as devices of increasing complexity, requiring new and complicated fabrication processes are designed and built, the problem of assuring their reliability becomes more difficult. The cost of qualifying parts becomes an important consideration that in turn depends on their demand.

The VHSIC program attempted to address these problems with a three-fold approach. The first encouraged Phase 1 chip suppliers to demonstrate the use of the existing qualification procedures. These procedures are:

- the certification of the production line (fabrication, assembly, and test procedures) in accordance with MIL-STD-976 to assure a controlled manufacturing process,
- characterization and documentation of of the device in a dated specification (called a "slash sheet") in accordance with MIL-STD-38510, and
- testing of a designated production lot in accordance with MIL-STD-38510 and MIL-STD-883C procedures.

Devices which satisfy these requirements are put on a Qualified Parts List (QPL). The status of these procedures as of December 1988 are given in the 1988 VHSIC Annual Report (Reference 2.29). More recent additions to the QPL are given below.

The second approach was to support the development of improved test methods, reliability prediction models, and software tools. Early contracts are listed in Appendix B (Early Phase 3 Projects, Section 8). Contracts completed after 1986 are listed in Section 3.2 of Appendix B. Two of these are discussed below: Reliability Assessment of Gate Arrays and Reliability Prediction Modeling. The TISSS project has already been discussed in Section 3.2.2.

The long term approach was to develop a set of generic qualification procedures that take advantage of test areas on the VHSIC chip, separate test chips, and separate test wafers to control and document the extremely complex fabrication process. The design procedures are also subject to certification. Manufacturers whose fabrication, design and control procedures meet the requirements have their facility placed on the Qualified Manufacturers List (QML).

Reliability Assessment of Gate Arrays (GTE)

This project by General Telephone and Electronics focused on the generic qualification of gate arrays and the reliability of representative products. The final technical report (Reference 3.42) contains the contractor's results of step-stress, life tests, and failure analysis done on CMOS standard evaluation circuits. The current military specifications for gate array devices require a Standard Evaluation Circuit (SEC) to be used to assess the quality and reliability of a manufacturer's gate array family. The concept behind the SEC is to run exhaustive reliability tests and characterize the electrical parameters of one device which represents the design rules and macrocell library of a particular technology and array family. Subsequent designs in the same family would not require the life tests and qualification screens specified for all QPL devices.

This program defined the recommended circuitry for CMOS and ECL SECs. To evaluate the effectiveness of current military requirements, the SECs of two manufacturers were tested. The SECs were electrically characterized and the results summarized. Reliability, step-stress, and life testing was done on a CMOS SEC to validate current test methods. The failure mechanisms studied were electromigration, hot electron effects, and dielectric breakdown. The program concluded that current high temperature life testing and burn-in testing are adequate to detect any electromigration and dielectric breakdown problems. The program recommended dynamic low temperature life testing of SECs and dynamic low temperature burn-in of production devices to monitor hot electron effects in CMOS devices. Also, a list of desirable features for computer aided design (CAD) tools was developed.

Reliability Prediction Modeling

IIT Research Institute (IITRI) and Honeywell SSED were teamed under Contract F30602-86-C-0261 to RADC/RBRA to develop a reliability prediction model for fielded CMOS VHSIC and VHSIC-like devices. Since little or no field reliability data was available, an approach was taken that used methods which deviated from the traditional statistical analysis of field failure rate data. Two models for predicting failure rates for VHSIC and VHSIC-like CMOS microcircuits were developed: a detailed model and a short form model.

The detailed model is based on the characteristics of specific failure modes, manufactrer specific information such as defect density, wearout performance, and key application data such as temperature and operating time. The short form model is a condensed version of the detailed model and does not require manufacturer specific information, but uses easily accessible information. The penalty in using the short model is its lower precision and accuracy relative to the detailed model.

The models account for both time dependent and defect-related failure mechanisms. A data base was built containing the life test, burn-in, and environmental test results from a variety of manufacturers. Much of the data contained in this data base was used in the quantification of early life failure rates for various specific failure mechanisms. Therefore, the

detailed model, in predicting defect-related early life failure rates, yields an industry wide representative failure rate. The use of actual defect densities, if properly measured, will result in predicted reliability values which are more precise and accurate than conventional regression type prediction models.

It was also determined in this study that it is these defect-related mechanisms that drive failure rate in the part's useful life. Wearout mechanisms were also modeled which will provide an approximate end of lifetime as a function of the part's design rules and its particular application.

The model addresses three time-dependent mechanisms: electromigration, time-dependent dielectric breakdown, and hot carrier effects. The model has factors for chip area, defect density, and/or minimum feature size so that changes in technology can readily be factored in. It has a correction factor to modify the model as VHSIC field experience becomes available and to modify the model for a particular fabrication process based on the availability of high quality life tests. The model can also utilize test pattern data from manufacturers in conjunction with the Yield Enhancement and Generic Qualification programs. There is a package factor which considers the number of package pins and includes the following package types: pin grid arrays, chip carriers, and dual-in-line packages. It also has factors for EOS/ESD and whether or not the device is on the QPL/QML.

The detailed model was validated with life test data that was available on 1.0 and 1.25 micron feature size devices from three separate manufacturing processes and both models were proposed for inclusion in MIL-HDBK-217 "Reliability Prediction of Electronic Equipment." The final report, (Reference 3.43) was circulated via an extensive mailing list. The models were well received and should prove to be very useful DoD/industry tools.

Qualification Procedures

As the VHSIC chips were being designed, developed, and produced, it became increasingly clear that the QPL procedures for qualifying them for military use were not effective and would become even less so as time progressed. Because of their functional complexity, the chips were much more application-specific than the standard logic or standard microprocessor chips used in the past. In addition, the dense, fine-line features of the chips made standard optical inspection and electrical testing ineffective in screening out the faulty or marginal ones. Finally, the cost of qualifying a specific part was sufficiently high that qualification was undertaken only if the part were assured of use in a large procurement. The current status of QPL is given below and the alternative Qualified Manufacturers List (QML) procedures are discussed.

Qualified Parts List (QPL): The present status of manufacturing line and chip qualification, conducted under the Defense Electronic Supply Center (DESC) Qualified Parts List (QPL) guidelines, is described below.

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- o A 1.25 micron (0.9 eff) CMOS 5 V gate array line was certified under MIL-STD-976 and MIL-M-38510, effective December 20, 1989. Included in this certification is the gate array design system, in accordance with the "generic" gate array certification/qualification method of MIL-M-38510/608.

- o The Parametric Monitor (PM) design was approved January 12, 1989 by RADC and DESC.

- o A Standard Evaluation Circuit (SEC) was approved on May 31, 1989 by RADC and DESC. This will serve as the qualification test vehicle, per MIL-M-38510/608 for a gate array family. The family consists of 54k, 28k, 20k and 3k gate arrays.

IBM

- o 620 SPEs were qualified to MIL-M-38510, effective June 1990.

Qualified Manufacturers List (QML): The goal of the QML program is to develop standards more appropriate for qualifying VHSIC chips than the traditional procedures. The new standards are based on establishing qualified manufacturing lines that can produce fully qualified parts without the costly testing of each individual part. Surrogate devices are used for controlling the process and revealing quality problems. CAD tools are fully integrated into the certification procedure and chip families and packaging techniques which apply to more than one device are dealt with generically. This process of "generic" qualification for military products also depends on tight control of the manufacturing process in order to assure that the quality and reliability of the product, once established, remain within required limits.

QML is a long term effort that is expected to continue beyond the VHSIC program . A joint DoD/Semiconductor Industry Association statement announcing this new strategy for military microcircuit manufacturing and procurement was released in February 1989. Ten major semiconductor companies participated in the refinement of the requirements originally developed under a VHSIC contract. These were AT&T, Harris Semiconductor (3 locations), IBM, Intel, LSI Logic, National Semiconductor, Texas Instruments, and VLSI Technologies. The result of this effort, MIL-I-38535 "General Specifications for Integrated Circuits (Microcircuits) Manufacturing", was issued on December 18, 1989. These companies are now in various stages of preparation for certification validation reviews based on the MIL-I-38535 requirements. Certification validation reviews were conducted at AT&T and Intel. The AT&T (Allentown Pa) 1.25 micron CMOS process was certified on December 19, 1989, and

full AT&T qualification was completed during the first quarter 1990. Similarly, Intel certified their 1.0 micron CMOS process in February 1990 and received full qualification shortly thereafter.

Efforts to include linear devices and GaAs technology into the QML concept are continuing. Through the MIMIC program, industry working groups have been established to address the QML requirements for GaAs circuits. Customer generated designs will be addressed in future updates to MIL-I-38535.

0.5 Micron QML: A 24 month modification to the IBM Phase 2 contract was awarded on June 1, 1988 to extend the QML procedures to 0.5 micron technology. The objectives were to (1) develop and implement statistical process control (SPC) techniques; (2) design and implement process control monitors and standar evaluation circuits as in-line process monitors and reliability indicators; (3) develop a reliability prediction model; (4) validate the model lthrough testing; and (5) certify and qualify the 0.5 micron CMOS process for inclusion on a qualified manufacturers list.

IBM has implemented a statistical process control program, as per JEDC Publication 19. A VHSIC/VLSI reliability model was completed and released to the Phase 2 program office. The screening and life test results for both the 1.0 micron and 0.5 micron CMOS signal processing element (SPE) chips matched the model predictions.

3.2.4 Maintenance Concepts for VHSIC

Honeywell performed a study of the impact that advanced microelectronics technology will have on the development of appropriate maintenance concepts. This study identified and characterized the maintainability and diagnostic problems that might occur in advanced microelectronic systems. The guidelines are useful for specifying realistic maintenance requirements and for designing systems to meet those requirements. The guidelines are written for the system, module, and chip levels of assembly and generally provide options for the designer to choose which are most appropriate to the task. They were developed with the knowledge that VHSIC characteristics, such as built-in-test, might mitigate the problem.

System level guidelines include a discussion of maintainability as a primary system requirement, equal in importance to the mission requirements of that system. Diagnostic information management, packaging, fault diagnosis techniques, and VHSIC-1 and VHSIC-2 maintainability features are discussed.

Module level guidelines cover the electrical and mechanical characteristics associated with the maintenance features and the use of built-in test and automatic test equipment. The role of the module level diagnostics as a link between chip and system processes is stressed.

Chip level guidelines focus on methods used in the design of chips to implement a hierarchy of maintenance diagnosis throughout the system.

Particular insight is provided into the techniques of good design for maintenance and the tradeoff between the level of maintainability achievable and its associated cost. Several

appendices, which contain detailed examples of diagnostic techniques, are included in the final report for this project (Reference 3.44).

3.3 Chip Fabrication

The following assessment of the impact of VHSIC on fabrication technology has been contributed by one of the program managers intimately involved in the development of the Phase 2 VHSIC "superchips" which successfully pushed the prototype production of high density, large area, one-half micron silicon fabrication technology to its limits.

The Impact of VHSIC on Fabrication Technology

Charles S. Meyer
Motorola

My involvement with the VHSIC Program started at its beginning in 1979. I helped prepare our Phase 0 proposal with teammates TRW and Sperry Univac, and I continued to work on the Program throughout Phase 1. I rejoined the TRW/Motorola effort as Motorola's Program Manager during the last two years of Phase 2 when it returned to our Advanced Products Research and Development Laboratory (APRDL).

What has been the impact of VHSIC on microcircuit fabrication technology? It is my opinion that it has served as a significant accelerating factor in our progression to successively denser integrated circuit generations.

The thrust of VHSIC technology was intended by the Government to be leading–edge in nature but firmly positioned in the mainstream of projected integrated circuit fabrication trends. This was true in Motorola's case because process/device development at both the 1.25 micron (Phase 1) and 0.5 micron (Phase 2) CMOS technology levels was planned and would have occurred without VHSIC. Even with VHSIC, Motorola paid for the process development activities itself. However, the Program provided us with the opportunity and funding to exercise these processes on real circuits earlier than would have otherwise been the case and to do this with schedule demands that forced the hard decisions necessary for yield enhancement.

An example from our Phase 1 experience was the use of polycide (the gate electrode material comprised of a sandwich of a polysilicon and low resistance silicide). We had developed the polycide process module and used it on a prototype commercial memory chip before employing it on our VHSIC circuit. The VHSIC design, in turn, arrived somewhat ahead of a commercial microprocessor part that was also scheduled to use polycide. This microprocessor's topography was closer to that of the VHSIC circuit than the memory and thus we got a jump start on exercising the polycide module in a "logic" process. Both circuits benefitted, I think, from subsequently being run in parallel.

In the case of Phase 2, we have concluded that the presence of VHSIC in APRDL accelerated our progress on 0.5 micron technology by almost a year. We had to redirect our internal resources to meeting the incredibly challenging demands involved in assembling a 0.5 micron, salicided–transistor, triple–level–metal

technology and successfully using it to fabricate 1.5 x 1.6 inch dice. Motorola's planned purchase of a high numerical aperture stepper had to be expedited and mastery of the equipment was accelerated by the need to perform optical stitching. Again, although this developmental work was funded by our company, the VHSIC time schedules forced us to "make way" sooner for this generation of technology and also provided the circuit vehicles to exercise it and measure progress. This 0.5 micron technology is being transferred to TRW under a separate contract for continued application to the Government projects.

From a more global perspective, apart from the hardware aspects, I feel that VHSIC has accomplished another important mission by facilitating the interaction between semiconductor technologists and military electronic equipment designers. As a result of this program, each has a better understanding of the other's capabilities and limitations. It is my expectation that success in future applications will show this to have been a major benefit of VHSIC.

3.3.1 1.25 Micron (Phase 1 and Yield Enhancement)

Introduction

The six contractors used several different fabrication technologies and each had different baseline processes. Thus, although there were some common problems, for the most part each contractor had to overcome a different set of obstacles. In every case, these processing difficulties were overcome and chips were successfully produced.

The fabrication goal of the VHSIC program was to develop a process which could produce complex 1.25 micron chips at a 10% or greater packaged yield so as to be affordable for use in military equipment. The process was to be well characterized and controlled so as to produce consistent yields. The chips were required to be very reliable in the hostile environments experienced in battlefield conditions.

For many of the Phase 1 chips, these targets could not be reached initially. Therefore, a Yield Enhancement effort was undertaken as an addition to each of the Phase 1 contracts. The goal was to center the process parameters to maximize yield and reproducibility. A target value for the yield of packaged chips was set at 10%. The yield inhibitors had to be identified and corrected by changing the manufacturing process. Progress toward the stated goal was measured by periodically running three consecutive lots nominally consisting of 20 wafers each. These three lots were collectively termed a Yield Verification Run (YVR). Yield at various points in the process was measured and compared to interim goals. The yield inhibitors were identified and listed in their importance to yield loss. This determined the areas on which the work concentrated during the next period. Summaries for each contractor's yield enhancement program are included below. Further details can be found in Reference 2.27.

Honeywell

Honeywell used an advanced digital bipolar (ADB III) fabrication process throughout the Phase 1 and Yield Enhancement programs. It is based on dielectric isolation, an ion implanted buried collector layer with sheet resistance 3 to 5 times lower than the original polysilicon buried layer process, and three layers of metalization for interconnections.

Maintaining a semi-planar oxide dielectric process greatly improved the integrity of the metal interconnection layers. Metalization coverage over "steps" in the underlaying insulator layer was enhanced by sloping the walls of the vias with a well controlled etching process. Buried-layer to buried-layer current leakage was reduced by modifying the KOH etch depth and by routinely monitoring the autodoping from the heavily doped buried layer. The standard dielectric process was replaced by a bias sputtered quartz process to improve planarization for better metal step coverage and to reduce metal streamers during the etch cycles.

A serious problem manifested itself in the form of severe crystal defects in the emitter structure of the bipolar device after the emitter anneal. These defects were traced to an effect by the ion implanter. The problem was eliminated by replacing the arsenic pentafluoride source gas with arsine source gas.

Variations in metal line width resulted from reflections from the surfaces during mask alignment. An anti-reflective coating of polyimide/dye was developed to solve this problem. This process also helped to reduce particle contamination and to improve the cycle time.

All of these process improvements led to a defect density in the VHSIC pilot line low enough to allow the fabrication of fully functional brassboard chips. However, even though the process could produce fully functional chips, the yield was below the target package yield of 10%.

At the beginning of the Yield Enhancement effort (1984) the major yield inhibitors were, in order of decreasing severity:

1. Collector-to-emitter "pipes"
2. Schottky diode leakage
3. Particulates in the equipment environment

By April 1986, the corresponding list was:

1. Particulates
2. Handling/edge defects
3. Interlayer metal shorts
4. Metal "streamers"
5. Pipes

As can be seen, two years of concentrated effort on the problem of pipes pushed it to the bottom of the list. As with most of the problems, the pipes were never totally eliminated but

reduced in density to a point that permitted significant yield improvements. The inhibitors were attacked one at a time until all were under control.

The manifestation of the pipe problem was collector-emitter (C-E) leakage. It dominated the inhibitor list for the first year of the program. The causes ranged from silicon suface roughness, after the KOH etch, to metallic contamination from the stainless steel spinner chucks and tweezers. Changing the KOH process, modifying the pre-epitaxial wafer scrub, and substituting delrin for the stainless steel resulted in a yield increase from 2% to 28%. Since a pre-epitaxial brush scrub left scratches on the wafers, a high pressure scrub was instituted to lower the defect density. Changing from intrinsic to extrinsic gettering also played a significant role in decreasing the density of pipes.

The problem with Schottky diode leakage was not the absolute value of leakage current but its variability. The problem was traced to the dry etch process. Process-induced fluorocarbon and metallic contamination, along with lattice damage, became worse during over-etching. To solve this problem, over-etch was reduced from 25% to 10% and the tooling in the etcher was coated to reduce alkali metal contamination. Changes to the palladium sputter deposit process were also instituted, which further reduced metallic contamination and limited lattice damage to the rear surface region. A subsequent dry etch of 50 A of silicon removed the problem of leakage variability.

The particulate problems remain on-going ones that are solved by constant attention to wafer handling, periodic maintenance, and upgrading of equipment or procedures. The solutions are evolutionary.

The final Honeywell ADB III process was shown to be capable and stable. Although not all of the problems encountered along the way were totally understood or eliminated, in every case a solution was implemented that allowed the processing to continue and the program objectives to be achieved (Reference 2.11).

The sequencer chip was used as the vehicle for the YVRs. The best lot in 1985 had a 14% probe yield. After several process improvements and simplifications were made in early 1986, the best probe yield achieved was 25%. The last YVR was on a sequencer redesigned in current mode logic technology, processed on 6-inch wafers at the Colorado Springs facility in 1987.

Hughes

The baseline process used 3-inch diameter silicon-on-sapphire (SOS) wafers. This starting material was an intrinsic silicon film, 0.5 micron thick, with a (100) surface orientation grown on a sapphire substrate. The device fabrication process flow is shown in Figure 3.3. After patterning, the silicon islands were defined by reactive ion etching to give an almost vertical edge profile.

The p- and n-channel regions were selectively implanted with both shallow and deep implants to provide the targeted MOS transistor threshold voltage, reduce back-channel leakages, and increase punch-through voltage. A 400 A radiation hard, wet-gate oxide was then grown at 850°C. This was followed by depositing 2500 A of polysilicon, which was then

1. MARK LAYERS

2. SI ISLAND MASK/ETCH
3. P-MASK/IMPLANT
4. N-MASK/IMPLANT

5. GATE OXIDE
6. POLY/$TaSi_2$ DEPOSITION

7. WINDOW MASK
8. POLY MASK/ETCH

9. WINDOW MASK
10. P+ MASK/IMPLANT
11. N+ MASK/IMPLANT

12. SILOX DEPOSITION
13. WINDOW MASK
14. CONTACT MASK/ETCH

15. AL/1% SI SPUTTER
16. WINDOW MASK
17. METAL MASK/ETCH

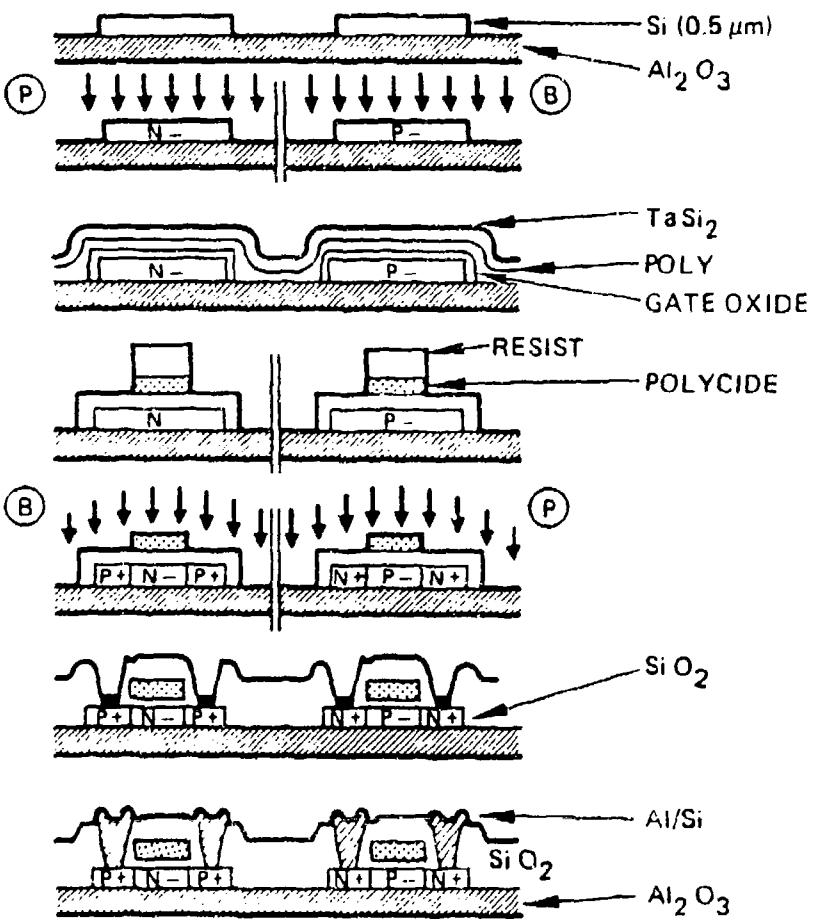


Figure 3.3 SOS-III VHSIC Phase 1 Fabrication Process (Hughes)

doped with phosphorous using $POCl_3$. A 3000 A thick film of tantalum silicide was deposited on top of the polysilicon and annealed at 850 °C in an argon atmosphere. This provided a resistivity of approximately 3 ohms per square for gate interconnects.

A single layer photoresist process was used to define uniform gate linewidths. The tantalum silicide gate layer was etched, then the p- and n-channel source-drain regions were selectively implanted with a thin layer of aluminum. Low pressure chemical vapor deposition (LPCVD) oxide was then deposited and annealed to provide isolation between the metal and gate interconnect layers. Annealing was performed at a low temperature to minimize the lateral diffusion of impurities under the gate region.

The contact regions were patterned and defined by dry plasma etching, followed by plasma ashing in oxygen to remove any polymer formed in the contact regions. Aluminum/silicon metal was sputtered on the wafers, patterned on a photo aligner, and etched before cleaning and annealing. The final process step (not shown in Figure 3.3) consisted of a standard protective glass deposition followed by patterning and etching to clear the bonding pads (Reference 2.12).

Eight Yield Verification Runs were processed on the correlator chip and subjected to extensive in-process and test analysis to monitor the progress of the yield enhancement program. Three key factors were used to measure the yield: the percentage of wafers that survived fabrication (throughput), electrical parameter characterization of test structures on a wafer (parametric), and functional wafer probe yield (functional). Although the throughput yield improved from three scrapped lots in 1985 to no scrapped lots in 1986, both the parametric and functional yields were highly erratic and uncorrelated. The best lot had a functional yield of 12%. During the course of the program, two test chips were used to measure metal and polycide bridging, continuity failures, gate shorts, and open contacts. Several process and manufacturing improvements were made (Reference 2.12).

IBM

During Phase 1, IBM transferred a 1.25 micron, n-channel, metal oxide, silicon (NMOS) process that was under development at the IBM Burlington, VT Laboratory to the Federal Systems Division manufacturing/pilot line facility in Manassas, VA. The basic features of this process were as follows:

- recessed oxide (ROX) for isolation between field effect transistor (FET) devices,
- insulated gate FET devices, provided in a menu of three different threshold voltage levels, to optimize circuit density, speed, and power (This enabled fabrication of devices operating in three different modes: enhancement, regular depletion, and weak depletion.),
- low resistance polysilicide for gate electrodes and short wiring runs, and
- two levels of electromigration-resistant metal wiring (aluminum-copper silicon) for intracircuit and global signal/power connections.

During the early phase of the project (October 1982 to June 1983), two major yield detractors were identified: contact resistance and erratic adhesion of the WSi_x polysilicide layer. The contact resistance problem was found to be caused by an unwanted polymer layer formed from the CF_4-H_2 gas mixture used in the reactive ion etch (RIE) process that occurred at low SiO_2 etch rates. The etch rate was increased by an optimal choice of power density, mass flow rate, and H_2 concentration during RIE. The etch rate was also found to be sensitive to the number of product wafers in a batch as the aluminum cathode was consumed. The problem was solved by incorporating an organic material as a cathode coating and subsequently optimizing the process parameters.

The major cause of the erratic WSi_x adhesion was identified as the $POCl_3$ technique used to dope the polysilicon layer. It resulted in the production of an interface SiO_2 layer during the WSi_x anneal. This increased the film stress and delaminated the WSi_x layer. The problem was solved by incorporating a 150A, conformal, polysilicon layer deposited immediately prior to the source-drain oxidation.

In the final phase of the project (June 1983 to March 1984), after completion of the first-pass fabrication of the Complex Multiply Accumulate (CMAC) chip, the major yield detractors were identified as input and reverse bias leakages. The problem was traced to a wet etch which attacked the gate oxide immediately underneath the polysilicide electrode. This subsequently led to a poor quality, wedge-shaped SiO_2 region underneath the polysilicide conductor causing significant leakage currents. The solution was to eliminate the wet etch entirely. A second component of the problem was poor step coverage for the first metal interconnect caused by inappropriate topography of the phospho-silicate glass (PSG) planarization. This problem was solved by changing the composition of the PSG layer (Reference 2.13).

The various process modifications described above allowed the 1.25-micron process to be successfully transferred to Manassas. Fully functional VHSIC CMAC chips were produced from both Pass 1 and Pass 2 design mask sets (Reference 2.13).

The yield enhancement program at IBM identified the key problems as metalization defects and polysilicide-to-substrate leakage. Both the CMAC and the SPE chips were used as YVR vehicles. After transfer of a new base line process from Yorktown to Manassas and further process improvements, the best CMAC lot had a probe yield of 8% while the best SPE achieved a yield of 42%.

Texas Instruments

Two technologies were developed to fabricate the Phase 1 ICs. The SRAM was implemented in an n-channel metal oxide semiconductor (NMOS) technology and the other devices were implemented in a bipolar Schottky transistor logic (STL) technology (Reference 2.14).

STL Process: STL is an IC design technology that uses an npn transistor, a base resistor, and two types of diodes to form a logic gate. The base-to-collector junction

of the npn transistor is clamped with a high barrier voltage Schottky diode. The connection from the collector of one gate to the base of the other is made through a low barrier voltage Schottky diode. In the process developed for Phase 1, the low barrier diode was fabricated in the collector areas using titanium-tungsten (TiW). The high barrier diode was fabricated between the collector and base area using platinum-silicide (PtSi).

The 1.25 micron STL process used eighteen mask levels. The levels define a process that included poly emitters, high and low barrier Schottky diodes, and triple-level metal. The processing sequence consisted of the following major steps:

- Buried collector process. The buried collector is necessary to lower the parasitic collector resistance of the npn transistor and to lower the gain of the parasitic substrate pnp transistor. An anneal step consumes some silicon over the n^+ regions and allows subsequent alignment to the buried collector.
- Epitaxy/nitride process. An included oxide layer serves as a pad to relieve stress between the nitride and the silicon.
- Oxide isolation process. To minimize the "bird's head" effect that forms when nitride masking is used for selective oxidation, the depth of the silicon etch and the thickness of the field oxide are chosen so that a thin layer of epitaxial n-type silicon connects the active region tanks. A channel stop later in the process is required to interrupt this leakage path.
- Boron implant for the transistor base, resistor, and channel stop formation processes. Photoresist is used as an implant mask in all cases.
- A deep n^+ diffusion connects the buried collector to the surface.
- Polysilicon emitter process. The implant does not penetrate the polysilicon, and the shallow emitter is formed by arsenic diffusing from the polysilicon into the silicon during the anneal cycle.
- Extrinsic base and resistor head formation. Substrate contacts are also made at this level by putting a p^+ region in a tank that also has the channel stop implant but does not have the buried collector layer.
- Contacts to the p-regions. PtSi forms the high barrier Schottky clamp where it makes contact to the n-type epitaxial region. It forms an ohmic contact to the p^+ regions and to the polysilicon.
- Contact oxide removal process. The contacts are opened for the logic diodes to be formed.
- Second and third level of metal with insulating layers of plasma oxide.

NMOS Process: An n-channel metal oxide semiconductor (NMOS) process was selected for the VHSIC 72k static RAM (SRAM). The process has four transistor types, single l[illegible] metal, and silicided polysilicon. Buried contacts are available to use polysilicon fo[illegible]cal interconnect. The major steps in this process were as follows:

- o Buried n^{++}. This mask level primarily defines the "Self Aligned Thick Oxide" subthreshold load transistors used in the memory array.
- o Gate oxide. The thin (250 A) gate oxide needed to permit IC operation at high speeds required special precautions in order to prevent contamination and avoid damaging electric fields during subsequent processing steps.
- o Buried contacts. This is needed to increase the SRAM cell packing density.
- o Gate channel length sizing control to achieve specified 40 ns access time.
- o Lightly doped drain structure. This is used to minimize short channels and the effects of hot electrons.
- o Silicided gates and junctions. $TiSi_2$ is used to obtain the lower resistivity needed for high speed.
- o Multilevel oxide contacts. The use of a two step dry contact etch process with furnace reflow of boron phosphosilicate glass in between is needed for the small contacts. The remaining traces of $TiSi_2$ would be removed by the standard wet etch process.

During 1985, the yield enhancement program focused on improving the front end process steps and isolating the yield loss mechanisms for both the NMOS and STL processes. The result of these efforts succeeded in surpassing the yield goals for each of the chip designs.

TRW

TRW fabricated seven bipolar parts designed with 1.0 micron design rules. In addition, a memory chip designed to 1.25 micron rules was fabricated in CMOS by Motorola, under subcontract to TRW.

Bipolar Process: The VHSIC bipolar process provided the following enhancements to an existing 1.0 micron bipolar process:

- o Arsenic implanted silicon for resistors.
- o A double level metalization system that included improvements to etching of Metal 1 sputtered Al(Cu) films (reactive ion etching) and to SiO_2 deposition between Metal 1 and Metal 2 layers (polyimide wet etch and plasma chemical vapor deposition).
- o Low temperature processing.
- o Computer aided manufacturing system for process and product control.

During the early years of the program (1982-83), several processing problems arose. Among them were oxide islands after Level 1 RIE, low yield on emitter windows, imperfect TiW etching and resist adhesion. These, however, did not prevent TRW from producing the first fully functional chip of the VHSIC program --- the

matrix switch --- in February 1983. By July 1984, four of the eight chip types had been tested to be fully functional.

In late 1984, the only substantial processing difficulty remaining was in etching the TiW layer of the Metal 1 film. In turn, this obstacle was also systematically eliminated leaving throughput as an issue to be addressed. A 1:1 projection stepper was installed in the pilot line, replacing a 10:1 reduction stepper that had required over eight hours for setup and reticle verification per exposure level. By January 1985, all eight chips (including the Motorola 4-port memory) had been successfully fabricated.

CMOS Process: A 1.25 micron CMOS process was developed, under subcontract to Motorola, to fabricate a four-port memory chip. The basic process, established in February 1982, consisted of bulk CMOS with p-wells, 1.25 micron polysilicon gates and dry etching employed on all critical layers. The capabilities to be added to the baseline process were initially planned as:

- o Refractory metal silicide ($TiSi_2$) shunts on the polysilicon to reduce resistance and thereby increase the operating speed of the chip.
- o Buried contacts from polysilicon to the n^+ diffusion layer to increase the layout circuit density.
- o A third layer of interconnect.

In October 1983, it was decided to use WSi_2 instead of $TiSi_2$ as the shunt material. Although the tungsten silicide has a higher average sheet resistance than the titanium silicide, it was found that internal stress caused by microcracks in the titanium silicide lines gave rise to a much higher actual line resistance. Erratic behavior of several related device parameters observed in 1983 were eliminated by the changeover to the tungsten silicide, changing the n^+ poly doping technique from ion-implanted arsenic to PH_3 gas diffusion, and modification of subsequent heat cycles parameters.

By October 1984, process modifications were complete and life tests showed that the four-port memory was capable of an equivalent of $2x10^7$ device hours of operation, exceeding the failure rate goal of 0.006%/1000 hours. Further design changes were made under the Yield Enhancement program to improve the circuit speed performance.

TRW designated the CAM chip as its YVR vehicle for its bipolar process, while subcontractor Motorola used the 4-port memory chip. The best probe yield at the wafer level for the CAM was 10%. After the 4-port yield inhibitor was identified as particles and after subsequent equipment and process improvements were made, the wafer probe yield improved to 15%.

Westinghouse

The VHSIC baseline process established at National Semiconductor Corporation (NSC) was CMOS. It was an n-well process with the well implanted into a 5-7 ohm-cm, p-type epi-layer. The well used a high energy phosphorous implant driven to a depth of 2.0 microns. A nitride (Si_3N_4) masked selective oxidation process was used for lateral isolation. A p-type field implant was added after the oxide was grown to prevent field inversion. Boron was implanted prior to gate oxidation to adjust the threshold. The gate oxide was 200 A thick. Tight control was maintained over this thickness. The gate electrode material was $POCl_3$ - doped polysilicon. The polysilicon was imaged using positive resist with a contrast enhancement layer. This process maintained excellent control over the imaging of 1.0 micron gates which were delineated by plasma etching. This process used chlorine chemistry with excellent etching selectivity of polysilicon to oxide (66:1). The etch was completely anisotropic giving etched gate lengths of 1.0 micron (0.8 micron L_{eff}).

Source/drain junctions were doped by ion implantation of BF_2 for p-channel devices and arsenic ions for n-channel devices. The junction depths were 0.25 micron. The contact resistances for these shallow junctions were minimized by selecting platinum silicide (PtSi) as the contact metallurgy.

The first dielectric layer, between gate and metal 1, was silicon oxide deposited at 900°C. After the 1.25 micron contacts were imaged, etched, and silicided, the first metal layer was deposited on the oxide and patterned. The second dielectric, (between metal 1 and metal 2) was a sandwich composed of a layer of phosphorus doped plasma oxide followed by a film of bias-sputtered quartz (BSQ) and capped by phosphorus doped plasma oxide. The BSQ profile was controlled by tailoring the bias voltage during the deposition cycle. This profile provided partial planarization to preclude metal 2 step coverage problems. Finally, 1.25 micron vias were opened and the top layer of metal interconnect was deposited.

Metal 1 and metal 2 were both sandwich structures made up of a titanium-tungsten (Ti-W) layer, a layer of aluminum deposited with 1% silicon, 0.5 micron for metal 1 and 0.8 micron for metal 2, and a thin top layer of Ti-W to serve as an anti-reflection coating which aided the lithography process. The minimum line-to-line metal pitch was 3.0 microns including contact and via pads.

A 0.5 micron thick boro-phospho-silicate glass (BPSG) on 0.12 micron nitride was developed as an alternative first layer dielectric where greater planarization became a necessity. The use of BPSG increased the process latitude in the metal 1 linewidth by 0.25 micron over the baseline process as measured by product yields. Yields for the baseline process were similar to those obtained with BPSG.

Intermittent cracking in the dielectric second layer was eliminated by modifying the heat cycle of the plasma oxide deposition and improving the uniformity of the dopant concentration.

During the Yield Enhancement effort, 41,600 defect-free 16k SRAMs, 9775 defect-free 64k SRAMs, 800 functional gate arrays, and 8 functional 30k gate custom chips were produced. The yield improvement over the period was more than a factor of 10 at the wafer

probe level. The highest lot yield for the 16k SRAM was 73%, and for the 64k SRAM was 25%. The net defect density typically ranged from 6 to 12 defects per square centimeter.

In summary, a CMOS baseline process established at NSC was improved through the Yield Enhancement program to exceed the VHSIC program yield objectives. 64k SRAM yields grew from 1% to 25%, and gate array yields grew from 0.5% to 10% during the course of the program. NSC's VHSIC production foundry was the first to receive DESC certification. A similar VHSIC baseline process was also established at Westinghouse Advanced Technology Laboratory (Reference 2.15).

3.3.2 0.5 Micron (Phase 2)

Introduction

The fabrication of devices with 0.5 micron minimum feature sizes presented a unique challenge to each of the three contractors and required new processes and fabrication tools. These processes and many of the problems that were encountered are described below. Ultimately, all three programs were completely successful, resulting in the manufacture of integrated circuits that reached new levels of functionality and performance.

Honeywell

It was decided to use electron beam lithography only where needed and optical lithography elsewhere. This mix and match scheme allowed the highest possible processing throughput. The technology used was current mode logic (CML) with trench isolation and four levels of metal. The lower levels used e-beam lithography and the upper levels optical lithography. The major effort, in the initial stages of this development, was on the four-level metal process. The most critical initial task was dielectric deposition and planarization. The planarization process took the form of a conformal coating of oxide which was etched back to expose the metal interconnect pads. To reduce the complexity of this process, it was decided to define the metal by removing a narrow border around the interconnect, leaving most of the metal between the interconnect. This would mean that the surface would be flat everywhere except in the borders. The oxide would be used to planarize this small part. The problems that arose from the use of this scheme were increased capacitance and slower performance, so the technique was subsequently abandoned.

Initially, the groove process appeared to be under good control. It was later found that the groove etch was the leading cause of collector-to-collector leakage. If the groove bottom was shaped improperly, stress would build up along the bottom edge causing crystal defects in the adjacent material. These defects would be the leakage paths between the collectors. About this same time, the JEOL e-beam machines used to define the grooves developed problems which affected the process schedules and which continued throughout the year.

During 1987, work continued on the groove isolation process, but the need for a process to form the interlayer metal connections (vias) took precedence. A decision was made to pursue the development of a blanket tungsten via fill process. During this period, optically defined grooves were shown to meet the pre-etch specification of 1.2 $\pm$ 0.1 microns and post etch specification of 1.1 $\pm$ 0.15 microns. This process replaced the e-beam for the groove lithography. Since optical lithography had greater throughput than e-beam this change helped reduce the cycle time.

The effort on planarization initially used bias sputtered quartz (BSQ), but investigations quickly revealed that the effectiveness of this method over very dense areas was degraded. This prompted a study of boro-silicate glass (BSG) for planarization. The test runs showed a dramatic improvement in the densely populated areas and results equivalent to BSQ in less populated areas. The adhesion of BSQ to BSG was the only area of doubt. After some experimentation, this question was resolved and a process was instituted in which improved the adhesion. The implementation of a new photoresist plug process significantly increased yield of the dielectric layers. The yield was such that dielectric leakage was no longer a yield inhibitor. This process also enhanced the planarization for the upper metal layers.

The third most serious yield inhibitor in this period was short circuits between metal lines. This problem was traced to the pre-metal high pressure scrub. This was replaced by the more effective brush scrub which totally solved the metal short problem.

The final problem was collector-emitter leakage. The following steps were implemented or changed to solve this problem: polysilicon backside gettered starting material, 0.1% oxygen emitter-drive ambient, increased groove-emitter space, increased groove sacrificial oxidation temperature, and removal of the reactive ion etch damage caused by the plasma planarization etchback.

All of these improvements allowed a fully functional BIU to be fabricated by the third quarter of 1988. The first fully functional Array Process Controller (APC) was demonstrated in April 1989. Further improvement of the metalization processing resulted in reduced levels of collector-emitter leakage, reduction in power supply shorts, and elimination of non-conductive vias --- all of which made possible the production of functional APCs and APUs. The non-conductive via problem was solved by increasing the thickness of the TiW anti-reflective coating from 300 A to 1500 A.

Due to a minor layout error, however, one of the resistors in the RAM interface cell of the APU was higher than the design value which limited the speed of the chip to less than the 100 MHz speed specification. But enough fully functional APC and APU chips were fabricated to satisfy the needs of the cruise missile guidance system brassboard.

With these deliveries, the process was shown to be capable of fabricating fully functional chips and, with the correction of the resistor problem, chips that will run at full speed.

In summary, the program goals to demonstrate a wafer fabrication process that could produce VHSIC circuits at yields sufficient to make the device affordable and reliable, were met. The final design used 0.5 micron minimum geometries and four levels of metal interconnect. The process was demonstrated with the fabrication and delivery of APC/APU

chips that were fully functional and operated at speeds sufficient to accomplish the tasks assigned them.

IBM

The IBM approach to VHSIC Phase 2 was to develop a 1.0 micron CMOS technology, which was then scaled to 0.5 micron. Process development for VHSIC CMOS device fabrication had been underway since 1983. These efforts included development of a 1.0 micron CMOS technology at IBM Burlington and a fully scaled 0.5 micron CMOS technology at IBM Research. In 1984, IBM began a coordinated company effort to transfer these processes to the Manassas VLSI pilot line facility.

Baseline Process: Key features of the partially scaled 0.5 micron CMOS technology are presented in the Table 3.1, with details in Reference 3.45.

The silicon wafers used in Phase 2 processing were 100 mm diameter p-type substrates from Monsanto. An epitaxial p^+ layer with boron doping of 1.0 E16 per cm^3 $\pm$ 20 percent was used. Careful evaluation of materials properties of starting epitaxial substrates from three vendors resulted in selection of this starting material. The boron doping density in the epilayer of Monsanto substrates had to be adjusted with a boron ion implant to achieve acceptable threshhold voltage characteristics for n- and p-channel devices. The resulting characteristics of optimized devices with 0.4 micron channel length were in good agreement with device model predictions and short channel effects could be eliminated.

The vertical profile supported 0.5 micron CMOS devices with 0.5 micron polysilicon gates formed with electron beam lithography. The remaining dimensions were patterned to 1.0 micron or greater with optical lithography. This approach guaranteed 0.5 micron speed performance and yet retained the greater maturity of the 1.0 micron chip manufacturing process.

Processing at the front end of the line (starting substrates to first level metal) included seven optical levels and one e-beam lithography level. An additional optical level for the buried contact was an optional feature. All ion implants, depositions by evaporation or CVD, all hot oxidations, and reactive ion etching steps were part of this process. Full capability for exercising all front end processing steps was established in the Manassas VLSI pilot line. Changes in the process flow could be implemented, such as the elimination of the TN photolevel, because of experience gained with fabrication of early test site hardware.

Back end of the line processing (everything after first metal) involved eight photolevels. These photolevels supported three wiring levels of aluminum/copper and pad transfer metalization for area array interconnects. Evaporations and insulator depositions as well as reactive ion etching for BEOL processing were also part of this sequence.

Table 3.1 IBM 0.5 Micron CMOS Technology Features

FEATURE	TYPE	TECHNOLOGY LEVERAGE
Substrate	p^- Epi on p^+ Substrate	Radiation/Latch-up Immunity
Well Structure	Retrograde-Doped n-type	Radiation/Circuit Density/ Latch-up Immunity
Isolation	Improved Local Oxidation	Radiation/Yield Density
Polysilicon Gate	n^+ (Salicided) Anisotropic RIE	Device Performance/Yield
Gate Oxide	12.5 nm	Reliability/Radiation
Power Supply	3.3 V $\pm$ 5%	Systems Compatibility
Lithography	Mixed Optical/E-Beam	Manufacturability, Performance
Minimum Feature Size	0.5 μm/1.0 μm	Density/Performance
Overlay	0.15 μm/0.45 μm	Registration Accuracy
Dic Size Junctions	$(5.5\ mm)^2$ to $(8.0\ mm)^2$	Manufacturability, Cost, Yield
n^+	0.2 μm As (Salicided)	Salicide Compatibility
p^+	0.2 μm B (Salicided)	Salicide Compatibility
Salicide	$TiSi_2$ (0.065 μm)	Device Performance
Passivation	Low Temperature Oxide/ Phosphosilicate Glass	Reliability
Contact Barrier	Ti/W or Ti	Reliability/Contact Resistance
Wiring Metalization	Three-Level Al/Cu	High Density
I/O-Count	220/Area Array Interconnects	High I/O-Count/Multichip Packaging/Reliability

Enhanced Process: Two levels of radiation hardness were specified in the program; a required, baseline level and a preferred, enhanced level (see Section 3.3.3). Tests of devices fabricated with the baseline process indicated that it exceeded all the radiation requirements and the enhanced requirements for transient upset, survivability, latch-up, and neutron fluence. Areas that required improvement in order to meet the enhanced requirements were identified as total dose and single event upset (SEU).

Total dose enhancement concentrated on hardening the gate oxide and field oxide including the "bird's beak" transition region. This was accomplished by a classified process that was independent of the chip design and proved successful as demonstrated by radiation testing. Polysilicon stringers were observed on initial test chips. These were eliminated by modifying the polysilicon RIE etching. The Phase 2 chip set was fabricated simultaneously in the baseline and enhanced processes. Since no first order impact on yield, cost, performance, or reliability was detected the enhanced Phase 2 process was adopted as the primary process.

To facilitate the design of static RAM (SRAM) cells with SEU protection, a second level of polysilicon was used for decoupling resistors and cell wiring in hardened SRAM designs. The process was tested on 4k x 9 memory arrays.

The performance and radiation hardening specifications were successfully met. Twelve split lots of Phase 2 product chips were successfully processed with both the baseline and enhanced 0.5 micron CMOS process versions. The 0.5 micron devices survived 30 Mrad(Si) total dose exposure without any functional failure and with minimal impact to worst case performance.

The overall processing flow, vertical device profiles, and other details of the enhanced process are given in Reference 3.45.

TRW

The original program plan called for TRW to produce superchips in a 0.5 micron, radiation hardened, bipolar technology based on modifying the Phase 1 triply diffused process; Motorola was to fabricate the same designs in CMOS. The TRW enhancements were to include a self-aligned polyemitter, trench isolation, ion implanted arsenic resistors, and triple level metal. The process required a total of 13 mask levels, all of which would be defined by e-beam lithography.

During 1985, TRW experienced inconsistent results with the e-beam version of the polyemitter process. There were also problems with some of the interlayer dielectric materials. Poor device parameters were obtained on test chips and other problems with the triple level metal system appeared. Furthermore, delays in delivery of the high throughput AEBLE-150 e-beam machine (see Section 3.3.4) forced the use of low throughput e-beam machines so that the slow gathering of experimental data slowed the progress of development.

Meanwhile, Motorola was proceeding with the development of a submicron CMOS process based initially on using p-/p epitaxial wafers, trench isolation, 150 A gate oxide and

polysilicon gates. Sidewall oxide was to be used for source and drain definition, partial planarization for first metal, and oxide planarization for second metal.

Early in 1987, a decision was made to discontinue the bipolar effort at TRW and to continue developing the CMOS process at Motorola. It was decided to first fabricate all macrocells to 0.8 micron design rules and then produce a CPUAX superchip (Section 3.4.2) in 0.5 micron geometry.

Motorola also had planned to use e-beam lithography, but when their AEBLE-150 machine was finally delivered they found that the overlay accuracy was inadequate. They then changed to all optical lithography with a step-and-repeat machine employing a high numerical aperture G-line (later I-line) lens.

The 0.5 micron processing was extremely challenging, especially the lithography which required 135 mask sets for the superchip. The final results were very successful; eleven macrocells were individually produced in 0.8 micron geometry and two in 0.5 micron geometry. A 0.5 micron BIU chip with 35k active devices and the CPUAX superchip with all the macrocells in 0.5 micron geometry were also produced, the latter containing a total of 4.1 million devices. The CPUAX and BIU were successfully demonstrated functioning as a programmable signal processor in December 1989.

3.3.3 Radiation Hardening - James J. McGarrity, Harry Diamond Laboratories

The Defense Nuclear Agency (DNA) administered a follow-on effort to the VHSIC Phase 1 program (Reference 3.46) that was designed to improve the capability of selected Phase 1 technologies to meet DoD's requirements for hardness to ionizing radiation in space. These space requirements are:

Neutron fluence	1E12 n/cm^2
Total ionizing dose	2E5 rads(Si)
Dose rate/upset	1E10 rads(Si)/s
Dose rate/survivability	1E12 rads(Si)/s
Single event upset	1E-10 upsets/bit-day
Latchup	none

The work was initiated between 1984 and 1986 via DNA awards to eight contractor/subcontractor teams. These efforts involved process development and/or circuit design, layout, fabrication, and characterization as appropriate to each particular hardening task. The areas of concern during the program were total dose (TD), dose rate/upset, latchup (LU), and single-event upset (SEU). The neutron hardness and dose rate/survivability of the Phase 1 technologies were considered to be adequate and were not specifically addressed.

Considerable progress was made in this area by developing new radiation resistant fabrication processes and transistor designs and by implementing innovative, device-level schemes. The DoD requirements were not only met, but in some cases were exceeded. The IBM work on Phase 2 radiation hardening is discussed in Section 3.3.2.

Westinghouse

A contract was initiated with Westinghouse (prime contractor) and National Semiconductor Corporation (NSC) to develop radiation-hardened versions of the 64k SRAM and the 10k gate array which they designed and produced in CMOS during the Phase 1 program.

Total dose hardness of the baseline process was limited largely by n-transistor leakage current brought on by positive charge buildup in the field oxide. The approach to hardening was to implement a self-aligned field edge (SAFE) implant of boron prior to oxidation to prevent charge inversion and thus cut off source-drain leakage paths. This step was later augmented in the gate array with a modest layout revision that recessed the n^+ source-drain regions away from the "bird's beak" edge of the field oxide. The combination of the SAFE implant plus the recessed n^+ yielded a gate array design capable of functioning up to the megarad level (Reference 3.47).

The latchup problem that was experienced initially with the baseline process (Reference 3.46) was eliminated by converting to substrates which used epitaxial p layers on p^+ as the starting material.

Motorola

A contract was initiated in FY88 with Motorola to demonstrate a space radiation hardened CMOS 6000 gate array with production to begin in FY89 (Reference 3.48). The total dose hardening approach was to revise the VHSIC baseline process while maintaining 85% process flow compatibility with the commercial CMOS process. Motorola modified the gate oxidation process to minimize the oxide charge and interface state contributions to the radiation-induced threshold voltage shift. They optimized the n^+ doping and implemented a graded drain to improve hot carrier stability at 5 V. Motorola demonstrated a gate oxide which resulted in a total n-channel threshold shift of only -0.50 V at 100 Mrads. The program was terminated in FY88 when Motorola announced it was moving its VHSIC technology from Arizona to Texas.

IBM

The objective of the IBM effort was to enhance the total dose and SEU tolerances of the 1.25 micron NMOS process. The main total dose hardening effort was directed toward solving the transistor leakage problem that had limited IBM's Phase 1 "enhanced" process to the 50 krad level. Additional process enhancements were developed that relied principally on heavier implants in the field and "bird's beak" regions to increase the threshold voltage in these areas. Transistors incorporating these enhancements exhibited little or no leakage current

increase at 500 krads, and threshold shifts were on the order of 0.5 V at 200 krads. In subsequent follow-on activities at IBM, circuits were shown to meet the 200 krad space hardness requirement (Reference 3.49).

A set of radiation environment specifications and goals were established for the baseline process. More stringent requirements for radiation hardening were set for the enhanced process. The technologies for each requirement were developed as parallel efforts. The radiation hardening requirements for both baseline and enhanced CMOS device technologies are given in Table 3-1 of Reference 3.45 which also compares VHSIC Phase 2 radiation requirements with those for VHSIC Phase 1. The work on radiation hardening during Phase 2 is also discussed in Section 3.3.2.

Hughes Aircraft Corporation

A comprehensive study was conducted into the effects of SOS starting material on back channel and edge leakage behavior following irradiation. It was found that back channel leakage could be minimized by the use of Union Carbide type B wafers. Unfortunately, leakage currents remained too high for the CMOS/SOS technology to be considered for high density SRAM applications. Evidence obtained during the study indicated that leakage was occurring along the bottom edge of the n-transistor sidewall as a result of charge buildup in the sapphire. Some additional improvements in total dose hardness (circuit functionality to approximately 5 krads) were realized during the other programs, but the leakage problem was never completely solved (Reference 3.50).

Harris/GE/RCA

At the time of the Phase 1 program, RCA was the major SOS device supplier in the United States and had demonstrated a 3 micron, 16k CMOS/SOS SRAM that was radiation hardened to space levels. Subsequently, a 1.25 micron technology was developed and RCA became a second source to Hughes during the Phase 1 program. Because of the interest in high density, hardened SRAMs for missile and space applications, a DNA contract was initiated with RCA to develop and produce a space-hardened 1.25 micron 64k CMOS/SOS SRAM.

The radiation hardening effort began in 1985 with an examination of means to improve the hardness of commercial SOS test chips. The major challenge was to harden the basic CMOS/SOS transistor structures to total dose. This involved optimization of processing parameters in order to harden (1) the gate oxide, (2) the mesa edge, and (3) the silicon sapphire interface. Special attention was also given during design of the SRAM to further improving its dose rate upset and SEU immunities. For example, upset immunity was increased in both environments through added memory cell capacitance.

Honeywell

Honeywell's Phase 1 bipolar technology proved to be extremely sensitive to single event upset (Reference 3.46), and a contract was initiated in 1985 to address this shortcoming.

Using the baseline ADB-III process at Honeywell, a family of registers and flip-flop macrocells hardened to SEU was designed, developed, and tested. Several variations of two circuit hardening techniques were implemented. These techniques provided SEU immunity by (1) keeping the correct data stored in a dual redundant register or (2) filtering the SEU by adding time delay to the flip-flop's feedback path.

The technique of using a dual redundant latch in place of each single flip-flop element provided the greatest SEU immunity (Reference 3.51). By storing data at two independent nodes (gated by Schottky diodes), the scheme permitted fast (1.4 ns - 3.1 ns) registers with linear energy transfer (LET) thresholds beyond 80 MeV/(mg/cm^2). While doubling the number of latches doubled the register layout area and power, the demonstrated error rates were less than 1E-10 upsets/bit-day. Since registers occupy only a small percentage of most bipolar layouts, these redundant macrocells can be added to designs with almost no impact on performance.

The second SEU hardening approach took advantage of the fact that the effect of an SEU strike dissipates within 2 to 380 ns of the event. With this information, flip-flop macrocells were designed with varying time delay "filter" elements (made from resistors, capacitors, and/or transistors) within the feedback path. This delayed feedback technique was used to intentionally slow the response time of several latch designs between 1.9 nsec and 30 nsec, which demonstrated enhanced LET thresholds between 5 and 38 MeV/(mg/cm^2), respectively. Delayed feedback techniques proved successful where layout area and power dissipation were most critical but speed could be sacrificed.

TRW

TRW's triple diffused (3D) bipolar technology exhibited latchup during dose rate testing at about 8E8 rad/s (Reference 3.46). The original solution to this problem involved enlarging the ground contacts on all n-type resistors. This solution prevents latchup by shunting the base-emitter junction of a parasitic lateral npn transistor in the latchup path, but requires additional layout area.

The purpose of the DNA hardening effort was to investigate an alternate solution to the latchup problem by using p^- on p^+ epitaxial substrates in a process that is normally fabricated without an epitaxial layer (Reference 3.52). Device modeling/simulation codes such as PISCES were used to determine the critical parameters controlling latchup.

Texas Instruments

Initial dose rate testing of the Array Control Sequencer (ACS) customization of the 10k gate array chip demonstrated latchup on the 2-volt logic supply at approximately 2E8 rads/s (References 3.46 and 3.53). The latchup sensitive areas of this 10k gate array were identified by scanning the die using a focused Nd/YAG laser with 150 micron spot size and observing whether latchup was induced. Infrared imaging of the hot regions revealed two suspect register file macrocells. Subsequent testing revealed that other customizations of this gate array which did not use these macrocells were immune to latchup.

Using a CAD workstation, layouts of latching and non-latching cells were compared. Non-latching cells had resistor well contacts spaced at regular intervals. The latching cell had a design error that resulted in only one contact being used in a large n-type epitaxial well containing over 5,000 resistors. Consequently, the well would become debiased in transient radiation environments and trigger a latchup condition. To remedy this problem, two hardening techniques were incorporated: (1) approximately 500 additional contacts were added to the resistor well; and (2) parts with a single well contact were fabricated using p^- on p^+ epitaxial substrates that incorporated deep trench isolation extending down through the field oxide into the heavily doped substrate.

Two-volt latchup was not observed when modified devices were exposed to 1E12 rads/s. The additional contacts eliminated latchup by shunting the base-emitter junction on a parasitic vertical pnp transistor that is formed by the resistor well. For the devices processed on p^+ substrates, the lower gain of the lateral parasitic npn transistor that is formed between the resistor well and an adjacent collector prevented the regeneration that results in latchup.

3.3.4 Improved Tools and Materials

E-Beam Lithography

E-Beam Lithography Equipment: E-beam lithography equipment with a capacity for high wafer throughput was developed to support the fabrication of 0.5 micron feature size VHSIC chips on a pilot line basis. Hughes/Perkin-Elmer (PE) developed such a machine (the AEBLE-150) under a VHSIC contract which started in 1981 and finished with final acceptance test by the Army in February 1985. PE undertook an additional, independent, three year effort to improve the resolution and overlay accuracy in order to meet the full machine specifications. An AEBLE 150 meeting the requirements was accepted by Motorola in September 1988. This successful development provided a capability for e-beam patterning which meets the needs of the U.S. for a machine capable of moderate production of submicron chips. At the present time, Perkin-Elmer has sold approximately 14 AEBLE-150 machines to U.S. and foreign companies. Further improvement of the capabilities of this machine to 0.25 micron resolution is being undertaken in a two year contract with the DARPA MIMIC program office. For further details, see References 3.54, 3.55, and 3.56.

Perkin-Elmer plans to introduce a 0.5 micron mask maker (MEBES IV) in 1991, and to have an enhanced AEBLE-150 capable of fabricating, by direct writing, 0.25 micron minimum feature size chips by 1993. A highly accurate 1.25 micron mask maker is planned for 1994/1995.

Electron Beam Lithography Components: The objective of this VHSIC Phase 3 contract with Hughes Aircraft was to develop technologies necessary to build a direct-write e-beam machine capable of meeting the VHSIC Phase 2 goals. Three tasks specifically addressed were: 1) the development of improved electron-beam column components; 2) the evaluation of a thermal field emitting electron source; and 3) the development of a very accurate high-speed digital-to-analog converter (DAC).

Hughes developed a unique single lens shaper, the scanning electronics, and the pattern generator, while Perkin-Elmer designed scanning optics, the final lens, and the basic LaB_6 e-gun. Hughes was successful not only in developing the DAC, they also supplied an extremely accurate 18-bit DAC, a 15-bit DAC, as well as a very fast 13-bit DAC for the electrostatic deflection system. The first 5 AEBLEs built had Hughes DACs in them. Further details are found in Reference 3.57.

Software for Electron Beam Lithography: The objective of this program by TRW and GCA was to develop the necessary software to operate the GCA e-beam machine, DWM-7000EB. The program called for the development of three versions of software.

Version 0 software consisted of the test programs necessary to support early integration, plus testing of the prototype instrument.

Version 1 software was the minimum software configuration required to support basic system functions and test software design and has the following characteristics: 1) emphasis on successful hardware/software integration rather than throughput; 2) step-and-repeat stage operation; 3) effect correction and first-order proximity; and 4) support of non-Manhattan geometries but no support for photocomposition.

Version 2 software consisted of programs required to support operation of a fully-functional production lithography system. This program funded the software functional specifications.

The goal of this program was to allow GCA to maintain the scheduled availability of an e-beam machine for the VHSIC Phase 2 submicron phase. This effort was primarily funded to insure the availability of an e-beam machine in the event that Hughes/Perkin-Elmer was unable to develop their e-beam machine in time.

The software program was completed on time and met all of the stated goals. However, GCA shut down the e-beam program in 1984 because of insufficient internal funds to maintain it. Their e-beam system, DWM 70000EB, was never marketed and the software technology was never used. See Reference 3.58 for further details.

X-Ray Lithography

All of the X-ray lithography programs were awarded under VHSIC Phase 3. Initially, there was a feasibility study program awarded to Perkin-Elmer. It showed that an X-ray-step-and-repeat lithography was possible and had high resolution capability providing the X-ray mask problem could be solved. In 1984, the Government awarded Perkin-Elmer a six year X-ray development program leading to a submicrometer X-ray step-and-repeat lithography system.

Extension of X-Ray Lithography Technology to VHSIC: The objective of this program with Perkin-Elmer was to develop alignment, work stage, mask, organic resist, and radiation damage free technologies, and to establish performance specifications for a high resolution (0.5 micron feature size), high throughput (eight 4-inch wafers/hour) X-ray lithographic machine. Induced radiation-damage-caused resist exposure was evaluated, and resist formulations were characterized for exposure properties, dry etch resistance, adhesion, and resolution.

This program was undertaken in support of the VHSIC Phase 2 goals of 0.5 micron linewidths. It was intended to establish a high throughput replication technique for VHSIC and other submicron circuits, while trying to understand the radiation effects. This program depended greatly on resist programs, mask technology, and the electron beam programs for mask making at submicron linewidths.

The project was completed in December 1981 and produced major enhancements to X-ray lithography. The success of this program led directly to a program to build an X-ray step-and-repeat lithography machine which is currently being funded through DARPA's X-ray lithography initiative.

The program identified alignment sensing techniques for the required mask/wafer error of 0.1 micron at 0.5 micron resolution. Titanium and silicon carbide masks were demonstrated. Several resist formulations were evaluated including dry developable resists. X-ray radiation studies showed no adverse effect on CMOS device yield, performance, or reliability. Specifications for an X-ray step and repeat lithography machine were developed. X-ray lithography was shown to be a viable technique for the high throughput production of submicron integrated circuits. Details will be found in References 3.59 and 3.60.

X-ray Lithography Equipment: The objective of this program with Perkin-Elmer was to develop a lithographic machine capable of patterning submicron chips at high throughput under moderate production volume. The key features of the X-ray step and repeat (XSAR) machine specifications and goals for this program were: (1) 0.5 micron resolution, (2) 20 wafer levels/hr (with a 10 millijoules/cm^2 resist sensitivity) and four inch diameter wafers, (3) development of a source for the fabrication of high quality masks, and (4) installation and testing of the tool in a VHSIC Phase 2 pilot line.

This program was undertaken in support of the VHSIC Phase 2 goals of 0.5 micron linewidths. It was a direct outgrowth of the "Extension of X-Ray Lithography

Technology to VHSIC" contract and depended greatly on resist programs and the electron beam programs for mask making at submicron linewidths.

The project was transferred to DARPA in 1989 and is now part of the National X-Ray Lithography Institute Initiative. As of January 1990, there were two fully operational XASR machines. One, at Perkin-Elmer has been used by SEMATECH and IBM. The other, at Honeywell, underwent pilot line production testing. These machines are currently for sale.

The program succeeded in building an X-ray step-and-repeat lithography machine capable of about 15 wafer levels/hr (with a 20 millijoules/cm^2 resist). It also developed a mask technology capable of producing <0.5 micron linewidths on a boron nitride membrane using gold as the absorber. The machine was demonstrated to the Government and the semiconductor industry and one is now installed in a pilot line environment. One other machine at Perkin-Elmer is available for use by interested parties.

X-Ray Lithography Exposure Station: The objectives of this program with Spire, which started in February 1988, were (1) to develop a simple, low cost, X-ray exposure station for X-ray resist and mask testing; (2) to develop high sensitivity, high resolution resists for X-ray lithography; (3) to test these resists in a pilot line environment, and (4) to provide a domestic, commercial source for these resists.

This program was undertaken to provide X-ray resists and a means of testing those resists in support of the VHSIC Phase 2 goals of 0.5 micron linewidths. It depends greatly on the electron beam program for making test masks at submicron linewidths.

The project was transferred to DARPA in 1989 and is now part of the National X-Ray Lithography Institute Initiative. As of January 1990, there was one test station ready for acceptance testing, and resists delivered are 10 times more sensitive than those on the commercial market. The project was cancelled at this point, with the machine to stay at Spire until a suitable place has been found for it.

The program succeeded in building a low cost X-ray exposure station with the capability of interchangeable targets. This enabled the machine to simulate X-rays from a variety of sources at different wavelengths. Negative resists were developed that are at least 10 times more sensitive that those on the commercial market. This exposure station can be used for testing resists or replicating masks where an alignment to another level is not needed.

Advanced Wafer Imaging System

The objectives of the VHSIC sponsored Advanced Wafer Imaging System (AWIS) program were to significantly advance the state-of-the-art technology in optical step-and-repeat lithography . The goal was to develop a production prototype machine which could produce

0.5 micron geometry chips of at least 1 cm^2 area, with an alignment accuracy of 0.1 micron at a rate of twenty five 4-inch wafers per hour.

GCA Corporation was selected to provide a vehicle for the evaluation of the feasibility of an AWIS machine. Accordingly, an optical stepper system with the characteristics given in the table below was developed and incorporated into a GCA DSW-8000 frame. In 1987, this system was delivered to IBM at Manassas, VA, to undergo characterization in the VHSIC-2 pilot line and to demonstrate its productivity in patterning 0.5 micron geometry devices.

Stabilization of the illumination system was achieved, and the stepper system was brought within the focus control specification in 1987. The system was fully tested and accepted in March 1988. It was made available to industry, university, and Government personnel, who conducted experiments in deep ultraviolet lithography. These experiments have been of great value in evaluating several resists developed by at least ten companies and in the overall development of deep ultraviolet lithography at 248 nanometers. Many publications resulted from this program (References 3.61-3.67). Characteristics of the stepper are summarized in the following table.

Prototype Stepper Characteristics

Stepper	GCA DSW-8000
Lens	Tropel 10-1435 KrF
Reduction Ratio . . .	10:1
Field Size	14 mm diameter (10 mm x 10 mm)
Numerical Aperture .	0.35
Wave Length	248.4 nm
Bandwidth	0.04 angstrom
Wafer Size	100 mm
Focusing System . . .	Broadband Low Grazing Angle

Laser Pantography

The Laser Pantography (LP) program at Lawrence Livermore National Laboratory (LLNL) has been funded in large part by the VHSIC program since July 1985. The LP program aimed to develop the processes, software, and equipment necessary to fabricate hybrid wafer-scale digital electronic systems. The program's emphasis has been on interconnect, either chip-to-chip or on-chip in the case of gate arrays.

Hybrid Wafer-scale Integration Technology: LLNL's Hybrid Wafer-Scale Integration (HWSI) technology enables the fabrication of very compact, highly reliable, high-speed electronic systems by using advanced electronic packaging techniques. The approach

is that of a "multichip module" in which the interconnection substrate is fabricated on a silicon wafer (a "silicon circuit board," or SiCB). The silicon substrate is a very good heat conductor and at the same time completely eliminates thermal expansion mismatch between the substrate and the chips. It also permits the interconnection module to be fabricated using more or less conventional integrated circuit (IC) fabrication equipment and techniques.

The LLNL metal interconnect is based on "medium film" technology: the metal (typically copper or gold) is about 5 microns thick and 10 microns wide over a ground plane. The pitch is typically 50 microns, which limits the crosstalk to acceptable levels. With this pitch, most complex systems can be routed on only two levels of microstrip interconnect. The fabrication techniques, the signal-propagation characteristics of these structures, and other features of the technology such as on-module resistors are described in Reference 3.68.

There are several techniques that may be used to electronically connect the integrated circuits to form a functional multichip module. In response to limitations of conventional bonding techniques, however, LLNL has developed a laser-based interconnection technology in which metalization is fabricated directly down the edges of the chips. This technology coupled with a high quality die attachment, has yielded extremely high pin-out (e.g., 25 micron pitch, or 1600 interconnections on a single 1 cm^2 die). It also has provided low inductance (<0.25 nH per interconnect) and outstanding heat conduction through the die attachment. The fundamentals of this interconnection technology are described in References 3.68-3.72. A recorder developed by Fairchild Corp. incorporating a solid state memory that utilizes this technology is now deployed in a space satellite. A 20-chip memory module on which chips occupy over 80% of the module area has been fabricated with the chip-to-module interconnect written on the vertical chip walls.

LLNL SiCB-based HWSI technology has been targeted toward compact, high performance digital and radio-frequency (rf) systems. Such systems may require liquid cooling. This has been achieved effectively and compactly by the use of microchannel cooling. Microchannel heat sinks can be fabricated directly within a silicon wafer, thus providing a thermal expansion match to the SiCB. During 1987, LLNL applied microchannel heat sinks to cooling solid-state lasers (Reference 3.73). During 1987 through 1989, LLNL applied them to cooling rf power amplifiers, under Air Force funding (Reference 3.74).

Laser Direct Write Double Level Metal Technology: An all-dry, double-level metal technology for personalization of VLSI gate arrays has been established. The goal is to provide rapid prototyping of new electronic systems, and to serve as the nucleus for a potential job-shop, low-volume manufacturing environment. This resistless, all-dry technology has numerous potential advantages. The direct-write eliminates the turnaround time for mask fabrication and inspection. The elimination of resist reduces the number of processing steps and eliminates the need for a class-10 yellow room environment.

LLNL has developed all six process modules for this technology: laser direct-write, metal sputter deposition, metal magnetically enhanced reactive-ion etching (RIE), oxide plasma-enhanced CVD (PECVD), oxide RIE, and Si PECVD. Integration of these modules into a coherent technology has been accomplished successfully (References 3.68 and 3.75). Using 3-micron lines on 5.5-micron pitch for metal 1 and 4-micron lines on 6.5-micron pitch for metal 2, double-level-metal interconnect through 100,000 laser-patterned, 2-micron vias has been successfully demonstrated using this technology. In split runs, LLNL also showed that the yield of laser patterning is comparable to, or somewhat better than, standard lithography.

LP Laser Equipment and CAD Systems:

LP Hardware: The LP program has developed two types of laser systems, one for custom VLSI interconnect on flat surfaces, and one for hybrids, where writing in the z-dimension is required in addition to x and y. The custom VLSI machine uses acoustooptic (A/O) beam deflection and A/O intensity control to scan a focused argon ion laser beam over a 0.5 mm x 0.5 mm area ("window") of the wafer surface. Precision translation stages move the wafer from window to window. The focal spot size is 1.0 micron and the positioning accuracy of the machine is 0.5 micron. The hybrid machine rasters the wafer back and forth under the focused argon ion beam at high speed while an A/O modulator controls the intensity. The spot size of the laser on the surface is 5 microns or greater, dimensions which are appropriate for the purposes of chip-to-chip interconnect. To permit laser writing on a vertical chip wall, the laser beam is incident on the SiCB plane at 45 degrees.

CAD Systems: The standard means of design entry via a schematic layout editor has been augmented with a VHDL entry path to allow the capture and simulation of designs in VHDL format. For more information see Reference 3.68.

Advanced Resist Materials and Processes

The objective of this program with Hewlett Packard was to develop very high performance electron beam resists. In negative resists, this means a sensitivity of 0.5 microcoulomb/cm^2 and a resolution of 0.5 micron lines and spaces. In positive resists, a sensitivity of 1.0 microcoulomb/cm^2 is required and a resolution of 1.25 micron lines with vertical walls. Linewidth control must be +/-0.1 micron with dry etch resistance comparable to optical positive resist in $CF_4/0_2$ and CCI_4 plasma, and in an argon ion mill. Other objectives include wide process tolerance, low pin hole density, resistance to conventional wet etchants, and good adhesion to Si, SiO_2, and Cr.

This program was undertaken in support of VHSIC Phase 2 goals of 0.5 micron linewidths and in direct support of the VHSIC electron beam lithography program. It was intended to enable the throughput and resolution of the VHSIC and other commercial e-beam resists to be greatly enhanced while providing good dry processing compatibility.

The project was completed in January 1983. The program produced both positive and negative resists with high sensitivity, good resolution, and high dry etch resistance. These include a high performance negative resist suitable for high sensitivity (<1 microcoulomb/cm^2) and submicron resolution (0.5 micron width $<25\%$ linewidth variation). Excellent masking capability for dry etching of polysilicon, silicon dioxide, and aluminum under IC processing conditions was demonstrated.

The program also produced two high sensitivity positive resists. One had a sensitivity of 15 microcoulombs/cm^2, resolution <0.5 micron, and fair dry etch resistance. The other was a silicon containing resist with high oxygen etch resistance useful for multilayer lithography. This resist had a sensitivity of 50 microcoloumbs/cm^2, <0.5 micron resolution, and excellent dry etch resistance.

Both positive and negative resists were sent to eight VHSIC contractors and the results were reviewed. Sensitivity, contrast, resolution, and dry etch resistance were in essential agreement with Hewlett-Packard data. Joint reviews were also held with Hughes Research Laboratory which had a similar resist contract with the Navy. Details are given in References 3.76 and 3.77.

3.3.5 Packaging

Introduction

From the start of the VHSIC program it was understood that the packaging and interconnection of integrated circuits would be critical if they were to operate properly in military systems. A large number of input/output pins would be required in order to interface these highly complex devices. This, coupled with the requirement that they operate at high clock speeds, meant that adequate cooling would be necessary to take care of the resulting high power dissipation. In addition, the package must allow the ICs to operate under severe environmental conditions.

Since no commercial products were available that met these requirements, an extensive and well-coordinated development effort was undertaken. The packaging/interconnect technology had to address such issues as: 1) the fabrication of fine lines on chip substrates, 2) the cooling of large chips with high power densities, 3) the construction of multilayer, hybrid substrates, 4) thermal expansion mismatch between dissimilar materials, 5) package hermiticity, and 6) low impedance leads to support fast rise times and low crosstalk.

In general, the development program was highly successful; the Phase 1 and Phase 2 chips were adequately packaged and the state-of-the-art was advanced substantially. Abbreviated descriptions of this effort comprise the remainder of Section 3.3.5. References to reports and contracts are provided for those needing further details.

Feasibility Studies

The earliest efforts to develop the necessary technology were several Phase 3 contracts awarded in 1980 that established the feasibility of various advanced packaging concepts.

- Honeywell developed the capacity to fabricate fine line contact grids on ceramic substrates. Attention was paid to ceramic selection and finishing, and various thin film processing techniques were explored (Reference 3.78). This technology became the basis for conductor patterning in copper/polyimide thin film multilayers that was eventually used in the Phase 2 program.

- General Electric demonstrated the technical feasibility of large, complex, high lead count, thermally and electrically efficient BeO ceramic package fabrication (Reference 3.79). The fabrication process proved difficult, however, resulting in high cost.

- Raytheon developed a methodology for evaluation of device and interconnect performance using various simulation programs (Reference 3.80). In a separate contract they also used standard multilayer wafer metalization processes to demonstrate interconnection technology suitable for submicron chips (Reference 3.81).

Phase 1 Chip Packages

Single chip packages, both surface mount and pin grid arrays, were developed to house the Phase 1 chips.

- The most important features of the packages for the Texas Instruments chip set were the low impedance signal and ground patterns and thermal pads that ran through the bottom of the package, underneath the die attach area (Reference 2.14).

- A family of three single-chip packages with 42, 161 and 224 I/O pins was developed for the Westinghouse chips. The package construction was co-fired alumina with perimeter leads on 20 mil centers (Reference 2.15).

- Honeywell developed three 180-pin array packages on 0.1 inch and 0.05 inch centers and a solder bumped TAB process. New unique features included buried strip line construction and programmable power and ground locations (Reference 2.11).

Advanced Packages

The next phase extended the VHSIC packaging effort to single chip packages, multichip carriers, and printed wiring boards to accommodate devices operating at 100 MHz clock rates with greater than 250 terminals. For the most part, the earlier contracts (1984) came under Phase 3, while the later contracts (1985-1986) were funded by the VHSIC Man(ufacturing) Tech(nology) program (Section 2.2.8).

- An early Westinghouse contract used computer modeling to determine the most important parameters of hermetic chip carrier (HCC) - printed wiring board (PWB) systems. Sample HCC-PWB assemblies were fabricated of different materials. The importance of closely matching the coefficient of thermal expansion between the HCC and PWB was confirmed (Reference 3.82).

- Hughes was the prime contractor for a study to determine the best fabrication approach for a high (>264) terminal count package with perimeter contacts suitable for connecting and protecting VHSIC devices. Co-fired ceramic packages produced by Textronix, Inc. offered the greatest ease of manufacture and reproducibility. The technology was developed to produce single and multichip packages as large as 2.5 in x 3.0 in with 20-mil and 25-mil pitch leads (Reference 3.83). Since 1985, Textronix has manufactured this type of package.

- Martin-Marietta and Honeywell undertook the challenging task of developing high lead/terminal count, fine pitch packages with high speed electrical performance. A 264-terminal, 20-mil pitch, 5-layer ceramic package was successfully designed and fabricated by Martin-Marietta (Reference 3.84) while Honeywell produced a 50-mil pin-grid array, 240 I/O package (References 3.85 and 3.86).

- A low dielectric constant laminate material for fabrication of printed wiring boards compatible with alumina leadless chip carriers was developed by Hughes References 3.87 and 3.88).

- Materials and manufacturing processes were developed by Texas Instruments for hermetic ceramic packages for mounting and interconnecting up to nine VHSIC chips operating at up to 100 MHz and having up to 303 I/O leads. Thin and thick film techniques, as well as tape automated bonding (TAB), were used as interconnecting schemes (Reference 3.89). Several U.S. sources are available for these multichip packages.

- Teledyne's approach to multichip packages was to develop a controlled impedance substrate. A low temperature co-fired base with a multilayer thin film polyimide microstrip and stripline signal path was used in order to achieve chip communication at 100 MHz. See Reference 3.90.

- Low cost, mass production methods for TAB were developed by Honeywell for interconnection of VHSIC chips to high lead count packages. See Reference 3.91.

- Martin Marietta was the prime contractor on a ManTech program to establish manufacturing techniques, processes, and controls to produce VHSIC assemblies. Westinghouse was responsible for chip screening and inspection, General Electric was in charge of the attachment of surface mounted devices to PWBs, and Martin Marietta developed electrical design guidelines to allow PWB designs of desired impedance and minimum crosstalk.

- A ManTech contract with General Ceramics developed first level packaging and interconnects.

- A ManTech contract with IBM explored tape (decal) interconnect technology.

- Third level interconnects were investigated by Sperry.

Testing and Screening

The replacement of aluminum or gold wires for electrical interconnections by polyimide tape and TAB structures introduced a potential reliability problem to microcircuits designed to operate in severe military environments.

- Sonoscan employed acoustic microscopy for non-destructive evaluation of the quality of metallurgical bonds formed between a tape structure and the chips or substrates being interconnected. Good results were obtained (Reference 3.92).

Phase 2 Chip Packages

Each of the three Phase 2 contractors had to overcome challenging problems in order to design and fabricate packages to house their complex, 0.5 micron devices. Package design, as IC design itself, now required computer aided modeling for the analysis of thermal and electrical characteristics that was needed to select specific design options.

- Honeywell designed, built, and demonstrated new single chip and multichip packages. The single chip packages (180- and 269-pin grid arrays) are based on co-fired multilayer ceramic and includes solder reflow TAB for the inner lead bonds and thermocompression outer lead bonds. The multichip package utilizes copper/polyimide fine line, thin film, multilayer interconnections. See References 3.93 and 3.94 for further details.

- The TRW program was divided into two areas: packaging the very large (1.6 in x 1.5 in) CPUAX SuperChip (Reference 3.95) and board interconnection. The specifications of the CPUAX co-fired alumina package for a cavity flatness of less than 0.001 in/in was successfully achieved. In order to limit voltage drops at internal nodes from the high transient currents expected from this complex chip, a unique power distribution grid was bonded to the face of the chip and parallel gold ribbons were welded from the internal package metalization to the grid in several places. The I/O lead count of 308 pins was selected to be compatible with a test socket developed by Texas Instruments (see Advanced Packages section above). An innovative, high speed, circuit board interconnection scheme, called "button boards", was developed and tested successfully. It consists of very small "steel-wool-like" buttons that make electrical contact between boards when the board assembly is placed under compression (Reference 3.96).

- IBM met all performance, reliability, and environmental objectives for its single chip (SCP) and multichip (MCP) packages. Both packages were attached by IBM's flip-chip, solder ball technique. The SCP is a peripherally leaded gullwing quad flat pack that can be surface mounted to a variety of printed wiring boards. It has 220 25-mil pitch I/O leads. The substrate consists of eight ceramic layers. Decoupling capacitor sites are included on the top surface which permits simultaneous switching of 64 0.5-micron off-chip drivers across the full military temperature range. Extensive computer modeling, used to determine the thermal resistance of the SCP, facilitated the design of the cooling scheme. The MCP (64 mm x 64 mm) can accommodate 16 chips and is based on a 42 layer multilayer ceramic substrate. Each chip can have up to 236 leads. A chip-to-chip data rate of 100 MHz was demonstrated. Extensive details are given in Reference 3.97.

3.4 Description of VHSIC Chips

At the beginning of Phase 1, the VHSIC contractors undertook to develop, as a group, 28 large, complex 1.25 micron silicon chips. They were chosen as demonstration vehicles to perform most of the signal processing functions required in military systems and were designed to meet the VHSIC specifications of speed, throughput, feature size, and environmental operating conditions. Shortly after the Phase 1 program began, two chips were added to the original 28 and one was dropped leaving a total of 29 deliverable Phase 1 VHSIC chips. In Phase 2, a total of 10 chips of much greater complexity and functionality were originally selected as demonstration vehicles for design and fabrication at 0.5 micron. Two of the chips were dropped from the delivery requirements and one was added. These chips are described below. Tables 3.2 and 3.3 list some of the physical and electrical characteristics of all of the delivered chips. Block diagrams of selected chips have been included to illustrate the variety of architectural and functional designs that were completed during the program (Figures 3.4 through 3.12). Detailed descriptions of the chips from each contractor are contained in the reference listed for that contractor.

3.4.1 Phase 1

Honeywell

The chip set (Reference 2.11 and Figure 3.4) consists of a parallel programmable processor (PPP), a sequencer, and an arithmetic chip intended for real-time image processing. The primary application is for the computation of enhancement and segmentation functions used in automatic target acquisition subsystems. An array of up to 32 PPP chips can be controlled by a single pair of chips (sequencer + arithmetic) at a maximum microinstruction rate of 25 MHz. Each PPP chip contains a 16-bit Processing Element (PE) which can communicate with its nearest alive neighbor to the left and right. An array of PPP chips has self-test (originating from the sequencer chip). Dead PPP chips can be identified and bypassed; spare chips can be inserted into the array under the control of the sequencer chip.

PPP: The PPP chip contains a 16-bit processing element (PE), a 512 x 8-bit PE memory, a double buffered input I/O memory, a double buffered output I/O memory, and a control/testing section. The PE can communicate with the left and right neighbor PEs in other PPP chips and can be interrogated by the controller sequencer chip. The PE has a status bit which goes off-chip where it is logically OR'd with other PE outputs. The PE has a PE memory associated with it. The address to the PE memory can come from the controller arithmetic chip (global address) or from the PE itself (local address). Each PE has an activity bit which disables writing into its own PE memory. A global constant can be transmitted to all of the PEs via the controller architecture.

Table 3.2

VHSIC Phase 1 Chip Characteristics
(Completed during 1983 - 1987)

Chip I.D.	Technology	Transistors (x1000)	Equiv. Gates (x1000)	On-Chip Memory	Size (Mils)	Power (Watts)	I/O (Package)
Honeywell: Pipeline Par Proc	ISL/CML	142	28	6K RAM	311x309	2.1	180
Sequencer	ISL/CML	136	27	80K ROM	300x300	1.8	180
Arithmetic Unit	ISL/CML	121	18	41K ROM	300x300	1.8	180
Hughes: Multiple Channel Correlator	CMOS/SOS	72	18	None	368x315	0.7	148
Single Channel Correlator	CMOS/SOS	78	20	None	397x367	0.5	148
Signal Tracking Subystem	CMOS/SOS	57	14	None	360x360	0.7	148
IBM: Complex Multiply/Accumulate	NMOS	101	37	None	320x320	3.3	240
T.I.: Data Processing Unit	STL		16	113K ROM	350x350	2.4	84
Vector Arithm Logic Unit	STL		17	8K ROM	353x365	2.4	164
Vector Address Generator	STL		12	64K ROM	301x312	2.1	84
Array Controller/Seq	STL		10	64K ROM	301x312	2.0	84
Device Interface Unit	STL		16	113K ROM	350x350	2.4	84
Multipath Switch	STL		4	None	250x265	1.3	84
General Buffer Unit	STL		10	64K ROM	301x312	1.5	84
Static RAM	NMOS	465		72K RAM	240x264	.45/.06	32
TRW: Window Addressable Memory	3D Bipolar	58	11	0.75K RAM	310x290	4.4	132
Content Addressable Memory	3D Bipolar	66	12	1.5K RAM	314x272	4.5	132
Register Arithm Logic Unit	3D Bipolar	41	6	0.5K RAM	337x330	3.8	132
Multiply/Accumulate	3D Bipolar	42	8	0.5K RAM	320x298	4.1	132
Address Generator	3D Bipolar	34	10	None	336x285	4.0	132
Microcontroller	3D Bipolar	25	6	None	346x306	3.0	132
Matrix Switch	3D Bipolar	13	2	None	200x200	2.6	132
Four Port Memory	CMOS	60	13	4K RAM	290x313	0.3	132
Westinghouse: Static RAM	CMOS	400	30	64K RAM	190x310	0.54	42
Pipeline Arithmetic Unit	CMOS	133	33	1K RAM	340x350	0.7	224
Extended Arithmetic Unit	CMOS	100	26	.5K RAM	340x350	0.41	224
Extended Arithmetic Unit Mult	CMOS	92	23	2K ROM	340x350	0.37	224
General Purpose Controller	CMOS	79	20	8K ROM/.5K RAM	340x350	0.65	224
10K Gate Array	CMOS	40	10	None	280x304	0.45	224

Table 3.3

VHSIC Phase 2 Chip Characteristics
(Completed during 1988 - 1990)

	Chip I.D.	Technology	Transistors (x1000)	Equiv. Gates (x1000)	On-Chip Memory	Size (Mils)	Power (watts)	I/O (package)
Honeywell:	Array Processor Unit *	CML	142	32	8K RAM	370x370	4.7	270
	Array Processor Controller *	CML	111	27	4K RAM	370x370	4.2	270
	Bus Interface Unit **	CML	48	19	None	280x280	3.2	180
IBM:	Systolic Processor	CMOS	80	33	None	215x215	0.9	180
	Configurable Static RAM	CMOS	144	9	18K RAM	215x215	0.68	180
	Address Generator	CMOS	48	24	None	215x215	0.6	180
	Bus Interface Unit	CMOS	36	15	None	215x215	0.85	180
	Signal Processing Element	CMOS		10	None	151x151		180
TRW:	CPUAX Superchip ***	CMOS	4100/1700		388K/168K	1500x1600	14	275
	Bus Interface Unit	CMOS	35		None	140x162	0.37	131
	Arithm Logic Macrocell	CMOS	40		None	310x166	1.04	72
	Mult/Accum Macrocell	CMOS	39		None	200x150	0.97	113
	Storage Element Macrocell	CMOS	37		2K	226x50	0.49	188
	Address Gen Macrocell	CMOS	15		None	130x132	0.54	72
	Memory IF/Read Macrocell	CMOS	14		None	100x90	0.28	74
	Memory IF/Write Macrocell	CMOS	15		None	110x90	0.28	130
	Column Disable Macrocell	CMOS	5		None	77x61	0.59	100
	One Port RAM Macrocell	CMOS	30		4K	56x60	0.20	20

* Personalization of a 70K configurable gate array
** Personalization of a 35K configurable gate array
*** Total number on chip/number needed to operate fully

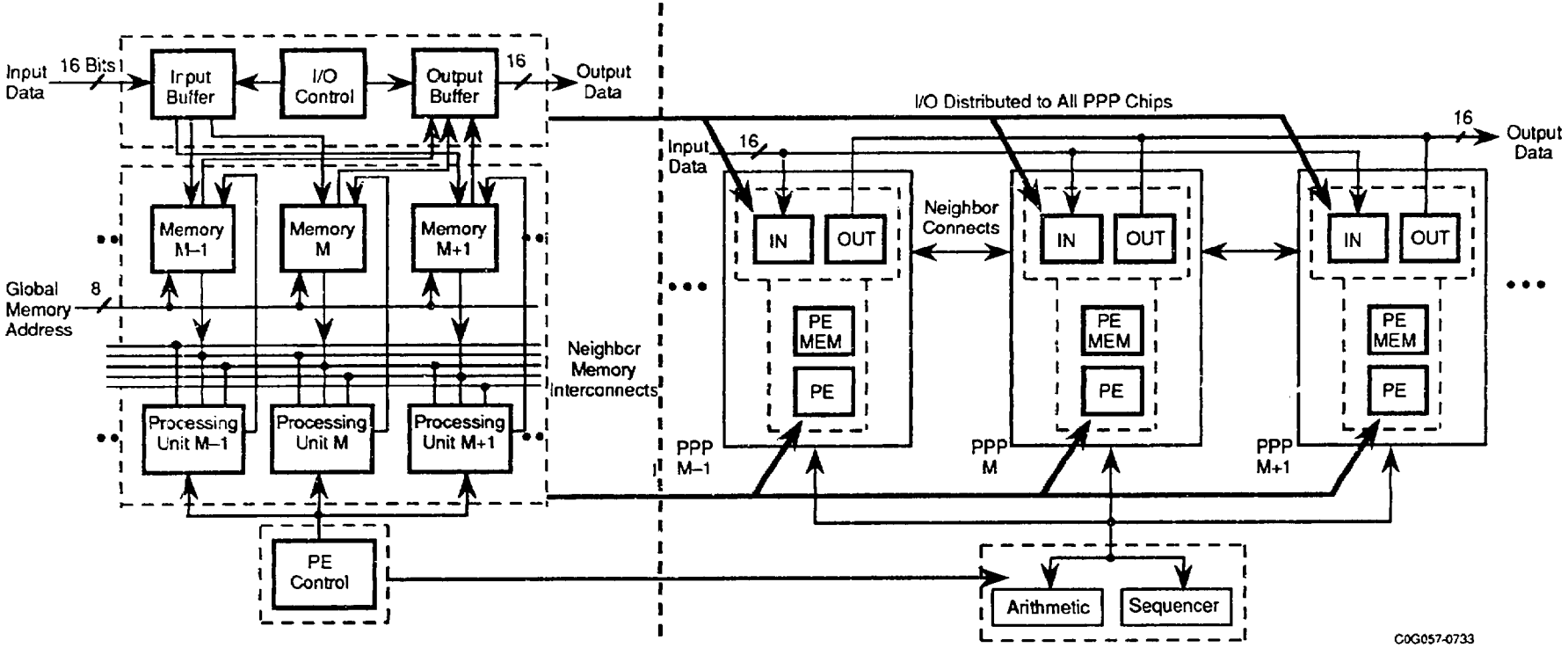


Figure 3.4 PPP Architecture Partitioning Into Chips (Honeywell)

Sequencer: The main function of the sequencer chip is to generate high-speed (25 MHz) control signals for the PPP and arithmetic chips. The sequencer is a microcode-sequenced machine, with a 1024 x 80 bit ROM on chip. The chip is capable of issuing a PPP control and address instruction every sequencer microcycle. The sequencer chip has a PPP chip test, an arithmetic chip test, and a self-test section. It also has an external RAM/ROM interface for microcode expansion, to bypass the internal microcode ROM during debug and checkout.

Arithmetic: The arithmetic chip has two arithmetic logic units (ALU), a special address generator, and a bus interface section. The primary function of the arithmetic chip is to generate addresses at high speed (25 MHz) for the PPP chips. The arithmetic chip is a microcode-sequenced machine, with a 512 x 80 bit microcode ROM on chip. A PPP control and address instruction can be issued every arithmetic chip microcycle. Additional hardware automatically addresses a PE's own or neighbor memories.

The arithmetic chip has a self-test section. It also has an external RAM/ROM interface, for microcode expansion, to bypass the internal microcode ROM during debug and checkout. The arithmetic chip can support two bus interfaces: a global bus for communicating with a higher level processor and a local bus for external data RAM usage.

Hughes

Hughes selected three key signal processing functions which are generic to anti-jam spread spectrum communication applications and designed each of the functions into a separate chip (Reference 2.12). Each chip is programmable through electronic reconfiguration of its internal cell interconnections to provide a wide range of system applications. An algebraic coder/decoder chip, which was designed early in the Phase 1 program, was replaced by the multichannel correlator described below.

Multichannel Digital Correlator: This chip performs matched filter detection of long coded preambles in which phase coherence is achievable over at least a portion of the preamble. Each chip is composed of four identical 32-stage, 4-bit, parallel correlator sections integrated into one 128-stage chip in a highly regular array. By cascading multiple chips, correlators up to 10,912 stages long may be built. For fast frequency hop applications, multiple input channels are provided for receivers operating over portions of the frequency band.

Single-Channel Digital Correlator: (Figure 3.5) The single-channel digital correlator performs the same matched filter detection of long coded preambles but the logic functions which provide independent input channels in the multichannel digital

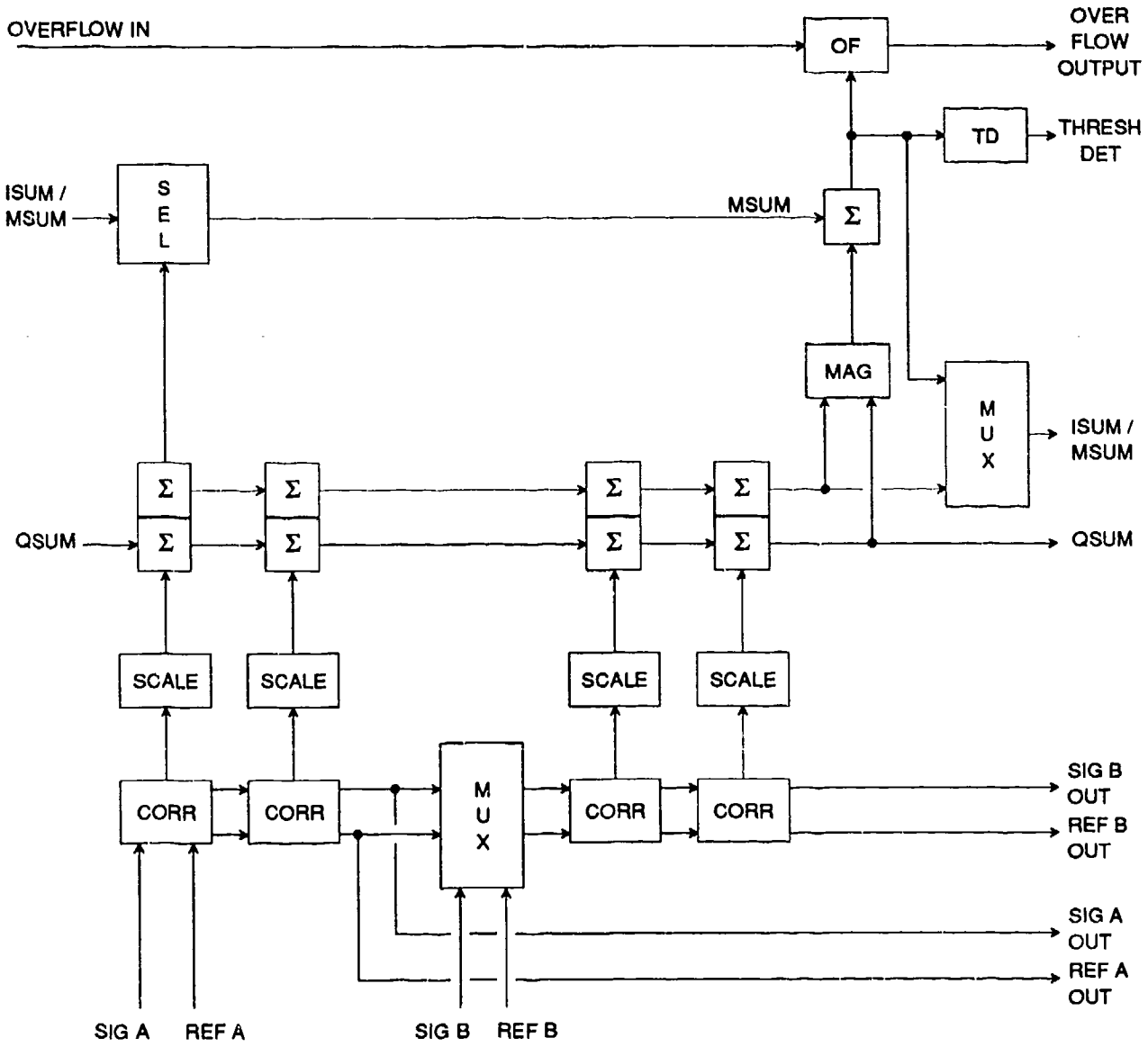


Figure 3.5 Single Channel Digital Correlator (Hughes)

correlator have been eliminated. Each of the four sections is independently controllable over a bus from an external control processor.

Signal Tracking Subsystem: The STS chip provides tracking and data detection functions. The chip contains a programmable pseudo-noise (PN) pattern generator. Three types of digital tracking loops are implemented on the chip. These provide PN code tracking and data demodulation and carrier phase or frequency tracking.

IBM

IBM designed a single chip tailored to the digital processing required in the front end of sensor systems such as sonar surveillance for which the signal processing demands are extremely high (Reference 2.13). Flexibility for use in a variety of such systems under different conditions is obtained by using an initialization parameter to select from among a set of six algorithms that have been implemented in the chip. For acoustic signal applications the algorithms include: finite impulse response (FIR) filtering, real and complex; real halfband FIR filter with quarter band shift; beamforming; complex band shift; and discrete Fourier transform.

Complex Multiplier/Accumulator (CMAC): (Figure 3.6) The CMAC is a parameter-selectable signal processor that can perform 100 million multiply and accumulate functions per second (with a 25 MHz clock). The high performance is achieved with a simple data flow that uses four subsections connected in a linear array. Each subsection contains a multiplier and adder which can be configured to execute real or complex multiplication and addition.

The chip also contains fault tolerant and self test features with monitoring and reconfiguration capabilities. A simplified version of this chip using only one of the arithmetic sections was designed and built. This signal processing element (SPE) chip became a part of Phase 2 of VHSIC and is described below.

Texas Instruments

Texas Instruments developed a set of eight ICs for military data processing and signal processing applications (Reference 2.14). The MIL-STD-1750A instruction set architecture (ISA) was selected for the data processor. An array processor optimized for 16-bit integer arithmetic was selected for the signal processor.

Data Processor Chip Family:

Data Processor Unit: (Figure 3.7) The DPU is a general purpose microprocessor which implements the MIL-STD-1750A instruction set with extended precision

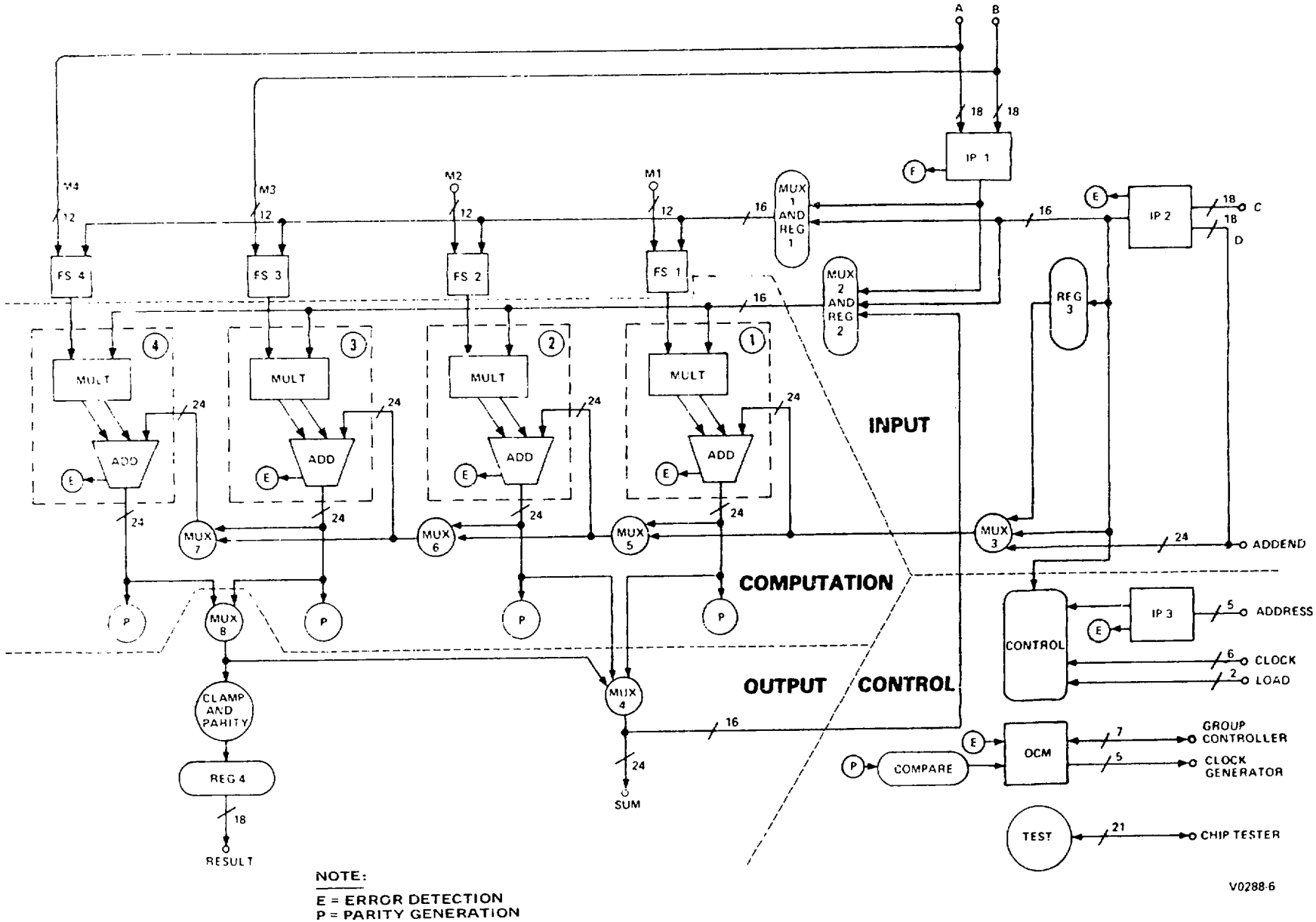


Figure 3.6 **Complex Multiplier/Accumulator (IBM)**

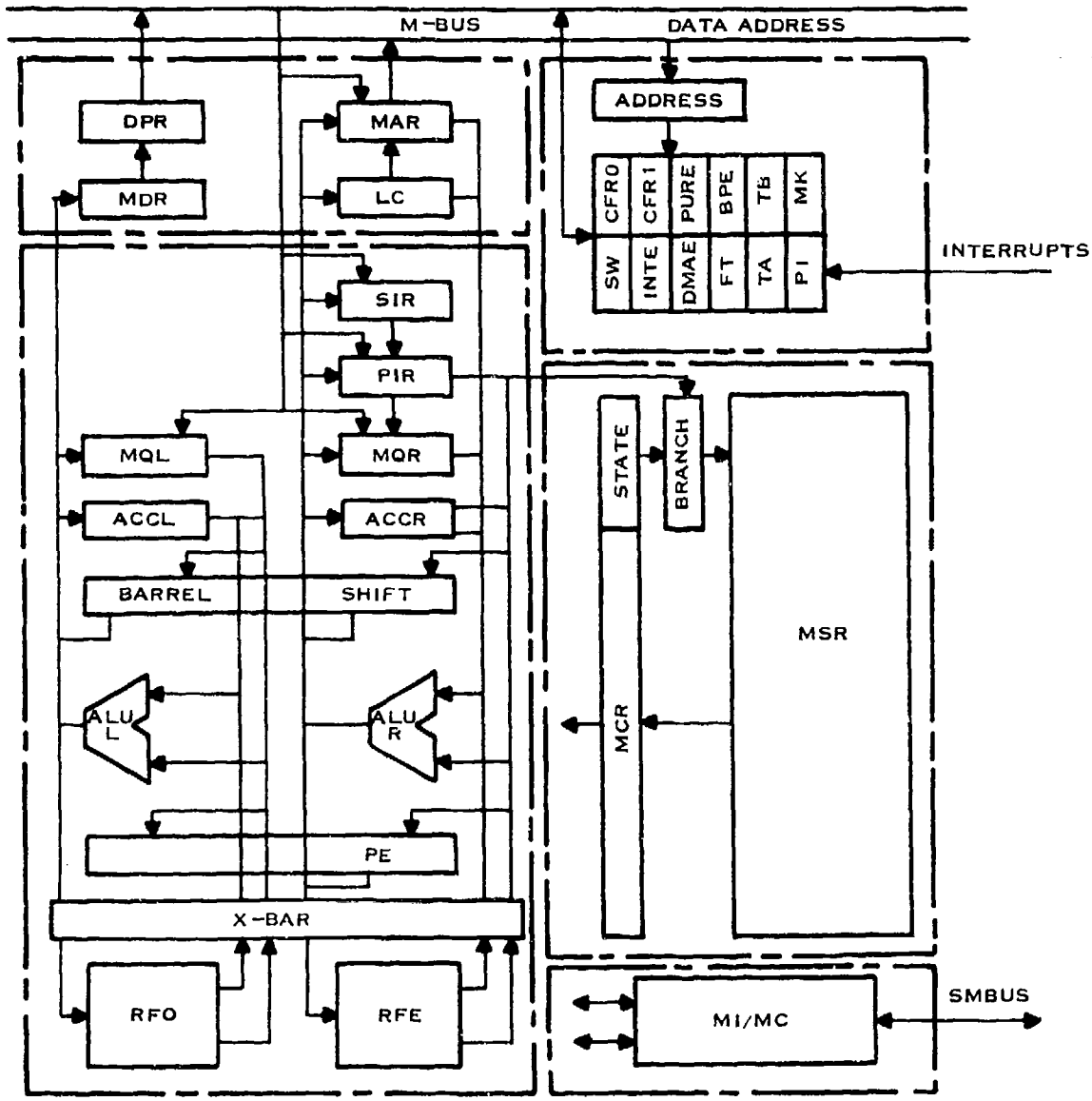


Figure 3.7 Data Processor Unit (Texas Instruments)

instructions. A pipelined architecture provides multilevel instruction look ahead and a 32-bit arithmetic path. The processor carries out all MIL-STD-1750A instructions including floating point, and provides the interfaces required to support interrupt structures, memory extension, and I/O command structures defined in the standard. Four memory addressing methods are supported by the DPU.

Device Interface Unit: The DIU provides interchip communications support for the multiprocessor with direct memory access, programmable I/O control, and operating system kernels. The chip is similar in structure to the DPU. Features unique to the DIU are provided in microcode.

General Buffer Unit: The GBU is a bus coupler between a memory bus and a system bus. It provides three methods for accessing the system bus: vying for the bus transmission, reception of message headers, and transmission of bus data.

Array Processor Chip Family:

Vector Arithmetic/Logic Unit: The VALU is a reconfigurable, 16-bit arithmetic pipeline with limited floating point operation and multiple precision. It is capable of 25-75 MOPS. The VALU includes a sequencer that generates 13-bit addresses for addressing external microinstruction memory.

Vector Address Generator: The VAG generates two dimensional array addresses with a full function ALU, concurrent I/O support, and self-sequencing capability.

Array Controller/Sequencer: The ACS is a general purpose microprogram sequencer which provides addresses for external or internal memory. The ACS also handles starting and stopping of the array processor during reset and maintenance operations.

Multipath Switch: The MPS is a 6 x 6 crossbar switch, 4-bit slice deep. The number, direction, and arrangement of the paths can be changed each clock cycle. The chip also contains a maintenance bus interface and controller to perform on-chip self testing.

Memory Chip:

Static Random Access Memory: The SRAM is read/write memory in an 8k x 9 bit array organization with on-chip parity checking and 1k block write protection. It has an internal register for pipeline operation and a reset function to return the SRAM to a known state.

TRW

TRW specialized the design of its chip set for high signal throughput electronic warfare (EW) applications but with sufficient flexibility to be useful in a wider range of signal processing systems (Reference 3.98).

Window Addressable Memory: (Figure 3.8) This specialized chip provides front-end signal sorting based on data falling between stored upper and lower limits in multiple dimensions. It uses eight 48-bit windows each with up to 12 fields (dimensions) that can be loaded under program control. An incoming 48-bit word can be simultaneously tested for inclusion in the windows. An indication is provided if inclusion occurs and a register specifies within which window or windows it was included.

Content Addressable Memory: This chip also provides high speed sorting capability based on data exactly matching stored words. It has thirty-two 48-bit memory cells on each chip that can be loaded under program control. An incoming 48-bit word can then be tested for a match with any memory word. Bit masking permits the comparison to ignore certain bits. A flag and match identifier are output.

Register Arithmetic Logic Unit: Arithmetic and boolean functions are implemented in a 16-bit word format. The chip can perform double precision computation or may be cascaded to implement a multi-chip RALU. A 16-bit x 32-word, 3-port RAM provides scratch pad memory.

Multiply/Accumulate: This chip computes sums of products, accumulates intermediate data, and outputs results for such functions as dot products, matrix multiplies, and FFTs. Instructions control the loading of the input, output, and internal registers as well as reading from and writing into the RAM.

Address Generator: The AG generates a 16-bit address each clock cycle for fetching and storing data words. Once set up, an AG will generate sequences of addresses with minimal control, including stopping or auto-restoring on completion. Operations involve up to 6 registers which are held in separate RAM files. An entire bank of 6 registers can be easily substituted for another to aid in context switching.

Microcontroller: The MC generates program addresses for fetching program control words. Address generation can be absolute or conditional, direct or offset.

Matrix Switch: The MS consists of an 8 x 8 crossbar switch, four bits deep to provide high speed data line switching. Each of the eight output ports can be configured

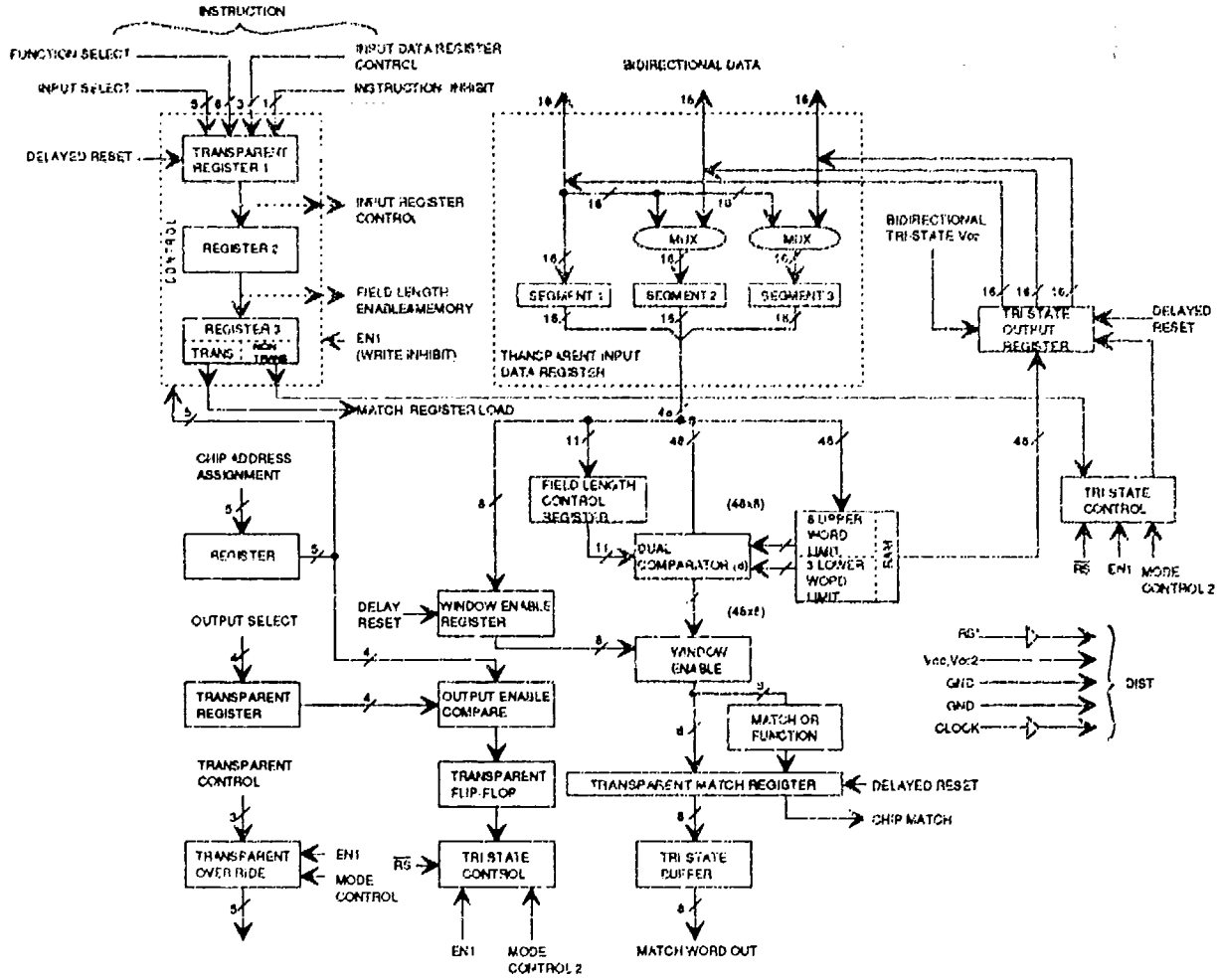


Figure 3.8 Window Addressable Memory (TRW)

to select any of the eight input ports. The switching state may be changed each clock cycle or set and left in any combination.

Four Port Memory: This chip has a 1024-word by 4-bit CMOS memory capable of reading two independent addresses and writing into another two independent addresses each clock cycle. Chip select address extension permits combining chips for up to 64k words of memory. It may be operated in a pipeline, synchronous, or asynchronous mode.

Westinghouse (Reference 2.15)

Pipeline Arithmetic Unit: (Figure 3.9) The pipelined arithmetic unit (PLAU) is a general purpose, programmable, 40-MHz chip vector signal processor. The PLAU supports logical, real, and complex operations in addition to integer and fixed point functions. The PLAU can also be organized in a variety of pipelined configurations and can be used in pairs to perform high speed complex computation.

Extended Arithmetic Unit: The extended arithmetic unit (EAU) is an arithmetic computing chip which can be combined with the general purpose controller, memories, and gate arrays to form a microcomputer which executes the MIL-STD-1750A instruction set. The major functional sections of the EAU are I/O, multiplier, 32-bit floating point ALU, 16-bit fixed point ALU, RAM, microcode command register, and built-in-test circuitry.

Extended Arithmetic Unit Multiplier: The 32-bit extended arithmetic unit multiplier (EAUM) chip provides high-speed, fixed and floating point multiply/divide operations. It supports the 1750A format and is optimized for 32-bit operations at a 25-MHz clock rate.

General Purpose Controller: The GPC is designed for use as the microprogrammed control element in embedded 1750A and 1750 GP computers. The GPC can directly address 256k of memory and has instruction fetch overlap capability. A built-in test capability also resides on the chip and can be used at the wafer, component, and module levels.

10k Gate Array: The gate array provides specialized support functions for the custom chips and the 64k SRAM. These functions include random control logic, interfaces, crossbar switching, barrel shifting, memory address generation, and clock distribution. The chip has 11.3k gates implemented as a routable array of 7904 cells surrounded by 152 I/O buffer cells. The chip is personalized with the help of a minicell library which contains approximately 60 standard logic functions. Approximately 20 percent of the gate count is dedicated to built in test.

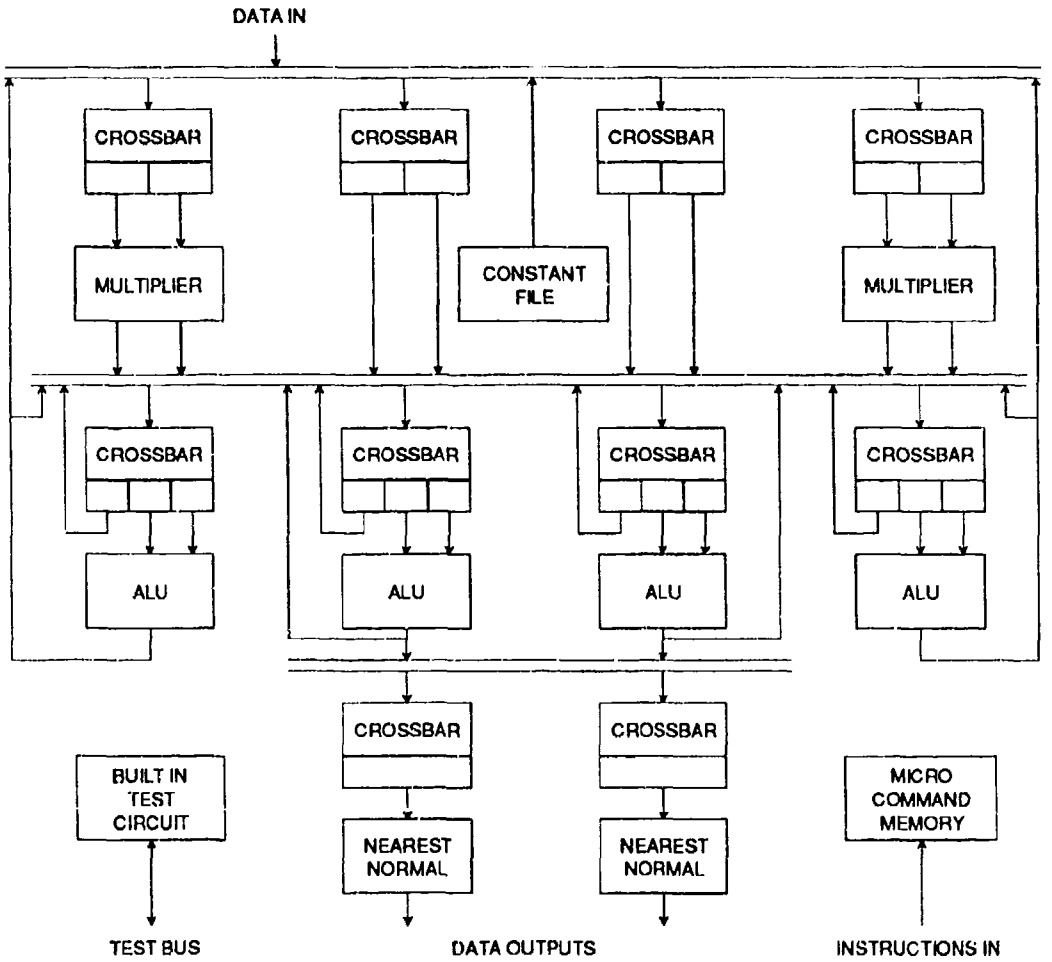


Figure 3.9 Pipeline Arithmetic Unit (Westinghouse)

Static RAM: The 64 kbit SRAM has separate pass/latch control inputs for the on-chip input and output registers. Four modes of operation are possible: (1) fully asynchronous; (2) asynchronous input and synchronous output; (3) synchronous input and asynchronous output; and (4) fully synchronous mode for pipelined operation. The design of the 64k SRAM uses column redundancy to enhance the yield.

3.4.2 Phase 2

Honeywell

Honeywell chose to design its Phase 2 brassboard chip set (Reference 3.99) using two generic bipolar CML gate arrays --- a 35,000 gate array for the BIU chip and a 70,000 gate array for an array processor and an array controller. The larger gate array is also configurable in the sense that custom macrocells may be substituted for any of the six sectors of the gate array. The brassboard chips were then designed as personalizations of the basic gate array by appropriately routing the upper metalization layers.

Array Processor Unit (APU): (Figure 3.10) This chip performs the basic arithmetic computation optimized for electrooptical image processing. It is similar in function to the PPP chip of Phase 1 described above.

Array Processor Controller (APC): This chip provides the control functions for the APU and memory chips which constitute a logical processor module.

Bus Interface Unit (BIU): The BIU provides a data interface between a standard backplane PI-bus and a Functional Interface Unit chip which then communicates with the rest of the chips in a board. The board side of the BIU is a direct memory address interface with multiple block and block skip addressing capability.

IBM

The IBM chip set was designed for general purpose, high speed, digital processing with specific application to the needs of sonar systems (Reference 3.45).

Systolic Processor (SP): (Figure 3.11) The SP chip contains a dual 16-bit multiply/32-bit ALU and features a high speed partial product adder funtioning at 100 MHz. The SP is pipelined internally to maintain a high throughput rate. The two multipliers can be used together to perform complex arithmetic or to perform two-point, real arithmetic.

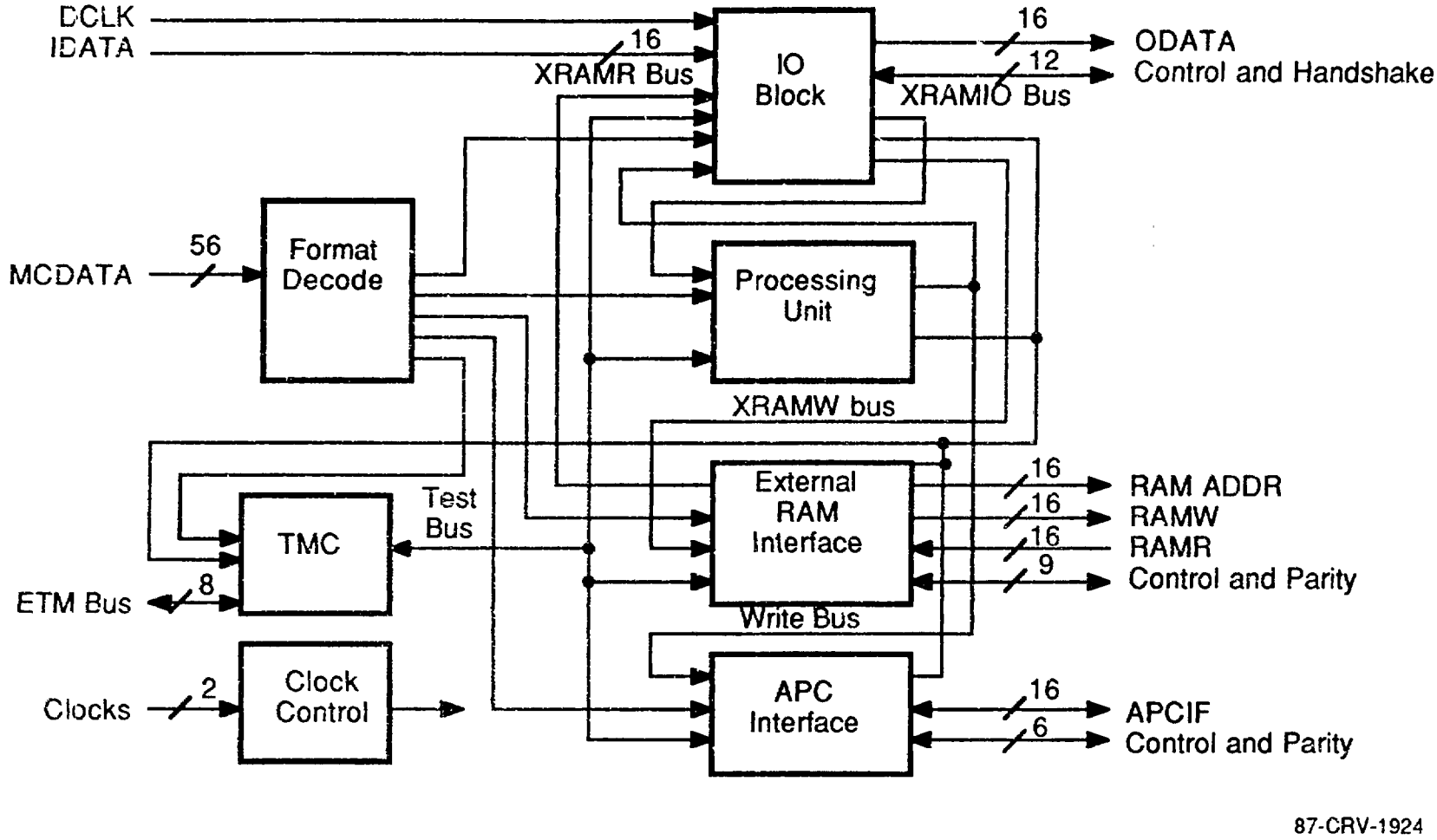


Figure 3.10 **Array Processor Unit (Honeywell)**

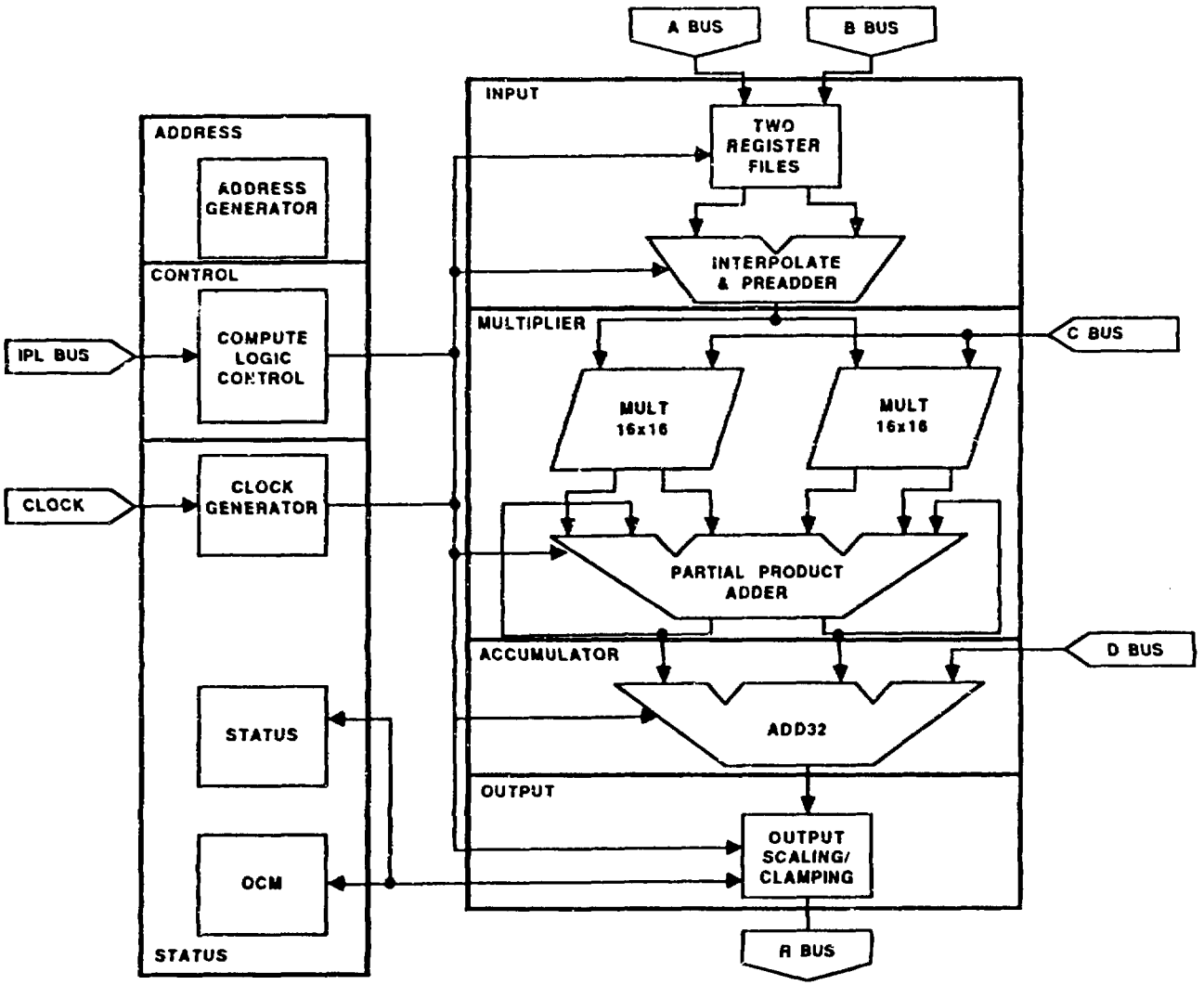


Figure 3.11 Systolic Processor (IBM)

Configurable Static Ram (CSR): This 18-kbit static RAM provides a complete memory subsystem on a chip. It has four independent 256 x 18-bit memories which can be reconfigured electronically to into a variety of 18-bit and 36-bit wide organizations. The CSR chip provides this reconfigurable structure through the use of two 18-bit input ports, two 18-bit output ports, and two address ports.

Address Generator (AG): The AG chip generates memory addresses for the CSR and also generates address sequences for use in digital processing. It has two programmable 16-bit address generators and a 12-bit address counter with programmable start and stop addresses.

Bus Interface Unit (BIU): The BIU provides an interface between a standard backplane PI-bus and the rest of the chips in a board. The board side of the BIU is a direct memory address interface with multiple block and block skip addressing capability. The BIU can be used to write and read data of control memory, to verify memory integrity through the read capability of the direct memory address, or for initial program loading of discrete registers into chips.

Signal Processing Element (SPE): The SPE performs multiply and accumulate algorithms. It consists of a single computational subsection similar to those in the CMAC chip described above and performs the same algorithms.

TRW

The TRW/Motorola team developed a unique design and fabrication methodology capable of producing "superchips" whose size (1.5 in x 1.6 in), number of transistors, and functionality were up to two orders of magnitude greater than current state-of-the-art integrated circuits (Reference 3.100). To accomplish this, the superchip is comprised of blocks called "macrocells", each equal to or greater in complexity and size than VHSIC Phase 1 chips. Different macrocell types are interconnected on one chip to achieve the functionality of the superchip. In order to attain overall yields of greater than 10%, a sufficient number of spares of each type must be provided to achieve a working superchip. Built-in test circuitry automatically checks the functionality of each macrocell and reconfigures their interconnections as needed. Triply redundant busses are used on the chip to ensure reliable connections between the various macrocells and I/O ports.

Two large area, 0.5 micron chips with high functional complexity ("superchips") were originally begun in Phase 2 in addition to a BIU chip. The superchips included a signal processor (in CMOS at Motorola and a convolver in bipolar at TRW). These superchips were designed but not built because the processing technology could not project a sufficiently high yield to make their successful fabrication likely. Instead the CPUAX, which consisted of the

central processing arithmetic portion of the signal processor, and the BIU were designed, fabricated in 0.5 micron CMOS, and successfully demonstrated.

Central Processing Unit Arithmetic/Extended (CPUAX): (Figure 3.12) The CPUAX chip is a large arithmetic unit with internal functional redundancy that serves to provide both initial high yield and extended life through self-reconfiguration every time the chip is powered-up. There are a total of 142 macrocells of nine different types in the CPUAX. Of these macrocells, 61 must be functionally active for the CPUAX to work, leaving 81 redundant cells for use in the re-configuration procedure.

The CPUAX performs dual, floating point computation in the MIL-STD-1750A format. The chip holds 4096 words of 32-bit table memory with 7-bit error detection and 96 words of 32-bit data memory. There are two 32-bit input and output ports and built-in self-test functions. The unit is capable of operating at 200 MFLOPS throughput rate.

The macrocells that comprise the CPUAX and the number of each required for full performance operation are: Memory Interface/Write (1), Memory Interface/Read (1), Address Generator (2), One Port RAM (39), Control Disable Block (8), Storage Element (6), Arithmetic Logic Unit (2), Multiply/Accumulator (2).

Bus Interface Unit (BIU): The Bus Interface Unit conforms to the same specifications as the BIUs of the other Phase 2 contracts. The specifications are documented in Reference 3.1. The BIU serves to interface the internal superchip data buses and test maintenance buses to the standard PI bus and the standard TM bus, respectively, for communication with external electronics. The PI bus interface operates at a maximum clock rate of 25 MHz and a throughput of 20 Mwords/sec.

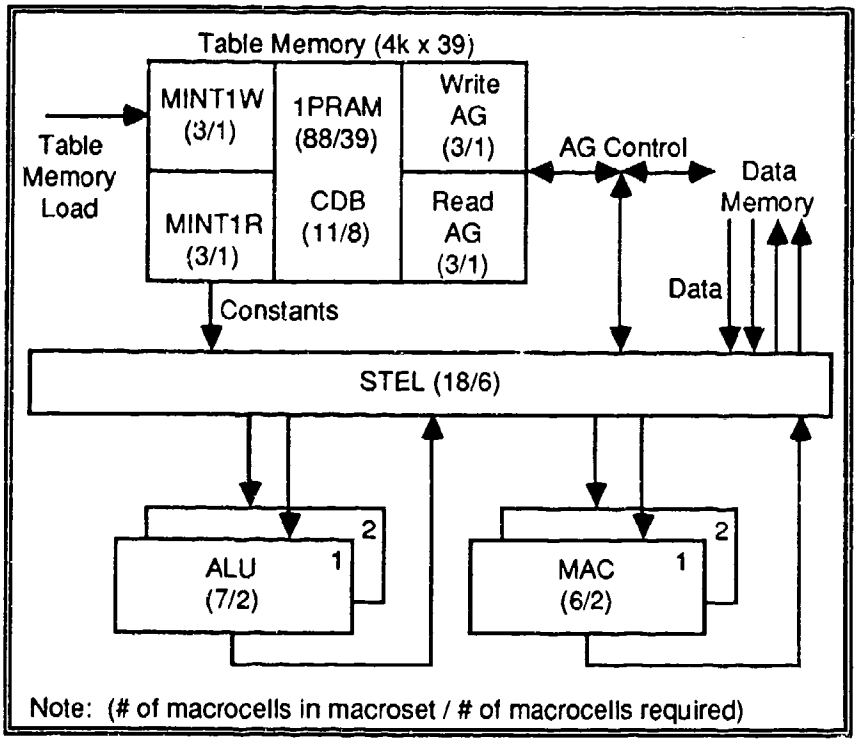


Figure 3.12 Central Processing Unit, Arithmetic Extended (TRW)

CHAPTER 4 - BRASSBOARD DEMONSTRATIONS

CHAPTER 4

BRASSBOARD DEMONSTRATIONS

The products that resulted from the development tasks carried out by the contractors during Phases 1, 2, and 3 of the VHSIC program were tested, evaluated, and demonstrated in a variety of ways. The Phase 1 and Phase 2 contracts called for the demonstration of VHSIC chips in brassboards which performed a useful system function --- such as high speed sorting of signals in electronic warfare receivers, or coding/decoding of secure communication channels. In most cases, the brassboard was designed to demonstrate a specialized function of a particular class of military equipment. In a few cases, the brassboard demonstrated a generic algorithm such as the Fast Fourier Transform which is widely used in signal processing applications.

In addition to the brassboard demonstrations described in this chapter, a substantial effort at Army, Navy, and Air Force facilities went into the test and evaluation of individual chip types delivered to the Services under the contracts. This activity is discussed in Section 3.2.1.

Finally, the VHDL and other software tools developed under VHSIC have been demonstrated through extensive use in many projects in order to improve the efficiency of the design process and to document the hardware design data. VHDL and supporting software tools allow the performance of a system to be analyzed through modeling and simulation. Modeling allows the designer to capture, refine, and verify the properties of the system at all levels of design. When the model can be simulated, then the behavior of the system in various dynamic states can be observed. Some of these software demonstration projects are discussed in Section 5.6.

4.1 Phase 1

4.1.1 Electrooptic Signal Processor (EOSP) - Honeywell

Honeywell designed its Phase 1 chips and demonstration brassboard for use in the processing of electrooptical image signals. The final demonstration of the brassboard was conducted for a tri-Service review team on September 17, 1985. Correct operation of the EOSP chip set was successfully demonstrated while performing two different image processing algorithms in near real-time. The capabilities of the chip set to perform self-test and to perform dynamic reconfiguration for fault tolerance were also successfully demonstrated.

The focal point of the brassboard demonstration was the segmentation algorithm. Microcode for the low-level computational primitives, which support both the execution of the algorithm and the fault tolerance functions, was generated and stored in the on-chip ROMs of the sequencer and arithmetic chips. These primitives were sufficient to demonstrate the image segmentation algorithm as well as several other general purpose signal and image processing algorithms.

Three manuals were prepared for delivery to the Air Force VHSIC Program Office. The "VHSIC EOSP User Manual" provides information to future users of the EOSP chip set. The tools utilized, the design methodology, and applications information is also provided. The "VHSIC Brassboard Development System Reference Manual" contains an operational description of the hardware and software developed under the VHSIC Phase 1 development program in support of the EOSP brasssboard development and demonstration. It can be used to operate and maintain the system. The "VHSIC EOSP Brassboard Reference Manual" provides descriptions of the brassboard hardware and firmware developed specifically to house, interconnect, and operate the Honeywell EOSP chip set for the purposes of test and demonstration. See Reference 2.11.

4.1.2 Enhanced Position Location Reporting System (EPLRS) - Hughes

The manpack user unit of the Army EPLRS (formally identified as the PLRS JTIDS Hybrid system) was the vehicle for brassboard demonstration of the Hughes VHSIC anti-jam communication chipset. The primary objectives were: (1) to demonstrate the performance capabilities of the three chip types to the greatest extent practical for this application and (2) to evaluate the potential benefits of the chip set for that system. The versatility of the chips was demonstrated by implementation of six new higher performance waveform modes in the brassboard unit and in a companion Demonstration Driver Unit. By capitalizing on the microprocessor controlled reconfigurability of each member of the chip set, a relatively simple technique for dynamically "programming" the signal processing parameters used by each chip was also demonstrated. The demonstration was successfully conducted at Hughes in late 1986. See References 4.1 and 4.2. Further activity in the insertion of VHSIC into the EPLRS is described in Section 5.1 (Army Insertions).

4.1.3 Acoustic Signal Processor - IBM

IBM successfully demonstrated its Phase 1 Complex Multiply and Accumulate (CMAC) chip in an acoustic signal processing brassboard on May 1, 1984. This demonstration verified the ability of the CMAC to carry out high speed signal preprocessor functions in Navy anti-submarine warfare equipment.

For example, the Navy's P3-C ASW aircraft processes and analyzes acoustic data from ocean sensors (sonobuoys) in the AN/UYS-1 Advanced Signal Processor (ASP). The data from each sonobuoy is demultiplexed by the Input Signal Conditioner (ISC) of the ASP into three separate data channels. These data channels are then analyzed by the ASP Arithmetic Processor (AP) to provide target detection and bearing information. The brassboard contained four VHSIC CMAC chips configured as a digital, high throughput replacement for the primarily analog ISC in the AN/UYS-1. It also contained an Availability Management Subsystem that monitored the status of the four CMAC chips and demonstrated all of the built-in-test and fault tolerant features of the CMAC. The brassboard subsystem was designed

as a plug-in, connector-compatible replacement for the ISC which would double the number of sonobuoys that could be processed by the ASP. No hardware modifications to the AN/UYS-1 were necessary.

The VHSIC brassboard not only demonstrated the VHSIC technology, design tools, and CMAC chip performance but also the high speed control concepts that were developed for the CMAC signal processing. It provided a baseline example for future technology insertion into the front end of acoustic signal processors. See Reference 2.13.

4.1.4 Multimode Fire and Forget Missile - Texas Instruments

The Texas Instruments Phase 1 demonstration brassboard was originally defined to support the Multimode Fire and Forget (M^2F^2) missile. During the program, the scope of the brassboard effort was expanded from a limited laboratory demonstration to a full flight test program. In order to have an early demonstration of the Phase 1 VHSIC chips, a new brassboard was designed and developed to verify the principal computational and I/O features of the chip set. In addition, a MIL-STD-1750A evaluation computer was developed as a testbed for functional evaluation of the DPU chip. High density array processor (AP) and data processor (DP) modules were also developed and delivered to several VHSIC insertion programs.

The brassboard developed to demonstrate the operation of the chip set contains a small MIL-STD-1750A computer which uses a DPU and two SRAMs as the CPU. Control and operator interface to the brassboard is provided from a personal computer. A successful demonstration of the MIL-STD-1750A evaluation computer was conducted in July 1986 at the Wright-Patterson AFB Software Engineering and Avionics Facility. See Reference 2.14.

4.1.5 Electronic Warfare Demonstrations - TRW

TRW demonstrated a preliminary version of its electronic warfare brassboard in December 1984, using seven functional VHSIC chips. The demonstration included a signal pre-processor, a pulse simulator, a maintenance system, and a VAX 11/788 as the testbed control computer. Final demonstration and acceptance by the Navy took place on April 16, 1985. A total of 57 VHSIC chips were used which included all eight types of the original TRW/Motorola chip set. This EW demonstration verified the operation in a high pulse environment, the self-test capability, and the reduced weight, size and power consumption. See References 4.3 and 4.4.

TRW also demonstrated the use of its Phase 1 chips in the AN/ALQ-131 equipment, an airborne pod-mounted electronic countermeasure (ECM) system. The VHSIC chips were used to redesign one of the circuit cards into a VHSIC Transmit Control Assembly (VTCA). Demonstration of the VTCA in the system in December 1985 was the first demonstrated insertion of VHSIC chips into an operational military system. The initial flight test of the

pod took place in July 1986. See page 1 of the VHSIC Annual Report for 1986, (Reference 2.27).

4.1.6 SRAM, Gate Array, Arithmetic Unit, and an ATF Complex Vector Processor - Westinghouse

Westinghouse demonstrated a 64k memory board (containing RAMs and gate arrays) and a custom chip, the pipelined arithmetic unit (PLAU), with control provided by a (non-VHSIC) 1750A data processor. These demonstrations were completed in January 1987. In addition, Westinghouse demonstrated a Complex Vector Processor (CVP) module for the Advanced Tactical Fighter (ATF) avionics using over fifty VHSIC chips. The CVP demonstration was completed in November 1988.

The CVP module contains over 500,000 gates and 512k bytes of memory and was demonstrated to operate at a 25 MHz clock rate. The CVP can process large vectors of 32-bit complex data. One of the key vector instructions in the instruction set is the Fast Fourier Transform. See Reference 2.15.

4.2 Phase 2

4.2.1 Acoustic Beamformer Module - IBM

For the demonstration of its 0.5 micron Phase 2 technology, IBM designed an acoustic beamforming brassboard. The beamforming computations dominate the throughput requirements of ASW systems as the size of the acoustic sensor array grows and the new ASW systems require the levels of speed and throughput provided by the IBM chip set. The demonstration of the brassboard with its 0.5 micron multi-chip modules took place on December 1, 1988. The beamformer algorithms as well as various diagnostic routines were successfully run at a 50 MHz on-chip clock rate. See Reference 3.45.

4.2.2 Cruise Missile Advanced Guidance - Honeywell

The plans and schedule for this Phase 2 brassboard demonstration are discussed in Section 5.3.3.

4.2.3 Demonstration Module - TRW

The TRW Phase 2 demonstration module consisted of three circuit boards using five VHSIC chip types --- the CPUAX superchip, Bus Interface Unit (BIU), Microcontrol Unit

(MCU), Universal Processor (UP), and Address Generator (AG). The signal processor architecture was divided into a self test and configuration processor (STCP), an I/O interface, and a central processor unit (CPU). The STCP was implemented as a single board with the UP plus an instruction ROM, 5k-word x 16-bit data RAM, and timing and control interface circuitry. The CPU was implemented in two boards. The first contained a 4k-word x 16-bit control memory with one MCU and a 4k-word x 32-bit vector memory with four AGs. The second board contained the CPUAX and interface circuitry. The entire unit was housed in a custom enclosure of 2016 cubic inches weighing 20 lbs.

The STCP, a 12.5 MIPS, 16-bit RISC computer, successfully executed the built-in self test (BIST) and configuration of the CPUAX. The BIST routines identified good and bad logic macrocells and memory macrocells within the CPUAX and then correctly configured around faulty macrocells to give a working CPUAX. The BIST operation ran at 16 MHz.

The fully configured CPUAX performed a radix-2, in-place, decimation-in-time, 512-point fast fourier transform (FFT) algorithm on several waveform types. The FFT algorithm used 83% of the internal processing throughput of the CPUAX and exercised almost all of the logic, memory, and buses of the CPUAX. The expected results for each input waveform were calculated off-line on a Sun computer by a program written to emulate the CPUAX precision. The results from the CPUAX exactly matched the predicted results. The BIST routines controlled by the Universal Processor provided identification and isolation of a short circuit (caused by a mask error) which severely loaded down an internal bus and limited the clock rate for the FFT demonstration to 10 MHz.

The tests demonstrated the feasibility of programmable, monolithic, wafer-scale integration by proving the functionality of the CPUAX, the largest monolithic logic circuit ever built. The redundancy in the CPUAX design enabled the achievement of a functional circuit, with 1.7 million devices designed to 0.5 micron rules, despite the presence of processing defects.

CHAPTER 5 - TECHNOLOGY INSERTION

CHAPTER 5

TECHNOLOGY INSERTION

The migration path from technology development to the full use of that technology in the acquisition of fielded military equipment can be a long and difficult one. As pointed out in the paper in Chapter 2 by Mr. L. W. Sumney, VHSIC was not ". . . intended, directed, nor funded. . ." to do that. The 1982 report of the Defense Science Board Task Force on VHSIC (Reference 5.1) discussed the problems of technology insertion in terms of the DoD acquisition process and noted that:

> "*. . . The importance of rapid technology insertion to provide visible and useful demonstrations of the VHSIC chip technology cannot be overemphasized. . . . U.S. military systems must be provided with the technology rapidly in order that key defense systems can become operational when needed to offset the continued growth of adversary forces and to maintain a credible response capability. The motivations for technology insertion are:*
>
> - *Higher performance in an existing function at the same cost*
> - *Equivalent performance at lower cost*
> - *Performance of a new function*
> - *Higher reliability*
> - *Reduced size and weight*
> - *Lower power*
> - *Ease of maintenance*"

But that report also pointed out that . . *"The weapon system acquisition process must accommodate realistic technology insertion plans instead of their coming as an afterthought."*

A notable example of the successful insertion of VHSIC technology that has passed the full scale development stage and is scheduled for early (1991) insertion is that of the AN/APG-68 airborne radar signal processor by Westinghouse for the F-16 aircraft. For additional examples of early insertions see the paper at the end of this chapter.

This chapter describes a number of the insertions of VHSIC technology into systems that were formally included in the VHSIC program and were jointly funded by the system program office and by VHSIC. The scope of the insertions ranges from (1) extensive hardware re-design of a system to use VHSIC hardware with the expectation that the VHSIC version would become the production prototype, to (2) detailed studies of the benefits that VHSIC insertion would have if it were implemented. Some projects that started out as firm hardware insertions had to be terminated because of major changes in the overall system development plans.

This chapter also includes some Air Force logistics retrofit projects and several software projects which were undertaken to demonstrate how effectively VHDL could be used to provide computer based documentation for the specification, design, and procurement of large systems.

In addition to these formal VHSIC insertion projects there were many independent Service sponsored insertions which are listed in Section 5.4 by name only.

The following paper has been included to describe the impact that VHSIC is projected to make on the total system life cycle --- design, acquisition, maintenance, and reprocurement. All of these problems grow more difficult and costly with the increased complexity of systems but the VHSIC technology provides a potential for more effective management of those complexities.

The Impact of VHSIC on the DoD System Life Cycle

Joel M. Schoen
The MITRE Corporation

The increased speed and density achievable with VHSIC technology makes it possible to design very complex electronic systems on a single silicon chip. The human mind, however, cannot handle the details of such complex systems without the assistance of computer aided engineering (CAE) tools. Therefore, in addition to the primary goal of developing the technology to fabricate high speed, high density IC chips for use in military weapon systems, the VHSIC program also supported the development of the CAE software tools needed for their design and application. The level of complexity achievable with these chips continues to increase with time as the submicron technology pioneered by VHSIC is transferred into the broad semiconductor community. The VHSIC insertion process then becomes, to some extent, an exercise in the management of greater and greater complexity.

The VHSIC Hardware Descriptive Language, VHDL, was developed as part of the VHSIC Program. A hardware descriptive language allows a hardware designer to describe or model the design of a digital circuit in a high level computer language. The model can then be used as a simulation of the real hardware to verify the correctness of the design. In 1987, VHDL became an Institute of Electrical and Electronic Engineers (IEEE) standard, and is rapidly becoming the medium for exchange of information concerning the behavior of digital components, subsystems, and systems. Requirement 64 of the MIL–STD 454L mandates the delivery of VHDL models of all application specific integrated circuits designed for the DoD after September 30, 1988. Moreover, there is a concerted effort by the Electronic Industries Association (EIA) to acquire VHDL models of standard commercial components. The availability of a library of VHDL models of

commonly used components will encourage VHDL simulation and verification at the printed–board level and beyond. It will also stimulate component reuse. It is anticipated that VHDL models will be required by the DoD for all printed board assemblies designed after 1990.

The use of VHDL to model and simulate digital entities at varying levels of abstraction, from the behavioral level to the logic gate level, enables one to go beyond the management of chip complexity. VHDL becomes a key tool for efficient system design. VHDL can be used to describe systems and subsystems as well as chips and, at the same time, can record design progress and document design intent. It does all this in a common data base. For example, the conformance of a design to its specification can be validated by means of VHDL simulation. In the same way, the performance of the chip within the system can be simulated using a VHDL description of the system. In this way, one can simulate the operation of application specific integrated circuits within the system for which they are intended. Any incompatibilities or design flaws can then be detected and corrected before any real hardware is built. Current CAE tools and fabrication processes can produce application specific integrated circuits with first–pass success rates in excess of 90%. By using the full chip plus system simulation capabilities of VHDL it will be possible to sharply increase the first–pass success rate for electronic system designs. This will have significant impact on system development cost.

The ability of VHDL to describe the requirements of digital integrated circuits (simply by describing the desired behavior of the circuit at its boundary terminals) makes it much easier to reprocure obsolete circuits. Rather than having to recreate the chip requirements from obsolete documentation, the VHDL description provides both a human– and machine–readable data base that can be used with logic synthesis and silicon compiler tools to create correct–by–construction designs. Structural and behavioral VHDL models have also been used as inputs to model–based diagnostic reasoning systems. Such systems are being developed to evaluate system diagnostic capabilities and to implement field and/or depot maintenance systems. VHDL therefore optimizes not only the design phase of the system life cycle, but also provides the software tool which can automate and improve system logistics.

Over the next few years, one can project that DOD will use VHDL as a vehicle to communicate technical information on digital systems with contractors and potential contractors throughout the system design cycle. This use of VHDL will apply at the digital system and subsystem levels, in addition to the integrated circuit level mandated by MIL–STD 454. Moreover, VHDL models may be required as deliverables as the design progresses, as well as for final documentation. The advantages of using VHDL for technical information transfer in the acquisition and life cycle support process will be treated in the remainder of this paper.

VHDL in the System Acquisition Process

The acquisition of modern electronic systems is made more difficult and costly by the continuously increasing complexity of the hardware, software, and documentation involved in the process.

Defining and communicating accurate, complete, and unambiguous requirement specifications early in the program is extremely difficult. On the other hand, the cost of rework in response to specification changes becomes more significant as the design progresses. Therefore, any additional work spent generating better specifications at the beginning is more than rewarded by reduction in rework costs.

Complex systems inherently require complex documentation. The procurement managers cannot absorb the contents of all the documents needed to comprehend all facets of the system design. The program office therefore perceives that the more complex the design, the greater the risk, even to the point that the system may not be successful.

During the development phase of a system, one of the most critical tasks is to distribute the total system requirements among the subsystems in an accurate and consistent fashion, so that when the system is assembled, the components will work together as intended and the system as a whole meets its requirements. "Configuration items" represent various components in the system hierarchy which are often documented independently of each other once the system partitioning has been done. Testing the configuration item to verify that the item will work in the system is not always straightforward. The requirements specified for the configuration item cannot necessarily be traced back to the system requirements in an obvious way. The configuration item may meet its own requirements and still fail to operate properly in the system.

The use of VHDL in the system acquisition process addresses many of these problems. It also makes effective use of computer aided engineering tools. It promotes better communications between the contractors and the program office, and provides better visibility into the design. It will lead to a higher level of confidence that the system will work properly when all its components are assembled. Moreover, it promotes the continuity of system data throughout the system's life cycle, from specification to implementation to maintenance.

The development of simulation models, as part of the specification development process, will assist both Government and contractors in eliminating ambiguities. VHDL provides a human– and machine–readable medium for precise communication between the project office and the contractor on system technical issues. Delivery of models, with increasing levels of detail as the design progresses, gives the project office continued visibility into the design process and, therefore, a higher level of confidence as to design fidelity with respect to the initial requirements. In addition, the ability of the VHDL simulators to work with models defined at higher functional levels can provide better allocations of system functionality to subsystem elements.

VHDL Support of Maintenance and Reprocurement

Recent developments in the field of artificial intelligence have resulted in model—based diagnostic reasoning systems to assist in maintenance at both the line and the depot levels. They can also be used to evaluate the self—test capabilities of systems. Model—based systems have an advantage over rule—based systems in that they can reason about system failures that have not been previously anticipated. Model—based reasoning systems can use their models to diagnose new failure modes. Several model—based diagnostic reasoning systems are being developed to use VHDL structural and behavioral models. A distinct advantage of the use of VHDL models is that the same model used to develop the system is used to diagnose system failures. No information is lost in constructing the diagnostic model.

Similarly, the use of VHDL models developed during system design can be used as a starting point for part reprocurement and second sourcing. This minimizes the need to collect and integrate data from various deliverables to create a reprocurement package. The VHDL model contains all requisite information about the component requirements and can be used in a simulation to demonstrate that the reprocured part will work in the system. The cost and time for reprocurement can thereby be minimized.

Summary

The benefit of utilizing VHDL for information transfer and simulation throughout the specification and development phases of the system acquisition process include accurate description of system requirements. Simulation is an accurate, efficient, and less costly way to monitor the progress of the design and development phases of system procurement. The use of VHDL during these processes will increase the probability of design success because requirements at the component level can be related to requirements at the system level. It results in easy tracing of requirements at all levels of detail and reduces cost by reducing the number of design revisions required. VHDL documentation of a system provides an archive for reprocurement, maintenance, support, and reuse. In this fashion, the VHDL models developed during the acquisition process provide for continuity of the design data through the system life cycle.

The introduction of these changes to the process by which we specify and design systems, based upon new CAE tools which fully use the VHDL and its capabilities, can provide tangible and far—reaching benefits. As these benefits become evident through increased experience, the VHDL and its future extensions are sure to become widely used in the DoD acquisition process.

5.1 Army System Insertion Projects

5.1.1 Miniaturized ESM/ELINT Direction Finding and Location Intercept (MEDFLI)

The goal of the MEDFLI program is to produce small lightweight EW payloads for airborne and ground applications that can handle the dense emitter signal environment of the 1990s and beyond. The objective of this insertion project is to improve the throughput and reliability of the MEDFLI signal processor, called the Modular Adaptive Signal Sorter (MASS), and to develop a special purpose VHSIC Threat Association Module (VTAM) for EW processing applications.

VMASS

The VHSIC MASS will process raw radar data to perform sorting, de-interleaving, and target characteristic functions. The program was started in August 1987 with General Electric as the contractor. It will use VHSIC technology to obtain faster signal processing capabilities and an overall reduction in size, weight, and power consumption. Five VHSIC chips are being developed and will be integrated into the VMASS hardware.

The design and implementation of the five VHSIC chips to replace the several boards will achieve the following:

	MASS	VMASS
Size	470 in^3	94 in^3
Weight	62 lbs	12 lbs
Speed	1	6:1
Power	255 W	53 W
Boards	13	3
CPU	16 bits	32 bits
Clock rate	12.5 MHz	20 MHz

In March 1990, the VMASS VHDL add-on was begun to fully describe and document the chips in VHDL. The risk of possible design obsolescence is greatly reduced by implementation in VHDL. An additional objective of this effort is to have hardware/software engineers evaluate the status of VHDL and related tools and determine the ability of the design community to apply VHDL to existing and future designs.

A further application of the VHSIC technology will be the extension of the VMASS System to a highly mobile single board MANPACK System. The design and development of MANPACK will provide a lightweight, powerful target tracking system unit that will include a self contained antenna, receiver, and processor. Four of the VMASS chips will be utilized

in addition to a newly designed VHSIC chip. VHDL behavioral and structural descriptions will be provided.

The impact of VHSIC technology for VMASS and MANPACK will provide two new advanced EW signal processing systems with immediate improved performance and significant lower size, weight, power, and cost. The newly developed chips will have many applications for other Army programs. The early-on capture of chip designs in both behavioral and structural VHDL will greatly reduce the risk of obsolescence and facilitate parts replacement. Details will be found in Reference 5.2.

VTAM

The VTAM program was started in 1985, with ESL, Inc., to take radar characterization reports from an electronic intelligence (ELINT) processor and compare them against a data base to determine the identification of the radar and, if possible, the platform. The VTAM also performs tracking of the emitter and determine geographical location. The VTAM uses VHSIC Window Addressable Memory (WAM) chips to perform very high speed data comparisons for various SIGINT and ELINT applications. After successful laboratory testing, the VTAM was integrated with the MEDFLI testbed during 1989/90. The chips developed under this program have already found SIGINT applications in other DoD programs. Details will be found in Reference 5.3.

5.1.2 Light Helicopter Program (LHX) Mission Computer

During 1985 and 1986, design work on advanced cockpit and mission equipment for the LHX helicopter program included a task to provide preliminary designs of a mission computer using VHSIC chips. The design effort was jointly funded by the Army AVSCOM LHX Program Office and the VHSIC Program Office. See References 5.4 - 5.8.

The LHX contractors have later formed into two teams --- Boeing/Sikorsky and McDonnell/Bell. Using the preliminary mission computer designs as a base, each of the two LHX contractor teams continued the design of a VHSIC version of the computer during 1987/1988. The contractor teams have demonstrated selected features and functions of breadboard signal and data processors, memory management, sensor data distribution, video processors, and bus interface modules. The design of the LHX depends on a high degree of automation in the helicopter platform and mission systems. Because of the weight and space limitations of the platform, the mission requirements can best be met with a VHSIC computer. Using alternative, less capable technologies, would result in more limited system performance.

These detailed mission computer design efforts have reduced the technical risk to acceptable levels for the beginning of the formal DEM/VAL program. The DEM/VAL effort began in November 1988 and was scheduled to run for 23 months. Upon completion of this effort the government will select one contractor team to continue into the formal FSD program to begin in December 1990. Development and formal laboratory demonstration of a complete VHSIC mission computer capability is part of the DEM/VAL program.

5.1.3 Enhanced PLRS User Unit (EPUU)

The PLRS (Position Location and Reporting System) is designed to provide Army ground troops with a system for battlefield tactical data transmission. A VHSIC version of the EPUU, which will have a three-fold increase in signal throughput, is being developed by Hughes Aircraft for the Army CECOM. The increased capacity is needed to meet the growth anticipated in the volume of data which must be electronically exchanged on the battlefield. A VHSIC chip set that will update the Signal Message Processor (SMP) module in the EPUU has been designed by Hughes Aircraft and fabricated by AT&T. There are also plans to design a second chip set for a second module in the EPUU. These two VHSIC modules will also reduce both the logistics and acquisition costs associated with the planned production of more than 20,000 EPUUs. Preliminary Government estimates indicate that over $100 million can be saved in acquisition and life cycle cost by this use of VHSIC components in the PLRS system.

On December 11, 1986, Hughes demonstrated the fully functional VHSIC-1 devices which transferred messages between a brassboard VHSIC EPUU and standard units. On March 3, 1988, the contractor demonstrated that the EPUU brassboard had a threefold increase in signal throughput over current designs. Preliminary results indicate that the performance of this EPUU is better than predicted by mathematical models. The EPUU brassboard contract was completed in March 1989, with acceptance demonstrations and delivery of the brassboard hardware.

The prototype SMP modules were completed in April 1990, tested, and delivered in June 1990. The modules will be integrated into twelve prototype VHSIC EPUUs which will be demonstrated and then undergo performance testing during 1990. See References 5.9 - 5.11.

5.1.4 Firefinder Radars

The Firefinder radars detect sources of hostile mortar, artillery, and rocket fire and accurately compute their location for the direction of counterfire. The use of VHSIC technology in the signal processor will significantly improve the performance of the weapon location computation, provide classification of the weapon type, and enhance the system performance in the presence of EW threats. The VHSIC processor reduces the processor power consumption by 60% and the parts count by 75%, which makes it a key subsystem in the evolution to a single vehicle Firefinder system from its present multiple vehicle configuration. Installation of the radar on a single vehicle will reduce the crew size from eight to four personnel for the AN/TPQ-36 version of the radar. The total projected life cycle cost savings is $430 million.

The program was initiated in September 1984 by the Army LABCOM with a contract to Hughes Aircraft. An initial systems analysis was followed by design, simulation, and fabrication of a signal processor module with four VHSIC chip types which were fabricated by LSI Logic. This module is broadly applicable to numerous computationally intense signal processing applications.

In 1989, a processor brassboard using eight VHSIC processor modules was integrated with a Firefinder radar and operated in a demonstration of the advanced electronic survivability of radar systems in the presence of hostile jammers. The system level testing demonstrated excellent suppression of jamming interference from both CW and pulsed jamming sources. A significant improvement in jammer cancellation performance over commonly used analog circuit designs was also demonstrated. The use of VHSIC technology permitted a significant reduction in size, cost, and weight and made viable the application of this high performance digital processing technique to mobile systems. The success of the VHSIC processor brassboard has made it a candidate for insertion in the upgraded AN/TPQ-36 or Firefinder II program scheduled to start in FY92. The VHSIC processor is also considered to have potential for application to ground based sensors of the Army Forward Area Air Defense (FAAD) system.

Other applications of this VHSIC processor demonstrated by Hughes Aircraft include the MK-48 ADCAP torpedo and Advanced Low Frequency Sonar (ALFS) for deployment as a dipping sonar system from helicopters.

5.1.5 Common Module VHSIC Integrated System (CVIS)

As part of the Army's Heavy Forces Modernization (HFM) program, the Armament Research Development and Engineering Center (ARDEC) is developing a standard signal processing system that is applicable to the M1 tank and other ground combat vehicles. The program is called the Common Module VHSIC Integrated System (CVIS).

The CVIS family of modules includes a 1750A data processor, an array processor, a global memory, a 1553B interface, and several other I/O modules. The modules interface to the VHSIC Phase 2 Pi-Bus and TM-Bus and will be packaged on double-sided surface mount SEM-E circuit modules. Increased speed, as well as reductions in weight, size, and power are expected through the use of VHSIC chips. The contractors are Westinghouse and General Dynamics (References 5.12 and 5.13). Laboratory demonstration of CVIS by General Dynamics was performed in April 1990. Follow on field demonstrations are being considered.

ARDEC plans to demonstrate a CVIS processor module in 1990 on a fire control platform and later in an HFM combat vehicle.

5.1.6 Tube Launched, Optically Tracked, Wire Guided Missile (TOW) VHSIC Automatic Target Tracker

The goal of this Army MICOM project was to upgrade antitank missile guidance from semi-automatic to fully automatic. This would relieve the gunner of the task of precision target tracking and also allow the control of more than one missile at a time. The development of an automatic target tracker for anti-tank missiles would benefit other weapons such as laser designators and gunfire control systems.

Various target trackers have been under development for many years with mixed success because of the difficult target signal characteristics. In addition, it is usually required that the expanded capability fit in the existing system volume. Because very high computer power is required for automatic tracking, it has been concluded that the only hope of meeting this goal is with VHSIC (or VHSIC-like) components.

The effort began with a pre-VHSIC breadboard target tracker built and tested by Texas Instruments. The results were encouraging enough to begin a VHSIC insertion brassboard effort in late FY85. Due to lack of funds and discouraging progress, the contract was terminated in 1988. A new contract was then let by DARPA to TI to finish the system and to perform the field/flight tests. The tests were conducted in early FY89. The test of the fully automatic VHSIC TOW system included tracking of two missiles simultaneously to two targets. In the field flight tests, single missiles were tracked successfully to non-moving targets, but the dual missile attempts were not successful.

In spite of the less than desired results, the program was considered useful for the lessons that have been learned which are applicable to the present and future developments. The eventual development of the improved TOW and LOSAT fire control systems are expected to benefit directly from these lessons. See References 5.14 and 5.15.

5.1.7 Hellfire Imaging Infrared Seeker

The Imaging Infrared (IIR) seeker for the Hellfire Fire and Forget missile system requires a signal processor with high data throughput, but which is very small, light weight, and low powered. Only through the use of VHSIC technology in the seeker and processor can this be accomplished.

Development contracts for a VHSIC processor for the seeker were awarded by MICOM in September 1985 to Texas Instruments, McDonnell-Douglas, and Ford Aeroneutronics. At the beginning of 1987, development of the VHSIC processor hardware for insertion into the Hellfire IIR seeker was well underway. However, the Joint Services Seeker Program, which was to furnish the sensor hardware for insertion into the Hellfire system, had been terminated.

In order to complete the program, the Texas Instruments Hellfire VHSIC insertion contract was modified to include the fabrication of a seeker head. The other contractors continued work only on the processor electronics. The Texas Instruments VHSIC chip set, which was the basis of both the TI and McDonnell Douglas activities, did not perform to specifications. As a result, during 1988, the TI and McDonnell efforts were discontinued.

The Ford program continued to successful completion in late FY89, producing a VHSIC Configurable Pipelined Processor (CPP) based on a gate array designed by Ford Aerospace and fabricated by Ford/LSI. This activity has been followed closely by MICOM and Naval Weapons Center (NWC) and both laboratories are planning to incorporate the CPP into in-house image processing and seeker development activities.

A follow-on contract is in place with Ford Aerospace to develop CPP programmed software and techniques and to train MICOM and NWC personnel in its use. CPP based

seeker electronics is a candidate for use on a current MICOM development program which will flight test seekers on a missile. See References 5.16 - 5.18.

5.1.8 Multi-Role Survivable Radar (MRSR)

The Multi-Role Survivable Radar (MRSR) fulfills the critical needs of Army air defense commanders who must operate effectively in an electronic countermeasures (ECM) and anti-radiation missile threat environment. The MRSR minimizes these threats by using frequency agility over its operation bandwidth, low peak power levels, and extremely low azimuth sidelobes. The MRSR is designed to go directly into the HAWK system.

The objective of this Army MICOM insertion effort is to determine the feasibility of designing a VHSIC signal processor which meets the requirements of the MRSR system.

Raytheon and Westinghouse completed designs of a VHSIC signal processor for their respective versions of the MRSR. The Westinghouse design is based upon a set of configurable gate arrays (CGAs) developed in the Westinghouse F-16 VHSIC Programmable Signal Processor (VPSP) Program. These CGAs are supplemented with three CGA personalizations designated specifically for the MRSR Program. The Raytheon MRSR signal processor design is based upon the Raytheon developed family of core chips.

Each contractor demonstrated that both the VHSIC manufacturing base and sufficient design tools are available to design the signal processing susbsystems for the MRSR using Phase 1 VHSIC parts.

5.1.9 Application to Army Command and Control System (ACCS)

The VHSIC application to ACCS project was a study by TRW to investigate the need for improved interoperability between the ACCS and its supporting systems. The primary goal was to determine if existing ACCS interface facilities can be effectively integrated into a generic, programmable communications unit with improved performance using VHSIC technology.

The initial part of the study investigated and identified existing equipment interface functions which could be implemented in VHSIC technology with increased functionality, improved performance, and expansion capabilities. The second, detailed part of the study provided in-depth analysis of one interface to ascertain the benefits of the proposed VHSIC design and its projected cost. The study started in February 1988 and continued for one year. See Reference 5.19.

5.2 Navy System Insertion Projects

5.2.1 AN/UYS-2 Enhanced Modular Signal Processor (EMSP)

The EMSP is the Navy's next generation standard signal processor. This system is designed to meet the Navy's air, sea, and shore signal processing requirements through the 1990s in sonar, radar, electronic surveillance, and communications systems. All new Navy programs requiring signal processing must use the EMSP, unless a waiver is granted.

The AN/UYS-2 is constructed of Standard Electronic Modules (SEMs) and is designed to be interoperable with other standard Navy computers. It has a modular, open architecture comprised of a series of functional elements connected via a non-blocking data switch that readily allows technology insertion in the form of new functional elements.

AT&T, under contract to NAVSEA, performed the system integration effort for VHSIC insertion. Honeywell, as subcontractor, has developed the chips, circuit card assemblies, and SEM modules for the demonstration model. VHSIC 1.2 micron CMOS technology was used in four personalized 20k gate arrays (the FIFO, FPM, RALU, and MEMINT chips) for the EMSP, which is a 16-bit floating point signal processor. Each EMSP will use up to 100 chips.

In April 1987, the interoperability and signal processing capabilities of the system were demonstrated to the Navy. In September 1987, SEM cards were inserted into the EMSP environmental prototype model and demonstrated while the system processed a sample of tactical data. A detailed analysis shows that the floating point AU has 46% more throughput than the fixed point AU on a comparable task basis (See References 5.20 and 5.21)

Development of the processors has been completed. Honeywell delivered working breadboards to AT&T in October 1989. The SEM-B processor is in production. Preproduction deliveries of the SEM-E processors are underway.

As a further upgrade, the Naval Sea Systems Command (PMS-412) will demonstrate the use of VHDL in developing a Matrix Processor (MP) functional element for the AN/UYS-2. VHDL descriptions and simulations will be used to evaluate the matrix processor supplied by each of several contractors. The VHDL modeling, using Navy supplied algorithms, will allow the Navy to determine efficiency and establish AN/UYS-2 compatibility prior to awarding a full scale development contract. VHDL description of the AN/UYS-2 interfaces will be supplied to the winner. These data are expected to be ready in 1991 and will allow any contractor to simulate, design, and build any processor for integration into the data-flow environment of the AN/UYS-2.

5.2.2 AN/AYK-14 VHSIC Processor Module (VPM)

The AN/AYK-14 Navy Standard Airborne Computer is a modular, general purpose digital computer that is currently used by more than 20 major weapon systems. This computer is functionally and physically partitioned into replaceable modules to provide operational flexibility. The computer is used in such weapon systems as the F/A-18, AV-8B, F-14D, V-22,

EA-6B, E-2C, SH-60B, P-3C, EP-3, ES-3, MK50, and the Automatic Carrier Landing System (ACLS). Total production quantities of 12,000 to 14,000 units are expected to be procured by 1995.

Control Data Corporation was awarded a contract by the Naval Air Systems Command, in February 1986, to design and develop a VHSIC version of this computer. The VHSIC Processor Module (VPM) will provide a five fold improvement in performance, store one million words of local memory on the module, be interchangeable with previous processor modules (software transportable), and have an MTBF in excess of 10,000 hours.

The five VHSIC chips for this development are based on 1.0 micron technology fabricated by LSI Logic using 100k gate array technology. Chip fabrication was complete and a laboratory version of the VPM was demonstrated in July 1989. Deliveries of VPM modules to Navy laboratories and program prime contractors began in late 1989. The production deliveries are scheduled to begin in October 1990 to the F/A-18, EA-6B, F-14D, and ACLS programs.

5.2.3 Advanced ASW Receiver

The effectiveness of Anti-Submarine Warfare operations becomes increasingly limited as improved submarine technology reduces the target signal level, eliminating the range of detection and accuracy of localization that were achievable in the past. New sonobuoy rf links must provide greatly increased channel capacity, bandwidth flexibility, and anti-jam protection in order to maintain an effective ASW capability.

During FY-89, the Naval Air Systems Command selected the Advanced ASW Receiver Advanced Technology Demonstration (ATD) project to be funded as an FY-92 start. This ATD effort will demonstrate a receiver based upon digital technology, that offers the benefits of multi-channel reception of analog and digital information, an ability to tailor channel band width to sensor type, rf anti-jam capability, reduced power drain, and reduced size and weight. In order to provide these features, the receiver will use a high performance A/D converter and a polyphase digital filter which incorporates the latest VHSIC technology in order to take advantage of advanced digital processing techniques. The receiver architecture has been successfully demonstrated at Naval Air Development Center, using discrete components in a bench top breadboard configuration. The high performance A/D converter has been demonstrated at Hughes.

The ATD advanced receiver will include a signal pre-conditioning module, an A/D converter, a digital pre-processing filter, and a phase detector. The proposed demonstration will provide proof of concept and reduce the risk for the receiver development phase. At the completion of the ATD, all component technologies, including VHSIC Phase 2, will have been demonstrated, as well as the operational benefits of the advanced receiver. The receiver will then transition into a development program for an improved sonobuoy communication link which can be configured for all ASW platforms.

5.2.4 HF/EHF Communications: VHSIC Terminal Brassboard (VTB)

The VHSIC Terminal Brassboard (VTB) was part of a joint Navy/Air Force project to assess the ability of VHSIC technology to meet the requirements for new, complex processing of communications signals. The VTB was designed with a common architecture for processing the signal waveforms received from both the High Frequency Anti-Jam (HFAJ) system and the Milstar EHF satellite system. The VHSIC terminal design was projected to reduce the size, weight, and power by 75% from current terminal designs. Significant improvements in reliability, maintainability, and long term system costs are also expected. These benefits make it possible to receive EHF, HFAJ, and other sophisticated communications signals on submarine and manpack terminals where very limited space and power are available.

The VTB was developed by TRW for the Naval Space and Warfare Systems Command. The design and fabrication of the chips for the VTB were completed during 1987, making extensive use of TRW chips developed during Phase 1 and under the VCP insertion program discussed below. The chips include a flexible VHSIC signal processor, an FFT chip set, a convolutional decoder, and a configurable gate array.

Development, fabrication, and integration of the VTB has been completed. Extensive testing of the EHF portion of the system was conducted at the Milstar test bed located in San Diego at the Naval Ocean Systems Center (NOSC) during the first and second quarters of 1989. The testing was accomplished using a satellite simulator at NOSC. On-the-air testing with the FLTSAT EHF Package (FEP) satellite (a precursor to Milstar) is being considered. It is anticipated that the VTB test data and architecture concepts will be major factors in the design of emerging submarine and special forces radio systems.

5.2.5 VHSIC Communications Processor (VCP)

The objective of this NAVAIR program was to demonstrate the improved performance of a communications processor which uses VHSIC technology. The VCP consists of a core signal processor in SEM-C format and a preprocessor that provides matched filtering. The processor architecture was developed by TRW during VHSIC Phase 1 for an EW brassboard. Derivatives of the VCP are being used in the ICNIA program and the VTB program described above. Both of the modules use TRW VHSIC-1 chips.

In the VCP, the preprocessor will digitize baseband analog waveforms from an rf front end and pass them to the signal processor for digital demodulation and filtering. The VCP program successfully demonstrated the demodulation of GPS, Link 11, and AM voice signals in December 1988. Concurrent processing of multiple signals will be performed.

During 1988, two terminals using the VCP were assembled, and integration and testing was started. Acceptance test and delivery of the units was accomplished in early 1989.

5.2.6 AN/SRS-1 Combat Direction Finder

This program is the result of a Sanders Associates IRAD study which demonstrated the greatly improved processing throughput of a vector product calculator (VPC) using VHSIC components. The technology insertion effort was initiated by SPAWAR in November 1985, with the goal of production in 1988.

In February 1987, the initial phase was completed (thirteen months after the start of the contract) with the design, development, and demonstration of a brassboard model of the VPC. It showed that the selected Phase 1 VHSIC chips from IBM, TRW, TI, and Motorola can be integrated with conventional logic components to achieve the design goals. The VPC was also designed to be used as an FFT engine in addition to its initial role as a generic array processor.

The second phase of this program, begun in March 1987, was to use gate arrays for the non-VHSIC chips in the VPC in order to reduce the number of circuit cards from four to one. This was accomplished and the VPC was successfully tested in the fourth quarter of 1988.

The VPC is scheduled to be integrated into the AN/SRS-1 FSED and tested in 1992. Production will follow formal system level operational test and evaluation.

5.2.7 MK-50 Torpedo

The Torpedo MK-50 is being developed by Honeywell for the Naval Sea Systems Command as the next generation torpedo for use against the continually evolving Soviet submarine threat. It will be the primary ASW weapon for air and surface platforms as well as the principal submarine standoff weapon.

VHSIC insertion provides significant benefits to the MK-50 system: a saving of 5 inches in length and 40 pounds in weight, which could be allocated to a larger warhead; increased reliability by having 1,300 fewer components and 15,000 fewer solder joints; power reduction of 16 watts; and 540 square inches less in circuit board area. The overall result is a reduction in acquisition cost of approximately $10,000 per torpedo, as well as a reduction in life cycle costs because of better reliability and maintenance characteristics with the same or better performance parameters. By adding the increased capability of a single board AN/AYK-14 computer (which is a separate VHSIC insertion program described below) the size and weight of the electronics section of the torpedo would be reduced even more.

VHSIC Phase 1 chips from several different manufacturers are being used in the digital receiver and in the command and control subsections. These include the TRW micro-controller chip, the TRW address generator chip, the TI SRAM, and a number of Westinghouse and LSI Logic gate array personalizations.

Final development is underway on the AYK-14 memory board and signal processor board. Both will be inserted in the first full production contract (FY91). The digital receiver is an identified part of the MK50 P^3I development plan. It is currently scheduled for introduction in the fourth production contract.

5.3 Air Force System Insertion Projects

5.3.1 Generic VHSIC Spaceborne Computer (GVSC)

The Generic VHSIC Spaceborne Computer (GVSC) project of the Air Force Space Technology Center (STC) extended the 1750A computer architecture to a 32-bit data structure and to a radiation-hard, space environment. The GVSC program, completed in January 1990, has demonstrated a 3-5 million instruction per second (MIPS) computer throughput and delivered 25 chip sets to AFSTC. GVSC chip sets are being delivered to BSTS, Milstar, and other DoD spacecraft systems for engineering evaluation.

The GVSC operates as a 16-bit processor to satisfy MIL-STD-1750A, but GVSC chip sets from both contractors (Honeywell and IBM) execute double-word (32-bit) fetches from memory and support 32-bit data busses both externally internally. Both machines are capable of executing most double precision (32-bit) operations in a single machine cycle. These features are representative of migration from 16-bit to 32-bit capability found in the GVSC class of machines, while maintaining downward compatibility with previous generation hardware. See Reference 5.22.

5.3.2 Advanced Spacecraft Computer Module (ASCM)

The ASCM program includes the development and qualification of advanced packaging technologies, advanced integrated circuits, and generic components (such as radiation hardened gate arrays), which are critical to the development and production of future space data processing systems. BSTS and several other AF Space Systems Division (SSD) programs need a radiation hardened, space qualified, high throughput computer by 1991, and ASCM is the only program targeted to provide the building blocks they require for mission success.

ASCM was started as an SDI program. However, many Air Force systems have similar requirements. Specifically, the Space Based Radar program has identified the control processor module (CPM) and the advanced technology insertion module (ATIM) as critical to the success of their mission and has determined that in excess of $140 million will be saved using the CPM and ATIM technologies from ASCM. Milstar is expecting to use the CPM technology, and ASCM is being considered for GPS and DMSP block changes as well. Delivery of a space qualified CPM to the BSTS program is scheduled for 3Q91, a space qualified ATIM is scheduled for 4Q93, and a full ASCM demonstration is scheduled for 4Q93.

5.3.3 Cruise Missile Advanced Guidance (CMAG)

The CMAG program is an advanced guidance technology program under which laser radar based guidance technology for cruise missile applications is being developed and demonstrated by General Dynamics (GD). The objective of the CMAG VHSIC insertion project is to demonstrate the performance improvement that can be obtained by using VHSIC

submicron chip technology. Under this Wright Research and Development Center (WRDC) program, a previously developed CMAG processor system will be replaced by a new design utilizing a submicron array processing chip set.

The CMAG processor will be configured from a combination of modules developed previously under the ARDEC/GD CVIS program and new modules being developed under the CMAG VHSIC insertion effort. The new modules will utilize VHSIC submicron developed by Honeywell and IBM under their respective VHSIC Phase 2 contracts. The modules will use the same two chips used on the CVIS modules for interfacing to the PI bus (the IBM VBIU and a GD ASIC). They will use the Honeywell APU/APC chip set as the processing element for a laser radar image processor and a TM bus interface chip currently under development by Honeywell. The resultant system will therefore include modules with different TM bus interface logic.

The guidance processor being replaced consists of approximately 30 circuit cards averaging over 100 ICs per card. An equivalent performance VHSIC processor configuration would consist of approximately 10 circuit modules of 30-40 ICs per module. This reduction in circuitry will permit the guidance subsystem to be packaged in a smaller volume dissipating less power and costing less to build and maintain.

The CMAG VHSIC processor will be demonstrated in a laboratory environment performing an advanced guidance function that includes laser radar image processing algorithms as well as guidance and navigation algorithms. The demonstration is scheduled for late 1990.

5.3.4 AN/APG-68 Radar Advanced Programmable Signal Processor (APSP)

The AN/APG-68 is an airborne fire control radar on the F-16 aircraft, which is being developed by Westinghouse for the Air Force, to provide air-to-air target detection and tracking. APSP will greatly improve the operational characteristics of the radar such as tracking range, target discrimination, and multiple target tracking. The program began in 1985 as the VHSIC Programmable Signal Processor (VPSP), and the first phase was completed with a successful brassboard demonstration in June 1988. Full scale development started in September 1988, and completion is planned for 1991. The production phase is scheduled to start in 1991.

5.3.5 Milstar Terminal/Modem Processor

Milstar is an EHF satellite communication system. The use of VHSIC technology will provide improved performance with reduced weight, space, power, and life cycle cost. It will become possible to install the Milstar terminal on platforms with space and weight restrictions that otherwise preclude such installation.

The program started at TRW in 1984. The processor uses the preprocessor portions of the EHF on-board brassboard plus additional Phase 1 convolutional, fast Fourier transform,

and multiplier/accumulator chips designed and fabricated at TRW. For the related Navy effort on the VHSIC Terminal Brassboard (VTB), see Section 5.2.4 above.

5.3.6 F-15 VHSIC Central Computer (VCC)

The F-15 central computer controls pilot displays, weapon launch systems, and the aircraft g-load warning system. The VHSIC central computer will have improved memory/throughput capabilities and a greater mean time between failures. The operational software will be programmed in Ada in order to improve maintainability. An IBM VHSIC 1750A processor forms the basis for this program. IBM is a subcontractor of McDonnell Douglas in this effort for the Air Force.

The program began in September 1988. The first limited production unit is planned for 1990. The operational software is planned for early 1992.

5.3.7 Radiation Hard 32-Bit Processor (RH32)

The Radiation Hard 32-Bit Processor (RH32) program for spaceborne and airborne real-time, fault tolerant processing applications was begun by merging the Air Force program for a 32-bit Common Avionics Processor (CAP-32) with the Strategic Defense Initiative RH32 program in January 1988.

The expanded RH32 contract program began in August 1988. The major objective of this Rome Air Development Center (RADC) program is to define, develop, and demonstrate a high performance, radiation hardened, 32 bit processor with the capability to address 4 gigabytes of memory. It must be programmable, have the capability for efficient execution of Ada software, and provide a sustained processing throughput of at least 20 million instructions per second in a worst-case, post-radiation environment. The RH32 program relies on radiation hard, VHSIC technology to meet performance requirements and is expected to result in a processor that has three to five times the throughput of current radiation hard processors and a significantly larger available memory address space. The RH32 includes requirements for reliability, testability, and fault tolerance which are key to the successful insertion of the RH32 processor into real-time systems.

The first phase of the RH32 program, completed in November 1989, resulted in the development of preliminary microcircuit specifications, a detailed description of the processor (including form, fit and function specifications for the processor and memory modules and their interfaces), and an evaluation of the radiation-hardness of the different technologies and processes proposed for the development of the processor microcircuits.

The second phase is scheduled for twenty-two months (January 1990 - November 1991) with two contractors: TRW and Honeywell. The second phase of the effort is concentrating on the detailed design, layout, fabrication, assembly, test, and evaluation of the microcircuits forming the core of the processor. A separate contract effort, the Reduced Instruction Set Computer Ada Environment (RISCAE), will develop an Ada environment for each of the

target machines. An integrated Ada environment should be available for use by December 1991.

5.3.8 VHSIC Avionics Modular Processor (VAMP)

Westinghouse Electric Corporation has designed, fabricated, and delivered advanced development models of the VAMP to the Air Force WRDC. The chips were designed by Westinghouse and fabricated by National Semiconductor. The VAMP includes the 1750A processor function in addition to other processing functions. It provides improved reliability, maintainability, and logistics support. Other features include VHSIC interoperability (PI Bus and TM Bus) and JIAWG standards.

5.3.9 Short Range Attack Missile (SRAM) II Missile Guidance Computer

The SRAM II vehicle is a rocket powered missile designed for the Air Force Air Systems Division to deliver a nuclear warhead in an air-to-ground mode. The Missile Guidance Computer (MGC) for SRAM II consists of two MIL-STD-1750A processors with 128k of memory each. The use of VHSIC technology reduces the life cycle costs and the number of computer processing units needed for flight control and navigation. Boeing is the MGC prime contractor with Texas Instruments supplying the VHSIC chips. The first flight of a full scale engineering system is planned for the second quarter of 1992. First production delivery is planned for April 1993.

5.3.10 Advanced Tactical Fighter (ATF) Processing

The Air Force Air Systems Division is using VHSIC in processors for the Advanced Tactical Fighter (ATF) to meet its high throughput, low weight, and high reliability needs. The demonstration/validation (DEM/VAL) models use 1.25 micron chips. Submicron chips (with up to 150k gates per chip) are planned for full scale development (FSD). The prime contractors are Lockheed for the YF-22 and Northrup for the YF-23. Chip manufacturers include Texas Instruments, Westinghouse, Hughes, AT&T, and TRW. The DEM/VAL phase began in 1987, deliveries have been completed, and a prototype processor has been operational since March 1989. Contract award for full scale development is planned for July 1991.

5.3.11 Common Signal Processor (CSP)

IBM has developed a modular common signal processor (CSP) based on VHSIC technology. It can be configured and programmed to process signals in a wide variety of

applications, such as high performance radars, secure communications, electronic warfare, image processing, and anti-submarine warfare. This WRDC program demonstrates the feasibility of a common signal processor which makes use of VHSIC technology to increase system performance without increasing weight, space, and power. Issues such as functional partitioning, module definition, standardization levels, and signal processor software development were examined.

The ten 1.0 micron CMOS VHSIC chips that were developed under this effort during 1987 and 1988 were used to design six CSP module types. These modules, in turn, were used to build the CSP brassboards which were delivered in June 1988. The brassboards have been provided to Westinghouse for use on the Ultra-Reliable Radar Program. The Ultra-Reliable Radar program was terminated in August 1989. The CSP units were returned to the Government. One was transferred to E-Systems for use on a demonstration contract. The other was transferred to the Air Force for use on an in-house project.

5.3.12 E-3A Signal Processor

The E-3A Sentry aircraft is the Air Force Airborne Warning and Control System (AWACS). This insertion effort by the Air Force is aimed at improving the performance and logistics characteristics of the signal processor used in the surveillance radar on board the Sentry.

Westinghouse completed an initial system insertion study in 1983. The follow-on design phase was completed in 1985 and a contract award for the hardware phase was made in August 1986. A systolic vector processor based on the Westinghouse PLAU chip was demonstrated in 1988. Full scale development is in progress.

5.3.13 Advanced Onboard Signal Processor Radiation Hardened Vector Processor (RHVP)

The purpose of the Advanced Onboard Signal Processor (AOSP) program at RADC is to develop spaceborne distributed processors that can provide real-time signal processing capabilities required for future system applications. The specific emphasis under this VHSIC insertion effort has been focused on the development of a radiation-hard, vector processor (RHVP) based upon the Macro Function Signal Processor (MFSP) concept. The processor is intended to function as an application processor unit within an AOSP node, but could also serve as an independent signal processor. VHSIC technology is being utilized to improve hardware reliability, increase processing capabilities, and reduce size, weight, and power consumption (SWAP).

Dual award contracts were given to IBM and TRW in September 1986 for the development of RHVP hardware. The TRW contract called for a tailored processor design that could satisfy the Boost Surveillance and Tracking (BSTS) program in terms of its vector processing requirements. The resulting design entailed the use of three new VHSIC CMOS chip types and three existing VHSIC Phase 1 chips. Detailed design of the three new chip

types was completed, data sheets prepared, and all work preparatory to chip fabrication was completed. Because of fund limitations, fabrication of the new chips and the RHVP brassboard did not occur, and the effort was descoped to a study. The Final Design Review documentation, along with the chip data sheets, served as the final contractual documentation. A significant amount of the RHVP architectural design effort was subsequently applied to TRW's VHSIC Phase 2 Superchip technology program.

The general purpose of the RHVP program with IBM is to provide a flexible processor architecture designed to accommodate a wide range of fixed and floating point formats. Enhanced architecture developments, such as the incorporation of the Generic VHSIC Spaceborne Computer (GVSC) scalar processor and shared memory for the vector and scalar processors, have been achieved. This structure eliminates the data transfer time between the processors, allows the application programmer to choose the processor (vector or scalar) that yields maximum performance for specific algorithms, and supports concurrent and independent vector and scalar processing. The processor is programmable via Ada calls, and an Ada S/W development environment has been provided.

The RHVP brassboard implementations were completed in November and December 1989, and final documentation for the brassboard phase of the contract is under Government review. The brassboards are fully compliant to the MFSP Prime Item Development Specification. Throughputs are 4.5 MIPS (DAIS) for the GVSC and 150 million floating point operations per second (MFLOPS) peak for the vector processor. Brassboard power consumption is 268 watts (peak). The RHVP is on the critical path for Phase 1 Strategic Defense System (SDS) deployment. RHVP breadboard H/W and S/W tools have been demonstrated in Boost Surveillance and Tracking (BSTS) Ground Demonstrations. A recent modification to the contract (signed April 1990) extended it for another 26 months. The modification entails additional work to make the design fully qualified for space flight. The Vector Processor design goal is to use VHSIC chip technology throughout and to provide standardized interfaces. Provisions for interoperability with other scalar processors (e.g., RH-32, MIPS), improved fault tolerance, reliability, and SWAP will be addressed. VHDL chip descriptions, to enable chip second sourcing, will be delivered.

5.3.14 AN/ALQ-131 Electronic Countermeasure Pod

The AN/ALQ-131 is an airborne pod-mounted system capable of countering threat radars. A VHSIC Transmit Control Assembly (VTCA) is being developed for retrofit into this electronic warfare (EW) pod. The major goals are to improve the system MTBF by 25%, reduce the mean time to repair (MTTR) by 50%, provide up to 50% growth space for future capabilities by reducing the printed wiring assembly board count, provide a common VTCA for all rf bands, and provide an extensive maintenance and diagnostics system (MADS) capability for each VTCA.

Development of the VTCA by TRW began in September 1983 under a contract from the Air Logistics Center at Warner-Robins AFB, and prototype specifications were delivered

in March 1984. The first insertion of VHSIC into an operational system took place in December 1985 with a demonstration of the VTCA in the AN/ALQ-131.

Accomplishments for 1986 included the delivery, flight testing, and laboratory testing of the Block I prototype. Initial flight test of the pod occurred on July 17, 1986 on an A-10 aircraft at Eglin AFB.

5.4 Other System Insertion Projects (Name only)

The VHSIC insertion projects described above represent those that were formally planned and jointly funded by the VHSIC Program Office and the corresponding System Program Offices. In addition to these, a large number of independent insertion projects were undertaken, some of which were IRAD funded and others funded by a particular Service. The list below briefly identifies some of these by company, Service, and system.

- o AT&T
  - (AN/UYS-2) Enhanced Modular Signal Processor (Navy)

- o General Dynamics
  - M1A2 tank power and data bus controller (Army)
  - Avionics 1750A microprocessor (Air Force)

- o Honeywell
  - Radiation Hardened Static RAMs (Army, Navy, NASA)
  - EMSP (Navy)
  - Milstar (AF)

- o Hughes
  - ATF common integrated processor (Air Force)
  - APG-65,-70,-71 radars (Air Force, Navy)
  - B-2 radar and upgrade (Air Force)
  - Advanced special receiver ALR-67 upgrade (Navy)
  - LEAP (SDIO)
  - AMRAAM processor and range correlator (Air Force)
  - MTSP (Army)
  - LHX risk reduction program (Army)
  - D3 fire control system (Army)
  - UHF follow-on to LANDSAT (Navy)
  - AUSSAT (Australian communications satellite)
  - EHF satellite payload (Navy)

- o IBM
  - Portable Jammer (Navy)

- Prism
- SABIR (Air Force)
- ISTP (NASA)
- ASW receiver (Navy)

o Lockheed
- Boost Surveillance and Tracking System (BSTS) (AF)
- Milstar Satellite Payload (AF)

o Raytheon
- Advanced On-board Signal Processing (AF/DARPA)
- Advanced processor for air-to-air missiles (AF)
- Aegis standard missile (Navy)
- AIM-54C Phoenix missile (Navy)
- AMRAAM missile producibility enhancement (Navy/AF)
- AN/SLQ-32 electronic warfare system (Navy)
- CCS/MK-2 (Command and Control Software for BSY-1 Submarine (Navy)
- Ground Base Radar (Army)
- IR Maverick AGM-65D (AF)
- Milstar (AF)
- Milvax (AF)
- MK-XV IFF (AF)
- Patriot WCC Missile (Army)
- Sparrow Missile (Navy)
- Tartar Missile (Navy)

o Texas Instruments
- ATF-YF-22 mission display processor (AF)
- Target Acquisition Systems (Army)
- Space Station (NASA)
- LHX Helicopter (Army)
- TOW 2 Auto Tracker (Army/DARPA)
- VETRONICS (Army)
- Anti-Armor Weapon System-Medium (AAWS-M) (Army)
- Short Range Attack Missile-II (SRAM-II) (AF)

o TRW
- Radiation hard 32 bit computer (AF)
- ICNIA (AF)
- INEWS (AF)
- Battle management processor (Army)
- Cryogenic CMOS for focal plane array (Navy)
- Mass memory subsystem (AF)

- Advanced spacecraft computer module (AF)
- Advanced communications satellite processor (Navy)
- Standard EHF package (SEP) (AF)
- ATF digital avionics (AF)

o Uniys
- V1750 processor for various programs (IRAD)
- Radiation hard 32-bit processor (AF/SDIO)

o Westinghouse
- Combined FLIR and Multifunction radar processor (Navy)
- Longbow signal processor (Army)
- ATF signal processor (AF)
- ARSR-4 (Air route surveillance radar) (FAA/AF)

5.5 Logistics Retrofit Engineering

Numerous Air Force electronic systems contain older devices which are rapidly becoming unavailable. The result is that a generation of front line weapon systems may soon become very difficult and expensive to maintain in operation. Many of the older components are also relatively unreliable which makes the system "go down" frequently, thus compounding poor system maintenance with poor operational availability.

For both of these reasons the Air Logistics Center at Sacramento (SM-ALC) has undertaken a number of VHSIC insertion projects with support from the VHSIC Program Office. The approach taken by the SM-ALC has been to use in-house facilities to customize commercially produced VHSIC gate arrays which can then perform the function needed to replace specific chips. If necessary, the customized gate array can be packaged to provide a "form, fit, and function" replacement for an obsolete or unreliable part.

Digital Signal Transfer Unit (DSTU)

The DSTU VHSIC board project was originated to replace an obsolete chip for the AJN-16 Inertial Navigation and APQ-130 radar on the F-111D aircraft. The VHSIC DSTU board is a form, fit, and function replacement which reduced the board cost from $24,000 to $2,000. The use of VHSIC reduced the total components used from 224 to 60. The board was flown on two operational F-111Ds at Cannon AFB in 1987.

Cheyenne Mountain Complex (CMC) Communication Multiplexer

The CMC Communication Multiplexer (Com Mux) provides an interface between internal and external CMC communication circuits and communication system computers. It is part of the CMC Communication and Integrated Display System and consists of two separate sets of four equipment cabinets.

The current system is unreliable and requires a great deal of support to repair. The VHSIC system will increase the MTBF from 60 hours to an estimated 5000 hours, decrease the repair time from two weeks to 10 minutes, and reduce the spares count by an estimated 90%. A design for the replacement Communication Multiplexer has been completed with final design review schedules for September 1990.

FPS-117 Seek Igloo Signal Processor Unit (SPU)

The FPS-117 is an air surveillance radar that provides real time tricoordinate radar target data and beacon replies within the surveillance volume. Currently, the system has a MTBF of 700 hours with a power consumption of 17 kW. The project will develop a VHSIC-like based modular system architecture incorporating a 32-bit microprocessor with extensive BIT/FIT and integrated diagnostics.

With the VHSIC insertion, the MTBF will be increased to an estimated 5000 hours and power consumption will be reduced to 1 kW. A design of the signal and data processor has been completed with final design review scheduled for December 1990.

F-111 Weapons Navigation Computer

The F-111 Weapons Navigation Computer (WNC) was experiencing flight safety hazards that grounded the aircraft. The hazard was identified as interference between the airborne radio and the computer memory clock. A new prototype WNC board using VHSIC technology has been designed to eliminate the interference and, at the same time, to upgrade the computer performance. The prototype is scheduled to complete flight test in December 1990.

5.6 Projects Involving VHDL Insertion

5.6.1 VHSIC Modular Adaptive Signal Sorter (VMASS) (Army)

The details of this contract are described in Section 5.1.1 above.

5.6.2 AN/UYS-2 Standard Signal Processor (Navy)

The details of this program are described in Section 5.2.1 above.

5.6.3 AN/BSY-2 Submarine Program (Navy)

The AN/BSY-2 submarine procurement office (NAVSEA PMS-418) has placed a requirement that VHDL descriptions be provided with its ASIC chip deliverables. General Electric (Syracuse) is developing the ASICs. Currently there are 49 unique designs. GE plans to convert the design descriptions from the Verilog design language to VHDL, using a software product called VDOC.

5.6.4 Joint Tactical Information Distribution System (JTIDS) - 2M Terminal (Army)

The VHDL and the VHSIC design methodology, developed as part of the VHSIC program, provide a well defined, top-down, modular approach to system design. They allow a project team to design, analyze, test, and integrate weapon system designs and architectures through simulation without costly circuit fabrication and re-design efforts. Then, at the end of the design process, all the system specifications and design data can be documented and archived for future reference. System level designs are accomplished using commercial tools, such as Teledyne Brown Engineering's "Technology for the Automatic Generation of Systems" (TAGS) and the "Architecture Design and Assessment System" (ADAS) developed under VHSIC by Research Triangle Institute.

In January 1989, the Army LABCOM's Design, Modeling, Simulation, and Assessment Center began benchmarking its system level simulation and modeling techniques on the Joint Tactical Information Distribution System (JTIDS) - 2M terminal.

The Joint Tactical Information Distribution System (JTIDS) is a joint Air Force/Army program to provide battlefield information distribution for the Services. JTIDS is being functionally described and simulated using the design tools. The design tools, along with VHDL, will be used to document and simulate the JTIDS architecture and provide insight into the "high pay off" technology insertion areas. A plan for VHSIC insertion into JTIDS was completed during 1Q FY90.

5.6.5 Advanced Tactical Fighter (ATF) (Air Force)

The VHSIC Hardware Description Language (VHDL) is currently being applied to avionics developed for the Advanced Tactical Fighter (ATF). The VHDL models to be acquired for ATF demonstrations will be utilized for various purposes, ranging from bus specification compliance, to assessment of diagnostic capabilities present in designs, to form, fit, function, and interface specification. Demonstrations of key aspects of these methodologies

are underway and specific implementations for receipt of information in these formats will be determined and used as a part of the ATF full scale development effort. See Section 5.3.10.

5.6.6 JIAWG (tri-Service)

A Joint Integrated Avionics Working Group (JIAWG) initiative is in the planning stages to demonstrate the application of VHDL for common avionics modules. Starting with an existing VHDL behavioral specification of the PI-Bus, several contractors will design gate level implementations, develop test vectors, and exchange the design and test information to verify that the designs do in fact meet the behavioral specifications. The contractors involved in the Army Light Helicopter (LH) program, Boeing-Sikorsky ("First Team") and McAir-Bell ("Super Team"), together with those involved in the Air Force Advanced Tactical Fighter (ATF) program, Lockheed (YF-22) and Northrop (YF-23), will be tasked with this effort. McAir is also involved in the Navy Advanced Tactical Aircraft (ATA) program.

5.6.7 Generic VHSIC Spaceborne Computer (GVSC) (Air Force)

The Generic VHSIC Spaceborne Computer (GVSC) program acquired VHDL descriptions for many of the GVSC microcircuits developed by the GVSC contractors --- Honeywell and IBM. These VHDL models ranged from Instruction Set Architecture (ISA) models for the chip sets to macrocell level models of the individual GVSC microcircuits. These models are currently under analysis at the Rome Air Development Center (RADC) to assess the level of modeling that will be of most benefit to the Advanced Spaceborne Computer Module (ASCM) Program. This VHDL development effort has provided the Government, as well as the contractors, with a great deal of experience in the development and acquisition of VHDL models for complex microcircuits. See Section 5.3.1 for more information on the GVSC.

5.6.8 Advanced Spaceborne Computer Module (ASCM) (Air Force)

The Advanced Spaceborne Computer Module (ASCM) program has defined several VHDL efforts for the ASCM contractors, Honeywell and IBM. Under this aggressive program the contractors will provide VHDL descriptions for the microcircuits and subassemblies developed during the effort. In addition, there will be an exchange of VHDL models between the two contractors and a fabrication of microcircuits from the exchanged VHDL descriptions. This VHDL description exchange will show the feasibility and workability of using VHDL descriptions as a second source mechanism for microcircuits targeted for space applications. See Section 5.3.2 for more information on the ASCM.

5.6.9 Radiation Hardened Vector Processor (RHVP) (Air Force)

The Radiation Hardened Vector Processor (RHVP) program is developing VHDL descriptions for the RHVP chip set in order to ensure second sourcing capabilities in the future. The RHVP contractor, IBM, will deliver VHDL structural descriptions of the RHVP microcircuits, at a sufficient level of modeling, to permit second sourcing. The level of modeling will be assessed by RADC prior to acceptance to ensure the most functional and cost effective VHDL models are procured to meet the second sourcing requirement. See Section 5.3.13 for more information on the RHVP program.

5.6.10 Single Channel Ground and Airborne Radio System (SINCGARS) (Army)

In an effort to expand the VHSIC program beyond the digital world, the Army ETDL has contracted with General Dynamics to extend the VHSIC design methodology so that it can be applicable to a system that contains both analog and digital processing. It will take a system from the requirements phase to the implementation phase using all available design automation resources and identifying all deficiencies. This methodology will then be applied to the development and capture of the second source Single Channel Ground and Airborne Radio System (SINCGARS).

The methodology begins with the requirements analysis phase. ADAS will provide the digital architecture while an analog software design tool will provide the analog architecture. ADAS will also provide an evaluation of the software/hardware partitioning. Once this is complete VHDL will be used to model the hardware at many levels of abstraction. The system can then be integrated as the individual partitions are developed and tested. The system will then be ready for delivery to the end user with meaningful documentation for future needs.

5.6.11 TD-660 Communications Multiplexer (Army)

The TD-660, a 12-channel, voice-to-digital multiplexer supported by the Army CECOM, had become a logistics problem due to parts obsolescence. Low MTBF, hard to get parts, tedious adjustments, and a large inventory made the TD-660 an attractive candidate for backfit technology insertion.

The old boards consisted of discrete transistors and hard to procure small scale and medium scale DTL logic integrated circuits. Field constraints limited the re-engineering to replacing the board set while preserving the backplane wiring. The contractor, AT&T, was assisted by Intermetrics, Inc. in capturing the re-engineered design in VHDL. Effective use of modern design tools reduced the re-engineering costs while the use of VHDL provided a hierarchical design capture that made the new design transparent to future technology.

The new design was implemented in VLSI ASICs resulting in reduced power consumption from 55 W to 37 W and a weight reduction from 7.7 lbs to 5.0 lbs.. It is

estimated that the projected increase in MTBF from 1190 hours to 9014 hours will result in a 10 year cost saving of $21 M in failed boards. Details will be found in Reference 5 23.

5.6.12 Silicon Services Using VHDL Chip Descriptions (Army)

This effort is designed to demonstrate the ability of VHDL to provide non-VHSIC DoD contractors access to VHSIC silicon services. IBM, in an extension to its Phase 2 contract, has established a library of VHDL macros that it will use to transfer designs from non-VHSIC DoD subcontractors to IBM. The transfer will be done using VHDL. The subcontractor will describe the high level architecture and macro integration in VHDL and will perform simulations to verify the design. A VHDL netlist will then be used to transfer the design to IBM for chip fabrication. Both parties will use commercially available products.

To conclude this chapter on the insertion of VHSIC into various systems, the following paper provides a case history of insertions which have been particularly successful in reaching operational applications at an early stage in the development of the technology.

The Impact of VHSIC on Weapon Systems: A Case Study

J.C. Stuelpnagel
Westinghouse Electric Corporation

The application of VHSIC technology to DoD weapon systems has been given high priority throughout the VHSIC program. Westinghouse has taken an aggressive role in this effort and, as a result, a number of weapon systems are now currently in Full Scale Development (FSD) using VHSIC very effectively to meet their operational needs. These successful applications are based on a hierarchical approach to system design with separately defined requirements at the device, module, integrated rack, and system levels. The technologies developed to support the applications include operating software, CAD tools, advanced fabrication technology, manufacturing technology, and component qualification.

The 1986 VHSIC Annual Report included Figure 5.1 to illustrate the dramatic impact that VHSIC electronics could have on airborne radar.

Since that time the Programmable Signal Processor (PSP) has gone through a design iteration and is now the Advanced Programmable Signal Processor (APSP). The APSP is currently in FSD for use in the F–16 (under an Air Force program), the AH–64 Apache (under an Army program), and other platforms. It is well on the way to becoming a set of common modules for use in all three Services.

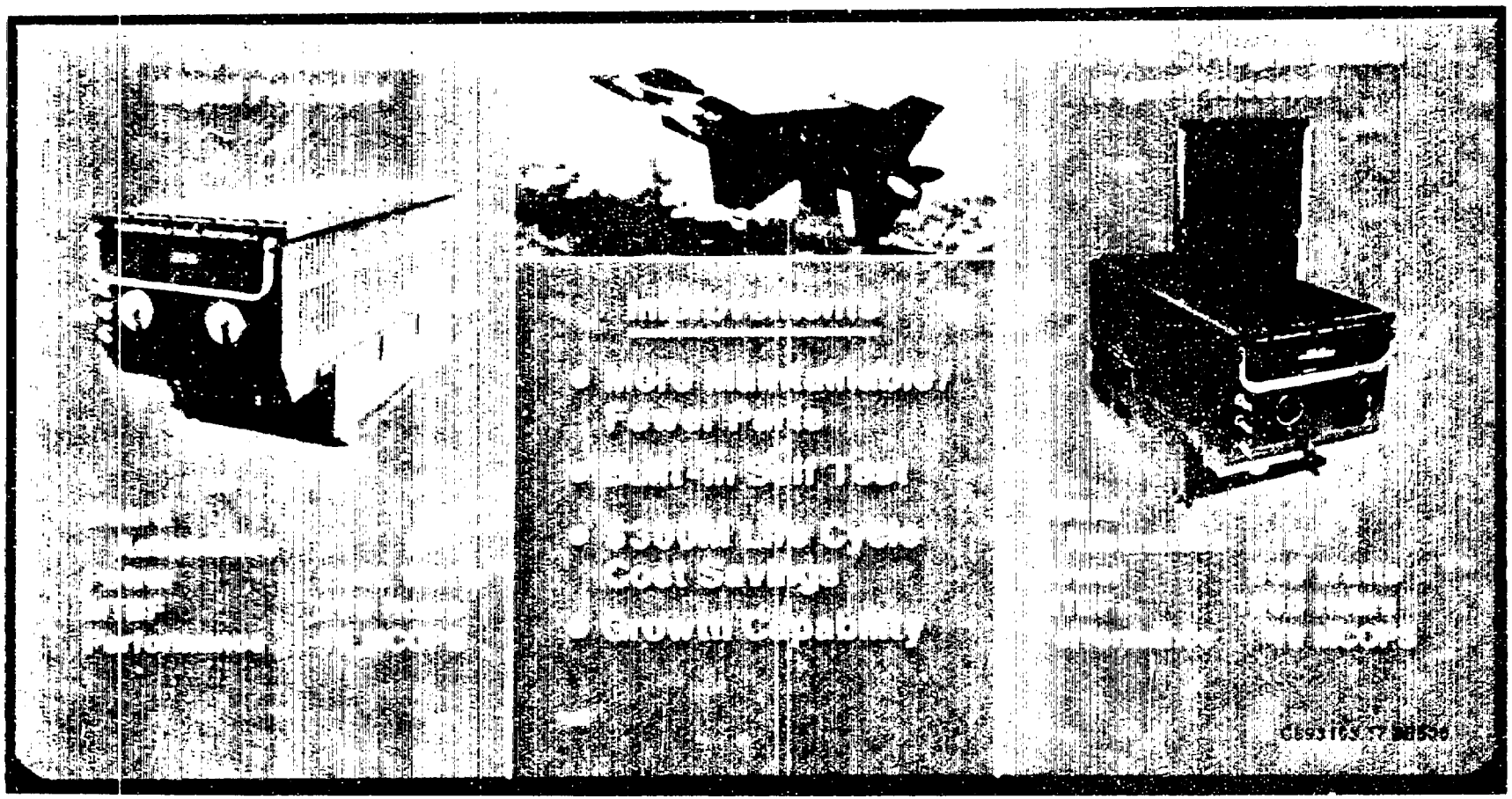


Figure 5.1 VHSIC Programmable Signal Processor Improvement (PSP)

The APSP modular architecture designed for the F–16 is shown in Figure 5.2. The Array Processor which performs the high speed signal processing, consists of the Array Processor Controller, the Processor Bulk Memory, and two Signal Processing Modules with the performance as shown in the figure. They interface with a dual–CPU radar computer implemented in VHSIC technology.

The same APSP can be used to provide target tracking functions for (electrooptical) FLIR systems and for a variety of signal processing functions in multi–function radars. For radar applications Westinghouse adapted the APSP architecture to different radar mode requirements by using two identical array processors with a larger bulk memory. The fundamental building blocks, however, are still the same as in the Array Processor for the APSP and are still implemented with VHSIC chips.

In the Longbow missile system for the Apache AH–64 helicopter, the same dual VHSIC array processor has been applied to a millimeter wave radar to perform target cueing for the Hellfire missile. Because of the different requirements, a multi–processor system of four CPUs is used, with a common data and control bus between the Signal Processor and the Data Processor. This system is very similar to the JIAWG or Pave–Pillar architecture now being used in emerging platforms.

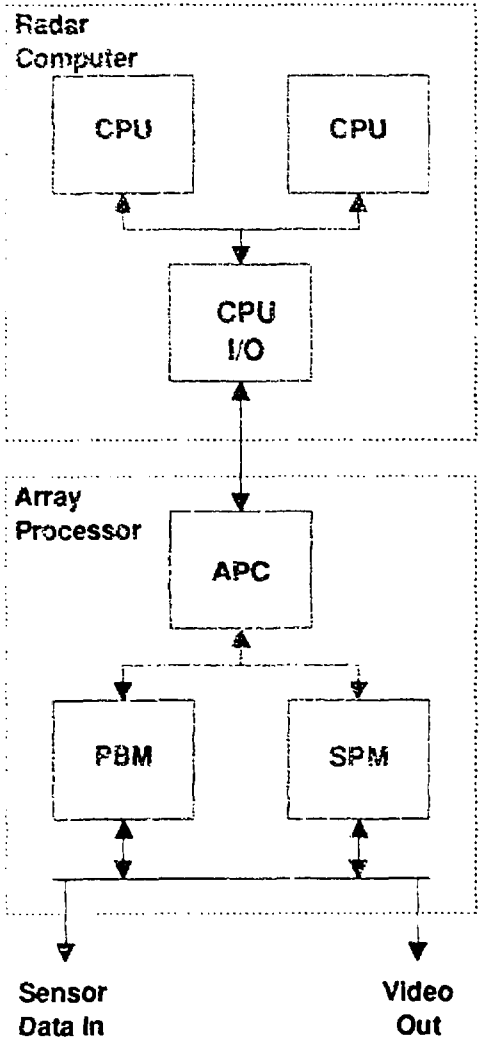
In summary, through the use of VHSIC technology, the PSP, thousands of which have been produced for the F–16 and B–1, has evolved into the APSP which is currently in Full Scale Development for the F–16, the AH–64, and other platforms.

Westinghouse is now in the process of using more of the VHSIC technology (the PI–Bus interface standard and submicron chips) plus the JIAWG standards (Joint Integrated Avionics Working Group) and SEM–E form factor to derive future standard signal processing module which can be used to upgrade the ATF and the LHX systems during a Pre–Planned Product Improvement. This signal processing module will perform one billion operations per second in the dual SEM–E configuration (using Ada as the programming language). This will truly be the common VHSIC signal processing module of the future.

In the area of airborne surveillance using the E–3 radar, shown in Figure 5.3, VHSIC technology will again provide dramatic improvements in detection range, processing speed, weight, power, size, and reliability, all of which are significant factors in operating the AWACS system. This program is currently in FSD for the Air Force.

Where the major requirement is that of low cost, high throughput, front end processing, at rates up to 800 hundred million operations per second/per module, Westinghouse developed a systolic array architecture using a chip called the Real Pipe Line Arithmetic Unit, or RPLAU. This module is used in the Air Route Surveillance Radar Four (ARSR–4) for target and weather processing. The system is currently in FSD for joint use by the FAA and the Air Force. One of the key requirements for this system is unattended operation. This requires application of the fault tolerance design concepts developed in VHSIC. Westinghouse is using 500 VHSIC chips in each of these systems ––– a major application of VHSIC technology.

F-16 APSP Modular Architecture



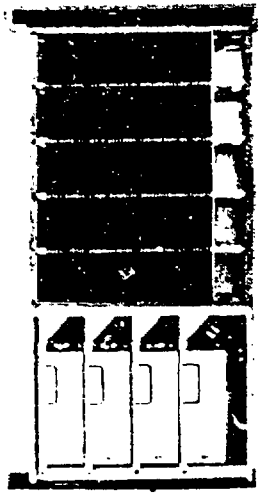
- 512 MOPS
- > 90% VHSIC Technology
- BIT/FIT to Device Level

Figure 5.2 VHSIC Advanced PSP Architecture

Impact of Electronics on Warfare

Airborne Surveillance

Present E-3 Processor



Performance	35 MCOPS
Power	3.4 kW
Boards	220
MTTR	22 min

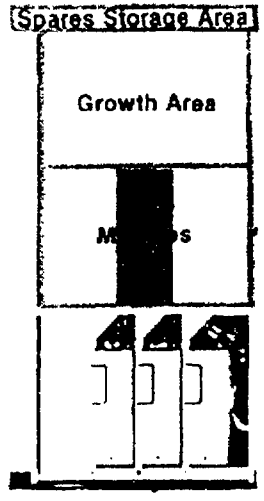
Improvements

Mission Adaptability
- Programmable

Fewer Parts
- Higher Reliability

Facilitates
- Longer Range Detection
- Detect Smaller Targets

VHSIC E-3 Processor



Performance	80 MCOPS
Power	1.1 kW
Board Pairs	7
MTTR	10 min

VHSIC

Figure 5.3 VHSIC Airborne Surveillance Radar Processor

Westinghouse is also using the same VHSIC technology on classified programs. One, in particular, has a requirement for hundreds of array processors performing over a hundred billion operations per second and requiring more than two hundred million bytes of memory.

In summary, the application of VHSIC technology has provided important benefits to DoD systems. Specific benefits for specific systems such as (1) low weight in AH—4 helicopter applications, (2) fault tolerance for ARSR—4 remote/unattended operation, and (3) improved performance within the same volume and power constraints for the AWACS, have all been attained. In the F—16, software compatibility with existing operational flight programs was an absolute requirement. In other environments, the ability to do multi—sensor processing with the same signal processing module significantly eases logistic support. Lower cost and higher reliability have been achieved in all cases.

CHAPTER 6 - TECHNOLOGY TRANSFER

CHAPTER 6

TECHNOLOGY TRANSFER

The VHSIC Program Office recognized, from the outset, that the transfer of VHSIC technology and products to both the DOD contractor community and DOD acquisition managers was essential for program success. It also recognized that historically this had been a difficult task to achieve. Novel approaches were needed to ensure that system designers would not only have access to VHSIC technology but also to VHSIC software and devices as quickly as they became available.

Technology transfer has been effected through information dissemination, military weapon system technology insertion projects, VHSIC program sponsored training courses, conferences and workshops, and transfer of some VHSIC developed state-of-the-art design tools, testability concepts, and other critical technologies to industry, universities, and non-military Government agencies. Some commercialization of VHSIC technology has also occurred.

A major source of information for the defense community is and will continue to be the Defense Technical Information Center (DTIC). DTIC has on file well over 1000 documents relative to VHSIC and VHSIC related technology. DTIC is accessible to qualified users, including U.S. Government agencies, their contractors, subcontractors, and potential contractors who have established a "need to know" at DTIC.

A special issue ot the "APL Technical Review", published by the Johns Hopkins University Applied Physics Laboratory, is devoted to VHSIC. It provides a series of invited articles covering the areas of VHSIC technology and chip sets, design methodology, technology insertion, system considerations, VHSIC tools, and system life-cycle supportability. See Reference 6.1.

The various aspects of VHSIC technology transfer are discussed in the following sections of this chapter.

6.1 Training

The VHSIC training program began in January 1984 in order to provide:

- o system managers and senior engineers with an awareness of the VHSIC products and design technologies being developed, and
- o working level engineers with instruction in the design of systems using VHSIC products through hands-on design workshops.

The primary techniques for accomplishing these objectives have been regional workshops, conferences, presentations, and brochures. For the hands-on workshops, special software has been developed for using VHSIC design tools, and detailed technical reference

material has been prepared in the form of application notes, performance data sheets, and text books.

VHSIC Application Workshops were organized and held throughout the country on a regional basis. The workshops provided comprehensive training and education in VHSIC technology for defense contractor personnel for the purpose of accelerating the application of VHSIC technology in military electronics. More than 3000 engineers and technical managers have attended them. Over thirty such workshops were held from 1984 through 1986.

The scope and depth of coverage of VHSIC technology at these workshops have enabled each attendee to evaluate the feasibility of using VHSIC technology in specific military system applications. Attendees were given the opportunity to present both application and work-related problems which were discussed by the group in terms of how VHSIC can be applied. The attendees were provided with approximately three days of instruction using text material which they took with them for future use in electronic design and for interface with the VHSIC community.

The instructional material (available from DTIC) included:

- Student Guide - a compilation of VHSIC design data and chip architectures. DTIC No. AD-B088-098

- VHSIC Specification Guide - an abbreviated version of all of the VHSIC chip specifications. DTIC No. AD-B088-097

- Interface Reference Guide - a collection of technical and management information about ICs, Computer Aided Design (CAD) availability, documents available, as well as key Government and industry personnel. DTIC No. AD-B088-099

A number of similar workshops have been held for DOD and other Government personnel at such in-house facilities as the Naval Ocean Systems Center (San Diego), the Naval Weapons Center (China Lake), Eglin Air Force Base (Florida), and the NASA Johnson Spaceflight Center (Houston).

A major follow-on effort to the Applications Workshops was developed by the Johns Hopkins University Applied Physics Laboratory and was initiated in June 1985. Called "Applications II", it was intended for those system designers who had attended the regional workshops. It built on their knowledge from earlier workshops and concentrated exclusively on how to design electronic subsystems using VHSIC products. This two day training program allowed hands-on use of some of the CAD tools developed for the VHSIC Program. Four Applications II workshops were held during the summer of 1985. Further extensions of these workshops were Applications III held by JHU/APL in October 1986, The Advanced Hands-On Applications Workshop IV (or VHSIC Tech-Fair) held in July 1987, and VHSIC Tech-Fair II, co-sponsored by the DoD VHSIC Program Office, the Defense Systems Management College, and JHU/APL in June 1988.

Other training workshops, seminars, and courses held have included the following:

- o IDAS Workshop, sponsored by the DoD VHSIC Program Office, held at University of Cincinnati, Cincinnati, OH, August 19-21, 1987
- o VHDL Users Group Workshop, sponsored by the DoD VHSIC Program Office, held at Virginia Polytechnic University, Blacksburg, VA, October 20-22, 1987
- o Seminar on VHSIC Technology and Applications Design, sponsored by Palisades Institute for Research Services, November 3-5, 1987
- o VHDL Tutorial, sponsored by the IEEE, ICCAD, Santa Clara, CA, November 9, 1987

The following training courses and materials were available as of September 1990:

- o VHDL training courses, offered by CAD Language Systems, Inc. Call (301) 963-5200.
- o VHDL training courses, offered by Intermetrics. Call (617) 661-1840.
- o ADAS Training Course, offered approximately six times a year by Cadre Technologies. Call (401) 351-5950

6.2 Conferences and Workshops

6.2.1 VHSIC Annual Conferences

From 1982-1987, the VHSIC Program Office sponsored annual three-day conferences covering all major aspects of the VHSIC program. A final one-day VHSIC Conference was held in November 1989. Proceedings of these conferences (with identifying DTIC numbers) are listed as References 6.2 through 6.8.

6.2.2 Topical Conferences and Workshops

In addition to the comprehensive VHSIC Annual Conferences, topical meetings and workshops were held covering the following specific VHSIC areas.

(a) Packaging
(b) Qualification, Reliability, and Logistics

(c) VHSIC Hardware Description Language (VHDL)
(d) Tester Independent Support Software Systems (TISSS)
(e) Engineering Information System (EIS)
(f) VHSIC Applications

(a) Packaging

- 1985 VHSIC Packaging Workshop, Naval Surface Weapons Center, Silver Spring, Maryland, June 5-6, 1985. Proceedings available from Palisades Institute for Research Services.

- 1986 VHSIC Packaging Workshop, Plymouth, Minnesota, September 15-17, 1986. Information available from Owen Layden, Army LABCOM, 201-544-2378.

- 1987 VHSIC Packaging Conference, April 21-22, 1987

- 1988 VHSIC Packaging Conference

- Tri Service Packaging/Interconnections Conference, Ft. Monmouth, NJ, May 1989

(b) Qualification, Reliability, and Logistics

- 1985 VHSIC/VLSI Qualifications Workshop, Vail, Colorado, September 18-20, 1985. Proceedings available from Palisades Institute for Research Services.

- 1986 VHSIC/VLSI Qualifications Workshop, Vail, Colorado, September 9-12, 1986. Proceedings available from DTIC: Nos. AD-B110-746,-747, -748, and -749.

- 1987 VHSIC Qualification, Reliability, and Logistics Workshop, sponsored by the DoD VHSIC Qualification Committee, Colorado Springs. August 25-27, 1987

- 1988 VHSIC/VLSI Qualification, Reliability, and Logistics Workshop, sponsored by the DoD VHSIC Qualification Committee, Scottsdale, Arizona, September 27-29, 1988. Proceedings available from Analytics, Inc.

- Advanced Microelectronics Technology, Qualification, Reliability and Logistics Workshop, Alberquerque, NM, August 29-31, 1989.

(c) VHSIC Hardware description Language (VHDL)

The following meetings were sponsored by the VHDL Users' Group. This group, established in April 1988, organizes and sponsors meetings on VHDL, publishes a regular newsletter, and maintains an electronic bulletin board system for information exchange.

- o VHDL Users' Group Meeting, at the Design Automation Conference, Anaheim, CA, June 26, 1988
- o VHDL Users' Group Meeting, Redondo Beach, CA, October 23-26, 1988
- o VHDL and Modeling in the DoD Procurement Process, Washington, D.C., June 21-23, 1989
- o VHDL and the Design Environment, Redondo Beach, CA, October 22-25, 1989
- o VHDL: The Emerging Design Standard, Boston, MA, April 4-6, 1990
- o VHDL Users' Group Third Annual Fall Meeting, San Jose, CA, October 1990

The following meetings on VHDL were sponsored or co-sponsored by the IEEE and other organizations.

- o VHDL Users' Workshop, Charlottesville, VA, IEEE sponsored, April 18-20, 1988
- o VHDL Developers Forum, Charlottesville, VA, September 14-16, 1989
- o VHDL Forum for CAD, Munich, West Germany, IFIP sponsored --- kickoff of European VHDL Users' Group, November 23-24, 1989
- o VHDL: The Standard Language in the CAE Environment, Jerusalem and Ramat Gan, Israel, Israel Society for CAD/CAM and Israel Ministry of Defense sponsored, December 14, 17, 1989
- o First European Working Conference on VHDL Methods, Marseilles, France, IMT, IEEE and AFCET sponsored, Sep 4-7, 1990

In addition, every major IC design conference in the industry has had one or more special sessions on VHDL over the past few years. Of note are the sessions in manufacturing and other technology conferences where VHDL's impact on the engineering design process is being reported.

(d) Tester Independent Support Software System (TISSS)

- o Industry Review, Melbourne, FL, September 1987
- o Industry Review, Phoenix, AZ, January 1988
- o Industry Review, Orlando, FL, May 24-25, 1988
- o Hands-on-Training, RADC, Rome, NY, June 1988

(e) Engineering Information System (EIS)

- o IEEE Design Automation Conference, Apache Junction, AZ, January 1, 1988
- o COMPCON, San Francisco, CA, February, 29, 1988
- o CAD Frameworkshop Standards Workshop, May 26, 1988
- o EIS Workshop, Baltimore, MD, November 14-18, 1988
- o COMPCON, March 1, 1989

(f) VHSIC Applications

- o Navy VHSIC Users Symposium, Johns Hopkins University Applied Physics Laboratory, Laurel, Maryland, April 26-27, 1983. Report JHU/APL/SR-83-2, Contract N00024-83-C-5301. Proceedings available from DTIC: No. AD-C032-934.

- o VHSIC Signal Processing Seminar, Naval Postgraduate School, Monterey, CA, June 17-18, 1986

- o Proceedings of the VHSIC Advanced Applications Workshop III, Johns Hopkins University Applied Physics Laboratory, Laurel, Maryland, October 29-30, 1986

- o VHSIC TECH-FAIR (Advanced Hands-On Applications Workshop IV), cosponsored by the DoD VHSIC Program Office and the Johns Hopkins University Applied Physics Laboratory, Laurel, Maryland, June 30-July 2, 1987. Information available from JHU/APL

- o VHSIC TECH-FAIR II, cosponsored by the DoD VHSIC Program Office, the Defense Systems Management College, and the Johns Hopkins Applied Physics Laboratory, Laurel, Maryland, June 28-30, 1988. Information available from JHU/APL.

- o Government Microcircuit Applications Conferences (GOMAC) 1978-1989. Includes papers on VHSIC applications in general sessions, topical sessions, and special sessions for VHSIC applications. Digests of Papers are available from DTIC as follows:

Year	Volume	DTIC No.
1978	VII	AD-B042-186
1980	VIII	AD-B070-117
1982	IX	AD-B070-118
1984	X	AD-B113-271
1985	XI	AD-B100-607
1986	XII	AD-B107-186
1987	XIII	AD-B119-187
1988	XIV	AD-B129-239
1989	XV	AD-B138-550

6.3 Technology Transfer of Design Tools

Modern sophisticated military electronic systems are becoming more and more complex. Consequently, there is a need to assist designers in making critical decisions early in the design cycle, reducing design time, and managing the overall design. It is evident that design tools play a major role in developing complex systems. With the help of advanced design tools, designers can accelerate the design process, make intelligent trade-offs between various types of hardware and software, assess performance, reliability, and testability and greatly limit the number of prototype items required for validating the system concepts. This reduces the cost and time required for initial system development and fielding, product improvements, and later upgrades to the system.

Many design tools developed during the VHSIC program were transferred to the general IC design community. The most significant of these was the transfer of the VHSIC Hardware Description Language into ANSI/IEEE standard 1076, which is fully discussed in Section 3.1.3. VHDL has become well established in both commercial and military circles. Significant work with VHDL has taken place in over 50 universities. It has come into use in all major CAD companies in the U.S. and in most of the major industrial countries in Europe and Asia as well as Canada, Australia, and Israel. The VHDL is now being marketed and sold commercially by Intermetrics and Valid Logic.

The VHDL software was initially transferred by the VHSIC program directly to all areas of industry, Government, and academia. By the end of the VHSIC program, the Army, Navy, and Air Force had shipped copies of VHDL and other design tool software, manuals, and information brochures to more than 100 companies, universities, and Government organizations. Some of the VHSIC software shipped, for example, by the Army included:

LCMTI	MPP/1750A Toolset
VHDL Workbench	PI- Bus
VHDL Synthesis	ADAS
MCXO VHDL	

In addition to the direct insertion of the VHDL software, the joint program with the Canadian Government, described in Section 3.1.3, aided the technology transfer process by developing industrial design practices around VHDL. It also developed additional design tools and adapted the software for operation on additional high performance workstations.

Another design technology transfer has been the Tester Independent Support Software System (TISSS) described in Section 3.2.2. TISSS began as a VHSIC program with continued funding by the Advanced Tactical Fighter Program in the Air Force. During the development of TISSS, a procedure was evolved for describing test vectors and test waveforms. The specification for this procedure is being considered as IEEE Standard 1029.1 - Waveform and Vector Exchange Specification. Several DoD programs are already using preliminary versions of this specification. The TISSS software itself is being transitioned by the Air Force directly to Air Force Logistics Centers as well as the Defense Electronic Supply Center.

Other VHSIC developed tools that have been transitioned as commercial products are the Architecture Design and Assessment System now marketed by CADRE, and the JRS Research Integrated Design Automation System.

The JRS Research tool set which synthesizes a processor architecture from the Ada or "C" application program, generates the VHDL model of the processor, and uses the model to automatically generate the compiler for the architecture is a unique capability not available from other sources and funded almost completely by the VHSIC program. This tool is now in use on several DoD programs and one commercial company.

The Engineering Information System funded by the VHSIC program has transitioned many concepts to industry through close association with the CAD Framework Initiative. The EIS prototype is being transitioned directly to the Sacramento Air Logistics Center as an Engineering Data Management System for the Air Force Advanced Tactical Fighter program.

6.4 Testability and Built-In-Self-Test

The increasing emphasis on built-in-test and built-in-self-test in the IC design community stemmed from the early VHSIC efforts with industrial and university contractors to develop efficient and economical methods of testing very complex ICs after they were manufactured and after they were installed in systems.

The testability concepts implemented by the VHSIC contractors in the area of testable circuit design are presently being used in many commercially available ICs. Several ASIC vendors presently include Scannable Sequential Elements in their design libraries.

Part of the effort on BIT and BIST led naturally to the development of the VHSIC test bus interoperability standards - the TM-Bus and the ETM-Bus which are discussed fully in Section 3.1.2. These standards have become the focus of steps toward establishing an industry-wide, IEEE set of standard test busses.

6.5 Commercial Applications

6.5.1 Desktop Supercomputers Using VHSIC

Commercial versions of VHSIC technology have been used to develop a series of low-cost, desktop supercomputers. The QUEN family of array processors was inaugurated at the IEEE Workstations Symposium held at the Johns Hopkins Applied Physics Laboratory (JHU/APL) in October 1989. Both the 1.25 micron, 25 megahertz technology and the efficient massively parallel array architecture are products of the VHSIC Program.

The QUEN processor, developed at JHU/APL, under Independent Research and Development funding, in conjunction with the VHSIC Program, brings low cost supercomputing to the desk top. It is the first available, commercial, parallel processor to bring CRAY 1 computation speeds into the minicomputer price range.

The QUEN approach to high speed computation uses the Memory-linked Wavefront Array Processor technology. Based on the concept of waves of computation traveling through an array of processors, it was created to provide high speed solutions of numerically intensive computational algorithms. In its most general form, the array is configured as an n-dimensional mesh of processors, each operating as an independent unit executing instructions stored in its private, local program memory. Data for each processor is contained in multiport memories connected to the adjacent processor on its boundaries. Computation and data flow in the mesh are controlled with hardware synchronization structures in each multiport memory.

The first processing implementation used all commercial logic chips and required 3 circuit boards. Each multiport memory required an additional circuit board. Once feasibility had been established, the first prototype memory/processing element module was developed using the VHSIC multiport memories from TRW and FPMAK arithmetic elements developed with VHSIC features by Raytheon. This unit operated at 10 MHz and required 2 circuit boards per memory/processing element. The technology was then transferred to Interstate Electronics Corporation for insertion into the commercial market. Here, a different approach was used for implementing the processor. Instead of using VHSIC components for the arithmetic elements, commercial VLSI chips were used with the interconnection logic done in VHSIC technology gate arrays. The large pin counts and density of VHSIC gate arrays permitted a single gate array chip to implement interconnection logic for both the memory and processing elements. The result was a single board module containing up to 128k words of 32-bit memory and 16k words of program memory, operating at 20 million floating point operations per second. In addition the cost of the unit was reduced by a factor of 2.

Today a family of QUEN Array Processors based on commercial spin offs of VHSIC technology is being marketed for commercial and military applications by Interstate Electronics Corporation. The processors are available embedded in an Intelligent Imaging system, and as attachments to VAX/VMS host computers or Sun workstations. The members of this family of processors are differentiated by the number of processing elements in a system. The largest unit provides 1.28 billion floating-point operations per second and the smallest 80 million. Two units, each capable of 128 million floating-point operations per

second, are installed at The Applied Physics Laboratory. One unit is installed on the JHU/APL computer network for general use while the other is used for sonar signal and image processing.

The use of VHSIC technology in this application reduced the size and cost of the unit and increased its processing speed, both by a factor of two. In addition, it increased system reliability and made comprehensive system testing possible. The QUEN supercomputer is a successful example of "dual use" technology. DoD developments are being used to meet Defense systems needs as well as to enhance the capabilities and competitiveness of U.S. commercial technology.

CHAPTER 7 - VHSIC INDUSTRIAL BASE

CHAPTER 7

VHSIC INDUSTRIAL BASE

It is evident that the system insertions and technology demonstrations of the VHSIC Program described in Chapters 4 and 5 have had a major impact on DoD system developments. Not only have the new hardware components gone into new systems but the techniques for designing complex chips and subsystems are being increasingly automated. Design automation is necessary in order to be able to handle the enormous amount of data required to design them accurately within reasonable time and cost limits. To support both the fabrication and design activities, an increasing number of companies are providing products and services which meet VHSIC requirements and which have become generally available to the defense community.

The impact of the VHSIC program on the industrial base is illustrated by the paper contributed by two VHSIC program managers from one of the largest members of the U.S. semiconductor industry. The sections following the paper describe the VHSIC manufacturing and design capabilities of a number of companies that responded, as of March 1990, to a request for such information. The descriptions are brief and are intended only to illustrate the general capabilities available at the time this report was written. For more detailed, specific, up-to-date information, direct contact with the companies is necessary.

The Impact of VHSIC at IBM: A Case Study

Robert H. Estrada, IBM VHSIC Program Manager
and
Harley A. Cloud, University of Maryland
(Former IBM VHSIC Program Manager)

IBM has been a participant in both Phase 1 and Phase 2 of the DoD VHSIC program. Over the ten year period of the VHSIC program it has provided IBM with the motivation and focus for establishing a semiconductor design and fabrication facility which meets the electronic technology needs of DoD systems and, which, at the same time, has interacted positively with its commercial semiconductor activities. Under this impetus, IBM enhanced its ability to design strategic and tactical systems, made the corporate commitment to establish a military IC pilot line that would be accessible to the military contractor community, and has incorporated many of the VHSIC technology advancements into IC products for space and tactical applications. The development of the VHSIC technology under the management of the DoD program offices has proven to be the critical integrating element for establishing these capabilities.

Under the VHSIC program, the major objectives and associated results at IBM can be summarized as follows:

- Established a 1.25 micron NMOS technology – 1982
- Established a 1.0 micron CMOS technology – 1985
- Established a 0.5 micron CMOS technology by scaling 1.0 micron CMOS to 0.5 micron CMOS – 1987
- Established an operational pilot line capable of producing VHSIC chips at 1.25, 1.0, and 0.5 micron levels meeting all DoD technical requirements, i.e. FTR, density, performance, etc.
- Established an automated design capability and operational pilot/foundry line at both 1.0 micron and 0.5 micron which meet VHSIC technical requirements. These facilities were made available for users within IBM and the DoD contractor community in 1988.
- Provided for the use of VHDL in both military and commercial design procedures in 1987 with full validation projected to be completed in 1990.

In undertaking the VHSIC program, IBM adopted a conservative development plan for Phase 1 by first establishing the design and fabrication capabilities needed to provide VHSIC products and support and then demonstrating these successfully in 1984 with a single, very advanced chip design using NMOS technology. This chip, identified as the Complex Multiply and Accumulate (CMAC), had 37,000 gates and 101,000 transistors, was 8 millimeters square, and performed very complex digital signal processing. VHSIC Phase 1 proved to be extremely valuable to IBM in learning how to produce such an advanced level of military IC technology reliably and efficiently.

As a result of the Phase 1 effort, IBM realized that the NMOS technology, though adequate for Phase 1, would not be able to meet the performance requirements anticipated for VHSIC Phase 2 or, more importantly, for future systems in general. IBM therefor made an internal transition from the 1.25 micron NMOS process to a 1.0 micron CMOS process which had been under development for commercial use. The 1.0 micron CMOS technology is now used in all of our products for DoD systems. The 1.0 micron CMOS process also served as a basis for the VHSIC Phase 2 program along with the Phase 1 design libraries and design tool methodology. The migration from NMOS to CMOS at IBM was accelerated by at least a year as a result of the VHSIC experience and was one of the most notable impacts of the VHSIC program.

A conservative fabrication approach was again chosen for Phase 2. The 1.0 micron CMOS technology was used with the MOS transistor gates scaled down to 0.5 micron in order to meet the VHSIC requirements for density, performance, and FTR. The design program, however, was a more ambitious effort than Phase 1.

Several chip types of different size, function, and performance were developed. These chip capabilities and associated brassboards were successfully demonstrated in December 1988.

In addition to the overall focus on the design and production of military ICs which VHSIC has provided, the program has also given much needed direction to the industrial community on the solution to many specific technical IC design and fabrication problems which are important for military systems. One of the most crucial of these problems is that of achieving the radiation hardness that is required for military equipments in tactical and strategic warfare conditions. Results in this area have been excellent. The radiation hard processing technology developed at IBM under VHSIC has been incorporated into the standard fabrication schedule for all military ICs with no appreciable increase in processing cost. The same process can also be used effectively in selected commercial applications such as space.

VHSIC has emphasized the use of test chips having structures on them carefully designed to provide data that predicts the performance, reliability, radiation effects, and yield of subsequent product chips. These test chips have provided excellent projections on how producible the tested technology will be. The VHSIC test chips and the data they provide has enabled IBM to construct more accurate yield and reliability models than heretofore. This concept is being further developed as the approach to the "generic" qualification of IC production lines ——— an effort which IBM strongly supports and is introducing into its production lines.

Packaging has been another key element of VHSIC emphasis. In order to meet the stringent VHSIC requirements, both single chip and multi—chip packages with very high I/O counts had to be developed. These packages have evolved into many products that IBM is producing for use in weapon systems as well as future commercial products.

VHSIC technology has made it possible for many advanced, multipurpose processing architectures to be realized for space, avionic, tactical, and strategic applications. The architectures emphasize real time processing, very high throughput, extensive instruction sets in a variety of environments from benign to extreme such as that needed in certain space applications. A key factor in this development has been the design and fabrication of a large family of generic multifunction chips in 1.0 micron CMOS technology. Over 40 product chips have been produced, many of which serve as the bases for subsystem level hardware modules that can be configured into systems using an Ada based support environment. In addition, automatic scaling of the 1.0 micron designs to 0.5 micron (FET gate length) has been demonstrated. This allows the production of higher speed chips for use in system upgrades and future applications.

The design and optimization of such architectures required the development of design and analysis tools such as the VHDL and built—in—test circuitry both of which have received high priority under VHSIC. IBM has been using and inserting these VHSIC technologies into a variety of military and commercial programs.

VHSIC has been an outstanding and productive program with many positive accomplishments achieved directly under the program sponsorship but also with many side benefits for corporate IBM. The VHSIC program came along at just the

right time. The objectives established by DoD strongly influenced our decision to establish a semiconductor capability for providing the advanced technology needed in future DoD systems. The objectives were also consistent with our long term commercial activities. The VHSIC activities within IBM could therefore be smoothly coordinated among four IBM corporate facilities. The program was managed and carried out primarily by the Federal Sector Division at Manassas, Virginia. Major contributions to the technology development were funded by IBM at the General Technology Divisions in Burlington, Vermont, and E. Fishkill, New York. The Thomas J. Watson Research Laboratory at Yorktown Heights, New York, also provided basic research and development support.

These coordinated activities were strongly focused and directed by the goals and schedule of the VHSIC program. The character and course of IBM's corporate policies and plans for advanced ICs for military use have been substantially modified and accelerated as a result of its participation in the VHSIC program.

7.1 Design and Manufacturing Capabilities

7.1.1 AT&T Microelectronics

- o Fabrication process
  - 1.25 micron bulk CMOS, 5 V, radiation hard; QML certified; single and double level metal interconnect

- o Devices for sale
  - Bulk CMOS, radiation hard, 256k and 64k SRAMs

- o Form
  - DIP, 24-pin, 600-mil ceramic package

- o Services available
  - Foundry

- o Point of contact
  - Edward J. Schmitt 201-771-4300
    Manager, Military/Aerospace
    Market Development
    AT&T Microelectronics
    2 Oak Way
    P.O. Box 610
    Berkeley Heights, NJ 07922

7.1.2 Honeywell

- o Fabrication processes
  - 1.25 micron bulk CMOS, radiation hard; QML certification in 1990
  - 0.8 micron silicon-on-insulator CMOS, radiation hard; in development

- o Devices for sale
  - Static RAMs, 16 to 64k
  - Digital gate arrays, 15k gates, radiation hard; VHDL model available
  - Standard cells, radiation hard; VHDL model available
  - Test bus interface unit, compatible with TM Bus Interface Specification, Version 3.0; VHDL model available

- o Form
  - PGA, LLCC, LCC, and hybrid packages available; pin counts 14 to 284 pins
  - Custom packaging

- o Design capability
  - Range from gate to mask level designs

- o Other services
  - Entry points range from net list to foundry
  - VHDL capability
  - Applications engineering
  - Design training seminars and workshops

- o Points of contact

- George Anderson (Radiation Hard Devices)	612-541-2045
- Charles Hudson (Test Bus Interface)	612-541-2185
- David Wick (Silicon Compiling)	612-541-2801
- Michael Caruso (Applications/Training)	612-541-2198

Honeywell Solid State Electronics Center
12001 Highway 55
Plymouth, MN 55441

7.1.3 Hughes Microelectronics Centers - Carlsbad and Newport Beach

- o Fabrication processes
  - 1.25 micron CMOS/SOS, 3.3 to 5 V, radiation hard
  - 1.1 micron CMOS, radiation hard
  - 0.9 micron CMOS, radiation hardening in development

- o Devices for sale
  - Multi-channel correlator
  - Single channel correlator
  - Signal tracking subsystem
  - Static shift register
  - Standard cell semi-custom devices
  - Configurable gate arrays

- o Forms
  - Chip
  - Single chip packages including PGA, LCC, LLCC, and quad flatpacks
  - Multichip packages

- o Design capabilities
  - Standard cell, full custom, structured-custom cell, and gate array
  - RAM, ROM, and PLA generators
  - Mentor Graphics and CALMA workstations
  - Design entry from behavioral, RTL, or logic description
  - VHDL capability expected in 1990

- o Other Services
  - Foundry service from CALMA tapes

- o Point of contact
  - R.W. Dodge 619-931-3196
    Hughes Microelectronics Center
    6155 El Camino Real
    Carlsbad, CA 92009

7.1.4 IBM

- o Fabrication processes
  - 1.0 micron CMOS, 5 V, DESC certified 12/11/87
  - 1.0 micron CMOS, 5 V, radiation hard

  - 0.5 micron CMOS baseline, 3.3 V
  - 0.5 micron CMOS, 3.3 V, radiation hard

- o Devices for sale
  - Configurable SRAM
  - Bus Interface Unit
  - Systolic Processor

- Address Generator
- Signal Processing Element
- 64k radiation hard SRAM
- 256k radiation hard SRAM (engineering samples)
- Fourier transform module boards
- Generic VHSIC Spaceborne Computer chip set
- Common Signal Processor chip set
- Radiation hard Vector Processor brassboards
- Radiation hard 32-bit Processor (in development)

o Form
- VHSIC chip on silicon
- Single chip package
- Multi chip package
- C4 flip chip
- Wirebond

o Design capabilities
- VHDL design capability 4Q90
- Custom, master image, gate array to 70k gates
- Subsystem and system level entry points
- Chip/system simulation (Hardware Accelerator)

o Other services
- Foundry: chip design, simulation, mask procurement, chip fabrication, and LSSD test methodology

o Points of contact
- Philip B. Johnson (Program Manager) 703-367-5547
- Jay Harford (VHSIC Marketing) 703-367-1041

IBM Federal Systems
9500 Godwin Drive
Manassas, VA 22110

7.1.5 LSI Logic Corporation

o Fabrication Process
- 1.0 micron CMOS, 5 V

o Devices for sale
- Gate arrays to 100k

- Standard cell based ASICs
- SPARC (scalable processor architecture) 32-bit RISC CPU
- Single chip floating point unit for SPARC
- Combined MMU, cache controller, cache tags for SPARC
- MIPS architecture 32-bit RISC processor with memory management
- MIPS architecture 32-bit floating-point processor
- MIPS architecture read-write buffer
- 32-bit IEEE floating point processor
- 8-bit error correcting Reed-Solomon Codec

o Form
- Chip and single-chip package

o Other services
- Design development tools with associated training courses
- VHDL models (under development)

o Point of contact
- Joe Ferro 408-434-6422
  Manager, Strategic Military Programs
  LSI Logic Corporation
  48660 Kato Road
  Fremont, CA 95438

7.1.6 Motorola

o Fabrication processes
- 1.2 micron CMOS, 5 V, 3-level metal, single layer poly
- 0.8 micron CMOS available late 1990
- Certification for wafer fabrication facility scheduled for 1990; back-end facilities (package and test) are currently certified.

o Devices for sale
- High density gate array family, 3k to 105k gates; RAM/ROM capability
- Custom bipolar and CMOS

o Form
- Single chip packages: chip carriers, quad flat pack, and pin grid arrays

o Design capabilities
- Designs accessible through Mentor/Sun workstations at the schematic entry level

- o Other services
  - VHDL models for gate arrays (under consideration)
  - Foundry (CALMA database supplied by customer)

- o Point of contact
  - Dick Hurley 602-897-3782
    MS EL-376
    Motorola, Inc.
    Military Products Operation
    2100 E. Elliott Road
    Tempe, AZ 85284

7.1.7 National Semiconductor Corporation

- o Fabrication processes
  - 0.8 micron CMOS, 5 V; in process of certification as beta site, within QML program
  - 0.8 micron BiCMOS, 5 V
  - 0.8 micron ECL, 5 V

- o Devices for sale
  - CMOS standard cells up to 80k gates
  - ECL and CMOS gate arrays from 7.5k to 250k

- o Form
  - Chips and single packages: PGA, DIP, leadless and leaded chip carriers

- o Design capabilities
  - National DA4 design automation software
  - VHDL simulation capability available through Vantage Analysis
  - Additional VHDL simulation under development in conjunction with Silicon Compiler Systems and Verilog
  - GENESIL compiler supports CMOS processes
  - Design entry through National DA4, customer's workstation, or GENESIL compiler

- o Other Services
  - Design tool training

- o Point of contact
  - Kirk Lemon 408-721-4172
    Military/Aerospace ASIC Marketing Manager

National Semiconductor Corporation
MS 10-105
2900 Semiconductor Drive
Santa Clara, CA 95052-8090

7.1.8 Performance Semiconductor Corporation

o Fabrication processes
- 1.25 micron CMOS, 5 V
- 1.0 micron CMOS, 5 V
- 0.75 micron CMOS, 3.3 V

o Devices for sale
- SRAMs to 256k
- SRAM modules 448k to 1.0M
- Logic Circuits
- 16-bit 1750A processors
- 32-bit RISC processors
- 3.3 V SRAMS to 64k
- ASICs through GENESIL design environment

o Form
- DIPs: plastic; ceramic; up to 600 mil
- Leaded and leadless chip carriers

o Point of contact
- Les Welborn 408-734-8200
  Performance Semiconductor Corp.
  610 E. Weddell Drive
  Sunnyvale, CA 94089

7.1.9 Raytheon Company

o Fabrication processes
- 1.25 micron CMOS, 5 V, radiation hard; certified to 9858 and 45208; compliant with 883 and 38510
- 1.0 micron CMOS, 5 V

o Devices
- Family of channeled gate arrays from 5k to 20k gates
- Family of standard cell arrays from 10k to 40k gates

- Family of sea-of-gates array from 77k to 167k gates
- FPMAK - Floating Point Multiply/Accumulate Kernel

o Form
- Wafer
- Chip or die
- Single chip package - DIP, PGA, LFP and LCC

o Design capabilities and entry points
- Simulation, fault grading, routing and DRC/ERC checking
- GDS II entry format
- Built-in test
- Integrated verified library for gate array and standard cell designs

o Other Services
- Custom chip foundry

o Point of contact
- Scott Stephen 508-470-9114
  Raytheon Company
  358 Lowell Street
  Andover, MA 01810

7.1.10 Silicon Compiler Systems

o Fabrication processes supported
- 1.2 and 1.0 micron CMOS, 5 V
- 1.25 micron CMOS, 5 V, radiation hardened

o Foundries supported
- Harris/GE
- Hewlett-Packard
- Motorola
- National Semiconductor
- NCR
- Performance Semiconductor
- VTC
- USC

o Products for sale/lease
- GENESIL silicon compiler for system engineers
- GDT silicon compiler for IC design engineers

- GENECAL tool for foundry calibration
- GENEPORT tool for addition of new compilers
- LogicCompiler logic synthesizer
- Automatic test vector generation
- LSIM mixed-mode analog and digital simulator
- Radiation hard libraries for GENESIL and GDT
- Radiation hard simulation and analysis tools
- VHDL simulation

o Design capabilities
- Full custom chip design
- Mixed mode multi-level simulation
- Fault simulation
- Design for test
- VHDL descriptions of new designs

o Other services
- Design tool training courses
- On-site IC design consulting
- Custom IC design contracts

o Points of contact

- Bernard Jamin-Bizet (GENESIL)	408-371-2900
- Richard Gordon (GDT)	201-580-0102
- Jim Griffeth (LSIM)	201-580-0102

Silicon Compiler Systems
2045 Hamilton Avenue
San Jose, CA 95125

7.1.11 Texas Instruments

o Fabrication processes
- 1.0 micron CMOS
- 0.8 micron CMOS
- 0.8 micron BICMOS

o Devices for sale
- 1.25 micron CMOS gate array family to 25k gates
- 1.0 micron CMOS standard cell family to 50k gates
- 0.8 micron BiCMOS gate array family to 100k gates

- 1.0 micron CMOS digital signal processor family, 33 MFLOPS, 16 MIPS maximum throughput
- 0.8 micron CMOS MIL-STD-1750A chip set, including:
  Data processor unit
  Memory management unit
  General logic unit
  Processor control interface
  Discrete input/output
  TM-Bus interface unit
  PI-Bus interface unit

o Form
- Single chip packages: DIP, PGA, quad flatpack, gullwing

o Design capabilities:
- Custom ASICs to 100k gates and standard ASICs (gate arrays or standard cells) using Daisy and Mentor workstations
- Silicon compiler design services
- Module design

o Points of contact:
- Robert F. Grimmer (chips) 214-480-1942
  Texas Instruments
  P.O. Box 660246 MS 3145
  Dallas, TX 75266

- Alan Johnson (modules) 214-575-5449
  Texas Instruments
  P.O. Box 869305 MS 8435
  Plano, TX 75086

7.1.12 TRW

o Fabrication processes
- 1.25 micron CMOS, 5 V, radiation hardened
- 0.5 micron CMOS, 3.3 V, radiation hardened (in development)
- 1.0 micron bipolar CML, 5 V, radiation hardened
- 1.25 micron CMOS, 5 V

o Devices

Phase 1
- Window Addressable Memory
- Content Addressable Memory
- Four-Port Memory
- Address Generator
- Microcontroller
- Matrix Switch
- Register Arithmetic Logic Unit
- Multiplier Accumulator
- Convolutional Decoder
- Convolver

Phase 2 (available now as engineering samples)
- Central Processing Unit Arithmetic Extended (CPUAX) Superchip
- Arithmetic Logic Unit
- Multiplier/Accumulator
- Storage Element
- Read Memory Interface
- Write Memory Interface
- Column Disable Block
- One Port RAM
- Microcontrol Unit
- Universal Processor
- Bus Interface Unit

o Form:
- Bare die (limited quantities for some designs)
- 132-pin JEDEC perimeter-leaded package
- 308-lead ceramic substrate package (for CPUAX)

o Design capabilities
- From system/subsystem specifications down to mask layout data
- VHDL chip descriptions accepted as part of entry data

o Point of contact
- Program Development Manager 213-814-2400
  Electronics and Technology Division
  TRW Electronic Systems Group
  One Space Park
  Redondo Beach, CA 90278

7.1.13 United Technologies Microelectronics Center

- o Fabrication Processes
  - 1.2 micron CMOS, radiation hardened
  - 1.2 micron CMOS
- o Devices for Sale
  - Gate arrays, 20k and 50k, rad-hard
  - Gate arrays, 25k and 60k (available 3Q90)
- o Form
  - Chip
  - Single-chip package
- o Fabrication and packaging capabilities
  - Foundry, PG tape, mask/reticle input
  - PGA, leaded chip carriers
- o Design Capabilities
  - Custom, standard cell, and gate array design services
  - Workstation and VAX-based design system supports design capture, logic, timing and fault simulation, and layout and test program generation.
- o VHDL Capability
  - Circuit description output in VHDL (available 2Q91)
- o Point of contact
  - Robert Cook 719-594-8124
    Semicustom Product Line Manager
    United Technologies Microelectronics Center
    1575 Garden of the Gods Road
    Colorado Springs, CO 80907

7.1.14 VTC Incorporated

- o Fabrication processes
  - 1.0 micron CMOS, 5 V
- o Devices
  - VME bus, VIC068 interface controller
  - VME bus, VAC068 address controller

- o Form
  - 144-pin PGA

- o Services available
  - 1.0 micron foundry on GENESIL silicon compiler

- o Point of contact
  - Craig Carrison 612-851-5200
    VTC Incorporated
    2401 East 86th Street
    Bloomington, MN 55425-2702

7.1.15 Westinghouse - Advanced Technology Division

- o Fabrication process and certification
  - 1.25 (0.9 eff) micron CMOS, 5 V, radiation hard; 3.3 V and SOI versions also available
  - Fabrication and assembly lines, and design system, certified by DESC December 20, 1989
  - Qualification of gate array family planned by 4Q90

- o Devices
  - Gate array family - 3k to 54k

- o Form
  - Tested chips
  - Leaded chip carriers/qual flat packs, 132 lead form to be qualified
  - Pin grid array packages
  - DIPs

- o Design facility
  - Gate array routing from Mentor net list
  - Masks made from CALMA database
  - Entry points: net list with test vectors or schematic or mask tape
  - Complete cell library in Mentor and Daisy workstations
  - Logic capture and simulation on Mentor and Daisy workstations
  - Fault simulation by Mentor Quickfault
  - VHDL description available at gate level
  - Built-in-test resources and methods for use on all designs
  - SOS GDT technology file created for custom circuit design
  - Full custom and memory design capability also available

- o Other services
  - SCS GENESIL Compiler calibration underway
  - Compiled circuit (SCS GENESIL) foundry capability planned for 3Q90

- o Points of Contact
  - D. R. Sartorio 301-765-6744
    Dr. R. C. Lyman 301-785-2379
    Westinghouse Electric Corporation
    P.O. Box 1521, MS 5210
    Baltimore, Maryland 21203

7.2 Commercially Available VHSIC Design Tools

As pointed out in a number of places in the previous chapters of this report, VHSIC has had a particularly significant influence on the development of design automation software. The accompanying paper, which discusses this role of VHSIC and VHDL, has been contributed by an active participant in the efforts to transform the developments into useful products for design automation.

The list following the paper is a sample of the companies that are developing design tools which directly support the VHDL in various design tasks and in making those tools commercially available.

The Impact of VHDL on Design Automation Tool Development, Acquisition, and Use

Randolph E. Harr
C.A.D.onomist
Chairman, VHDL User's Group

Introduction

VHDL is a powerful language standard being used for a wide number of tasks in the electronic design process. It has been adopted in the Department of Defense and commercial design community relatively quickly. When released by the US Government to the electronics industry in 1986, VHDL was more advanced than the other design languages generally available in the CAE marketplace. There are many factors that have pushed the CAE industry into adopting VHDL quickly. Vendors without an advanced design language as well as vendors wishing to

enhance the capabilities of their proprietary languages have both readily adopted VHDL.

Since becoming an IEEE standard, VHDL has taken on a life of its own and continues to be improved in response to the needs of the market. Design automation tool suppliers add new capabilities for systems design to VHDL and integrate it with other tools that are part of the total design process. Users are asking for the standard in order to decrease costs in acquiring and using multi-vendor tool sets and to protect engineering investments in designs. Outlined below are the benefits derived from VHDL and the activities taking place in the design automation community.

VHDL ——— An Industry Standard

VHDL can be termed an industry standard due to the many organizations adopting its technology. These efforts are in addition to the internal Department of Defense efforts. The Computer Society of the IEEE Design Automation Standards Subcommittee (DASS) and the Standards Coordinating Committee on Test (SCC-20) both standardized the language during 1987. Subsequently, the IEEE Test Technology Committee, the Electronics Industries Association (EIA), and the Standard Computer Kompenten (STACK) all adopted VHDL as a base language for developing further usage standards. The American National Standards Institute (ANSI) has since ratified the IEEE standard. And yet an additional endorsement is impending: the National Institute for Standards and Technology (NIST, formerly NBS) is soon to adopt VHDL as a Federal Information Processing Standard (FIPS). Even wider adoption is expected as more experience is gained in applying the language to related areas of the design process.

Given VHDL is already a standard, one may wonder why all the additional standards activities exist. The reason lies in the fact that VHDL, although embodying concepts unique to hardware design, is a general language. It, like natural or computer programming languages, is rich and verbose. Therefore, many ways of expressing the same or similar meaning exist. By creating usage standards from electronic design information models, unambiguous information exchange can occur. There are many industry groups which are undertaking the task of defining these usage standards.

Worth mentioning first are the efforts going on within the DoD at standardizing the method of representing test information. These efforts are resulting in the IEEE standardization of a test waveform language termed WAVES. The multi-level draft standard incorporates unrestricted VHDL as the most powerful specification level. WAVES will be a usage standard which assists the specification of test information in design tools and eventual transfer of test information to hardware testers.

The Electronic Industries Association (EIA) has taken an aggressive stance on design automation issues by forming the new Design Automation Division. Their project, the VHDL Model Development and Validation (VMDV) consortia, is expected to pay for the development of source code VHDL models of standard component parts. These models will be suitable for use in board level simulation,

along with custom behaviors, to verify board designs and custom (ASIC) specifications. The models developed are expected to meet (if not exceed) the military VHDL documentation standards. They are expected to be used in developing DoD acceptance procedures.

There are other standards organizations which are working at specifying standard uses for VHDL. They are the Standard Computer Kompenten (STACK), the IEEE CS DATC Design Automation Standards Subcommittee (DASS) and the VHDL Users' Group.

STACK is a European and United States industry—represented organization whose goal is to define a standard method of interchanging functional models of components used in the design of large, digital electronic systems. They have adopted VHDL as their base language and are now working on usage standards.

The IEEE DASS is the organization with the official VHDL standard charter and has eight working groups looking into various Design Automation and VHDL standards. Four of note are the VHDL Analysis and Standardization Group (VASG), the VHDL Modeling Working Group, the VHDL Intermediate Form and Analysis Standardization Group (VIFASG), and the WAVES Working Group.

The VHDL Users' Group formed in early 1988 to provide a wider forum for the exchange of VHDL information. Their main activities are in holding two general meetings a year, providing a newsletter, maintaining an electronic Bulletin Board Systems (BBS), and supporting Special Interest Group (SIG) activities. The group serves as a focal point for VHDL information gathering, discussion, and dissemination. For example, the BBS file repositories have most of the VHDL standard packages (source files), models, benchmarks, and documents available for collection.

A sub—group of the VHDL Users' Group is the ad hoc VHDL Design Exchange Group (VDEG). They are developing a subset of VHDL's capabilities that will allow current CAE vendors to utilize VHDL within their existing tool environment while maintaining a smooth transition from the tremendous investment in CAE tools and capabilities already installed. To date, the group has decided on an interoperable type package and primitive component library for gate level simulation. Additional efforts at defining common supportable subsets and model timing are underway.

A major benefit of the usage standards is in the development of interoperable simulation models of commercial components. With such standards, these models are being developed by independent organizations. Much like the VHSIC interoperability standards define the standard electrical interface between chips and boards, VHDL interoperability standards perform the analogous function for models in design tools. The end result is that the models need only be created once for each part, not for each design tool and vendor.

Developers of Design Automation Tools

Many CAE vendor companies were just launching internal development efforts into tools for advanced systems design when VHDL came about. Design tools applied to problems above the gate (implementation) level require hardware

description languages (HDL) as part of the design process. VHDL, being a published industry standard, significantly reduces the costs to acquire and develop these advanced CAE systems. In addition, a standard HDL allows the "integration not interface" (Reference 7.1) of the many tools required to do complex digital electronic systems design.

The impact on the design automation tool industry of VHDL has been extensive. A standard HDL reduces the cost to develop and maintain tools based on an HDL technology. It also becomes easier to understand advancements in design tool technology. In fact, due to VHDL's power, there has been a new wave of start—up organizations in an otherwise consolidating industry.

The VHDL standard has considerably reduced the cost to develop CAE related tools industry wide. No longer does a company need to research previous industry and university work to develop a proprietary HDL. Instead, a much smaller cost is needed to acquire and incorporate the standard HDL. This is especially true for companies without a previous HDL commitment. Also, VHDL is rich in features and is advanced, compared to other HDLs. Therefore, absorption of the standard dramatically increases the knowledge base of a particular company. Finally, because it is an industry standard, there are additional technology and tools available to assist in developing a complete tool solution.

The VHDL standard reduces the tool developers cost to maintain tools. A tool company need not maintain a constant investment into keeping a proprietary HDL current. Instead, a much smaller investment into helping maintain the VHDL standard within the industry as a whole is all that is required. Currently, VHDL is ahead of the needs of the market. So for the near term, the maintenance cost is less with the standard. Cost maintenance will continue to be lower as long as the standard keeps up with the technological requirements of tools and users.

The VHDL standard increases the ability for a tool company to absorb state—of—the—art technology. Research results of universities are more readily understood and accepted when based on a known, existing standard. Point solution tools are usable by a wider community, thus allowing the development cost to be spread across the industry.

VHDL has brought a new infusion of growth into the CAE market by giving start—up companies a unique entry point into the market. With these vendors, VHDL has the most to offer without bringing extra burden. This can be seen in both new, advanced technology companies and those from existing product markets.

Advanced technology CAE companies have the most to gain and least to lose in picking up VHDL. In most cases, they are start—ups, or just growing into the use or need for a standard HDL. Therefore, they have no real commitment to a proprietary HDL. In fact, these companies want a non—proprietary HDL in order to make their technology more useful to a wider audience. Designers wishing to be aggressive in the adoption of VHDL or an advanced CAE technology rely on these early adopters of the standard.

There are many examples of start—up ventures based on the VHDL technology. Vantage Analysis Systems, CAD Language Systems, Inc., VISTA Technologies, and Expertest are just a few. Each has a unique tool for a different

purpose or segment of the market. Some additional "start–up ventures" are actually older companies who have refocused or expanded into the CAE market as a result of VHDL. Examples here are Intermetrics, JRS Research, ComDisco, and RTI / CADRE Technologies. Many of these new companies got their start (and capital) as VHSIC tool contractors.

All these companies contribute further to the standardization effort by introducing VHDL into a new, growing market. A prime example of an advanced technology that needed a standard HDL is the synthesis industry which switched to using VHDL almost overnight.

VHDL has became the language from which synthesis tools and research is based. For this reason, it is expected that synthesis requirements of the language will make a major impact on the form and function of behavioral models eventually delivered to the DoD. A goal for the behavioral models in the DoD is to provide a means for future reprocurement of parts after the source or base technology becomes obsolete. Synthesizeable models which represent engineering specifications will allow for the quick redevelopment of manufactured parts.

Previously, the synthesis companies were either selling their own proprietary language or adopted a vendor's language. If using a proprietary language, they introduced yet another language into the design environment when selling their tool. If based on a vendor's language, they were tied to that vendor's customer base. In either case, they were always being faced with the need to accommodate other HDLs that customers used. VHDL eliminated this need, thus removing a tremendous burden on the industry to create custom links and training for a multitude of languages.

Although overlooked by many, this was most notably demonstrated by IBM's Advanced Business Systems Division. This commercial concern picked up the VHDL standard before IEEE sanction and built a behavior to silicon synthesis system around it. Their practical use of the DoD 7.2 standard led to many of the revisions in the IEEE 1076 standard. The successful application of HDL technology led to widespread endorsement of VHDL within IBM.

Commercial examples of the adoption of VHDL in the synthesis community are pervasive. Synopsys, SILC Technologies, and Trimeter have released or plan VHDL releases. Additionally, VLSI Technology, Viewlogic, and SCS have released synthesis systems supporting VHDL.

In a new twist, Synopsys has made available a reverse synthesizer which will take in gate level netlists of many forms and create a VHDL gate netlist or synthesizeable RTL behavior. In this way, older technology designs can be reverse engineered quickly and re–implemented in a current technology. They hope to capture a portion of the large reprocurement market with this technology.

But it is not just the start–up concerns who have been introducing VHDL as a standard. Existing CAE workstation vendors have been quick to adopt the standard. The major workstation companies in the CAE tool market had the least incentive to adopt a standard language. They already had significant investments in tools based on proprietary languages including libraries, database formats, and entry/edit tools. In addition, their large installed base and third party tool market were additional incentives not to replace their technology. Except for start–up companies, there was initially little movement towards using VHDL.

HDL technology was introduced into traditional CAE workstation systems as a method to create new, custom primitives in a library. In this way, the design system became more independent of the physical technology. But as users started creating their own primitives, uses of the physical design tools earlier in the design cycle naturally evolved. Now, the bulk of physical IC and logic designers are actually utilizing the tools for system design techniques.

Viewlogic was the first CAE company to modify and release a system with VHDL as part of a design system. Although limited to a "behavior" subset of the language needed by their customers, it served to introduce the language into a wide, installed base. At the time, Viewlogic did not have an HDL and so adopted the portion of VHDL that would meet their need instead of inventing a proprietary one. As VHDL grows in standardization, Viewlogic is evolving its release into full language support.

The market was still slow to adopt VHDL until the industry leader, Mentor Graphics, jumped in. Mentor, with a claimed installed base of 20,000 sets, announced its intention to base its product on full VHDL. VHDL was added to the large project of a complete re—coding and introduction of new technologies into its design system. This single announcement became the "straw that broke the camels back". Soon all the other vendors announced support, stepped up commitment, and were competing to be the first and best. Nine months later, at the 1989 annual design automation industry show, every major vendor was either demonstrating or promoting a VHDL capability.

For example, out of six major CAE platform vendors, Mentor Graphics, Valid Logic, DAZIX, Cadence, Intergraph, and Viewlogic, all have commitments to deliver or are delivering VHDL in one form or another. Of the additional major simulation companies, ZYCAD, IKOS, HHB Systems, GenRad, Teradyne, and Gateway Design Automation, all have released or are preparing for release VHDL systems. Some of them are major commitments with complete implementations and new tools. Others are more minor by providing only a capability to translate a limited VHDL feature set into (and out of) their existing language and environment. Increasingly though, an initial announcement of limited support has been followed up by a major commitment to full VHDL as the market demand grows.

As expected, given the government requirement adopted in 1988, the ASIC vendors are the most prevalent suppliers of VHDL design tools, second only to the workstation vendors. Support for primitive libraries in many proprietary languages is no longer required. They can now develop VHDL models once, internally, and release the same set across the various tools.

Examples of ASIC suppliers currently supporting or expecting to support VHDL are Honeywell, VLSI Technology, Intel, Texas Instruments, and National Semiconductor. In addition, in a recent survey of military ASIC vendors (Reference 7.2) who were asked about their VHDL simulation capability, two of twenty nine said they supplied it now while an additional twenty three said it was planned for release in the next twelve months. Truly the pace is picking up.

The developers of design automation tools are not the only ones reaping immediate benefits out of the language standard. Users who acquire and apply the tools are also aware of benefits gained from VHDL.

Users of VHDL Based Tools See Reduced Costs

Design automation tool users have many needs which VHDL based tools address. The merger mania that had hit the tool industry was proving that they needed control over their design information. Additionally, modeling above the gate level has become a requirement, not an option, with more of the designers.

VHDL—based tools are expected to significantly decrease the cost for users to acquire tools. Tools generating and utilizing VHDL will be much simpler to integrate than those based on incompatible, proprietary languages. Traditionally, it has been the end user who must integrate tools from different vendors when creating a complete environment. With tools based on VHDL, there is a greater chance that output of one vendor will be directly usable as input to another. This will make it possible for even vendors to work together at making tools compatible.

Verification of VHDL—based designs with tools from different vendors will always be possible for users. Even if there is no direct compatibility (that is, two tools utilize incompatible subsets of VHDL), a VHDL description created for one tool can be verified against VHDL generated by another tool. This is done by extracting the VHDL descriptions from both tools and comparing them in a full VHDL environment.

The cost to use design automation tools is reduced when the base language is VHDL. Training engineers takes less effort when all the tools are based on a single HDL. Design information is kept in a non—proprietary form with VHDL, thus allowing information to be more readily extracted and used. This is especially important when previous designs need to be upgraded. Finally, designs are under the control of the designer who may decide to modify HDL code as it is transferred between tools.

Introduction of New Benefits and Technology

VHDL makes possible additional benefits and technology for users than could otherwise be achieved. This is especially true in the board design area where merchant component parts and user specific ICs are integrated into a single design. In this environment, it is crucial for the board and ASIC design tools to be integrated. VHDL provides the integration path by being usable as the base HDL in both environments, thus allowing specifications in both environments to be developed and verified against each other.

As an example, board simulation will now be a feasible method of verifying ASIC functional specifications. A functional specification of an ASIC developed in VHDL can be used to verify the board design, generate test vectors, and used as input to a synthesis tool. At minimum, the board level function can be compared against the gate level implementation done in VHDL. The board netlist in VHDL can be back annotated with layout timing information. It should be noted that VHDL on its own does not guarantee these abilities. It is the adoption of usage specifications and standard design methodologies on top of VHDL which allow this

information transfer and extraction from tools.

The capability to use an ASIC specification in a board simulation rests on the availability of standard component models. Models of standard components are now more available partly due to the maturing industry, new technology, and VHDL. The cost of developing models of standard components is cheaper with VHDL because a model is now usable with more vendors tools. Additionally, the features of simulators are being standardized in VHDL based tools, thus removing custom model development costs. The market is set for a new round of growth with semiconductor suppliers eventually providing support.

The major vendors of standard component models are Logic Automation, Quadtree, LMSI, EIS Modeling and Speed Electronics. In most cases, there is tremendous added benefit when going to VHDL based models that follow the industry usage standards. All the above vendors supply models for major VHDL tool vendor products.

There are two critical tasks that have seen little progress to date but are required to make VHDL a success in the procurement process. These are the validation of tools processing the standard language and validation of the models that are executable specifications of the hardware. The tools processing VHDL must be validated to be in conformance with the standard if true information portability between tools is to exist. Models must be validated against actual specifications, real hardware implementations, and interoperable usage standards if true design information transfer between organizations is to occur. These large tasks are not going to occur in the commercial industry without assistance.

The future holds much promise related to VHDL. Although Government efforts continue (and need to continue) internally to apply and adopt the language in new ways, the commercial market has already surpassed the Government's commitment and is extending the language in ways not thought of originally. By developing the seeds and firmly planting them, the DoD has spurred new growth and integration in the fragmented design automation industry.

Simulators/Analyzers

7.2.1 Dazix

Description: Subset analyzer-simulator

Contact: Nahid Nassirian 415-960-6702
Dazix
PO Box 7006
700 E. Middlefield Rd.
Mountain View, CA 94039-7006

7.2.2 Expertest

Description: VHDL fault simulator

Contact: W. Van Cleemput 415-969-0701
2101 Landings Dr.
Mountain View, CA 94043

7.2.3 Intermetrics

Description: VHDL analyzer and simulator
VAX/VMS
SUN 3 OS 4.XX; SUN 4
APOLLO 3XXX, 4XXX
DEC PMAX
IBM PC 386 (Unix)
Training

Contact: Rachel Rusting 617-661-1480
Intermetrics, Inc.
7333 Concord Ave.
Cambridge, MA 02138

7.2.4 Mentor Graphics

Description: VHDL simulation environment and synthesis; available third quarter 1990

Contact: Rob Mendesdacosta 513-626-1254
Mentor Graphics Corporation
8500 SW Creekside Place
Beaverton, OR 97005-7191

7.2.5 Microelectronics and Computer Technology Corp.

Description: VHDL analyzer and simulator; available to members only

Contact: Bill Read
MCC CAD Program
3500 W. Balcones Center Dr.
Austin, TX 78759

7.2.6 Teradyne

Description: Read and write subset of structural and behavioral VHDL; Vanguard schematic capture will produce structural VHDL. AIDA and LASAR simulators will support VHDL.

Contact: Philip Odence 617-482-2700
Teradyne, Inc.
321 Harrison Ave.
Boston, MA 02118

7.2.7 Valid Logic Systems, Inc.

Description: VHDL analyzer/simulator interfaced to valid schematic editor

Contact: Don Mazur 408-432-9400
Valid Logic Systems, Inc.
2820 Orchard Pkwy.
San Jose, CA 95134

7.2.8 Vantage Analysis

Description: VHDL analyzer and simulator for APOLLO and SUN workstations; interfaced to Mentor software

Contact: Tom Miller 415-659-0901
Vantage Analysis
42840 Christy St.
Freemont, CA 94538

7.2.9 View Logic Systems

Description: Subset VHDL analyzer and simulator for IBM PC/AT class computers

Contact: Ron Ranauro 617-480-0881
View Logic Systems
275 Boston Post Rd. W
Marlboro, MA 01752

7.2.10 Zycad

Description: VHDL analyzer and simulator for general Unix hosts and VAX/VMS interfaced to other analysis tools in the N.2 tool set

Contact: Brian LaPorte 415-688-7486
ZYCAD Corporation
1380 Willow Road
Menlo Park, CA 94025

Hardware Accelerators

7.2.11 Ikos Systems

Description: Interface to IKOS accelerator

Contact: IKOS Systems Inc 408-245-1900
145 Wolfe Rd
Sunnyvale, CA 94086

7.2.12 Zycad

Description: VHDL interface, at the structural level, to the Zycad accelerator

Contact: Todd Oseth 201-538-7833
Zycad
10 Madison Ave.
Morristown, NJ 07960

Synthesis

7.2.13 JRS Research Laboratories

Description: VHDL synthesis to Seattle Silicon Concorde retargetable Ada to microcode compiler via VHDL model

Contact: Erwin Warshawsky 714-974-2201
JRS Research Laboratories

1036 W Taft Ave.
Orange, CA 92665-4121

7.2.14 Silc Technologies, Inc.

Description: VHDL synthesis tool

Contact: Lawrence Beecher 617-273-1144
Silc Technologies, Inc.
34 Third Ave.
Burlington, MA 01803

7.2.15 Silicon Compiler Systems (Now Mentor Graphics)

Description: VHDL synthesis to compiled silicon and compiled silicon to VHDL; available early 1990

Contact: Kirk Lemon 408-371-2900
Silicon Compiler Systems
2045 Hamilton Ave.
San Jose, CA 95125

7.2.16 Synopsys, Inc.

Description: Synthesis tool

Contact: Steve Carlson 415-962-5000
Synopsys, Inc.
1500 Salado Dr.
Mountain View, CA 94043

7.2.17 Trimeter, Inc. (Now Mentor Graphics)

Description: Synthesis tool

Contact: Henry Alward 503-645-7039
Trimeter Technologies
15455 N.W. Greenbrier Parkway
Beaverton, OR 97006

Modeling

7.2.18 EIS Modeling, Inc.

Description: Various VHDL related services, including model development, application specific training, test, and verification of models; LSI LCA 10000 macrocell models

Contact: Gabe Moretti 415-964-2296
EIS Modeling, Inc.
2483 Old Middlefield Way, Suite 130
Mountain View, CA 94043

7.2.19 Logic Automation

Description: VHDL models of standard commercial parts

Contact: Tony Johnson 503-690-6900
19500 NW. Gibbs Dr.
Beaverton, OR 97006

7.2.20 LSI Logic Corp.

Description: VHDL descriptions of macrocells, synthesis from VHDL description to silicon

Contact: Robert Dahlberg
LSI Logic Corp.
E-196
1501 McCarthy Blvd.
Milpitas, CA 95035

7.2.21 Quadtree Software Corporation

Description: VHDL models of electronic parts

Contact: Vicki Andrews 408-436-3550
Quadtree Software Corporation

2020 N. First Street, Suite 205
San Jose, CA 95131

7.2.22 VLSI Technology, Inc.

Description: VHDL descriptions of macrocells; synthesis from VHDL to silicon

Contact: VLSI Technology, Inc. 408-434-3000
1109 McKay Dr.
San Jose, CA 95131

Integration and Adaptation

7.2.23 Cadence

Description: Various VHDL tools around Cadence Framework, Schematic Editor, etc.

Contact: Cadence 408-943-1234
555 River Oakes Parkway
San Jose, CA 95134

7.2.24 CAD Language Systems, Inc.

Description: VHDL training courses; VHDL integration platform targeted to a wide variety of hosts and operation systems for integrated tools such as synthesizers, timing verifiers, and simulators

Contact: Mark Steffler 301-963-5200
CAD Language Systems, Inc.
15245 Shady Grove Road, Suite 310
Rockville, MD 20850

7.2.25 Cadre Technology

Description: Architecture Design and Assessment System (ADAS)

Contact: Cadre Technology 401-351-2273
222 Richmond St.
Providence, RI 02903

7.2.26 Fintronic, USA

Description: VHDL translators and interfacing

Contact: Alec Stanculescu 415-345-4574
Fintronic, USA
40 Stoney Point Place
San Mateo, CA 94402

7.2.27 Gateway Design Automation (Now Cadence)

Description: Translator for Verilog to VHDL; VHDL analyzer simulator

Contact: Ronna Alintuck 508-458-1900
Gateway Design Automation Corporation
Two Lowell Research Center Dr.
Lowell, MA 01852-4995

7.2.28 GenRad Incorporated

Description: Translator for VHDL to/from HILO

Contact: Raymond F. McNulty 508-369-4400 X 2970
Douglas S. Clauson 508-369-4400 X 2862
GenRad, Inc.
300 Baker Ave.
Concord, MA 07142

7.2.29 Ilogix, Inc.

Description: VHDL output from Statemate

Contact: Ilogix, Inc. 617-272-8090
22 Third Ave.
Burlington, MA 01803

7.2.30 Research Triangle Institute

Description: Translators for VHDL structure to schematic, schematic to VHDL structure, VHDL structure to EDIF 2.0, EDIF 2.0, to VHDL structure, VHDL to GENESIL, GENESIL to VHDL

Contact: Wayne Hansley 919-541-6180
Research Triangle Institute
P.O. Box 12914
Research Triangle Park, NC 27709

7.2.31 Silvar-Lisco

Description: Translator for Helix to VHDL; VHDL analyzer simulator

Contact: Silvar-Lisco 415-324-0700
1080 Marsh Road
Menlo Park, CA 94025

7.2.32 Vista Technologies

Description: Interactive VHDL tutorial and editor for Sun workstations

Contact: S. Swamy 708-706-9300
Vista Technologies
1100 Woodfield Rd., Suite 108
Schaumburg, IL 60173-5121221

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VHSIC Program Directors/Managers (1980 - 1990)

DOD	Army	AF	Navy	NASA
L. W. Sumney	C. G. Thornton	W. J. Edwards	N. Butler	H. Benz
E. D. Maynard, Jr.	P. Hudson	J. M. Blasingame	E. D. Cohen	
J. M. MacCallum	H. Borkan	R. M. Werner	P. Gariano, Jr.	
L. Cohn (DNA)	R. H. Sproat		J. P. Letellier	

Contributors to the VHSIC Final Report

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DoD	Report Contractors	Invited Contributors
S. E. Turnbach	H. A. Alperin (Vela Associates)	H. A. Cloud (U. of Maryland)
E. C. Urban	A. Brodzinsky (Vela Associates)	R. H. Estrada (IBM)
	D. I. Gordon (Vela Associates)	R. E. Harr (CAD)
	J. Hower (Eagle Research)	C. S. Meyer (Motorola)
	J. Recine (Analytics)	R. M. Rolfe (IDA)
		J. M. Schoen (MITRE)
		J. D. Stuelpnagel (Westinghouse)
		L. W. Sumney (SRC)
		L. R. Weisberg (Honeywell)

Contributors (continued)

Army	Navy	Air Force
A. Bramble	J. Holtkamp	W. Debany
K. Chan	P. Hunter	H. Dessault
C. F. Cook, Jr.	I. Lagnado	T. Glum
R. V. Garver	J. P. Letellier	M. Gorniak
J. Key	G. Perseghin	F. G. Hall
O. Layden	P. Reimel	R. Herndon
S. Lee	D. Rooney	J. Hines
A. V. Lukosevicius	T. Singleton	D. Lewallen
J. McGarrity	R. Woodruff	F. Long
P. McHugh	G. Woodward	P. Mano
R. Mitchell		D. Mays
V. Organic		C. Messenger
T. J. Peacher		D. Richards
L. Simon		W. Russell
T. Tippit		F. Schmandt
G. Tomlin		P. Speicher
S. Waldman		B. Spink
D. Woo		R. Stegmaier
L. L. Yung		J. Stauss
		N. Taylor

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APPENDIX A - REFERENCES

CHAPTER 2: HISTORY, STRUCTURE, AND POLICIES

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2.21 RCA VHSIC Submicrometer Program Definition (Phase 0') Final Technical Report, 08/01/83-02/28/84, Contract N00039-C-83-0639

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Section 3.4: Chip Descriptions

3.98 TRW VHSIC Phase 1 Interim Technical Report #2, 11/03/81-05/03/82, Contract N00039-81-C-0414, DTIC No. AD-B069-021

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CHAPTER 4: DEMONSTRATION OF VHSIC TECHNOLOGY

4.1 VHSIC Insertion into PJH, System Design Study, Final Report, Hughes Aircraft Company, Fullerton, CA, March 1985, Contract DAAB07-84-C-K588

4.2 VHSIC Insertion into EPLRS, Breadboard/Brassboard Development Model, Final Technical Report, Hughes Aircraft Company, Fullerton, CA, January 1990, Contract DAAB07-84-C-K588, CDRL-J002-001-ACN-1566

4.3 TRW VHSIC Phase 1 Interim Technical Report #6, for period 12/01/83 - 05/30/84, Contract N00039-81-C-0414, DTIC No. AD-B087-777

4.4 TRW VHSIC Phase 1 Interim Technical Report #7, for period 05/31/84 - 10/31/84, Contract N00039-81-C-0414, DTIC No. AD-B096-737

CHAPTER 5: VHSIC TECHNOLOGY INSERTION

5.1 Defense Science Board Report of the Task Force on the VHSIC Program: "Optimal Planning and Execution of DoD VLSI Activities", February 17, 1982, Office of the Undersecretary of Defense for Research and Engineering

5.2 VHSIC Modular Adaptive Signal Sorter (VMASS), Contract DAAB07-87-C-P040, General Electric Company, Technical Report DELEW-TR-82-065-2

5.3 VHSIC Threat Association Module (VTAM), Contract DAAL01-85-C-0648, ESL, Incorporated, Technical Report AMSEL-TR-85-C-0648 (CONFIDENTIAL)

5.4 LHX Mission Computer, ARTI Program, Final Technical Report for Period December 1983-July 1986, Bell/Helicopter Textron, Contract DAAJO2-86-C-0017, USAAVSCOM TR-86-D-16A/B

5.5 LHX Mission Computer, ARTI Program, Final Technical Report for Period December 1983-July 1986, United Technologies Corporation, Sikorsky Aircraft Division, Contract DAAJO2-86-C-0016, USAAVSCOM TR-86-D-20A/B

5.6 LHX Mission Computer, ARTI Program, Final Technical Report for Period December 1983-July 1986, IBM Federal Systems Division, USAAVSCOM TR-86-D-22A/B

5.7 LHX Mission Computer, ARTI Program, Final Technical Report for Period December 1983-July 1986, McDonnell Douglas Helicopter Company, Contract DAAJ02-86-C-0017, USAAVSCOM TR-86-D-13A/B

5.8 LHX Mission Computer, ARTI Program, Final Technical Report for Period December 1983-July 1986, Boeing-Vertol Company, Contract DAAJO2-86-C-0016, USAAVSCOM TR-86-D-21A/B

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5.12 Common-Module VHSIC Integrated System (CVIS), Final Report Westinghouse, Contract DAAA21-87-C-0281

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5.14 VHSIC Automatic Target Tracker for Line of Sight Missile Guidance Applications: Breadboard Demonstration Program, Texas Instruments, Contract DAAH01-83-C-A091, MICOM Report RE-85-32, July 1985

5.15 VHSIC Automatic Target Tracker Brassboard Demonstration Program Final Report, (in preparation), Texas Instruments, Contracts DAAH01-85-C-1161 and MDA972-88-C-0052

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5.19 VHSIC Application to Army Command and Control System (ACCS), Contract DAAB07-88-C-A006, TRW, Final Technical Report, April 7, 1989

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5.22 Generic VHSIC Spaceborne Computer, Phase II, Final Technical Report, Honeywell Contract F29601-87-C-0118, dated January 18, 1990

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CHAPTER 6: TECHNOLOGY TRANSFER

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6.3 Proceedings of 1983 VHSIC Conference, National Bureau of Standards, Gaithersburg, MD, September 19-21, 1983, DTIC Nos. AD-B076-951, 952, 953, 954, 955, 956

6.4 Proceedings of 1984 VHSIC Conference, Naval Surface Weapons Center, Silver Spring, MD, December 5-7, 1984, DTIC No. AD-B088-800

6.5 Proceedings of 1985 VHSIC Conference, Naval Surface Weapons Center, Silver Spring, MD, December 4-6, 1985, DTIC No. AD-B098-014

6.6 Proceedings of 1986 VHSIC Conference, Johns Hopkins University, Applied Physics Laboratory, Laurel, MD, December 8-10, 1986, DTIC No. AD-B108-700

6.7 Proceedings of 1987 VHSIC Conference, Johns Hopkins University, Applied Physics Laboratory, Laurel, MD, November 17-19, 1987, DTIC No. AD-B118-900

6.8 Proceedings of 1989 VHSIC Conference, Hyatt Orlando, Kissimmee, FL, November 6, 1989, DTIC NO. AD-B138-260

CHAPTER 7: VHSIC INDUSTRIAL BASE

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APPENDIX B - VHSIC CONTRACTS

Contractor	Contract Number	DoD Monitor	Appendix A Reference[1]
CHAPTER 2: HISTORY, STRUCTURE, AND POLICIES			
VHSIC Program Definition (Phase 0)			
General Electric	DAAK20-80-C-0255	Army LABCOM/ETDL	2.1
Honeywell	F33615-80-C-1124	AF WRDC/EL	2.2
Hughes	DAAK20-80-C-0256	Army LABCOM/ETDL	2.3
IBM	N00039-80-C-0284	Navy SPAWAR/VHSIC	2.4
Raytheon	F33615-79-C-1853	AF WRDC/EL	2.5
Rockwell	DAAK20-80-C-0257	Army LABCOM/ETDL	2.6
Texas Instruments	F33615-80-C-1123	AF WRDC/EL	2.7
TRW	N00039-80-C-0282	Navy SPAWAR/VHSIC	2.8
Westinghouse	N00039-80-C-0283	Navy SPAWAR/VHSIC	2.9
VHSIC Phase 1			
Honeywell	F33615-81-C-1527	AF WRDC/EL	2.11
Hughes	DAAK20-81-C-0383	Army LABCOM/ETDL	2.12
IBM	N00039-81-C-0416	Navy SPAWAR/VHSIC	2.13
Texas Instruments	DAAK20-81-C-0382	Army LABCOM/ETDL	2.14
TRW	N00039-81-C-0414	Navy SPAWAR/VHSIC	
Westinghouse	F33615-81-C-1532	AF WRDC/EL	2.15
VHSIC Submicron Program Definition (Phase 0')			
AT&T	DAAK20-83-C-0415	Army LABCOM/ETDL	2.16
Harris	F33615-83-C-1102	AF WRDC/EL	2.17
Honeywell	F33615-83-C-1103	AF WRDC/EL	2.18
Hughes	DAAK20-83-C-0414	Army LABCOM/ETDL	2.19
IBM	N00039-83-C-0638	Navy SPAWAR/VHSIC	2.20
RCA	N00039-83-C-0639	Navy SPAWAR/VHSIC	2.21
Texas Instruments	DAAK20-83-C-0413	Army LABCOM/ETDL	2.22
TRW	N00039-83-C-0640	Navy SPAWAR/VHSIC	2.23
Westinghouse	F33615-83-C-1104	AF WRDC/EL	2.24

Early VHSIC Phase 3 Contracts (Completed before 1986): These contracts are listed by subject at the end of this appendix. See pages 252 through 257.

[1] For those contracts on which final reports have been delivered to the Government.

CHAPTER 3: DEVELOPMENT TASKS

Section 3.1: Design

Interoperability Standards

VHSIC Interoperability Standards
IBM/Honeywell/TRW DAAK20-85-C-0376 Army LABCOM/ETDL 3.1

VHSIC Hardware Description Language (VHDL)

VHSIC Hardware Description Language (VHDL)
Intermetrics F33615-83-C-1003 AF WRDC/EL 3.2

VHDL Independent Validation and Verification (IV&V)
UTMC F33615-85-C-1760 AF WRDC/EL

Joint US/Canadian VHDL Rehost
Intermetrics/ F33615-87-C-1463 AF WRDC/EL
Bell Northern

Design Tools

VHDL Design Workbench
Gould/Vista Tech. DAAL01-85-C-0435 Army LABCOM/ETDL

ADAS Integration into VHDL Support Environment
RTI N00039-86-C-0057 Navy NRL/Code 5305 3.3, 3.4

VHDL Synthesis Tool
Honeywell F33615-85-C-1261 AF WRDC/EL 3.5

Enhanced AMSDS (Automated VHDL/Microcode Compiler Synthesis and Design System)
JRS Research N00039-87-C-0256 Navy NSWC/Code U-33

VHDL/MIXSIM Simulator
Unisys (Sperry) DAAL01-85-C-0436 Army LABCOM/ETDL

VHSIC Silicon Compiler
Research Triangle Institute, Silicon Compiler Systems, and E-Systems 3.10 - 3.11
F33615-85-C-1863 AF WRDC/EL

VHDL Annotation Language (VAL)
Stanford University F33615-86-C-1137 AF WRDC/EL 3.12 - 3.14

AMSDS JRS Research	N00039-86-C-0056	Navy NSWC/Code U-33	
Advanced Design AutoMation (ADAM) System U. So. California	N00039-87-C-0194	Navy NWC/Code 3649	
Hierarchical Design for Testability RTI	DAAL01-86-C-0039	Army LABCOM/ETDL	
Analog Design with VHDL Dartmouth Univ.	F33615-87-C-1423	AF WRDC/EL	3.30
Object Oriented Chip Design Using VHDL Rensselaer Polytech	F33615-87-C-1435	AF WRDC/EL	
Artificial Intelligence for VHSIC Systems Design RTI / OCTY, Inc.	DAAL01-86-C-0040	Army LABCOM/ETDL	3.31, 3.32
Engineering Information System (EIS) Honeywell et al	F33615-87-C-1401	AF WRDC/EL	3.33, 3.34

Section 3.2: Test and Life Cycle Support

Tester Independent Support Software System (TISSS) Harris Corporation	F30602-84-C-0168	AF RADC/RBR	
TISSS Independent Validation and Verification Digicomp	F30602-86-D-0025	AF RADC/RBR	
VHSIC Phase 1 Microcircuit Testers GenRad, Inc.	F33615-84-C-5076	AF RADC/RBRP	
Reliability Assessment of Gate Arrays GTE	F30602-86-C-0176	AF RADC/RBRA	3.37
Reliability Prediction Modeling ITTRI/Honeywell	F30602-86-C-0261	AF RADC/RBRA	3.38
VHSIC Generic Qualification Procedures GE/AT&T/Honeywell	F30602-86-C-0172	AF RADC/RBRA	
Maintenance Concepts for VHSIC Honeywell	F30602-86-C-0091	AF RADC/RBES	3.39

Section 3.3: Fabrication

VHSIC Submicron Technology (Phase 2)

Honeywell	F33615-84-C-1500	AF WRDC/EL	3.99
IBM	DAAK20-84-C-0376	Army LABCOM/ETDL	3.45
TRW/Motorola	N00039-84-C-0111	Navy SPAWAR/VHSIC	

Radiation Hardening

Radiation Hardened Bulk CMOS

Motorola	DNA001-84-C-0403	DNA/RAEE

Radiation Hardened CMOS/SOS

GE (RCA)	DNA001-84-C-0404	DNA/RAEE

Radiation Hardened Bulk CMOS

Westinghouse/National Semiconductor	DNA001-86-C-0134	DNA/RAEE

Radiation Hardened CMOS/SOS

Hughes Aircraft	DNA001-86-C-0407	DNA/RAEE

Radiation Hardened STL Bipolar

Texas Instruments	DNA001-86-C-0175	DNA/RAEE

Radiation Hardened 3D Bipolar

TRW	DNA001-86-C-0186	DNA/RAEE

Electromagnetic Effects Chip Hardening

Booz-Allen	DAAL02-86-C-0042	Army LABCOM/HDL

Enhancement of Materials for SOS Technology

Union Carbide Corp.	N00014-87-C-2019	Navy NRL/Code 6800

Lithography

Electron Beam Lithographic Equipment (VHSIC Phase 1)

Hughes/Perkin-Elmer	DAAK20-81-C-0384	Army LABCOM/ETDL	3.54

Electron Beam Lithography Components for Direct Writing of VHSICs (Phase 3)

Hughes Research	DAAK20-80-C-0262	Army LABCOM/ETDL	3.57

Software for Electron Beam Lithography (Phase 3)

TRW/GCA	DAAK20-80-C-0263	Army LABCOM/ETDL	3.58

Extension of X-ray Lithography Technology to VHSIC (Phase 3)			
Perkin-Elmer	DAAK20-80-C-0261	Army LABCOM/ETDL	3.59
X-ray Lithography Equipment			
Perkin-Elmer	DAAK20-84-C-0378	Army LABCOM/ETDL	
X-ray Lithography Exposure Station			
Spire Corporation	DAAL01-88-C-0807	Army LABCOM/ETDL	
Advanced Wafer Imaging System (AWIS)			
GCA Corporation	DAAL01-85-C-0460	Army LABCOM/ETDL	
Laser Pantography at Lawrence Livermore National Laboratory			
LLNL	FY1175-89-N9618	Navy NRL/Code 5305	
Advanced Resist Materials and Processes			
Hewlett Packard	DAAK20-80-C-0264	Army LABCOM/ETDL	3.76, 3.77

Packaging

Electronic Packaging for VHSIC (Phase 3)			
Honeywell	DAAK20-80-C-0267	Army LABCOM/ETDL	3.78
Improved Performance Package for VHSIC			
General Electric	F33615-80-C-1191	AF WRDC/MPO	3.79
Technical Guidelines for LSI Hybrid Microcircuits			
Raytheon	DAAK20-80-C-0302	Army LABCOM/ETDL	3.80
High Density - High Performance Hybrid Circuit Technolgy			
Raytheon	F33615-80-C-1193	AF WRDC/ELEL	3.81
HCC Compatible PWB Materials			
Westinghouse	F33615-82-C-5047	AF WRDC/EL	3.82
High Density Multilayer Package Devlopment			
Hughes Aircraft	DAAK20-83-C-0429	Army LABCOM/ETDL	3.83
High Density Multilayer Package Devlelopment			
Martin Marietta	DAAK20-84-C-0427	Army LABCOM/ETDL	3.84
High Density Multilayer Package Development			
Honeywell	DAAK20-84-C-0430	Army LABCOM/ETDL	3.85
VHSIC Low Dielectric Constant Printed Circuit Wiring Boards			
Hughes	F33615-84-C-1415	AF WRDC/EL	3.88

VHSIC Multichip Packaging			
Texas Instruments	DAAL01-85-C-0442	Army LABCOM/ETDL	3.89
VHSIC Multichip Microcircuit Manufacturing Technology			
Teledyne	N66001-85-C-0218	Navy NOSC/Code 551	3.90
VHSIC Tape Automated Bonding Processes			
Honeywell	DAAL01-85-C-0441	Army WRDC/ETDL	3.91
Manufacturing Technology for Advanced Data/Signal Processing			
Martin Marietta	F33615-85-C-5065	AF WRDC/EL	
First Level Packaging and Interconects			
General Ceramics	DAAL01-86-C-0001	Army LABCOM/ETDL	
Tape (Decal) Intereonneet Technolgy			
IBM	N66001-85-C-0021	Navy NOSC/Code 551	
Third Level Interconnects for VHSIC			
Sperry	N66001-86-C-0150	Navy NOSC/Code 551	
Nondestructive Evaluation of Metallized Tape Bonds Formed by Tape Automated Bonding			
Sonoscan	F30602-86-C-0050	AF RADC/RBRE	3.92

CHAPTER 4: DEMONSTRATION OF VHSIC TECHNOLOGY

VHSIC Insertion into PJH/EPLRS			
Hughes Aircraft	DAAB07-84-C-K588 DAAB07-82-C-J096	Army CECOM /C^3 Systems Center	4.1, 4.2

CHAPTER 5: VHSIC TECHNOLOGY INSERTION

Army System Insertion Projects

MEDFLI-VMASS			
General Electric	DAAK20-87-C-P040	Army CECOM /EW Center/RSTA	5.2
MEDFLI-VTAM			
ESL Corporation	DAAK20-85-C-0648	Army CECOM /EW Center/RSTA	5.3
LHX Mission Computer			
Boeing/Sikorsky	DAAJ02-86-C-0016	Army AVSCOM	5.4 - 5.8
McAir/Bell	DAAJ02-86-C-0017	/SFAE-LH-TM	

Enhanced PLRS User Unit (EPUU)			
Hughes Aircraft	DAAB07-82-C-J097	Army CECOM	5.9 - 5.11
	DAAB07-84-C-K588	/C^3 Systems Center	
Firefighter Radars			
Hughes Aircraft	DAAK20-84-C-0433	Army SFAE-IEW-RD-EL	
Common-Module VHSIC Integrated System (CVIS)			
Westinghouse	DAAA21-87-C-0281	Army ARDEC	5.12
General Dynamics	DAAA21-87-C-0287	/SMCAR-FSF-BD	5.13
TOW VHSIC Automatic Target Tracker			
Texas Instruments	DAAH01-85-C-1161	Army MICOM /AMSMI-RD-AS-OG	5.14
	MDA972-88-C-0052	DARPA	5.15
Hellfire PA/VHSIC Chip Integration			
McDonnell Douglas	DAAH01-85-C-A104	Army MICOM /AMSMI-RD-AS-IR	5.16
Hellfire IIR Seeker			
Ford Aerospace/Comm	DAAH01-86-C-A138	/AMSMI-RD-AS-IR	5.17
Texas Instruments	DAAH01-85-C-A118	/AMSMI-RD-AS-IR	5.18
Multirole Survivable Radar (MRSR)			
Raytheon	DAAH01-85-C-A034	Army MICOM	
Westinghouse	DAAH02-85-C-A033	/AMSMI-RD-AS-RA	
Army Command and Control System			
TRW	DAAB07-88-C-A006	Army CECOM /C^3 Systems Center	5.19

Navy System Insertion Projects

AN/UYS-2 Enhanced Modular Signal Processor (EMSP)			
AT&T/Honeywell	N00024-81-C-7318	Navy NAVSEA-PMS412	5.20 - 5.21
JRS, Inc.	N00039-87-C-0256		
To be determined	N00024-90-R-5214 (RFP)		
AN/AYK-14 VHSIC Processor Module (VPM)			
Control Data Corp.	N00019-86-C-0002	Navy NAVAIR-PMA209	
Advanced ASW Receiver			
To be determined	Marked for FY-92	Navy NAVAIR-933-A	
HF/EHF Communications: VHSIC Terminal Brassboard (VTB)			
TRW	N00039-81-C-0414	Navy SPAWAR	

VHSIC Communications Processor (VCP)			
TRW	N00019-82-C-0330	Navy NAVAIR-933-K	
AN/SRS-1 Combat Direction Finder			
Sanders Associates	(Classified)	Navy SPAWAR-PMW143-2	
MK-50 Torpedo			
Honeywell	N00024-83-C-6254	Navy NAVSEA-PMS406	
Air Force System Insertion Projects			
Generic VHSIC Spaceborne Computer (GVSC)			
IBM	F29601-87-C-0006	AF STC/SWL	
Honeywell	F29601-87-C-0118	AF STC/SWL	5.22
Advanced Spacecraft Computer Module (ASCM)			
(Various)		AF STC/SWL	
Cruise Missile Advanced Guidance (CMAG)			
General Dynamics	F33615-84-C-1460	AF WRDC/AL	
Honeywell	F33615-84-C-1500	AF WRDC/AL	
AN/APG-68 Radar Advanced Programmable Signal Processor (APSP)			
Westinghouse	F33657-81-C-0115	AF ASD/F-16 SPO	
MILSTAR Terminal/Modem Processor			
TRW	N00039-81-C-0414	AF RADC/DCCR	
F-15 VHSIC Central Computer (VCC)			
McAir/IBM	F33657-84-C-2228 (P01E7E358)	AF ASD/F-15 SPO	
Radiation Hard 32-Bit Processor (RH32)			
Phase 1			
TRW/McAir	F30602-88-C-0058	AF RADC/RBRA	
Unisys/UTMC	F30602-88-C-0059		
Honeywell/Westinghouse	F30602-88-C-0060		
IBM	F30602-88-C-0061		
Phase 2			
TRW	F30602-88-C-0058		
Honeywell	F30602-88-C-0060		
VHSIC Avionics Modular Processor (VAMP)			
Westinghouse	F33615-84-C-1465	AF WRDC/AAAS	

SRAM-II Missile Guidance Computer

Boeing /Texas Instruments	F33657-86-C-0012	AF ASD/YGEA

Advanced Tactical Fighter (ATF) Processing

(To be determined)	(Award in mid-1991)	AF ASD/YFEA

Common Signal Processor (CSP)

IBM	F33615-84-C-1470	AF WRDC/AAAT

E-3A Signal Processor

Westinghouse	F30602-86-C-0221	AF ESD

Advanced Onboard Signal Processor (AOSP) Radiation Hardened Vector Processor (RHVP)

TRW	F30602-86-C-0150	AF RADC/DCCR
IBM	F30602-86-C-0151	AF RADC/DCCR

AN/ALQ-131 Electronic Countermeasures Pod

TRW	F09603-85-C-0867	AF ALC/Warner Robins AFB

Logistics Retrofit Engineering

VHSIC TTL Gate Array

Honeywell	F04606-86-C-0913	AF SM-ALC

Logistics Retrofit Engineering: 1750A Electronic Module

General Dynamics	F04606-87-D-0034	AF SL-ALC

Projects Involving Insertion of VHDL

AN/BSY-2 Submarine Program

General Electric	N00025-88-C-6150	Navy NAVSEA PMS-418

Single Channel Ground and Airborne Radio Systems (SINCGARS)

General Dynamics	DAAB07-89-D-T055	Army LABCOM ETDL

TD-660 Communications Multiplexer

AT&T	DAAB07-87-C-R037	Army CECOM	5.23

APPENDIX B / VHSIC CONTRACTS

EARLY PHASE 3 PROJECTS (Completed prior to 1986)

Contractor	Contract Number	Subject	DTIC Number
1. Architectural Studies			
Arizona State U.	N00039-80-C-0511	Signal Processing Algorithms On Chips	AD-B072-124
Boeing	F33615-80-C-1196	Storage/Logic Arrays	AD-B954-381L
Carnegie Mellon	N00039-80-C-0640	A Hierarchical Design Approach For VHSIC	AD-B071-076
Lockheed	N00019-80-C-0610	Study Of VHSIC Applications In Naval Patrol Aircraft	AD-8074-271/2
Naval Air Development Ctr	In-House	Generalized Computer System Simulator For VHSIC	
Research Triangle Institute	DAAK20-80-C-0275	Signal Processor Architecture Performance Evaluation Tool	AD-B102-719L
Sanders Associates	F33615-80-C-1192	Memory Processor Study	AD-B068-519
Stanford Resch Institute	F30602-80-C-0303	Fault Tolerant Architecture For VHSIC	AD-B065-4998
Stanford Resch Institute	N00039-80-C-0571	Assignment Algorithms For Control Of VHSIC Chips	AD-B067-642
Texas Instrum.	DAAK20-80-C-0276	Data Flow Architecture	AD-B071-864/5-7

TRW	F33615-80-C-1202	Software Architecture Study	AD-B067-869
Univ. of Southern Calif.	N00039-80-C-0641	Architectures For Radar Signal Processing	

2. Lithography

American Science and Engineering	N00019-80-C-0568	Concentrating Collimating Illumination For X-Ray Lithography	AD-B073-623
AVCO Research	F19628-80-C-0176	High Intensity Pulsed Plasma X-Ray Source	AD-B066-469L
EBC Corp.	N00019-80-C-0618	Ultra High Speed Submicron Direct Write E-Beam System	
Hewlett Packard	DAAK20-80-C-0264	Advanced Resist Materials And Processes	
Hughes Research	N00019-80-C-0616	Improved Resists For Electron-Beam Lithography	
Hughes Research	DAAK20-80-C-0262	E-Beam Lithography Componenets For Directly Writing VHSIC	AD-B094-565L
Naval Research Laboratory	IN-HOUSE	X-Ray And E-Beam Effects On MOS Devices	
Perkin Elmer	DAAK20-80-C-0261	Proposal To Extend Microlithography Technology	AD-B074-215
Stanford Resch Institute	F33615-80-C-1194	Intense Plasma X-Ray Source For Submicron Lithography	

TRW	DAAK20-80-C-0263	Electron Beam System Software	AD-B078-420/421
Varian Associates	F19628-80-C-0173	Develop Direct Write e-beam Lithography Components	

3. Processing

AVCO RESEARCH	N00039-80-C-0589	CORONAPHORESIS FOR GAS PURIFICATION	AD-B077-419
CORNELL U.	F33615-80-C-1197	IMPROVE CRYSTAL QUALITY OF SI ON INSULATED SUBSTRATES	
HUGHES RESEARCH	N00019-80-C-0616	LOW-TEMPERATURE SILICON EPITAXY	
HUGHES RESEARCH	DAAK20-80-C-0268	LOW TEMPERATURE PHOTOCHEMICAL PROCESSING FOR VHSIC APPLICATIONS	AD-B085-497L
HUGHES RESEARCH	DAAK20-80-C-0269	LASER ANNEALING	
HUGHES RESEARCH	DAAK20-80-C-0270	ELECTRON BEAM PROCESSING	
PERKIN-ELMER	DAAK20-80-C-0265	EXTEND MICROLITHOGRAPHY TECHNOLOGY THROUCH PLASMA ETCHING	AD-B085-912

4. Design Automation

CAL INST TECH	N00014-79-C-0924	DEMONSTRATE USE OF VLSI DESIGN RULES STANDARDS & INTERFACES	AD-B077-602/3/4
GE	F33615-80-C-1083	CAD FOR TESTABLE LSI	AD-B095-571L
SANDIA LAB	P.O. 81-19638/39	CRITICAL VHSIC DESIGN TOOLS	
TRW	F33615-80-C-1198	TRANSPORTABILITY OF CAD DATA	AD-B067-139

UNIV. SOUTHERN CALIFORNIA	DAAK20-80-C-0278	DESIGN AUTOMATION	AD-B075-616

5. Materials and Characterization

CORNELL U.	F33615-80-C-1197	ANALYTICAL METHODS FOR DETECTING SUBSTRATE DEFECTS	
HUGHES AIRCRAFT	DAAK20-80-C-0273	REFRACTORY METAL FOR INTERCONNECTION	AD-B082-339
WESTINGHOUSE	DAAK20-80-C-0271	MOBILITY/DRIFT VELOCITY MEASUREMENT IN INVERSION LAYERS	
WESTINGHOUSE	F33615-79-C-1946	IMPROVED SOS FOR VHSIC	AD-B078-171
WESTINGHOUSE	N00039-80-C-0662	LOW DEFECT DENSITY SILICON SUBSTRATES FOR NMOS	AD-B102-419L

6. Device Technology

Cornell Univ.	F33615-80-C-1197	Simple Submicron Device Models For Circuit Simulation	AD-B958-232L
Cornell Univ.	F33615-80-C-1197	Submicron Devices: Exact Simulation and Simple Models	
GE	DAAK20-80-C-0272	Development FET Silicon On Sapphire For IC Gates	AD-B068-304
Hughes Aircraft	N00019-80-C-0616	Static Induction Transistor (SIT) Logic Technology	

Rockwell	DAAK20-80-C-0274	Low Resistivity Gates For CMOS ICs	AD-B066-109L
The Analytical Science Corp.	N00039-80-C-0086	Industry Impact Of VHSIC Program: A Preliminary Analysis	
Westinghouse	F33615-80-C-1199	Electronically Alterable ROM For VHSIC	AD-B080-958

7. Packaging

GE	F33615-80-C-1191	Improved Performance Package For VHSIC	AD-B080-965
Honeywell	DAAK20-80-C-0267	Electronic Packaging For VHSIC	AD-B070-866
Raytheon	F33615-80-C-1193	High Density, High Performance Hybrid Circuit Technology	AD-B069-485
Westinghouse	F33615-82-C-5047	HCC-Compatible PWB Materials	

8. Testing and Reliability

Hughes Aircraft	DAAK20-80-C-0277	Failure Management Design System	AD-B074-223
Hughes Aircraft	F30602-80-C-0321	Electron Beam Circuit Tester	AD-B073-808
Hughes Aircraft	N00039-80-C-0625	Acoustic Microscopy For Inspection Of VHSIC Chips	
University of Illinois	N00039-80-C-0556	Reliable, High Performance VHSIC System	AD-B089-167
National Bureau Of Standards	N00019-79-IP-990003	Measurement Technology For VHSIC	

Prospective Computer Analysts	F30602-84-C-0167	Tester Independent Support Software System	
Research Triangle Institute	N00039-80-C-0648	Identify And Assess On-Chip Self Test And Repair Concepts	AD-B087-155
Rockwell	F33615-82-C-5110	Test Structure Development	
Stanford Univ.	DAAK20-80-C-0266	Testing VHSIC Devices	
Texas Instrum.	F30602-81-C-0032	Develop Test Technology For VHSIC	
University of Southern Cal.	N00039-80-C-0641	Design For Testability And Reliability	AD-B086-080
Aerospace/JPL	F4071-83-C-0084	VHSIC Yield Enhancement Test Structure	

APPENDIX C - GLOSSARY OF ACRONYMS AND TECHNICAL TERMS

3D	Triple Diffused (bipolar process)
4PM	Four Port Memory
A-6F	Navy Attack Aircraft
AASP	Advanced Anti-Radiation Missile Signal Processor
ABBM	Acoustic Beamformer Brassboard Module
ACCS	Army Command and Control System
ACE	Array Computing Element
ACLS	Automatic Carrier Landing System
ACS	Array Controller/Sequencer
Ada	DoD High Order Programming Language
ADAM	Advanced Design Automation System
ADAS	Architectural Design and Assessment System
ADB	Advanced Digital Bipolar (Honeywell technology)
AEBLE	Advanced Electron Beam Lithography Equipment
AEGIS	Advanced Electronic Guidance and Intercept System
AFIT	Air Force Institute of Technology
AG	Address Generator
AI	Artificial Intelligence
AJ	Anti-Jam or Jam Resistant
ALFS	Advanced Low Frequency Sonar
ALU	Arithmetic Logic Unit
ALWT	Advanced Lightweight Torpedo (MK-50)
AMAC	Add Multiply Accumulate
AMGS	Automatic Microcode Generation System
AMRAAM	Advanced Medium Range Air-to-Air Missile
AMSDS	Automated Microcode Compiler Synthesis & Design System
AMTE	Automated Microcircuit Test Equipment
AN/SRS-1	Navy Combat Direction Finder
AN/AYK-14(V)	Navy Embedded Standard Airborne Computer
AN/APG-65	Navy Coherent Multimode Pulse Doppler Radar
AN/UYS-1,-2	Navy Standard Signal Processors
AN/SLQ-32	Navy Electonic Warfare System
AN/TPQ-36,-37	Artillery Locating Radars (Firefinder)
AN/ALQ-131	Airborne Pod-Mounted Electronic Countermeasure
AN/APG-68	Airborne Fire Control Radar
AN/BQQ-5	Sonar System
AN/ALR-56C,-74	Air Force Radars
AOSP	Advanced Onboard Signal Processor
AP	Arithmetic Processor
APC	Array Processor Controller
APE	Asynchronous Processing Element
APIO	Array Processor Input/Output
APSP	Advanced Programmable Signal Processor
APU	Arithmetic Pipeline Unit; Array Processing Unit
ARM	Anti-Radiation Missile
ARSR	Air Route Surveillance Radar

ASCM ..... Advanced Spaceborne Computer Module
ASIC ..... Application Specific Integrated Circuit
ASP ..... Advanced Signal Processor
ASW ..... Antisubmarine Warfare
ATA ..... Advanced Tactical Aircraft
ATE ..... Automatic Test Equipment
ATF ..... Advanced Tactical Fighter
ATH ..... Advanced Technology Helicopter
ATIM ..... Advanced Technolgy Insertion Module
ATPG ..... Automatic Test Pattern Generation
ATR ..... Automatic (or Aided) Target Recognition
AU ..... Arithmetic Unit
AV-8B ..... Marine Vertical Takeoff and Landing (VTOL) Aircraft
AWACS ..... Airborne Warning and Control System
AWIS ..... Advanced Wafer Imaging System
BEOL ..... Back End of Line
BiCMOS ..... Bipolar and CMOS combined on a chip
BILBO ..... Built-in Logic Block Observer
BIST ..... Built-In Self Test
BIT ..... Built-In Test
BIU ..... Bus Interface Unit
BOPS ..... Billion Operations Per Second
BPSG ..... Borophosphosilicate Glass
Brassboard ..... Field Demonstrable Electronic Model
Breadboard ..... Laboratory Demonstrable Electronic Model
BSQ ..... Bias Sputtered Quartz
BSTS ..... Boost Surveillance and Tracking System
C3I ..... Command, Control, Communications, and Intelligence
C4 ..... Controlled Collapsible Chip Connection (IBM)
CAD ..... Computer Aided Design
CALMA ..... Graphics design system marketed by CALMA Corporation
CALS ..... Computer Aided Acquisition and Logistics System
CAM ..... Computer-Assisted Manufacturing
CAM ..... Content Addressable Memory
CAP-32 ..... 32-Bit Common Avionics Processor
CAVP ..... Complex Arithmetic Vector Processor
CC-BUS ..... Chip to Chip Bus
CCS/MK 2 ..... Command Control Software for BSY-1 Submarine
CDP ..... Configurable Data Path (chip)
CDR ..... Critical Design Review
CDRL ..... Contract Data Requirements List
CFI ..... CAD Framework Initiative
CGA ..... Configurable Gate Array
CMAC ..... Complex Multiply Accumulate
CMAG ..... Cruise Missile Advanced Guidance
CML ..... Current Mode Logic
CMOS ..... Complementary Metal-Oxide Semiconductor

CPM ..... Control Processor Module
CPU ..... Central Processing Unit
CPUAX ..... Central Processing Unit Arithmetic Extended
CS ..... Convolver Superchip (TRW)
CSP ..... Common Signal Processor
CSR ..... Configurable Static RAM
CTTC ..... Circuit Technology Test Chip (Honeywell)
CVD ..... Chemical Vapor Deposition
CVIS ..... Common Module VHSIC Integrated System
C-E ..... Collector-Emitter
DAC ..... Digital-to-Analog Converter
DAIS ..... Digital Avionics Information System (1750A Computer Instructions Mix)
DASS ..... (IEEE) Design Automation Standards Subcommittee
DAST ..... Design, Architecture, Software, and Test
DEM/VAL ..... Demonstration/Validation
DESC ..... Defense Electronics Supply Center
DF ..... Direction Finder
DFT ..... Design for Test
DIFAR ..... Directional Frequency Analysis and Recording
DIP ..... Double In-line Package
DIU ..... Device Interface Unit
DLM ..... Design Library Manager
DNA ..... Defense Nuclear Agency
DOD ..... Department of Defense
DPU ..... Data Processor Unit
DRAM ..... Dynamic RAM
DRC ..... Design Rule Check
DSPE ..... Double Solid Phase Epitaxy
DTIC ..... Defense Technical Information Center
DXMD ..... Diagnostic Maintenance Device
E-BEAM ..... Electron-Beam
E-2C ..... Navy Airborne Warning and Control System (AWACS)
E-3A ..... Sentry Air Force AWACS
EA-6B ..... Navy EW Aircraft
EAR ..... Export Administration Regulations
EAU ..... Extended Arithmetic Unit
EAUM ..... Extended Arithmetic Unit Multiplier
EBL ..... Electron Beam Lithographic (Machine)
ECCM ..... Electronic Counter Countermeasure(s)
ECL ..... Emitter Coupled Logic
ECM ..... Electronic Countermeasure(s)
EDIF ..... Electonic Design Information Format
EEPROM ..... Electrically Erasable Programmable Read-Only Memory
EHF ..... Extremely High Frequency
EIA ..... Electronics Industries Association
EIS ..... Engineering Information System
ELINT ..... Electronic Intelligence

EMC ..... Electromagnetic Compatibility
EME ..... Electromagnetic Effects
EMI ..... Electromagnetic Interference
EMP ..... Electromagnetic Pulse; Electromagnetic Potential
EMSP ..... Enhanced Modular Signal Processor
EO ..... Electro-Optic
EOSP ..... Electro-Optic Signal Processor
EOSPC ..... Electro-Optic Signal Processor Controller
EP-3E ..... Electronic Surveillance Aircraft
EPLRS ..... Enhanced Position Location Reporting System
EPUU ..... Enhanced PLRS User Unit
ERC ..... Electrical Rule Check
ESD ..... Electrostatic Discharge
ESM ..... Electronic Support Measure
ETM-Bus ..... Element Test and Maintenance Bus
EW ..... Electronic Warfare
F-14D ..... Navy Fighter Aircraft
F/A-18 ..... Navy Fighter Attack Aircraft
FAR ..... Federal Acquisition Regulation
FEOL ..... Front End of Line
FEP ..... FLTSAT EHF Package
FET ..... Field Effect Transistor
FF ..... Flip-flop
FFT ..... Fast Fourier Transform
FIPS ..... Federal Information Processing Standard
FIR ..... Finite Impulse Response
Firefinder ..... Artillery Locating Radars AN/TPQ-36,-37
FLIR ..... Forward Looking Infrared
FLTSAT ..... Fleet Satellite
FOG-M ..... Fiber Optic Guided Missile
FPAP ..... Floating Point Arithmetic Processor
FPMAK ..... Floating Point Multiply/Accumulate Kernel
FSD ..... Full Scale Development
FSED ..... Full Scale Engineering Development
FTR ..... Functional Throughput Rate
GBU ..... General Buffer Unit
GFE ..... Government Furnished Equipment
GOMAC ..... Government Microelectronics Applications Conference
GPC ..... General Purpose Computer
GPS ..... Global Positioning System
GVSC ..... Generic VHSIC Spaceborne Computer
HBX ..... High Brightness X-ray
HCC ..... Hermetic Chip Carrier
HDL ..... Hardware Description Language
Hellfire ..... Anti-Armor Weapon System
HF ..... High Frequency
HFM ..... Heavy Forces Modernization (Army program)

HOL ..... Higher Order Language
HPM ..... High Power Microwaves
HSL ..... Hierarchical System Language
HWSI ..... Hybrid Wafer Scale Integration
I/O ..... Input/Output
IAC ..... Information Analysis Center
IAPU ..... Image Array Processing Unit
IC ..... Integrated Circuit
ICNIA ..... Integrated Communication, Navigation, Identification Avionics
IDAS ..... Integrated Design Automation System
IEEE ..... Institute of Electrical and Electronics Engineers
IFF ..... Indentification Friend or Foe
IIR ..... Imaging Infrared
INEWS ..... Integrated Navigation & Electronic Warfare System
IPS ..... Instructions Per Second
IRAD ..... Independent Research and Development
IRHVTA ..... Infra-Red (seeker for) High Value Target Acquisition
IRST ..... Infrared Search and Track
ISA ..... Instruction Set Architecture; Imaging Sensor Autoprocessor
ISC ..... Input Signal Conditioner
ITAR ..... International Traffic in Arms Regulations
IV&V ..... Independent Validation and Verification
IVTM ..... Interconnect Verification Test Module
IVV ..... Independent Validation and Verification
JEDEC ..... Joint Electronic Devices Engineering Council
JEOL ..... Japanese Made Electron Beam Lithography Machine
JIAWG ..... Joint Integrated Avionics Working Group
JTAG ..... Joint Test Action Group
JTIDS ..... Joint Tactical Information Distribution System
K, k ..... Kilo- (10^3)
LAMPS ..... Light Airborne Multipurpose System
LCC ..... Leaded Chip Carrier
LCCC ..... Leadless Ceramic Chip Carrier
LEAP ..... A Strategic Defense Initiative Program
LET ..... Linear Energy Transfer
LFP ..... Linear Format Package
LHX ..... Light Helicopter Experimental
LLCC ..... Leadless Chip Carrier
LMT ..... Logic Macrocell Test
LOFAR ..... Low Frequency Analysis and Recording
Longbow ..... Uses Signal Processor for Army Apache-64 Helicopter
LP ..... Laser Pantography
LPCVD ..... Low Pressure Chemical Vapor Deposition
LRE ..... Logistics Retrofit Engineering Program
LRM ..... Line Replaceable Module
LSI ..... Large Scale Integration
LSSD ..... Level Sensitive Scan Design

LU ..... Latchup
M ..... Mega- (10^6)
m ..... Milli- (10^{-3})
M2F2 ..... Multimode Fire and Forget Missile
MAC ..... Multiplier/Accumulator
MADS ..... Maintenance And Diagnostics System
MASA ..... (Air Force) Modular Avionics Support Architecture
MASS ..... Modular Adaptive Signal Sorter
Maverick ..... An Air Force Air-to-Air Missile
MC ..... Micro-Controller
MCC ..... Multichannel Correlator
MCC ..... Multiple Chip Carrier
MCP ..... Multichip Package
MCTL ..... Military Critical Technologies List
MEBES ..... E-Beam Exposure System for Mask Making
MEDFLI ..... Miniaturized Electronic Direction Finding Location Indicator
MeV ..... Million Electron Volts
MFLOPS ..... Million Floating-Point Operations per Second
MFSP ..... Macro Function Signal Processsor
MGC ..... Missile Guidance Computer
Micrometer ..... Same as Micron: = 10^{-6} Meter
Micron ..... Same as Micrometer: = 10^{-6} Meter
MIL-STD ..... Military Standard
Milstar ..... EHF Satellite Communication System
MILVAX ..... Military version of the DEC VAX 32-bit commercial computer
MIPS ..... Million Instructions Per Second
MK-50 ..... Advanced Light Weight Torpedo (ALWT)
MMG ..... Multimode Guidance
MMS ..... Mass Memory Superchip (TRW)
MMU ..... Memory Manager Unit
MMW ..... Millimeter Wave
MOPS ..... Million Operations Per Second
MOS ..... Metal-Oxide Semiconducter
MOSFET ..... Metal-Oxide Semiconductor Field Effect Transistor
MPS ..... Multipath Switch
Mrad ..... Megarad = 10^6 rads
MRSR ..... Multirole Survivable Radar
MS ..... Matrix Switch
ms ..... Millisecond = 10^{-3} second
MSI ..... Medium Scale Integration
MT ..... Maufacturing Technology
MTBF ..... Mean Time Between Failure; Mean Time Between Fault
MTTR ..... Mean Time to Repair
NMOS ..... N-Channel Metal-Oxide Semiconductor
NPN, npn ..... Transistor layer arrangement: n-, p-, and n-type
ns ..... Nanosecond = 10^{-9} second
OPS ..... Operations per Second

OSD ..... Office of the Secretary of Defense
OUSDA ..... Office of the Under Secretary of Defense for Acquisition
OUSDRE ..... Office of the Under Secretary of Defense for Research and Engineering
P3-C ..... Navy ASW Aircraft
P3 ..... Naval Patrol Aircraft
P3I ..... Preplanned Product Improvement
Patriot ..... An Army Ground Based Radar
PAU ..... Pipeline Arithmetic Unit
Pave Sprinter ..... Modular Avionics Demonstration Program
PE ..... Processing Element
PECVD ..... Plasma Enhanced Chemical Vapor Deposition
PGA ..... Pin Grid Array
PI-BUS ..... Parallel Interface Bus (designed during VHSIC-2)
PISCES ..... A Device Modeling/Simulation Code
PJH ..... PLRS/JTIDS Hybrid
PLA ..... Programmable Logic Array
PLAU ..... Pipeline Arithmetic Unit
PLRS ..... Position Location Reporting System
PN ..... Pseudo Noise
PNP, pnp ..... Transistor layer arrangement: p-, n-, and p-type
POC ..... Proof of Concept
Polysilicide ..... Polycrystalline Silicon-Metal Compound (e. g. $MoSi_2$)
PPP ..... Parallel Pipeline Processor
PRDA ..... Project Research & Development Announcement
Prism ..... A classified military program
PROM ..... Programmable Read-Only Memory
PSG ..... Phosphosilicate Glass
PSP ..... Programmable Signal Processor
PWB ..... Printed Wiring Board
QCI ..... Qualification Conformance Inspection
QML ..... Qualified Manufacturers List
QPL ..... Qualified Products List
RALU ..... Register Arithmetic Logic Unit
RAM ..... Random Access Memory
RFI ..... Radio Frequency Interference
RFP ..... Request for Proposals
RHVP ..... Radiation Hard Vector Processor
RH-32 ..... Radiation Hard 32-bit Processor
RIE ..... Reactive Ion Etch
RISC ..... Reduced Instruction Set Computer
RISCAE ..... Reduced Instruction Set Computer Ada Environment
ROM ..... Read Only Memory
ROX ..... Recessed Oxide
RPV ..... Remotely Piloted Vehicle
RTL ..... Register Transfer Language
RWR ..... Radar Warning Receiver
S3 ..... Naval Early Warning Aircraft (including radar system)

SABIR ..... Space Based Interceptor program
SAFE ..... Self Aligned Field Edge
SCC ..... Single Channel Correlator
SCM ..... Single-Chip Module (used interchangeably with SCP)
SCP ..... Single-Chip Package (used interchangeably with SCM)
SDI ..... Strategic Defense Initiative
SDS ..... Strategic Defense System
SEC ..... Standard Evaluation Circuit
SECDED ..... Single Error Correct, Double Error Detect
SEM ..... Standard Electronic Module
SEMATECH ..... An Industrial Semiconductor Development Consortium
SEP ..... Standard Extremely High Frequency (EHF) Package
SEU ..... Speech Enhancement Unit
SEU ..... Single-Event Upset
SGEMP ..... System Generated Electromagnetic Pulse
SH-60B ..... (Sikorsky) Helicopter Aircraft
SI Chip ..... System Interface Chip (BIU + FIU)
SiCB ..... Silicon Circuit Board
SIGINT ..... Signal Intelligence
SINCGARS ..... Single Channel Ground and Airborne Radio System
SLAM ..... Scanning Laser Acoustic Microscope
SOI ..... Silicon on Insulator
SOS ..... Silicon on Sapphire
SOW ..... Statement of Work
SP ..... Signal Processor
SPARC ..... Scalable Processor Architecture
SPE ..... Signal Processing Element
SPEAR ..... Solid Phase Epitaxy and Regrowth
SPICE ..... Public Domain Integrated Circuit Simulation Program
SPS ..... Systolic Processing Superchip (TRW)
SQC/SPC ..... Statistical Quality & Process Control
SRAM ..... Static Random Access Memory
SRAM ..... Short Range Attack Missile
SSI ..... Small Scale Integration
STACK ..... Standard Computer Kompenten
STCP ..... Self Test Configuration Processor
STL ..... Schottky Transistor Logic
STS ..... Signal Tracking Subsystem
SubACS ..... Submarine Advanced Combat System
SWAP ..... Size, Weight, and Power
SYSCLK ..... System Clock
TAB ..... Tape Automated Bonding
TAM ..... Threat Association Module
TD ..... Total Dose
TDL ..... Test Description Language
TEA ..... Test Engineer's Assistant
TISSS ..... Tester Independent Support Software System

TIU ..... Test Interface Unit (Honeywell)
TM-BUS ..... Test and Maintenance Bus
TOW ..... Tube Launched, Optically Tracked, Wire Guided Missile
TREE ..... Transient Radiation Effects in Electronics
TSL ..... Test Specification Language
TTL ..... Transistor-Transistor Logic
TVL ..... TISSS Vector Language
VAG ..... Vector Address Generator
VAL ..... VHDL Annotation Language
VALU ..... Vector Arithmetic/Logic Unit
VAMP ..... VHSIC Avionics Modular Processor
VAX ..... DEC 32-Bit Commercial Computer
VBIU ..... VHSIC Bus Interface Unit
VCB ..... VHSIC Communications Brassboard
VCC ..... VHSIC Central Computer (for F-15)
VCP ..... VHSIC Communications Processor
VDEG ..... VHDL Design Exchange Group
VHDL ..... VHSIC Hardware Description Language
VHSIC ..... Very High Speed Integrated Circuits
VID ..... VHSIC Insertion Demonstration for the EMSP
VIFASG ..... VHDL Intermediate Form, Analysis, and Standardization Group
VLM ..... Very Large Memory
VLSI ..... Very Large Scale Integration
VMASS ..... VHSIC Modular Adaptive Signal Sorter
VMDV ..... VHDL Model Development and Validation
VME Bus ..... Standard Digital Equipment Corporation Bus
VPC ..... Vector Product Calculator
VPM ..... VHSIC Processor Module
VPO ..... (DoD) VHSIC Program Office
VPSP ..... VHSIC Programmable Signal Processor
VSC ..... VHSIC Signal Conditioner
VTAM ..... VHSIC Threat Association Module
VTB ..... VHSIC Terminal Brassboard
VTCA ..... VHSIC Transmit Control Assembly
WAM ..... Window Addressable Memory
WAVES ..... Waveform and Vector Exchange Specification
WCL ..... Wireless Command Link
WNC ..... Weapons Navigation Computer
WSI ..... Wafer Scale Integration
XSAR ..... X-ray Step and Repeat Lithographic Machine
YAG ..... Yttrium Aluminum Garnet
YE ..... Yield Enhancement
YVR ..... Yield Verification Run