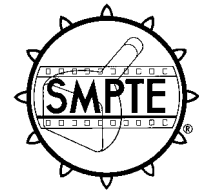


## for Television — 10-Bit 4:2:2 Component and $4f_{sc}$ Composite Digital Signals — Serial Digital Interface



### 1 Scope

This standard describes a serial digital interface for 525/60 and 625/50 digital television equipment operating with either 4:2:2 component signals or  $4f_{sc}$  composite digital signals. This standard has application in the television studio over lengths of coaxial cable where the signal loss does not exceed an amount specified by the receiver manufacturer. Typical loss amounts would be in the range of 20 dB to 30 dB at one half the clock frequency with appropriate receiver equalization. Receivers designed to work with lesser signal attenuation are acceptable.

### 2 Normative references

The following standards contain provisions which, through reference in this text, constitute provisions of this standard. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent edition of the standards indicated below.

ANSI/SMPTE 125M-1995, Television — Component Video Signal 4:2:2— Bit-Parallel Digital Interface

ANSI/SMPTE 244M-1995, Television — System M/NTSC Composite Video Signals — Bit-Parallel Digital Interface

ANSI/SMPTE 267M-1995, Television — Bit-Parallel Digital Interface — Component Video Signal 4:2:2  $16 \times 9$  Aspect Ratio

ANSI/SMPTE 291M-1996, Television — Ancillary Data Packet and Space Formatting

SMPTE RP 165-1994, Error Detection Checkwords and Status Flags for Use in Bit-Serial Digital Interfaces for Television

SMPTE RP 184-1996, Specification of Jitter in Bit-Serial Digital Systems

IEC 1179 (1993), Helical-Scan Digital Composite Video Cassette Recording System Using 19 mm Magnetic Tape, Format D2 (NTSC, PAL, PAL-M), Section 5, Video Interface

ITU-R BT.601-5, Studio Encoding Parameters of Digital Television for Standard 4:3 and Wide-Screen 16:9 Aspect Ratios

### 3 Signal levels and specifications

The specifications in this clause are defined for measurement of the serial output of a source derived from a parallel domain signal whose timing and other characteristics meet good studio practices. Specifications at the output of equipment located at other places in an all-serial digital chain are not addressed by this standard. Clock frequency is the serial clock and is equal to the bit rate for each television system.

**3.1** The output of the generator shall be measured across a 75-ohm resistive load connected through a short coaxial cable. Figure 1 depicts the measurement dimensions for amplitude, risetime, and overshoot (see annex A for the preferred measurement method for these parameters).

**3.1.1** The generator shall have an unbalanced output circuit with a source impedance of 75 ohms and a return loss of at least 15 dB over a frequency range of 5 MHz to the clock

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frequency of the signal being transmitted (NTSC, PAL, or 4:2:2).

**3.1.2** The peak-to-peak signal amplitude shall be  $800 \text{ mV} \pm 10\%$ .

**3.2** The dc offset, as defined by the mid-amplitude point of the signal, shall be nominally  $0.0 \text{ V} \pm 0.5 \text{ V}$ .

**3.3** The rise and fall times, determined between the 20% and 80% amplitude points, shall be no less than 0.4 ns, no greater than 1.50 ns, and shall not differ by more than 0.5 ns.

**3.4** Overshoot of the rising and falling edges of the waveform shall not exceed 10% of the amplitude.

**3.5** The jitter in the timing of the transitions of the data signal shall be measured in accordance with SMPTE RP 184. Measurement parameters are defined in SMPTE RP 184 and shall have the following values for compliance with this standard:

Timing jitter lower band edge	10 Hz	B1
Alignment jitter lower band edge	1 kHz	B2
Upper band edge	>1/10 clock rate	B3
Timing jitter (note 1)	0.2 UI p-p	A1
Alignment jitter (UI = unit interval)	0.2 UI p-p	A2
Color bar test signal (note 2)	EG 1	
Serial clock divider (note 3)	$\neq 10$	n

#### NOTES

1 Designers are cautioned that the clock in parallel signals conforming to interconnection standards, such as ANSI/SMPTE 125M, may contain jitter up to 6 ns p-p. Deriving the serial signal directly from the unfiltered parallel clock could result in excessive serial signal jitter (see annex B for further information on timing jitter).

2 Color bars are chosen as a nonstressing test signal for jitter measurements. (Similar color bar signals should be used for 625-line systems.) Use of a stressing signal with long runs of zeros may give misleading results.

3 Use of a serial clock divider value of 10 is acceptable; however, it may mask word-correlated jitter components. The divider value should be stated in conjunction with jitter specifications.

**3.6** The input to the serial receiver signal shall present an impedance of 75 ohms with a return loss of at least 15 dB over a frequency range of 5 MHz to the clock frequency of the signal being transmitted.

## 4 Connector and cable types

**4.1** The connector shall have mechanical characteristics conforming to the 50-ohm BNC type. Mechanical dimensions of the connector may produce either a nominal 50-ohm or nominal 75-ohm impedance and shall be usable at frequencies up to 850 MHz. However, the electrical characteristics of the connector and its associated interface circuitry shall provide a resistive impedance of 75 ohms. Where a 75-ohm connector is used, its mechanical characteristics must reliably interface with the nominal 50-ohm BNC type defined by IEC 169-8.

**4.2** Application of this standard does not require a particular type of coax. It is necessary for the frequency response of the coax loss, in decibels, to be approximately proportional to  $1/\sqrt{f}$  from 1 MHz to the clock frequency of the signal being transmitted to ensure correct operation of automatic cable equalizers over moderate to maximum lengths.

## 5 Channel coding

**5.1** The channel coding shall be scrambled NRZI.

**5.2** The generator polynomial for the scrambled NRZ shall be  $G_1(X) = X^9 + X^4 + 1$ . The polarity-free scrambled NRZI sequence shall be produced by  $G_2(X) = X + 1$ . The input signal to the scrambler shall be positive logic (the highest voltage represents data 1 and the lowest voltage data 0 [see annex C]).

**5.3** Data word length shall be 10 bits.

NOTE – Because some parallel interfaces may carry only 8 bits of data, values in the range  $3FC_h$  to  $3FF_h$  must be treated as equivalent to  $3FF_h$  for the purpose of detecting

ancillary data flags or other identifying flags using those values.

## 6 Transmission order

The LSB of any data word shall be transmitted first.

## 7 Component 4:2:2 signals

**7.1** The input source for generating a serial 4:2:2 data stream shall be as defined by ANSI/SMPTE 125M, ANSI/SMPTE 267M, or ITU-R BT.601.

**7.1.1** Because some parallel component digital interfaces may carry only 8 bits of video data, it is necessary for the data serializer to identify this condition and to add the necessary data to convert the 8-bit signal to a 10-bit representation. EAV and SAV of the 8-bit signals should be converted in the following manner:

<u>8 bit</u>	<u>10 bit</u>
FF	3FF
00	000
00	000
PQ	XYZ (= PQ data left shifted twice with subordinate bits set to zero)

**7.2** The bit rate for the resulting serial data stream shall be nominally 270 Mb/s for 13.5-MHz luminance sampled  $4 \times 3$  or  $16 \times 9$  aspect ratio pictures and 360 Mb/s for 18-MHz luminance sampled  $16 \times 9$  aspect ratio pictures.

**7.3** Ancillary data space is reserved for error detection data formatted per SMPTE RP 165 as follows:

<u>Standard</u>	<u>Lines</u>	<u>Words</u>
525 13.5-MHz sampling	9, 272	1689 - 1711
525 18-MHz sampling	9, 272	2261 - 2283
625 13.5-MHz sampling	5, 318	Y850 - Y861
625 18-MHz sampling	5, 318	Y1138 - Y1149

**7.4** Ancillary data, if present on the parallel interface, shall be passed transparently except for data specified in 7.3.

## 8 Composite NTSC $4f_{sc}$ signals

### 8.1 Input source

The input source for generating a serial  $4f_{sc}$  composite data stream shall be ANSI/SMPTE 244M.

**8.1.1** Because some ANSI/SMPTE 244M interfaces may carry only 8 bits of video data, it is necessary for the data serializer to identify this condition and to add the necessary data to convert the 8-bit signal to a 10-bit representation.

### 8.2 Bit rate

The bit rate for the resulting data stream shall be nominally 143 Mb/s.

### 8.3 Signal processing

Signal processing of the input signal is necessary to provide timing and synchronizing information in the serial digital domain. This information is designated TRS-ID, timing reference signal and line number identification.

**8.3.1** The TRS and line number ID shall be present only following the sync leading edge which identifies a horizontal rate transition.

**8.3.2** The TRS signal shall consist of four words located at word number addresses 790, 791, 792, 793. Corresponding word values are 3FF, 000, 000, 000.

**8.3.3** Line number ID shall be one word. The line number word-number address shall be 794 with the following values:

<u>b2</u>	<u>b1</u>	<u>b0</u>		
0	0	0	Line 1 - 263	Field 1
0	0	1	Line 264 - 525	Field 2
0	1	0	Line 1 - 263	Field 3
0	1	1	Line 264 - 525	Field 4
<u>b7</u>	<u>b6</u>	<u>b5</u>	<u>b4</u>	<u>b3</u>
(MSB)				(LSB)

The possible values of X1 are restricted by the use of 5 bits and indicate the following:

X1 = 0 Not used.

$1 \leq X1 \leq 30$  X1 indicates the line number of each field (lines 1 - 30 in odd fields, lines 264 - 293 in even fields).

X1 = 31 To indicate line number 31 and up of each odd field and line number 294 and up on each even field.

$X1 = 16(b7) + 8(b6) + 4(b5) + 2(b4) + 1(b3)$ .

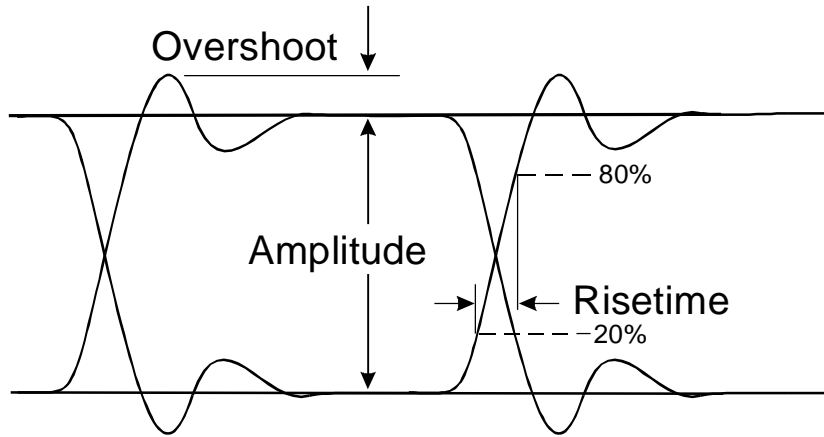
b8 is even parity for b7 through b0.

$b9 = \overline{b8}$ .

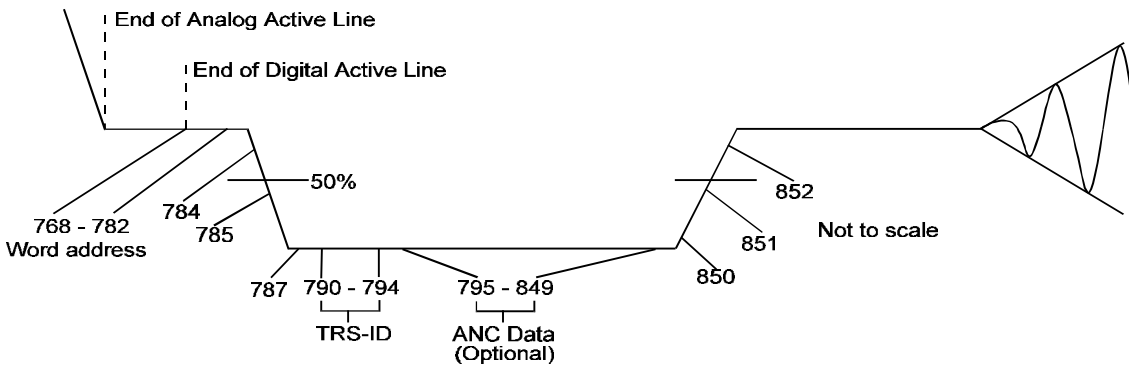
**8.4 Ancillary data**

Ancillary data may be present within the following word number boundaries (see figures 2, 3, and 4):

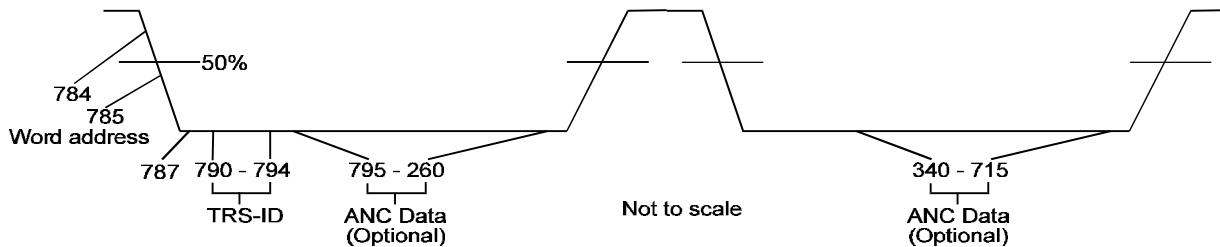
- 795 - 849 for horizontal sync period
- 795 - 815 for equalizing pulse period
- 340 - 360
- 795 - 260 for vertical sync period
- 340 - 715



**Figure 1 - Waveform measurement dimensions**



**Figure 2 - NTSC composite digital horizontal sync period details**



**Figure 3 - NTSC vertical sync details**

**8.4.1** The first word in an ancillary data packet shall be the ANC data flag and shall have the value 3FC (see 5.3 regarding 8- to 10-bit conversion).

**8.4.2** There may be multiple ANC data flags in the allocated ancillary data space. Each ANC data flag shall identify the beginning of another data block.

**8.4.3** Ancillary data blocks shall be formatted as defined in ANSI/SMPTE 291M.

**8.4.4** Ancillary data space at word address 795 - 815 on lines 9 and 272 is reserved for error detection data formatted per SMPTE RP 165.

## 9 Composite PAL $4f_{sc}$ signals

### 9.1 Input source

The input source for generating a serial  $4f_{sc}$  composite data stream shall be IEC 1179.

**9.1.1** Because some IEC 1179 interfaces may carry only 8 bits of video data, it is necessary for the data serializer to identify this condition and to add the necessary data to convert the 8-bit signal to a 10-bit representation.

### 9.2 Bit rate

The bit rate for the resulting serial data stream shall be nominally 177.3 Mb/s.

### 9.3 Signal processing

Signal processing of the input signal is necessary to provide timing and synchronizing information in the serial digital domain. This information is designated TRS-ID, timing reference signal and line number identification.

**9.3.1** The TRS and line number ID shall be present only following the sync leading edge which identifies a horizontal rate transition.

**9.3.2** The TRS signal shall consist of four words located at word number addresses 967, 968, 969, 970. Corresponding word values are 3FF, 000, 000, 000.

**9.3.3** Reset of the TRS position relative to the H-sync edge shall take place once per field on only one of lines 625 - 4 and one of lines 313 - 317. Reset is necessary due to the non-integer number of samples per line. Therefore, from a sample numbering standpoint, all lines will have 1135 samples except the two lines used for reset which will have 1137 samples. The additional samples will be numbers 1135 and 1136 just prior to the first active picture sample 000. This does not affect the continuous signal concept where all but two lines in a field have 1135 samples and the other two have 1136. (The line numbers with 1136 samples are a function of  $S_cH$  phase and the criteria for determining which samples fall in which lines.)

Designers should note that sample locations in figures 4, 5, and 6 represent the first line following the above-mentioned reset. Subsequent nearby low-line numbers will be similar, but the samples are slightly earlier on each line due to the noninteger number of samples per line. Initial determination of the position of TRS should, therefore, be done on the line following sample numbering reset or a nearby subsequent line.

Considering the 0  $S_cH$  phase requirement of IEC 1179 and the sample numbering system described above, the TRS location is known and starts exactly with sample 967 on each line, but its time from the leading edge of sync varies due to the noninteger number of samples per line.

**9.3.4** Line number ID shall be one word. The line number word-number address shall be 971 with the following values:

<u>b2</u>	<u>b1</u>	<u>b0</u>		
0	0	0	Line 1 - 313	Field 1
0	0	1	Line 314 - 625	Field 2
0	1	0	Line 1 - 313	Field 3
0	1	1	Line 314 - 625	Field 4
1	0	0	Line 1 - 313	Field 5
1	0	1	Line 314 - 625	Field 6
1	1	0	Line 1 - 313	Field 7
1	1	1	Line 314 - 625	Field 8
<u>b7</u>	<u>b6</u>	<u>b5</u>	<u>b4</u>	<u>b3</u>
(MSB)				(LSB)

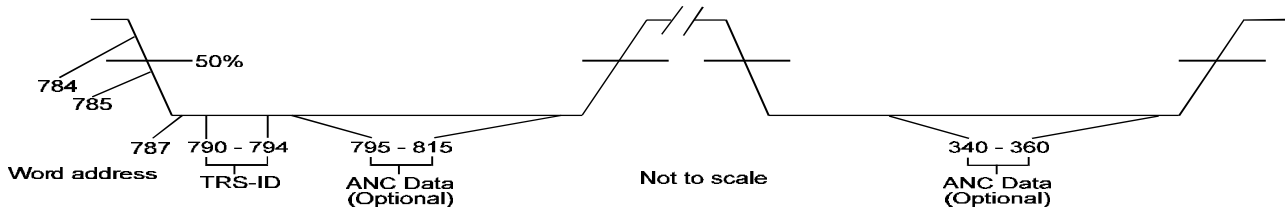


Figure 4 – NTSC equalizing pulse details

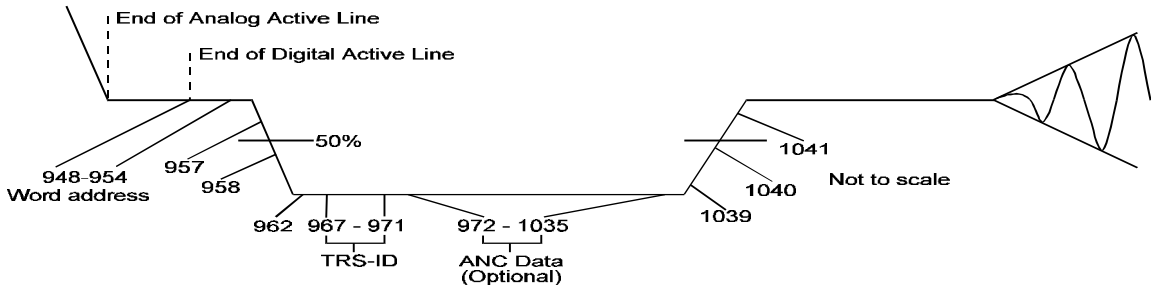


Figure 5 – PAL composite digital horizontal sync period details

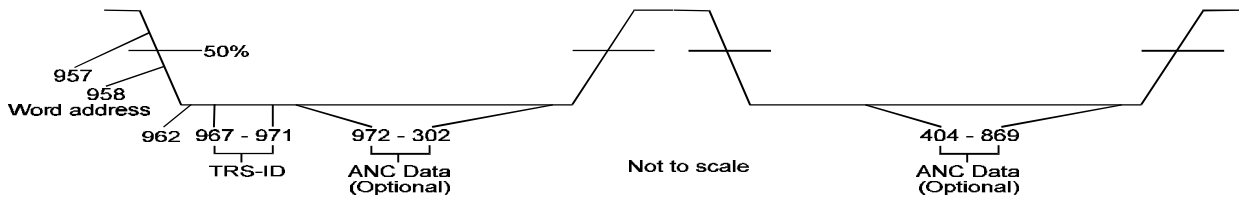


Figure 6 – PAL vertical sync details

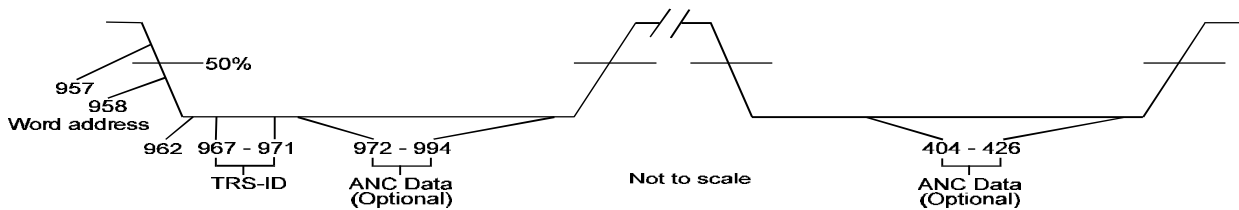


Figure 7 – PAL equalizing pulse details

The possible values of X1 are restricted by the use of 5 bits and indicate the following:

X1 = 0	Not used.
$1 \leq X1 \leq 30$	X1 indicates the line number of each field (lines 1 - 30 in odd fields, lines 314 - 343 in even fields).
X1 = 31	To indicate line number 31 and up of each odd field and line number 344 and up on each even field.
X1 = 16 (b7) + 8 (b6) + 4 (b5) + 2 (b4) + 1 (b3).	
b8 is even parity for b7 through b0.	
b9 = $\overline{\text{b8}}$ .	

#### 9.4 Ancillary data

Ancillary data may be present within the following word number boundaries (see figures 5, 6, and 7):

972 - 1035	for horizontal sync period
972 - 994 404 - 426	for equalizing pulse period
972 - 302 404 - 869	for vertical sync period

**9.4.1** The first word in an ancillary data packet shall be the ANC data flag and shall have the value 3FC (see 5.3 regarding 8- to 10-bit conversion).

**9.4.2** There may be multiple ANC data flags in the allocated ancillary data space. Each ANC data flag shall identify the beginning of another data block.

#### Annex A (informative) Waveform measurement method

The preferred method for measuring serial digital waveform amplitude, risetime, and overshoot is using a 1-GHz bandwidth oscilloscope. Input impedance of the oscilloscope should be 75 ohms with a return loss greater than 20 dB to

#### Annex B (informative) Timing jitter specification

Low-frequency jitter in the range of 10 Hz to 1 kHz is indicated by the difference between timing jitter (A1) and alignment jitter (A2) measurements. Although purely digital systems will operate correctly with significant amounts of low-frequency jitter, this standard (3.5) specifies a tight

**9.4.3** Ancillary data blocks shall be formatted as defined in ANSI/SMPTE 291M.

**9.4.4** Ancillary data space at word address 972 - 992 on lines 5 and 318 is reserved for error detection data formatted per SMPTE RP 165.

### 10 Levels of operation

To define the level of support for this standard by each type of equipment, one or more suffix letters are added to the standard number.

#### 10.1 Default compliance

Default compliance is defined as operation at all levels.

#### 10.2 Support levels

Level A – 143 Mb/s, NTSC  
Level B – 177 Mb/s, PAL  
Level C – 270 Mb/s, 525/625 component  
Level D – 360 Mb/s, 525/625 component

#### 10.3 Examples of compliance nomenclature

A D-2 VTR accepting only composite digital NTSC would be said to conform to ANSI/SMPTE 259M-A.

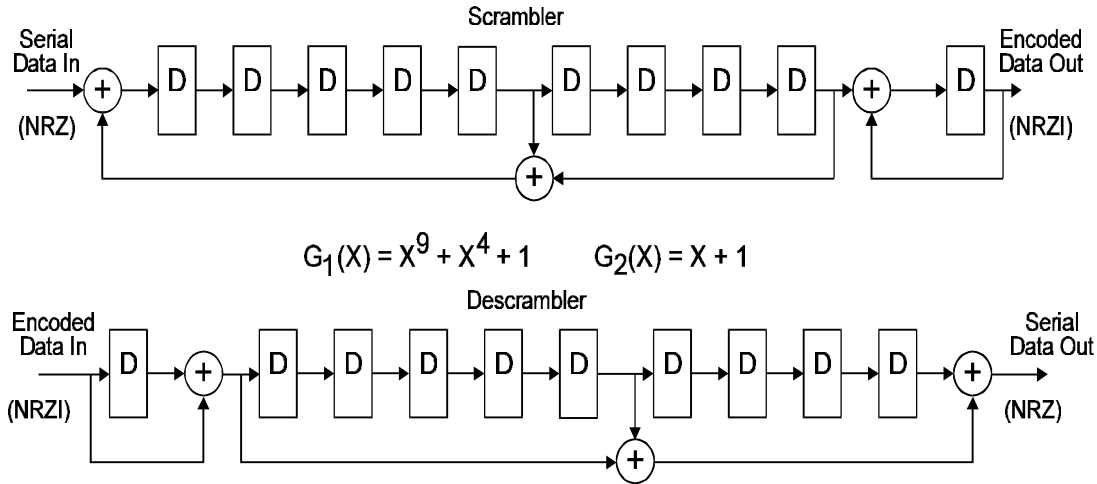
A multistandard routing switcher with a maximum bit rate of 270 Mb/s would be said to conform to ANSI/SMPTE 259M-ABC.

400 MHz. Measurements should be made using a 2-m length of coax between the transmitter and oscilloscope with no more than 0.15 dB/m loss at 135 MHz.

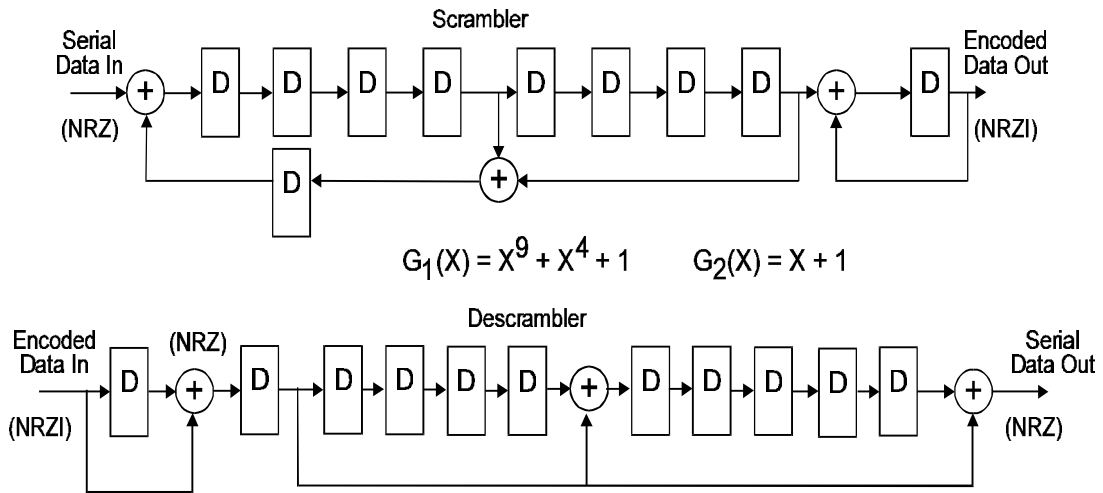
tolerance for timing jitter to ensure operation in mixed digital/analog systems. Methods do exist for handling larger amounts of low-frequency jitter in such systems; therefore, SMPTE engineering committees are continuing to evaluate the preferred value for the A1 specification.

**Annex C (informative)**  
**Generator polynomial implementations**

Possible generator polynomial implementations are given in figures C.1 and C.2.



**Figure C.1 – Possible generator polynomial – Method 1**



**Figure C.2 – Possible generator polynomial – Method 2**

**Annex D (informative)**  
**Bibliography**

ANSI/SMPTE 170M-1994, Television — Composite Analog Video Signal — NTSC for Studio Applications

SMPTE EG 1-1990, Alignment Color Bar Test Signal for Television Picture Monitors

SMPTE RP 192-1996, Jitter Measurement Procedures in Bit-Serial Digital Interfaces

IEC 169-8 (1978), Part 8: R.F. Coaxial Connectors with Inner Diameter of Outer Conductor 6.5 mm (0.256 in) with Bayonet Lock — Characteristic Impedance 50 Ohms (Type BNC), Appendix A (1993), and Amendment No. 1 (1996)

ITU-R BT.470-4, Television Systems