Icarus Verilog and Free/Open Source EDA Tools

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25/02/2006

Preamble

- Not a professional EDA Developer, a hobbyist.
- Professionally a Embedded Software Engineer.
- Less emphasis on technical details of VLSI
- More focus on Icarus Verilog Features and other 'Free' EDA Tools available.
- Contributions to the Free Software World and relevance to students.
- Possible additions and references will be given.

EDA - An Introduction

- Electronic design Automation - Category of tools for designing and producing electronic systems ranging from printed circuit boards (PCBs) to integrated circuits.

- Unlike the mainstream computer applications segment ,the EDA segment has been ,least to say disappointing when it comes to Free and Open Source[FOSS] tools. (Reasons are many)

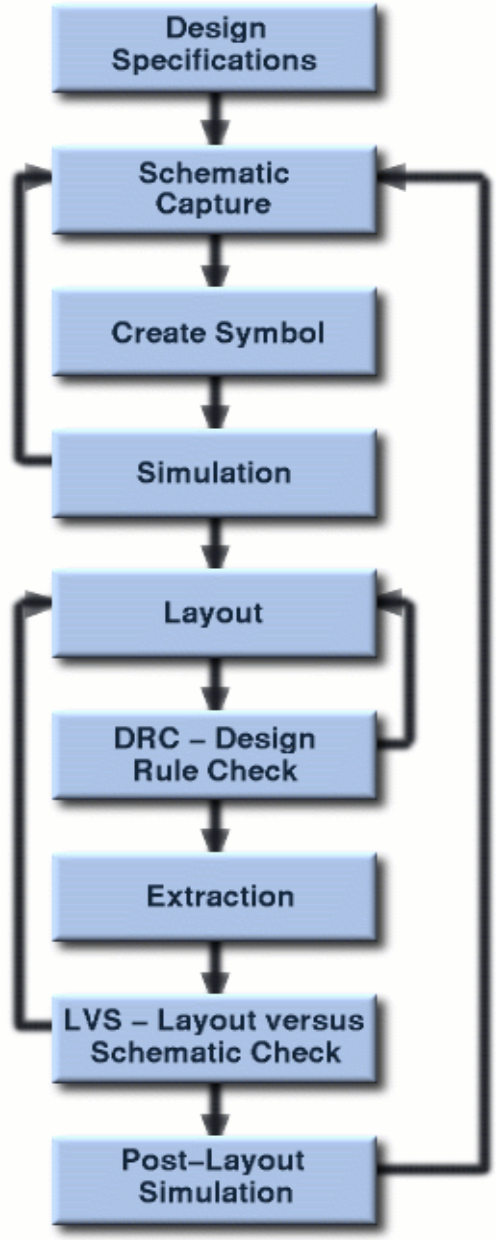
- The 'Free' EDA is now gaining significant attention because of super high pricing of commercial software.

VLSI Design Flows – An Introduction

- VLSI --> Contains millions gates --> Hundreds of Millions of transistors
- **Very-large-scale integration (VLSI)** of systems of transistor-based circuits into integrated circuits on a single chip first occurred in the 1980s as part of the semiconductor and communication technologies that were being developed.

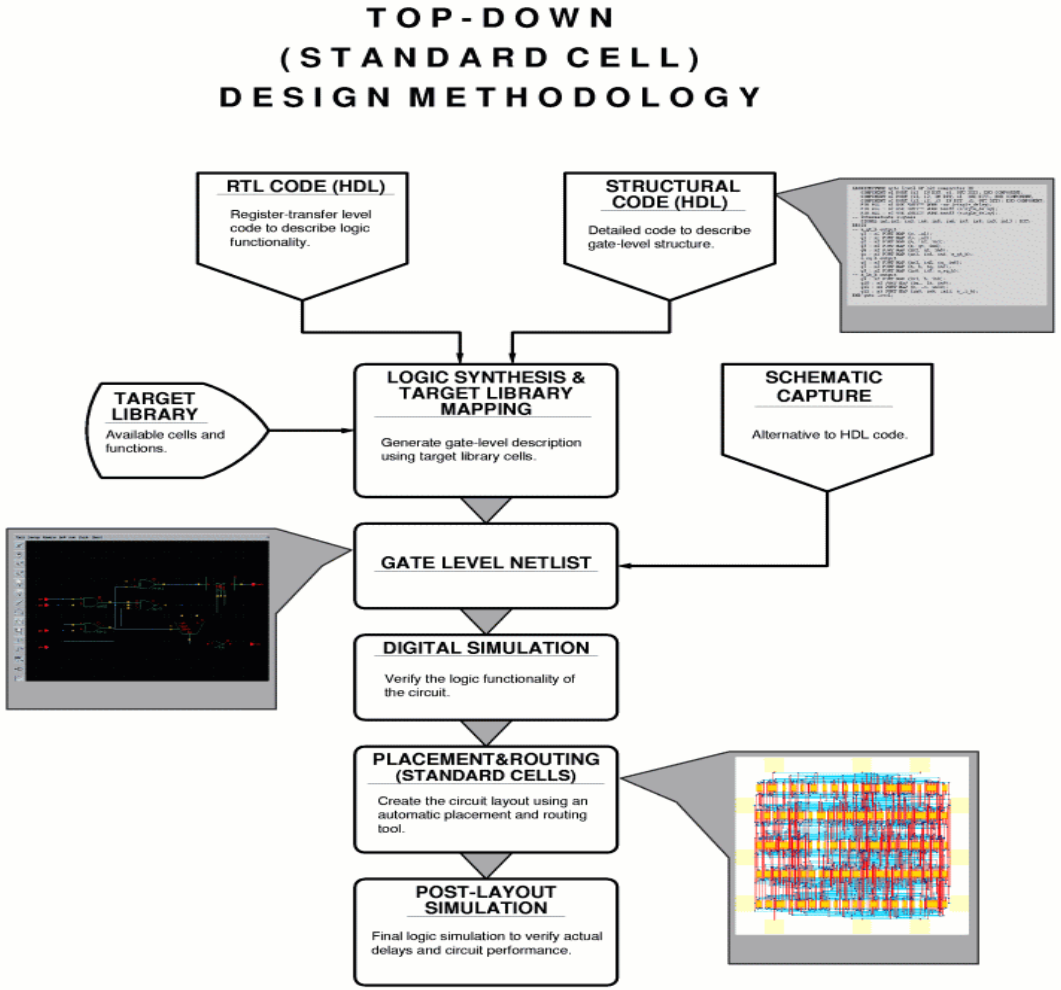
  - **Top Down Design [Semi Custom Flow]**
  - **Bottom Up Design [Full Custom Flow]**

Bottom Up Design Flow



- The bottom-up design methodology is based on (mainly) manual construction of circuit building blocks at the transistor and mask-layout level
- Flexibility at lower level design issues such as transistor size optimization and parasitics minimization.
- Better suited for the design of very dense, high-performance digital modules as well as analog and mixed-signal integrated circuits.

Top Down Design Flow



Icarus Verilog – Technical Details

- A Command line Verilog simulation and synthesis tool
- A Compiler, compiling source code written in Verilog (IEEE-1364) into some target format.
- The currently supported targets are vvp for simulation, and xnf and fpga for synthesis
- Selection of the Verilog language generation to support in the compiler. Selects between IEEE1364-1995(1), IEEE1364-2001(2). Increases compatibility with other tools down the chain.
- The Icarus Verilog compiler supports module libraries as directories that contain Verilog source files.
- Main porting target is Linux, although it works well on many similar operating systems such as Windows, MacOS.

Icarus Verilog – PLI Support

- Verilog PLI(Programming Language Interface) is a mechanism to invoke C or C++ functions from Verilog code.
- Function Invoked --> System Call [Eg. $monitor, $display]
- Capabilities of Verilog PLI
  - *Not possible using Verilog Syntax*
  - *Custom Output Displays*
  - *Access to Simulation Data Structure*
  - *Simulation Analysis*
  - *lots more.....*
- Icarus Verilog supports PLI 2.0 [aka VPI – Verilog Procedural Interface]
  - just for info [CVER supports PLI 1.0]

Icarus Verilog – Admin and Licensing

- Administrative
  - Current Stable release is v0.8
  - ftp://ftp.icarus.com/pub/eda/verilog/v0.8
  - Development Snapshots available for Download and are made almost weekly [ftp://icarus.com/pub/eda/verilog/snapshots]
- Licensing
  - The compiler itself is released under GNU GPL
  - Free to distribute. Info regarding GPL license available at http://www.gnu.org/copyleft/gpl.html

gEDA – GPL'd Electronic Design Automation

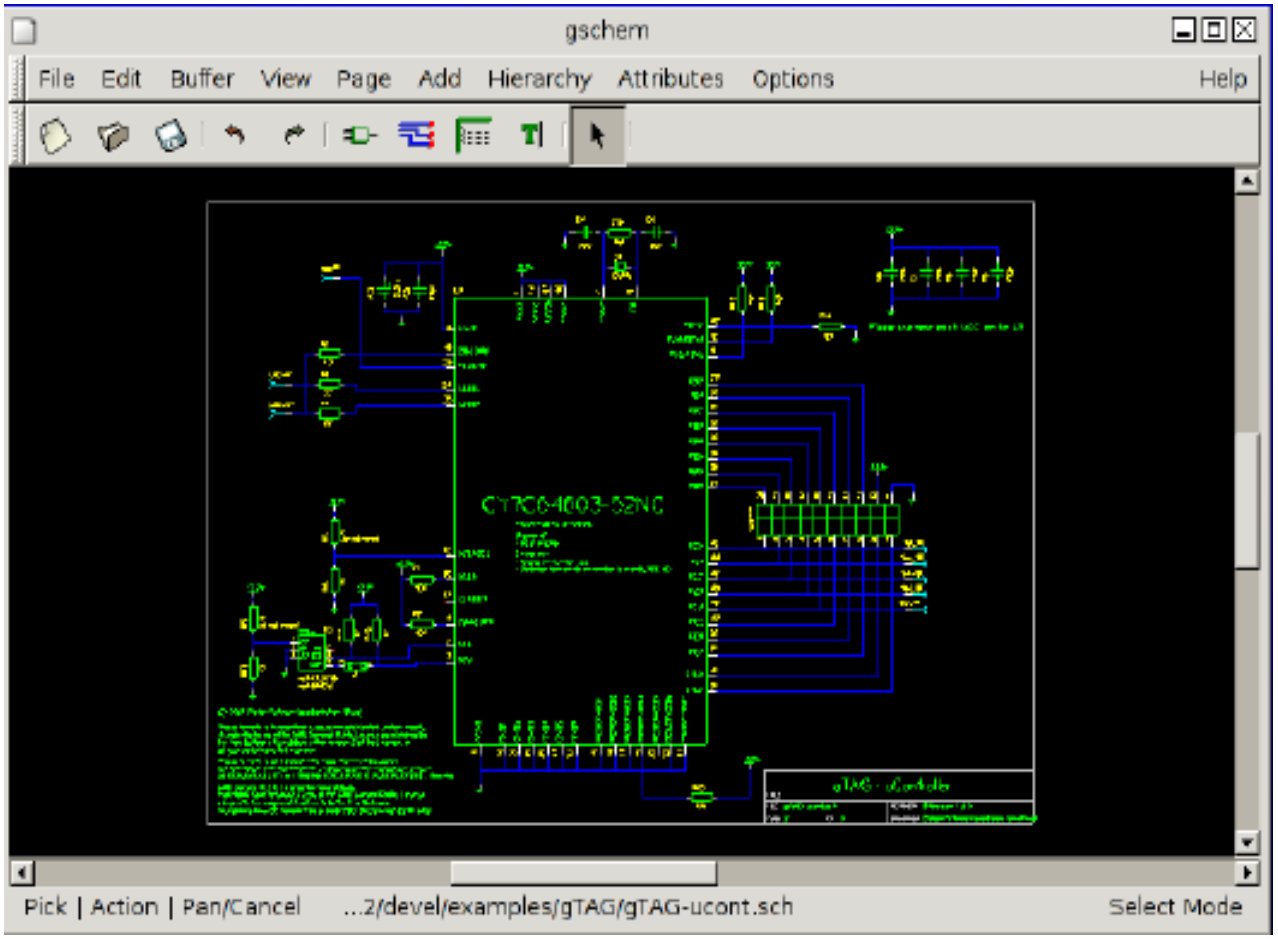
- GPL'd tools for EDA design
- A Free Software project
- Website: http://geda.seul.org
- Consists of about 10 sub-projects
- Low to Middle level complexity Ckt Design
- Tool flow from Schematic to PCB layout
- Favourite users
  - Ronja and Open Automation Project

gEDA – Continued... [why ??]

- Free to distribute, copy.
- An Open Development LifeCycle
- MultiPlatform Support
- Legacy design Support
- Open and Documented File Formats

gEDA Tools – Schematic Capture

- gSchem - facilitates the graphical input of components/circuits.



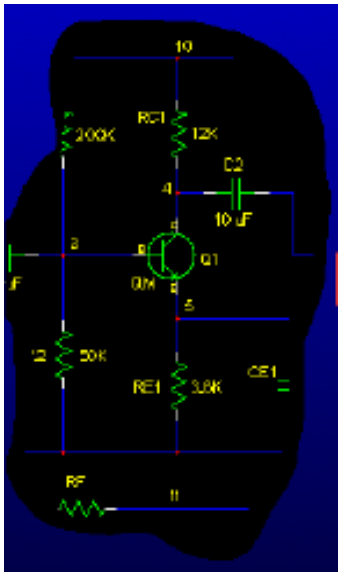
gEDA Tools – Schematic Capture

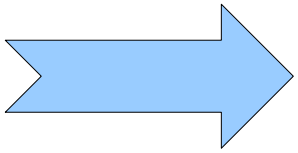
- Features of gSchem
  - Electrical Connectivity Awareness
  - Generate netlists
  - Hierarchial Design
- gschem does not do
  - DRC [Design Rule Check]
  - A more flexible component library

Visit http://www.geda.seul.org/tools/gschem/index.html

gEDA – Netlist Creator

- gNetList – A graphical to Textual converter :)
  - Supported Netlist formats can be obtained from http://www.geda.seul.org/tools/gnetlist/index.html





```
**************************
* Spice file generated b
* spice-sdb version 12.2
* provides advanced spic
* Documentation at http:
**************************
VCC 10 0 DC 15V
RL 9 0 10K
C3 7 9 10 uF
RF 2 11 25K
CF 11 8 10 uF
RC2 10 7 6.8K
RE2 8 0 3.6K
C2 4 6 10 uF
R4 6 0 30K
RE1 5 0 3.6K
RS 12 2 150
C1 2 3 10 uF
R2 3 0 50K
R1 10 3 200K
```

gEDA – Other Tools

- GTKWave
  - GTKWave is VCD/EVCD/LXT/Synopsis .out format electronic waveform viewer
  - Website: http://www.cs.man.ac.uk/apt/tools/gtkwave/index.html
- ngSpice
  - Mixed-signal circuit simulator based on three open source software packages: Spice3f5, Cider1b1 and Xspice.
- PCB
  - interactive printed circuit board editor for the X11 window system
  - offers high end features such as an autorouter and trace optimizer which can tremendously reduce layout time
  - Website: http://pcb.sourceforge.net/

Other Useful 'Free' Tools

- MAGIC http://opencircuitdesign.com/magic/
- Electric
- FreeHDL
- Lots more....

What does FOSS have for me??

- 'Free' EDA tools help to understand how industry grade EDA tools work as they use similar algorithms.
- 'Free' EDA tools can be used by people who want to learn but do not have access to tools
- Open standards will aid tool interoperability.
- If you feel a lack of a particular feature implement it and get recognised globally :)

References & useful Links

- http://www.icarus.com
- http://www.eda.org
- http://ronja.twibright.com
- http://www.asic-world.com
- http://www.tuxmaniac.com [:)]
- http://www.opencores.org
- http://www.opencollector.org